SY2A22404

High-Efficiency, Fast-Response, 3.5A, 40V Input Synchronous Step-Down Regulator

General Description

The SY2A22404 high-efficiency synchronous step-down DC-DC converter operates over a wide input voltage range (4.2V to 40V) and can deliver 3.5A load current. The device integrates the main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize conduction loss.

The SY2A22404 employs a peak-current-mode control strategy with a constant switching frequency that is adjustable from 300kHz to 2.2MHz using an external resistor. When the internal clock becomes active, the top FET switches on. When the top FET current-sense signal reaches internal V_{COMP}, the top FET switches off and the bottom FET switches on. The internal clock frequency is programmable using the external resistor R_{FS}.

The device operates with low quiescent current (18µA typical) to achieve high efficiency under light load, and it features an internal soft-start to limit inrush current during power-on.

The SY2A22404 is available in a compact 8-pin SO8E package.

Features

- 4.2–40V Input Voltage Range
- 3.5A Output Current Capability
- Low $R_{DS(ON)}$ for Internal Switches:115mΩ Top, 80mΩ Bottom
- 18µA Quiescent Current
- Internal Compensation
- Internal 1ms Soft-Start Limits Inrush Current
- Adjustable Switching Frequency Range: 300kHz to 2.2MHz
- ±2% 0.6V Reference over the -40°C to +125°C Temperature Range
- Cycle-by-Cycle Peak Current Limit
- Short-Circuit Protection
- Thermal Shutdown and Automatic Recovery
- RoHS-Compliant and Halogen-Free
- Compact SO8E Package
- Automotive AEC-Q100 Grade 1 Certified

Applications

- Automotive
- Industrial
- High-Voltage DC/DC Converters

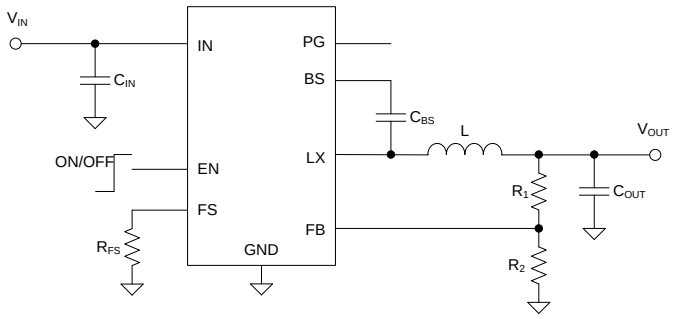


Figure 1. Typical Application Circuit

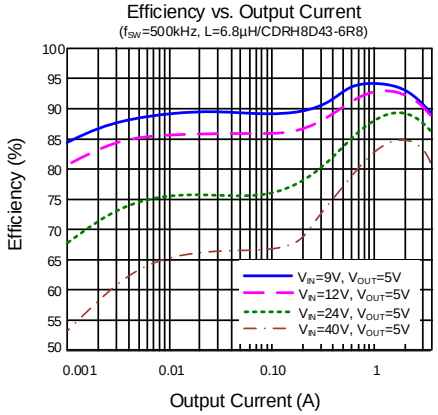


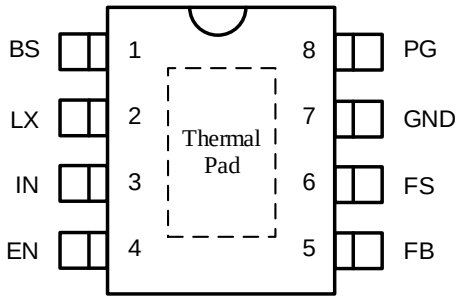
Figure 2. Efficiency vs. Load Current

Ordering Information

Ordering Part Number	Package type	Top Mark
SY2A22404FCA	SO8E RoHS-Compliant and Halogen-Free	**BTS*xyz***

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	BS	Bootstrap pin. Supply high-side gate driver. Connect a 0.1µF ceramic capacitor between the BS and the LX pin.
2	LX	Inductor pin. Connect this pin to the switching node of the inductor.
3	IN	Input pin. Decouple this pin from the GND pin with a minimum 4.7µF ceramic capacitor.
4	EN	Enable control. Pull high to turn on. Do not leave floating.
5	FB	Output feedback pin. Connect this pin to the center point of the output resistor-divider to program the output voltage: $V_{OUT} = 0.6 \times (1 + R1/R2)$.
6	FS	Frequency-setting pin. Connect a resistor from this pin to GND to program the switching frequency. Switching frequency: $f_{SW}(kHz) = 10^6/(9.3 \times R_{FS}(k\Omega) + 30)$
7	GND	Ground
8	PG	Power-good indicator. Open-drain output. Externally pulled high when V_{OUT} is within regulation range; otherwise internally pulled low.
–	Thermal Pad	GND pin must be electrically connected to the exposed pad on the printed circuit board for proper operation.

Block Diagram

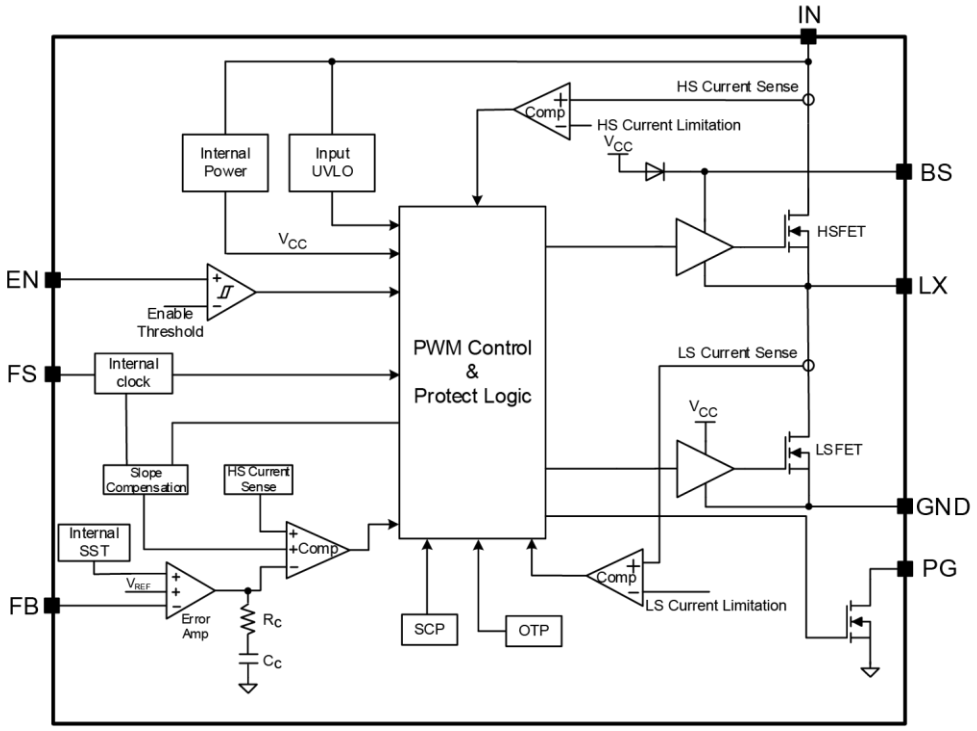


Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN	-0.3	44	V
LX, FB, EN, FS, PG	-0.3	44	
BS-LX	-0.3	4	
Dynamic LX Voltage in 20ns Duration (3)	GND -	IN + 3	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering,10s)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Min	Max	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance		40	°C/W
θ_{JC} Junction-to-Case Thermal Resistance		12	
P_D Power Dissipation T_A= 25°C		2.5	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN	4.2	40	V
Junction Temperature	-40	125	°C
Ambient Temperature	-40	125	

Electrical Characteristics

(V_{IN} = 12V, T_J = -40°C to +125°C. Typical values are at T_J = 25°C, unless otherwise specified

Parameter (Note 4)		Symbol	Test Conditions	Min	Typ	Max	Unit
Input	Input Voltage Range	V_{IN}		4.2		40	V
	Input UVLO Threshold	V_{UVLO}		3.6	3.9	4.2	V
	UVLO Hysteresis	V_{HYS}			0.3		V
	Quiescent Current	I_Q	I_{OUT} = 0, V_{FB} = V_{REF} × 105%, T_J = 25°C	10	18	25	μA
			I_{OUT} = 0, V_{FB} = V_{REF} × 105%, T_J= -40°C–125°C	5	18	33	
	Shutdown Current	I_{SHDN}	EN = 0, T_J = 25°C			1	μA
			EN = 0, T_J = -40°C–125°C			5	
Output	Feedback Reference Voltage	V_{REF}	T_J = 25°C	0.594	0.6	0.606	V
			T_J = -40–125°C	0.588	0.6	0.612	V
	FB Input Current	I_{FB}	V_{FB} = 0.65V	-50		50	nA
	Output Discharge Current	I_{DIS}			45		mA
	Soft-Start Time	t_{SS}		0.5	1	2	ms
	Output Undervoltage Protection Threshold	V_{UVP}			33%		V_{REF}
	Hiccup Duty Cycle	D_{HICCUP}			12.5		%
Power Good	Power-Good Threshold	V_{PG}	V_{FB} falling, PG from high to low		89%		V_{REF}
			V_{FB} rising, PG from low to high		93%		V_{REF}
			V_{FB} rising, PG from high to low		115%		V_{REF}
			V_{FB} falling, PG from low to high		113%		V_{REF}
	Power-Good Delay	t_{PG_F}	PG falling edge		10		μs
		t_{PG_R}	PG rising edge		150		μs
	Power-Good Output Low Voltage	$V_{PG,LOW}$	I_{PG_LOW} = 10mA			0.7	V
MOSFET	Top FET R_{ON}	$R_{DS(ON)1}$		70	115	210	mΩ
	Bottom FET R_{ON}	$R_{DS(ON)2}$		45	80	135	mΩ
	Top FET Current Limit	$I_{LIM,TOP}$		4.4	5.5	6.6	A
Enable (EN)	EN High Threshold	V_{ENH}		1.08	1.2	1.32	V
	EN Low Threshold	V_{ENL}		0.9	1.0	1.1	V
Frequency	Oscillator Frequency Program Range	$f_{OSC,RNG}$	R_{FS} = 45.6k–360k	300		2200	kHz
	Oscillator Frequency Accuracy	$f_{OSC,ACC}$	f_{OSC} = 2MHz, with R_{FS} resistor of 1% accuracy	-12%		12%	f_{OSC}
	Min ON Time	$t_{ON,MIN}$			90		ns
	Min OFF Time	$t_{OFF,MIN}$	f_{OSC} = 2MHz		90		ns
OTP	Thermal Shutdown Temperature	T_{SD}			160		°C
	Thermal Shutdown Hysteresis	$T_{SD,HYS}$			20		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a two-layer Silergy demo board.

Note 3: The device is not guaranteed to function outside its operating conditions.

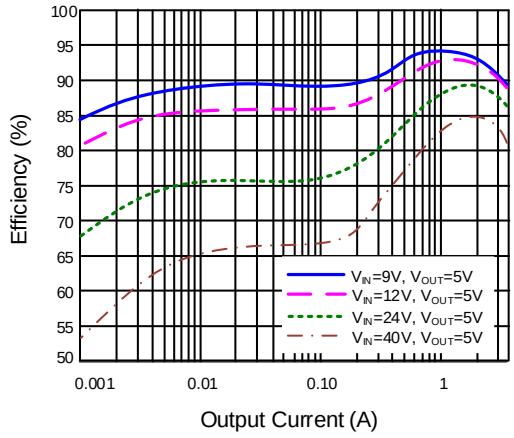
Note 4: The values are guaranteed by test design or statistical correlation. High junction temperatures degrade operating lifetime. Operating lifetime is derated for junction temperatures greater than 125°C.

Typical Performance Characteristics

(V_{IN} = 12V, C_{OUT} = 44µF, f_{SW} = 500kHz, T_A = 25°C unless otherwise specified)

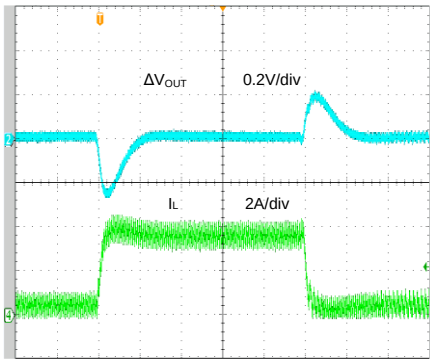
Efficiency vs. Output Current

(L=6.8µH/CDRH8D43-6R8)



Load Transient

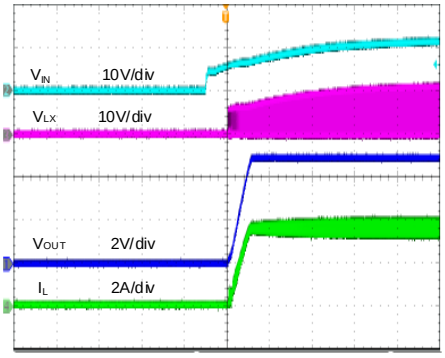
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0.35A ~ 3.5A)



Time (40µs/div)

Startup from V_{IN}

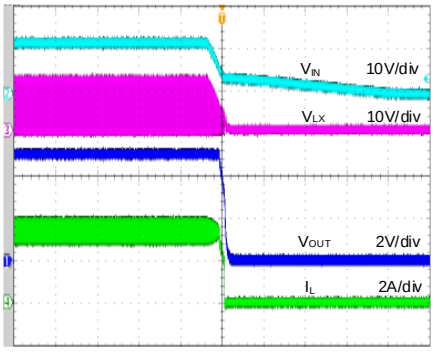
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3.5A)



Time (2ms/div)

Shutdown from V_{IN}

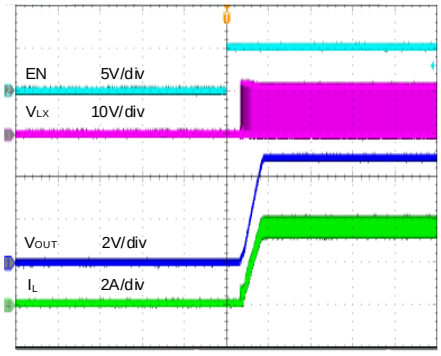
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3.5A)



Time (2ms/div)

Startup from Enable

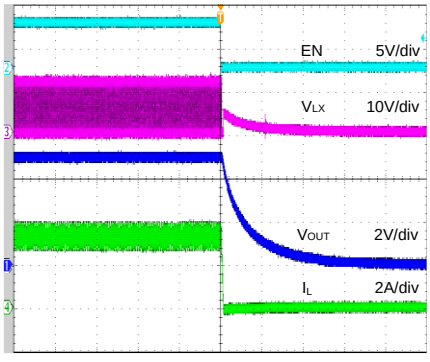
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3.5A)



Time (2ms/div)

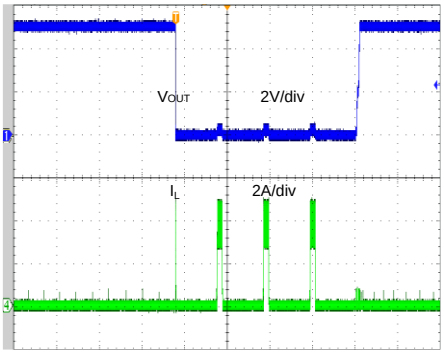
Shutdown from Enable

(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3.5A)



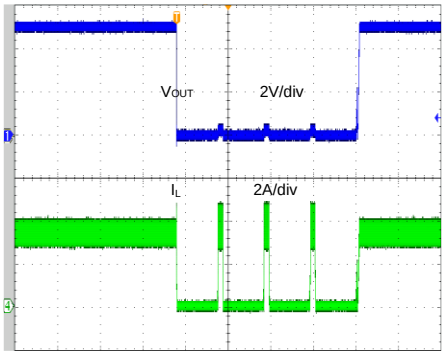
Time (100µs/div)

Short Circuit Protection
(V_{IN}=12V, V_{OUT}=5V, 0A to Short)



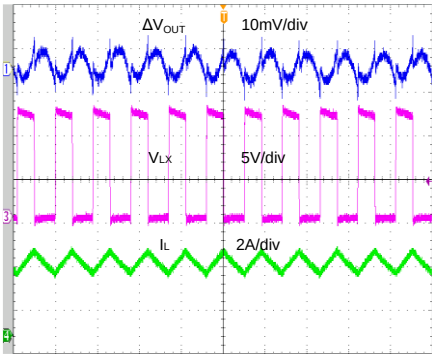
Time (20ms/div)

Short Circuit Protection
(V_{IN}=12V, V_{OUT}=5V, 3.5A to Short)



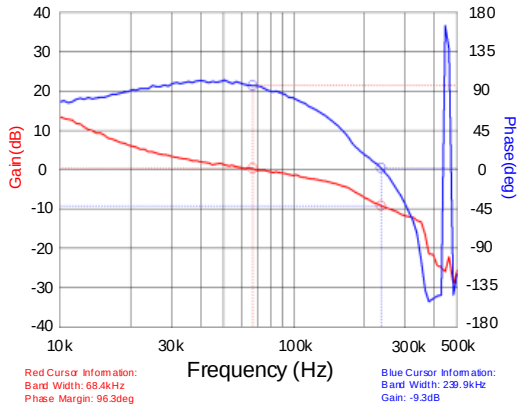
Time (20ms/div)

Output Ripple
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}= 3.5A)

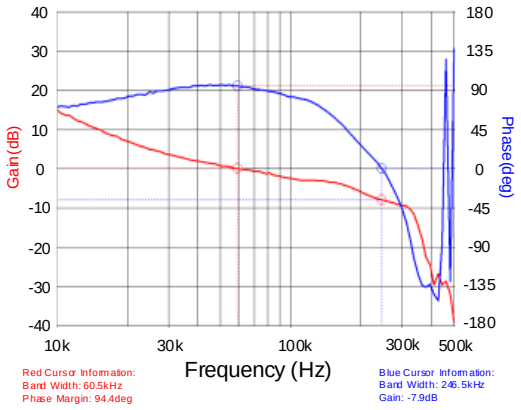


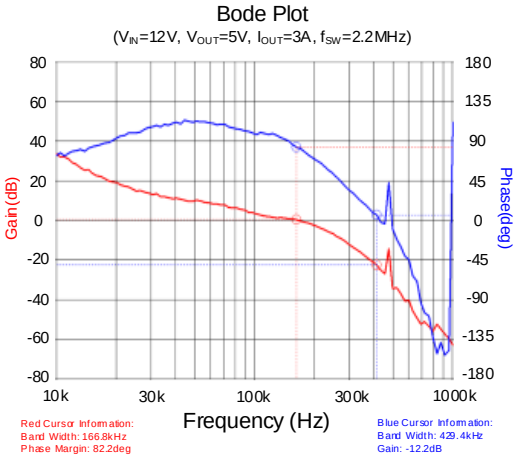
Time (2μs/div)

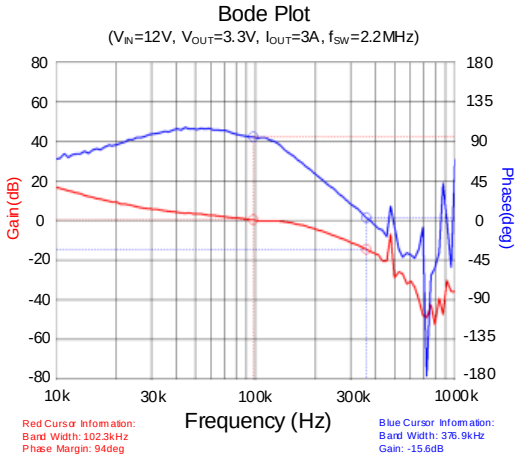
Bode Plot
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A, f_{SW}=500kHz)



Bode Plot
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=3A, f_{SW}=500kHz)







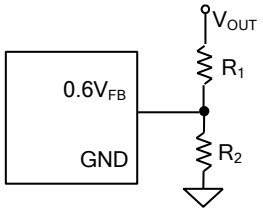
Detailed Description

The SY2A22404 is highly integrated, so only the following components need to be selected for the targeted application specifications: input capacitor C_{IN}, output capacitor C_{OUT}, output inductor L, and feedback resistor-dividers R1 and R2.

Feedback Resistor-Divider R1 and R2

Select R1 and R2 to program the proper output voltage. To minimize power consumption under light loads, select large resistance values for both R1 and R2. A value between 10kΩ and 1MΩ is highly recommended for both resistors. Given V_{OUT} = 3.3V and R1 = 100kΩ, then R2 can be calculated as 22.2kΩ using the following equation:

$$R2 = \frac{0.6V}{V_{OUT} - 0.6V} \times R1$$



With a calculated value of 22.2kΩ for R2, a standard 1% 22.1kΩ resistor is selected.

Input Capacitor C_{IN}

For the best performance, select a typical X5R or better grade ceramic capacitor with a 10V rating, and greater than 4.7μF capacitance. The capacitor should be placed as close as possible to the device, while also minimizing the loop area formed by C_{IN} and the IN/GND pins. When selecting an input capacitor, ensure that its voltage rating is at least 20% greater than the maximum voltage of the input supply. X5R or X7R dielectric types are the most often selected due to their small size, low cost, surge current capability, and high RMS current rating over a wide temperature and voltage range.

In situations where the input rail is supplied through long wires, it is recommended to add some bulk capacitance like electrolytic, tantalum or polymer type capacitors to reduce the overshoot and ringing caused by the added parasitic inductance.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is a voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1 - D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. A single 4.7μF X5R capacitor is sufficient in most applications.

Output Capacitor C_{OUT}

Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting the component. For the best performance, use an X5R or better grade ceramic capacitor with a 6.3V rating, and capacitance greater than 22μF.

For applications where the design must meet stringent ripple requirements, the following considerations must be followed:

The output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple). When calculating total ripple, both should be considered.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

The capacitive ripple might be higher because the effective capacitance for ceramic capacitors decreases with the voltage across the terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.

Output Inductor L

There are several considerations in choosing the output inductor:

1) It is suggested to choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \frac{V_{OUT}(1\text{-}V_{OUT}/V_{IN,MAX})}{f_{SW} \times I_{OUT,MAX} \times 0.4}$$

where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY2A22404 is highly tolerant of different ripple current amplitudes. Consequently, the final choice of inductance can differ slightly from the calculation value without significantly impacting performance.

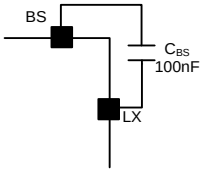
2) The selected saturation current rating of the inductor must be greater than the peak inductor current under full-load conditions:

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency. It is recommended to choose an inductor with DCR less than 50mΩ to achieve high overall efficiency.

External Bootstrap Capacitor

The external bootstrap capacitor provides the gate driver voltage for the internal high-side MOSFET. A 100nF low-ESR ceramic capacitor connected between the BS pin and the LX pin is recommended.



Switching Frequency Setting

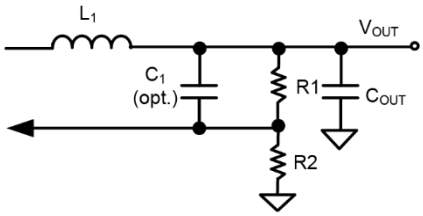
Connect a resistor from the FS pin to GND to adjust the switching frequency. The switching frequency is adjustable from 300kHz to 2.2MHz, as calculated by the following equation:

$$f_{SW}(\text{kHz}) = \frac{10^6}{9.3 \times R_{FS}(\text{k}\Omega) + 30}$$

where R_{FS} is in kΩ.

Load-Transient Considerations

The SY2A22404 integrates compensation components to achieve fast transient responses and improve stability. In some applications, adding a ceramic capacitor in parallel with R1 may further speed up the load-transient response. This is recommended for applications with large load-transient step requirements.



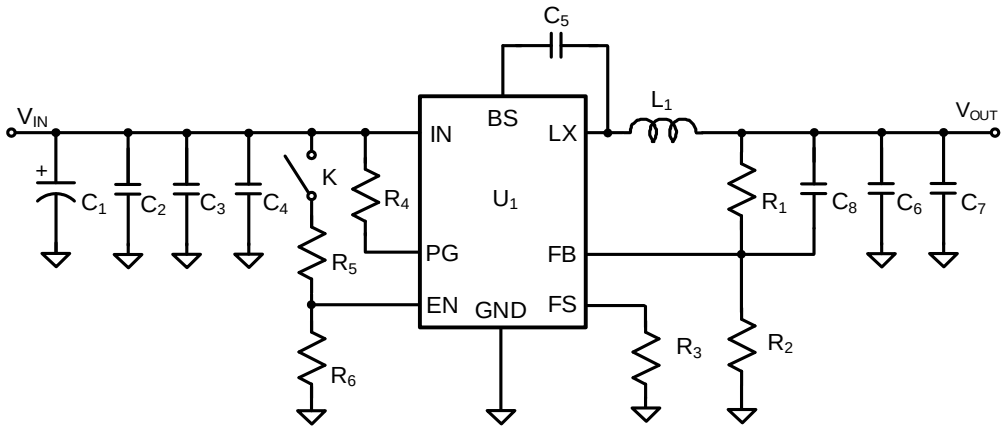
Short-Circuit Protection

The SY2A22404 includes integrated hiccup mode short-circuit protection. If the device V_{OUT} drops below 33% of the setpoint, the short-circuit protection mode will be initiated. The device will shut down for approximately 20ms, and then restart with a complete soft-start cycle that is approximately 2ms. If the short-circuit condition remains, the hiccup cycle of shutdown and restart will continue indefinitely.

Overtemperature Protection (OTP)

The SY2A22404 includes overtemperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This will shut down switching operation when the junction temperature exceeds 160°C. Once the junction temperature cools down by approximately 20°C, the IC will resume normal operation with a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the OTP threshold.

Application Schematic (V_{OUT} = 3.3V)



BOM List

Designator	Description	Part Number	Manufacturer
U1	3.5A, Buck	SY2A22404AIC	Silergy
L1	Inductor 6.8μH /4.4A	CDRH8D43-6R8NC	Sumida
C1	47μF/50V Electrolytic Cap		
C2	Null		
C3	10μF/50V/X5R,1206	C3216X5R1H106K	TDK
C4, C5	100nF/50V/0603	C1608X7R1H104K	TDK
C6, C7	22μF/16V/X5R, 1206	C3216X5R1C226M	TDK
C8	68pF/50V/C0G, 0603	C1608C0G1H680J	TDK
R1	100kΩ, 1%, 0603		
R2	13.7kΩ, 1%, 0603		
R3	200kΩ, 1%, 0603		
R4	100kΩ, 1%, 0603		
R5	10kΩ, 1%, 0603		
R6	1MΩ, 1%, 0603		

Recommended Components for Typical Applications

V_{OUT} (V)	R1(kΩ)	R2(kΩ)	C7(pF)	L1/Part Number
1.2	100	100	22	2.2μH/VLS6045EX-2R2N
1.8	100	49.9	47	3.3μH/VLS6045EX-3R3N
3.3	100	22.1	68	4.7μH/VLS6045EX-4R7M
5.0	100	13.7	100	6.8μH/VLS6045EX-6R8M

Layout Design

For optimal design, follow these PCB layout considerations:

- For minimum noise and maximum efficiency, place the following components close to the IC: C_{IN}, L, R1, and R2.
- To achieve the best thermal and noise performance, maximize the PCB copper area connecting to the GND pin. A ground plane is highly recommended if board space allows.
- C_{IN} must be close to pins IN and GND. Minimize the loop area formed by C_{IN}, V_{IN}, and GND.
- To reduce potential noise:
  - Minimize the PCB copper area connected to the LX pin.
  - R1, R2, and the trace connected to the FB pin must **not** be adjacent to the LX net on the PCB layout.
- If the system chip interfacing with the EN pin has a high impedance state during shutdown mode, and the IN pin is connected directly to a power source such as a Li-ion battery, add a 1MΩ pulldown resistor between the EN and GND pins to prevent noise from falsely triggering the regulator during shutdown mode.

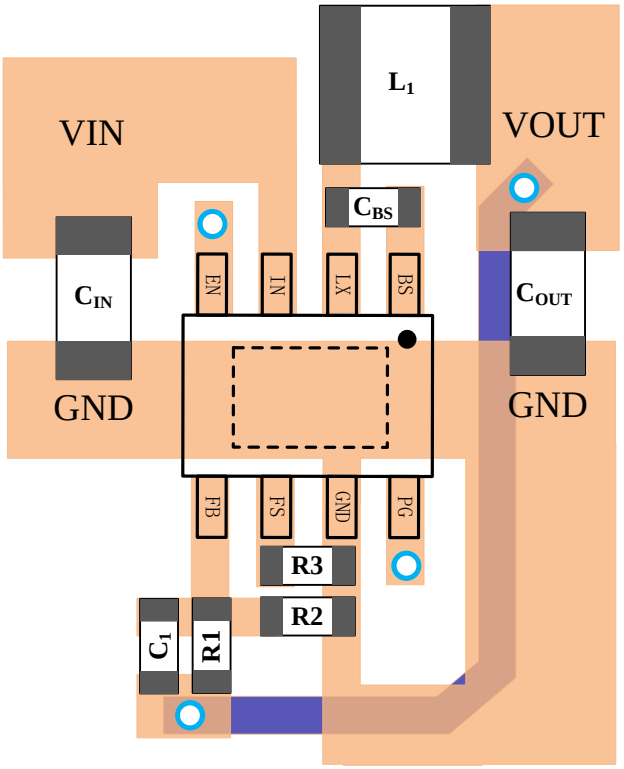
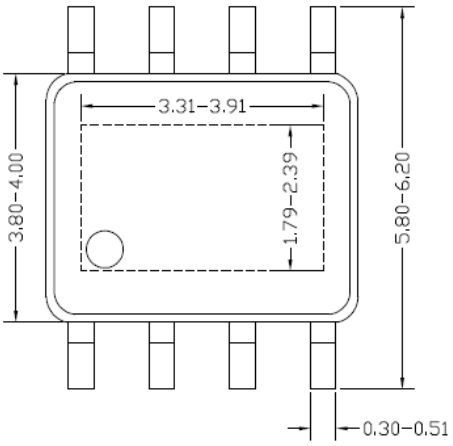
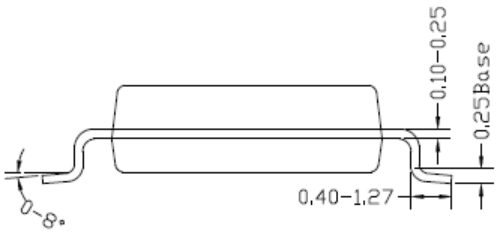


Figure 4. PCB Layout Suggestion

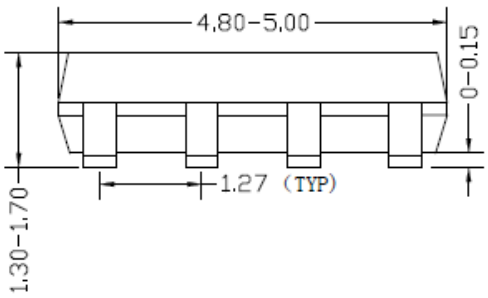
SO8E Package Outline and PCB Layout



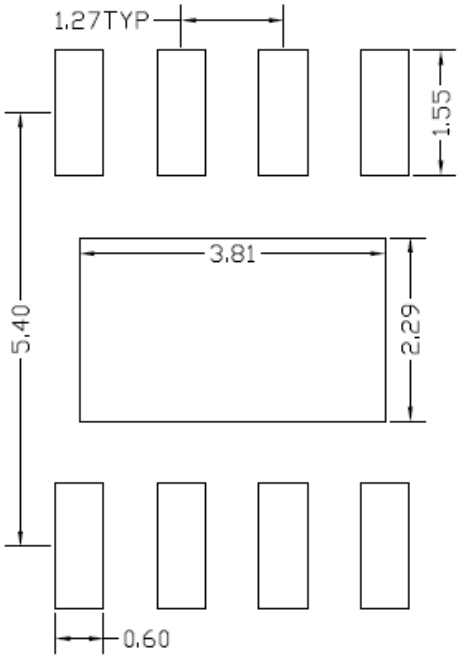
Top View



Side View



Front View

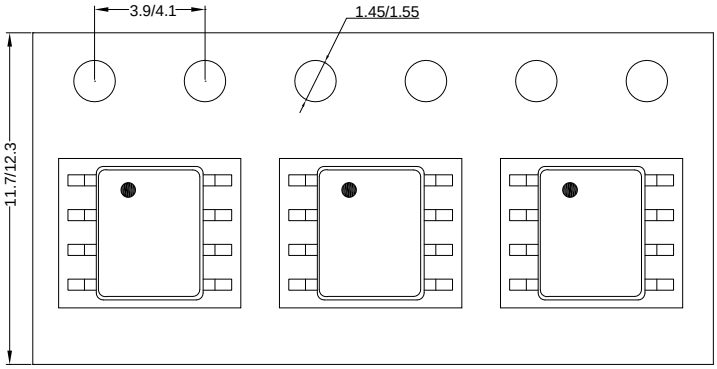


Recommended PCB Layout
(Reference Only)

Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

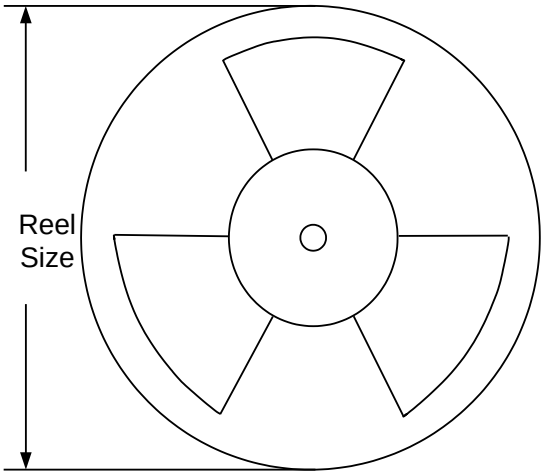
Taping and Reel Specification

Taping Orientation



Feeding direction ⟶

Carrier Tape and Reel Specification for Packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SO8E	12	8	13"	400	400	2500

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Mar.28, 2020	Revision 0.9	Initial Release
Mar.28, 2021	Revision 1.0	Production Release

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