

General Description

SY205260DVC is an ultra-low capacitance transient voltage suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for high-speed data interfaces. With a typical capacitance of 0.5pF, SY205260DVC is designed to protect against over-voltage and over-current transient events. It complies with IEC 61000-4-2 (ESD) ($\pm 15\text{kV}$ air, $\pm 15\text{kV}$ contact discharge), IEC 61000-4-5 (surge) (6 A, 8/20 μs).

The combined features of low capacitance, small size, and high ESD robustness make SY205260DVC ideal for high-speed data ports and high-frequency lines (e.g., HDMI & DVI) applications. The low clamping voltage of the SY205260DVC guarantees minimum stress on the protected IC.

Each SY205260DVC device can protect four high-speed data lines. The SY205260DVC is available in a small DFN2.5 $\times$ 1.0-10 package.

Features

- For Operating Voltage of 5.0V and Below
- Low Capacitance: 0.5pF for Each Channel
- Transient Protection for High-Speed Data Lines
 - IEC 61000-4-2 (ESD) $\pm 15\text{kV}$ (Air) $\pm 15\text{kV}$ (Contact)
 - IEC 61000-4-5 (Surge) 6A (8/20 μs)
- Small Package (2.5mm $\times$ 1.0mm $\times$ 0.55mm)
- Protects Four Data Lines
- Low Leakage Current: 0.1 μA @ V_{RWM} (Max.)
- Low Clamping Voltage
- Each I/O pin can withstand over 1000 ESD strikes for $\pm 8\text{kV}$ contact discharge.
- Pb-free and RoHS Compliant

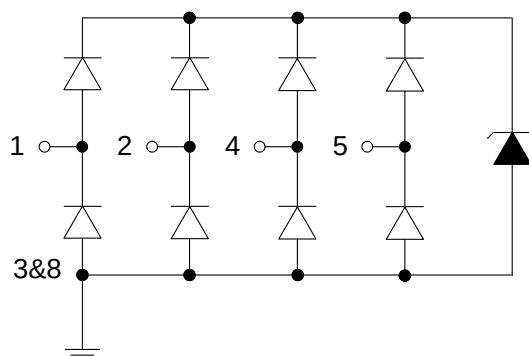
Applications

- Serial ATA
- PCI Express
- Desktops, Servers, and Notebooks
- MDDI Ports
- USB 2.0, 3.0, and 3.1
- Display Ports
- HDMI 1.3, 1.4, and 2.0
- Digital Visual Interfaces (DVI)

Mechanical Characteristics

- DFN2.5 $\times$ 1.0-10 Package
- Marking: Device Code, Date code
- Packaging: Tape and Reel

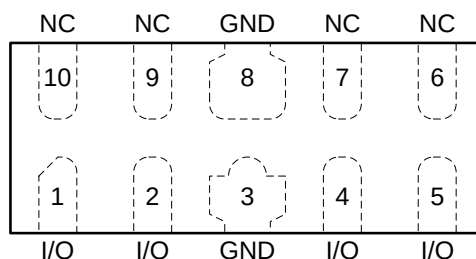
Circuit Diagram



Ordering Information

Part Number	Package Type	Top Mark
SY205260DVC	DFN2.5×1.0-10 RoHS Compliant and Halogen Free	N5YWA

Pinout (Top View)



Marking Codes



Note 1: “N5” is device code, fixed.

Note 2: “YWA” is date code.

Absolute Maximum Rating

Parameter	Symbol	Value	Units
Maximum Peak Pulse Current (8/20μs)	I_{PP}	6	A
Maximum Peak Pulse Power (8/20μs)	P_{PK}	42	Watts
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	±15	kV
Operating Temperature	T_{OPT}	-40/+125	°C
Storage Temperature	T_{STG}	-55/+150	°C

Electrical Characteristics ($T_A = 25^\circ\text{C}$)

Parameter	Symbol	Test Condition	Mini	Typ	Maxi	Units
Nominal Reverse Working Voltage	V_{RWM}				5.0	V
Reverse Leakage Current @ V_{RWM}	I_R	$V_{RWM} = 5V, T_A = 25^\circ\text{C}$		0.01	0.1	μA
Triggering Voltage @ I_{t1}	V_{t1}	$I_{t1} = 10\mu\text{A}$	5.0		10	V
Holding Voltage @ I_h	V_h	$I_h = 50\text{mA}$	5.0		9.0	V
Clamping Voltage @ I_{PP}	V_C^1	$I_{PP} = 6A, t_p = 8/20\mu\text{s}$		7.0		V
Clamping Voltage @ I_{PP}	V_C^1	$I_{PP} = 16A, t_p = 10/100\text{ns}$		8.5		V
Dynamic Resistance	$R_{DYN}^{1,2}$	$t_p = 10/100\text{ns}$		0.18		Ω
Parasitic Capacitance	C_{ESD}^1	$V_R = 2.5V, f = 1\text{MHz}$		0.50	0.80	pF

Note 1: Guaranteed by design and not subject to production test.

Note 2: R_{DYN} calculated based on $I_{PP}=8A$ to $I_{PP}=16A$, $t_p = 10/100\text{ns}$.

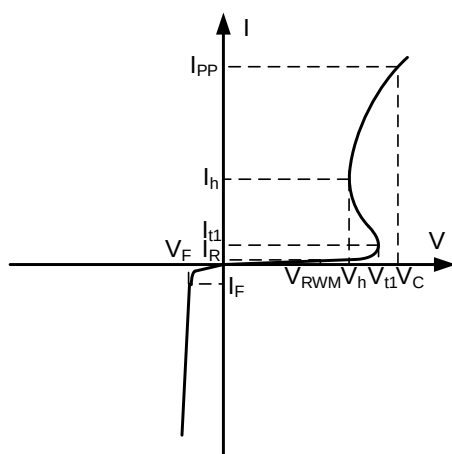
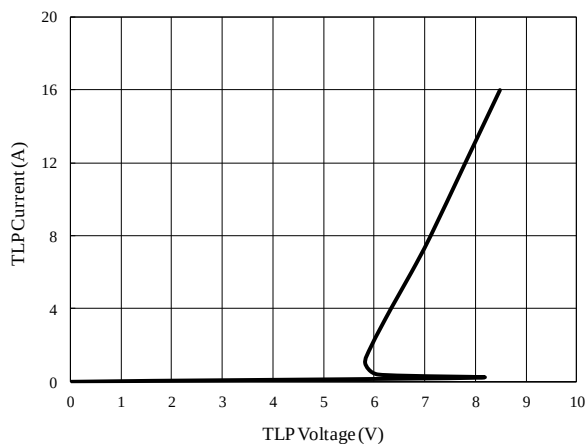


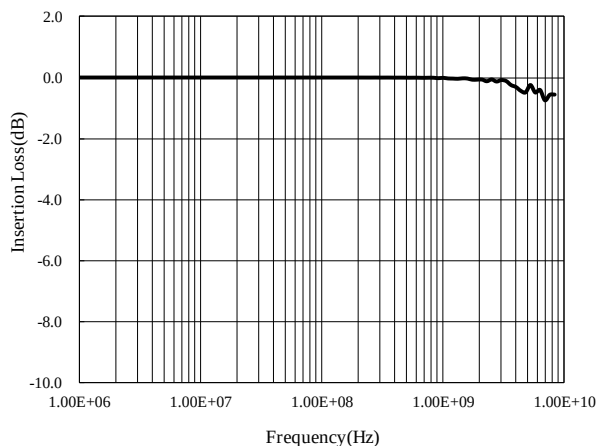
Figure 1. Uni-directional TVS

Typical Characteristics

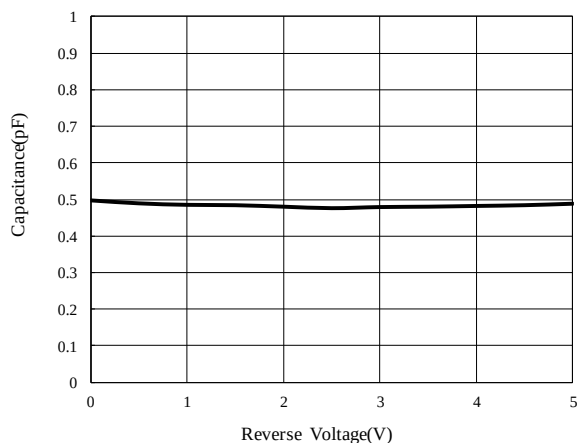
TLP Testing of I/O to GND



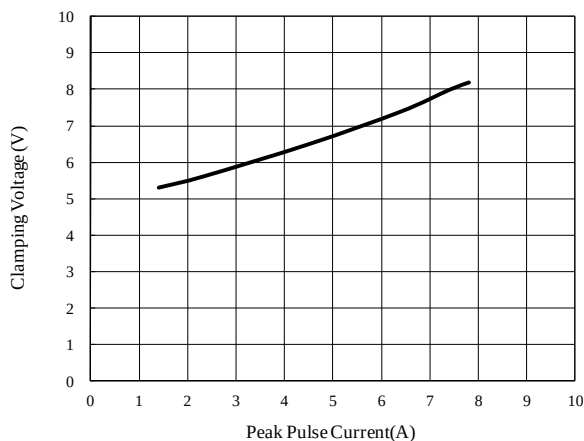
Insertion Loss S21 of I/O to GND



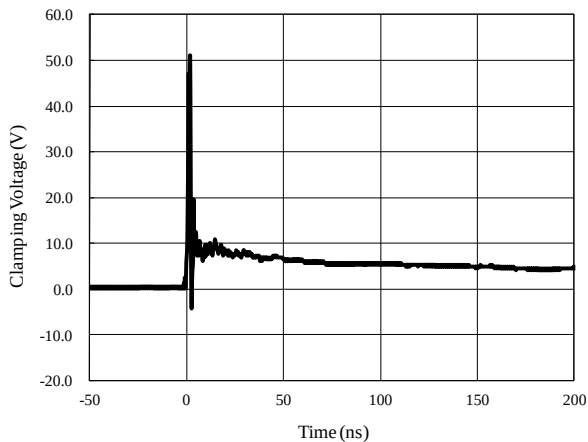
Capacitance vs. Voltage of I/O to GND



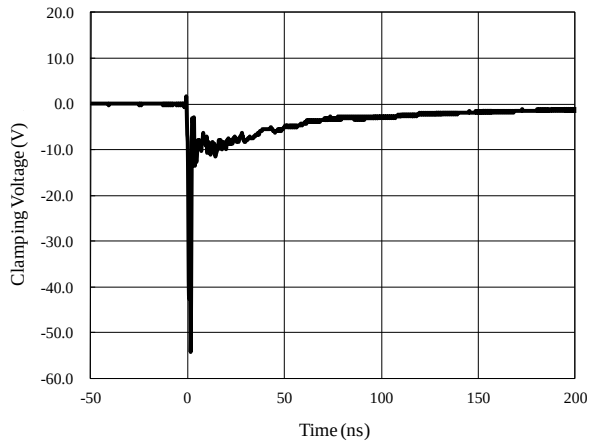
Clamping Voltage vs. Peak Pulse Current (8/20μs)



ESD Clamping of I/O to GND (+8kV Contact per IEC 61000-4-2)



ESD Clamping of I/O to GND (-8kV Contact per IEC 61000-4-2)



Application Information

Pin Connections

SY205260DVC is designed to provide ESD protection for four data lines simultaneously. The pin connections are shown in Figure 2.

The four parallel data lines can be connected from the protected IC to the I/O port connector and directly to the four SY205260DVC I/O pins. Pins 3 and 8 of SY205260DVC should connect to the ground. The connection wires should be as short as possible to minimize the parasitic inductance.

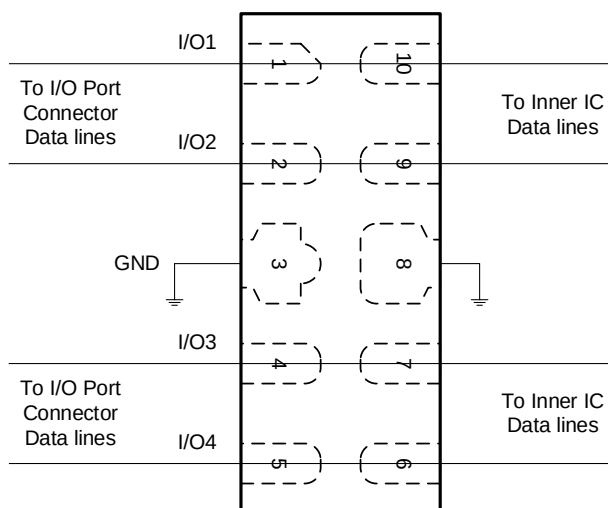


Figure 2. SY205260DVC Pin Connections in PCB

PCB Layout Guidelines

For optimum ESD protection and circuit performance, the following PCB layout guidelines are recommended:

- Place SY205260DVC as close to the connector port as possible.
- The distance between the SY205260DVC ground pin and the GND reference path should be as short as possible.
- Use large vias to connect the SY205260DVC GND pins to the PCB VCC and GND.
- Avoid running critical signals near board edges.

Application Information

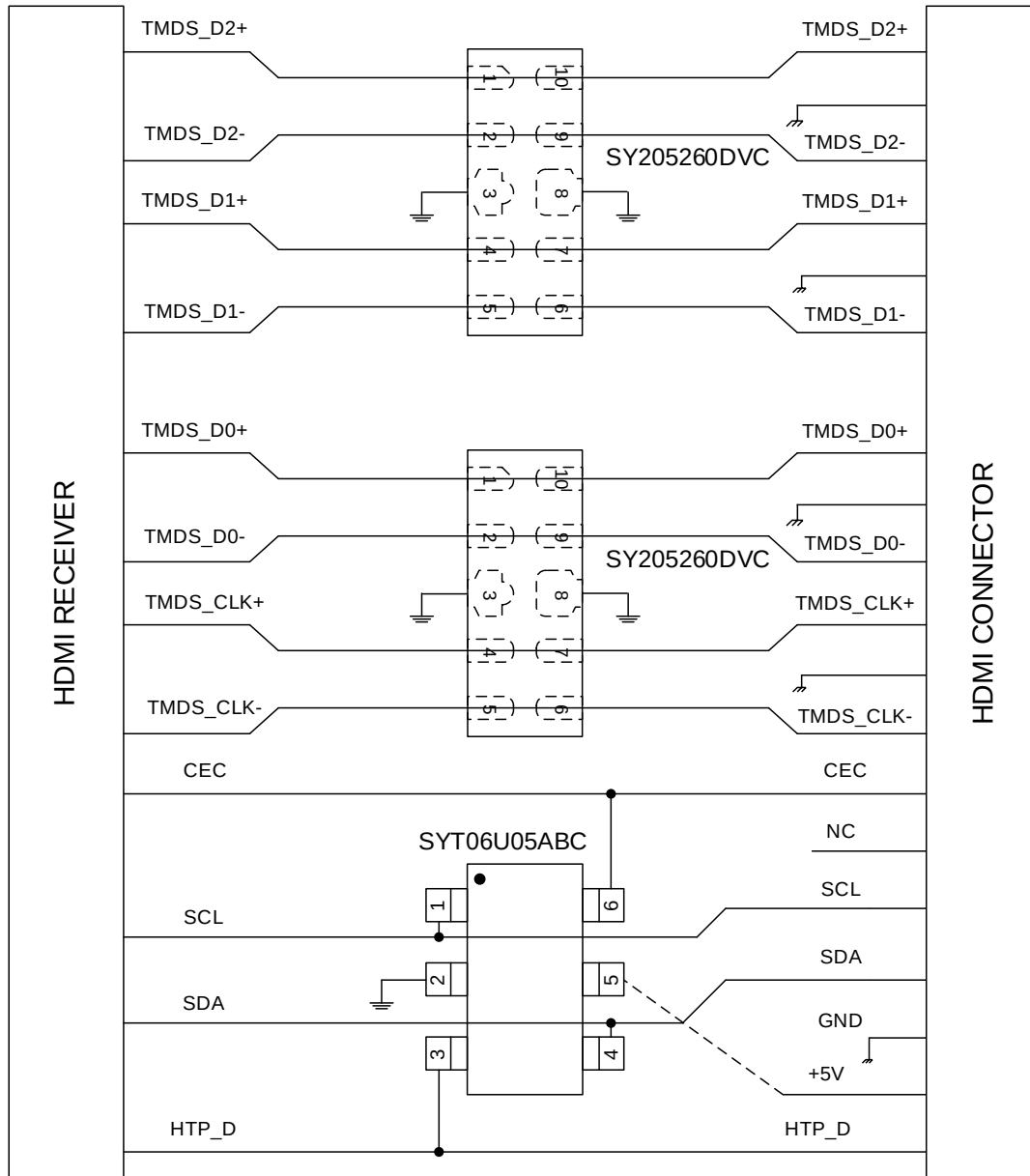
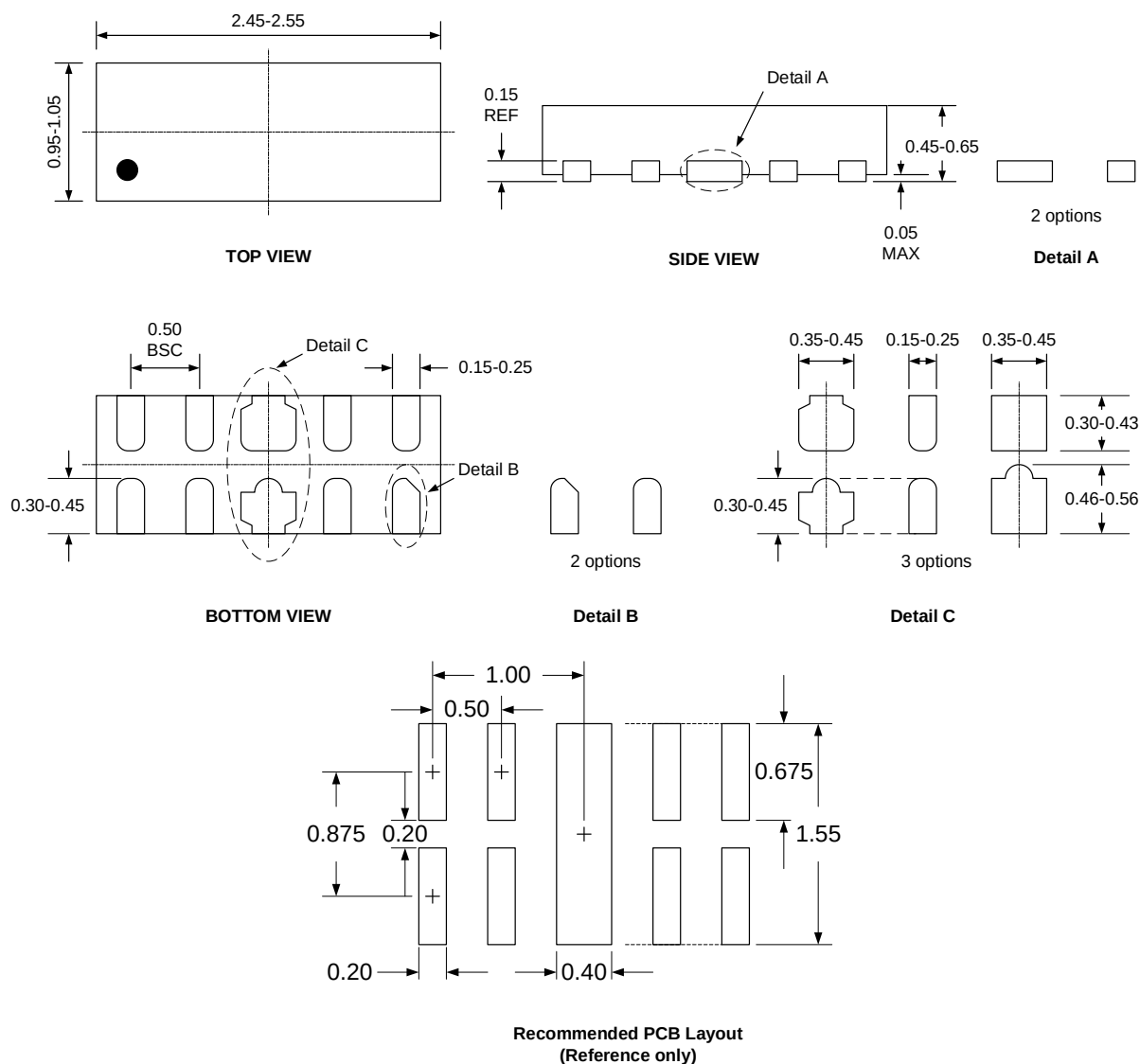


Figure 3. Layout Top View for HDMI Interface with SY205260DVC and SYT06U05ABC

DFN2.5×1.0-10 Package Outline

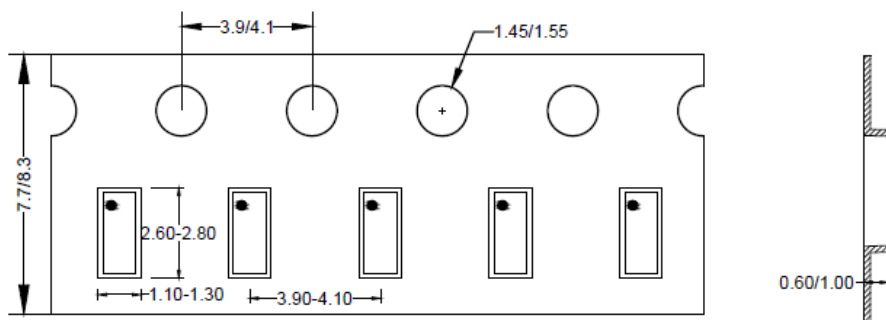


Package Dimensions (Controlling Dimensions are in Millimeters)

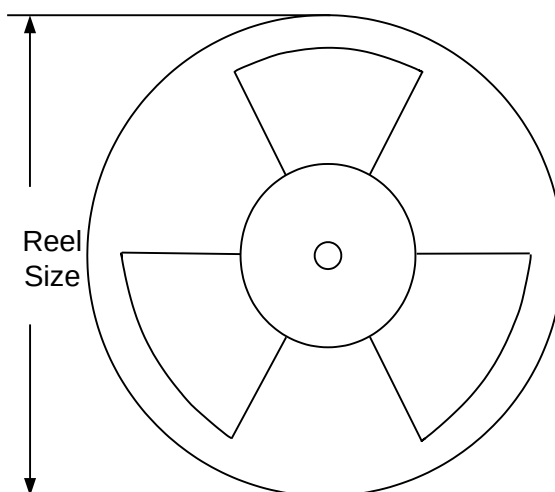
Note: All dimensions are in millimeters and exclude mold flash and metal burr

Tape and Reel Specification

DFN2.5×1.0-10 Taping Orientation



Carrier Tape & Reel Specification for Packages



Package Types	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Qty per Reel(pcs)
DFN2.5×1.0-10	8	4	7"	3000



Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
0.9	06/11/2021	Initial Release	
1.0	06/11/2022	Production Release	

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