

1. General description

Planar passivated Silicon Controlled Rectifier (SCR) in a SOT78 (TO-220AB) plastic package intended for use in applications requiring very high inrush current capability, high thermal cycling performance and high junction temperature capability ($T_{i(max)} = 150$ °C).

2. Features and benefits

- High bidirectional blocking voltage capability
- · High junction operating temperature capability
- High thermal cycling performance
- · Planar passivated for voltage ruggedness and reliability
- · Very high current surge capability

3. Applications

- Capacitive Discharge Ignition (CDI)
- Crowbar protection
- Inrush protection
- Motor control
- Voltage regulation

4. Quick reference data

|--|

| Symbol | Parameter | Conditions | Min | Тур | Max | Unit |
|---------------------|--|--|-----|-----|------|------|
| V _{RRM} | repetitive peak reverse voltage | | - | - | 800 | V |
| I _{T(AV)} | average on-state current | half sine wave; T _{mb} ≤ 129 °C; <u>Fig. 1</u> | - | - | 12.7 | A |
| I _{T(RMS)} | RMS on-state current | half sine wave; T _{mb} ≤ 129 °C; <u>Fig. 2;</u> <u>Fig. 3</u> | - | - | 20 | A |
| I _{TSM} | non-repetitive peak on- state current | half sine wave; T _{j(init)} = 25 °C; t _p = 10 ms; <u>Fig. 4</u> ; <u>Fig. 5</u> | - | - | 210 | A |
| | | half sine wave; T _{j(init)} = 25 °C; t _p = 8.3 ms | - | - | 231 | A |
| Tj | junction temperature | | - | - | 150 | °C |
| Static chara | acteristics | | - | | | |
| I _{GT} | gate trigger current | V _D = 12 V; I _T = 0.1 A; T _j = 25 °C; <u>Fig. 7</u> | - | 4.5 | 32 | mA |
| Dynamic ch | aracteristics | | | | 1 | |

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| Symbol | Parameter | Conditions | Min | Тур | Max | Unit |
|---------------------|-----------------------------------|--|------|-----|-----|------|
| dV _D /dt | rate of rise of off-state voltage | V_{DM} = 402 V; T _j = 150 °C; exponential waveform; gate open circuit | 1000 | - | - | V/µs |
| | | V_{DM} = 536 V; T _j = 150 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit | 500 | - | - | V/µs |

5. Pinning information

| 1 2 | K | cathode | | |
|--------|---|-----------------------------------|----|-------------|
| 2 | | | mb | A H K |
| | A | anode | | G sym037 |
| 3 | G | gate | | Symusi |
| mb | A | mounting base; connected to anode | | |

6. Ordering information

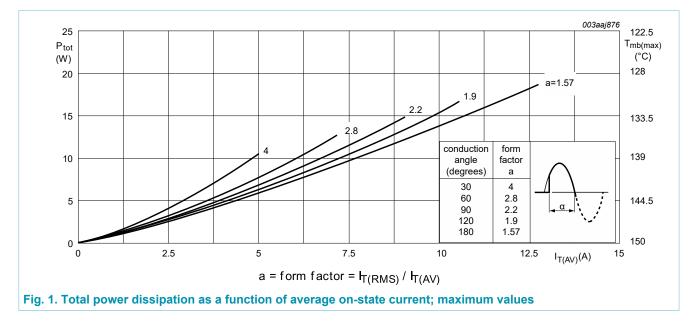
| Table 3. Ordering information | | | | | | | |
|-------------------------------|----------|--|---------|--|--|--|--|
| Type number | Package | | | | | | |
| | Name | Description | Version | | | | |
| TYN20-800T | TO-220AB | plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB | SOT78 | | | | |

7. Limiting values

Table 4. Limiting values

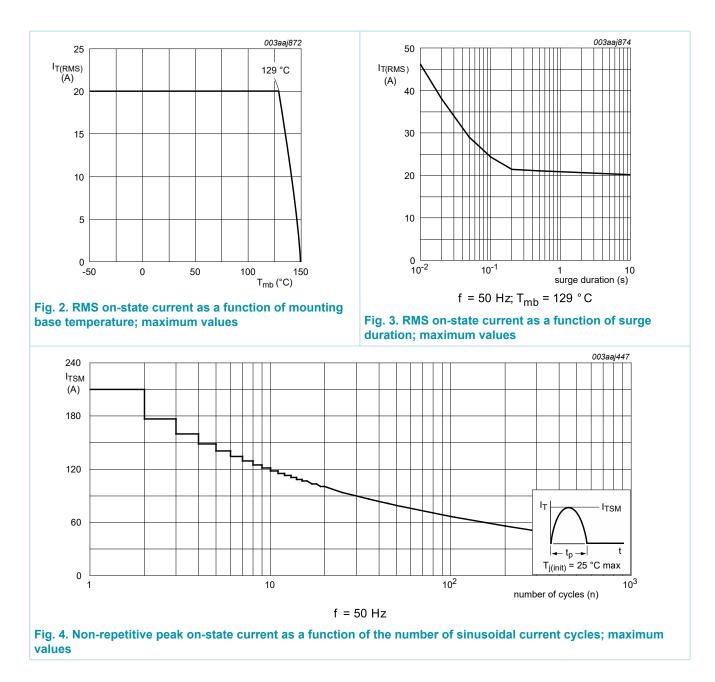
In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---------------------|--|--|-----|-------|------|
| V _{DRM} | repetitive peak off-state voltage | | - | 800 | V |
| V _{RRM} | repetitive peak reverse voltage | | - | 800 | V |
| I _{T(AV)} | average on-state current | half sine wave; $T_{mb} \le 129 \text{ °C}$; Fig. 1 | - | 12.7 | А |
| I _{T(RMS)} | RMS on-state current | half sine wave; T _{mb} ≤ 129 °C; <u>Fig. 2;</u> <u>Fig. 3</u> | - | 20 | A |
| I _{TSM} | non-repetitive peak on- state current | half sine wave; T _{j(init)} = 25 °C; t _p = 10 ms; <u>Fig. 4; Fig. 5</u> | - | 210 | A |
| | | half sine wave; T _{j(init)} = 25 °C; t _p = 8.3 ms | - | 231 | А |
| l ² t | I ² t for fusing | t _p = 10 ms; sine-wave pulse | - | 220.5 | A²s |
| dl _T /dt | rate of rise of on-state current | I _G = 70 mA | - | 100 | A/µs |
| I _{GM} | peak gate current | | - | 5 | А |
| V _{RGM} | peak reverse gate voltage | | - | 5 | V |
| P _{GM} | peak gate power | | - | 20 | W |
| P _{G(AV)} | average gate power | over any 20 ms period | - | 1 | W |
| T _{stg} | storage temperature | | -40 | 150 | °C |
| Tj | junction temperature | | - | 150 | °C |



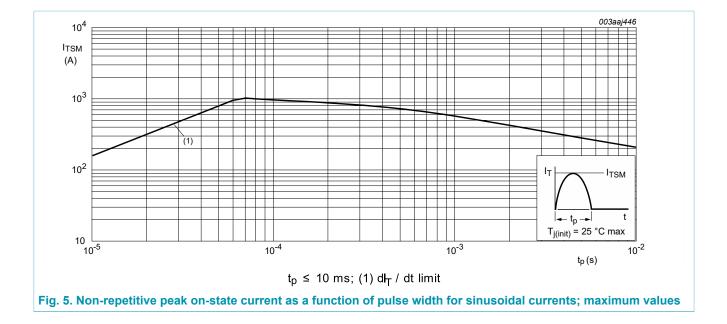
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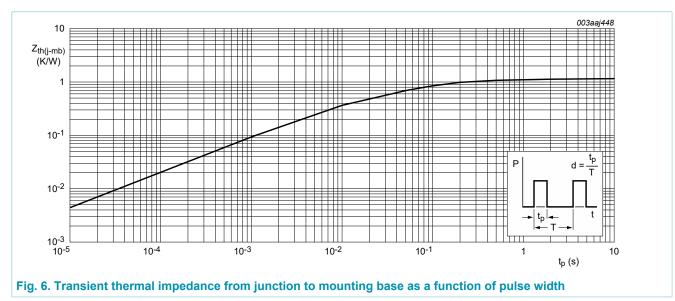
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8. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Тур | Max | Unit |
|-----------------------|--|---------------|-----|-----|-----|------|
| R _{th(j-mb)} | thermal resistance from junction to mounting base | Fig. <u>6</u> | - | - | 1.1 | K/W |
| R _{th(j-a)} | thermal resistance from junction to ambient free air | in free air | - | 60 | - | K/W |



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9. Characteristics

| Symbol | Parameter | Conditions | Min | Тур | Max | Unit |
|---------------------|-----------------------------------|--|------|-----|-----|------|
| Static chara | acteristics | · · · · · · · · · · · · · · · · · · · | | | | |
| I _{GT} | gate trigger current | V _D = 12 V; I _T = 0.1 A; T _j = 25 °C; <u>Fig. 7</u> | - | 4.5 | 32 | mA |
| IL | latching current | V _D = 12 V; I _G = 0.1 A; T _j = 25 °C; <u>Fig. 8</u> | - | 21 | 60 | mA |
| I _H | holding current | V _D = 12 V; T _j = 25 °C; <u>Fig. 9</u> | - | 16 | 40 | mA |
| V _T | on-state voltage | I _T = 32 A; T _j = 25 °C; <u>Fig. 10</u> | - | 1.2 | 1.5 | V |
| V _{GT} | gate trigger voltage | V _D = 12 V; I _T = 0.1 A; T _j = 25 °C; Fig. 11 | - | 0.7 | 1.3 | V |
| | | V _D = 400 V; I _T = 0.1 A; T _j = 150 °C; Fig. 11 | 0.2 | 0.4 | - | V |
| I _D | off-state current | V _D = 800 V; T _j = 150 °C | - | 0.2 | 1 | mA |
| I _R | reverse current | V _R = 800 V; T _j = 150 °C | - | 0.2 | 1 | mA |
| Dynamic ch | aracteristics | | · | | | |
| dV _D /dt | rate of rise of off-state voltage | V_{DM} = 402 V; T _j = 150 °C; exponential waveform; gate open circuit | 1000 | - | - | V/µs |
| | | V_{DM} = 536 V; T_j = 150 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit | 500 | - | - | V/µs |
| t _{gt} | gate-controlled turn-on time | I_{TM} = 40 A; V _D = 800 V; I _G = 100 mA; dI _G /dt = 5 A/µs; T _j = 25 °C | - | - | 2 | μs |
| t _q | commutated turn-off time | $V_{DM} = 536 \text{ V}; \text{ T}_{j} = 125 \text{ °C}; \text{ I}_{TM} = 20 \text{ A};$ $V_{R} = 25 \text{ V}; (dI_{T}/dt)_{M} = 30 \text{ A/}\mu\text{s}; dV_{D}/$ $dt = 50 \text{ V/}\mu\text{s}; \text{R}_{GK(ext)} = 100 \Omega; (V_{DM} = 67\% \text{ of } V_{DRM});$ exponential waveform; gate open circuit | - | 70 | - | μs |

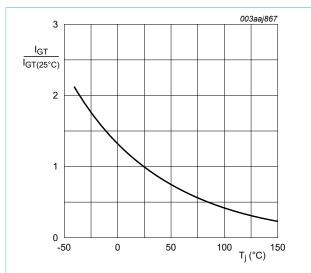


Fig. 7. Normalized gate trigger current as a function of junction temperature

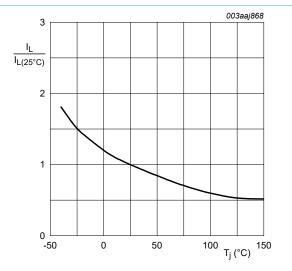
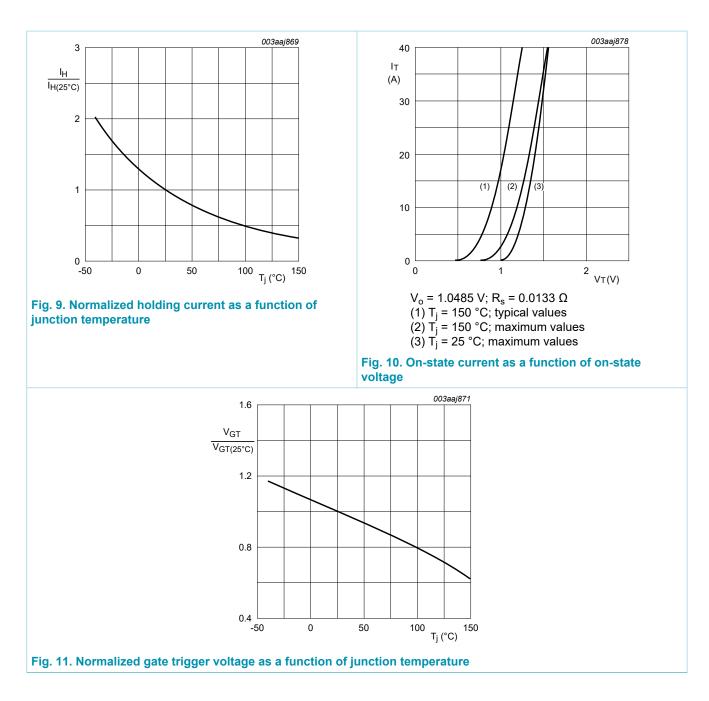


Fig. 8. Normalized latching current as a function of junction temperature

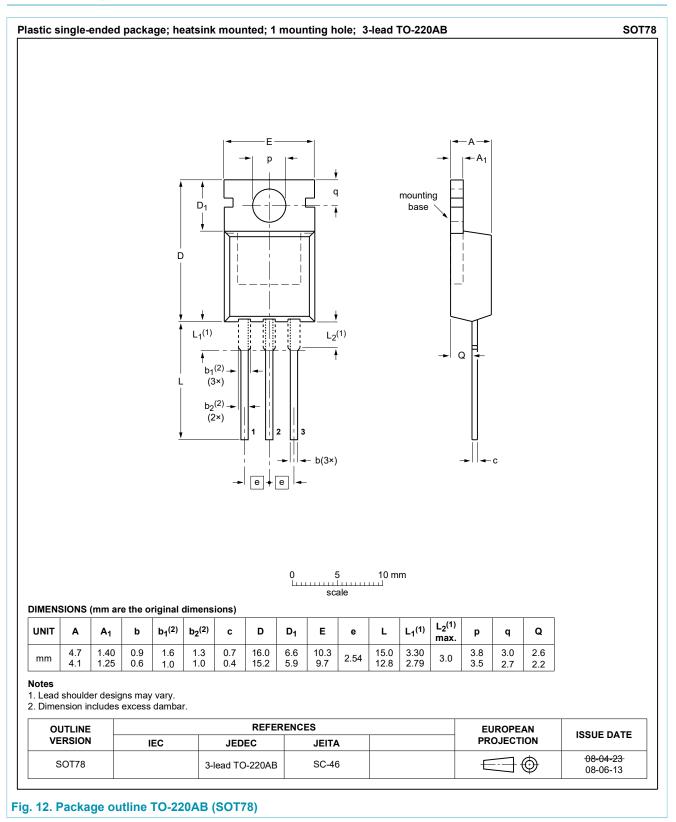
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10. Package outline



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11. Legal information

Data sheet status

| Document status [1][2] | Product status [<u>3]</u> | Definition |
|--------------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

- [2] The term 'short data sheet' is explained in section "Definitions".
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