

1. General description

Planar passivated Silicon Controlled Rectifier (SCR) in a SOT186A (TO-220F) "full pack" plastic package intended for use in applications requiring very high inrush current capability, high thermal cycling performance and high junction temperature capability ($T_{j(max)} = 150$ °C).

2. Features and benefits

- · High junction operating temperature capability
- High thermal cycling performance
- High voltage capability
- Isolated package
- · Planar passivated for voltage ruggedness and reliability
- Very High current surge capability

3. Applications

- Ignition circuits
- Motor control
- · Protection circuits e.g. SMPS inrush current
- Voltage regulation

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{RRM}	repetitive peak reverse voltage		-	-	800	V
I _{T(AV)}	average on-state current	half sine wave; T _h ≤ 86 °C; <u>Fig. 1</u>	-	-	10.2	A
I _{T(RMS)}	RMS on-state current	half sine wave; T _h ≤ 86 °C; <u>Fig. 2;</u> <u>Fig. 3</u>	-	-	16	A
I _{TSM}	non-repetitive peak on- state current	half sine wave; T _{j(init)} = 25 °C; t _p = 10 ms; <u>Fig. 4; Fig. 5</u>	-	-	210	A
		half sine wave; T _{j(init)} = 25 °C; t _p = 8.3 ms	-	-	231	A
Tj	junction temperature		-	-	150	°C
Static chara	acteristics	·				
I _{GT}	gate trigger current	V _D = 12 V; I _T = 0.1 A; T _j = 25 °C; <u>Fig. 7</u>	-	4.5	25	mA
Dynamic ch	aracteristics	·				

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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
dV _D /dt	rate of rise of off-state voltage	V_{DM} = 536 V; T _j = 150 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit	300	-	-	V/µs

5. Pinning information

Table 2	. Pinning in	formation		
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	К	cathode	mb	A H K
2	А	anode		Ğ sym037
3	G	gate		Symoor
mb	n.c.	mounting base; isolated		
			TO-220F (SOT186A)	

6. Ordering information

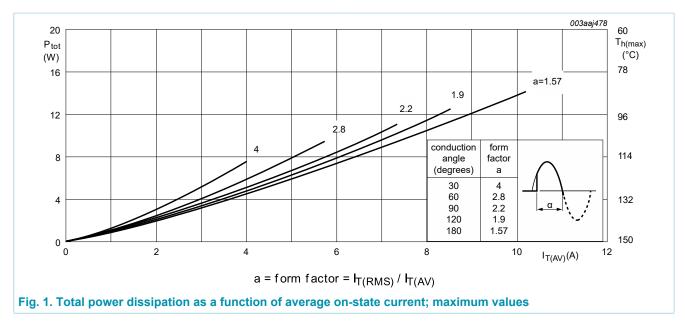
Table 3. Ordering information						
Type number	Package					
	Name	Description	Version			
TYN16X-800RT	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A			

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

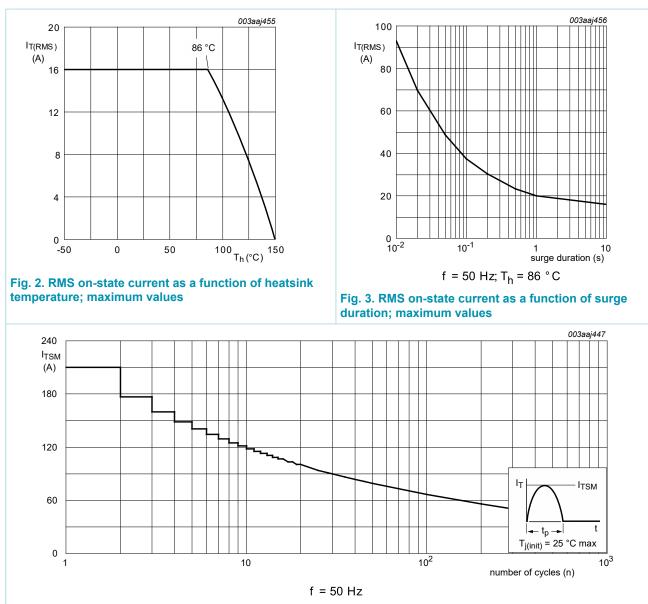
Symbol	Parameter	Conditions	Min	Max	Unit
V _{DRM}	repetitive peak off-state voltage		-	800	V
V _{RRM}	repetitive peak reverse voltage		-	800	V
I _{T(AV)}	average on-state current	half sine wave; T _h ≤ 86 °C; <u>Fig. 1</u>	-	10.2	А
I _{T(RMS)}	RMS on-state current	half sine wave; T _h ≤ 86 °C; <u>Fig. 2; Fig. 3</u>	-	16	А
I _{TSM}	non-repetitive peak on- state current	half sine wave; T _{j(init)} = 25 °C; t _p = 10 ms; Fig. 4; Fig. 5	-	210	A
		half sine wave; $T_{j(init)}$ = 25 °C; t_p = 8.3 ms	-	231	А
l ² t	I ² t for fusing	t _p = 10 ms; SIN	-	220.5	A²s
dl _T /dt	rate of rise of on-state current	I _G = 50 mA	-	50	A/µs
I _{GM}	peak gate current		-	5	А
V _{RGM}	peak reverse gate voltage		-	5	V
P _{GM}	peak gate power		-	20	W
P _{G(AV)}	average gate power	over any 20 ms period	-	1	W
T _{stg}	storage temperature		-40	150	°C
Tj	junction temperature		-	150	°C



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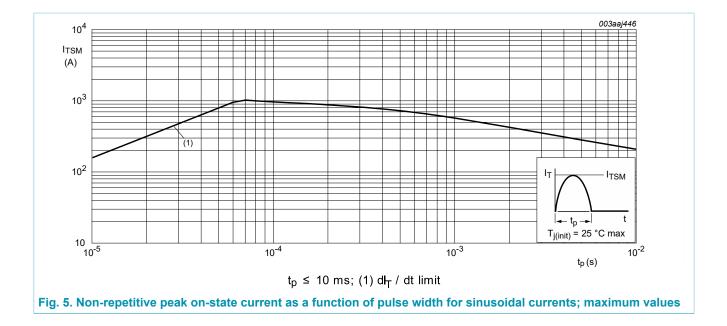
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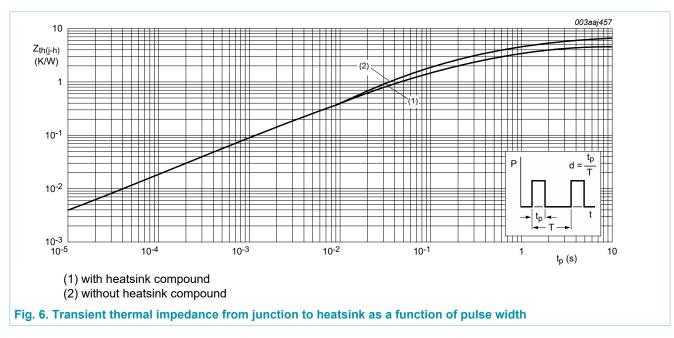
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8. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-h)}	thermal resistance from junction to heatsink	with heatsink compound; Fig. 6	-	-	4.5	K/W
		without heatsink compound; Fig. 6	-	-	6.5	K/W
R _{th(j-a)}	thermal resistance from junction to ambient free air	in free air	-	55	-	K/W



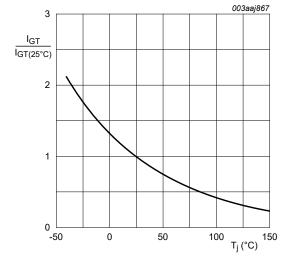
9. Isolation characteristics

Table 6. Isolation characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{isol(RMS)}	RMS isolation voltage	from all terminals to external heatsink; sinusoidal waveform; clean and dust free; 50 Hz \leq f \leq 60 Hz; RH \leq 65 %; T _h = 25 °C	-	-	2500	V
C _{isol}	isolation capacitance	from anode to external heatsink; f = 1 MHz; T _h = 25 °C	-	10	-	pF

10. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	cteristics	· · · · ·				
I _{GT}	gate trigger current	V _D = 12 V; I _T = 0.1 A; T _j = 25 °C; <u>Fig. 7</u>	-	4.5	25	mA
I _L	latching current	V _D = 12 V; I _G = 0.1 A; T _j = 25 °C; <u>Fig. 8</u>	-	21	60	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; <u>Fig. 9</u>	-	16	40	mA
V _T	on-state voltage	I _T = 32 A; T _j = 25 °C; <u>Fig. 10</u>	-	1.2	1.5	V
V _{GT}	gate trigger voltage	V _D = 12 V; I _T = 0.1 A; T _j = 25 °C; Fig. 11	-	0.7	1.3	V
		V _D = 400 V; I _T = 0.1 A; T _j = 150 °C; Fig. 11	0.2	0.4	-	V
ID	off-state current	V _D = 800 V; T _j = 150 °C	-	0.2	1	mA
I _R	reverse current	V _R = 800 V; T _j = 150 °C	-	0.2	1	mA
Dynamic ch	aracteristics	· · ·	'			
dV _D /dt	rate of rise of off-state voltage	V_{DM} = 536 V; T _j = 150 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit	300	-	-	V/µs



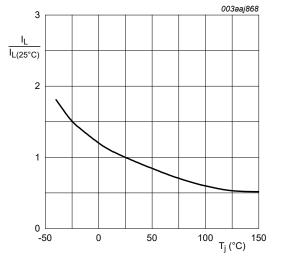
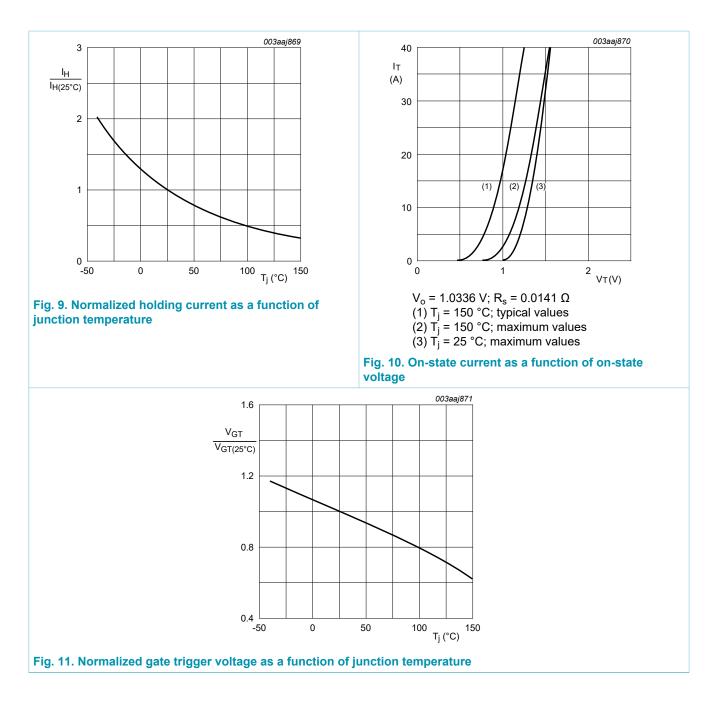


Fig. 7. Normalized gate trigger current as a function of
junction temperatureFig. 8. Normalized latching current as a function of
junction temperature

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11. Package outline

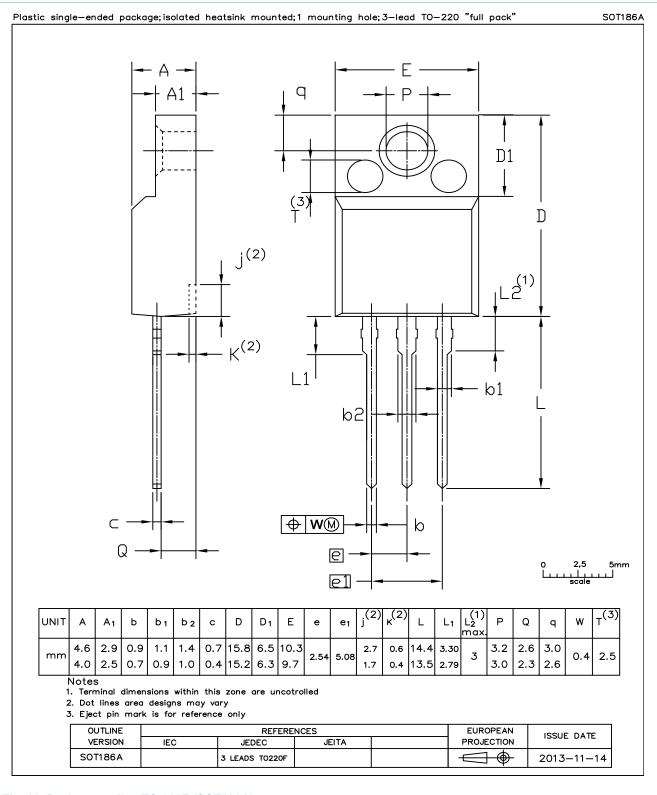


Fig. 12. Package outline TO-220F (SOT186A)

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12. Legal information

Data sheet status

Document status [1][2]	Product status [<u>3]</u>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <u>http://www.ween-semi.com</u>.

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