

1. General description

Planar passivated Silicon Controlled Rectifier with sensitive gate in a SOT54 (TO-92) plastic package. This SCR is designed to be interfaced directly to microcontrollers, logic ICs and other low power gate trigger circuits.

2. Features and benefits

- · High voltage capability
- · Planar passivated for voltage ruggedness and reliability
- Sensitive gate

3. Applications

- Ignition circuits
- Lighting ballasts
- Protection circuits
- Switched Mode Power Supplies

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{RRM}	repetitive peak reverse voltage			-	-	600	V
I _{T(AV)}	average on-state current	half sine wave; T _{lead} ≤ 83 °C; <u>Fig. 1</u>		-	-	0.5	Α
I _{T(RMS)}	RMS on-state current	half sine wave; T _{lead} ≤ 83 °C; <u>Fig. 2</u> ; <u>Fig. 3</u>		-	-	0.8	Α
Ітѕм	non-repetitive peak on- state current	half sine wave; $T_{j(init)}$ = 25 °C; t_p = 10 ms; Fig. 4; Fig. 5		-	-	8	Α
		half sine wave; $T_{j(init)}$ = 25 °C; t_p = 8.3 ms		-	-	9	А
Tj	junction temperature			-	-	125	°C
Static characte	eristics						
I _{GT}	gate trigger current	$V_D = 12 \text{ V}; I_T = 10 \text{ mA}; T_j = 25 \text{ °C};$ Fig. 7		-	50	200	μΑ
Dynamic characteristics							
dV _D /dt	rate of rise of off-state voltage	V_{DM} = 402 V; T_j = 125 °C; R_{GK} = 1 k Ω ; (V_{DM} = 67% of V_{DRM}); exponential waveform; Fig. 12		500	800	-	V/µs

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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
		V_{DM} = 402 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit; Fig. 12	-	25	-	V/µs

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	Α	anode		A -
2	G	gate		G sym037
3	K	cathode	TO-92 (SOT54)	Symoon

6. Ordering information

Table 3. Ordering information

	<u></u>							
Type number	Package	age						
	Name	Description	Version					
BT169G	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54					

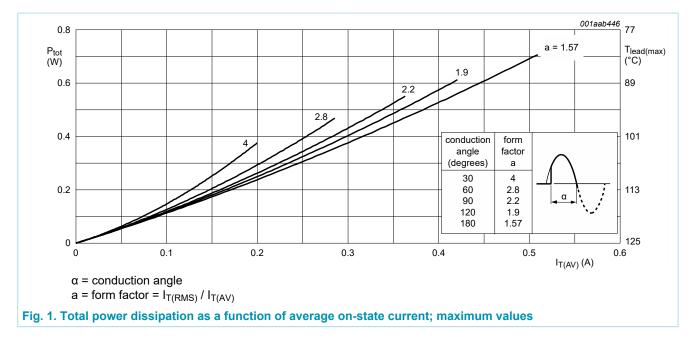
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7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	600	V
V_{RRM}	repetitive peak reverse voltage		-	600	V
I _{T(AV)}	average on-state current	half sine wave; T _{lead} ≤ 83 °C; <u>Fig. 1</u>	-	0.5	Α
I _{T(RMS)}	RMS on-state current	half sine wave; T _{lead} ≤ 83 °C; <u>Fig. 2</u> ; <u>Fig. 3</u>	-	0.8	Α
I _{TSM}	non-repetitive peak on- state current	half sine wave; $T_{j(init)} = 25$ °C; $t_p = 10$ ms; Fig. 4; Fig. 5	-	8	Α
		half sine wave; T _{j(init)} = 25 °C; t _p = 8.3 ms	-	9	Α
I ² t	I ² t for fusing	t _p = 10 ms; SIN	-	0.32	A²s
dl _T /dt	rate of rise of on-state current	$I_T = 2 \text{ A}$; $I_G = 10 \text{ mA}$; $dI_G/dt = 100 \text{ mA}/\mu\text{s}$	-	50	A/µs
I _{GM}	peak gate current		-	1	Α
V_{RGM}	peak reverse gate voltage		-	5	V
P _{GM}	peak gate power		-	2	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.1	W
T _{stg}	storage temperature		-40	150	°C
T _j	junction temperature		-	125	°C



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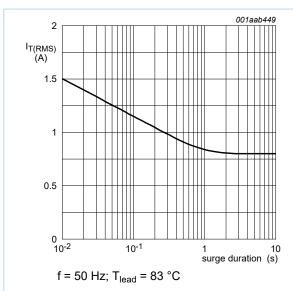


Fig. 2. RMS on-state current as a function of surge duration for sinusoidal currents

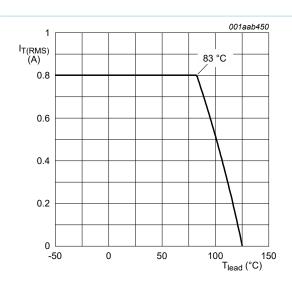


Fig. 3. RMS on-state current as a function of lead temperature; maximum values

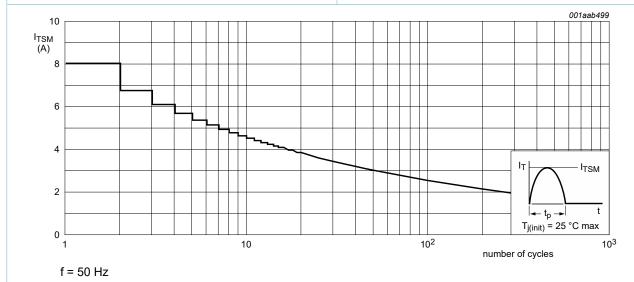
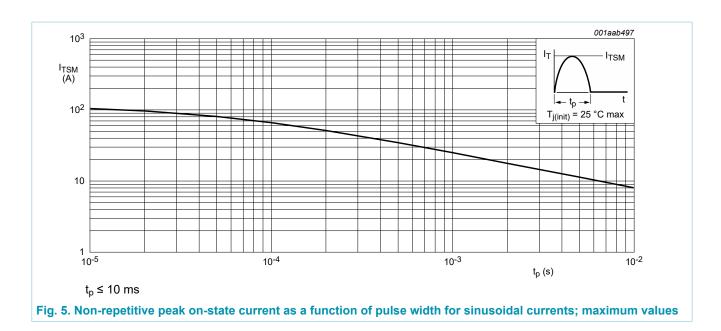


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

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8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-lead)}	thermal resistance from junction to lead	<u>Fig. 6</u>	-	-	60	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	printed circuit board mounted: lead length = 4 mm	-	150	-	K/W

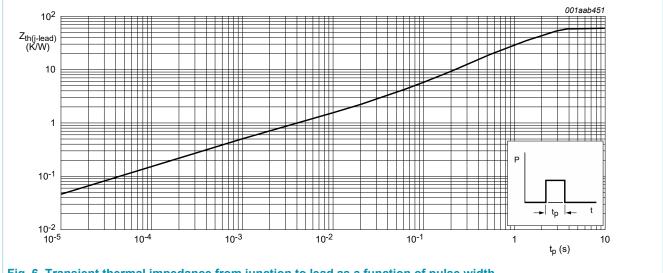


Fig. 6. Transient thermal impedance from junction to lead as a function of pulse width

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9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static char	acteristics		,			
I _{GT}	gate trigger current	$V_D = 12 \text{ V}; I_T = 10 \text{ mA}; T_j = 25 \text{ °C};$ Fig. 7	-	50	200	μΑ
IL	latching current	$V_D = 12 \text{ V}; I_G = 0.5 \text{ mA}; T_j = 25 ^{\circ}\text{C};$ Fig. 8	-	2	6	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; <u>Fig. 9</u>	-	2	5	mA
V_T	on-state voltage	I _T = 1.2 A; T _j = 25 °C; <u>Fig. 10</u>	-	1.25	1.7	V
V_{GT}	gate trigger voltage	$V_D = 12 \text{ V}; I_T = 10 \text{ mA}; T_j = 25 \text{ °C};$ Fig. 11	-	0.5	0.8	V
		V_D = 600 V; I_T = 10 mA; T_j = 125 °C; Fig. 11	0.2	0.3	-	V
I _D	off-state current	$V_D = 600 \text{ V}; R_{GK(ext)} = 1 \text{ k}\Omega; T_j = 125 °C$	-	0.05	0.1	mA
I _R	reverse current	$V_R = 600 \text{ V}; T_j = 125 \text{ °C}; R_{GK(ext)} = 1 \text{ k}\Omega$	-	0.05	0.1	mA
Dynamic cl	haracteristics					
dV _D /dt	rate of rise of off-state voltage	V_{DM} = 402 V; T_j = 125 °C; R_{GK} = 1 kΩ; (V_{DM} = 67% of V_{DRM}); exponential waveform; Fig. 12	500	800	-	V/µs
		V_{DM} = 402 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit; Fig. 12	-	25	-	V/µs
t _{gt}	gate-controlled turn-on time	I_{TM} = 2 A; V_D = 600 V; I_G = 10 mA; $dI_G/$ dt = 0.1 A/µs; T_j = 25 °C	-	2	-	μs
t _q	commutated turn-off time	V_{DM} = 402 V; T_j = 125 °C; I_{TM} = 1.6 A; V_R = 35 V; $(dI_T/dt)_M$ = 30 A/µs; dV_D/dt = 2 V/µs; $R_{GK(ext)}$ = 1 k Ω ; $(V_{DM}$ = 67% of $V_{DRM})$	-	100	-	μs

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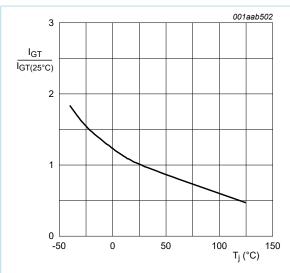


Fig. 7. Normalized gate trigger current as a function of junction temperature

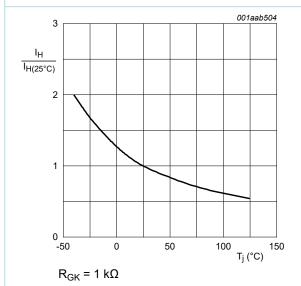


Fig. 9. Normalized holding current as a function of junction temperature

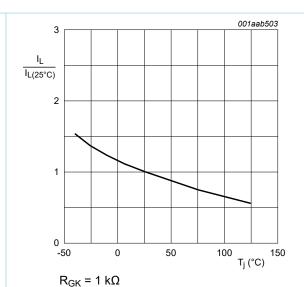
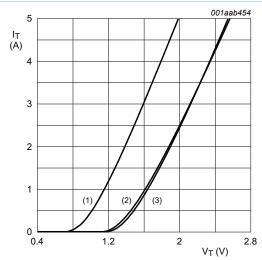


Fig. 8. Normalized latching current as a function of junction temperature



 V_o = 1.067 V; R_s = 0.187 Ω

(1) T_i = 125 °C; typical values

(2) T_j = 125 °C; maximum values (3) T_j = 25 °C; maximum values

Fig. 10. On-state current as a function of on-state voltage

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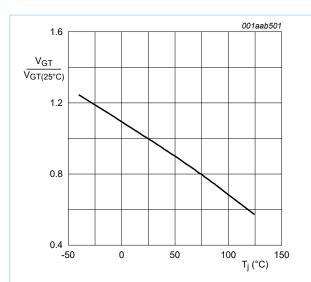


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

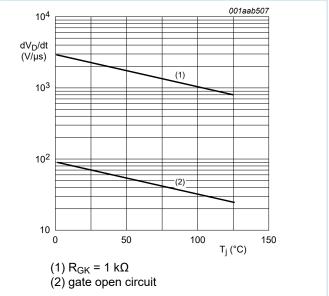
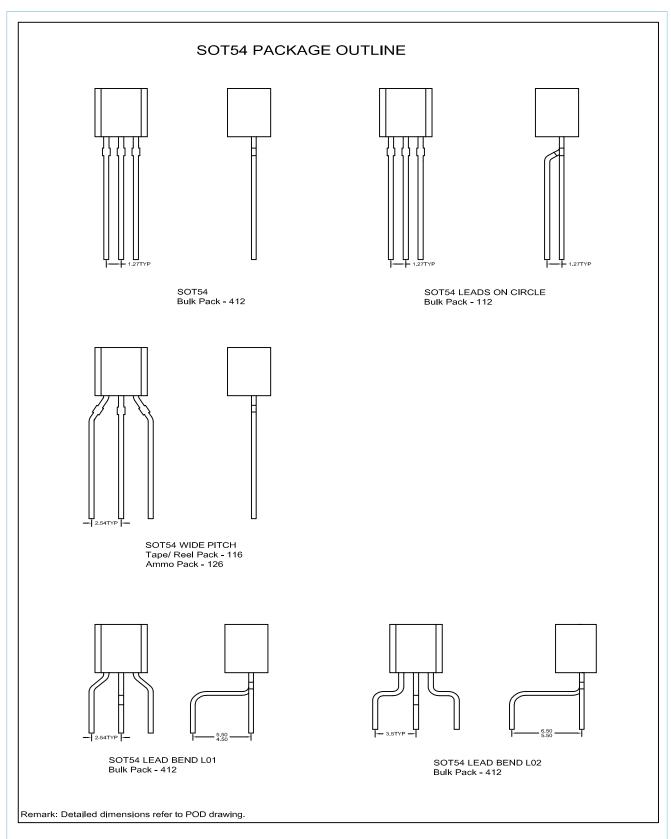


Fig. 12. Critical rate of rise of off-state voltage as a function of junction temperature; typical values

10. Package outline



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11. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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