

1. General description

Planar passivated SCR with sensitive gate in a SOT223 surface mountable plastic package. This SCR is designed to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

2. Features and benefits

- Sensitive gate
- Planar passivated for voltage ruggedness and reliability
- Direct triggering from low power drivers and logic ICs
- Surface mountable package

3. Applications

- Circuit breakers
- RCD/GFI/LCCB applications

4. Quick reference data

Table 1. Qui	ck reference data					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{RRM}	repetitive peak reverse voltage		-	-	600	V
I _{T(AV)}	average on-state current	half sine wave; T _{sp} ≤ 112 °C; <u>Fig. 1</u>	-	-	0.63	A
I _{T(RMS)}	RMS on-state current	half sine wave; T _{sp} ≤ 112 °C; <u>Fig. 2;</u> <u>Fig. 3</u>	-	-	1	A
I _{TSM}	non-repetitive peak on- state current	half sine wave; $T_{j(init)} = 25 \text{ °C}$; $t_p = 10 \text{ ms}$; Fig. 4; Fig. 5	-	-	8	A
		half sine wave; T _{j(init)} = 25 °C; t _p = 8.3 ms	-	-	9	A
Tj	junction temperature		-	-	125	°C
Static chara	acteristics					
I _{GT}	gate trigger current	V _D = 12 V; I _T = 10 mA; T _j = 25 °C; <u>Fig. 9</u>	20	50	200	μA
Dynamic ch	naracteristics					
dV _D /dt	rate of rise of off-state voltage	V_{DM} = 402 V; T _j = 125 °C; R _{GK} = 1 kΩ; (V_{DM} = 67% of V_{DRM}); exponential waveform; Fig. 14	500	800	-	V/µs

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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
		V_{DM} = 402 V; T _j = 125 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit; Fig. 14	-	25	-	V/µs

5. Pinning information

Table 2.	Pinning in	formation		
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	К	cathode	4	А - Д К
2	А	anode		Ğ sym037
3	G	gate		symosi
4	mb	mb; connected to anode	☐1	

6. Ordering information

Table 3. Ordering infor	mation					
Type number	Package					
	Name	Description	Version			
BT168GW	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223			

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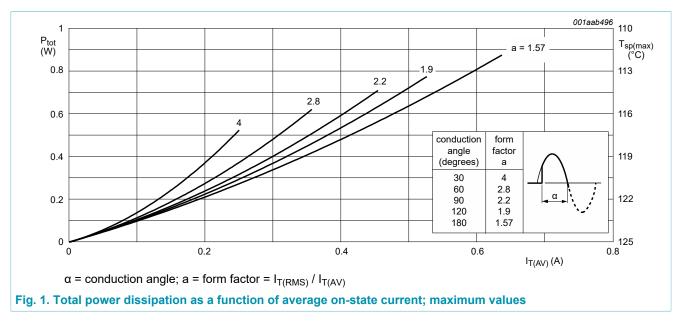
7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

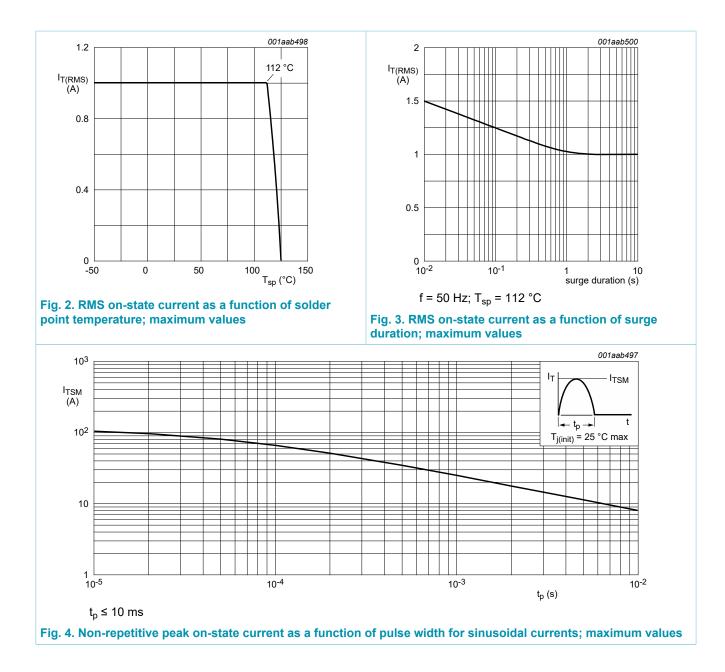
Symbol	Parameter	Conditions		Min	Max	Unit
V _{DRM}	repetitive peak off-state voltage		[1]	-	600	V
V _{RRM}	repetitive peak reverse voltage			-	600	V
I _{T(AV)}	average on-state current	half sine wave; T _{sp} ≤ 112 °C; <u>Fig. 1</u>		-	0.63	А
I _{T(RMS)}	RMS on-state current	half sine wave; T _{sp} ≤ 112 °C; <u>Fig. 2</u> ; <u>Fig. 3</u>		-	1	А
I _{TSM}	non-repetitive peak on- state current	half sine wave; $T_{j(init)}$ = 25 °C; t_p = 10 ms; Fig. 4; Fig. 5		-	8	A
		half sine wave; T _{j(init)} = 25 °C; t _p = 8.3 ms		-	9	А
l ² t	I ² t for fusing	t _p = 10 ms; SIN		-	0.32	A²s
dl _T /dt	rate of rise of on-state current	I_T = 2 A; I_G = 10 mA; dI_G/dt = 100 mA/µs		-	50	A/µs
I _{GM}	peak gate current			-	1	А
V _{RGM}	peak reverse gate voltage			-	5	V
P _{GM}	peak gate power			-	2	W
P _{G(AV)}	average gate power	over any 20 ms period		-	0.1	W
T _{stg}	storage temperature			-40	150	°C
Tj	junction temperature			-	125	°C

[1] Although not recommended, off-state voltages up to 800 V may be applied without damage, but the thyristor may switch to the onstate.



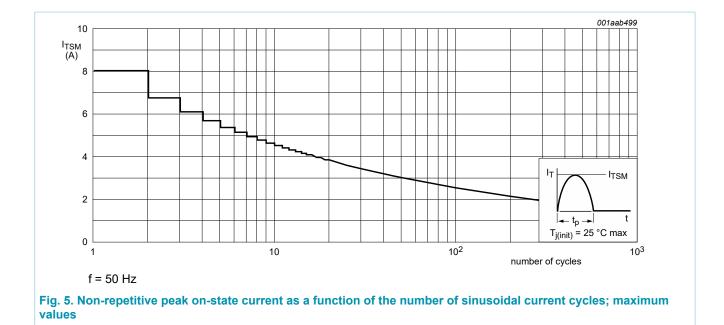
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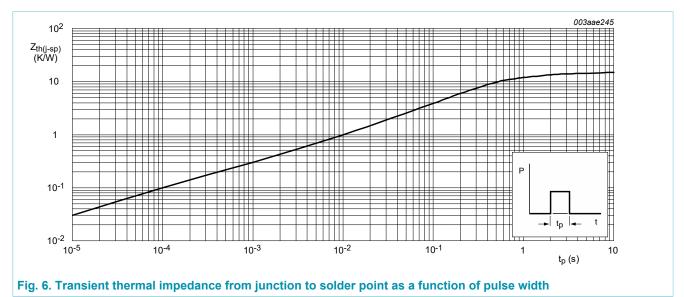
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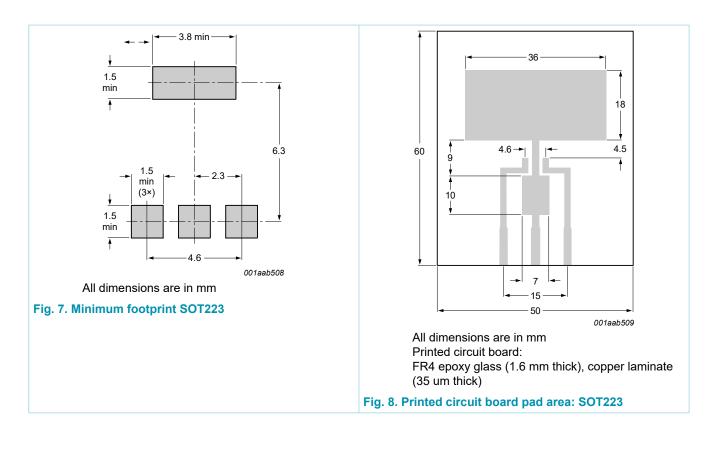
8. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-sp)}	thermal resistance from junction to solder point	Fig. 6	-	-	15	K/W
R _{th(j-a)}	thermal resistance from junction to ambient free air	printed circuit board mounted; minimum footprint; Fig. 7	-	156	-	K/W
		printed circuit board mounted; pad area; <u>Fig. 8</u>	-	70	-	K/W



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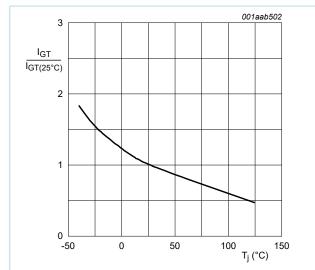
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9. Characteristics

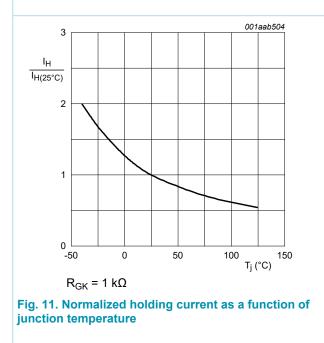
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
I _{GT}	gate trigger current	V _D = 12 V; I _T = 10 mA; T _j = 25 °C; Fig. 9	20	50	200	μA
IL	latching current	V_D = 12 V; I _G = 0.5 mA; T _j = 25 °C; R _{GK(ext)} = 1 kΩ; Fig. 10	-	2	6	mA
I _H	holding current	V_D = 12 V; T _j = 25 °C; R _{GK(ext)} = 1 kΩ; Fig. 11	-	2	5	mA
V _T	on-state voltage	I _T = 1.2 A; T _j = 25 °C; <u>Fig. 12</u>	-	1.25	1.7	V
V _{GT}	gate trigger voltage	V _D = 12 V; I _T = 10 mA; T _j = 25 °C; Fig. 13	-	0.5	0.8	V
		V _D = 600 V; I _T = 10 mA; T _j = 125 °C	0.2	0.3	-	V
I _D	off-state current	V_D = 600 V; $R_{GK(ext)}$ = 1 k Ω ; T_j = 125 °C	-	0.05	0.1	mA
I _R	reverse current	V_R = 600 V; T _j = 125 °C; R _{GK(ext)} = 1 k Ω	-	0.05	0.1	mA
Dynamic ch	aracteristics					
dV _D /dt	rate of rise of off-state voltage	$ V_{DM} = 402 \text{ V}; \text{T}_{j} = 125 ^{\circ}\text{C}; \text{R}_{GK} = 1 \text{k}\Omega; \\ (\text{V}_{DM} = 67\% \text{ of } \text{V}_{DRM}); \text{ exponential} \\ \text{waveform}; \overline{\text{Fig. } 14} $	500	800	-	V/µs
		V_{DM} = 402 V; T _j = 125 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit; Fig. 14	-	25	-	V/µs
t _{gt}	gate-controlled turn-on time	$\begin{split} I_{TM} &= 2 \text{ A}; V_D = 600 \text{V}; I_G = 10 \text{mA}; \text{d} \text{I}_G \text{/} \\ \text{d} t &= 0.1 \text{A} / \mu \text{s}; \text{T}_j = 25 ^\circ \text{C} \end{split}$	-	2	-	μs
t _q	commutated turn-off time		-	100	-	μs

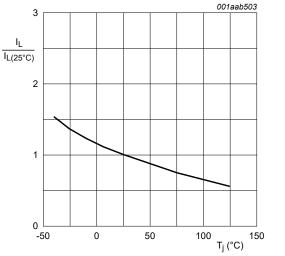
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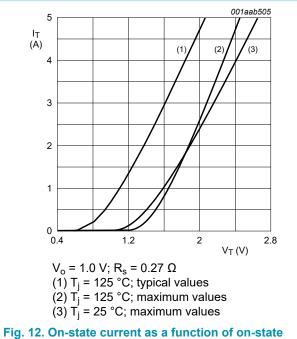








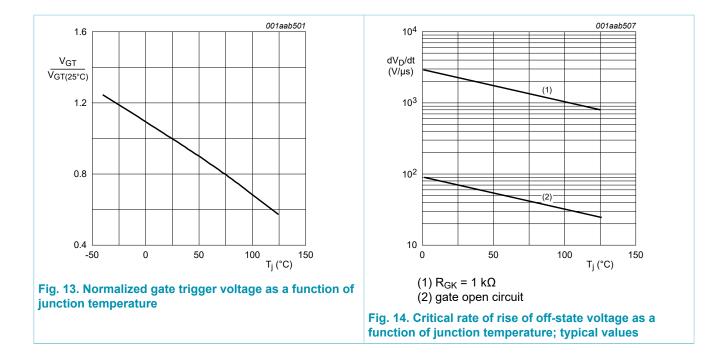




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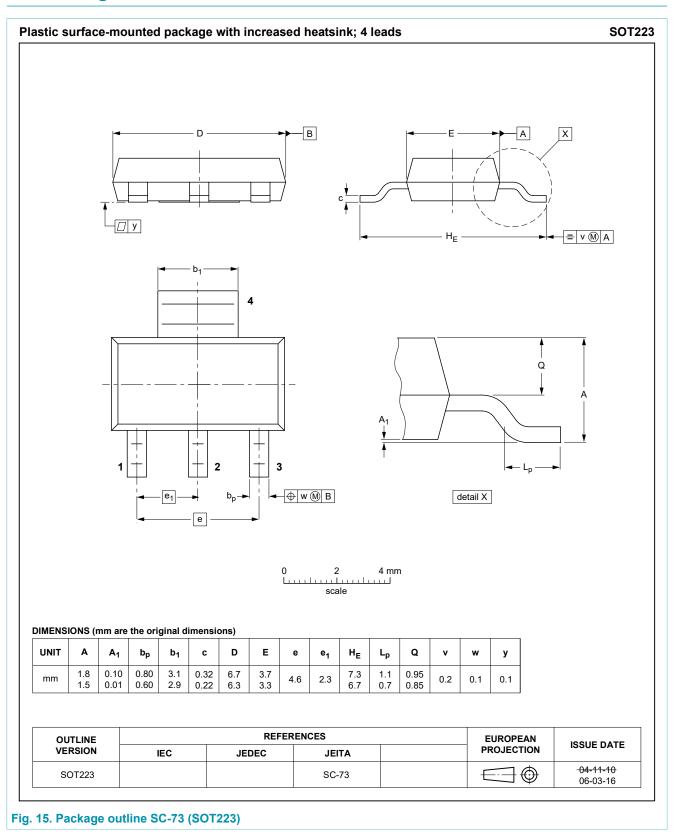
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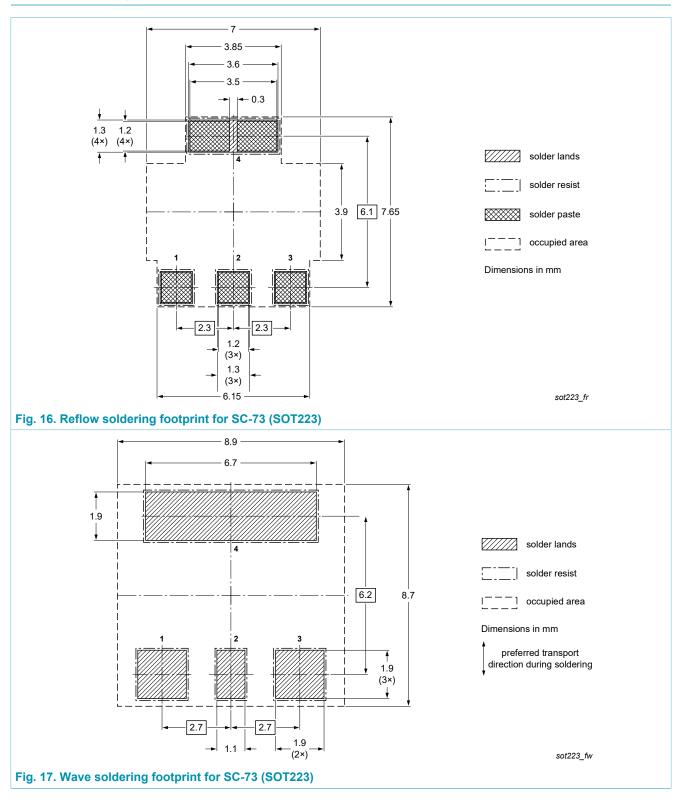
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10. Package outline



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11. Soldering



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12. Legal information

Data sheet status

Document status [1][2]	Product status [<u>3]</u>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

- [2] The term 'short data sheet' is explained in section "Definitions".
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