

1. General description

AC Thyristor Triac power switch in a SOT404 (D2PAK) surface mountable plastic package with self-protective clamping capabilities against low and high energy transients. This "series CTN" triac will commute the full RMS current at the maximum rated junction temperature ($T_{j(max)} = 150\text{ °C}$) without the aid of a snubber. It is used in applications where "high junction operating temperature capability" is required.

2. Features and benefits

- Clamping structure ensuring safe high over-voltage withstand capability
- High junction operating temperature capability ($T_{j(max)} = 150\text{ °C}$)
- High minimum IGT for guaranteed immunity to gate noise
- Full cycle AC conduction
- Over-voltage withstand capability to IEC 61000-4-5
- Pin compatible with standard triacs
- Planar passivated for voltage ruggedness and reliability
- Protective self turn-on capability for high energy transients
- Safe clamping capability for low energy over-voltage transients
- Less sensitive gate for high noise immunity
- Surface mountable package
- Triggering in three quadrants only
- Very high immunity to false turn-on by dV/dt and IEC 61000-4-4 fast transient
- Package meets UL94V0 flammability requirement
- Package is RoHS compliant

3. Applications

- AC fan, pump and compressor controls
- Highly inductive, resistive and safety loads
- Large and small appliances (White Goods)
- Reversing induction motor controls
- Applications subject to high temperature ($T_{j(max)} = 150\text{ °C}$)

4. Quick reference data

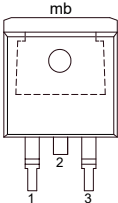
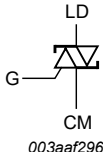
Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------|-----------------------------------|--|-----|-----|-----|------|
| V_{DRM} | repetitive peak off-state voltage | | - | - | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{mb} \leq 121\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3 | - | - | 12 | A |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|---------------------------------------|--|------|-----|-----|--------------------|
| I_{TSM} | non-repetitive peak on-state current | full sine wave; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5 | - | - | 120 | A |
| | | full sine wave; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$; $t_p = 16.7\text{ ms}$ | - | - | 132 | A |
| T_j | junction temperature | | - | - | 150 | $^{\circ}\text{C}$ |
| V_{PP} | peak pulse voltage | $T_j = 25\text{ }^{\circ}\text{C}$; non-repetitive, off-state; Fig. 6 | - | - | 2 | kV |
| Static characteristics | | | | | | |
| I_{GT} | gate trigger current | $V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD+ G+; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 8 | 5 | - | 35 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD+ G-; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 8 | 5 | - | 35 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD- G-; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 8 | 5 | - | 35 | mA |
| I_H | holding current | $V_D = 12\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 10 | - | - | 30 | mA |
| V_T | on-state voltage | $I_T = 17\text{ A}$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 11 | - | - | 1.5 | V |
| V_{CL} | clamping voltage | $I_{CL} = 0.1\text{ mA}$; $t_p = 1\text{ ms}$; $T_j = 25\text{ }^{\circ}\text{C}$ | 850 | - | - | V |
| Dynamic characteristics | | | | | | |
| dV_D/dt | rate of rise of off-state voltage | $V_{DM} = 536\text{ V}$; $T_j = 125\text{ }^{\circ}\text{C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit | 4000 | - | - | V/ μs |
| | | $V_{DM} = 536\text{ V}$; $T_j = 150\text{ }^{\circ}\text{C}$; exponential waveform; gate open circuit | 2000 | - | - | V/ μs |
| dI_{com}/dt | rate of change of commutating current | $V_D = 400\text{ V}$; $T_j = 150\text{ }^{\circ}\text{C}$; $I_{T(RMS)} = 12\text{ A}$; $dV_{com}/dt = 20\text{ V}/\mu\text{s}$; gate open circuit; snubberless condition | 12 | - | - | A/ms |
| | | $V_D = 400\text{ V}$; $T_j = 150\text{ }^{\circ}\text{C}$; $I_{T(RMS)} = 12\text{ A}$; $dV_{com}/dt = 10\text{ V}/\mu\text{s}$; gate open circuit | 15 | - | - | A/ms |
| | | $V_D = 400\text{ V}$; $T_j = 150\text{ }^{\circ}\text{C}$; $I_{T(RMS)} = 8\text{ A}$; $dV_{com}/dt = 1\text{ V}/\mu\text{s}$; gate open circuit | 20 | - | - | A/ms |

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|---------------------|--|--|
| 1 | CM | common |  <p>D2PAK (SOT404)</p> |  <p>003aaf296</p> |
| 2 | LD | load | | |
| 3 | G | gate | | |
| mb | LD | mounting base; load | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|----------------|---------|--|---------|
| | Name | Description | Version |
| ACTT12B-800CTN | D2PAK | plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) | SOT404 |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---------------------|--------------------------------------|---|-----|-----|------------------------|
| V_{DRM} | repetitive peak off-state voltage | | - | 800 | V |
| $I_{\text{T(RMS)}}$ | RMS on-state current | full sine wave; $T_{\text{mb}} \leq 121\text{ }^{\circ}\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3 | - | 12 | A |
| I_{TSM} | non-repetitive peak on-state current | full sine wave; $T_{\text{j(init)}} = 25\text{ }^{\circ}\text{C}$; $t_{\text{p}} = 20\text{ ms}$; Fig. 4 ; Fig. 5 | - | 120 | A |
| | | full sine wave; $T_{\text{j(init)}} = 25\text{ }^{\circ}\text{C}$; $t_{\text{p}} = 16.7\text{ ms}$ | - | 132 | A |
| I^2t | I^2t for fusing | $t_{\text{p}} = 10\text{ ms}$; sine-wave pulse | - | 72 | A^2s |
| di_{T}/dt | rate of rise of on-state current | $I_{\text{G}} = 70\text{ mA}$ | - | 100 | $\text{A}/\mu\text{s}$ |
| I_{GM} | peak gate current | $t = 20\text{ }\mu\text{s}$ | - | 2 | A |
| P_{GM} | peak gate power | | - | 5 | W |
| $P_{\text{G(AV)}}$ | average gate power | over any 20 ms period | - | 0.5 | W |
| T_{stg} | storage temperature | | -40 | 150 | $^{\circ}\text{C}$ |
| T_{j} | junction temperature | | - | 150 | $^{\circ}\text{C}$ |
| V_{PP} | peak pulse voltage | $T_{\text{j}} = 25\text{ }^{\circ}\text{C}$; non-repetitive, off-state; Fig. 6 | - | 2 | kV |

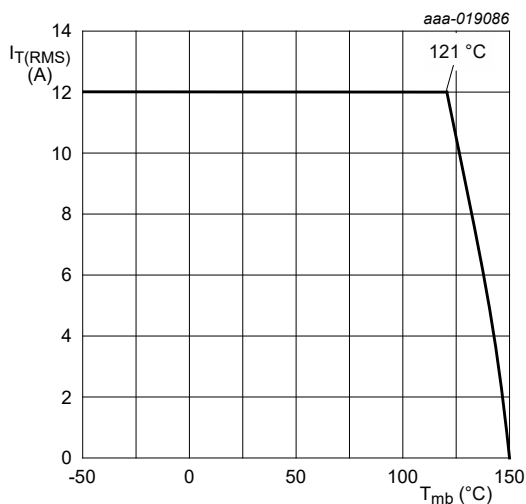
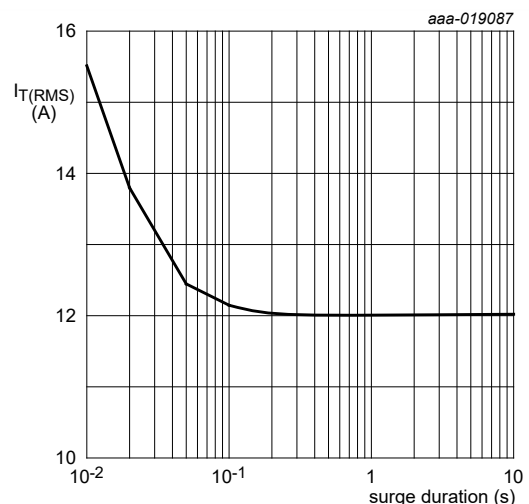


Fig. 1. RMS on-state current as a function of mounting base temperature; maximum values



$f = 50\text{ Hz}$; $T_{\text{mb}} = 121\text{ }^{\circ}\text{C}$

Fig. 2. RMS on-state current as a function of surge duration; maximum values

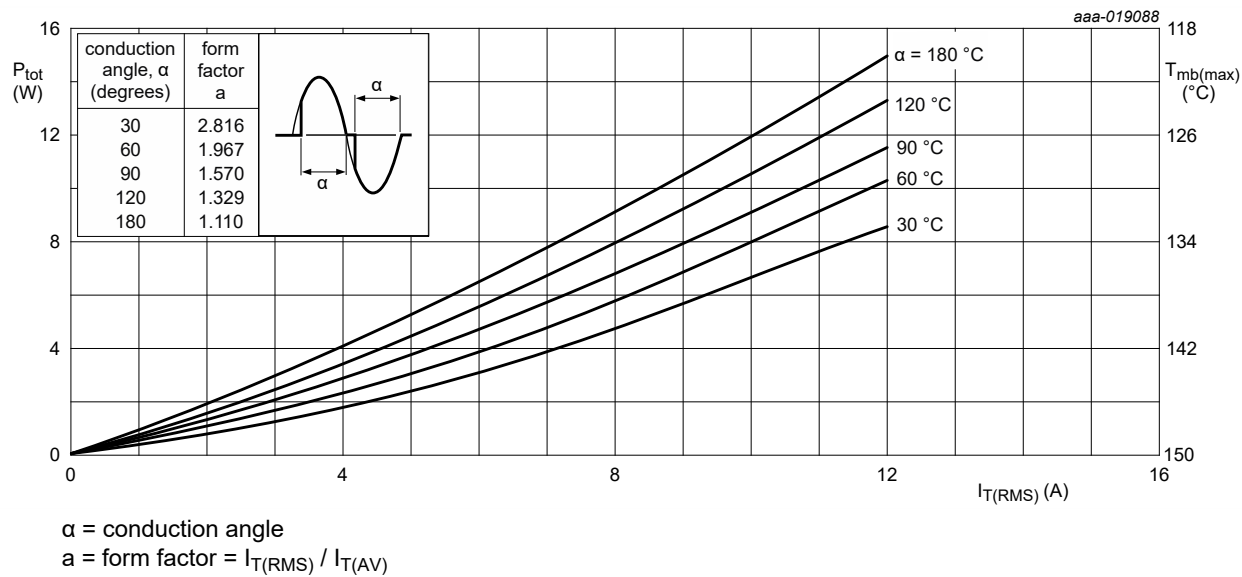


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

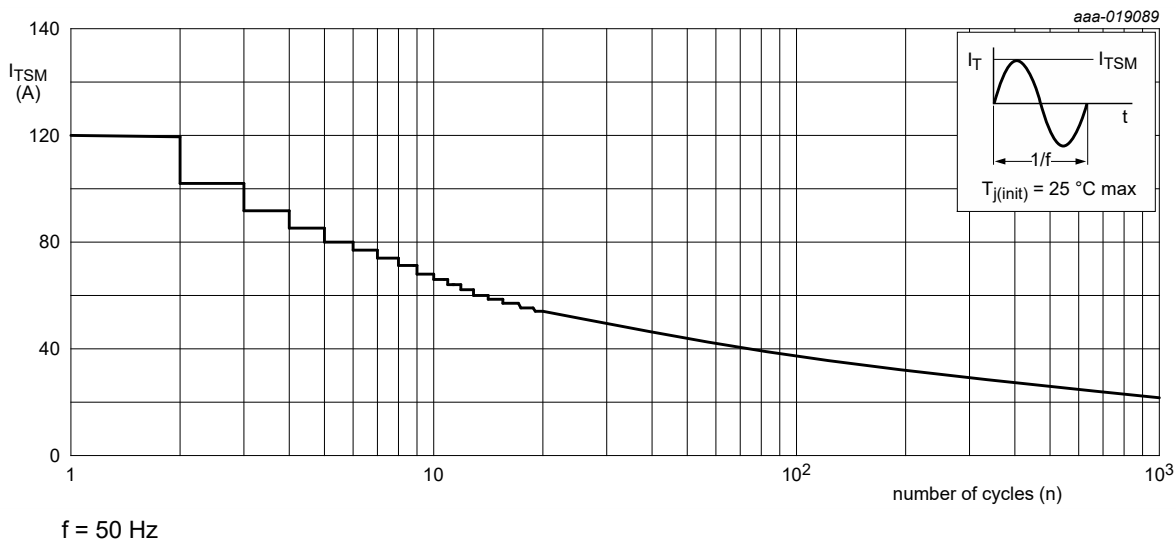


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

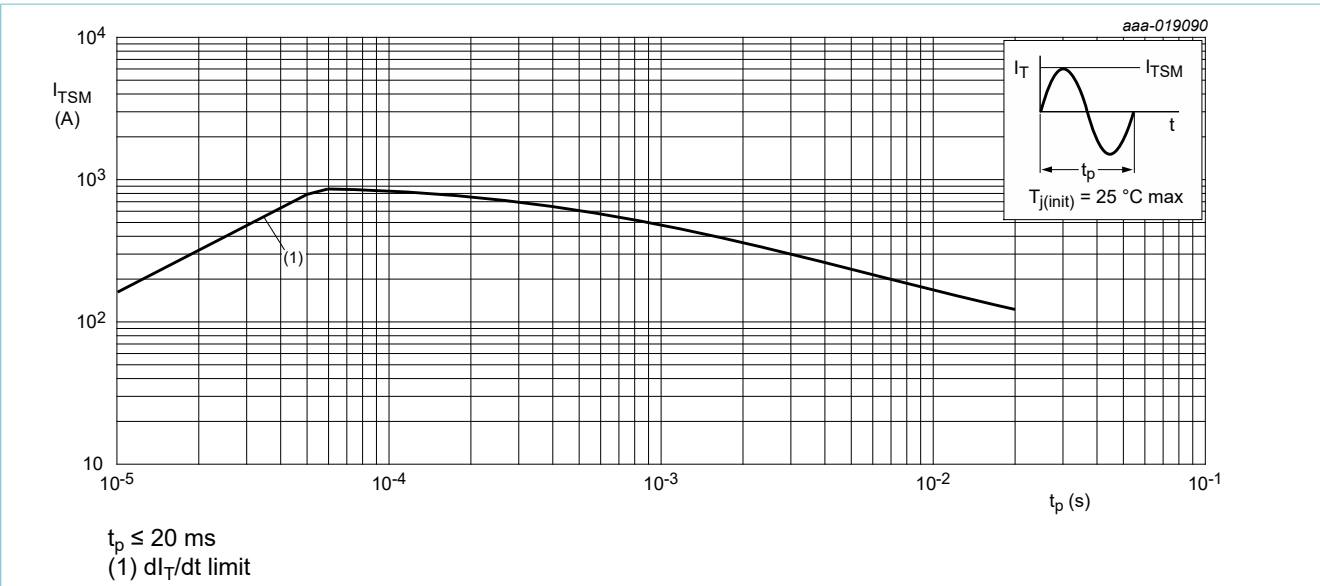


Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

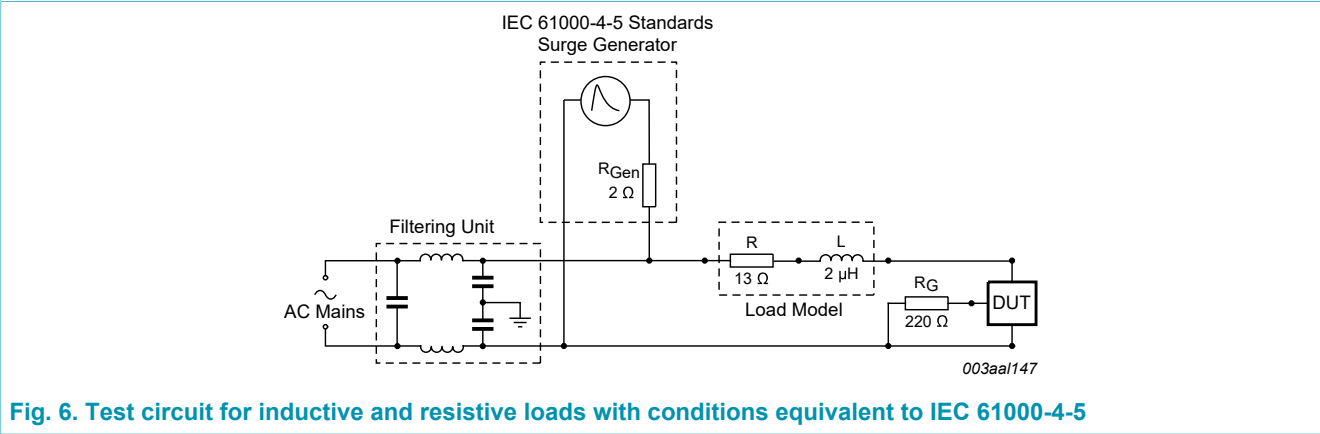


Fig. 6. Test circuit for inductive and resistive loads with conditions equivalent to IEC 61000-4-5

8. Thermal characteristics

Table 5. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|--|--|-----|-----|-----|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | full cycle; Fig. 7 | - | - | 2 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient free air | in free air; printed circuit board (FR4) mounted | - | 55 | - | K/W |

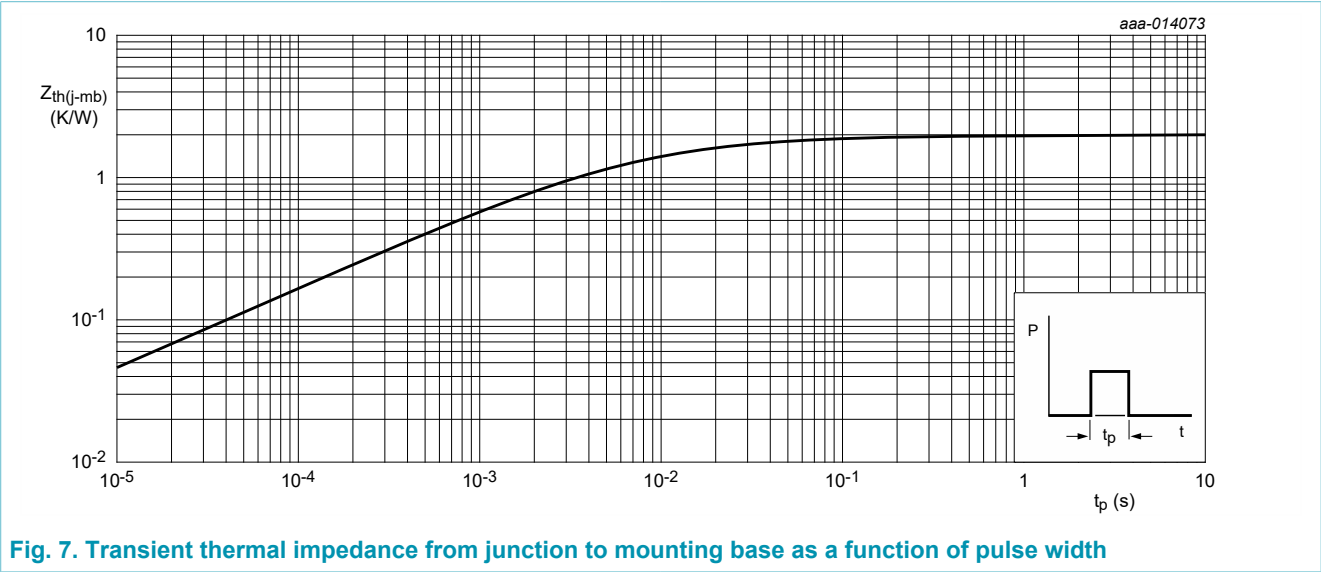
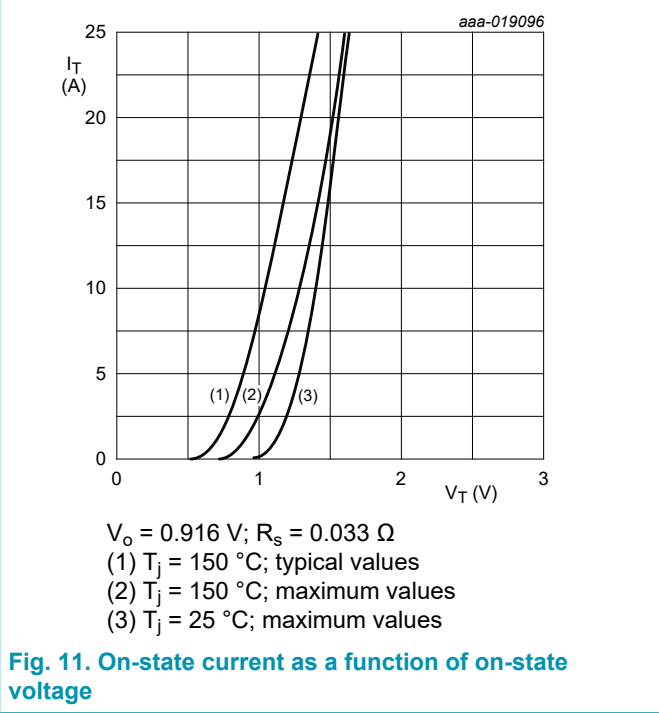
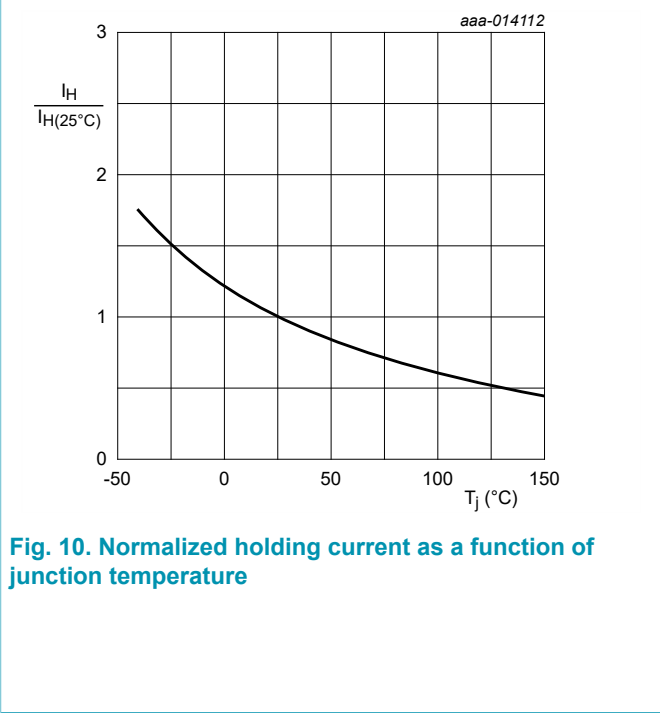
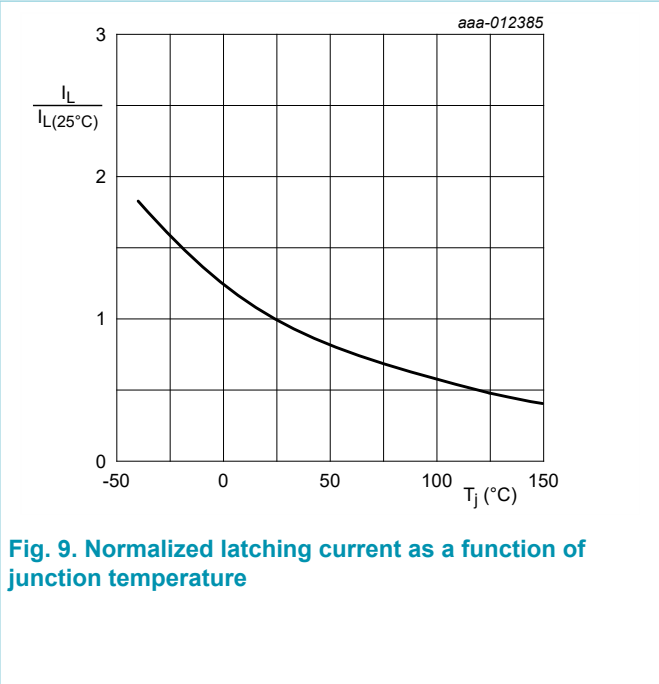
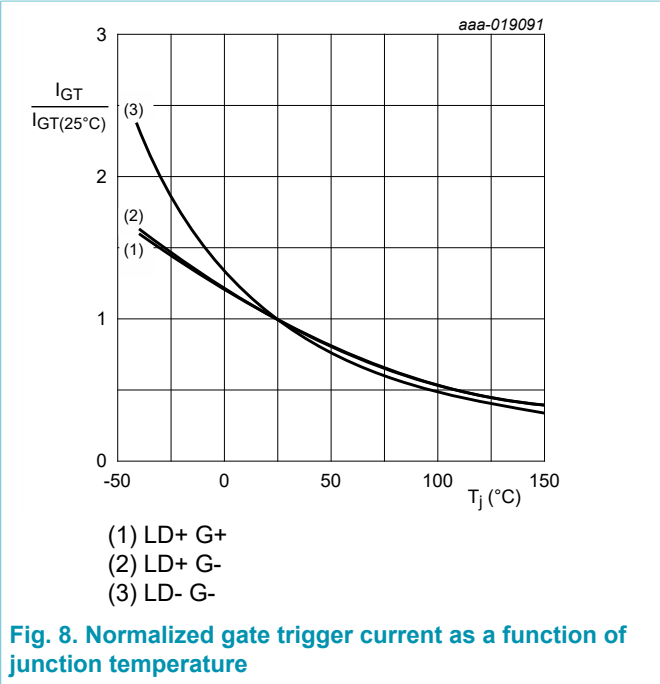


Fig. 7. Transient thermal impedance from junction to mounting base as a function of pulse width

9. Characteristics

Table 6. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|---------------------------------------|--|------|------|-----|------------------|
| Static characteristics | | | | | | |
| I_{GT} | gate trigger current | $V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD+ G+; $T_j = 25\text{ °C}$; Fig. 8 | 5 | - | 35 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD+ G-; $T_j = 25\text{ °C}$; Fig. 8 | 5 | - | 35 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD- G-; $T_j = 25\text{ °C}$; Fig. 8 | 5 | - | 35 | mA |
| I_L | latching current | $V_D = 12\text{ V}$; $I_G = 100\text{ mA}$; LD+ G+; $T_j = 25\text{ °C}$; Fig. 9 | - | - | 40 | mA |
| | | $V_D = 12\text{ V}$; $I_G = 100\text{ mA}$; LD+ G-; $T_j = 25\text{ °C}$; Fig. 9 | - | - | 60 | mA |
| | | $V_D = 12\text{ V}$; $I_G = 100\text{ mA}$; LD- G-; $T_j = 25\text{ °C}$; Fig. 9 | - | - | 40 | mA |
| I_H | holding current | $V_D = 12\text{ V}$; $T_j = 25\text{ °C}$; Fig. 10 | - | - | 30 | mA |
| V_T | on-state voltage | $I_T = 17\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11 | - | - | 1.5 | V |
| V_{GT} | gate trigger voltage | $V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; $T_j = 25\text{ °C}$; Fig. 12 | - | 0.8 | 1 | V |
| | | $V_D = 400\text{ V}$; $I_T = 100\text{ mA}$; $T_j = 150\text{ °C}$; Fig. 12 | 0.2 | 0.45 | - | V |
| I_D | off-state current | $V_D = 800\text{ V}$; $T_j = 25\text{ °C}$ | - | - | 10 | μA |
| | | $V_D = 800\text{ V}$; $T_j = 150\text{ °C}$ | - | - | 2 | mA |
| V_{CL} | clamping voltage | $I_{CL} = 0.1\text{ mA}$; $t_p = 1\text{ ms}$; $T_j = 25\text{ °C}$ | 850 | - | - | V |
| Dynamic characteristics | | | | | | |
| dV_D/dt | rate of rise of off-state voltage | $V_{DM} = 536\text{ V}$; $T_j = 125\text{ °C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit | 4000 | - | - | V/ μs |
| | | $V_{DM} = 536\text{ V}$; $T_j = 150\text{ °C}$; exponnetial waveform; gate open circuit | 2000 | - | - | V/ μs |
| di_{com}/dt | rate of change of commutating current | $V_D = 400\text{ V}$; $T_j = 150\text{ °C}$; $I_{T(RMS)} = 12\text{ A}$; $dV_{com}/dt = 20\text{ V}/\mu\text{s}$; gate open circuit; snubberless condition | 12 | - | - | A/ms |
| | | $V_D = 400\text{ V}$; $T_j = 150\text{ °C}$; $I_{T(RMS)} = 12\text{ A}$; $dV_{com}/dt = 10\text{ V}/\mu\text{s}$; gate open circuit | 15 | - | - | A/ms |
| | | $V_D = 400\text{ V}$; $T_j = 150\text{ °C}$; $I_{T(RMS)} = 8\text{ A}$; $dV_{com}/dt = 1\text{ V}/\mu\text{s}$; gate open circuit | 20 | - | - | A/ms |



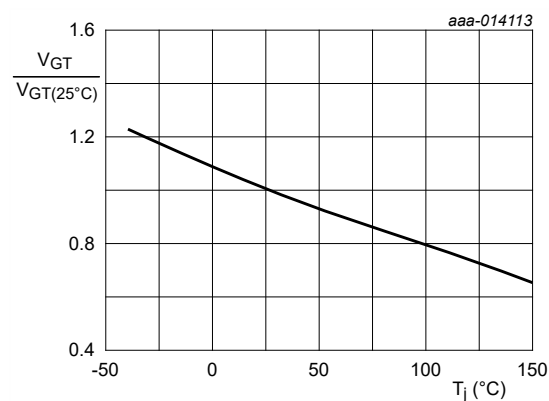


Fig. 12. Normalized gate trigger voltage as a function of junction temperature

10. Package outline

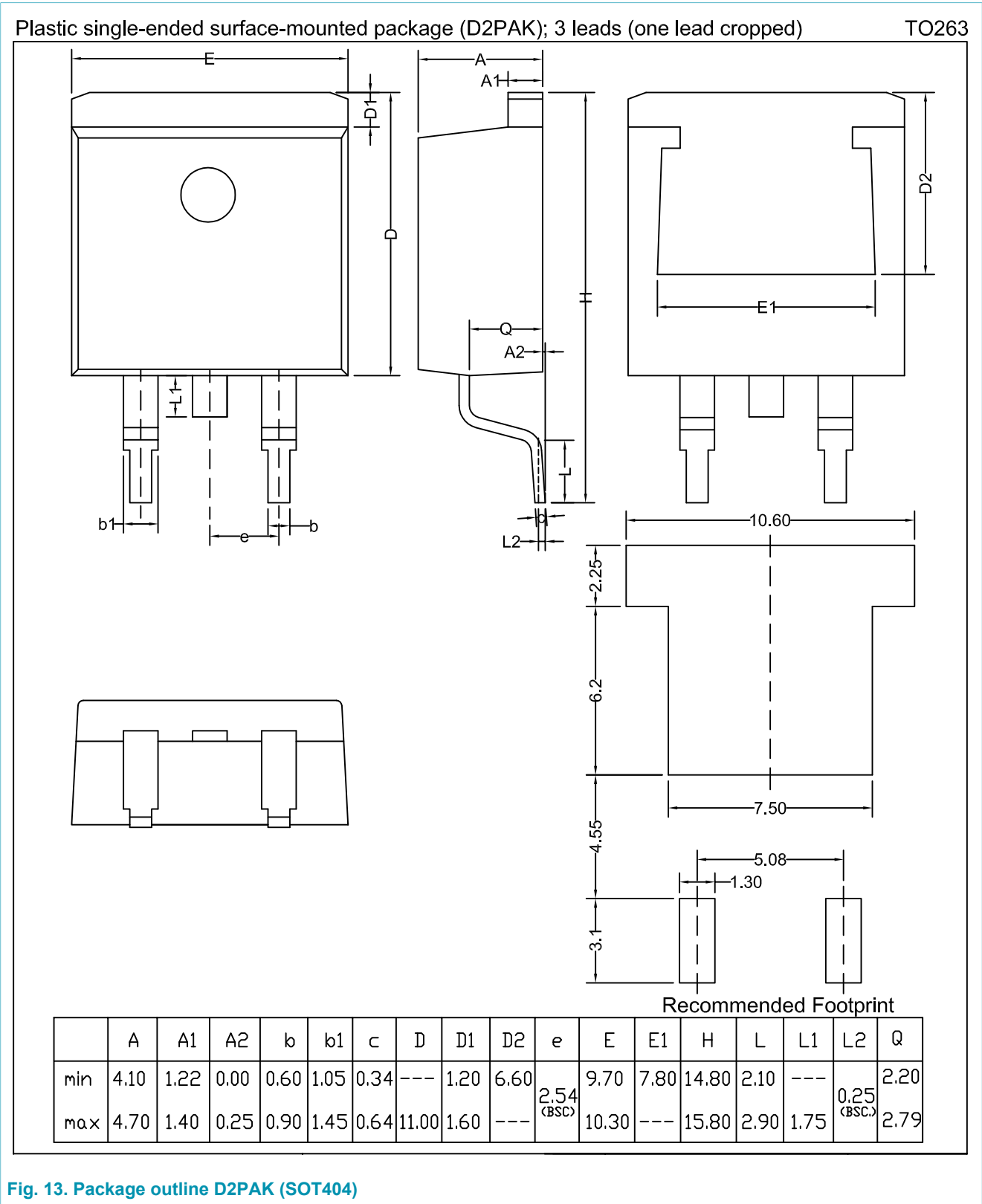


Fig. 13. Package outline D2PAK (SOT404)

11. Legal information

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| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
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| Product [short] data sheet | Production | This document contains the product specification. |

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- [2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 20 August 2018

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