Product Document

Published by
ams OSRAM Group

Datasheet

DS001047

AS7331

Spectral UVA/B/C Sensor

v4-00 • 2023-Mar-24

Content Guide

1 General Description

The AS7331 is a low-power, low noise integrated UV sensor. The three separated UVA, UVB and UVC channels convert optical radiation signals via photodiodes to a digital result and realize a continuous or triggered measurement. The irradiance responsivity can be adjusted via Gain, conversion time and internal clock frequency to effect sensitivity, full scale range and LSB. The by the AS7331 detected amount of radiation in the set Gain and conversion time configuration will be provided as digital counts by the AS7331. The AS7331 offers a range of 12 Gain steps by a factor of two for each step. The conversion time is internally controlled over a wide range of 15 steps by a factor of two for each step. With the input pin (SYN), the conversion time can be externally controlled to adapt the measurement to the given environment and time base.

With its irradiance responsivity factor and conversion time, the AS7331 supports an overall huge dynamic range up to 3.43E+10 (resolution multiplied by gain range). It achieves an accuracy of up to 24-bit signal resolution (internal via I²C and shifter 16-bit), with an irradiance responsivity per count down to 2.38 nW/cm² at 64 ms integration time. Via an integrated divider, the 16-bit I²C output can be adjusted to the significant bits of interest.

Equation 1:

$$Dynamic\ Range = \frac{MAX\ measureable\ value\ = Max.Full\ Scale\ Range}{MIN\ measureable\ value = Min.Least\ Significant\ Bit}$$

Automatic power down (sleep function) between subsequent measurements offers operation with very low current consumption. Furthermore, a synchronized mode and other control modes adjustable by user programming can be used. The supported operating modes of the AS7331 are:

- CMD Mode – Single measurement and conversion (controlled via I²C interface).
- CONT Mode – Continuous measurement and conversion (periodically recurring measuring cycles) start and stop controlled via I²C interface.
- SYN[x] Modes – Synchronized measurement and conversion:
  - [SYNS Mode] synchronization of start via the control signal at pin SYN.
  - [SYND Mode] synchronization of start and stop of measuring cycles via control signal at pin SYN.

The conversion data can be accessed by the I²C interface with programmable slave addresses via 16- bit / 400 kHz fast mode. The measurement of the current conversion time for an externally triggered measurement can be performed. The measurement modes will not affect the settings of the irradiance responsivity and conversion time. Furthermore, the converter supports functions like power down and standby, which is suitable in mobile applications. Based on the high flexibility, the AS7331 is suitable as an optical converter for three different wavelength ranges. The device achieves a high dynamic range for fluorescence applications and for measurements of UV radiations. This makes the UV sensors excellently suited for photometry applications (UV exposure, UV-index), for monitoring of UVC disinfection treatments, fluorescence detection, and mobile devices for UV radiation measurements. The AS7331 contains an integrated temperature sensor for rough compensation of the thermic behavior. The device is available in a small SMD package.

1.1 Key Benefits and Features

The benefits and features of AS7331, Spectral UVA/B/C Sensor are listed below:

Figure 1:
Added Value of Using AS7331

Benefits	Features
Separated UVA, UVB and UVC radiation measurements	Three separated UV detectors with interference filter technology
UV-radiation measurements from low to high radiation conditions	High dynamic range up to 3.43E+10 (16…24-Bit ADC)
Usable for fluorescence light conditions	High sensitivity up to 421 counts/(µW/cm²) in UVA, Smallest LSB 2.38 nW/cm² (at 64 ms integration time).
Up to four AS7331 sensors on the same I²C bus in parallel	Adjustable I²C addresses
Mobile applications	Low-power operation, Power-on Reset, Power-down and standby, small OLGA package
Temperature compensation of measurement results	Integrated temperature sensor

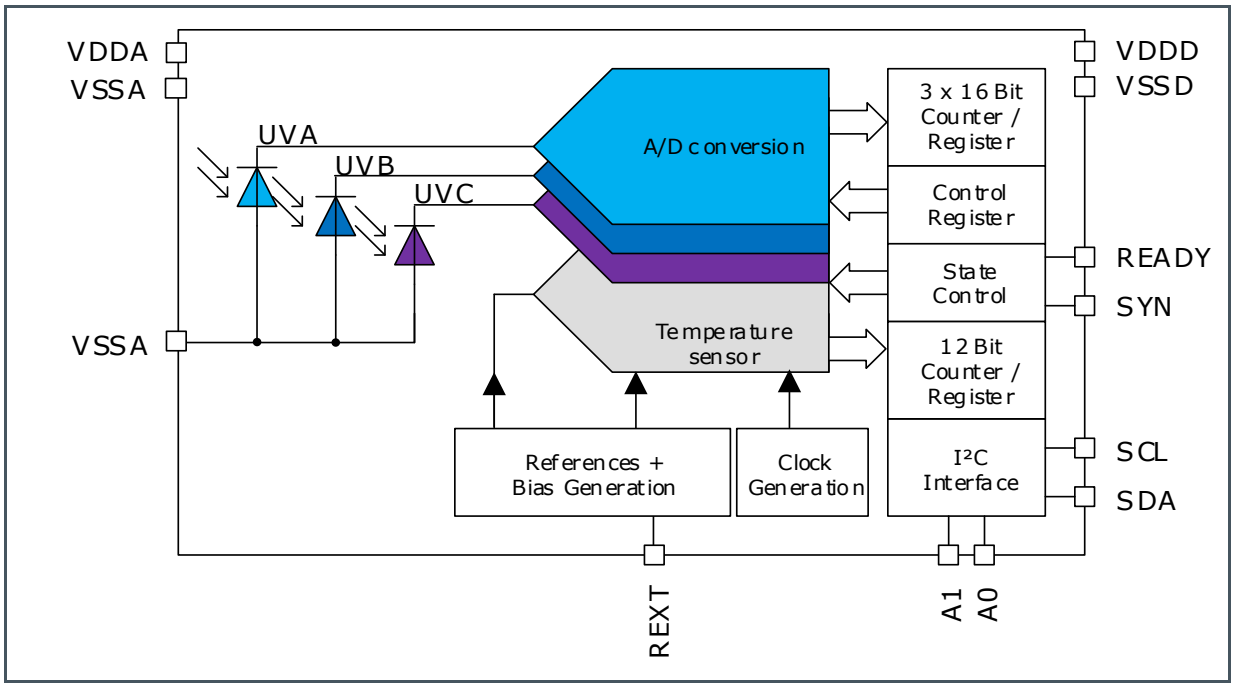
1.2 Applications

- UV-Disinfection (water, air, surfaces)
- UV-Curing
- Phototherapy
- Analytics
- Home Appliances
- Horticulture

1.3 Block Diagram

Figure 2 shows the main components of the AS7331. The photodiodes convert the incoming radiation to a photocurrent and with a subsequent current-to-digital converter to digital data. An internal reference generator provides all the necessary references for the A/D conversion and the photodiodes by using an external resistor R_{EXT} at pin REXT. The results of the A/D conversion are stored in three 16-bit registers and can be accessed via the I²C interface. For the externally triggered start or start and stop of the measurement, the input pin SYN can be used. The output READY reflects the status of the conversion. The internal temperature sensor delivers the on-chip temperature, stored as a 12-bit value in a 16-bit register, which can be accessed via the I²C interface as well. The pins A0 and A1 set the I²C slave address. Separated analog and digital power supply and ground pins reduce noise coupling.

Figure 2:
Functional Blocks of the AS7331



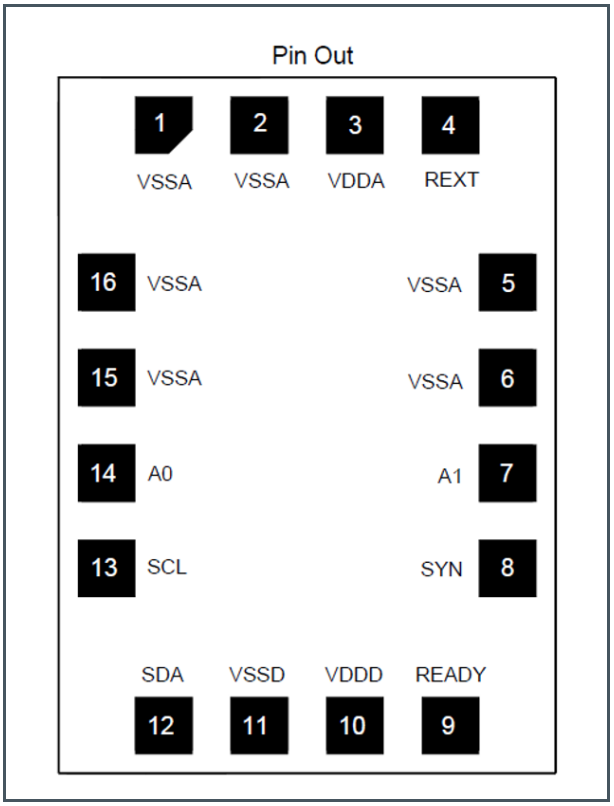
2 Ordering Information

Ordering Code	Package	Marking	Delivery Form	Delivery Quantity
AS7331-AQFM	OLGA16	AS7331	Tape & Reel	1000 pcs/reel
AS7331-AQFT	OLGA16	AS7331	Tape & Reel	5000 pcs/reel

3 Pin Assignment

3.1 Pin Diagram

Figure 3:
AS7331 Pin Diagram



3.2 Pin Description

Figure 4:
Pin Description of the AS7331

Pin Number	Pin Name	Pin Type(1)	Description
1, 2	VSSA	P	Analog ground.
3	VDDA	P	Analog power supply.
4	REXT	A_I/O	External reference resistor.
5, 6	VSSA	P	Analog ground.

Pin Number	Pin Name	Pin Type(1)	Description
7	A1	DI	Variable I²C slave address bit 1.
8	SYN	DI	Input for external controlled conversion.
9	READY	DO	Conversion status, configurable as push pull or open drain output stage (default push pull).
10	VDDD	P	Digital power supply.
11	VSSD	P	Digital ground.
12	SDA	D_I/O_OD	I²C data input / output, open drain output stage.
13	SCL	DI	I²C clock input.
14	A0	DI	Variable I²C slave address bit 0.
15, 16	VSSA	P	Analog ground.

(1) **Explanation of abbreviations**:

DI	Digital Input
DO	Digital Output
P	Power pin
A_I/O	Analog in-/output
D_I/O_OD	Digital in-/output, open drain

4 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings of the AS7331

Symbol	Parameter	Min	Max	Unit	Comments
Electrical Parameters					
V_{DD}	Maximum power supply voltage range	-0.5	5	V	V_{DDA} and V_{DDD}
$DIFF_{VDD}$	Supply voltage difference	-0.3	0.3	V	V_{DDA} - V_{DDD}
	Input and output voltages	-0.5	V_{DD}+0.5	V	A0, A1, SCL, SDA, SYN, READY
Electrostatic Discharge					
ESD_{HBM}	Electrostatic discharge HBM		±750	V	JS-001-2017
ESD_{CDM}	Electrostatic discharge CDM		±500	V	JS-002-2018
Optical Parameters					
α_I	Angle of incidence	-10	10	°	
Temperature Ranges and Storage Conditions					
T_A	Operating ambient temperature	-40	85	°C	
T_{STRG}	Storage temperature range	-40	85	°C	
T_{BODY}	Package body temperature		260	°C	IPC/JEDEC J-STD-020(1)
RH_{NC}	Relative humidity (non-condensing)	5	85	%	
MSL	Moisture sensitivity level		3		Maximum floor life time of 168h

(1) The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.” The lead finish for Pb-free leaded packages is “Matte Tin” (100 % Sn).

5 Electrical Characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods. All voltages are with respect to ground (GND). Device parameters are guaranteed at V_{DD} = 3.3 V and T_A = 25 °C unless otherwise noted.

Figure 6:
Electrical Characteristics of the AS7331

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Operating Power Supply Voltage	VDDA and VDDD	2.7	3.3	3.6	V
REXT	External Resistor at Pin REXT	REXT (TCREXT ≤ 50ppm/K)	3.267	3.3	3.333	MΩ
I_{VDD}	Current Consumption	Active mode during measurement.		1.42	2	mA
I_{VDDSB}	Standby Current Consumption	Standby state			970	µA
I_{VDDPD}	Power Down Current Consumption	Power down state.			1	µA
V_{IH}	Input High Level	A0, A1, SCL, SYN	0.7			VDDD
V_{IL}	Input Low Level	A0, A1, SCL, SYN			0.3	VDDD
V_{OH}	Output High Level	READY I_{OHL} ≤ 3 mA	0.8			VDDD
V_{OL}	Output Low Level	SDA, READY I_{OHL} ≤ 3 mA			0.4	V
I_{OHL}	Output Drive Strength	Concerning to V_{OH} and V_{OL}		3	6	mA
I_{ILEAK}	Input Leakage Current	VSSD ≤ VIN ≤ VDDD	-5		5	µA
f_{CLKMIN}	Min. Internal Clock Frequency(1)	CREG3:CCLK = 00b		0.975		MHz
f_{CLKMAX}	Max. Internal Clock Frequency(1)	CREG3:CCLK = 11b		7.8		MHz

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{STARTSB}$	Startup Time after Standby state(1)	Until the start of the first measurement.		4	5	µs
$T_{STARTPD}$	Startup Time after Power Down state(1)	Until the start of the first measurement.		1.2	2	ms
T_{SYNDEL}	SYN Trigger Delay(1)	From falling SYN-edge to the start of the measurement.			3	$1/f_{CLK}$
T_{SYN}	SYN Negative or Positive Pulse Width(1)	SYN recognized as the start or end pulse of the measurement.	3			$1/f_{CLK}$
Temperature Sensor(1)						
T_abs_err	Temperature Absolute Error		-10		10	K
ADC(1)						
RES	ADC Resolution		10		24	bit
T_{CONV}	Conversion Time	CREG3:CCLK = 00b f_{CLKMIN}	1		16384	ms
		CREG3:CCLK = 11b f_{CLKMAX}	0.125		2048	ms
ΔT_{CONV}	Conversion Time Tolerance	Related to f_{CLK}	-25		25	%
INL	Integral Nonlinearity		-0.02		0.02	%
DNL	Differential Nonlinearity	No missing codes.	-0.5		0.5	LSB
D_{FSR}	Full Scale ADC Code	Per channel	1024		65535	counts
D_{DARK}	Dark ADC Count Value	E_e = 0; GAIN = 2048x T_{CONV} = 64 ms @ f_{CLKMIN}		8		counts
ENOB	Effective Number of Bits	GAIN = 64x T_{CONV} = 64 ms @ f_{CLKMIN}		15.4		bit

(1) These parameters are representative results by lab characterization and not included in the mass production test.

6 Typical Operating Characteristics

6.1 Optical Characteristics

Figure 7:
Optical Characteristics of the AS7331

Symbol	Parameter(1)	Conditions	Min	Typ	Max	Unit
$Re_{GAIN2048}$	Irradiance Responsivity for CREG1:GAIN = 2048x	A channel λ = 360 nm		385		counts/ (µW/cm²)
		B channel λ = 300 nm		347		
		C channel λ = 260 nm		794		
Re_{GAIN1}	Irradiance Responsivity for CREG1:GAIN = 1x	A channel λ = 360 nm		0.188		counts/ (µW/cm²)
		B channel λ = 300 nm		0.170		
		C channel λ = 260 nm		0.388		
$FSR_{GAIN2048}$	Full Scale Range of detectable Irradiance for CREG1:GAIN = 2048x	A channel λ = 360 nm		170		µW/cm²
		B channel λ = 300 nm		189		
		C channel λ = 260 nm		83		
FSR_{GAIN1}	Full Scale Range of detectable Irradiance for CREG1:GAIN = 1x	A channel λ = 360 nm		3.49e5		µW/cm²
		B channel λ = 300 nm		3.86e5		
		C channel λ = 260 nm		1.69e5		

(1) The optical characteristics are representative results by lab characterization and not included in the mass production tests. All values are measured at an integration time of 64 ms.

6.2 Optical Responsivity

Figure 8:
Normalized Spectral Responsivity of the AS7331

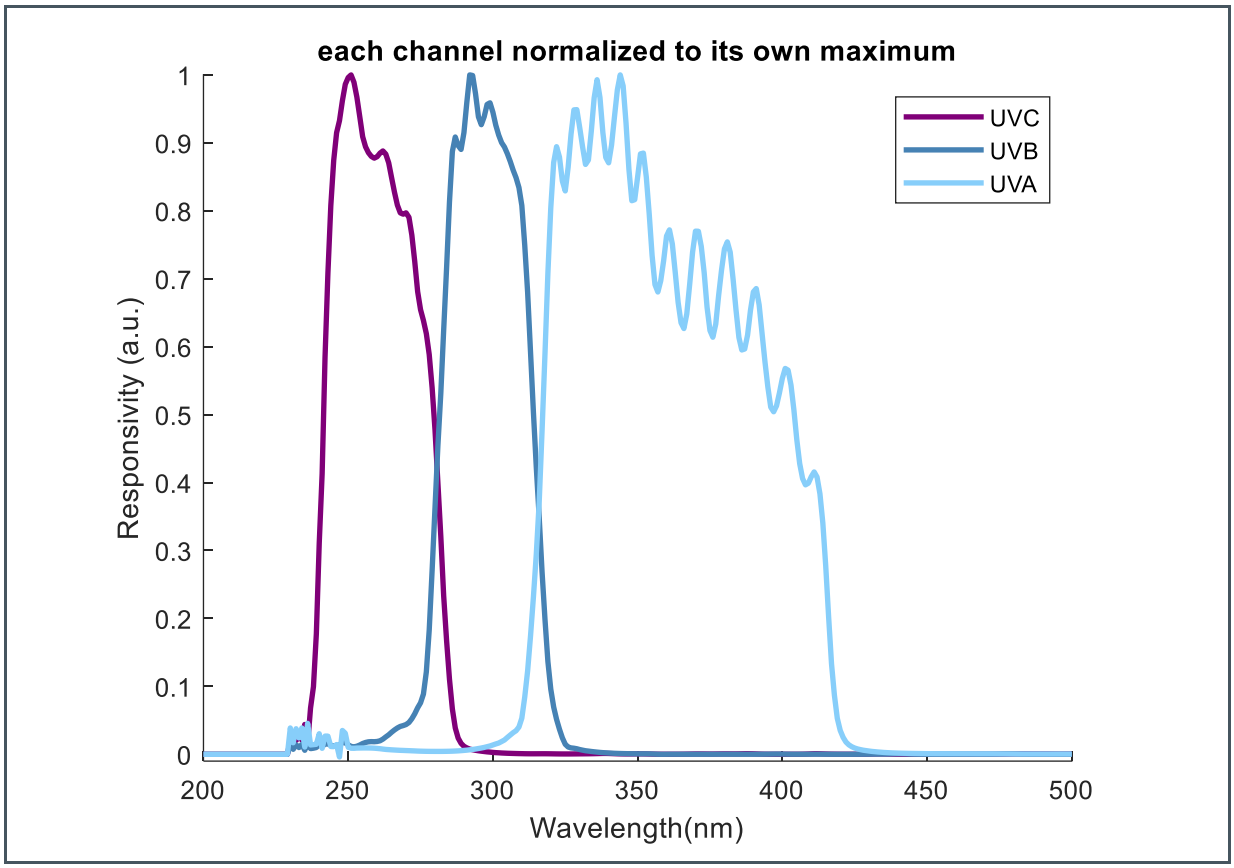
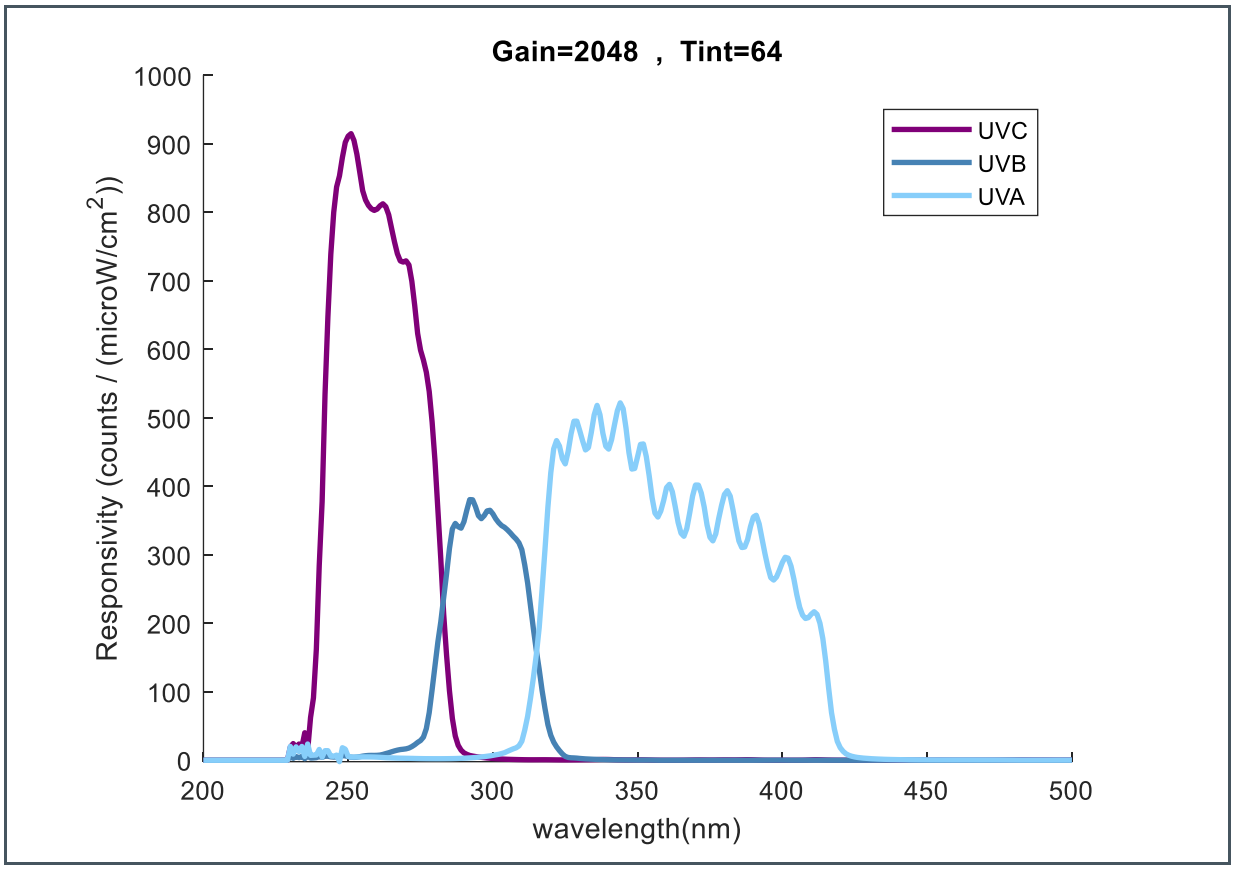


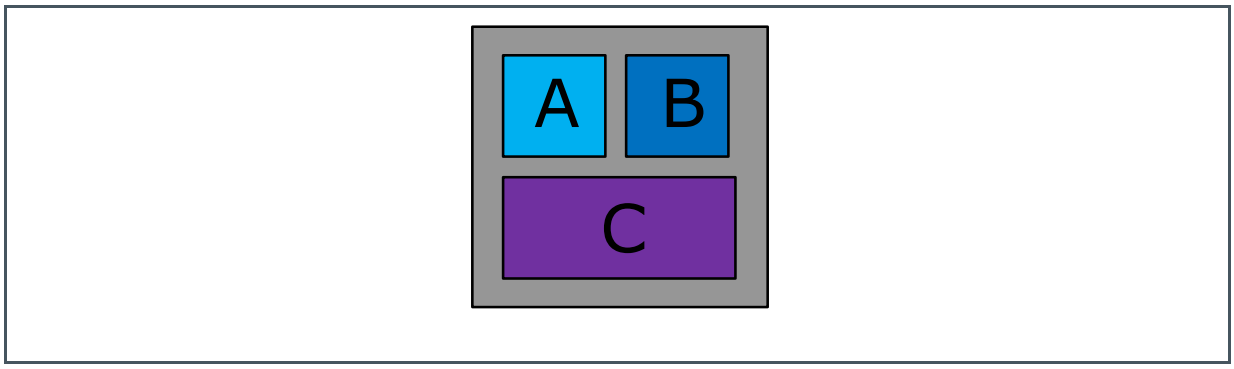
Figure 9:
Spectral Responsivity of the AS7331



7 Functional Description

The AS7331 includes three internal photodiodes with different spectral sensitivities and three ADCs, each one for each spectral photodetector. The irradiance responsivity R_e and the time of conversion T_{CONV} are user-defined and determined by the registers CREG1:GAIN and CREG1:TIME. Both, Gain and conversion time can be adapted to match the measurement conditions. At the end of each conversion, the digital equivalents of the filtered input light signal regarding the area of the sensor are stored in the output registers (MRES1 … MRES3). With the divider, the 16-bit of interest can be selected out of the 24-bit ADC output. Additionally, a temperature sensor works in parallel to the three optical channels, delivering the on-chip temperature at the end of conversion. The READY pin remains at a low logic level during the conversion. The rising edge and the following high logic level of READY signal, the end of the conversion. Internal information related to the conversion is available in a status register as well.

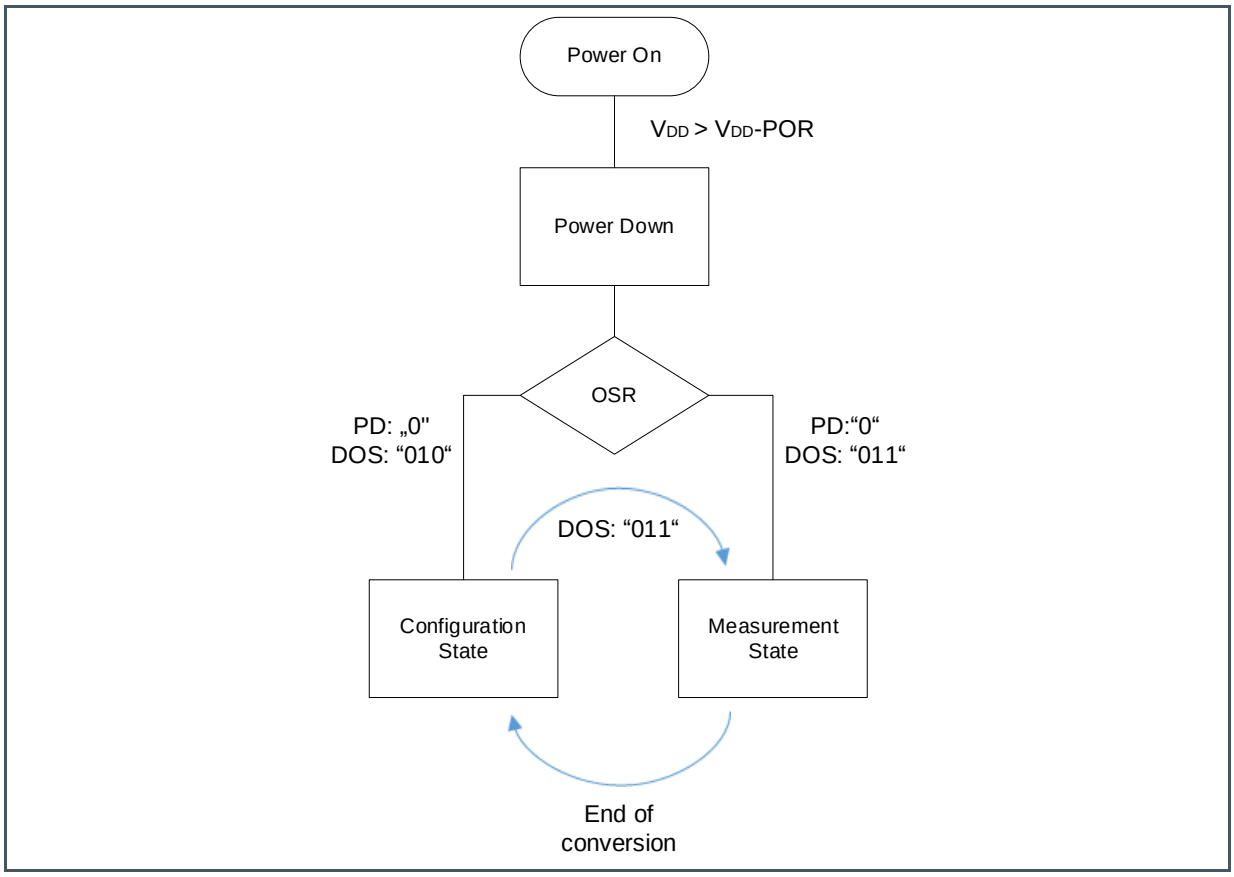
Figure 10:
Photodiode Array



7.1 Operational States

The AS7331 operates in two different states “**Configuration**” and “**Measurement**”. The three least significant bits of the Operational State Register (OSR) as Device Operational State (DOS) define the current state. After applying the power supply voltage, including power-on reset, or after software reset, the AS7331 stays in the Power-Down state. Then it is ready to be programmed via the I²C interface. When Power-Down is switched off (OSR: PD set to ‚0‘), the AS7331 starts in the Configuration state (CONFIG) or the Measurement state (MMODE) according to its DOS programming.

Figure 11:
Simplified State Diagram



7.1.1 Configuration State

This state enables access to the configuration registers (CREG1, CREG2, and CREG3). Irradiance responsivity (R_e) and conversion time (T_{CONV}) can be determined by the settings of the registers CREG1:GAIN and CREG1:TIME as well as the kind of measurement mode that can be chosen via the register CREG3:MMODE. A measurement is not possible in this state. Because of that, any access to the measurement result registers is disabled.

7.1.2 Measurement State

In this state the signal-to-digital conversion can be performed. Access to the output result registers is enabled, but at this time, there is no access possible to the configuration registers. Specific settings for the measurement should be performed by programming the configuration registers before the measurement is started (see chapter 8.2.6). The change between the Configuration and Measurement states can be performed by programming the DOS value of the operational state register OSR (see Figure 45). Afterward, a change from Measurement state to Configuration state will occur immediately.

Any active measurement is stopped and all output result registers as well as the status register are reset as well.

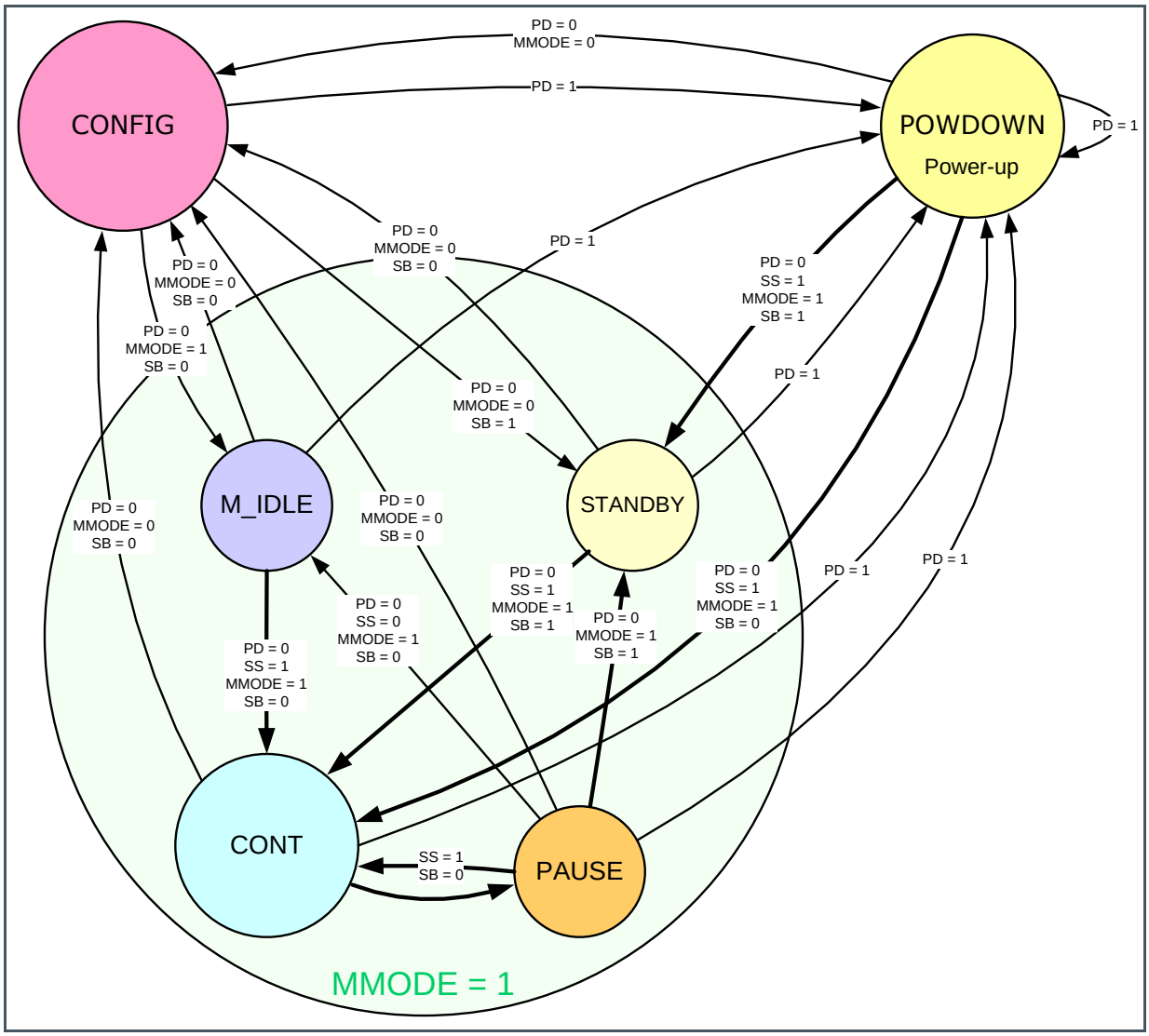
7.2 Measurement Modes

The AS7331 provides four different modes to perform the measurement. The register CREG3:MMODE (see Figure 50) defines the measurement mode that is performed by the device. In general, it is recommended not to communicate via the I²C during the conversion. Use pause times between two conversion cycles for data transfer via the I²C interface. To support such behavior, a variable pause time (T_{BREAK}) is implemented (register BREAK in Figure 51), which delays the start of the next conversion cycle in the measurement modes CONT, SYNS, and SYND. The I²C commands sent to the AS7331 always take effect after the complete I²C write cycle with an I²C stop condition at the end.

7.2.1 Continuous Measurement Mode – CONT

The A/D conversion is sequentially performed. The first conversion starts by setting the bit OSR:SS to “1”. If the power down or Standby option is switched on, the device deactivates it and initializes the continuous measurement. The measurement can only be stopped by resetting the OSR:SS bit.

Figure 12:
State Machine of CONT Mode



The conversion time (T_{CONV}) is determined by the content of the register CREG1:TIME (see Figure 48). The rising edge of READY signalizes the end of each conversion and its available valid results. Figure 48 shows the principle sequence for a measurement starting in CONT mode, while waiting in the Measurement state shows IDLE:

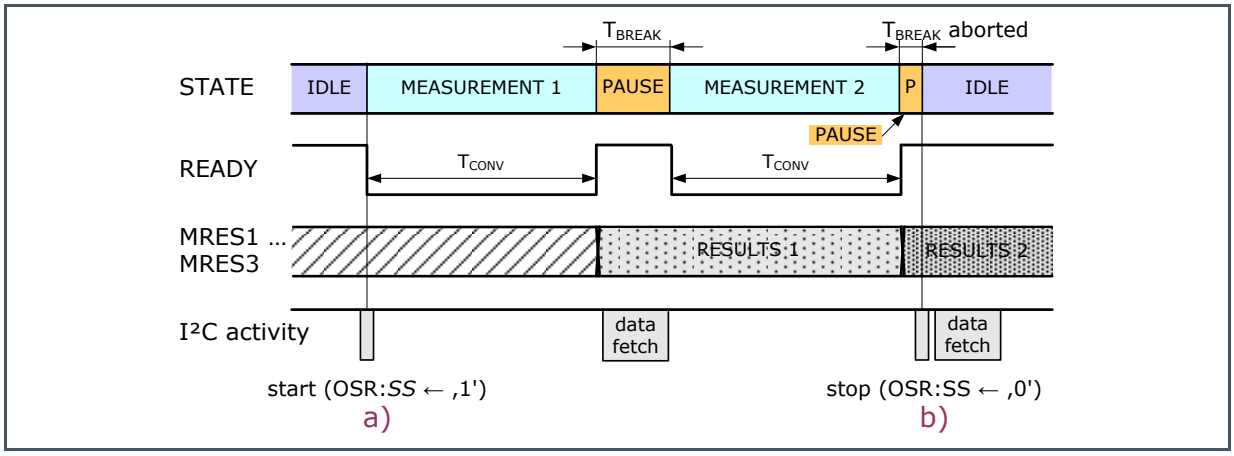
1. OSR programming: 83h, start of continuous measurement via OSR:SS = “1”, while the device is already in measurement mode (OSR:DOS = 011b),
2. OSR programming: 03h, abortion of continuous measurement via OSR:SS = “0” while pause time (T_{BREAK}) is already activated to get the last measurement results.

It is recommended to read the measurement results during the break between two consecutive conversions. This pause time (T_{BREAK}) can be configured in steps of 8 µs up to 2040 µs (Figure 53).

Information

Please note that the break time should be long enough to prevent overlapping of data fetch activities with the measurement for avoiding measurement disturbances, which could cause distortions of the measurement results.

Figure 13:
Principle Sequence for a Measurement Start in CONT Mode



7.2.2 Command Measurement Mode – CMD

The CMD mode enables a start of a single conversion. Each conversion starts by setting the bit OSR:SS to “1”. The conversion time (T_{CONV}) is determined by the content of the register CREG1:TIME (see Figure 48). Figure 14 shows the first measurement starting from the Configuration state by setting the bits of the Device Operational State (OSR:DOS) and Start/Stop (OSR:SS) at the same time with OSR = 83h. To start the next measurement, OSR = 80h is set (only bit OSR:SS, OSR:DOS = 000b corresponds to NOP – no operation, see also Figure 45.

The rising edge of READY signalizes the end of conversion and its valid output data can be read via the I²C interface (data fetch).

Figure 14:
State Machine of CMD Mode

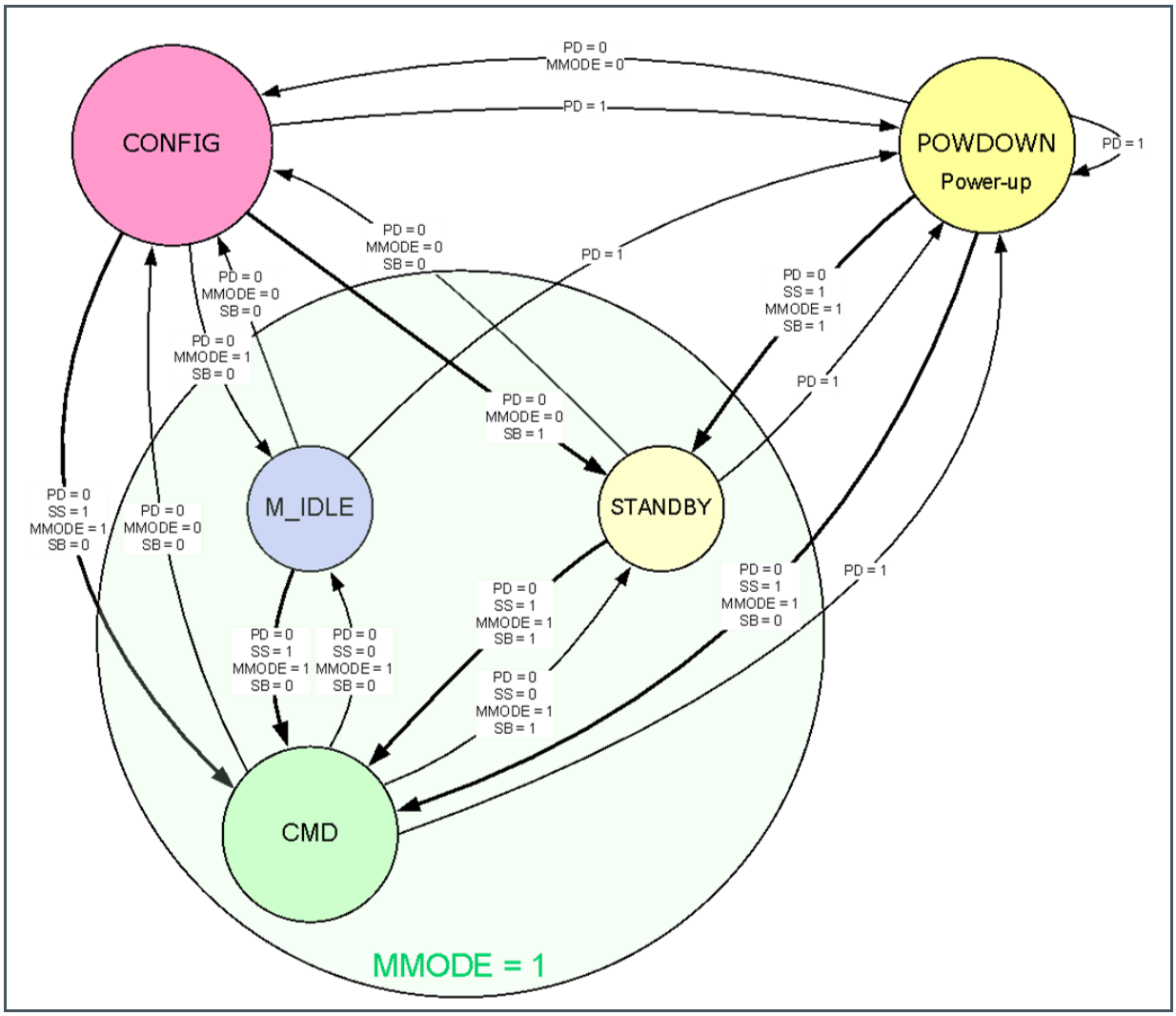
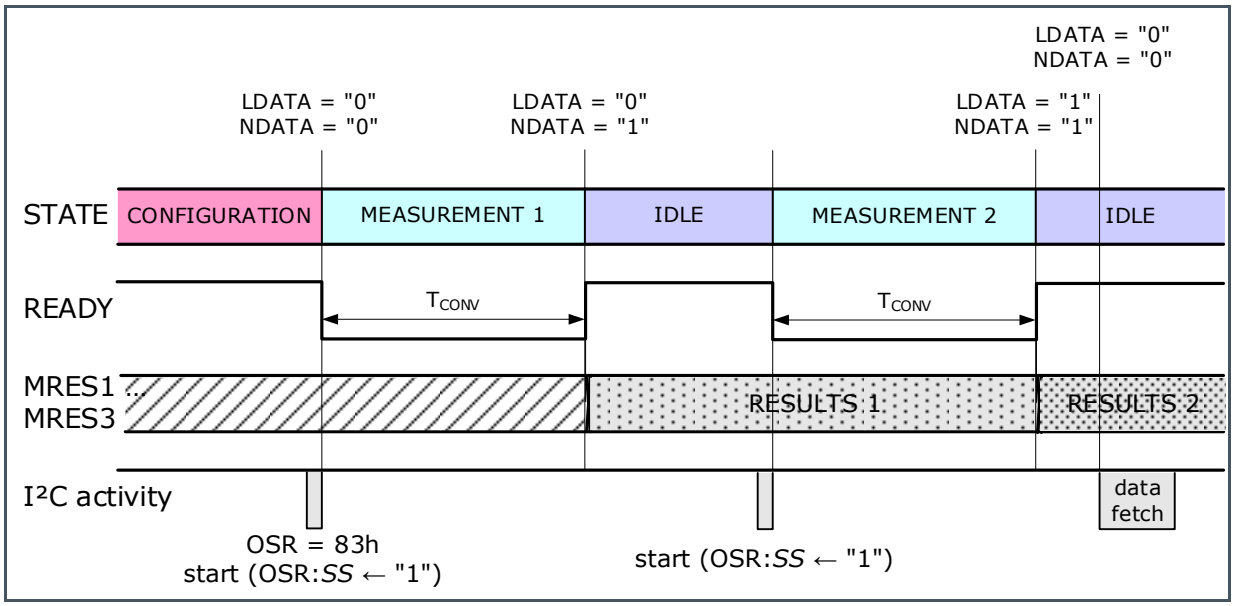


Figure 15 shows the principle sequence for a measurement to start in CMD mode coming from the Configuration state and waiting in the Measurement state between the measurements is shown as IDLE:

- OSR programming: 83h, changes to the Measurement state and starts measurement via OSR:SS = “1”;
- “Automatically” OSR programming: 03h, reset bit OSR:SS to “0” at the end of the conversion.

Figure 15:
Principle Sequence for a Measurement Start in CMD Mode Coming From Configuration State

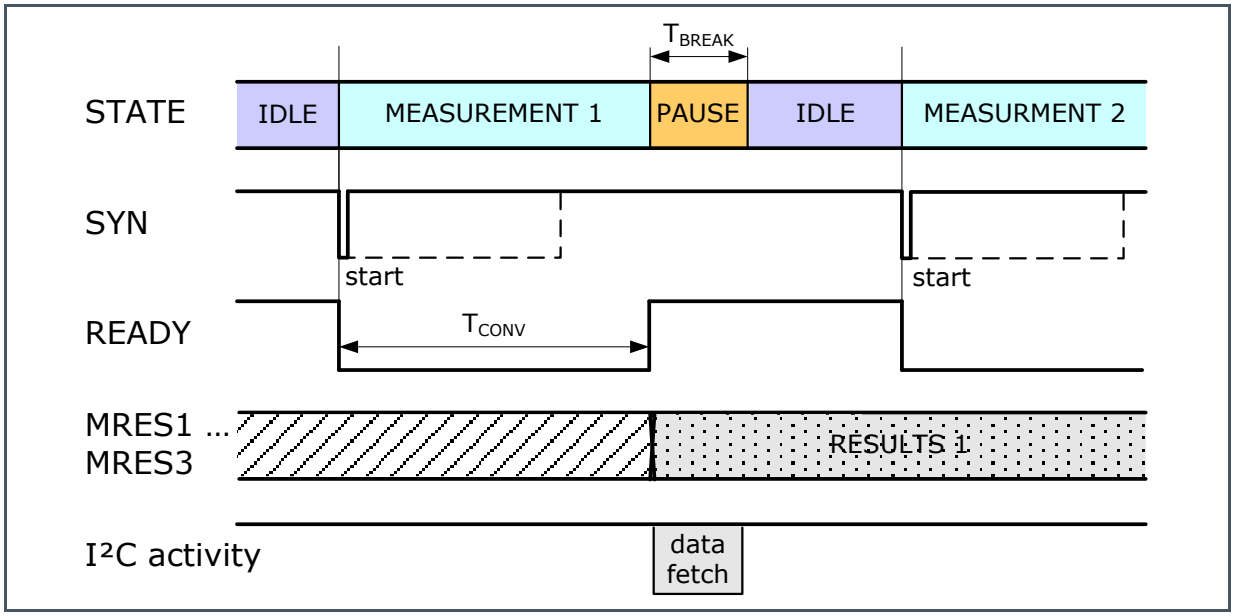


7.2.3 Synchronous Measurement Mode – SYNS

In this measurement mode, the input pin, SYN, acts as a trigger event for the start of A/D conversion. The falling edge at the SYN pin starts the measurement. The conversion time (T_{CONV}) is determined by the content of the register CREG1:TIME (see Figure 48). The READY pin signalizes the progress of conversion (see Figure 16), its rising edge shows the end of conversion and its available valid results. The data fetch should be performed between the rising edge of signal READY and the next falling edge of signal SYN, in order to allow distortion-free measurements. SYN pulses during the programmed pause time T_{BREAK} are ignored to avoid a start of the measurement during a running data fetch. The bit OSR:SS also takes effect in the SYNS mode, because the start of the measurement is only possible with OSR:SS = “1”.

Figure 16 shows the principle sequence for a measurement to start in SYNS mode, OSR:DOS = 011b and OSR:SS = “1” already set and waiting in Measurement state is shown as IDLE.

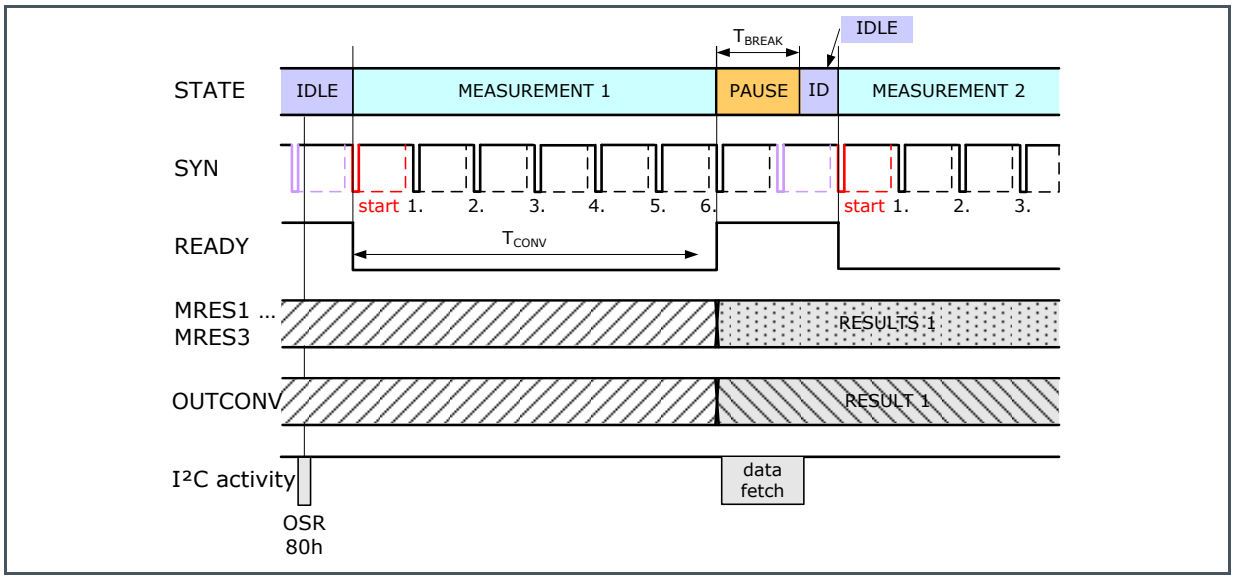
Figure 16:
Principle Sequence for a Measurement Start in SYNS Mode, OSR:DOS = 011b and OSR:SS = “1”



7.2.4 Synchronous Measurement Start and End Mode – SYND

In this mode, the signal at pin SYN completely controls the start and stop of measurement. When the device is waiting in the Measurement state and OSR:SS is set to “1” the first falling edge at pin SYN starts the measurement. Each following falling edge of signal SYN, which occurs within the conversion time, can continue or stop the measurement. The content of the register EDGES determines which edge is the stopping one. That means the measurement will not stop until a certain number of falling edges at pin SYN pass within the conversion time. The value of register EDGES determines the number of edges (see Figure 17 and chapter 8.2.7). Figure 17 shows the principle sequence for a measurement to start in SYND mode. While waiting in the Measurement state is shown as IDLE, after OSR:SS is set to “1” (see Figure 45) the AS7331 waits for signal SYN to start. The conversion time is set to 06h in register EDGES, during the pause time (T_{BREAK}), and falling edges at pin SYN are ignored.

Figure 17:
Principle Sequence for a Measurement Start in SYND Mode



The conversion time (T_{CONV}) is determined by the duration between the edges of the start and stop of the SYN signal. If CREG2:EN_TM is set to “1”, the register OUTCONV contains an equivalent amount of T_{CONV} as counts of the internal clock. With the value of OUTCONV, the measurement results can be calculated more precisely (see chapter 7.6).

7.3 Energy Saving Options

The usage of the energy-saving options is consistent for all measurement modes. The signal path at pin READY always represents, independent of wake-up times or synchronizing events at pin SYN concerning the internal clock, the real measurement process. Every measurement mode can be terminated with OSR:SS = “0” or changing to the configuration state at every time, whereas uncompleted A/D conversions are not stored. In the case of both energy-saving options power down state (POWDOWN) and standby state (STANDBY) are switched on (OSR:PD = “1” and CREG3:SB = “1”). The startup times ($T_{STARTPD}$ and $T_{STARTSB}$) run one after the other after power down and standby are switched off.

7.3.1 Power Down

Power down is an option to reduce power consumption. After applying the power supply voltage including power-on reset or after software reset, the AS7331 stays in power down state. The clock generator and all analog parts of the device are turned off. The power consumption of the device is close to zero. The digital part of the AS7331 stays idle, but full communication via the I²C interface is granted in the configuration and measurement state.

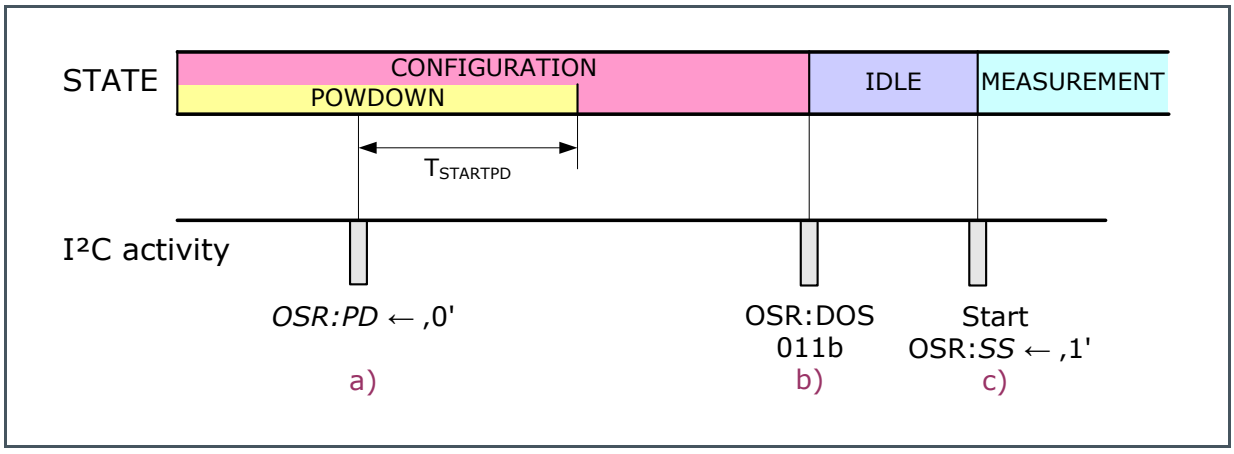
In case the Device Operational State (DOS) is set to the measurement mode, the start/stop of measurement is possible by setting the OSR:SS bit and reading measurement data. The power down can be switched on and off by the bit OSR:PD (Figure 45). Switching on power down via the bit OSR:PD = “1”, changes the AS7331 to the power down state after the end of an ongoing measurement. Switching off power down (OSR:PD = ‚0‘) results in a change to the Idle state (IDLE for waiting) or standby state depending on the bit CREG3:SB. This change to another operational state is delayed by the startup time ($T_{STARTPD}$) typically of 1.2 ms. A conversion can start in all the measurement modes while the power down state is activated (OSR:PD = “1”). In the measurement modes CMD and CONT, it is done by setting the bit OSR:SS to ‚1‘. In addition, the falling edge of the signal at pin SYN for the measurement modes SYNS and SYND initiate the start. In all cases, the start of the conversion is delayed by the startup time ($T_{STARTPD}$). After the conversion in the CMD, SYNS and SYND modes, the AS7331 changes back into the power down state, whereas the measurement of the CONT mode is interactive until it is stopped by setting the bit OSR:SS = to “0” before it changes back into the power down state.

There are two methods for startup of the AS7331:

1. After applying the power supply voltage, including power-on reset, or after software reset, the OSR:PD bit must be set to “0” via the I²C interface communication. The analog part and the internal clock system start to work along with the defined configuration of the AS7331. Nevertheless, it is still possible to change the configuration in front of the time b) in Figure 18. The Device Operational State changes to the Measurement state to start the measurement (OSR:SS = “1”) without further delay caused by energy-saving options.
Figure 18 shows the principle sequence after power-on reset and separated writing of the bits OSR:PD, OSR:DOS, and OSR:SS:

a) OSR programming: 02h, after $T_{STARTPD}$ continuing within only the configuration state,
b) OSR programming: 03h, change to the Measurement state – waiting is shown as IDLE,
c) OSR programming: 80h, start of the measurement as stated in the device’s configuration.

Figure 18:
Principle Sequence After Power-On Reset and Separated Writing of the Bits OSR:PD, OSR:DOS and OSR:SS



2. Coming from power down state activated by OSR:PD = “1”, the AS7331 is not actively switched on until OSR:SS is set to “1” (together while or with OSR:DOS = 011b). This means the bit OSR:SS is a direct start condition for the CMD and CONT modes, whereas for both SYN modes, the falling edge at pin SYN is necessary for the startup. The programmed measurement mode follows after startup, marked by the falling edge of the signal path at the READY pin. If the configuration contains CREG3:SB = “1” (as the example in Figure 19 shows), additionally after startup time ($T_{STARTPD}$), the wake-up time ($T_{STARTSB}$) of 4 µs follows, before the measurement starts.

Figure 19:
Principle Start of the Measurement from OSR:PD = “1” and CREG3:SB = “1”

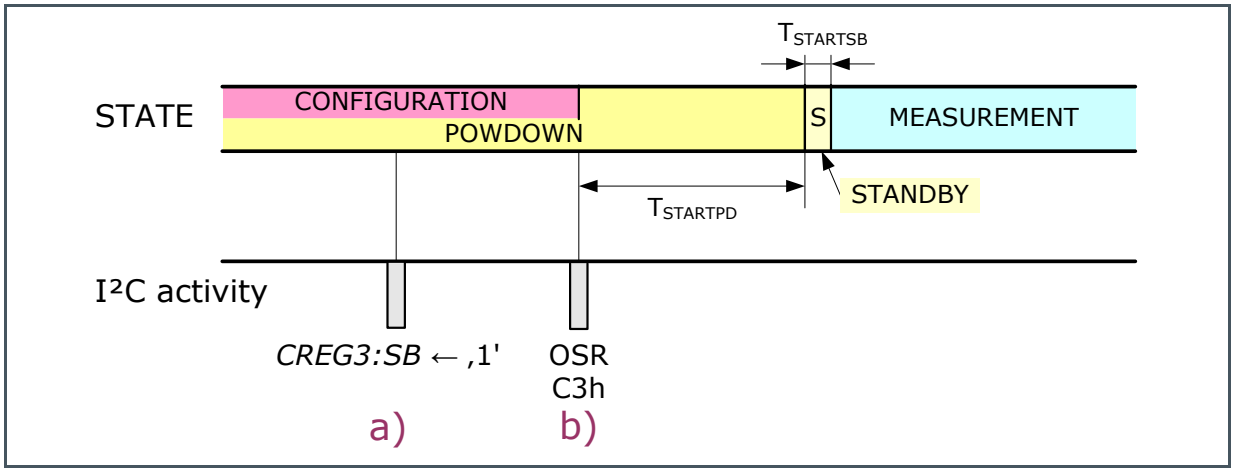


Figure 19 shows the principle start of the measurement from OSR:PD = “1” and CREG3:SB = “1”:

a) CREG3 programming: bit CREG3:SB = “1”,
b) OSR programming: C3h, start of the measurement with prior run of $T_{STARTPD}$ and $T_{STARTSB}$.

The programmed energy-saving option (before or when the measurement is started or during the measurement) is switched on after the regular end of the measurement and storing of the results within the buffer registers. In case of an abortion of the measurement with OSR:SS = “0” or switching to the configuration state the energy saving option is switched on without saving any results.

7.3.2 Standby

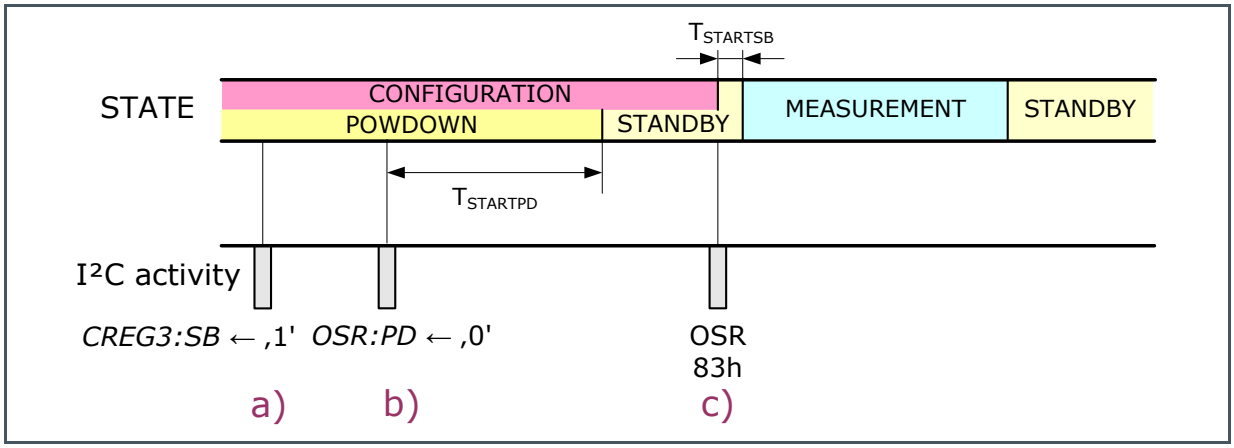
Standby is another option for reducing the power consumption, but compared to power down, fewer internal analog components are switched off to be able to become active again in a very short time. The digital part of the AS7331 stays idle, but full communication via the I²C interface is granted in configuration and measurement states. The CREG3:SB bit can only be changed in the configuration mode. The wake-up process is possible in combination with the start condition of the configured measurement mode. Standby is automatically deactivated by starting the CMD or CONT measurement mode by setting the bit OSR:SS to “1”. In addition, for the measurement modes SYNS and SYND, an initiated start is necessary by the falling edge of the signal at pin SYN. While starting

the measurement, the A/D conversion follows immediately after the wake-up time ($T_{STARTSB}$) of about 4 µs.

Figure 20 shows the principle start and stop sequence of measurement after startup with OSR:PD = “0” and CREG3:SB = “1”:

a) CREG3 programming: Bit CREG3:SB = “1”,
b) OSR programming: 02h, after startup continuing with configuration mode,
c) OSR programming: 83h, measurement start, wake-up and conversion, return to standby after measurement ends.

Figure 20:
Principle Start and Stop Sequence of a Measurement After Startup with OSR:PD = “0” and CREG3:SB = “1”

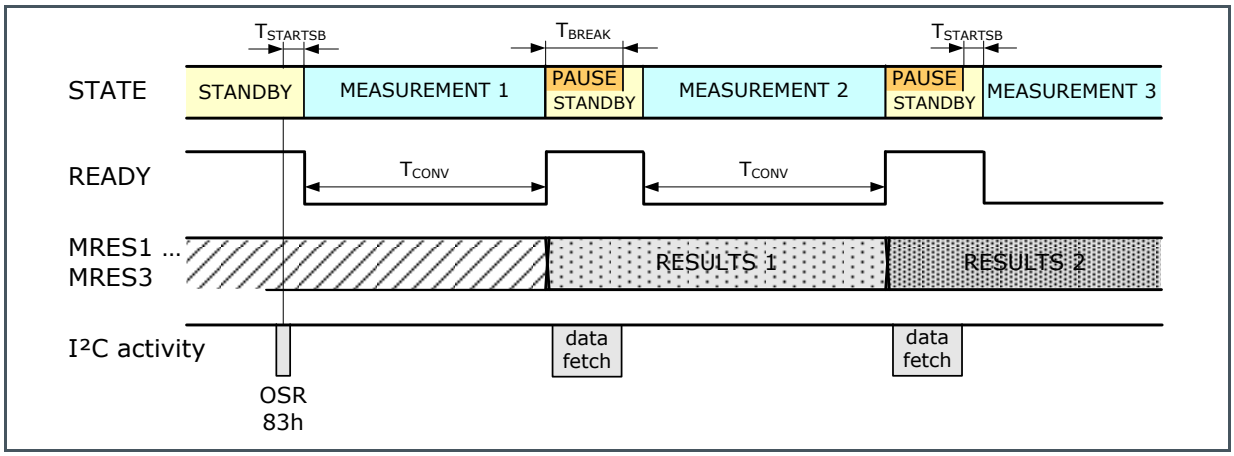


7.3.3 Examples

For both modes, CONT and SYN, it is recommended to configure a pause time, T_{BREAK}, (register BREAK Figure 51), to avoid disturbances during the A/D conversion caused by the I²C interface communication. The selectable pause time using the register BREAK should be long enough, such that all the output results are read before the next conversion starts (automatically in CONT modus or synchronized via pin SYN in SYN modes). While the pause time (T_{BREAK}) is running, it is possible to save energy if the bit CREG3:SB is configured to “1”. The wake-up time, $T_{STARTSB}$, of about 4 µs is short, compared to the necessary time for the I²C communication protocol represented by the BREAK register.

Figure 21 shows the principle sequence of CONT mode; if CREG3:SB is set to “1”, saving energy is possible while the pause time T_{BREAK} is activated for I²C interface communication.

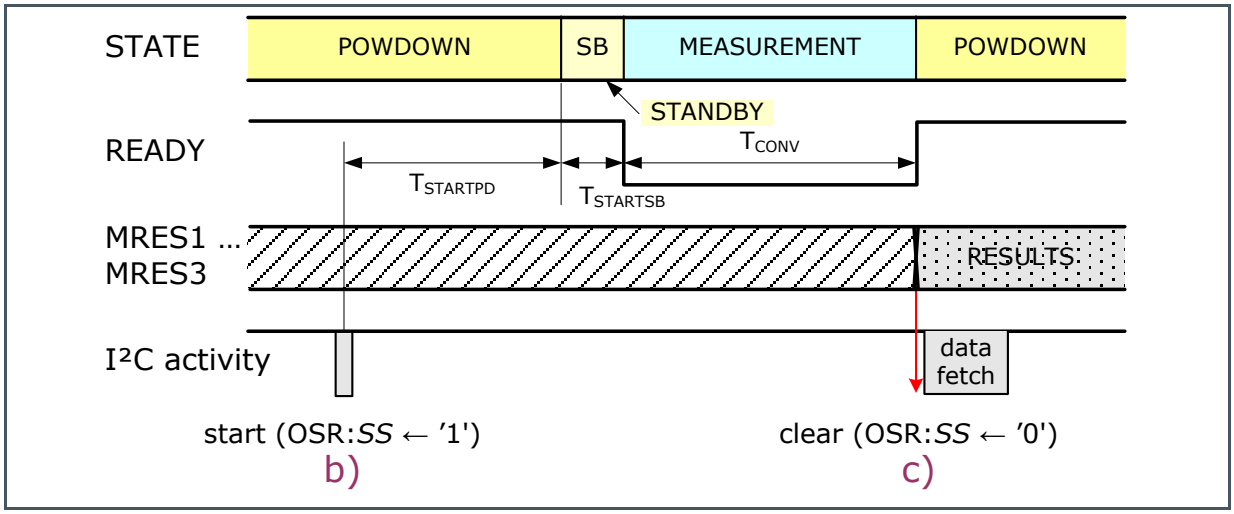
Figure 21:
Principle Sequence of CONT Mode – if CREG3:SB is Set to “1”



Another example shows, that after the end of a conversion in CMD mode the AS7331 returns to power down and/or standby state depending on the bits OSR:PD and CREG3:SB. In case of both bits are “0” while the measurement state the device would return to idle, waiting for the next measurement to start. Figure 22 shows the principle sequence whereas measurement starts in CMD mode with power down and standby switched on (device is already in measurement state):

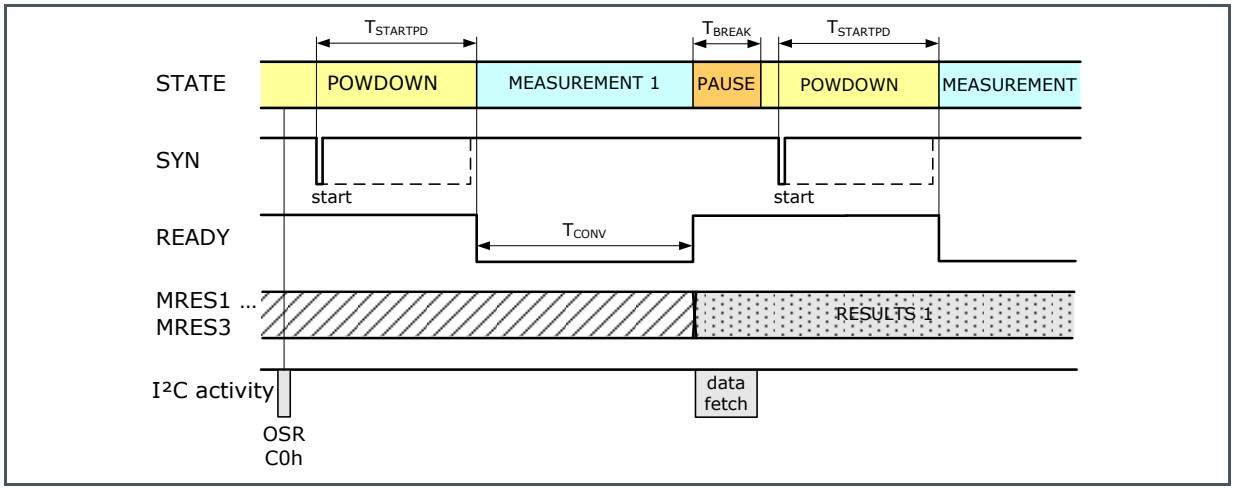
a) CREG3 programming: Bit CREG3:SB = “1” was set in Configuration state (not shown),
b) OSR programming: C0h, “startup” and “wake-up” before conversion starts,
c) “Automatically” OSR programming: 43h, the end of conversion resets bit OSR:SS, to power down.

Figure 22:
Principle Sequence Whereas Measurement is Started in CMD Mode with Power Down, Standby Switched On



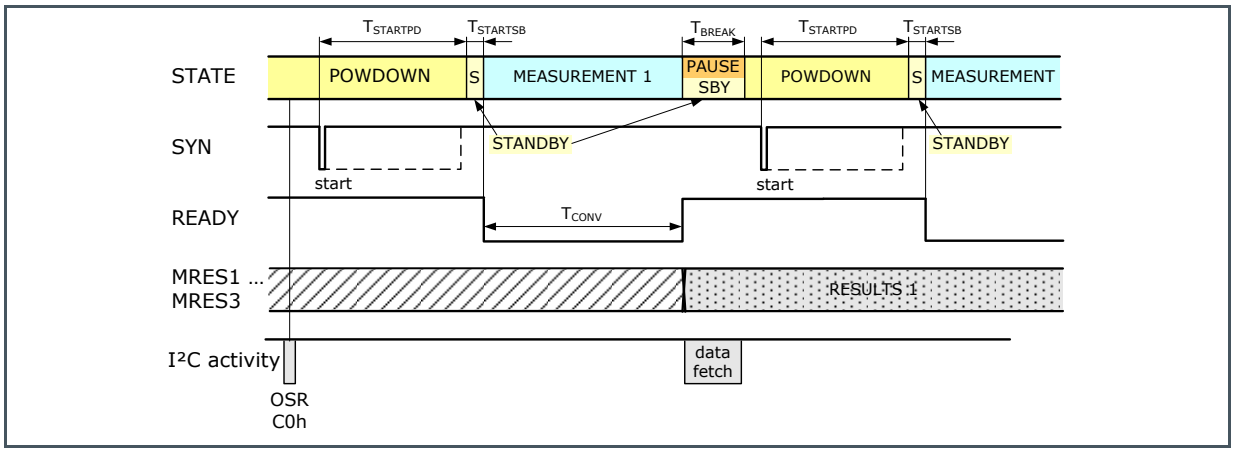
It is also possible to use the power down state in combination with SYNS mode. The falling edge at pin SYN immediately starts the conversion after power down ends shown by the signal at pin READY. That kind of measurement is only useful in case the distance between falling edges at pin SYN is more than the conversion time, pause time, and startup time altogether. Figure 23 shows the principle sequence of measurement in SYNS mode being ready (bits OSR:PD = “1” and OSR:SS = “1”) and waiting for the falling edge at pin SYN to startup.

Figure 23:
Principle Sequence of Measurement in SYNS Mode



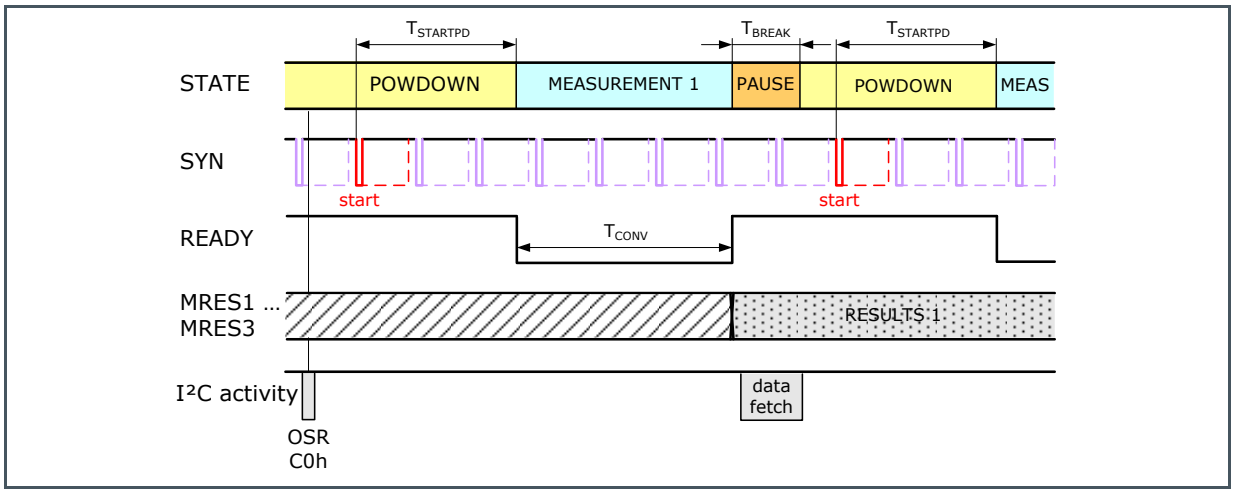
By additionally activating standby (bit CREG3:SB = “1”), a maximum amount of energy can be saved, because the operational readiness is not given until shortly before A/D conversion starts. When starting reading process of the results (pause time), the device is also saving energy in the standby state (see Figure 24). Figure 24 shows the principle sequence of measurement in SYNS mode being ready with OSR:PD = “1” (as in Figure 23), but with bit CREG3:SB = “1” to save a maximum amount of energy as explained above.

Figure 24:
Principle Sequence of Measurement in SYNS Mode Being Ready with OSR:PD = “1”



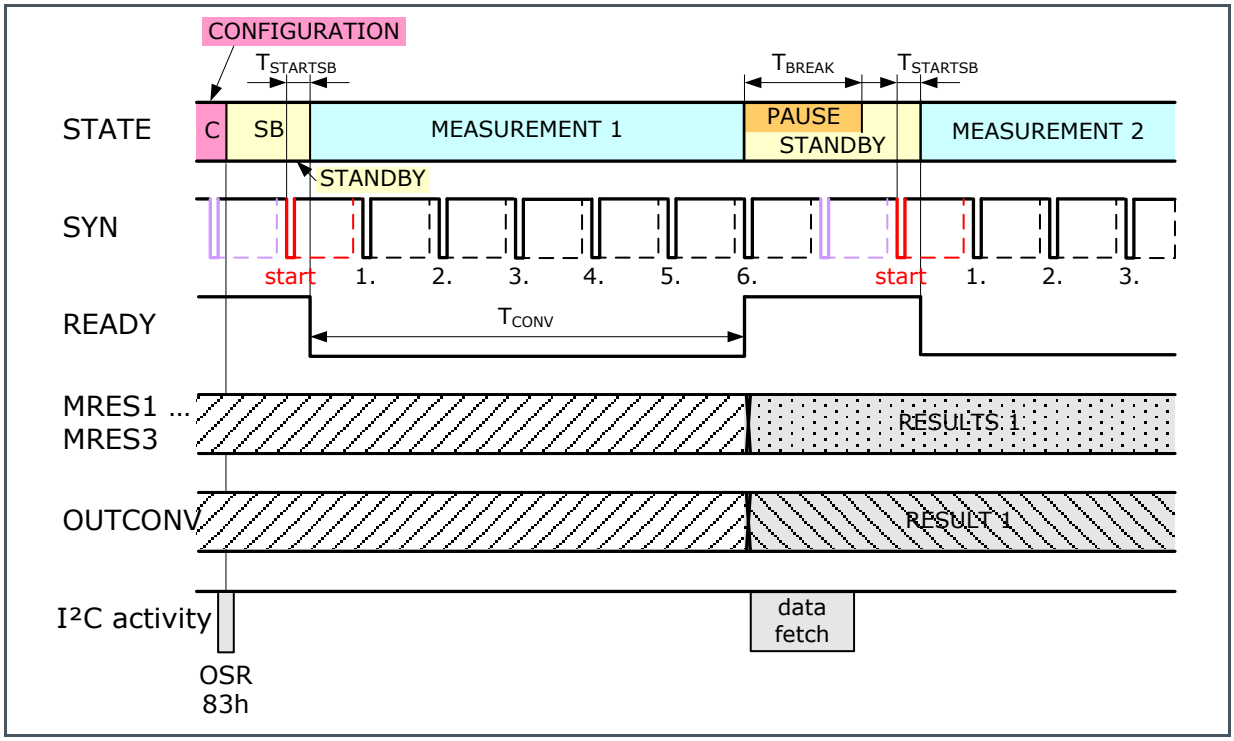
The following example of a SYNS mode shows the correct measurement procedure but with an unfavorable chosen application. After the start of measurement with bit OSR:SS = “1” only the falling edges marked in red (see Figure 25) at pin SYN are accepted as the start condition. Because of the tight distances of the SYN edges, many falling edges are ignored during the startup phase ($T_{STARTPD}$), conversion time (T_{CONV}), and pause time (T_{BREAK}).

Figure 25:
Principle Sequence of Measurement in SYNS Mode (OSR:PD, OSR:SS are set to “1”)



Continuously occurring SYN pulses (e.g. generated by a PWM controlling the measurement mode SYND) are ignored in the configuration state and whilst pause time, T_{BREAK}, (see Figure 26) is activated. It is recommended to increase the default value of the BREAK register accordingly, if the time reference result OUTCONV must be read via the I²C interface. The EDGES register gives the conversion time, but as shown in Figure 26 the real conversion time is always represented by T_{CONV} at pin READY. Furthermore, the output result OUTCONV can be used to get the right measurement result (see also chapters 7.4 and 7.6). Figure 26 shows the principle sequence of measurement in SYND mode, which is ready for wake-up after switching off the power down state with OSR:PD = “0”, and setting OSR:SS to “1” in the configuration state, then waiting for the start via pin SYN (with exemplary settings of EDGES = 06h and CREG3:SB = “1” for energy-saving during pause time T_{BREAK}).

Figure 26:
Principle Sequence of Measurement in SYND Mode Ready for Wake-Up After Switch Off Power Down State



7.4 Transfer Function

In general, the implemented A/D converter represents a delta-sigma converter, which performs charge balancing between the input light at the photodiodes and an internal reference. The input currents of the photodiodes result in pulse density modulated digital signals, further filtered by counters up to 24- bits. The counters will be set by definition of T_{INT}. A 64 ms conversion time is required as minimum for a 16-bit I²C output (Figure 27). In the end, each channel's counter status represents a digital equivalent of the average input light irradiance regarding the channel's sensor area within the conversion time interval. The input light irradiance can be calculated from the measurement result by:

Equation 2:

$$E_e = \frac{MRES}{R_e} = \frac{FSR_{E_e}}{N_{CLK}} \bullet MRES$$

Equation 3:

$$E_e = \frac{FSR_{E_e}}{T_{CONV} \bullet f_{CLK}} \bullet MRES$$

Where:

MRES = Digital output value of the conversion (content of output registers MRES1 to MRES3).

E_e = Input light irradiance regarding to the photodiode's area within the conversion time interval.

FSR_{Ee} = Full Scale Range of detectable input light irradiance E_e.

R_e = Irradiance responsivity (see Figure 12).

T_{CONV} = Conversion time interval.

N_{CLK} = Number of clock cycles within the conversion time interval T_{CONV} (see Figure 11).

f_{CLK} = Clock frequency.

In the CONT, CMD and SYNS modes the conversion time, T_{CONV}, is internally generated[1]. In the SYND mode the conversion time is defined by the timing of the external pulses at the SYN pin and the number of pulses stored in the EDGES register (see Figure 17 chapter 7.6 and chapter 8.2.7).

The number of clock counts within this interval is a constant number, which keeps the output result independent of the internal clock frequency. In this case, the input light irradiance E_e, regarding the area of the photodiode of the channel can be represented by Equation 2. In SYND mode Equation 3 represents the externally generated conversion time T_{CONV}, and the conversion result. If the conversion time measurement is activated (CREG2:EN_TM = "1") the number of clock counts within the externally given conversion time can also be internally captured. So the input light irradiance E_e regarding the photodiode's area of the channel can be calculated as:

Equation 4:

$$E_e = \frac{FSR_{E_e}}{OUTCONV} \bullet MRES$$

Where:

MRES = Digital output value of the conversion (content of output registers MRES1 to MRES3).

E_e = Input light irradiance regarding the photodiode's area within the conversion time interval.

FSR_{Ee} = Full Scale Range of detectable input light irradiance E_e.

OUTCONV = Conversion time duration expressed as the number of clock counts within this time.

In this way, the input light irradiance can be measured independently of the internal frequency and the external conversion time variations in SYND mode.

[1] The system clock is internally generated and is subject to technological tolerances. As such, the clock frequency may vary, which must be considered when calculating the time to be programmed (e.g. registers BREAK for pause time T_{BREAK} or CREG1:TIME for conversion time T_{CONV}).

The calculation of the input light irradiance by Equation 4 is more precise than the result of Equation 3 because the tolerances of the clock frequency $f_{CLK,}$ are eliminated. The irradiance responsivity $R_{e,}$ and internal conversion time T_{CONV} are determined by the content of register bits CREG1:GAIN and CREG1:TIME (see Figure 48). Their values directly determine the sensitivity, the LSB value, and the full-scale range (FSR) of the detectable irradiance, $E_{e,}$ of the A/D conversion.

Information

The values in the Figure 27 up to Figure 32 are calculations based on the general sensitivity without any influences of system and opto-mechanical setup. These values are only an indication for the sensor configuration.

Figure 27:
UVA-Channel (λ = 315 nm – 410 nm) Programmable FSR and LSB of the Detectable Input Light Irradiance E_e

TIME(1)	0	1	2	3	4	5	6	7
N_{CLK}(1)	1024	2048	4096	8192	16384	32768	65536	131072
T_{CONV}[ms](1)	1	2	4	8	16	32	64	128
RESOL[bit](1)	10	11	12	13	14	15	16	17
GAIN(1)	FSR [µW/cm²] of detectable irradiance E_e (channel A)							
2048x	170.000(2)							85.000
1024x	340.000							170.000
512x	680.000							340.000
256x	1360.000							680.000
128x	2720.000							1360.000
64x	5440.000							2720.000
32x	10880.000							5440.000
16x	21760.000							10880.000
8x	43520.000							21760.000
4x	87040.000							43520.000
2x	174080.000							87040.000
1x	348160.000							174080.000
GAIN(1)	LSB [nW/cm²] – least significant bit of FSR (channel A)							
2048x	166.02	83.01	41.50	20.75	10.38	5.19	2.59	1.30
1024x	332.03	166.02	83.01	41.50	20.75	10.38	5.19	2.59
512x	664.06	332.03	166.02	83.01	41.50	20.75	10.38	5.19
256x	1328.13	664.06	332.03	166.02	83.01	41.50	20.75	10.38
128x	2656.25	1328.13	664.06	332.03	166.02	83.01	41.50	20.75
64x	5312.50	2656.25	1328.13	664.06	332.03	166.02	83.01	41.50
32x	10625.00	5312.50	2656.25	1328.13	664.06	332.03	166.02	83.01

TIME(1)	0	1	2	3	4	5	6	7
16x	21250.00	10625.00	5312.50	2656.25	1328.13	664.06	332.03	166.02
8x	42500.00	21250.00	10625.00	5312.50	2656.25	1328.13	664.06	332.03
4x	85000.00	42500.00	21250.00	10625.00	5312.50	2656.25	1328.13	664.06
2x	170000.00	85000.00	42500.00	21250.00	10625.00	5312.50	2656.25	1328.13
1x	340000.00	170000.00	85000.00	42500.00	21250.00	10625.00	5312.50	2656.25

(1) TIME (T_{CONV}) – given by CREG1:TIME = 0 … 7 dec, N_{CLK} – number of clock cycle within conversion time T_{CONV}, RESOL – Resolution of internal A/D conversion, GAIN = 1x given by CREG1:GAIN = 11 dec up to GAIN = 2048x given by CREG1:GAIN = 0 dec (see Figure 48).

(2) Basic sensitivity of the UVA-channel.

Figure 28:
UVA-Channel (λ = 315 nm – 410 nm) Programmable FSR and LSB of the Detectable Input Light Irradiance E_e

TIME(1)	8	9	10	11	12	13	14	15
N_{CLK}(1)	262144	524288	1.05E+06	2.10E+06	4.19E+06	8.39E+06	1.68E+07	1024
T_{CONV}[s](1)	0.256	0.512	1.024	2.048	4.096	8.192	16.384	0.001
RESOL[bit](1)	18	19	20	21	22	23	24	10
GAIN(1)	FSR [µW/cm²] of detectable irradiance E_e (channel A)							
2048x	42.50	21.25	10.63	5.31	2.66	1.33	0.66	170.00
1024x	85.00	42.50	21.25	10.63	5.31	2.66	1.33	340.00
512x	170.00	85.00	42.50	21.25	10.63	5.31	2.66	680.00
256x	340.00	170.00	85.00	42.50	21.25	10.63	5.31	1360.00
128x	680.00	340.00	170.00	85.00	42.50	21.25	10.63	2720.00
64x	1360.00	680.00	340.00	170.00	85.00	42.50	21.25	5440.00
32x	2720.00	1360.00	680.00	340.00	170.00	85.00	42.50	10880.00
16x	5440.00	2720.00	1360.00	680.00	340.00	170.00	85.00	21760.00
8x	10880.00	5440.00	2720.00	1360.00	680.00	340.00	170.00	43520.00
4x	21760.00	10880.00	5440.00	2720.00	1360.00	680.00	340.00	87040.00
2x	43520.00	21760.00	10880.00	5440.00	2720.00	1360.00	680.00	174080.00
1x	87040.00	43520.00	21760.00	10880.00	5440.00	2720.00	1360.00	348160.00
GAIN(1)	LSB [nW/cm²] – least significant bit of FSR (channel A)							
2048x	0.65	0.32	0.16	0.08	0.04	0.02	0.01	166.02
1024x	1.30	0.65	0.32	0.16	0.08	0.04	0.02	332.03
512x	2.59	1.30	0.65	0.32	0.16	0.08	0.04	664.06
256x	5.19	2.59	1.30	0.65	0.32	0.16	0.08	1328.13
128x	10.38	5.19	2.59	1.30	0.65	0.32	0.16	2656.25
64x	20.75	10.38	5.19	2.59	1.30	0.65	0.32	5312.50
32x	41.50	20.75	10.38	5.19	2.59	1.30	0.65	10625.00

TIME(1)	8	9	10	11	12	13	14	15
16x	83.01	41.50	20.75	10.38	5.19	2.59	1.30	21250.00
8x	166.02	83.01	41.50	20.75	10.38	5.19	2.59	42500.00
4x	332.03	166.02	83.01	41.50	20.75	10.38	5.19	85000.00
2x	664.06	332.03	166.02	83.01	41.50	20.75	10.38	170000.00
1x	1328.13	664.06	332.03	166.02	83.01	41.50	20.75	340000.00

(1) TIME (T_{CONV}) – given by CREG1:TIME = 8 … 15 dec, N_{CLK} – number of clock cycle within conversion time T_{CONV}, RESOL – Resolution of internal A/D conversion, GAIN = 1x given by CREG1:GAIN = 11 dec up to GAIN = 2048x given by CREG1:GAIN = 0 dec (see Figure 48).

Figure 29:
UVB-Channel (λ = 280 nm – 315 nm) Programmable FSR and LSB of the Detectable Input Light Irradiance E_e

TIME(1)	0	1	2	3	4	5	6	7
N_{CLK}(1)	1024	2048	4096	8192	16384	32768	65536	131072
T_{CONV}[ms](1)	1	2	4	8	16	32	64	128
RESOL[bit](1)	10	11	12	13	14	15	16	17
GAIN(1)	FSR [µW/cm²] of detectable irradiance E_e (channel B)							
2048x	189.00(2)							94.50
1024x	378.00							189.00
512x	756.00							378.00
256x	1512.00							756.00
128x	3024.00							1512.00
64x	6048.00							3024.00
32x	12096.00							6048.00
16x	24192.00							12096.00
8x	48384.00							24192.00
4x	96768.00							48384.00
2x	193536.00							96768.00
1x	387072.00							193536.00
GAIN(1)	LSB [nW/cm²] – least significant bit of FSR (channel B)							
2048x	184.57	92.29	46.14	23.07	11.54	5.77	2.88	1.44
1024x	369.14	184.57	92.29	46.14	23.07	11.54	5.77	2.88
512x	738.28	369.14	184.57	92.29	46.14	23.07	11.54	5.77
256x	1476.56	738.28	369.14	184.57	92.29	46.14	23.07	11.54
128x	2953.13	1476.56	738.28	369.14	184.57	92.29	46.14	23.07
64x	5906.25	2953.13	1476.56	738.28	369.14	184.57	92.29	46.14
32x	11812.50	5906.25	2953.13	1476.56	738.28	369.14	184.57	92.29

TIME(1)	0	1	2	3	4	5	6	7
16x	23625.00	11812.50	5906.25	2953.13	1476.56	738.28	369.14	184.57
8x	47250.00	23625.00	11812.50	5906.25	2953.13	1476.56	738.28	369.14
4x	94500.00	47250.00	23625.00	11812.50	5906.25	2953.13	1476.56	738.28
2x	189000.00	94500.00	47250.00	23625.00	11812.50	5906.25	2953.13	1476.56
1x	378000.00	189000.00	94500.00	47250.00	23625.00	11812.50	5906.25	2953.13

(1) TIME (T_{CONV}) – given by CREG1:TIME = 0 … 7 dec, N_{CLK} – number of clock cycle within conversion time T_{CONV}, RESOL – Resolution of internal A/D conversion, GAIN = 1x given by CREG1:GAIN = 11 dec up to GAIN = 2048x given by CREG1:GAIN = 0 dec (see Figure 48).

(2) Basic sensitivity of the UVB-channel.

Figure 30:
UVB-Channel (λ = 280 nm – 315 nm) Programmable FSR and LSB of the Detectable Input Light Irradiance E_e

TIME(1)	8	9	10	11	12	13	14	15
N_{CLK}(1)	262144	524288	1.05E+06	2.10E+06	4.19E+06	8.39E+06	1.68E+07	1024
T_{CONV}[s](1)	0.256	0.512	1.024	2.048	4.096	8.192	16.384	0.001
RESOL[bit](1)	18	19	20	21	22	23	24	10
GAIN(1)	FSR [µW/cm²] of detectable irradiance E_e (channel B)							
2048x	47.25	23.63	11.81	5.91	2.95	1.48	0.74	189.00
1024x	94.50	47.25	23.63	11.81	5.91	2.95	1.48	378.00
512x	189.00	94.50	47.25	23.63	11.81	5.91	2.95	756.00
256x	378.00	189.00	94.50	47.25	23.63	11.81	5.91	1512.00
128x	756.00	378.00	189.00	94.50	47.25	23.63	11.81	3024.00
64x	1512.00	756.00	378.00	189.00	94.50	47.25	23.63	6048.00
32x	3024.00	1512.00	756.00	378.00	189.00	94.50	47.25	12096.00
16x	6048.00	3024.00	1512.00	756.00	378.00	189.00	94.50	24192.00
8x	12096.00	6048.00	3024.00	1512.00	756.00	378.00	189.00	48384.00
4x	24192.00	12096.00	6048.00	3024.00	1512.00	756.00	378.00	96768.00
2x	48384.00	24192.00	12096.00	6048.00	3024.00	1512.00	756.00	193536.00
1x	96768.00	48384.00	24192.00	12096.00	6048.00	3024.00	1512.00	387072.00
GAIN(1)	LSB [nW/cm²] – least significant bit of FSR (channel B)							
2048x	0.72	0.36	0.18	0.09	0.05	0.02	0.01	184.57
1024x	1.44	0.72	0.36	0.18	0.09	0.05	0.02	369.14
512x	2.88	1.44	0.72	0.36	0.18	0.09	0.05	738.28
256x	5.77	2.88	1.44	0.72	0.36	0.18	0.09	1476.56
128x	11.54	5.77	2.88	1.44	0.72	0.36	0.18	2953.13
64x	23.07	11.54	5.77	2.88	1.44	0.72	0.36	5906.25

TIME(1)	8	9	10	11	12	13	14	15
32x	46.14	23.07	11.54	5.77	2.88	1.44	0.72	11812.50
16x	92.29	46.14	23.07	11.54	5.77	2.88	1.44	23625.00
8x	184.57	92.29	46.14	23.07	11.54	5.77	2.88	47250.00
4x	369.14	184.57	92.29	46.14	23.07	11.54	5.77	94500.00
2x	738.28	369.14	184.57	92.29	46.14	23.07	11.54	189000.00
1x	1476.56	738.28	369.14	184.57	92.29	46.14	23.07	378000.00

(1) TIME (T_{CONV}) – given by CREG1:TIME = 8 … 15 dec, N_{CLK} – number of clock cycle within conversion time T_{CONV}, RESOL – Resolution of internal A/D conversion, GAIN = 1x given by CREG1:GAIN = 11dec up to GAIN = 2048x given by CREG1:GAIN = 0 dec (see Figure 48).

Figure 31:
UVC-Channel (λ = 240 nm – 280 nm) Programmable FSR and LSB of the Detectable Input Light Irradiance E_e

TIME(1)	0	1	2	3	4	5	6	7
N_{CLK}(1)	1024	2048	4096	8192	16384	32768	65536	131072
T_{CONV}[ms](1)	1	2	4	8	16	32	64	128
RESOL[bit](1)	10	11	12	13	14	15	16	17
GAIN(1)	FSR [µW/cm²] of detectable irradiance E_e (channel C)							
2048x	83.00(2)				41.50			
1024x	166.00				83.00			
512x	332.00				166.00			
256x	664.00				332.00			
128x	1328.00				664.00			
64x	2656.00				1328.00			
32x	5312.00				2656.00			
16x	10624.00				5312.00			
8x	21248.00				10624.00			
4x	42496.00				21248.00			
2x	84992.00				42496.00			
1x	169984.00				84992.00			
GAIN(1)	LSB [nW/cm²] – least significant bit of FSR (channel C)							
2048x	81.05	40.53	20.26	10.13	5.07	2.53	1.27	0.63
1024x	162.11	81.05	40.53	20.26	10.13	5.07	2.53	1.27
512x	324.22	162.11	81.05	40.53	20.26	10.13	5.07	2.53
256x	648.44	324.22	162.11	81.05	40.53	20.26	10.13	5.07
128x	1296.88	648.44	324.22	162.11	81.05	40.53	20.26	10.13
64x	2593.75	1296.88	648.44	324.22	162.11	81.05	40.53	20.26

TIME(1)	0	1	2	3	4	5	6	7
32x	5187.50	2593.75	1296.88	648.44	324.22	162.11	81.05	40.53
16x	10375.00	5187.50	2593.75	1296.88	648.44	324.22	162.11	81.05
8x	20750.00	10375.00	5187.50	2593.75	1296.88	648.44	324.22	162.11
4x	41500.00	20750.00	10375.00	5187.50	2593.75	1296.88	648.44	324.22
2x	83000.00	41500.00	20750.00	10375.00	5187.50	2593.75	1296.88	648.44
1x	166000.00	83000.00	41500.00	20750.00	10375.00	5187.50	2593.75	1296.88

(1) TIME (T_{CONV}) – given by CREG1:TIME = 0 … 7 dec, N_{CLK} – number of clock cycle within conversion time T_{CONV}, RESOL – Resolution of internal A/D conversion, GAIN = 1x given by CREG1:GAIN = 11 dec up to GAIN = 2048x given by CREG1:GAIN = 0 dec (see Figure 48).

(2) Basic sensitivity of the UVC-channel.

Figure 32:
UVC-Channel (λ = 240 nm – 280 nm) Programmable FSR and LSB of the Detectable Input Light Irradiance E_e

TIME(1)	8	9	10	11	12	13	14	15
N_{CLK}(1)	262144	524288	1.05E+06	2.10E+06	4.19E+06	8.39E+06	1.68E+07	1024
T_{CONV}[s](1)	0.256	0.512	1.024	2.048	4.096	8.192	16.384	0.001
RESOL[bit](1)	18	19	20	21	22	23	24	10
GAIN(1)	FSR [µW/cm²] of detectable irradiance E_e (channel C)							
2048x	20.75	10.38	5.19	2.59	1.30	0.65	0.32	83.00
1024x	41.50	20.75	10.38	5.19	2.59	1.30	0.65	166.00
512x	83.00	41.50	20.75	10.38	5.19	2.59	1.30	332.00
256x	166.00	83.00	41.50	20.75	10.38	5.19	2.59	664.00
128x	332.00	166.00	83.00	41.50	20.75	10.38	5.19	1328.00
64x	664.00	332.00	166.00	83.00	41.50	20.75	10.38	2656.00
32x	1328.00	664.00	332.00	166.00	83.00	41.50	20.75	5312.00
16x	2656.00	1328.00	664.00	332.00	166.00	83.00	41.50	10624.00
8x	5312.00	2656.00	1328.00	664.00	332.00	166.00	83.00	21248.00
4x	10624.00	5312.00	2656.00	1328.00	664.00	332.00	166.00	42496.00
2x	21248.00	10624.00	5312.00	2656.00	1328.00	664.00	332.00	84992.00
1x	42496.00	21248.00	10624.00	5312.00	2656.00	1328.00	664.00	169984.00
GAIN(1)	LSB [nW/cm²] – least significant bit of FSR (channel C)							
2048x	0.32	0.16	0.08	0.04	0.02	0.01	0.00	81.05
1024x	0.63	0.32	0.16	0.08	0.04	0.02	0.01	162.11
512x	1.27	0.63	0.32	0.16	0.08	0.04	0.02	324.22
256x	2.53	1.27	0.63	0.32	0.16	0.08	0.04	648.44
128x	5.07	2.53	1.27	0.63	0.32	0.16	0.08	1296.88

64x	10.13	5.07	2.53	1.27	0.63	0.32	0.16	2593.75
32x	20.26	10.13	5.07	2.53	1.27	0.63	0.32	5187.50
16x	40.53	20.26	10.13	5.07	2.53	1.27	0.63	10375.00
8x	81.05	40.53	20.26	10.13	5.07	2.53	1.27	20750.00
4x	162.11	81.05	40.53	20.26	10.13	5.07	2.53	41500.00
2x	324.22	162.11	81.05	40.53	20.26	10.13	5.07	83000.00
1x	648.44	324.22	162.11	81.05	40.53	20.26	10.13	166000.00

(1) TIME (T_{CONV}) – given by CREG1:TIME = 8 … 15 dec, N_{CLK} – number of clock cycle within conversion time T_{CONV}, RESOL – Resolution of internal A/D conversion, GAIN = 1x given by CREG1:GAIN = 11 dec up to GAIN = 2048x given by CREG1:GAIN = 0 dec (see Figure 48).

In the SYND mode, the maximum value of the conversion result depends on the externally controlled conversion time. This maximum achievable count is equal to OUTCONV and differs from the full-scale count achievable in CMD, CONT, and SYNS modes.

The value of CREG1:TIME defines the number of clock counts during the conversion time. It defines the conversion time duration and maximal resolution of the A/D conversion. This is valid for the CONT, CMD, and SYNS modes.

In the SYND mode, the value of CREG1:TIME does not have any meaning for the conversion time duration, because this time is externally defined.

For values of CREG1:TIME higher than 6 dec (0110b), T_{CONV} becomes bigger than 2^{16}, which results in A/D conversions with a higher resolution starting from 17-bit up to 24-bit. Only the least 16 significant bits are further processed and stored in the result registers. Using the implemented divider (see chapter 7.5) helps to access the upper 8-bits, too.

The value of CREG1:GAIN defines the A/D converter's gain (see Figure 48 and the FSR values in Figure 27 to Figure 32), which determines the sensor's irradiance responsivity R_e. The values of CREG1:GAIN, of the referred tables, are only valid for a clock frequency $f_{CLK,}$ of 1 MHz. For higher clock frequencies, some gain increments are not accessible. Figure 33 shows the valid gains dependent on the chosen internal system clock via CREG3:CCLK.

Figure 33:
Achievable GAIN for Different Internal Clock Frequencies Chosen by CREG3:CCLK

CREG3:CCLK [dec]	0	1	2	3
f_{CLK} [MHz]	1.024	2.048	4.096	8.192
CREG1:GAIN [dec]		Adjustable GAIN		
0	2048x	1024x	512x	256x
1	1024x			
2	512x	512x		
3	256x	256x	256x	
4	128x	128x	128x	64x
5	64x	64x	64x	
6	32x	32x	32x	16x
7	16x	16x	16x	
8	8x	8x	8x	4x
9	4x	4x	4x	
10	2x	2x	2x	1x
11	1x	1x	1x	

During the measurement cycle, within the conversion time T_{CONV}, an input signal overdrive must be avoided - even if it occurs limited in time, related to T_{CONV}. In this case, the input light is too much concerning the chosen irradiance responsivity R_e, of the AS7331 tolerates. An internal function of the analog conversion monitors all channels during the conversion process, in terms of the relation of input light and chosen irradiance responsivity R_e, determined via CREG1:GAIN. In case the input light of at least one of the channels is too much, the status bit STATUS:ADCOF (see Figure 55) is set to signal the problem and the chosen GAIN of the A/D converter (CREG1:GAIN) has to be decreased, to reduce the irradiance responsivity R_e, of the sensor.

7.5 Divider

To expand the measurement ranges, an internally implemented divider or pre-scaler can be used to scale the results. This might be necessary if the resolution of the conversion is set to a value higher than 16 bits. If the digital divider is used, the conversion result is downscaled according to the equation:

Equation 5:

$$E_e = \frac{2^{1+DIV[\text{dec}]} \bullet MRES}{R_e} = \frac{FSR_{E_e}}{N_{CLK}} \bullet 2^{1+DIV[\text{dec}]} \bullet MRES$$

Where:

MRES = Digital output value of the conversion (content of output registers MRES1 to MRES3).

E_e = Input light irradiance regarding the photodiode's area within the conversion time interval.

FSR_{Ee} = Full Scale Range of detectable input light irradiance E_e.

R_e = Irradiance responsivity (see Figure 48).

N_{CLK} = Number of clock cycles within the conversion time interval T_{CONV} (see Figure 48).

$2^{1+DIV[dec]}$ = Value of the divider factor respectively prescaler (CREG2:DIV = 7…0), see Figure 49.

The A/D converters of the AS7331 operate with a resolution of 24 bits, but their results are only provided as 16-bit wide values. The divider allows you to read out the otherwise unavailable upper 8 bits, depending on the value of CREG2:DIV if CREG2:EN_DIV is set to "1".

Therefore, the divider acts as a feature to digitally downscale the converter gain, but with a larger full-scale range (FSR). The effective dynamic range of the device is increased without changing the conversion time.

Figure 34:
Relation of the Measurement Result to the Conversion Time Without Divider Respectively Prescaler

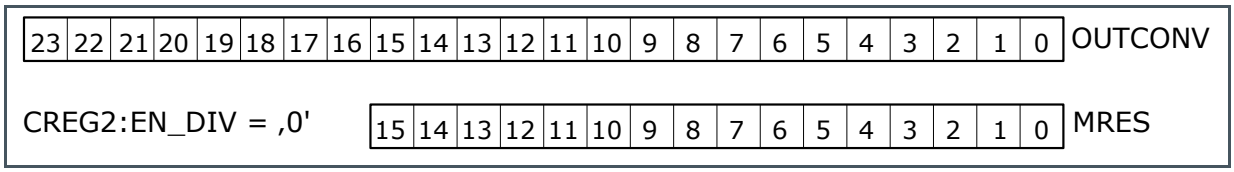
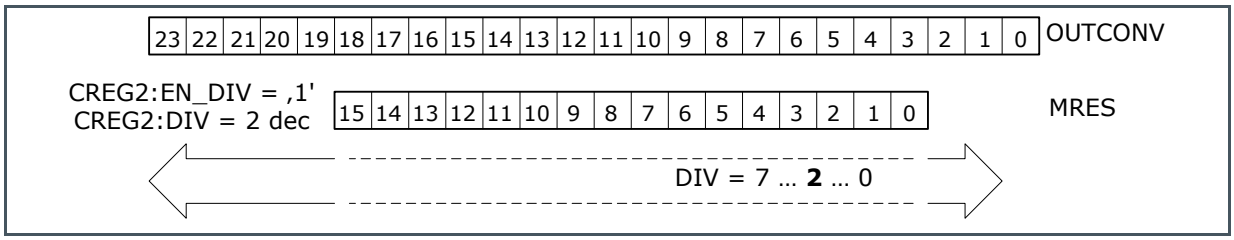


Figure 34 shows the width of the register for the conversion time (OUTCONV), which represents the internal resolution of the A/D conversion. Furthermore, the measurement result (MRES[1…3]) is shown, which is 16-bit wide. For all conversion times from 2^{10} to 2^{16}, there is no need to use the divider, because OUTCONV is limited to the conversion time length.

For conversion times bigger than 2^{16}, the conversion result is longer than 16 bits. Without the function of the divider, the result always contain the 16 least significant bits. The divider makes it possible to access the most significant bits by shifting the 16-bit resolution of the measurement result over the possible range of the resolution given by the conversion time register (OUTCONV).

Figure 35 shows an example, where CREG2:DIV = 2 dec, and therefore the divider factor is 2^3. Thus, MRES corresponds to the bits 18 to 3 of register OUTCONV, making the least significant bits and the full-scale range eight times higher than if the divider is not used.

Figure 35:
Relation of the Measurement Result to the Conversion Time with Enabled and Set Divider



7.6 Conversion Time Measurement in SYND Mode

In the case of SYND measurement mode, the conversion time is fully controlled by the external signal at the SYN pin. The relative deviation of this time to the internal clock frequency[2] can produce some deviations in the conversion result. However, this time can be measured in time units of the internal system clock extended up to 24 bits. It allows for the recalculation of the measured input light more precisely (see chapter 7.4). Furthermore, the measurement result can be compensated for any deviation, which can occur in the clock frequency due to temperature or supply voltage variations. The conversion time measurement can be enabled by setting bit CREG2:EN_TM bit to “1” (see Figure 49). At the end of the conversion, the result is stored into the output register, OUTCONV, (see Figure 54) synchronously with the measurement results (MRES).

The stored value follows the relation:

Equation 6:

$$OUTCONV = T_{CONV} \bullet f_{CLK}$$

The bit STATUS:OUTCONVOF of the status register (see Figure 55) shows an overflow of the conversion time counter, OUTCONV. In case it happens and the conversion is still in process, the counter, OUTCONV, starts again at 0. For the calculation of the full-scale range (FSR) see Equation 2, Equation 3, Equation 4 in chapter 7.4.

7.7 Temperature Measurement

In addition to the three optical channels, a temperature measurement is done in parallel. The measurement result is available as TEMP of the output result registers. The resolution of the temperature measurement is 12 bits by a step size of 0.05 K per bit, which means 20 counts per Kelvin. The value of the chip temperature (silicon – measured in °C) is equal to:

[2] The system clock is internally generated and is subject to technological tolerances, which means that clock frequencies of different devices may vary.

Equation 7:

$$T_{CHIP} = TEMP \bullet 0.05°C - 66.9°C$$

In other words TEMP = 922h (2338 dec) corresponds to 50 °C as a reference point to start calculations.

The temperature measurement is available in the measurement modes CONT, CMD, and SYNS. With the values of CREG1:TIME < 2 dec, the resolution of the temperature measurement is reduced, but in this case, the output value of TEMP is internally corrected.

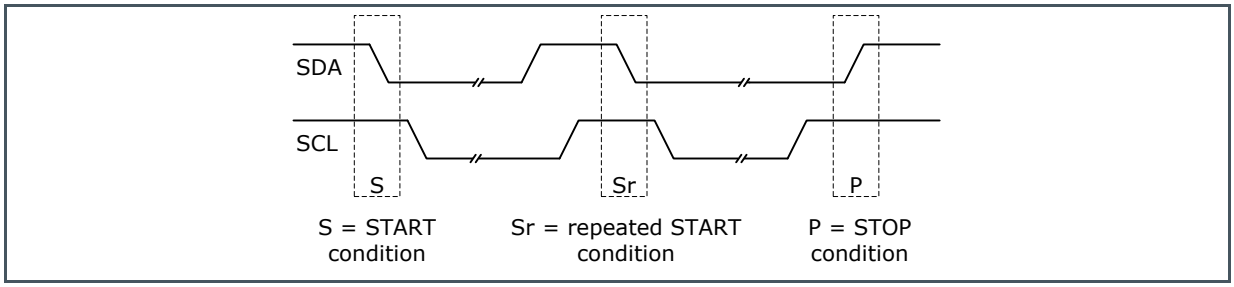
In the SYND measurement mode, it is important to enable the conversion time measurement (CREG2:EN_TM = “1”) to get any result of the temperature measurement. In addition, the value of output register, OUTCONV has to be more than 2^{12}, given by the external conversion time at the SYN pin.

7.8 I²C Communication

The two-wired serial interface is compatible with the fast mode I²C protocol, with a bit rate of up to 400 kbit/s. The AS7331 exclusively operates as a slave with its slave address [6:0] = (1, 1, 1, 0, 1, A1, A0). The input pins A1 and A0, which allows running four AS7331 on the same I²C bus concurrently, define the two lowest-order bits. Within the AS7331, the SCL pin of the I²C interface is realized as an input pin, where in single master applications, the I²C master could drive the SCL line with a push-pull stage. In all other cases, the requirements for bus termination using standard pull-up according to the I²C (pins SCL and SDA) should be considered - especially regarding noise environments and EMC in PCB design. For the I²C interface, the timing diagram and its timing specification, please see Figure 39. Clock stretching is not supported by the AS7331. I²C commands towards the AS7331 take effect after the end of the I²C write cycle (I²C Stop condition).

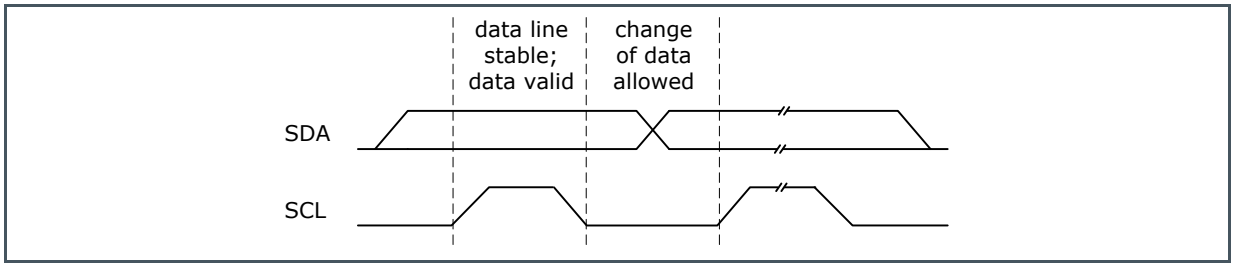
Each data transfer begins with a start (S) condition, defined by a high to low transition of SDA while SCL is high. The transfer is terminated by a stop (P) condition, which is defined by a low to high transition of SDA while SCL is high. A repeated start condition (Sr) can be generated instead of a stop condition if the transfer should be continued with a new data block. The start and repeated start conditions are functionally equivalent.

Figure 36:
Start and Stop Conditions of the I²C Bus



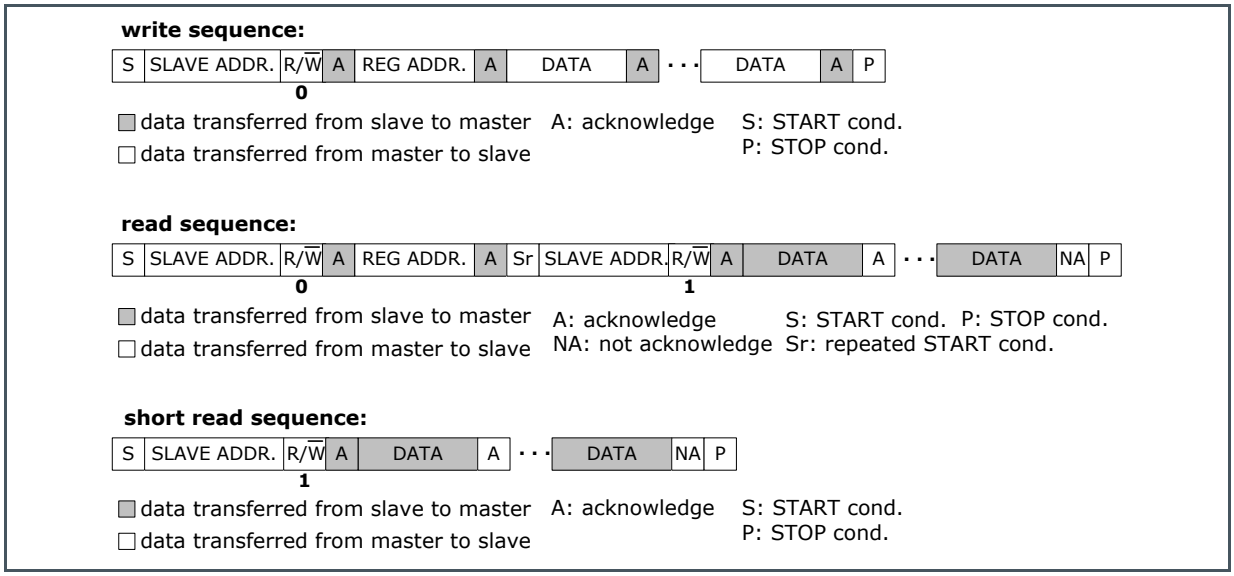
After the protocol starts, the data at the SDA pin must be fully stable during the high phase of the I²C clock at the SCL pin. The change of the communication data at the SDA pin is only allowed during the low phase of the SCL clock.

Figure 37:
Bit – Transfer on I²C Bus



Each data transfer consists of 1 byte, which has to be followed by an acknowledge bit (A) (see Figure 38). The bits arrive with the MSB first. The acknowledge signal shall be pulled low by the receiver during the high period of the ninth clock pulse while the transmitter releases the SDA line. When SDA stays high during the ninth clock pulse, the not acknowledge signal (NA) is output. After the not acknowledge signal, the master generates either a stop or a repeated start condition, depending on whether the master either wants to abort or start a new transfer. In the case of the AS7331 as a slave, a not acknowledge (NA) is only generated if the device address did not match.

Figure 38:
I²C Write and Read Sequences



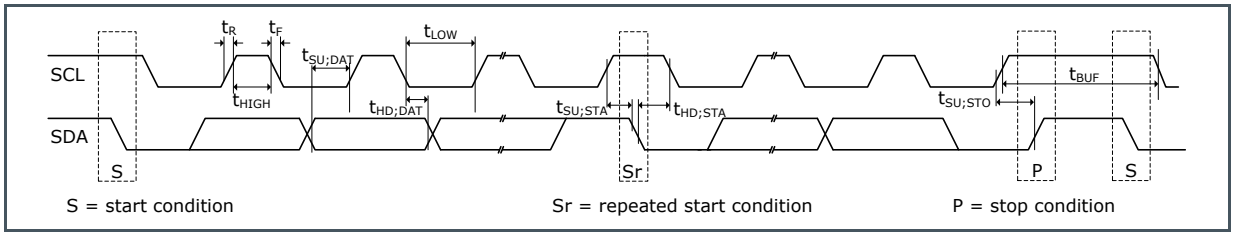
7.8.1 I²C Timing Characteristics

Figure 39:
I²C Slave Timing Characteristics of the AS7331

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	I²C Clock Frequency at SCL.	R_{PULLUP} ≥ 820 Ω $CL_{(SCL, SDA)}$ ≤ 400 pF			400	kHz
t_{HIGH}	SCL High Pulse Width.		0.6			µs
t_{LOW}	SCL Low Pulse Width.		1.3			µs
t_R	SCL and SDA Rise Time.				0.3	µs
t_F	SCL and SDA Fall Time.				0.3	µs
$t_{HD;STA}$	Hold Time Start Condition.		0.6			µs
$t_{SU;SDA}$	Setup Time Start Condition.		0.6			µs
$t_{HD;DATM}$	SDA Data Hold Time (Master).	Data transfer from master to slave	0.02			µs
$t_{HD;DATS}$	SDA Data Hold Time (Slave).	Data transfer from slave to master	0.3		0.9	µs
$t_{SU;DAT}$	Data Setup Time.		0.1			µs
$t_{SU;STO}$	Setup Time Stop Condition.		0.6			µs
t_{BUF}	Bus Free Time between a Stop and a Start Condition.		1.3			µs

7.8.2 I²C Timing Diagrams

Figure 40:
I²C Slave Timing Diagram



7.8.3 I²C Write Protocol

The start byte consists of the slave address followed by the bit R/W set to “0” for the write direction. The first byte after the start byte is always the address pointer to the internal register, which the master wants to write. When the master sends the next byte, it is stored in the internal register,

addressed by the address pointer (REG ADDR.) before. Then acknowledge is sent by the device, and it internally increments the address pointer to the next internal register address. Each next data byte, which is transferred by the master, is sequentially stored in the internal register.

If the master generates a stop condition, the transfer is aborted, and a new write sequence must be started from the beginning.

7.8.4 I²C Read Protocol

The start byte consists of the slave address followed by the bit R/W set to “0” for the write direction. The first byte after the start byte is always the address pointer to the internal register, which the master wants to read and acknowledge. After that, the master sends a repeated start condition and repeats the slave address but with the bit R/W reversed. An acknowledge is then sent by the slave, which starts the data transfer to the master. The first transferred byte is the content of the internal register, which was pointed by the address pointer. Then the master acknowledges each transferred byte. The internal address pointer of the AS7331 automatically increments after each transferred register, which allows a sequential read-out of the internal registers. If a not acknowledge occurs from the master, it sends the stop condition next and the transfer is finished.

A shortened read sequence is also possible, as shown in Figure 53. With the default of the bit OPTREG:INIT_IDX = “1” (see Figure 53) the internal address pointer starts at register address 2h, if the Measurement state is activated (OSR:DOS = 011b). In the case the Configuration state is activated (OSR:DOS = 010b), the internal address pointer starts at register address 0h.

7.8.5 I²C Addressable Register Space

Figure 41 shows the overview of the internal registers of the AS7331, which can be accessed via the I²C interface. The control register bank can only be accessed in the configuration state, and the registers are all 8 bits long. The output registers can only be accessed in the measurement state. They are read-only registers and 16 bits long, except OUTCONV, which is 24 bits long.

OUTCONV is separated into two parts to fit into the output register’s structure. OUTCONV_L contains the first lower bytes, and OUTCONV_H contains the most significant byte of OUTCONV in the first byte. The second byte is 00h.

The AS7331 transfers the output data registers with the least significant byte first. The output register data transfer can start at any address. If during the sequential data read the highest possible address is achieved (CREG2:EN_TM = “0”: address 4h; CREG2:EN_TM = “1”: address 6h), the internal pointer is reset to the address 2h, so that the next transferred data byte corresponds to the low byte of MRES1. However, the maximum number of output data transferred must not exceed a total number of bytes accessible if all (6 bytes if conversion time measurement (CREG2:EN_TM) is not activated, otherwise 10 bytes). The register OUTCONV is only available in case bit CREG2:EN_TM is set to “1”.

Figure 41:
Register Access Overview

Address[1] [hex]	Access in Configuration State		Access in Measurement State	
	Write	Read	Write (1 Byte)	Read (2 Bytes)
0	OSR		OSR	OSR + STATUS
1	–		–	TEMP
2	–	AGEN	–	MRES1 (A)
3	–		–	MRES2 (B)
4	–		–	MRES3 (C)
5	–		–	OUTCONV_L[2]
6	CREG1		–	OUTCONV_H[2]
7	CREG2		–	–
8	CREG3		–	–
9	BREAK		–	–
A	EDGES		–	–
B	OPTREG		–	–

(1) The 4 MSB bits of the register address are ignored.
(2) OUTCONV is only available in SYND measurement mode with bit CREG2:EN_TM = “1”. The least significant byte comes first.

7.8.6 I²C General Procedure to Start with the AS7331

After applying the power supply voltage, the AS7331 is in the configuration state, but in the power down mode. The user can now set up the device for the application by writing the control registers. The success of the configuration can be proven by reading the control registers.

Before starting a measurement, the state must be changed to the Measurement state. The last three bits (DOS) of the register OSR should be loaded with 011b. Now a conversion can be started with the measurement mode, which is selected by CREG3:MMODE. A falling slope of the output pin READY indicates the start. The rising edge at pin READY signals the end of conversion, and the measurement results can be read via I²C communication.

If a new configuration should be implemented, the device’s state needs to be changed to the configuration state. Therefore the value 010b should be written into the bits OSR:DOS. This operation resets all measurement result registers to 00h, while the configuration registers keep their actual values. Afterward, the new configuration can be done.

Figure 42:
Example of Addressing the AS7331 to Read the Configuration Registers

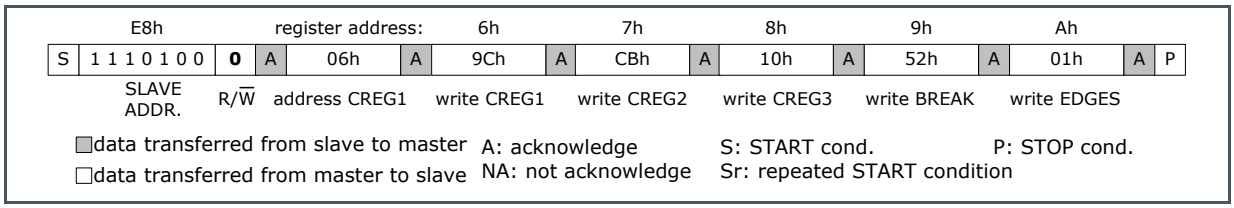
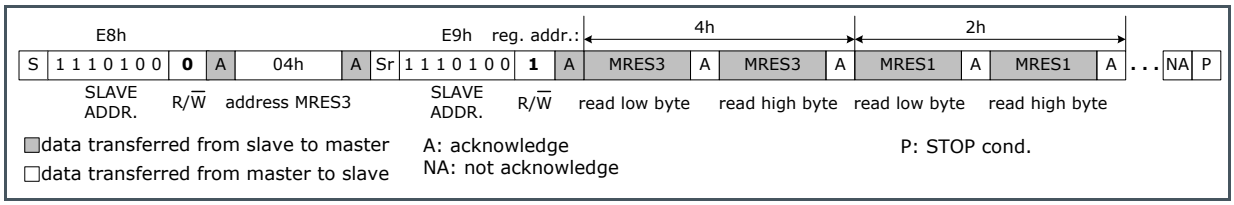


Figure 43:
Example of Addressing the AS7331 to Read the Measurement Result Registers Starting at Address 4h



The access of the result register bank with 2 byte addresses each (starting with the low byte), which is only possible within the measurement state, has a special feature (see Figure 43). After reaching the last valid result register address (4h or 6h if SYND mode is activated with CREG2:EN_TM = “1”) the next result register address is the default one, 2h, during read on. The setback of the result register address 2h in the measurement mode does not take place if an address was set above the valid addressable space.

8 Register Description

The device is controlled and monitored by registers accessed through the I²C interface. These registers provide device control functions and can be read to determine the device status and acquire device data.

The register set is summarized below in Figure 44. The values of all registers and fields that are listed as reserved, or are not listed, must not be changed. Two-byte fields are always latched with the low byte, followed by the high byte. The “Name” column illustrates the purpose of each register by highlighting the function associated with each bit. The bits are shown from MSB (D7) to LSB (D0). The grey fields are reserved, and their values must not be changed.

8.1 Register Overview

Figure 44:
Register Overview

Addr [hex]	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0	**OSR**	SS	PD			SW_RES	DOS		
2	**AGEN**	DEVID				MUT			
6	**CREG1**	GAIN				TIME			
7	**CREG2**		EN_TM			EN_DIV	DIV		
8	**CREG3**	MMODE			SB	RDYOD		CCLK	
9	**BREAK**	BREAK							
A	**EDGES**	EDGES							
B	**OPTREG**								INIT_IDX

8.2 Detailed Register Description

8.2.1 Operational State Register - OSR (Address 0h)

Figure 45:
Operational State Register

Addr: 0h		OSR			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7	SS	0	RW	**Number**	**Function**
				0	Stop of measurement.
				1	Start of measurement (only if DOS = MEASUREMENT).
6	PD	1	RW	**Number**	**Function**
				0	Power Down state switched OFF.
				1	Power Down state switched ON.
3	SW_RES	0	RW	Only active during write access, a read access always returns “0”.	
				Number	**Function**
				0	-
				1	Software reset
2:0	DOS	010	RW	Device operational state. The OSR result of a register read process always returns 010b or 011b for the DOS bits.	
				Number	**Function**
				00X	NOP (no change of DOS).
				010	Operational state: CONFIGURATION
				011	Operational state: MEASUREMENT
				1XX	NOP (no change of DOS).

DOS switches the operational state of the AS7331 between configuration and measurement. The configuration state enables access to the control register bank (Figure 44) and no measurement takes place. The measurement access to the result registers can only be performed in the measurement state. Then any access to the control register bank (except OSR) will not be possible. If the operational state is switched back to the configuration state by DOS = 010b, the control registers will keep their values and the measurement result registers will be cleared. Any ongoing measurement will

be stopped immediately. The DOS sequence, “NOP”, (00Xb or 1XXb) does not change the operational state, but the values of the other written OSR bits are effective.

Setting SW_RES to “1” causes a software reset of the AS7331. A running measurement stops immediately and the AS7331 is set to the configuration state and all registers are reset to their initial values. The start of measurement is controlled by the value of bit SS. This bit is only interpreted in the measurement state.

The power down mode is controlled by the value of the PD bit.

The power down takes effect in both operational states: configuration and measurement. If the power down state is switched on while the device is in measurement state, the power down is only performed during the breaks between two conversions.

Figure 46:
Examples for Programming the Operational State Registers at Address 0h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
SS	**PD**	**-**	**-**	**SW_RES**	**DOS**			**Operational State**	
0	1	-	-	0	0	1	0	Configuration state (Power Down state switched on)	42h
0	0	-	-	0	0	1	0	Configuration state (Power Down state switched off)	02h
0	0	-	-	0	0	1	1	Measurement state (Power Down state switched off)	03h
1	0	-	-	0	0	1	1	Measurement state and Start of measurement (Power Down state switched off)	83h
1	0	-	-	0	0	0	0	Provided that Measurement state is active – Start of measurement (Power Down state switched off)	80h
0	1	-	-	0	0	1	1	Measurement state (Power Down state switched on)	43h
1	1	-	-	0	0	1	1	Measurement state, Start of measurement and internal startup (“overwrite” of PD = “1”)	C3h
1	1	-	-	0	0	0	0	Provided that Measurement state is active – Start of measurement and internal startup (“overwrite” of PD = "1“)	C0h
(0)	(1)	-	-	1	(0)	(1)	(0)	Software reset	0Ah

8.2.2 API Generation Register - AGEN (Address 2h)

The value of this read-only register indicates the generation of the Control Register Bank. The register’s value changes whenever any formal modification is introduced to the Control Register Bank.

This case indicates that the Application Programming Interface (API) has been changed. The default value for the AS7331 is 21h.

Figure 47:
API Generation Register

Addr: 2h		AGEN		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	DEVID	0010	RO	Device ID number.
3:0	MUT	0001	RO	Mutation number of control register bank.

8.2.3 Configuration Register 1 – CREG1 (Address 6h)

CREG1:GAIN determines the irradiance responsivity of the sensor, which is different regarding the channels A, B, and C, and in each case regarding to the used wavelength λ. Internally the A/D converter runs with different gain factors concerning the bit CREG1:GAIN (see Figure 33).

CREG1:TIME controls the conversion time duration as a multiple of the internal clock periods. In case the start and end of measurement are controlled externally via the input trigger signal at the SYN pin (equal to SYND mode). CREG1:TIME does not influence the conversion time.

Figure 48:
Configuration Register 1

Addr: 6h		CREG1					
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**			
7:4	GAIN	1010	RW	Defines the irradiance responsivity of the AS7331. CREG1:TIME = 1010b (1024 ms) CREG3:CCLK = 00b (1 MHz)			
				Value [b]	**Index Channels A/B/C**	**Full Scale Range E_e [µW/cm²]**	**Effective LSB of FSR [nw/cm²]**
				0000	$GAIN_A$ = 2048x	10.63	0.16
					$GAIN_B$ = 2048x	11.81	0.18
					$GAIN_C$ = 2048x	5.19	0.08
				0001	$GAIN_A$ = 1024x	21.25	0.32
					$GAIN_B$ = 1024x	23.63	0.36
					$GAIN_C$ = 1024x	10.38	0.16

Addr: 6h		CREG1					
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**			
				0010	$GAIN_A$ = 512x	42.50	0.65
					$GAIN_B$ = 512x	47.25	0.72
					$GAIN_C$ = 512x	20.75	0.32
				0011	$GAIN_A$ = 256x	85.00	1.30
					$GAIN_B$ = 256x	94.50	1.44
					$GAIN_C$ = 256x	41.50	0.63
				0100	$GAIN_A$ = 128x	170.00	2.59
					$GAIN_B$ = 128x	189.00	2.88
					$GAIN_C$ = 128x	83.00	1.27
				0101	$GAIN_A$ = 64x	340.00	5.19
					$GAIN_B$ = 64x	378.00	5.77
					$GAIN_C$ = 64x	166.00	2.53
				0110	$GAIN_A$ = 32x	680.00	10.38
					$GAIN_B$ = 32x	756.00	11.54
					$GAIN_C$ = 32x	332.00	5.07
				0111	$GAIN_A$ = 16x	1360.00	20.75
					$GAIN_B$ = 16x	1512.00	23.07
					$GAIN_C$ = 16x	664.00	10.13
				1000	$GAIN_A$ = 8x	2720.00	41.50
					$GAIN_B$ = 8x	3024.00	46.14
					$GAIN_C$ = 8x	1328.00	20.26
				1001	$GAIN_A$ = 4x	5440.00	83.01
					$GAIN_B$ = 4x	6048.00	92.29
					$GAIN_C$ = 4x	2656.00	40.53
				1010	$GAIN_A$ = 2x	10880.00	166.02
					$GAIN_B$ = 2x	12096.00	184.57
					$GAIN_C$ = 2x	5312.00	81.05
				1011	$GAIN_A$ = 1x	21760.00	332.03
					$GAIN_B$ = 1x	24192.00	369.14
					$GAIN_C$ = 1x	10624.00	162.11
3:0	TIME	0110	RW	Defines the integration time of the AS7331 measurement.			
				Conversion time (f_{CLK} = 1024 MHz)			

Addr: 6h	CREG1						
Bit	Bit Name	Default	Access	Bit Description			
				Value [b]	Value [dec]	T_{CONV} in ms	Number of clocks
				0000	0	1	1024 2^{10}
				0001	1	2	2048 2^{11}
				0010	2	4	4096 2^{12}
				0011	3	8	8192 2^{13}
				0100	4	16	16384 2^{14}
				0101	5	32	32768 2^{15}
				0110	6	64	65536 2^{16}
				0111	7	128	131072 2^{17}
				1000	8	256	262144 2^{18}
				1001	9	512	524288 2^{19}
				1010	10	1024	1048576 2^{20}
				1011	11	2048	2097152 2^{21}
				1100	12	4096	4194304 2^{22}
				1101	13	8192	8388608 2^{23}
				1110	14	16384	16777216 2^{24}
				1111	15	1	1024 2^{10}

8.2.4 Configuration Register 2 – CREG2 (Address 7h)

In general, the registers CREG2 and CREG3 define the measurement modes and additional device specific options.

Figure 49:
Configuration Register 2

Addr: 7h	CREG2				
Bit	Bit Name	Default	Access	Bit Description	
				Value	Function
6	EN_TM	1	RW	0	In combination with SYND mode, the internal measurement of the conversion time is disabled and no temperature measurement takes place.

Addr: 7h		CREG2			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
				1	Internal measurement of the externally defined conversion time via SYN pulse in SYND mode is enabled (OUTCONV results are generated as well as temperature values for output register TEMP).
3	EN_DIV	0	RW	**Value**	**Function**
				0	Digital divider of the measurement result registers is disabled.
				1	Digital divider of the measurement result registers is enabled (might be needed @ CREG1:TIME > 6 dec).
2:0	DIV	000	RW	**Value**	**Value of the divider ($2^{1+DIV[dec]}$)**
				000	2^1
				001	2^2
				010	2^3
				011	2^4
				100	2^5
				101	2^6
				110	2^7
				111	2^8

In SYND mode, the conversion time is externally controlled via pin SYN. In that case, the bit CREG2:EN_TM enables the counting of internal clocks within the externally given conversion time, as well as the access to the output register, OUTCONV, which contains the counting result. It is possible to count several clocks up to 24 bits. In case this function is not used in SYND mode (equal to CREG2:EN_TM = “0”), no result for temperature measurement is generated and the values for the output register TEMP will not be valid.

The bit CREG2:EN_DIV enables the internal prescaler, which could be interesting for conversion times more than 16-bits (CREG1:TIME ≥ 0111b) and if SYND mode is used. The value of CREG2:DIV is only valid with CREG2:EN_DIV = “1”. Then the measurement range is extended while the resolution of the 16-bit register results is reduced at the same time (see chapter 7.5). Thus, it is also possible to generate complete measurement results for conversion times from 2^{17} to 2^{24} system clocks (CREG1:TIME). If the chosen value of the prescaler is too small, a counter overflow could occur, which is shown by the bit STATUS:MRESOF of the result register bank.

8.2.5 Configuration Register 3 – CREG3 (Address 8h)

Figure 50:
Configuration Register 3

Addr: 8h		CREG3			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:6	MMODE	01	RW	**Value [b]**	**Function**
				00	CONT mode (continuous measurement).
				01	CMD mode (measurement per command).
				10	SYNS mode (externally synchronized start of measurement).
				11	SYND mode (start and end of measurement are externally synchronized).
4	SB	0	RW	**Value [b]**	**Function**
				0	Standby is switched OFF.
				1	Standby is switched ON.
3	RDYOD	0	RW	**Value [b]**	**Function**
				0	Pin READY operates as Push Pull output.
				1	Pin READY operates as Open Drain output.
1:0	CCLK	00	RW	**Value [b]**	**Internal clock frequency f_{CLK}**
				00	1.024 MHz
				01	2.048 MHz
				10	4.096 MHz
				11	8.192 MHz

The bits CREG3:MMODE specify the measurement mode, which should be compatible with the given application.

The bit CREG3:SB controls the operational state Standby of the AS7331. In the Standby state the power consumption of the device is reduced, but the internal circuit is ready to continue after 4 µs wake-up time by switching off Standby.

With bit CREG3:RDYOD the output READY pin can be changed from push-pull to open-drain behavior. The open-drain output allows running two or more AS7331 simultaneously whilst connected

to one READY line with a pull-up resistor. As long as one device still measures, the READY line is active low.

The internal clock frequency f_{CLK}, is controlled by the bits of CREG3:CCLK. Higher clock rates result in shorter conversion times for the measurement. However take care of CREG1:GAIN – with higher frequencies than 1 MHz, in some cases, the irradiance responsivity is reduced (see Figure 33).

8.2.6 BREAK Register (Address 9h)

The register BREAK defines the time between two consecutive measurements of CONT, SYNS, and SYND modes.

Figure 51:
BREAK Register

Addr: 9h		BREAK			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
				Value [dec]	**Function**
7:0	BREAK	19h	RW	0…255	Break time T_{BREAK} between two measurements (except CMD mode): from 0 to 2040 µs, step size 8 µs. The value 0h results in a minimum time of 3 clocks of f_{CLK}.

8.2.7 EDGES Register (Address Ah)

The register EDGES becomes operative in SYND mode. After a measurement was started in SYND mode, it defines the necessary number of additional falling edges at input SYN until the conversion is terminated. The value EDGES = “0” is not allowed and results in the initial value “1”.

Figure 52:
EDGES Register

Addr: Ah		EDGES			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
				Value [dec]	**Function**
7:0	EDGES	01h	RW	1…255	Number of SYN falling edges.

8.2.8 Option Register - OPTREG (Address Bh)

The register bit OPTREG:INIT_IDX allows to communicate via the I²C with simple masters, which do not support the I²C repeated START condition. In this case, the start address for a read operation can only be set by complete write access with the I²C STOP condition at the end. For this kind of simple I²C master, the bit INIT_IDX has to be “0”. Then, the reading of data starts at the given index address. After each data transfer, the index address is incremented.

With INIT_IDX set to “1”, each short read operation starts at the default address 2h in Measurement mode and 0h in Configuration mode. The setting of the internal read index address followed by the I²C repeated START condition, works as usual. After each data transfer, the index address is incremented. Please also see chapter 7.8.4.

Figure 53:
Option Register

Addr: Bh		OPTREG		
Bit	**Bit Name**	**Default [b]**	**Access**	**Bit Description**
7:1	-	0111001	-	Reserved (Default value after power-on reset and software reset, but different, irrelevant values after changing CREG1:GAIN or CREG3:CCLK. The recommended write value is 0000000b in case of OPTREG:INIT_IDX should be changed.)

Addr: Bh		OPTREG			
Bit	**Bit Name**	**Default [b]**	**Access**	**Bit Description**	
				Value [b]	**Function**
0	INIT_IDX	1	RW	0	Defining the index address is only possible via write sequence and not affected by I²C STOP condition, which is necessary, if the I²C master does not support the I²C repeated START condition.
				1	Each I²C STOP condition sets the internal register address to the default value. After writing an index address, it is possible to change the data direction for reading using I²C repeated START condition.

8.2.9 Output Register Bank

All output result registers are 16-bit registers. The read access of the registers is only possible if the Measurement state is activated. One exception offers register OSR, which is also writable. In that case, one byte is assigned to the address 0h (see chapter 8.2.1). However, the read access of address 0h in the Measurement state results in the first byte for OSR information and the second byte for STATUS information.

Figure 54:
Output Result Register Bank

Address(1) [hex]	Access(2)	Name	Number of Bits	Description
0	RW	OSR	8(1)	Operational State Register.
	RO	STATUS	8(1)	Status Register.
1	RO	TEMP	16(2)	Temperature Measurement Result (0h + 12 bits for the value).
2	RO	MRES1	16(2)	Measurement Result A-Channel.
3	RO	MRES2	16(2)	Measurement Result B-Channel.
4	RO	MRES3	16(2)	Measurement Result C-Channel.
5	RO	OUTCONVL	16(2)	Time reference, result of conversion time measurement (least significant byte and middle byte).

Address[1] [hex]	Access[2]	Name	Number of Bits	Description
6	RO	OUTCONVH	16[2]	Time reference, result of conversion time measurement (most significant byte and one empty byte with 00h).

(1) Read access of address 0h in measurement state results in a first byte for OSR information and a second byte for STATUS information.
(2) The Least Significant Byte comes first.

STATUS Register (Address 0h)

Figure 55:
STATUS Register

Addr: 0h		STATUS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	OUTCONVOF[1][2]	-	RO	Digital overflow of the internal 24-bit time reference OUTCONV.
6	MRESOF[2]	-	RO	Overflow of at least one of the measurement result registers MRES1 … MRES3.
5	ADCOF[2]	-	RO	Overflow of at least one of the internal conversion channels during the measurement (e.g. caused by pulsed light) – analog evaluation is made.
4	LDATA[3]	-	RO	Measurement results in the buffer registers were overwritten before they were transferred to the output result registers. A transfer takes place as part of an I²C read process of at least one register of the output register bank.
3	NDATA[4]	-	RO	New measurement results were transferred from the temporary storage to the output result registers.
2	NOTREADY	-	RO	Corresponds to the inverted signal at the output pin READY. **Value** / **Function** 0 – Measurement progress is finished or not started yet.

Addr: 0h		STATUS			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
				1	Measurement is in progress.
1	STANDBYSTATE	-	RO	**Value**	**Standby**
				0	OFF
				1	ON
0	POWERSTATE	-	RO	**Value**	**Power Down state**
				0	OFF
				1	ON

(1) Overflow of the internal 24-bit conversion time counter – only possible in SYND mode with externally synchronized start and stop of conversion.
(2) The status flag is generated while a measurement is in progress. It always matches to the actual results of the output register bank.
(3) A reading process of the register STATUS always resets this status flag.
(4) A reading process of the register STATUS and/or at least one result register always resets this status flag.

The bit STATUS:OUTCONVOF, shows an overflow of the 24-bit counter of the internal reference for the conversion time. This can only occur in SYND mode with CREG2:EN_TM = “1” and in case of accordingly long externally given conversion times. After a counter overflow, the counter starts again from zero.

The bit STATUS:MRESOF, shows an overflow in one or more result registers of MRES1 … MRES3. This can only happen if the conversion time is longer than 2^{16} (CREG1:TIME = 7…15 dec), in accordance with a higher input signal. The overflowed register stops at its maximum value, FFFFh.

With the bit STATUS:ADCOF, an input signal overdrive is signalized, which could occur during the measurement cycle limited in time so that no overflow of the result registers (MRESOF) is necessarily produced. However, the measurement results are not correct in this case. To eliminate this issue, the irradiance responsivity (R_e) of the sensor has to be decreased via CREG1:GAIN.

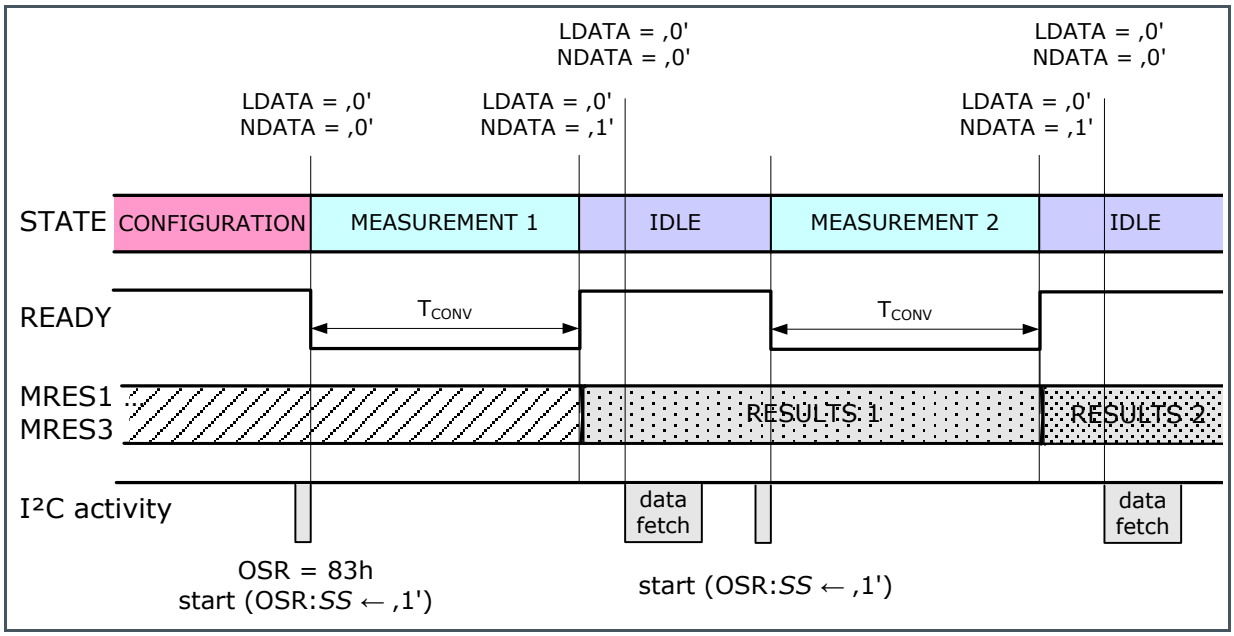
The status bits OUTCONVOF, MRESOF, and ADCOF, always correspond to the actual content of the measurement result registers MRES1…3.

The bits STATUS:LDATA and STATUS:NDATA, show the status of the measurement results. At the end of each measurement cycle, the results of the counters are stored in buffer registers. The flag NDATA is set to “1” to show the update (see Figure 56). With the start of each I²C read operation, the content of all buffer registers is transferred to the result registers. This ensures that during the I²C readout operation, the values of the result registers do not change.

As long as an I²C-reading of the measurement result registers is in the process (no I²C stop condition has been sent), no further update of the measurement result registers concerning newer data of the buffer registers will happen.

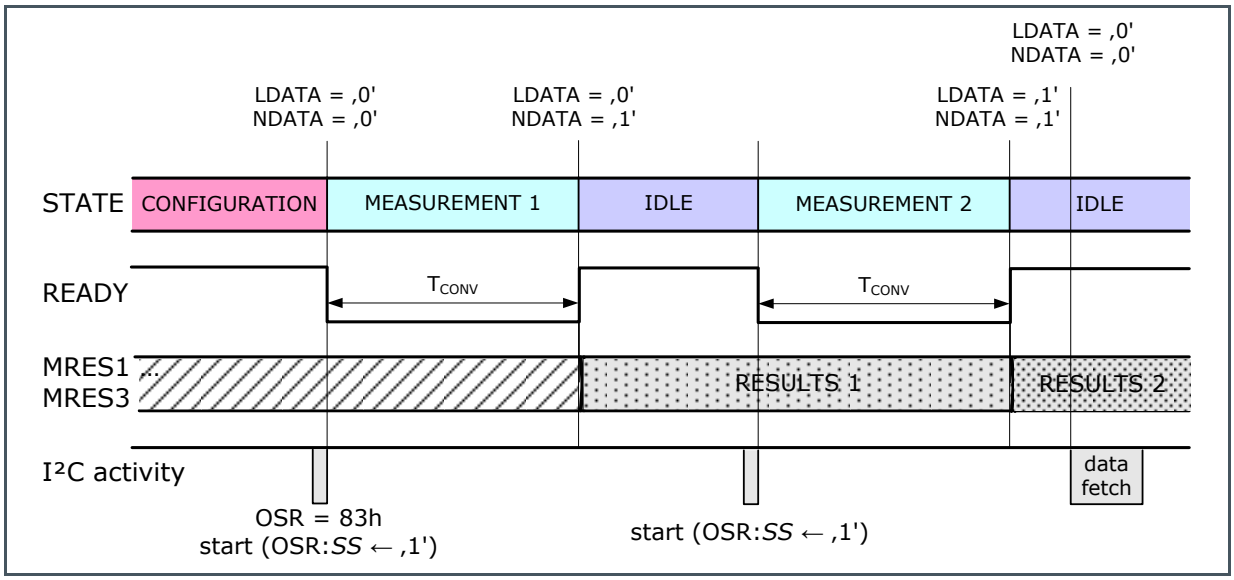
The status bit NDATA, is reset to “0” after reading the status register or at least one measurement result register.

Figure 56:
Update Time of the Status Register Bits for an Accurate Measurement and Read Behavior



If the buffer registers contain new values (NDATA = “1”) and new measurement finishes before an I²C reading process occurs, the new measurement results are stored in the buffer registers. The older measurement results are overwritten. The status bit LDATA, shown in Figure 57 indicates this. The LDATA bit is only reset to “0” by reading the status register, as it allows checking for the loss of information after multiple measurement cycles.

Figure 57:
Update Time of the Status Register Bits, if Some Measurement Results Were not Picked up



The status bits STATUS:STANDBYSTATE and STATUS:POWERSTATE, always show the actual status of the internal control signals for Standby and power down. In both cases, it can differ from the actual set bits CREG3:SB and OSR:PD, due to the behavior of the control signals while a measurement is in process. The reading of the 16-bit values of the output result registers always starts with the least significant byte.

The measurement value TEMP at address 1h is a 12-bit value, but its higher 4 bits until 16 are filled with 0h. For Measurement modes programmed with CREG1:TIME < 2^{12}, there is a TEMP result with a lower resolution. If the SYND mode is used and the OUTCONV register is set inactive by CREG2:EN_TM = “0”, any temperature measurement is not possible. In case CREG2:EN_TM is enabled (“1”), the TEMP value is only valid for conversion times with ≥ 2^{12} internal system clocks, f_{CLK}, represented by the OUTCONV register.

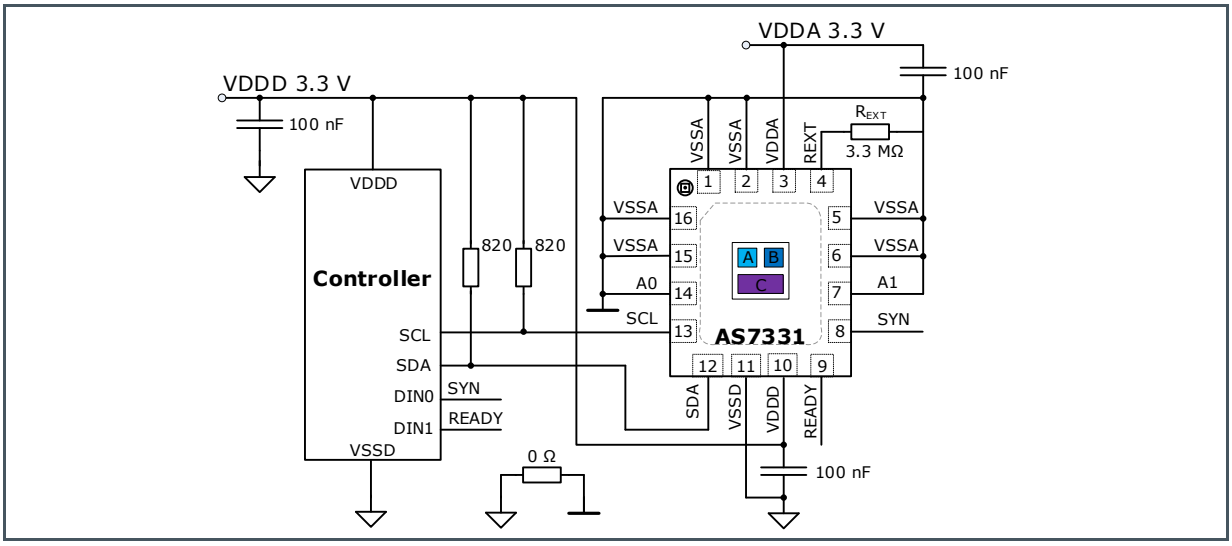
Power-on reset, software-reset or return to the Configuration state resets the complete output register bank.

9 Application Information

9.1 Schematic

Figure 58 shows a typical application circuit. Digital and analog grounds should be routed separately onto the printed circuit board and must be connected near the device.

Figure 58:
Typical Application Circuit



Please make sure all the specified components within the application circuit work according to their operating range and the parameters in the datasheet. For example, voltage regulators (workspace load current, separated analog and digital, or decoupled power supplies based on a common regulator) need special treatment to avoid noise or deviations during operation.

9.2 External Components

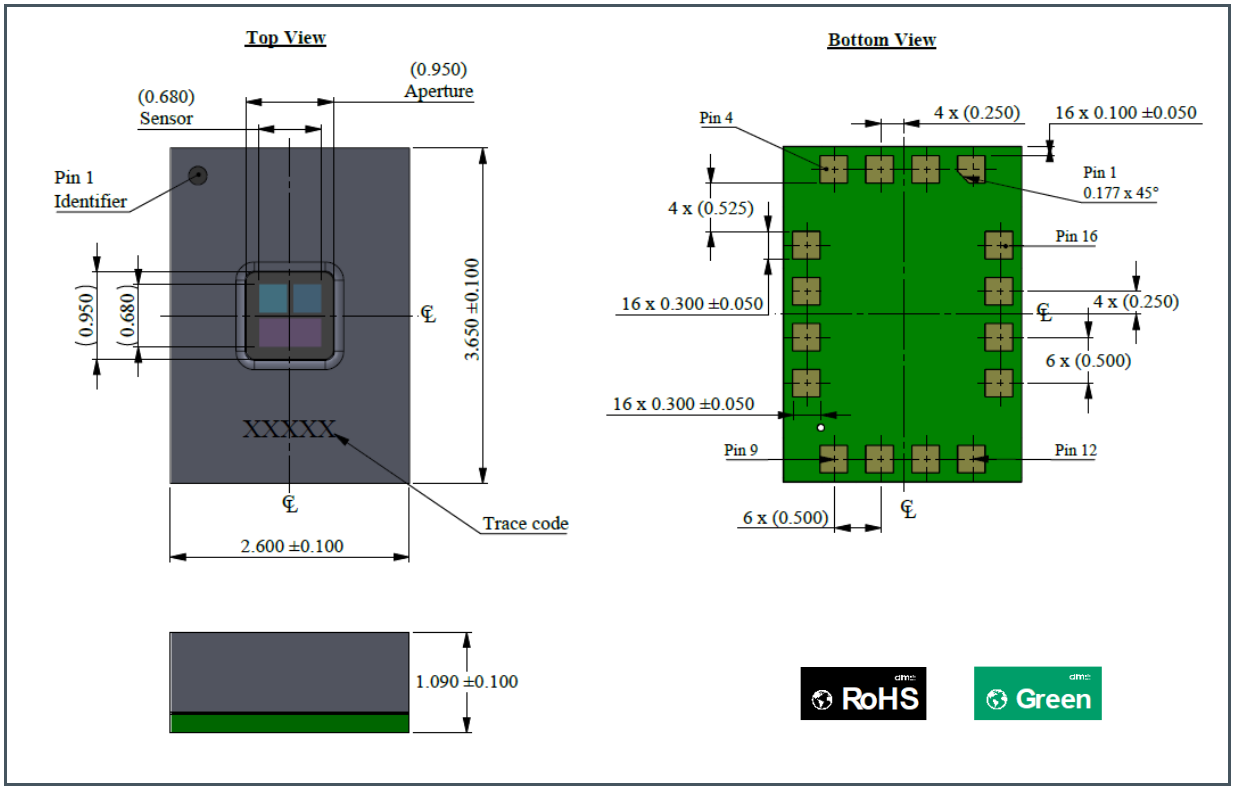
The AS7331 and its external components for references and/or power supply (e.g. reference resistor, R_{EXT}) should be placed on the same PCB side.

9.3 PCB Layout

The analog supply must be placed as close as possible to the AS7331. The connection between the analog and digital grounds must be beneath (LP level) and/or near the AS7331.

10 Package Drawings and Markings

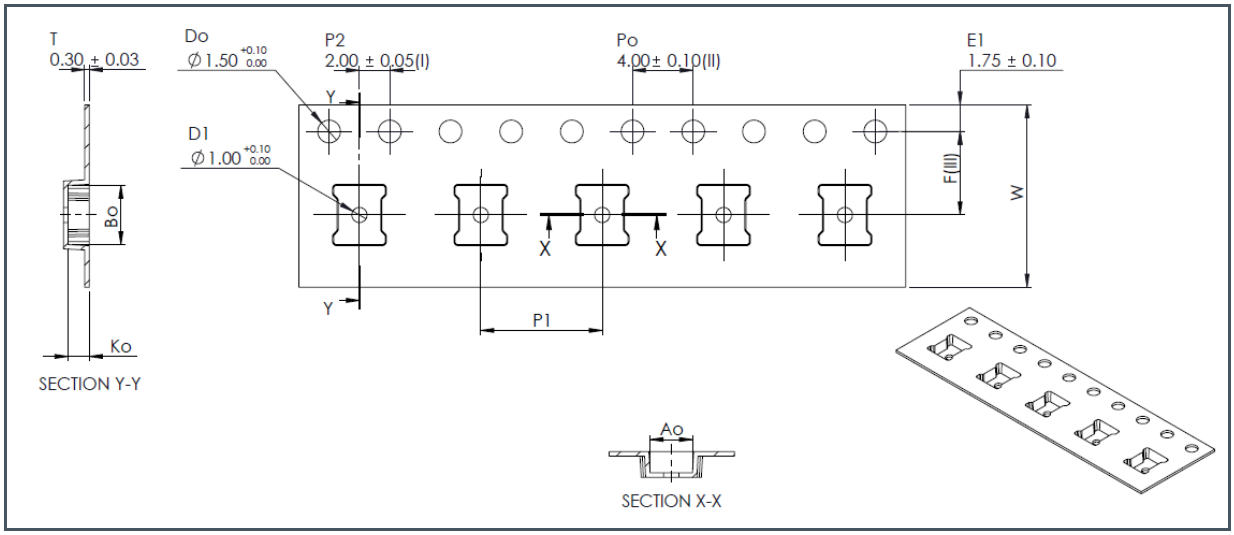
Figure 59:
AS7331 OLGA16 Package Outline Drawing



(1) All dimensions are in millimeters and angles are in degrees.
(2) Dimensions and tolerances conform to ASME Y14.5M-1994.
(3) N is the total number of terminals.
(4) This package contains no lead (Pb).
(5) This drawing is subject to change without notice.

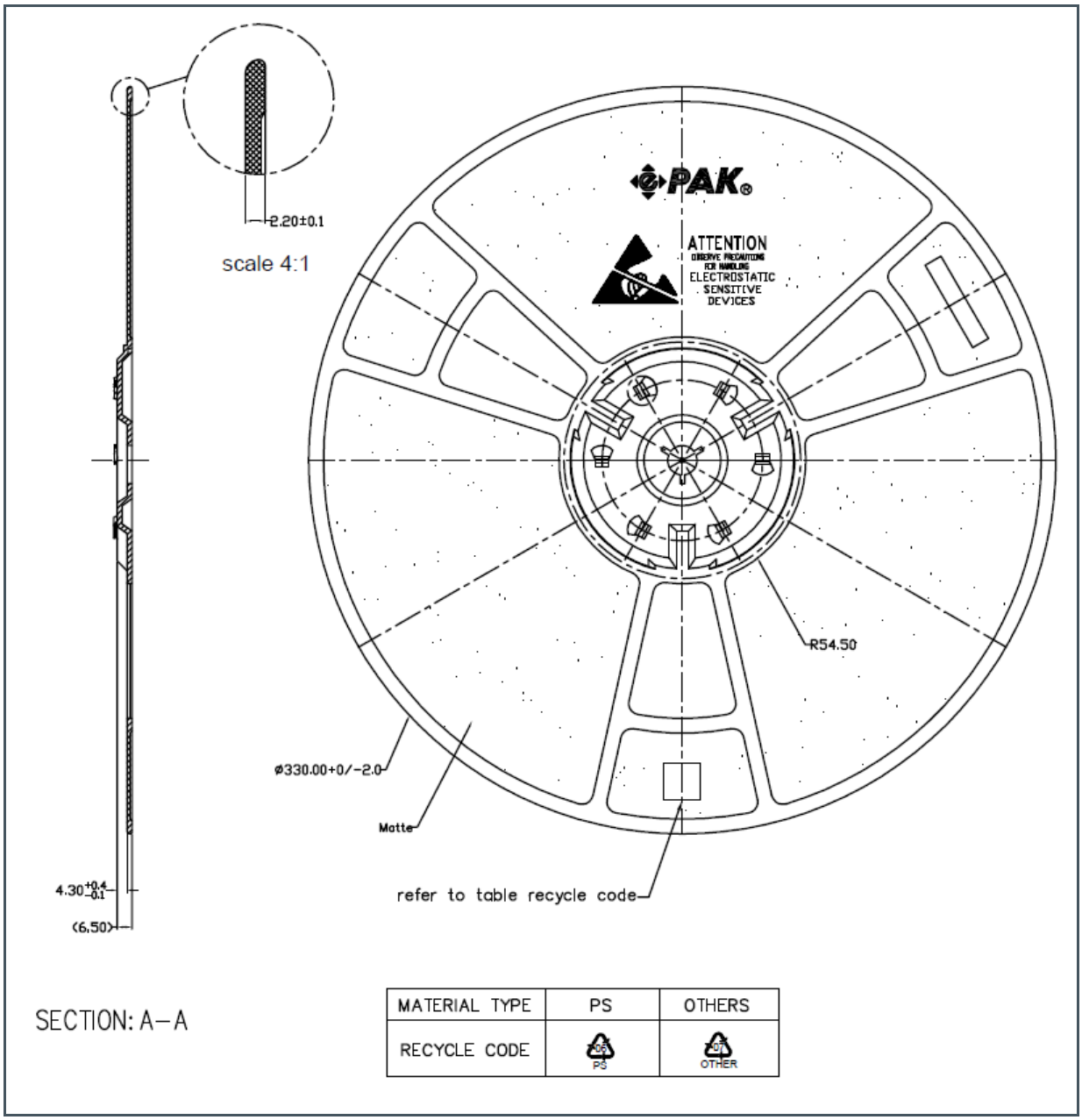
11 Tape & Reel Information

Figure 60:
AS7331 Tape Dimensions



(1) All dimensions are in millimeters. Angles in degrees.
(2) This drawing is subject to change without notice.

Figure 61:
AS7331 Reel Dimensions



(1) All dimensions are in millimeters. Angles in degrees.
(2) This drawing is subject to change without notice.

12 Soldering & Storage Information

12.1 Soldering Information

Figure 62:
Solder Reflow Profile Graph

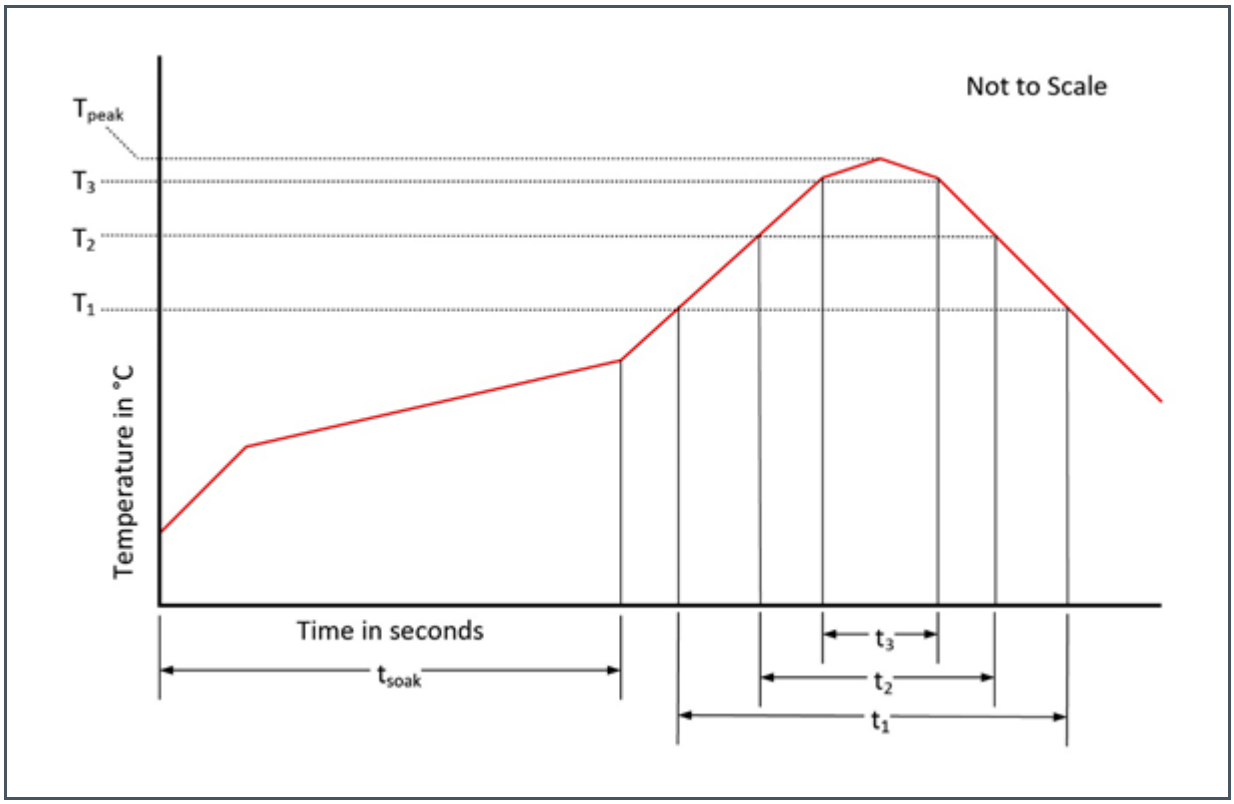


Figure 63:
Solder Reflow Profile

Parameter	Reference	Device
Average temperature gradient in preheating		2.5 °C/s
Soak time	t_{soak}	2 to 3 minutes
Time above 217 °C (T1)	t_1	Max 60 s
Time above 230 °C (T2)	t_2	Max 50 s
Time above T_{peak} – 10 °C (T3)	t_3	Max 10 s
Peak temperature in reflow	T_{peak}	260 °C

Parameter	Reference	Device
Temperature gradient in cooling		Max −5 °C/s

Information

For cleaning the sensor after soldering, we recommend a pH neutral cleaner such as Isopropanol (IPA) with a pH of 7. Do not use any solvents with a pH smaller or larger than 7.

12.2 Storage Information

12.2.1 Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package.

To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping. Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 24 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 24 months
- Ambient Temperature: <40 °C
- Relative Humidity: <90 %

Rebaking of the devices will be required if the devices exceed the 24 months shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

Floor Life

The module has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

- Floor Life: 168 hours
- Ambient Temperature: <30 °C
- Relative Humidity: <60 %

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50 °C for 12 hours.

13 Revision Information

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams-OSRAM AG standard warranty as given in the General Terms of Trade
Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams-OSRAM AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

Changes from previous version to current revision v4-00	Page
Updated Figure 6, I_{VDD} typical value updated	10
Added Chapter 12.2: Storage Information	68

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

14 Legal Information

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