DIO2115E

2-Vrms Audio Driver with Adjustable Gain

Features

- Voltage Output at 32Ω Load
  20mW 1% THD+N with 3.3V supply voltage
- No Pop/Clicks Noise when Power ON/OFF
- No Need for Output DC-Blocking Capacitors
- Optimized Frequency Response between 20Hz–20kHz
- Accepting Differential Input
- Featuring external under voltage mute
- HBM ESD protection: Output pin 8kV
- Available in DQFN-16 package

Applications

- Set-Top Boxes
- High Definition DVD Players
- Car Entertainment System
- Medical

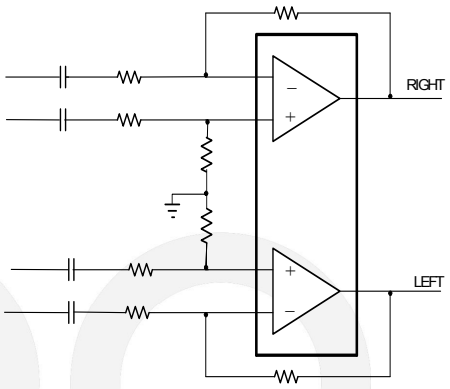
Descriptions

The DIO2115E is an integrated solution for Set-top box and high definition player, and designed to optimize the audio driver circuit performance while reducing the BOM cost by eliminating the peripheral discrete components for noise reduction. DIO2115E features a 2Vrms stereo audio driver that designed to allow for the removal of output AC-coupling capacitors.

Featuring differential input mode, gain range of ±1V/V to ±10V/V can be achieved via external gain resistor setting.

Meanwhile, the DIO2115E offers built-in shut-down control circuitry for optimal pop-free performance. Under under-voltage condition, DIO2115E is able to detect it and mutes the output.

Block Diagram



Ordering Information

Order Part Number	Top Marking		T_A	Package	
DIO2115ELN16	21E	Green/RoHS	-40 to +85°C	DQFN-16	Tape & Reel, 3000

Pin Assignment

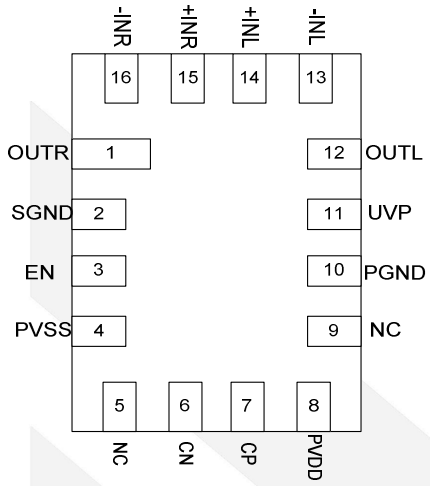


Figure 1 Top View

Pin Descriptions

PIN		I/O	Description
Name	NO.		
OUTR	1	O	Right-channel output
SGND	2	P	Signal ground
EN	3	I	Enable input, active-high
PVSS	4	P	Supply voltage
NC	5,9	I/O	No Connected
CN	6	I/O	Charge-pump flying capacitor negative terminal
CP	7	I/O	Charge-pump flying capacitor positive terminal
PVDD	8	P	Positive supply
PGND	10	P	Power ground
UVP	11	I	Under voltage protection input
OUTL	12	O	Left-channel output
-INL	13	I	Left-channel negative input
+INL	14	I	Left-channel positive input
+INR	15	I	Right-channel positive input
-INR	16	I	Right-channel negative input

Note: For simplicity, all V_{DD} below stands for PVDD.

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maxim rating conditions for extended periods may affect device reliability.

Parameter		Rating	Unit
Supply Voltage		-0.3 to 7.5	V
Input Voltage		GND-0.3 to V_{DD}+0.3	V
Minimum load impedance		32	Ω
EN to GND		-0.3 to V_{DD}+0.3	V
Storage Temperature Range		-65 to 150	°C
Junction Temperature		-65 to 150	°C
HBM ESD, JESD22-A114	Output Pins	8	kV

Recommend Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended Operating conditions are specified to ensure optimal performance to the datasheet specifications. DIOO does not Recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	3	5	5.5	V
V_{IH}	EN High level Input Voltage(V_{DD}=3.3V)	1.1			V
V_{IL}	EN Low level Input Voltage(V_{DD}=3.3V)			0.3	V
T_A	Operating Temperature Range	-40		85	°C

Electrical Characteristics

Typical value: T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{OS}	Output Offset Voltage	V_{DD}=3-5V, Input grounded, unity gain	-3	0	3	mV
OVP	V_{DD} Over Voltage Protection	V_{DD}>5.5V, then IC shut down		5.7		V
PSRR	Power supply rejection ratio			90		dB
V_{OH}	High level output voltage	V_{DD}=3.3V,R_L=2.5kΩ	3.2			V
V_{OL}	Low level output voltage	V_{DD}=3.3V,R_L=2.5kΩ			-3.10	V
I_{IH}	EN High level input current	V_{DD}=3.3V,V_I=V_{DD}			1	μA
I_{IL}	EN Low level input current	V_{DD}=3.3V,V_I=0V			1	μA
I_{DD}	Supply current	V_{DD}=3.3V, V_I= V_{DD}, No load		11		
		Shut down mode, V_{DD}=3-5V			1	mA

Operating Characteristics

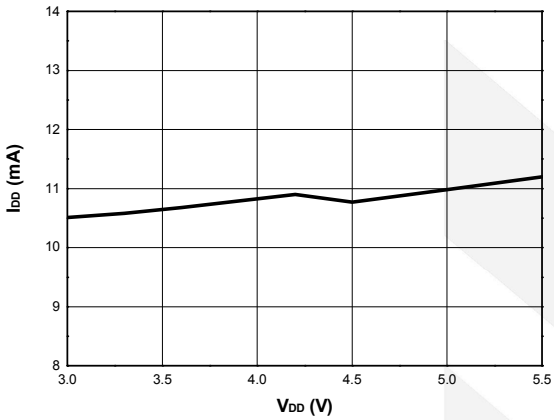
Typical value: V_{DD}=3.3V, R_L=2.5kΩ, C_{PUMP}=1μF,C_{PVSS}=1μF, C_{IN}=10μF, R_{IN}=10kΩ, R_{fb}=20kΩ,T_A=25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_O	Output Voltage	THD+N<1%, V_{DD}=3.3V, f=1kHz	2.05			V_{RMS}
Po	Output Power	THD+N<1%,V_{DD}=3.3V,R_L=32Ω, C_{PVSS}=22μF, T_A=25°C	20			mW
THD+N	Total harmonic distortion + noise	V_O=2V_{RMS}, f=1kHz, R_L=600Ω		0.001		%
X_{TALK}	Channel crosstalk	V_O=2V_{RMS}, f=1kHz		95		dB
I_O	Maximum output current	V_{DD}=3.3V		60		mA
SNR	Signal noise ratio	V_O=2V_{RMS}, BW=22kHz, A-weighted		112		dB
SR	Slew rate			12		V/μs
V_N	Noise output voltage	BW=20Hz to 22kHz,V_{DD}=3.3V		4.5		μV_{RMS}
G_{BW}	Unity gain bandwidth			7		MHz
A_{VO}	Open loop voltage gain			140		dB
V_{UVP}	External under-voltage detection		1.08	1.11	1.14	V
I_{Hys}	External under-voltage detection hysteresis current			5		μA
f_{CP}	Charge pump frequency			310		kHz
Attenuation @mute	Input-to-output attenuation in shutdown	EN=0V		90		dB

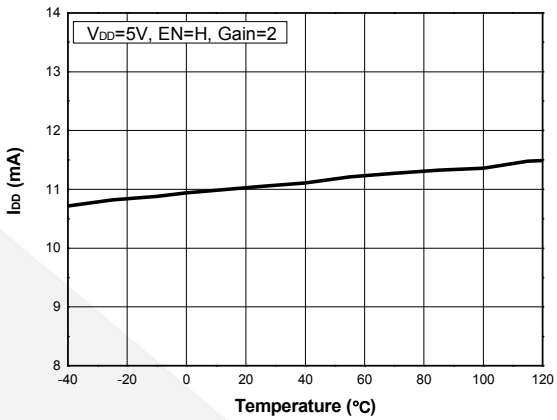
Typical Performance Characteristics

At T_A = +25°C, C_{PUMP}=1μF,C_{PVSS}=1μF,unless otherwise noted.

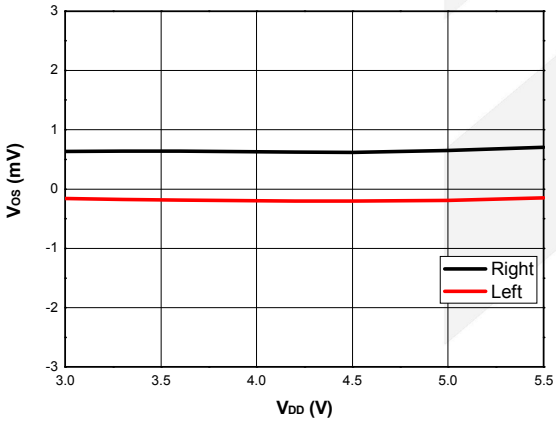
I_{DD} vs. V_{DD}



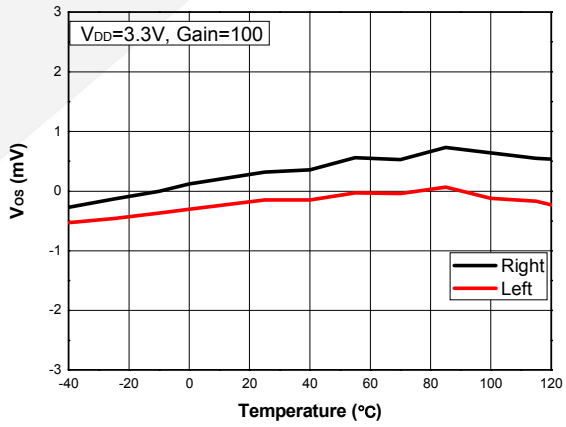
I_{DD} vs. Temperature



V_{OS} vs. VDD

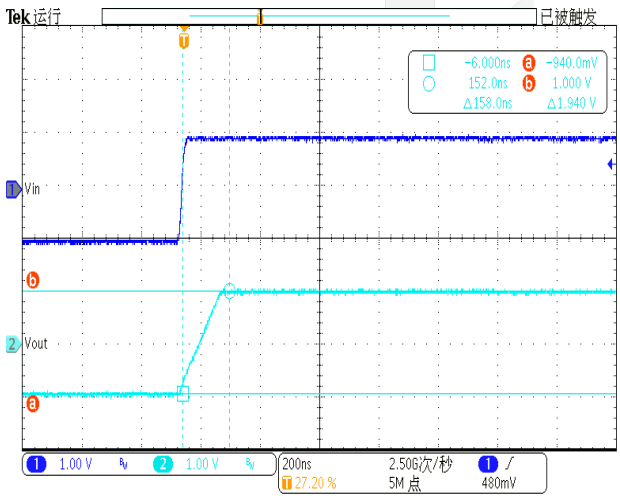


V_{OS} vs. Temperature



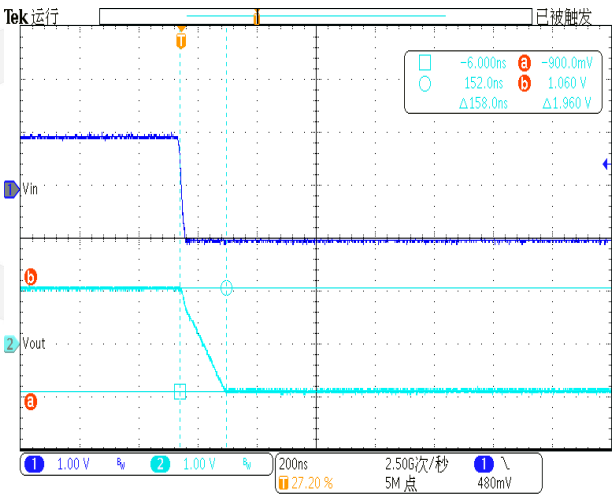
Slew Rate

V_{DD}=3.3V, G=1 (buffer), V_{IN}=0~1V@1kHz Rise

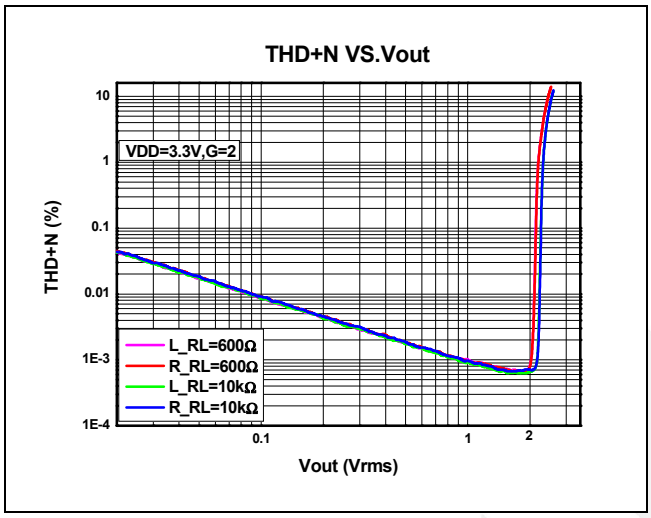


Slew Rate

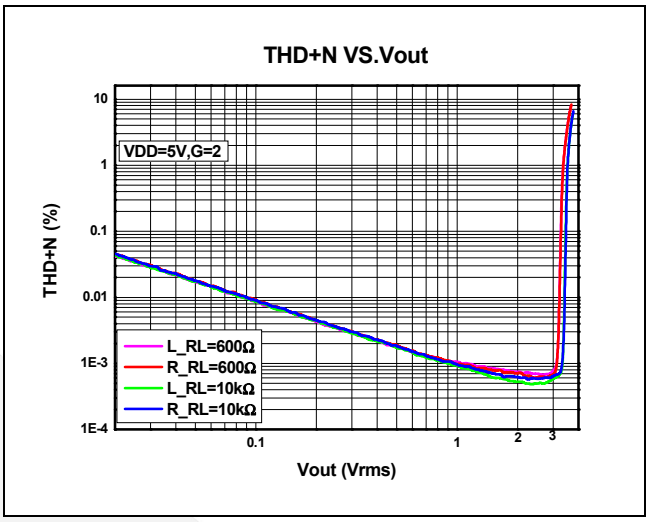
V_{DD}=3.3V, G=1 (buffer), V_{IN}=0~1V@1kHz Fall



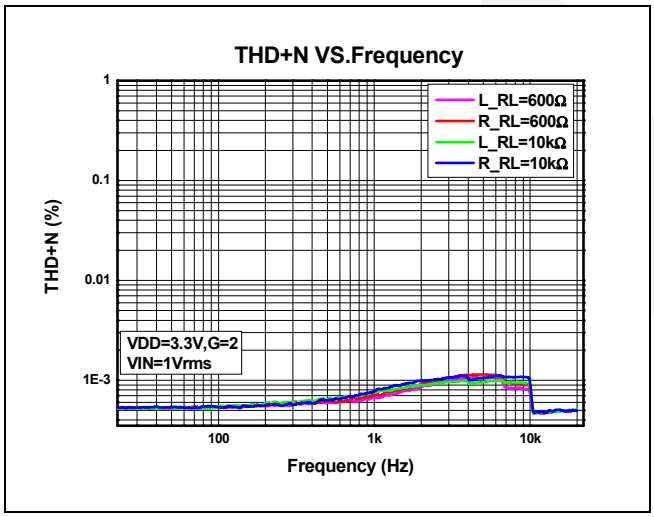
THD+N vs. V_{OUT}



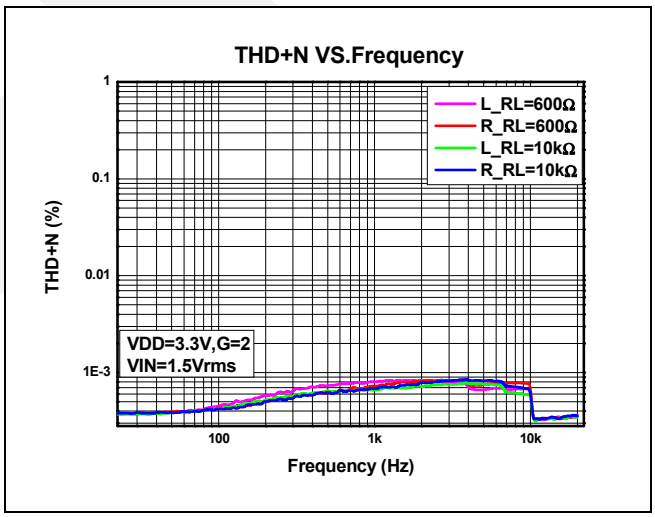
THD+N vs. V_{OUT}



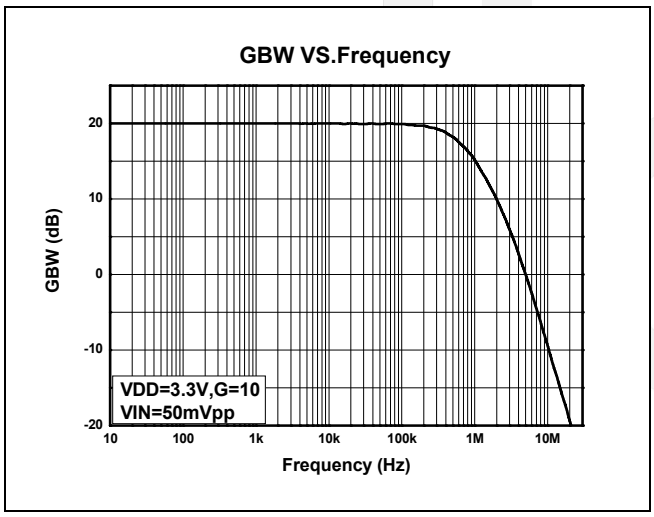
THD+N vs. Frequency



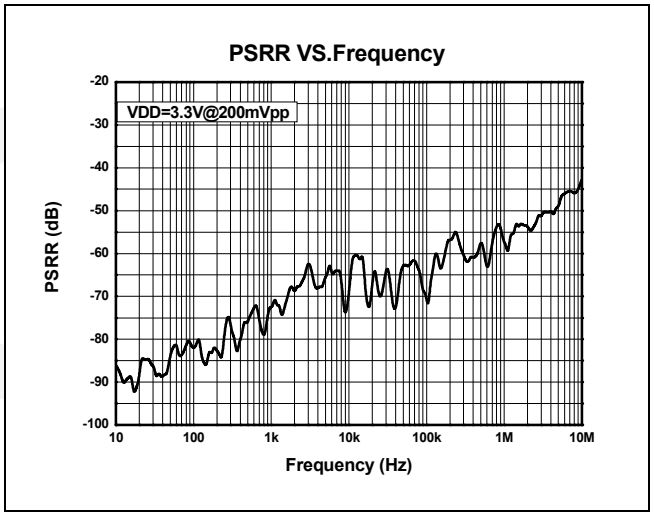
THD+N vs. Frequency



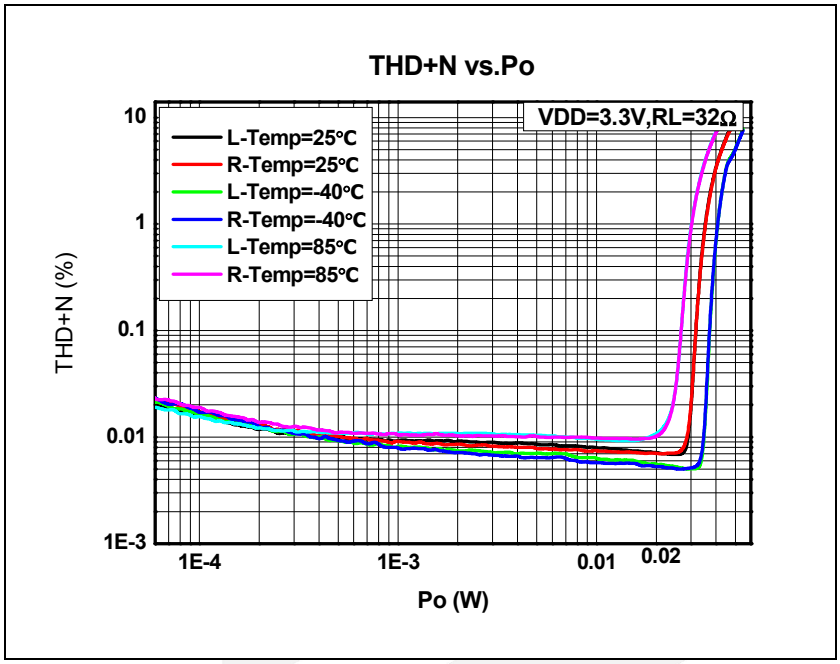
GBW vs. Frequency



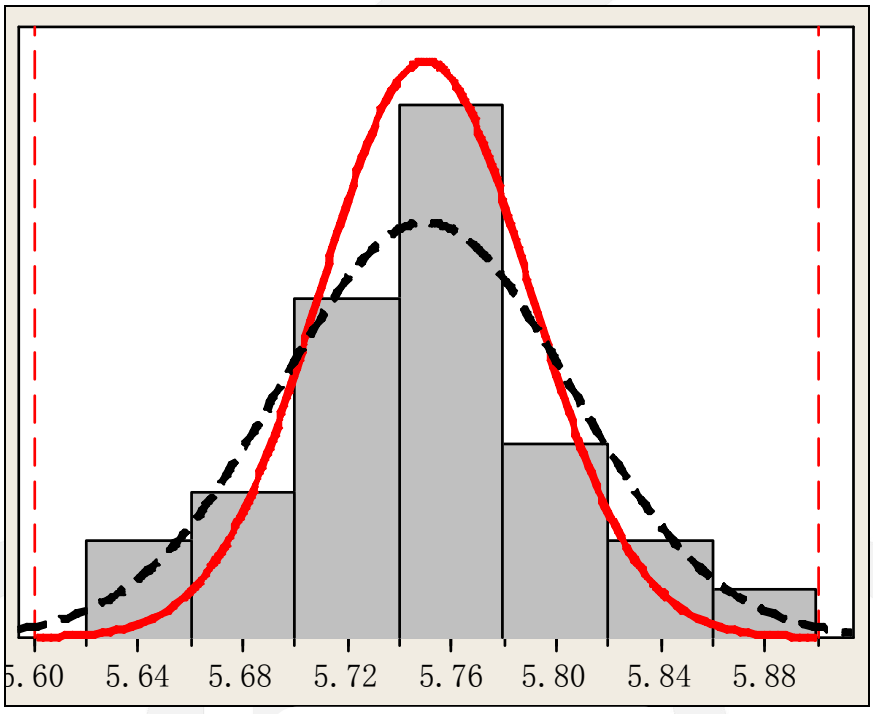
PSRR vs. Frequency



THD+N Ratio vs. Output Power

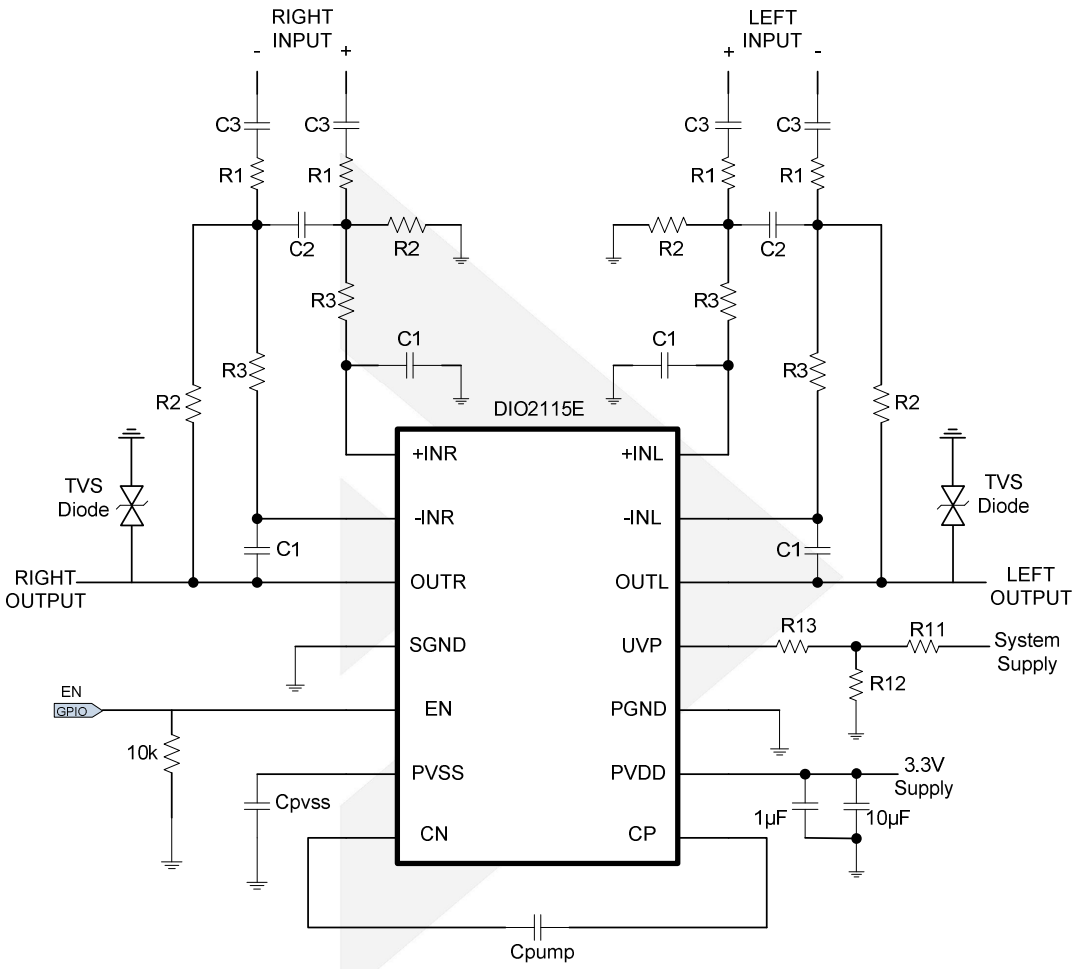


OVP



Over Voltage Protection (V)

Application Circuit



Differential-input, single-ended output, second-order filter

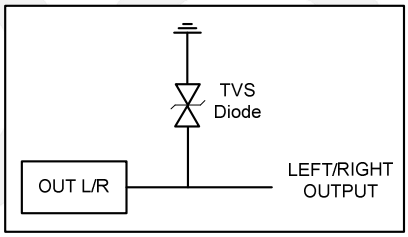
R1=15kΩ, R2=30kΩ, R3=47kΩ, C1=33pF, C2=150pF, C3=6.8μF, R11=5.6kΩ, R12=2.43kΩ, R13=15KΩ

Cpvss=0.33-1μF, Cpump=0.33-1μF

Notes:

1. In some applications, if the power supply noise needs to be filtered, the ferrite bead is recommended in a value of 600ohm@100MHz, instead of RC network. RC network normally will lower the power supply resulting in the degraded the audio performance. If the resistor is not chosen properly, which can trigger the internal UVP detection circuit and shut down the output. As depicted below.

2. In order to protect the device against the power surge, transient voltage suppressor (TVS) devices are recommended at the output pins OUTL/OUTR.



Application Notes

Gain-Setting Resistors Ranges and Input-Blocking Capacitors

The gain-setting resistors, R_{IN} and R_{FB}, must be chosen so that noise, stability, and input capacitor size of the DIO2115E are kept within acceptable limits. Voltage gain is defined as R_{FB} divided by R_{IN}.

Table 1 lists the recommended resistor value for different gain settings. Selecting values that are too low demands a large input ac-coupling capacitor $C_{IN.}$ Selecting values that are too high increases the noise of the amplifier.

The gain-setting resistor must be placed close to the input pins to minimize capacitive loading on these input pins and to ensure maximum stability.

Table 1 Input Capacitor with 2Hz cutoff and Resistor Values Recommended

Input Res., R_{IN}	Feedback Res., R_{fb}	Inverting Gain
22 kΩ	22 kΩ	-1 V/V
15 kΩ	30 kΩ	-2 V/V
10 kΩ	100 kΩ	-10 V/V

$$f_{CIN} = \frac{1}{2\pi R_{IN} C_{IN}} \quad \text{or}$$

$$C_{IN} = \frac{1}{2\pi R_{IN} f_{CIN}}$$

Equation 1 Cutoff decision Cutoff

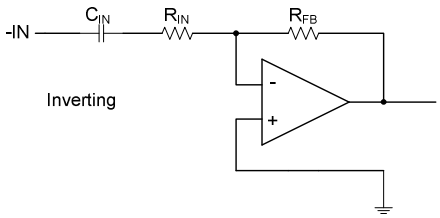


Figure 2 Inverting Gain Configurations

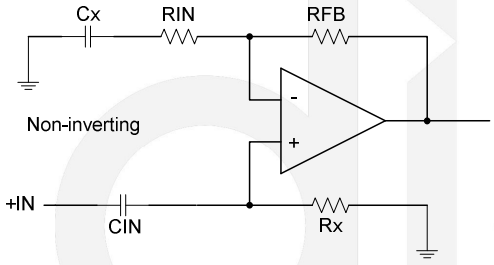


Figure 3 Non-Inverting Gain Configuration

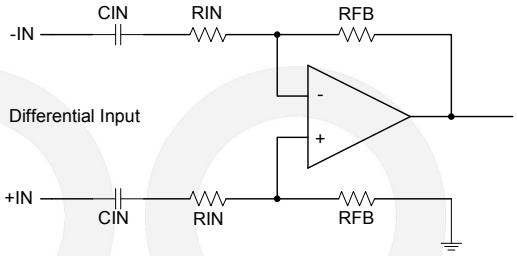


Figure 4 Differential Gain Configuration

INPUT-BLOCKING CAPACITORS

DC input-blocking capacitors are required to be added in series with the audio signal into the input pins of DIO2115E. These capacitors block the dc portion of the audio source and allow DIO2115E inputs to be properly biased to provide maximum performance.

These capacitors form a high-pass filter with the input resistor, R_{IN}. The cutoff frequency is calculated using the equation below. For this calculation, the capacitance used is the input-blocking capacitor, and the resistance is the input resistor chosen from Table 1; then the frequency and/or capacitance can be determined when one of the two values is given.

2nd Order Filter Typical Application

Several audio DACs used today require an external low-pass filter to remove out-of-band noise. This is possible with the DIO2115E, as it can be used like a standard OPAMP. Several filter topologies can be implemented, both single-ended and differential. In Figure 3, a multi-feedback (MFB) with differential input and single-ended input is shown.

An ac-coupling capacitor to remove dc content from the source is shown; it serves to block any dc content from the source and lowers the dc-gain to 1, helping reducing the output dc-offset to minimum.

The resistor values should have a low value for obtaining low noise, but should also have a high enough value to get a small size ac-coupling capacitor.

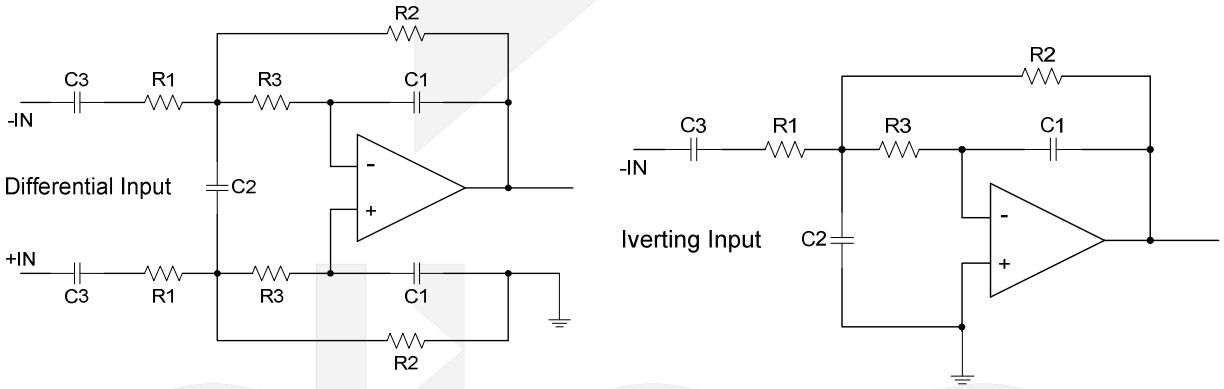


Figure 5 Second-Order Active Low-Pass Filter

Charge Pump Flying Capacitor and PVSS Capacitor

The charge pump flying capacitor serves to transfer charge during the generation of the negative supply voltage. The PVSS capacitor must be at least equal to the charge pump capacitor in order to allow maximum charge transfer. Low ESR X5R or X7R capacitors are recommended selection, a value of typical 0.33μF is recommended for C_{PUMP}, and a value of typical 1μF is recommended for PVSS. Capacitor values can be smaller than the value recommended, but the maximum output voltage may be reduced and the device may not operate to specifications. Increasing PVSS capacitor can improve ability of driving output power, the minimum of output power is 20mW when PVSS capacitor value is 22μF.

Decoupling Capacitors

The DIO2115E requires adequate power supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. A good low equivalent-series-resistance (ESR) X5R or X7R ceramic capacitor, typically a combine of paralleled 0.1μF and 10μF, placed as close as possible to the device V_{DD} lead works best. Placing this decoupling capacitor close to the DIO2115E is important for the performance of the amplifier. For filtering lower-frequency noise signals, a 10μF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

Pop-Free Power-Up

Pop-free power up is ensured by keeping the EN (shut down pin) low during power-supply ramp up and ramp down. The EN pin should be kept low until the input ac-coupling capacitors are fully charged before asserting the EN pin high to achieve pop-less power up. Figure 6 illustrates the preferred sequence.

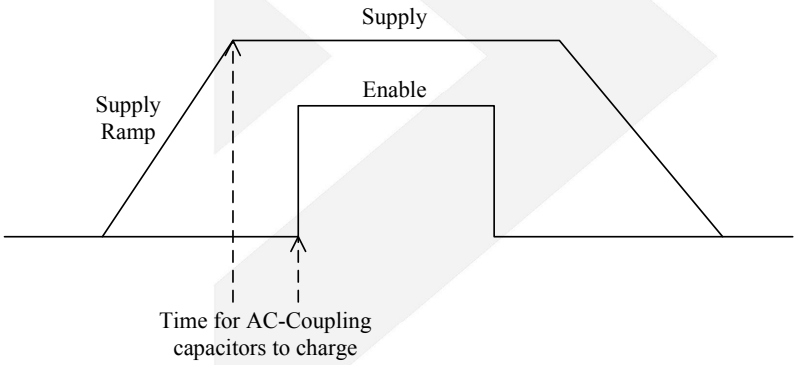


Figure 6 Power-Up Sequences

External Under-voltage Detection

External under-voltage detection can be used to shut down the DIO2115E before an input device can generate a pop noise. Although the shut down voltage is 1.11V, customers need to consider the accuracy of system passive components such as resistors and associated temperature variation. Users often select a resistor divider to obtain the power-on and shut down threshold for the specific application. The typical thresholds can be calculated as follows, respectively for VSUP_MO at 5V and 12V. Usually for best power down noise performance, 12V supply is recommended for UVP circuitry as below. Typically this 12V is the power supply which generates the 5V supply for DIO2115E PVDD pins.

Case 1: VSUP_MO= 12V (**Recommended**)

V_{UVP}=(1.11V-6μA*R13)*(R11+R12)/R12;

$V_{hysteresis}$=5μA*R13*(R11+R12)/R12;

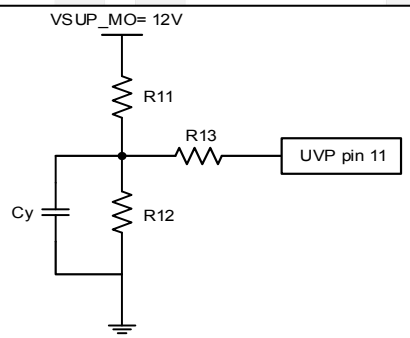
With the condition R13>>R11//R12.

For example, if R11=11k, R12=1.4k and R13=47k,

Then V_{UVP}=7.334V; $V_{hysteresis}$=2.081V

Here, V_{UVP} is the shut down threshold.

In this case, the voltage at UVP pin 11 is greater than 1.311V under worst case of VSUP_MO ripples.



Case 2: VSUP_MO= 5.0V

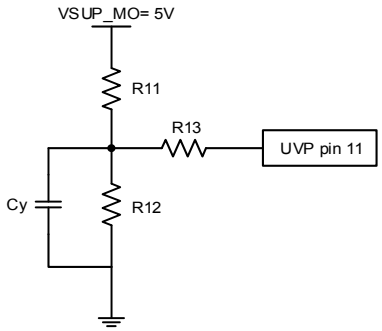
V_{UVP}=(1.11V-6μA*R13)*(R11+R12)/R12;

$V_{hysteresis}$=5μA*R13*(R11+R12)/R12;

With the condition R13>>R11//R12.

For example, if R11=5.6k, R12=2.2k and R13=47k,

Then V_{UVP}=2.936V; $V_{hysteresis}$=0.833V



Here, V_{UVP} is the shut down threshold. In this case, the voltage at UVP pin 11 is greater than 1.368V under worst case of VSUP_MO ripples.

Capacitive Load

The DIO2115E has the ability to drive a high capacitive load up to 220pF directly. Higher capacitive loads can be accepted by adding a series resistor of 47Ω or larger.

PCB Layout Design Recommendation

It is very important that PCB layout can effect system audio performance. The below route rule will be recommended.

1. The PVDD capacitor and the charge pump flying capacitor should be placed as close as possible to the pin.
2. The PVSS capacitor should be placed as possible to the pin, if capacitor value greater than or equal 22μF, 0805 package will be recommended to choose.
3. Left and Right channels of chip should be use independent ground loop itself (as: LGND/RGND), finally by using 0 ohm resistor respectively connected to chip SGND.
4. The output pins OUTL/OUTR should be parallel Bi-direction TVS devices against ESD.

Figure 7 shows a sample layout.

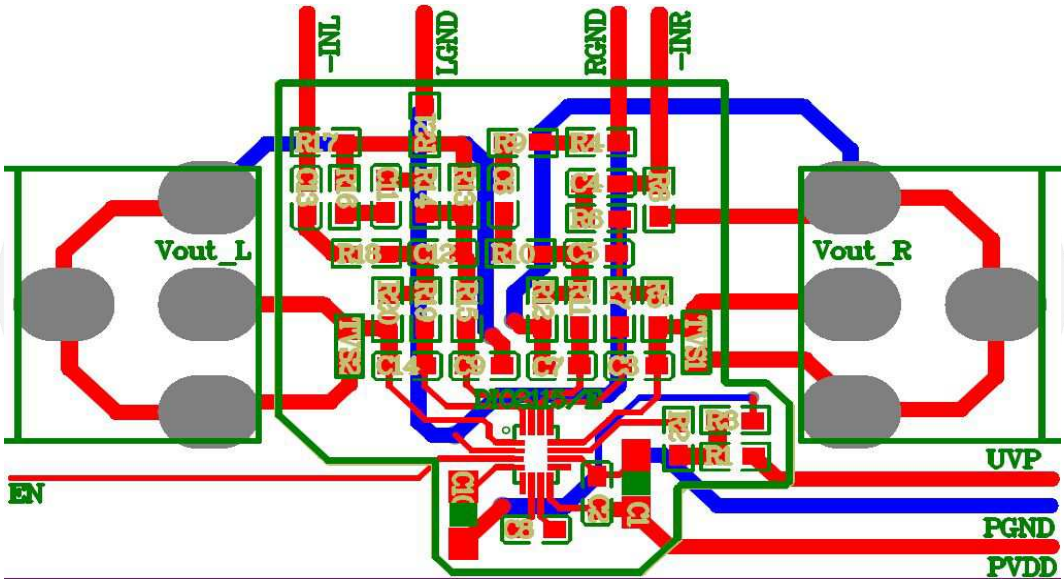
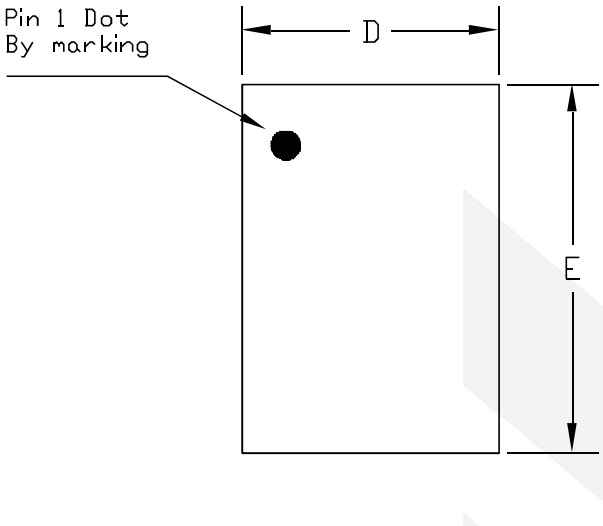
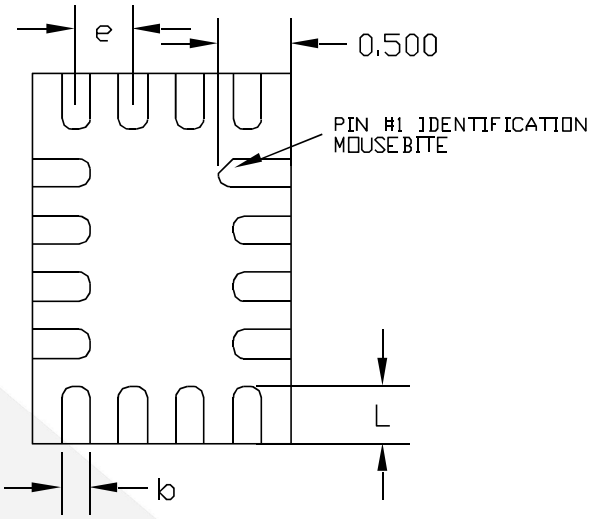


Figure 7 PCB Layout recommended

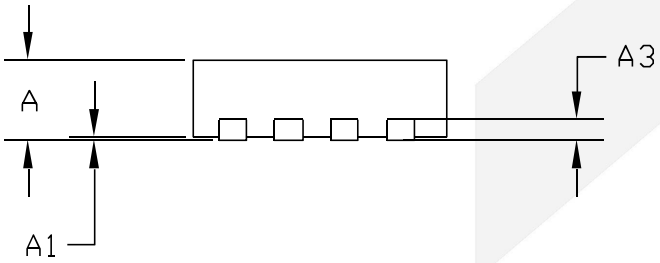
Physical Dimensions: DQFN-16



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions In Millimeters		
	Min	Nom	Max
A	>0.50	0.55	0.60
A1	0.00	-	0.05
A3	0.15 REF		
D	1.75	1.80	1.85
E	2.55	2.60	2.65
L	0.35	0.40	0.45
b	0.15	0.20	0.25
e	0.40 BSC		

CONTACT US

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