DIO5110
Dual Bootstrapped, 12V MOSFET Driver with Output Disable

Features

- Wide voltage range from 5.5V to 13.2V
- All-In-One Synchronous Buck Driver
- Bootstrapped High-Side Drive
- Maximum 4.0A Peak Source Current Capability
- Maximum 3.5A Peak Sink Current Capability
- One PWM Signal Generates Both Drives
- Anti-cross Conduction Protection Circuitry
- Under voltage lockout function
- Over temperature shutdown function
- These are Pb-Free Devices

Applications

- Multiphase Desktop CPU Supplies
- Single-Supply Synchronous Buck Converters

Descriptions

The DIO5110 is a single Phase 12V MOSFET gate drivers optimized to drive the gates of both high-side and low-side power MOSFETs in a synchronous buck converter. The high-side and low-side driver is capable of driving a 3000pF load with a 25ns propagation delay and a 30ns transition time.

With a wide operating voltage range, high or low side MOSFET gate drive voltage can be optimized for the best efficiency. Internal adaptive non-overlap circuitry further reduces switching losses by preventing simultaneous conduction of both MOSFETs.

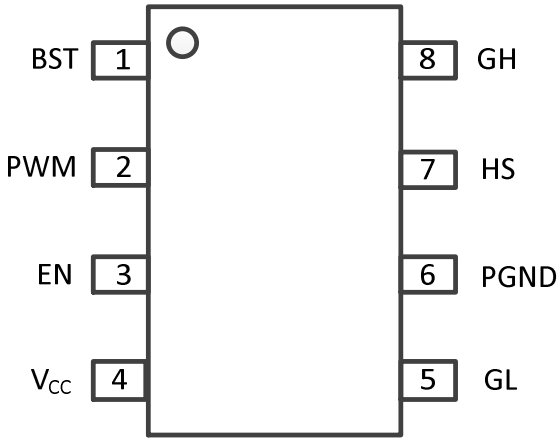
The floating top driver design can accommodate V_{BST} voltages as high as 35V, with transient voltages as high as 40V. Both gate outputs can be driven low by applying a low logic level to the Output Disable (EN) pin. An Under voltage Lockout function ensures that both driver outputs are low when the supply voltage is low, and a Thermal Shutdown function provides the IC with over temperature protection.

Ordering Information

Order Part Number	Top Marking		T_A	Package	
DIO5110CS8	DIO5110	Green	-40 to 85°C	SOIC-8	Tape & Reel, 2500
DIO5110DN8	D5110	Green	-40 to 85°C	DNF3*3-8	Tape & Reel, 5000
DIO5110ED8	510	Green	-40 to 85°C	DFN2*2.2-8	Tape & Reel, 3000

Pin Assignment

SOIC-8



DFN3*3-8/DFN2*2.2-8

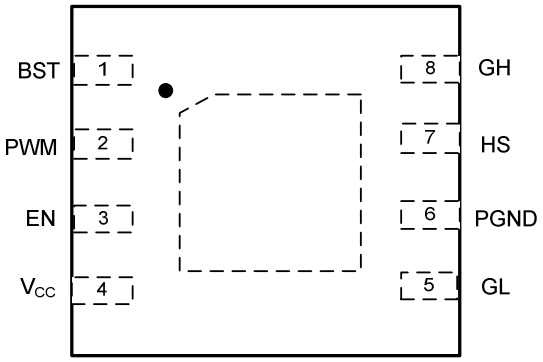


Figure 1 Top View

Pin Descriptions

Name	Description
BST	Upper MOSFET Floating Bootstrap Supply. A capacitor connected between BST and HS pins holds this bootstrap voltage for the high-side MOSFET as it is switched. The recommended capacitor value is between 100nF and 1.0μF. An external diode is required with the DIO5110.
PWM	Logic-Level Input. This pin has primary control of the drive outputs.
EN	Output Disable. When low, normal operation is disabled forcing GH and GL low.
V_{CC}	Input Supply. A 1.0μF ceramic capacitor should be connected from this pin to GND.
GL	Output drive for the lower MOSFET.
PGND	Power Ground. Should be closely connected to the source of the lower MOSFET.
HS	Switch Node. Connected to the source of the upper MOSFET.
GH	Output drive for the upper MOSFET.

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maxim rating conditions for extended periods may affect device reliability.

Pin Symbol	Pin Name	Min	Max	Unit
V_{CC}	Main Supply Voltage Input	-0.3	15	V
PGND	Ground	0	0	V
BST	Bootstrap Supply Voltage Input	-0.3	58	V
			60(<40ns)	V
HS	Switching Node (Bootstrap Supply Return)	-5	58	V
		-10	60(<40ns)	V
GH	High-Side Driver Output	-0.3	BST+0.3	V
		-2		V
GL	Low-Side Driver Output	-0.3	V_{CC}+0.3	V
		-5		V
PWM	GH and GL Control Input	-0.3	6.5	V
EN	Output Disable	-0.3	6.5	V
Operating Ambient Temperature Range		0 to 85		℃
Junction Temperature Range		0 to 150		℃
Storage Temperature Range		-65 to 150		℃

Recommend Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended Operating conditions are specified to ensure optimal performance to the datasheet specifications. DIOO does not Recommend exceeding them or designing to Absolute Maximum Ratings.

Parameter	Rating	Unit
Supply Voltage	5.5 to 13.2	V
Operating Temperature Range	0 to 85	°C

Electrical Characteristics

Typical value: Vcc=12V, T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply						
V_{CC}	Supply Voltage Range		5.5		13.2	V
I_{SYS}	Supply Current	BST=12V, PWM=0V		1.5	3.0	mA
EN Input						
V_{EN_HI}	Input Voltage High		2.0			V
V_{EN_LO}	Input Voltage Low				0.8	V
V_{EN_HYS}	EN Input Hysteresis			0.3		V
I_{EN}	Input current	No internal pull up or pull down resistors	-1.0		1.0	μA
PWM Input						
V_{PWM_HI}	Input Voltage High		2.0			V
V_{PWM_LO}	Input Voltage Low				0.8	V
V_{PWM_HYS}	PWM Input Hysteresis			0.3		V
I_{PWM}	Input current	No internal pull up or pull down resistors	-1.0		1.0	μA
High-Side Driver						
$R_{DS(ON)\_HH}$	Output Resistance, Sourcing Current	BST-HS=12V		1.0	1.8	Ω
$R_{DS(ON)\_HL}$	Output Resistance, Sinking Current	BST-HS=12V		1.0	1.8	Ω
R_{OUT_H}	Output Resistance, Unbiased	BST-HS=0V		15		kΩ
t_{rGH}	Transition Times	BST-HS=12V, C_{LOAD}=3.0nF		15	55	ns
t_{fGH}				11	45	
t_{pdhGH}	Propagation Delay Times	BST-HS=12V, C_{LOAD}=3.0nF	32	45	70	ns
t_{pdlGH}		BST-HS=12V, C_{LOAD}=3.0nF		25	40	
t_{pdlEN}				20	40	
t_{pdhEN}				25	55	
R_{SW}	SW Pull down Resistance	HS to PGND		15		kΩ
Low-Side Driver						
$R_{DS(ON)\_LH}$	Output Resistance, Sourcing Current			1.0	1.8	Ω
$R_{DS(ON)\_LL}$	Output Resistance, Sinking Current			1.0	1.8	Ω
R_{OUT_L}	Output Resistance, Unbiased	V_{CC}=PGND		15		kΩ
t_{rGL}	Transition Times	C_{LOAD}=3.0nF		15	50	ns

t_{fGL}				11	30	
t_{pdhGL}	Propagation Delay Times	C_{LOAD}=3.0nF		20	40	ns
t_{pdlGL}				20	40	
t_{pdlEN}				20	40	
t_{pdhEN}				20	40	
T_{Timer}	Timeout Delay	GH-HS=0		95		ns
Under voltage Lockout						
V_{UVLO+}	UVLO Startup		4.5	5.0	5.5	V
V_{UVLO-}	UVLO Shutdown		4.2	4.7	5.2	V
V_{UVLO_HYS}	Hysteresis		0.1	0.3	0.5	V

Specifications subject to change without notice.

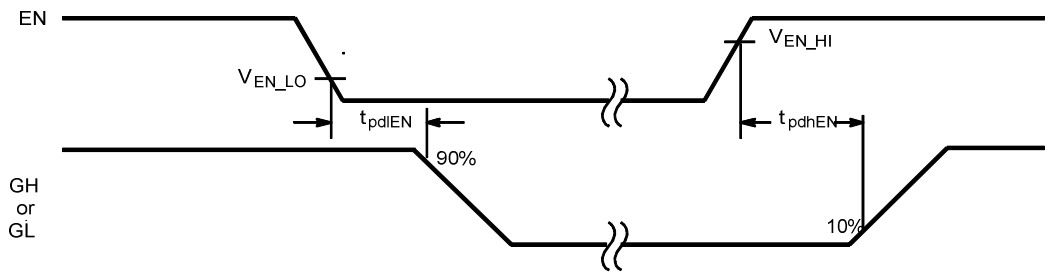


Figure 2. Output Disable Timing Diagram

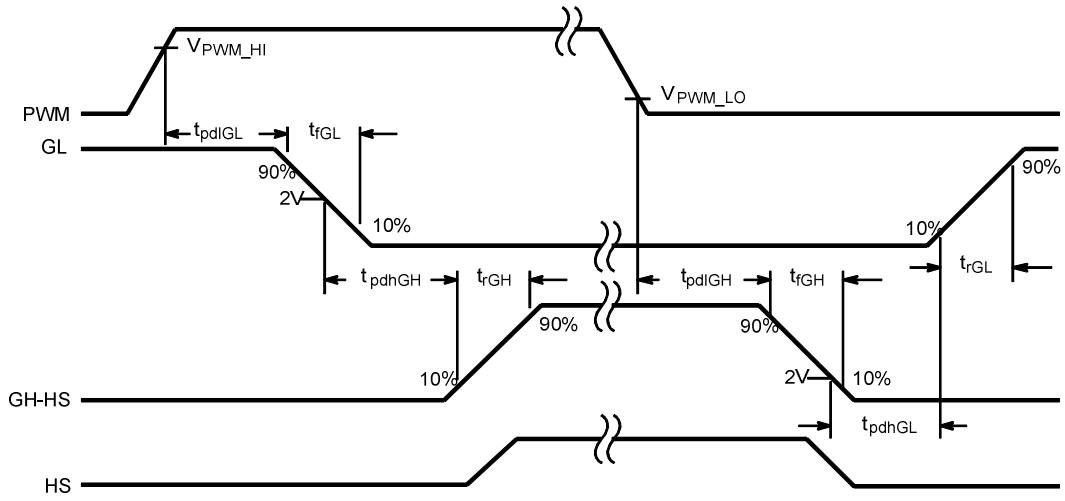
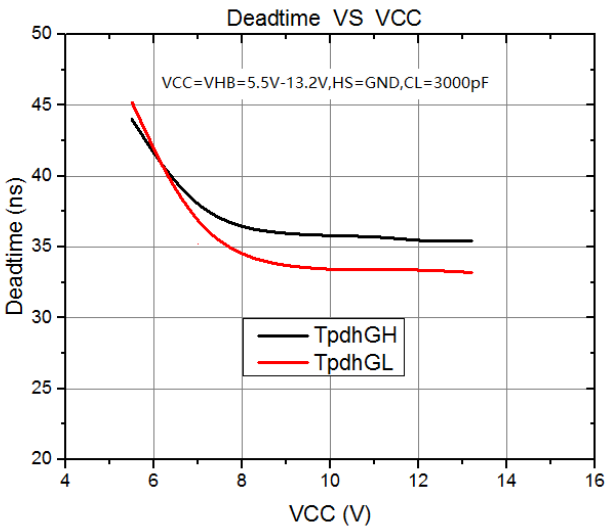


Figure 3. Non-overlap Timing Diagram

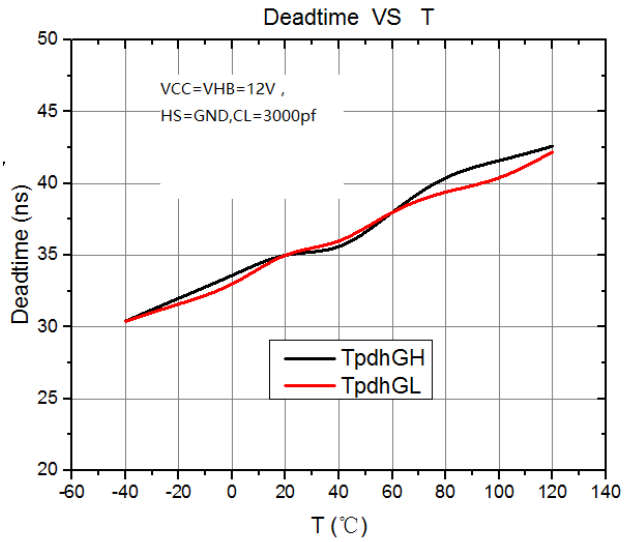
Typical Performance Characteristics

T_A = 25°C, unless otherwise specified.

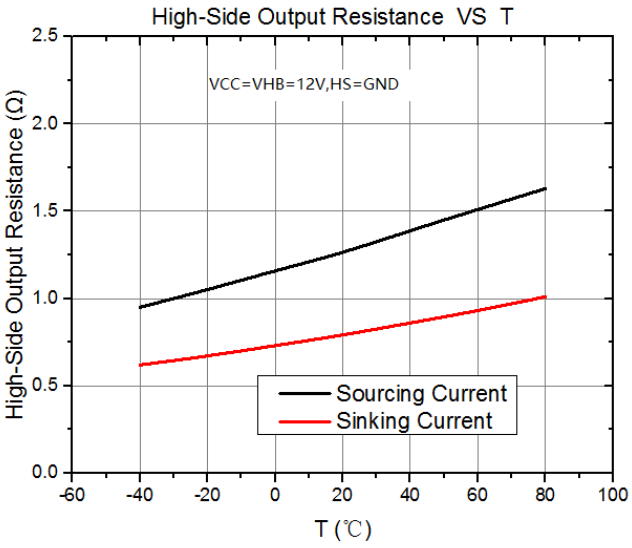
Dead time vs. V_{CC}



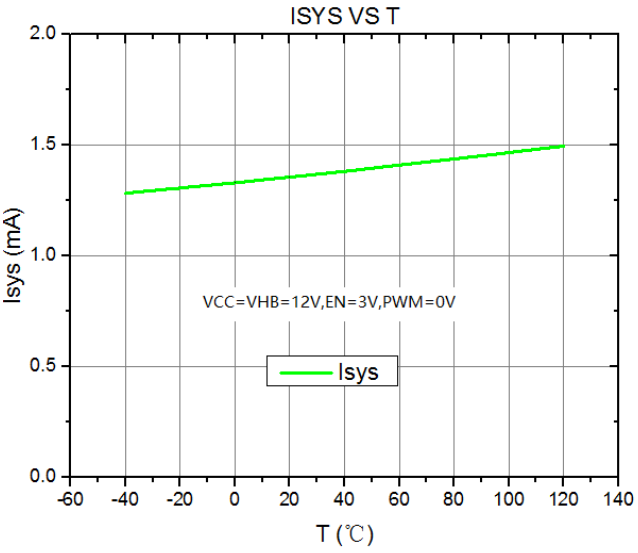
Dead time vs. Temperature



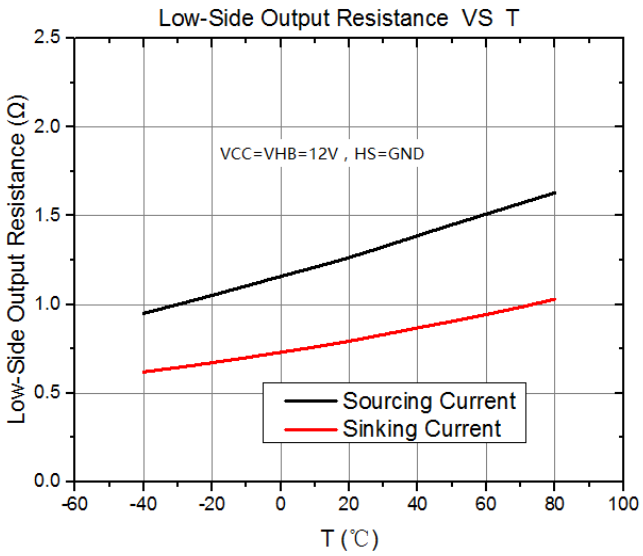
High-Side Output Resistance vs. Temperature



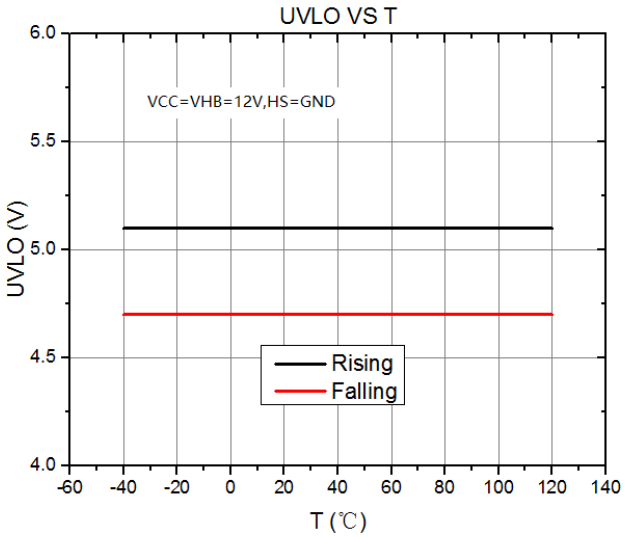
I_{SYS} vs. Temperature



Low-Side Output Resistance vs. Temperature



UVLO vs. Temperature



Application Circuit

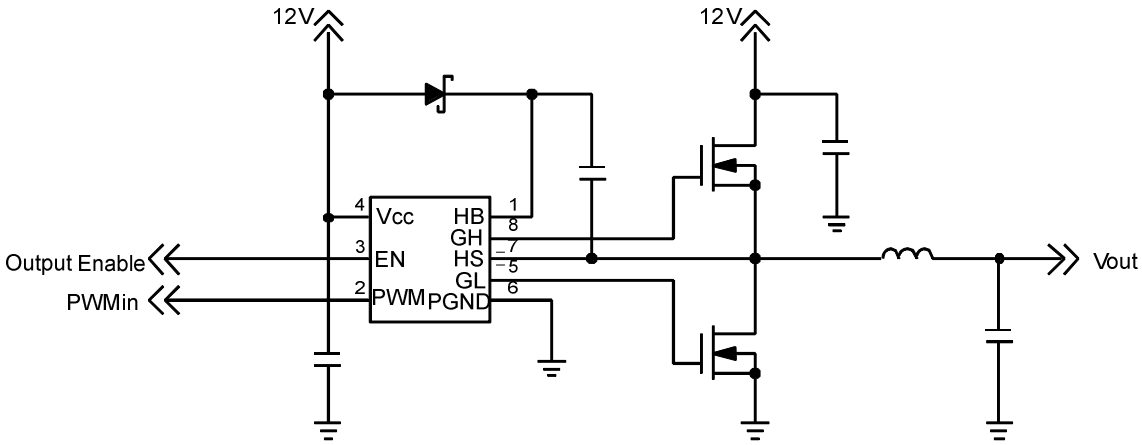


Figure 4. Example Circuit

Functional Block Diagraph

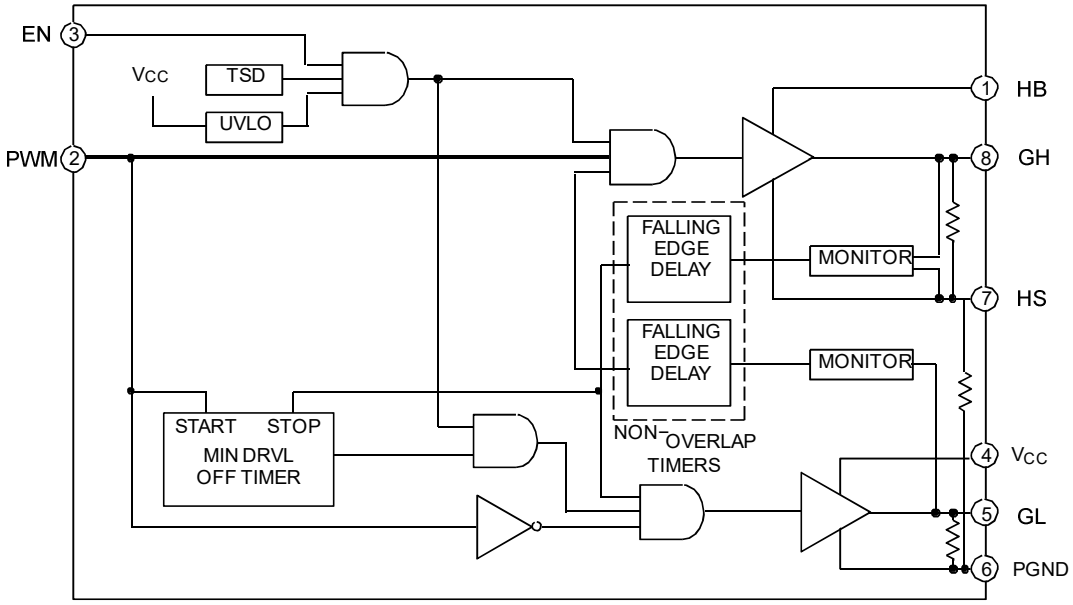


Figure 5. Functional Block Diagraph

Application Information

Theory of Operation

The DIO5110 are single phase MOSFET drivers designed for driving two N−channel MOSFETs in a synchronous buck converter topology. The DIO5110 will operate from 5.5 V to 13.2 V, but have been optimized for high current multi−phase buck regulators that convert 12V rail directly to the core voltage required by complex logic chips. A single PWM input signal is all that is required to properly drive the high−side and the low−side MOSFETs. Each driver is capable of driving a 3nF load at frequencies up to 1 MHz.

Low-Side Driver

The low−side driver is designed to drive a ground−referenced low RDS(on) N−Channel MOSFET. The voltage rail for the low−side driver is internally connected to the VCC supply and PGND.

High-Side Driver

The high−side driver is designed to drive a floating low RDS(on) N−channel MOSFET. The gate voltage for the high side driver is developed by a bootstrap circuit referenced to Switch Node (HS) pin.

The bootstrap circuit is comprised of an external diode, and an external bootstrap capacitor. When the DIO5110 are starting up, the HS pin is at ground, so the bootstrap capacitor will charge up to V_{CC} through the bootstrap diode See Figure 4. When the PWM input goes high, the high−side driver will begin to turn on the high−side MOSFET using the stored charge of the bootstrap capacitor. As the high−side MOSFET turns on, the HS pin will rise. When the high−side MOSFET is fully on, the switch node will be at 12 V, and the BST pin will be at 12 V plus the charge of the bootstrap capacitor (approaching 24 V).

The bootstrap capacitor is recharged when the switch node goes low during the next cycle.

Safety Timer and Overlap Protection Circuit

It is very important that MOSFETs in a synchronous buck regulator do not both conduct at the same time. Excessive shoot−through or cross conduction can damage the MOSFETs, and even a small amount of cross conduction will cause a decrease in the power conversion efficiency.

The DIO5110 prevent cross conduction by monitoring the status of the external MOSFETs and applying the appropriate amount of “dead−time” or the time between the turn off of one MOSFET and the turn on of the other MOSFET.

When the PWM input pin goes high, GL will go low after a propagation delay ($tpdl_{GL}$). The time it takes for the low−side MOSFET to turn off (tf_{GL}) is dependent on the total charge on the low−side MOSFET gate. The DIO5110 monitor the gate voltage of both MOSFETs and the switch node voltage to determine the conduction status of the MOSFETs. Once the low−side MOSFET is turned off an internal timer will delay ($tpdh_{GH}$) the turn on of the high−side MOSFET.

Likewise, when the PWM input pin goes low, GH will go low after the propagation delay (tpd_{GH}). The time to turn off the high−side MOSFET (tf_{GH}) is dependent on the total gate charge of the high−side MOSFET. A timer will be triggered once the high−side MOSFET has stopped conducting, to delay ($tpdh_{GL}$) the turn on of the low−side MOSFET.

Power Supply Decoupling

The DIO5110 can source and sink relatively large currents to the gate pins of the external MOSFETs. In order to maintain a constant and stable supply voltage (V_{CC}) a low ESR capacitor should be placed near the power and ground pins. A 1μF to 4.7μF multi layer ceramic capacitor (MLCC) is usually sufficient.

Input Pins

The PWM input and the Output Disable pins of the DIO5110 have internal protection for Electro Static Discharge (ESD), but in normal operation they present a relatively high input impedance. If the PWM controller does not have internal pulldown resistors, they should be added externally to ensure that the driver outputs do not go high before the controller has reached its under voltage lockout threshold.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_{BST}) and the internal (or an external) diode. Selection of these components can be done after the high−side MOSFET has been chosen. The bootstrap capacitor must have a voltage rating that is able to withstand twice the maximum supply voltage. A minimum 50 V rating is recommended. The capacitance is determined using the following equation:

$$C_{BST} = \frac{Q_{GATE}}{\Delta V_{BST}}$$

where QGATE is the total gate charge of the high−side MOSFET, and _V_{BST} is the voltage droop allowed on the high−side MOSFET drive.

The bootstrap diode must be rated to withstand the maximum supply voltage plus any peak ringing voltages that may be present on HS. The average forward current can be estimated by:

$$I_{F(AVG)} = Q_{GATE} \times f_{MAX}$$

Where f_{MAX} is the maximum switching frequency of the controller. The peak surge current rating should be checked in−circuit, since this is dependent on the source impedance of the 12 V supply and the ESR of C_{BST}.

CONTACT US

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