



DIO2674

Four-Channel, 6th-Order SD and 1080p HD Video Filter

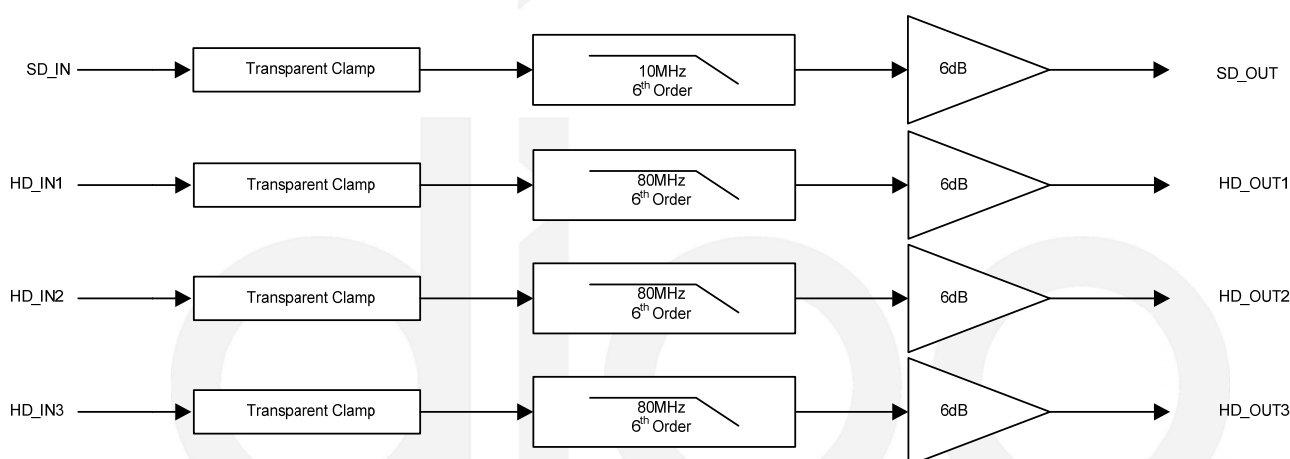
Features

- One SD channel with 6th-order, 10MHz filter
- Three HD channels with 6th-order, 80MHz filter
- Transparent Input Clamping
- Fixed 6dB Gain
- AC or DC Coupled Inputs
- AC or DC Coupled Outputs
- Operates from 3.135V to 5.25V
- Single Power Supply
- RoHS or Green TSSOP-14 Package
- 6500V ESD protection

Applications

- DVD Players
- Video Amplifiers
- Cable set-top boxes
- Personal Video Recorders
- Communications Devices
- Video on Demand

Block Diagram



Ordering Information

Order Part Number	Top Marking		T _A	Package	
DIO2674CT14	DIO2674	Green	-40 to +85°C	TSSOP-14	Tape & Reel, 2500

Descriptions

DIO2674 is a low voltage, four channels video amplifier with integrated 6dB reconstruction filter and input clamps. In fact, DIO2674 integrates a single SD video driver plus a triple HD video driver. DIO2674 can improve image quality compared to the passive LC filters.

All channels can be directly driven by a DC-coupled or an AC-coupled signal. Internal diode-like clamps and bias circuitry may be used if AC-coupled inputs are required. The output in DIO2674 can also drive AC or DC coupled single (150Ω) or dual (75Ω) loads. The DC coupling capacitors can be removed.



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Pin Assignments

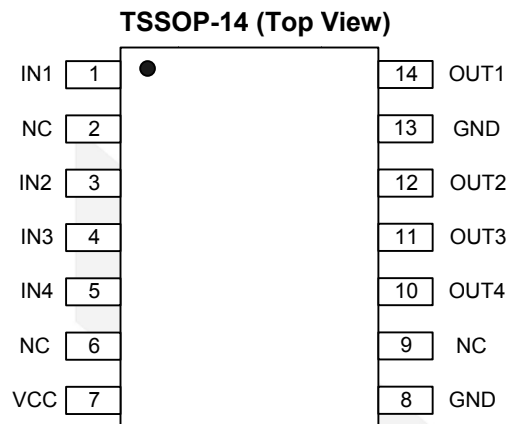


Figure 1 Pin Assignment (Top View)

Pin Description

Pin	Name	Type	Description
1	IN1	Input	Channel SD Video Input
2	NC		No Connection
3	IN2	Input	Channel HD Video Input (Pr)
4	IN3	Input	Channel HD Video Input (Pb)
5	IN4	Input	Channel HD Video Input (Y)
6	NC		No Connection
7	VCC	Power	Positive Power Supply
8	GND	Ground	Ground
9	NC		No Connection
10	OUT4	Output	Channel HD Video Output (Y)
11	OUT3	Output	Channel HD Video Output (Pb)
12	OUT2	Output	Channel HD Video Output (Pr)
13	GND	Ground	Ground
14	OUT1	Output	Channel SD Video Output



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Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Rating" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter		Rating	Unit
Supply Voltage		-0.3 to 6.0	V
Input Voltage		-0.3 to $V_{CC}+0.3$	V
Storage Temperature Range		-65 to 150	°C
Junction Temperature		150	°C
Lead Temperature Range		260	°C
TSSOP-14 Θ_{JA}		125	°C/W
ESD	HBM, JEDEC: JESD22-A114	6500	V
	CDM, JEDEC: JESD22-C101	2000	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation to ensure optimal performance to the datasheet specifications. DIOO does not recommend exceeding them or designing to Absolute Maximum Ratings.

Parameter		Rating	Unit
Supply Voltage		3.135 to 5.25	V
Operating Temperature Range		-40 to 85	°C



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Electrical Characteristics

Typical value: $T_A = 25^{\circ}\text{C}$, $V_{CC}=5\text{V}$, $R_{SOURCE}=37.5\Omega$, $R_L=150\Omega$ loads; referenced to 400kHz, all inputs are AC couple with $0.1\mu\text{F}$; all outputs are AC coupled with $220\mu\text{F}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC ELECTRICAL CHARACTERISTICS						
I_{CC}	Supply Current	HD Channels Selected + SD		78	90	mA
V_{IN}	Input Common Mode Voltage Range		GND		1.4	V
PSRR	Power Supply Rejection			-50	-60	dB
HIGH DEFINITION AC PERFORMANCE						
AV	Channel Gain		5.8	6.0	6.2	dB
BW	Band Width	-1dB, $R_{SOURCE}=75\Omega$		58		MHz
		-3dB, $R_{SOURCE}=75\Omega$		80		
AR	Attenuation	$f=148\text{MHz}$, $R_{SOURCE}=75\Omega$		-27		dB
THD	Output Distortion	$V_{OUT}=1.4\text{V}_{PP}$, $f=10\text{MHz}$		0.6	1.4	%
		$V_{OUT}=1.4\text{V}_{PP}$, $f=20\text{MHz}$		0.8	2.0	
X_{TALK}	Crosstalk	$f=1\text{MHz}$, $V_{IN}=1.4\text{V}_{PP}$		-75		dB
SNR	Signal to Noise Ratio	100kHz to 30MHz, 100% White Signal		65		dB
	Group Delay	100kHz to 30MHz		5		ns
	Propagation Delay	Input to Output		20		ns
SR	Slew Rate	2V Output 80% to 20%		100		V/ μs
STANDARD DEFINITION AC PERFORMANCE						
AV	Channel Gain		5.8	6.0	6.2	dB
BW	Bandwidth	-1dB		9		MHz
		-3dB		10		
AR	Attenuation	$f=27\text{MHz}$		-53		dB
DG	Differential Gain			0.6		%
DP	Differential Phase			1.2		°
THD	Output Distortion	$f=4\text{MHz}$			1.5	%
X_{TALK}	Crosstalk	$f=1\text{MHz}$		-75		dB
SNR	Signal to Noise Ratio			70		dB
t_{PD}	Propagation Delay			80		ns
	Group Delay	$f=400\text{kHz}$, 6.5MHz		10		ns
CLG_SD	Chroma Luma Gain	$f=3.58\text{MHz}$ ref to SD in at 400kHz	95	100	105	%
CLD_SD	Chroma Luma Delay	$f=3.58\text{MHz}$ ref to SD in at 400kHz		5.5		ns

Notes: $\text{SNR}=20 \cdot \log(714\text{mV} / \text{rms noise})$.

Specifications subject to change without notice.

Application Circuit

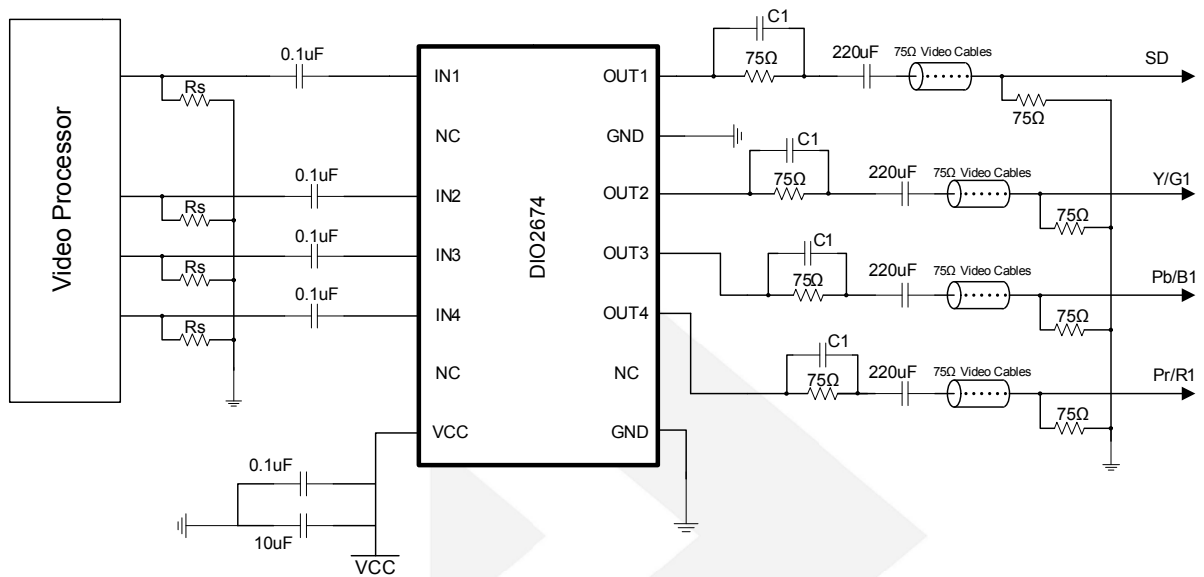


Figure 2 Input and Output AC-Coupling Application

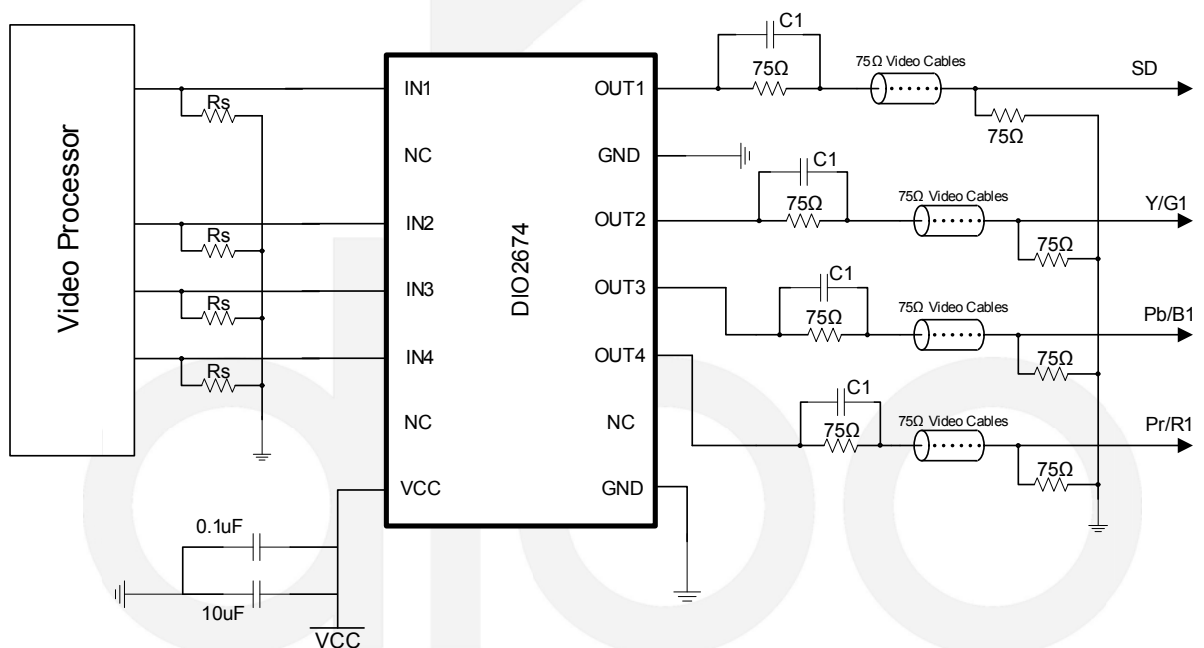


Figure 3 Input and Output DC-Coupling Application

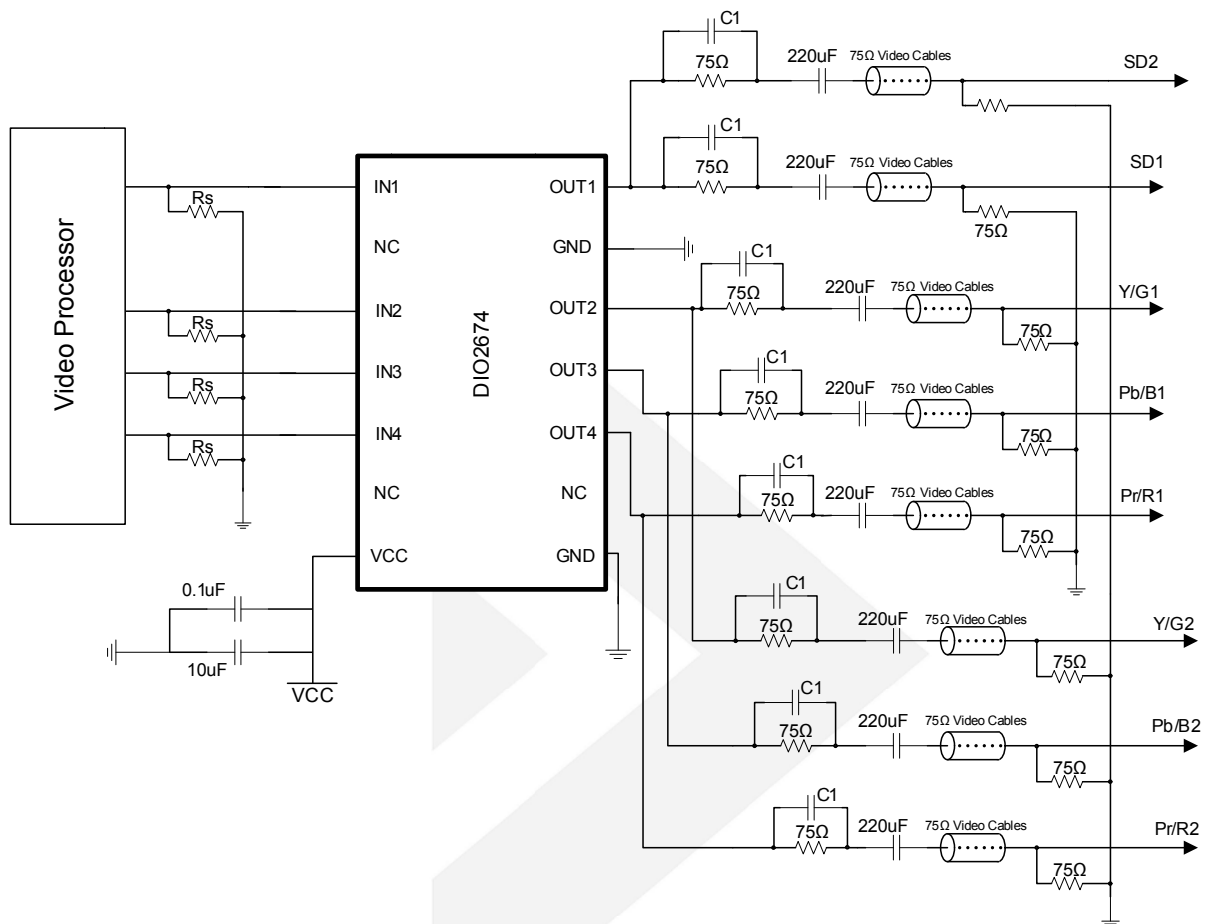


Figure 4 Input DC-Coupling Application and Output AC-Coupling with Double Load

Note: The value of C1 is recommended 2 to 4pF



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Applications Information

Functional Description

The DIO2674 provides 6dB gain from input to output. In addition, the input is slightly offset to optimize the output driver performance. The offset is held to the minimum required value to decrease the standing DC current into the load. Typical voltage levels are shown in Figure 5.

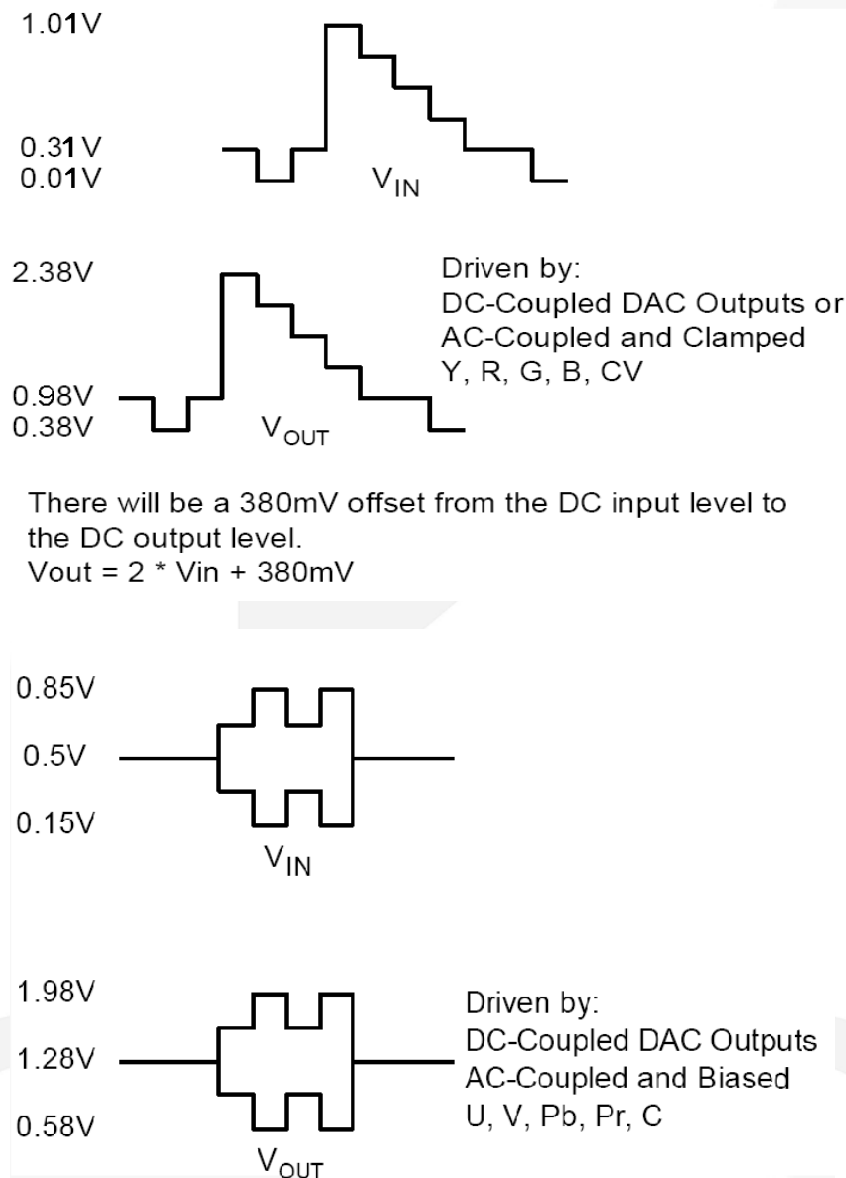


Figure 5. Typical Voltage Levels

The DIO2674 provides an internal diode clamp to support AC coupled input signals. If the input signal does not go below ground, the input clamp does not operate. This allows DAC outputs to directly drive the DIO2674 without an AC coupling capacitor. The worst-case sync tip compression due to the clamp does not exceed 7mV. The input level set by the clamp, combined with the internal DC offset, keeps the output within its acceptable range. When the input is AC-coupled, the diode clamp sets the sync tip (or lowest voltage) just below ground.

For symmetric signals like Pb and Pr; the average DC bias is fairly constant and the inputs can be AC-coupled with the addition of a pull-up resistor to set the DC input voltage. DAC outputs can also drive these same signals without the AC coupling capacitor. A conceptual illustration of the input clamp circuit is shown in Figure 6.

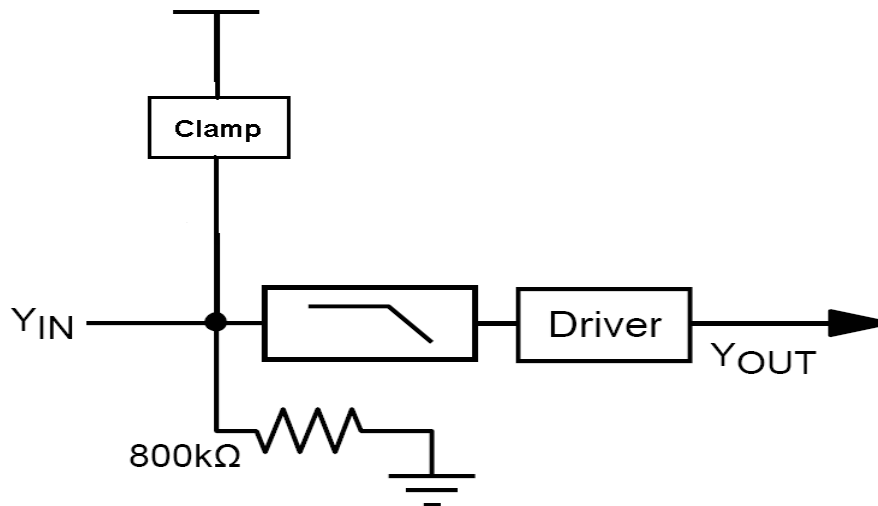


Figure 6. Input Clamp Circuit

I/O Configurations

For DC-coupled DAC drive with DC-coupled outputs, use the configuration in Figure 7.

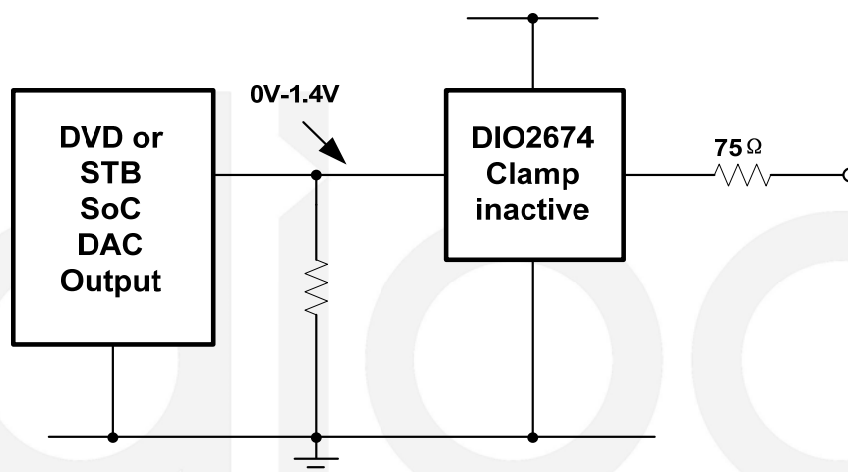


Figure 7. DC-coupled Inputs and Outputs

Alternatively, if the DAC's average DC output level causes the signal to exceed the range of 0V to 1.4V, it can be AC-coupled, as shown in Figure 8.

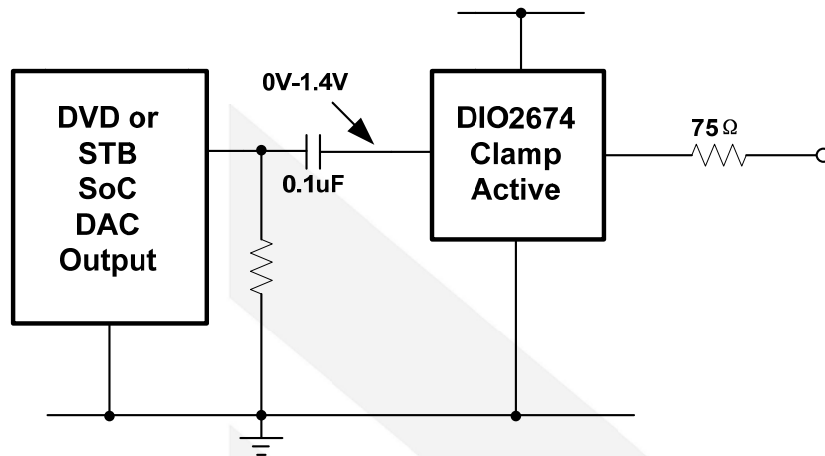


Figure 8. AC-coupled Inputs, DC-coupled Outputs

When the DIO2674 is driven by an unknown external source or a SCART with its own clamping circuitry the inputs should be AC-coupled, shown in Figure 9.

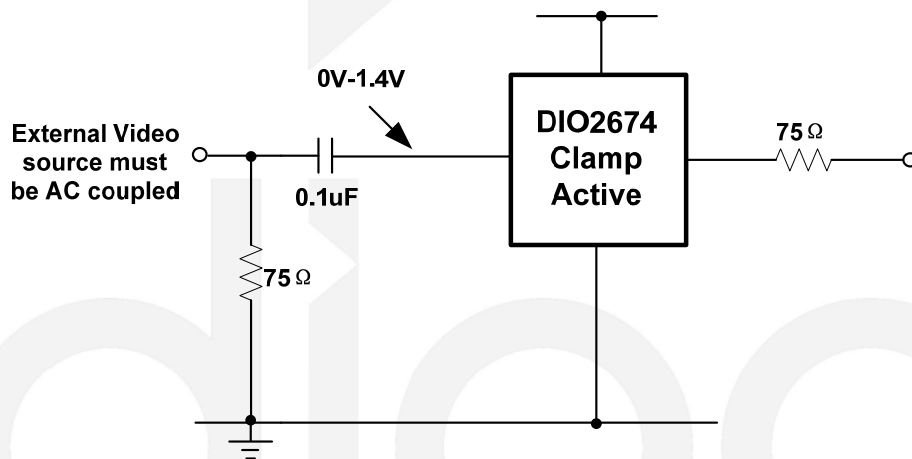


Figure 9. SCART with DC-coupled Outputs

The same method can be used for biased signals with the addition of a pull-up resistor to make sure the clamp never operates. The internal pull-down resistance is $800\text{k}\Omega \pm 20\%$, so the external resistance should be $7.5\text{M}\Omega$ to set the DC level to 500mV . If a pull-up resistance of less than $7.5\text{M}\Omega$ desired, add an external pull-down such that the DC input level is set to 500mV .

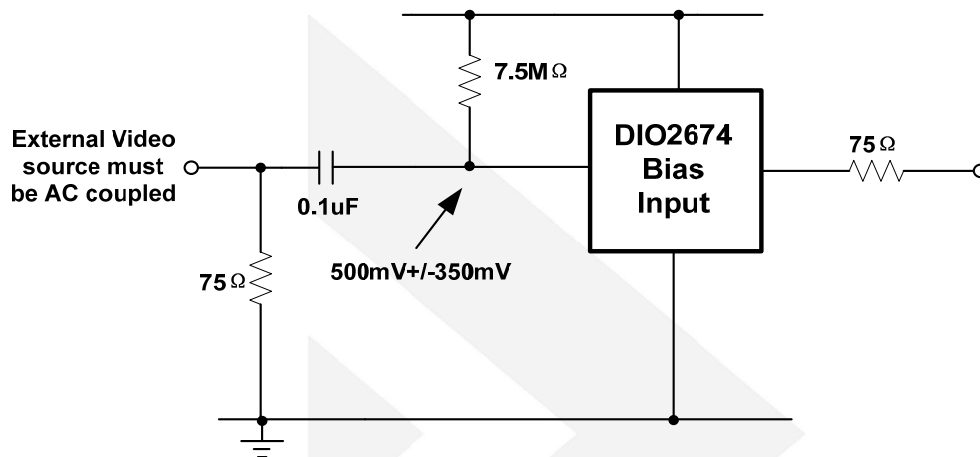


Figure 10. Biased SCART with DC-coupled Outputs

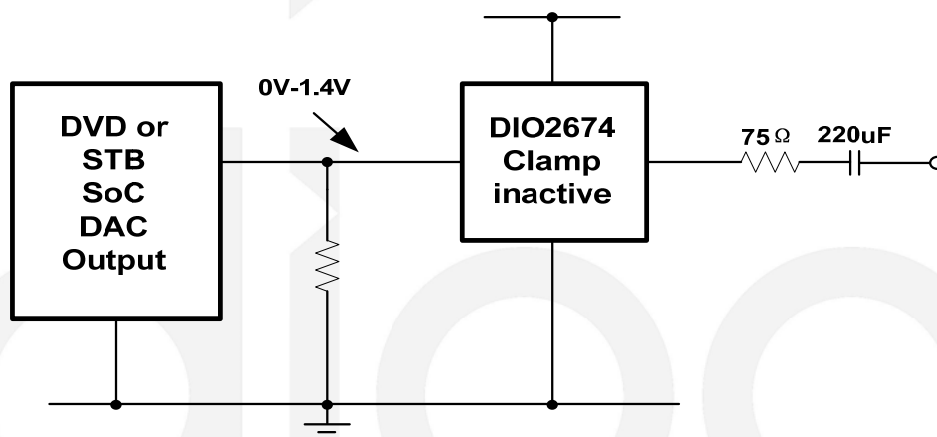


Figure 11. DC-coupled Inputs, AC-coupled Outputs

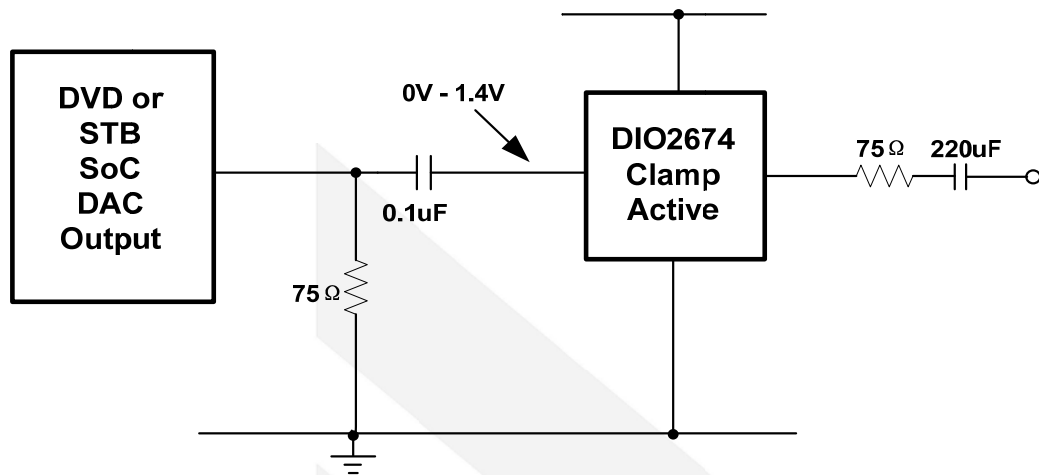


Figure 12. AC-coupled Inputs and Outputs

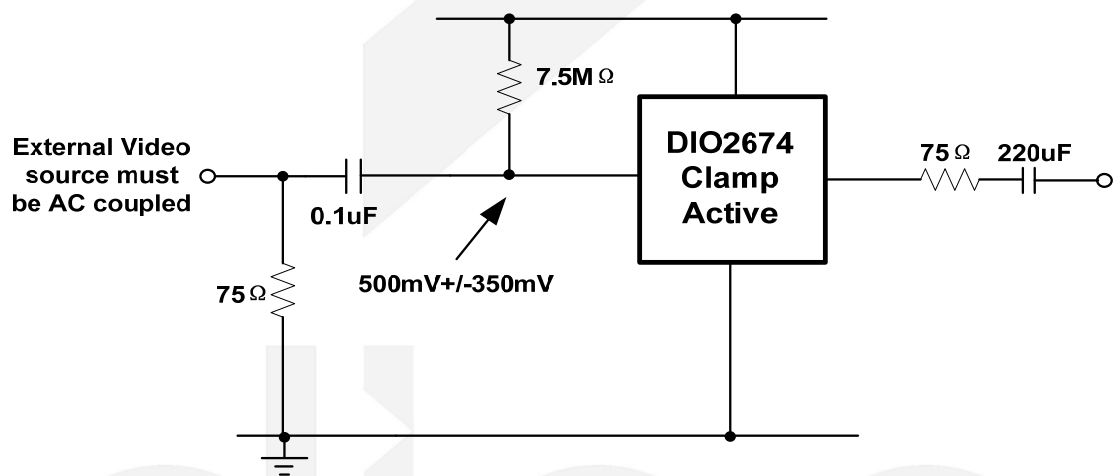


Figure 13. Biased SCART with AC-Coupled Outputs

Note: The video tilt or line time distortion is dominated by the AC-coupling capacitor. The value may need to be increased beyond 220 μF to obtain satisfactory operation in some applications.



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Power Dissipation

The DIO2674 output drive configuration must be considered when calculating overall power dissipation. Care must be taken not to exceed the maximum die junction temperature. The following example can be used to calculate the DIO2674's power dissipation and internal temperature rise.

$$T_J = T_A + P_d \cdot \Theta_{JA} \quad \text{where} \quad P_d = P_{CH1} + P_{CH2} + P_{CH3}$$

$$\text{and} \quad P_{CHx} = V_S \cdot I_{CH} - (V_O/R_L)$$

$$\text{Where } V_O = 2V_{IN} + 0.380V$$

$$I_{CH} = (I_{CC}/3) + (V_O/R_L)$$

V_{IN} = RMS value of input signal

$$I_{CC} = 78\text{mA}$$

$$V_S = 5V$$

R_L = channel load resistance

Board layout affects thermal characteristics. *Refer to the Layout Considerations section for more information.*

The DIO2674 is specified to operate with output currents typically less than 50mA, more than sufficient for a single (150Ω) video load. Internal amplifiers are current limited to a maximum of 120mA and should withstand brief duration, short-circuit conditions; however, this capability is not guaranteed.

Layout Consideration

Layout and supply bypassing play major roles in high frequency performance and thermal characteristics.

For optimum results, follow the steps below as a basis for high-frequency layout:

- Include 10μF and 0.1μF ceramic bypass capacitors
- Place the 10μF capacitor within 0.75 inches of the power pin.
- Place the 0.1μF capacitor within 0.1 inches of the power pin.
- Connect all external ground pins as tightly as possible, preferably with a large ground plane under the package.
- Layout channel connections to reduce mutual trace inductance.
- Minimize all trace lengths to reduce series inductances. If routing across a board, place device such that longer traces are at the inputs rather than the outputs. If using multiple, low-impedance DC coupled outputs, special layout techniques may be
- employed to help dissipate heat.

If a multilayer board is used, a large ground plane directly under the device helps reduce package case temperature.

For dual-layer boards, an extended plane can be used. Worst-case additional die power due to DC loading can be estimated at ($I^2 \cdot R_{load}$) per output channel. $75 \cdot (2.8/75)^2 \cdot 4 \cdot 50\% = 209\text{mW}$, total.



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CONTACT US

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