DIO5105
40V Half-Bridge HVIC

Features

- All-In-One Synchronous Buck Driver
- Bootstrapped High-Side Drive
- Programmable Dead-Time
- One PWM Signal Generates Both Drives
- Anti-cross Conduction Protection Circuitry
- EN for Disabling the Driver Outputs Meets CPU VR Requirement when Used with Patented Flex Mode Controller
- These are Pb-Free Devices

Applications

- Multiphase Desktop CPU Supplies
- Single-Supply Synchronous Buck Converters

Descriptions

The DIO5105 is a single Phase 40V MOSFET gate drivers optimized to drive the gates of both high-side and low-side power MOSFETs in a synchronous buck converter. The high-side and low-side driver is capable of driving a 3000pF load with a 20ns rise time and a 15ns fall time.

With a wide operating voltage range, high or low side MOSFET gate drive voltage can be optimized for the best efficiency. Internal adaptive non-overlap circuitry further reduces switching losses by preventing simultaneous conduction of both MOSFETs.

The floating top driver design can accommodate BST voltages as high as 40V, with transient voltages as high as 60V. Both gate outputs can be driven low by applying a low logic level to the Output Disable (EN) pin. An Under voltage Lockout function ensures that both driver outputs are low when the supply voltage is low, and a Thermal Shutdown function provides the IC with over temperature protection.

Ordering Information

Order Part Number	Top Marking		T_A	Package	
DIO5105MP10	DIO5105	Green	-40 to 85°C	MSOP-10	Tape & Reel, 3000

Pin Assignment

MSOP-10

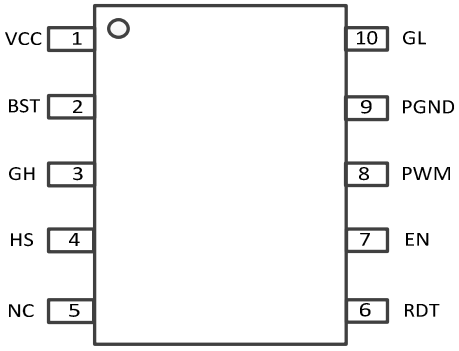

Figure 1 Top View

Pin Descriptions

Name	Description
VCC	Input Supply. A 1.0μF ceramic capacitor should be connected from this pin to PGND.
BST	Upper MOSFET Floating Bootstrap Supply. A capacitor connected between BST and HS pins holds this bootstrap voltage for the high-side MOSFET as it is switched. The recommended capacitor value is between 100nF and 1.0μF. An external diode is required with the DIO5105.
GH	Output drive for the upper MOSFET.
HS	Switch Node. Connected to the source of the upper MOSFET.
NC	No Connect.
RDT	A resistor from RDT to PGND programs the dead time. The resistor should be placed close to the IC to minimize noise coupling from adjacent PC board traces.
EN	Output Disable. When low, normal operation is disabled forcing GH and GL low.
PWM	Logic-Level Input. This pin has primary control of the drive outputs.
PGND	Power Ground. Should be closely connected to the source of the lower MOSFET.
GL	Output drive for the lower MOSFET.

Signal Truth Table

VCC	EN	GL	GH
$<V_{CCUV-}$	X	0	0
12V	3V	0	12V
12V	0V	0	0

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maxim rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Rating	Unit
V_{CC}	Main Supply Voltage Input	-0.3 ~ 18	V
BST	Bootstrap Supply Voltage Input	-0.3 ~ 58	V
HS	Switching Node (Bootstrap Supply Return)	V_{BST}-18 ~ V_{BST}+0.3	V
GH	High-Side Driver Output	V_{HS}-0.3 ~ V_{BST}+0.3	V
GL	Low-Side Driver Output	-0.3 ~ V_{CC}+0.3	V
PWM, EN	Control Input	-0.3 ~ V_{CC}+0.3	V
dV_S/dt	Offset voltage slew rate range	≤50	V/ns
Power Dissipation, P_D @ T_A = 25°C, MSOP-10		1.0	W
Package Thermal Resistance, Θ_{JA} MSOP-10		125	℃/W
Junction Temperature Range		≤150	℃
Storage Temperature Range		-55 ~ 150	℃

Recommend Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended Operating conditions are specified to ensure optimal performance to the datasheet specifications. DIOO does not Recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min	Max	Unit
V_{BST}	Bootstrap Supply Voltage Input	V_{HS}+3.0	V_{HS}+15	V
V_{HS}	Switching Node (Bootstrap Supply Return)	-2	40	V
V_{GH}	High-Side Driver Output	V_{HS}	V_{BST}	V
V_{CC}	Main Supply Voltage Input	3.0	15	V
V_{GL}	Low-Side Driver Output	0	V_{CC}	V
	Control Input (PWM,EN)	0	V_{CC}	V
T_A	Ambient Temperature	-40	125	℃

Electrical Characteristics

Typical value: Vcc=V_{BST}=12V, V_{HS}=PGND, RDT=100kΩ, T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply Current						
I_{QCC}	V_{CC} Quiescent Current	V_{PWM}=V_{EN}=0V		0.8	1.2	mA
I_{QBS}	V_{BST} Quiescent Current	V_{PWM}=V_{EN}=0V		0.4	0.6	mA
I_{LK}	Leakage Current	V_{BST}=V_{HS}=40V		0.1	5.0	μA
Input PWM						
$V_{PWM,TH+}$	PWM Rising Threshold			1.8	2.2	V
$V_{PWM,TH-}$	PWM Falling Threshold		0.8	1.5		V
V_{PWM+}	PWM High Input Bias Current	V_{PWM}=5V	12	20	30	μA
V_{PWM-}	PWM Low Input Bias Current	V_{PWM}=0V			1	μA
R_{PWM}	PWM Input Pull-down Resistor		160	260	400	kΩ
Input EN						
$V_{EN,TH+}$	EN Rising Threshold			1.8	2.2	V
$V_{EN,TH-}$	EN Falling Threshold		0.8	1.5		V
I_{EN+}	EN High Input Bias Current	V_{EN}=5V	12	20	30	μA
I_{EN-}	EN Low Input Bias Current	V_{EN}=0V			1	μA
R_{EN}	EN Input Pull-down Resistor		160	260	400	kΩ
UVLO						
V_{CCUV+}	UVLO Startup		2.6	2.9	3.2	V
V_{CCUV-}	UVLO Shutdown		2.4	2.7	3.0	V
V_{CCUVH}	Hysteresis		0.1	0.2		V
RDT Control						
V_{RDT}			0.9	1	1.1	V
I_{RDT}		RDT=0	0.75	1.0	1.25	mA
GH Output						
V_{OHH}	High-level output voltage	I_O=-20mA		0.05	0.85	V
V_{OLH}	Low-level output voltage	I_O=20mA		0.025	0.04	V

I_{OHH}	High-level output short-circuit pulse current	V_O=0V, V_{PWM}=5V	1.5	2.1		A
I_{OLH}	Low-level output short-circuit pulse current	V_O=12V, V_{PWM}=0V	1.8	2.5		A
GL Output						
V_{OHL}	High-level output voltage	I_O=-20mA		0.05	0.85	V
V_{OLL}	Low-level output voltage	I_O=20mA		0.025	0.04	V
I_{OHL}	High-level output short-circuit pulse current	V_O=0V, V_{PWM}=5V	1.5	2.1		A
I_{OLL}	Low-level output short-circuit pulse current	V_O=12V, V_{PWM}=0V	1.8	2.5		A
Switching Time						
ton	Output rising edge transmission time	RDT=10k		160	240	ns
		RDT=100k		490	600	ns
toff	Output falling edge transmission time			90	150	ns
DT	Dead time	RDT=10k		70		ns
		RDT=20k		110		ns
		RDT=30k		130		ns
		RDT=40k		150		ns
		RDT=100k		400		ns
tr	Output rising time	C_L=3000pF		20		ns
tf	Output falling time	C_L=3000pF		15		ns
MT	High-low side delay match	RDT=10k			30	ns
		RDT=100k			50	ns
ten	Enable startup delay time	RDT=10k		160	240	ns
tsd	Enable shutdown delay time			90	150	ns

Specifications subject to change without notice.

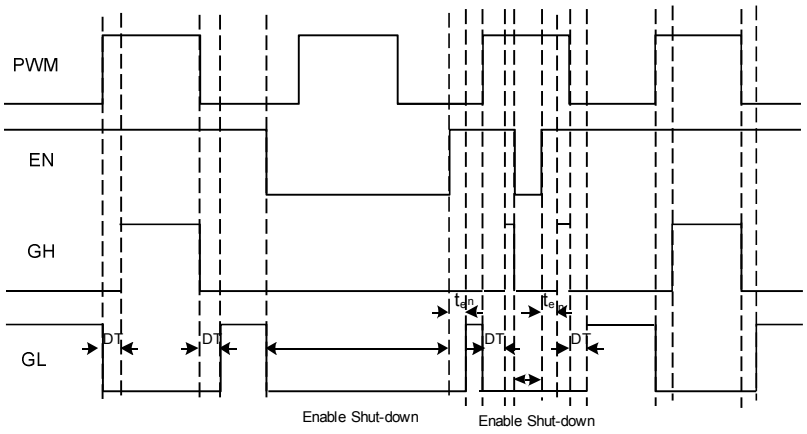

Figure 2. Non-overlap Timing Diagram

Application Circuit

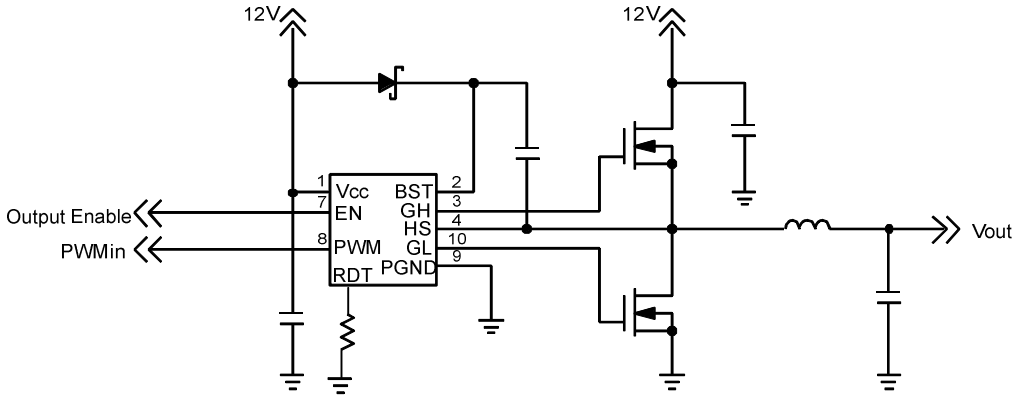

Figure 3. Example Circuit

Functional Block Diagraph

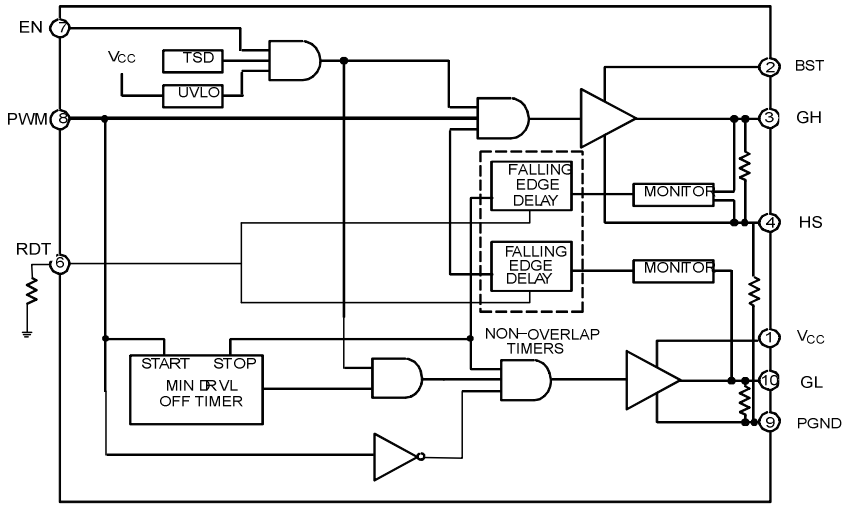

Figure 4. Functional Block Diagraph

Application Information

Overview

The DIO5105 is a single PWM input gate driver with Enable that offers a programmable dead-time. The dead-time is set with a resistor at the RDT pin and can be adjusted from 30ns to 500ns. The wide dead-time programming range provides the flexibility to optimize drive signal timing for a wide range of MOSFETs and applications.

The RDT pin is biased at 1V and current limited to 1mA maximum programming current. The time delay generator will accommodate resistor values from 0k to 200k with a dead-time time that is proportional to the RDT resistance. Grounding the RDT pin programs the DIO5105 to drive both outputs with minimum dead-time.

Theory of Operation

The DIO5105 are single phase MOSFET drivers designed for driving two N−channel MOSFETs in a synchronous buck converter topology. The DIO5105 will operate from 2.7V to 15V, but have been optimized for high current multi−phase buck regulators that convert 12V rail directly to the core voltage required by complex logic chips. A single PWM input signal is all that is required to properly drive the high−side and the low−side MOSFETs. Each driver is capable of driving a 3nF load at frequencies up to 1MHz.

Low-Side Driver

The low−side driver is designed to drive a ground−referenced low $R_{DS(on)}$ N−Channel MOSFET. The voltage rail for the low−side driver is internally connected to the VCC supply and PGND.

High-Side Driver

The high−side driver is designed to drive a floating low $R_{DS(on)}$ N−channel MOSFET. The gate voltage for the high side driver is developed by a bootstrap circuit referenced to Switch Node (HS) pin.

The bootstrap circuit is comprised of an external diode, and an external bootstrap capacitor. When the DIO5105 are starting up, the HS pin is at ground, so the bootstrap capacitor will charge up to V_{CC} through the bootstrap diode See Figure 3. When the PWM input goes high, the high−side driver will begin to turn on the high−side MOSFET using the stored charge of the bootstrap capacitor. As the high−side MOSFET turns on, the HS pin will rise. When the high−side MOSFET is fully on, the switch node will be at 12V, and the BST pin will be at 12V plus the charge of the bootstrap capacitor (approaching 24V).

The bootstrap capacitor is recharged when the switch node goes low during the next cycle.

Safety Timer and Overlap Protection Circuit

It is very important that MOSFETs in a synchronous buck regulator do not both conduct at the same time. Excessive shoot−through or cross conduction can damage the MOSFETs, and even a small amount of cross conduction will cause a decrease in the power conversion efficiency.

The DIO5105 prevent cross conduction by monitoring the status of the external MOSFETs and applying the appropriate amount of “dead−time” or the time between the turn off of one MOSFET and the turn on of the other MOSFET.

When the PWM input pin goes high, GL will go low after a propagation delay. The time it takes for the low−side MOSFET to turn off is dependent on the total charge on the low−side MOSFET gate. The DIO5105 monitor the gate voltage of both MOSFETs and the switch node voltage to determine the conduction status of the MOSFETs.

Once the low−side MOSFET is turned off an internal timer will delay the turn on of the high−side MOSFET.

Likewise, when the PWM input pin goes low, GH will go low after the propagation delay. The time to turn off the high−side MOSFET is dependent on the total gate charge of the high−side MOSFET. A timer will be triggered once the high−side MOSFET has stopped conducting, to delay the turn on of the low−side MOSFET.

Power Supply Decoupling

The DIO5105 can source and sink relatively large currents to the gate pins of the external MOSFETs. In order to maintain a constant and stable supply voltage (V_{CC}) a low ESR capacitor should be placed near the power and ground pins. A 1μF to 4.7μF multi layer ceramic capacitor (MLCC) is usually sufficient.

Input Pins

The PWM input and the Output Disable pins of the DIO5105 have internal protection for Electro Static Discharge (ESD), but in normal operation they present a relatively high input impedance. If the PWM controller does not have internal pull down resistors, they should be added externally to ensure that the driver outputs do not go high before the controller has reached its under voltage lockout threshold.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_B) and the internal (or an external) diode. Selection of these components can be done after the high−side MOSFET has been chosen. The bootstrap capacitor must have a voltage rating that is able to withstand twice the maximum supply voltage. A minimum 50V rating is recommended. The capacitance is determined using the following equation:

$$C_B = \frac{Q_{GATE}}{\Delta V_B}$$

where Q_{GATE} is the total gate charge of the high−side MOSFET, and _V_{BST} is the voltage droop allowed on the high−side MOSFET drive.

The bootstrap diode must be rated to withstand the maximum supply voltage plus any peak ringing voltages that may be present on HS. The average forward current can be estimated by:

$$I_{F(AVG)} = Q_{GATE} \times f_{MAX}$$

Where f_{MAX} is the maximum switching frequency of the controller. The peak surge current rating should be checked in−circuit, since this is dependent on the source impedance of the 12V supply and the ESR of C_B.

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