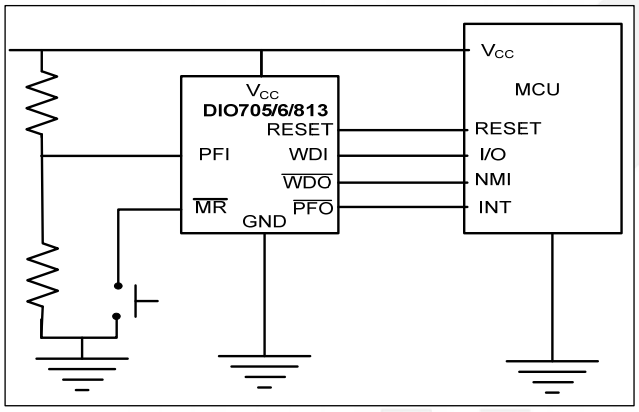
DIO705/706/707/708/813
Low Power Microprocessor Supervisory Circuits

Features

- Guaranteed reset valid at V_{CC}=1.15V
- Reset threshold can be from 2.6V to 5.0V with 0.1V step
- Low operating current: 52uA@5V
- Reset pulse width:200ms
- Independent watchdog timer, 1.6s timeout
- Voltage monitor for power fail or low battery warning
- Pin-to-Pin compatible with industry standard 705/706/707/708/813
- Available in Package of SOIC-8

Typical Application



Descriptions

DIO705/706/707/708/813 series is a family of microprocessor (uP) supervisory circuit that monitors microprocessor's supply voltage and battery voltage. The series integrates uP reset circuit with 200ms delay; Watchdog, manual reset circuit and a power fail comparator with 1.22V threshold. These devices reduce system complexity, hence improve system reliability.

DIO705/706/707/708/813 series has several functional options. Each device generates a reset signal when V_{CC} is lower than reset threshold. In addition, DIO705, DIO706 and DIO813 have a watchdog timer whose timeout period is 1.6s. DIO707 and DIO708 provide both active low and active high reset signals, but have no watchdog function. DIO813 are same as DIO705/706 except active high reset is provided instead of active low. DIO705/706/707/708/813 series is ideal for applications in automotive systems, computers, controllers and intelligent instruments. All devices are available in SOIC-8 package.

Applications

- Computers
- Controllers
- Intelligent instruments
- Automotive systems

Ordering Information

Order Part Number	Top Marking	Green	T_A	Package	
DIO705CS8	DIO705	Yes	-40 to 85°C	SOIC-8	Tape & Reel, 2500
DIO706XCS8	DIO706X	Yes	-40 to 85°C	SOIC-8	Tape & Reel, 2500
DIO707CS8	DIO707	Yes	-40 to 85°C	SOIC-8	Tape & Reel, 2500
DIO708XCS8	DIO708X	Yes	-40 to 85°C	SOIC-8	Tape & Reel, 2500
DIO813XCS8	DIO813X	Yes	-40 to 85°C	SOIC-8	Tape & Reel, 2500

Ordering Information

Ordering Code = Part No. + Package Code;

CS: stands for SOIC-8

X: Refer to Device Function Reference Table as Below

Device Function Reference Table

Part No.	Reset Threshold	Reset Active Low or High	Watchdog Function
DIO705	4.65V	Low	Yes
DIO707	4.65V	Low and High	No
DIO813L	4.65V	High	Yes
DIO706	4.4V	Low	Yes
DIO708	4.4V	Low and High	No
DIO813M	4.4V	High	Yes
DIO706J	4.0V	Low	Yes
DIO708J	4.0V	Low and High	No
DIO813J	4.0V	High	Yes
DIO706T	3.08V	Low	Yes
DIO708T	3.08V	Low and High	No
DIO813T	3.08V	High	Yes
DIO706S	2.93V	Low	Yes
DIO708S	2.93V	Low and High	No
DIO813S	2.93V	High	Yes
DIO706R	2.63V	Low	Yes
DIO708R	2.63V	Low and High	No
DIO813R (DIO706P)	2.63V	High	Yes

Pin Assignments

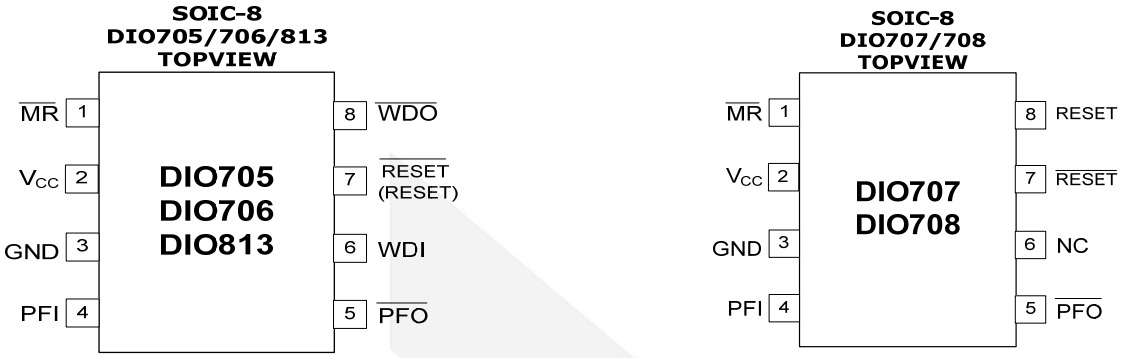


Figure 1 Pin Assignment

Pin Description

Pin No.			Name	Function
DIO705 DIO706X	DIO707 DIO708X	DIO813X DIO706P		
1	1	1	$\overline{MR}$	Manual reset input. *When voltage at $\overline{MR}$ is pulled low, a reset pulse will be triggered. The active low input has a pull up current. It can be driven by TTL or CMOS logic as well as shorted to GND with a switch*
2	2	2	V_{CC}	Positive supply input
3	3	3	GND	Negative supply input
4	4	4	PFI	Power fail monitor input. *When the voltage at PFI is below than 1.22V, $\overline{PFO}$ goes low, Connect PFI to GND or V_{CC} when not used.*
5	5	5	$\overline{PFO}$	Power fail monitor output. *When the voltage at PFI is less than 1.22V, $\overline{PFO}$ goes low; otherwise $\overline{PFO}$ goes high.*
6		6	WDI	Watch-dog input. *If WDI remains high or low for 1.6s, the on chip watchdog timer runs out and $\overline{WDO}$ goes low. Floating WDI or connecting WDI to high impedance three state buffer disables watchdog function. The watchdog timer clears whenever RESET is asserted, or WDI is three stated, or WDI sees a rising or falling edge.*
7	7		$\overline{RESET}$	Active low reset output. *$\overline{RESET}$ stays in low if V_{CC} is lower than reset threshold; it remains in low for 200ms after V_{CC} becomes higher than reset threshold or $\overline{MR}$ goes from low to high.*
8		8	$\overline{WDO}$	Watchdog output. *$\overline{WDO}$ goes low if watchdog timer finishes its 1.6s count, and will not go high again until the watchdog timer is cleared. Whenever V_{CC} is below reset threshold, $\overline{WDO}$ stays low, and as soon as V_{CC} rises above reset threshold, $\overline{WDO}$ goes high without delay.*
	8	7	RESET	Active high reset output. *RESET stays in high if V_{CC} is lower than reset threshold; it remains in high for 200ms after V_{CC} becomes higher than reset threshold or $\overline{MR}$ goes from low to high.*

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maxim rating conditions for extended periods may affect device reliability.

Parameter		Rating	Unit
Terminal Voltage(With respect to GND)	V_{CC}	-0.3 to 6.0	V
	Other Inputs	-0.3 to 6.0	
Terminal Current	V_{CC}	20	mA
	GND	20	mA
	All Input Pins	20	mA
	All Output Pins	20	mA
Thermal Resistance(DIP8)		120	°C/W
Power Dissipation(SOIC8)		190	°C/W
Maximum Junction Temperature		150	°C
Operating Temperature/T_A		-40 to 85	°C
Storage Temperature/T_{STO}		-65 to 150	°C
Lead Temperature Rating		300	°C
ESD Rating	HBM	2	KV

Electrical Characteristics

Typical value: T_A = 25°C, V_{CC}=5V, unless otherwise specified.

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{CC}	Operating Voltage Range		1.15		5.5	V
I_{VCC}	Supply Current	DIO705/706X/813X		52	105	uA
		DIO707/708X		30	60	
V_{RES}	Reset Threshold	DIO705/707/813L	4.5	4.65	4.75	V
		DIO706/708/813M	4.25	4.4	4.5	
		DIO706J/708J/813J	3.9	4.0	4.1	
		DIO706T/708T/813T	3.0	3.08	3.15	
		DIO706S/708S/813S	2.85	2.93	3.0	
		DIO706P/706R/708R/813R	2.55	2.63	2.70	

H_{VRES}	Reset Threshold Hysteresis				0.01V_{RES}		V
t_{RES}	Reset Pulse Width			140	200	280	ms
V_{OH1}	$\overline{\text{RESET}}$ or RESET Output Voltage	I_{SOURCE}=800uA, V_{CC}=5V		V_{CC}-1.2			V
		I_{SOURCE}=8uA, V_{CC}=1.2V		1.0			
V_{OL1}		I_{SINK}=3.2mA, V_{CC}=5V				0.3	
		I_{SINK}=150uA, V_{CC}=1.2V				0.3	
t_{WD}	Watchdog timeout period			1	1.6	2.25	s
t_{WP}	WDI Pulse Widht	V_{CC}=5V		50			ns
		V_{CC}<4.5V		120			
	WDI Input Threshold	Low				0.16V_{CC}	V
		High	V_{CC}=5V	3.5			
			V_{CC}<4.5V	0.75V_{CC}			
	WDI Pull up Resistance	V_{CC}>V_{RES}		125	250	500	kΩ
	WDI Pull down Resistance	V_{CC}>V_{RES}		88	175	350	
V_{OH1}	$\overline{\text{WDO}}$ Output Voltage	I_{SOURCE}=800uA		V_{cc}-1.2			V
V_{OL2}		I_{SINK}=3.2mA				0.3	
	$\overline{\text{MR}}$ Pull up Current	$\overline{\text{MR}}$=0V, V_{CC}=5V		100	250	600	uA
		$\overline{\text{MR}}$=0V, V_{CC}=4V		60	152	360	
		$\overline{\text{MR}}$=0V, V_{CC}=3V		32	75	180	
		$\overline{\text{MR}}$=0V, V_{CC}=2.5V		20	44	105	
$T_{\overline{MR}}$	$\overline{\text{MR}}$ Pulse Width	V_{CC}=5V		150			ns
		V_{CC}<4.5V		500			ns
	$\overline{\text{MR}}$ Input Threshold	V_{CC}=5V	Low			0.8	V
			High	2.0			
		V_{CC}<4.5V	Low			0.16V_{CC}	V
			High	0.65V_{CC}			
t_{MD}	$\overline{\text{MR}}$'s Delay to RESET	V_{CC}=5V				250	ns
		V_{CC}<4.5V				750	ns
V_{PFI}	PFI Input Threshold			1.184	1.22	1.256	V
I_{PFI}	PFI Input Current				0		nA
V_{OH3}	$\overline{\text{PFO}}$ Output Voltage	I_{SOURCE}=800uA		V_{CC}-1.2			V
V_{OL3}		I_{SINK}=3.2mA				0.3	

Specifications subject to change without notice.

Block Diagram

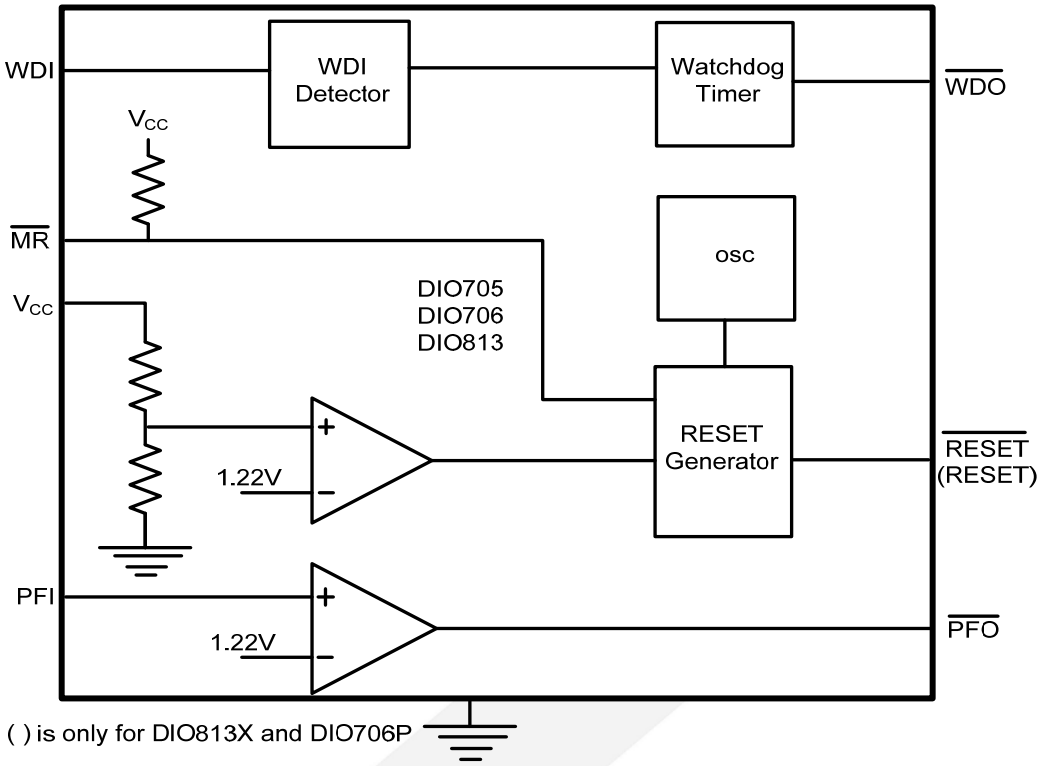


Figure 2 DIO705/706X/813X Block Diagram

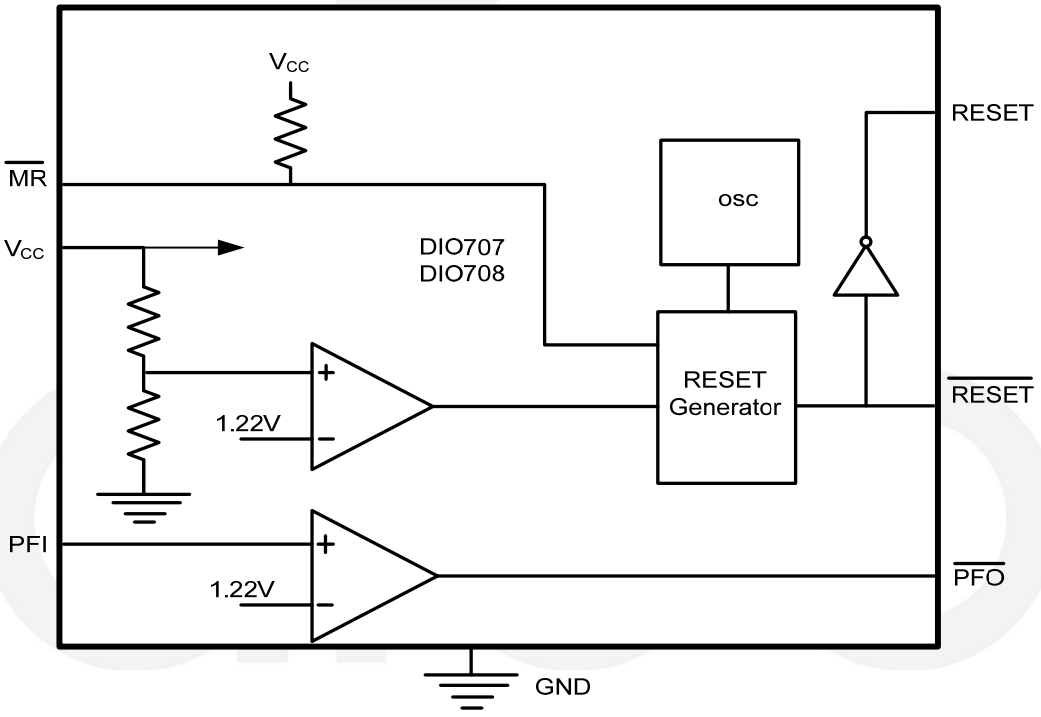
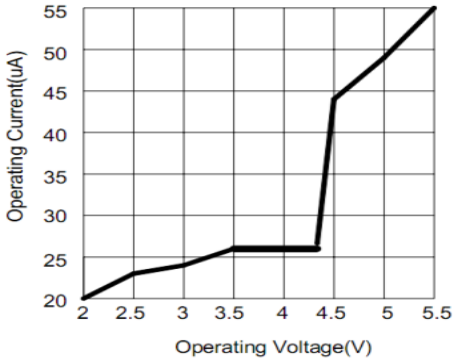


Figure 3 DIO707/708X Block Diagram

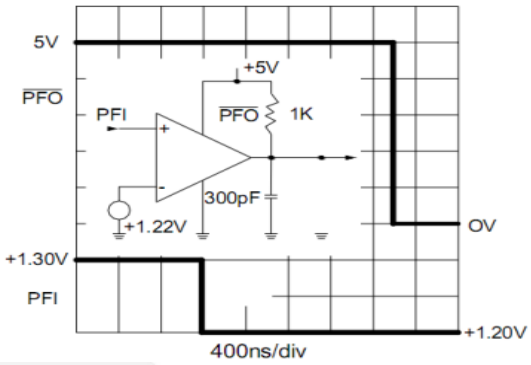
Typical Operating Characteristics

All typical value are at V+=5V, T_A = 25°C, unless otherwise specified.

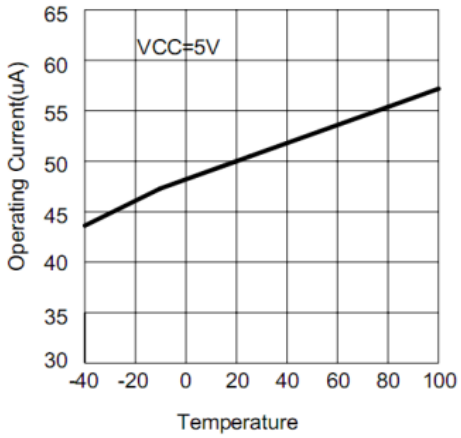
DIO706 Operating Current Vs. Operating Voltage



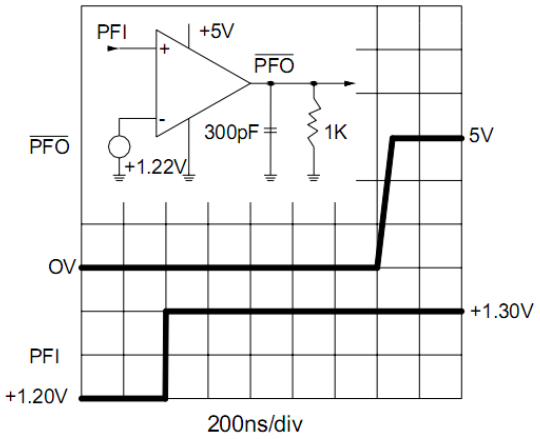
Power-fail Comparator Assertion Response Time



DIO706 Operating Current Vs. Temperature



Power-fail Comparator De-assertion Response Time



Application Information

DIO705/706/707/708/813 series is a microprocessor supervisory circuit that monitors the power supply to digital circuits such as microprocessor, controller and memory. These devices assert reset during power up, power down or brownout condition to prevent code execution errors.

RESET Output

On power up, once V_{CC} reaches 1.15V, DIO705/706/707/708/813 series output a reset signal. As V_{CC} increases, the reset signal stays valid; When V_{CC} rises above reset threshold, an internal timer releases RESET ($\overline{RESET}$) after 200ms. RESET ($\overline{RESET}$) becomes valid once V_{CC} dips below reset threshold during power down or in brownout condition. If brownout occurs in the middle of a previously initiated reset pulse, the pulse will continue for at least another 200ms. On power down, once V_{CC} falls below reset threshold, RESET stays valid and is guaranteed in the correct logic state until V_{CC} drops below 1.15V for the whole temperature range. Please refer to Figure 5. DIO705/706 series provide active low $\overline{RESET}$ signal；DIO707/708 series provide both active high and active low $\overline{RESET}$ signals；DIO813 series provide active high RESET signal.

Watchdog Timer

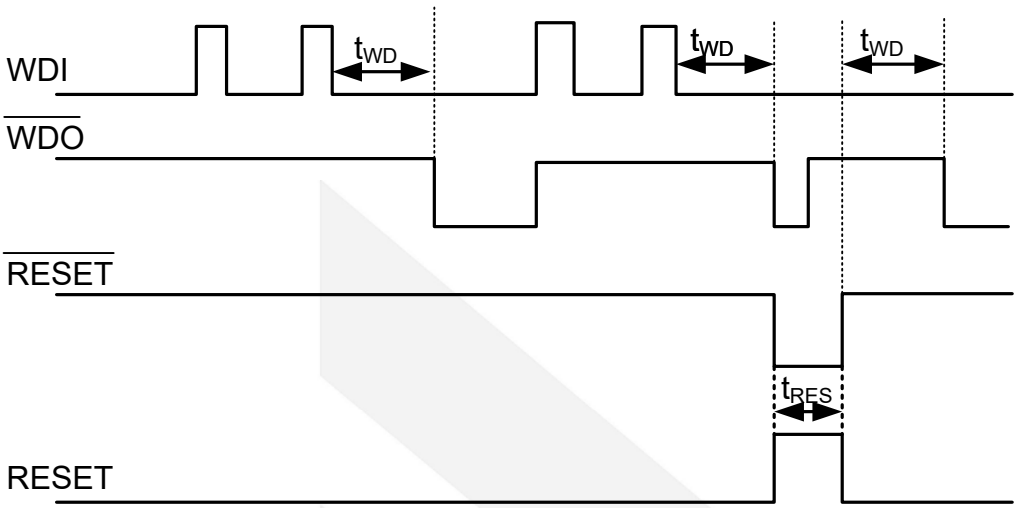
DIO705/706/813 series have an independent watchdog timer that can monitor uP's activity. If uP does not toggle the watchdog input (WDI) within 1.6s and WDI is not three-stated, $\overline{WDO}$ goes low. As long as RESET is asserted, or WDI is three-stated, or WDI is left floating, the watchdog timer stays cleared and will not count, in this case $\overline{WDO}$ is in high state. When V_{CC} stays below reset threshold, $\overline{WDO}$ goes low whether or not the watchdog timer has timed out yet. Please refer to figure 4.

Manual Reset

Manual reset input allows reset signal to be triggered by push button or switch. The push button or switch is effectively denounced by 140ms minimum reset pulse width. $\overline{MR}$ is TTL/CMOS logic compatible. $\overline{MR}$ can be used to force a watchdog timeout to generate a reset pulse in DIO705/706/813 series by connecting $\overline{WDO}$ to $\overline{MR}$. Please refer to Figure 5.

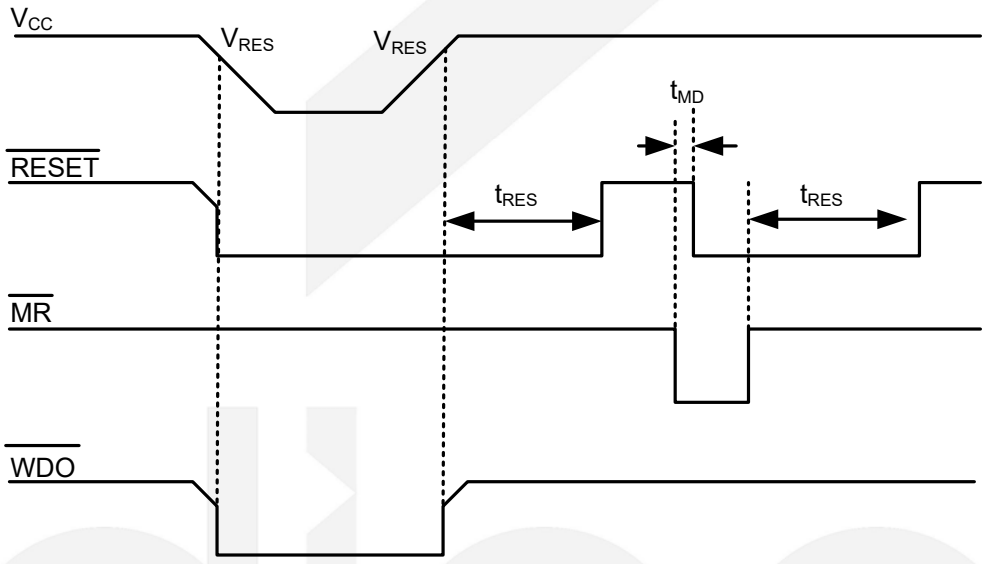
Power fail Comparator

The power fail comparator can be used for various purpose because its output and non-inverting input are not internally connected. The inverting input is internally connected to a 1.22V reference voltage.



Note 1: RESET (RESET) is triggered by $\overline{MR}$
Note 2: RESET is only for DIO813X and DIO706P

Figure 4. Watchdog Timing



Note:Active high RESET is the inverse of the $\overline{RESET}$ shown

Figure 5 RESET, $\overline{MR}$ and $\overline{WDO}$ timing WDI floating

Ensuring a Valid RESET Output Down to V_{CC}=0V

When V_{CC} falls below 1.15V, the DIO705/706/707/708 series $\overline{RESET}$ output no longer sinks current, it becomes an open circuit, and hence $\overline{RESET}$ output is at undetermined voltage. If a pull-down resistor is added from $\overline{RESET}$ pin to GND as shown in Figure 6, then $\overline{RESET}$ output will be held at low state. The resistor's value is not critical. it should be about 100KΩ, large enough not to load, small enough to pull $\overline{RESET}$ to ground.

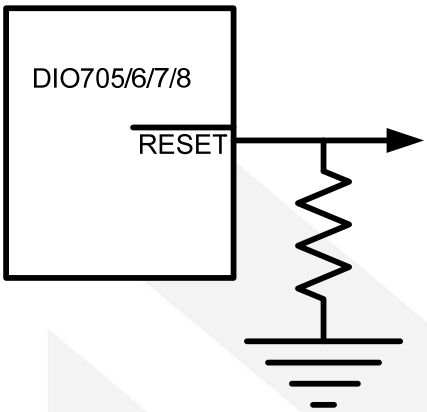


Figure 6 RESET Valid to Ground Circuit

Monitoring Voltages other than The unregulated DC Input

You can monitor voltages other than the unregulated DC by connecting a voltage divider to PFI and adjusting the ratio appropriately. If required, add a hysteresis by connecting a resistor (with a value approximately 10 times the sum of 2 resistors in voltage divider network) between PFI and $\overline{PFO}$. A capacitor between PFI and GND will reduce the power fail circuit's sensitivity to high-frequency noise on the line being monitored. RESET can be asserted on the other voltage in addition to V_{CC} line by connecting $\overline{PFO}$ pin to $\overline{MR}$ pin, in this case, a RESET pulse will be initiated when PFI drops below 1.22V. Figure 7 shows DIO705/706/707/708 series configured to assert RESET when V_{CC} falls below reset threshold, or when 12V power supply falls below 10V.

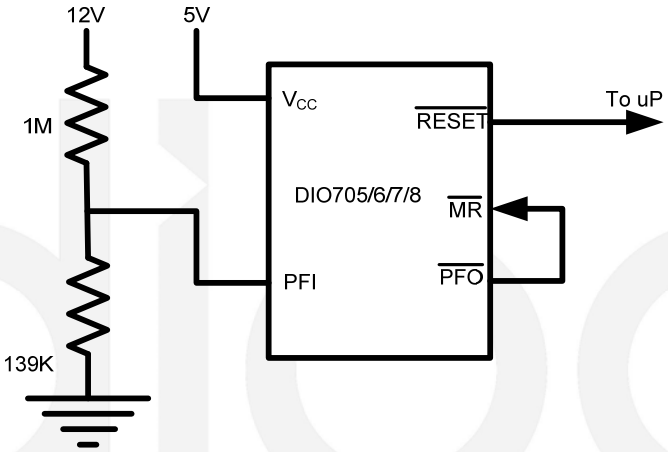


Figure 7 Monitoring Both 5V and 12V

Monitoring a Negative Voltage

The power fail comparator can also monitor a negative supply rail as shown in Figure 8. When the negative rail is good (A negative voltage of large magnitude), $\overline{PFO}$ is low, and when the negative rail is degraded (A negative voltage of less magnitude), $\overline{PFO}$ is high. By adding the resistors and transistor as shown, a high $\overline{PFO}$ triggers a RESET pulse. As long as $\overline{PFO}$ remains high, the DIO705/706/707/708/813 series will keep RESET asserted. Note that the circuit's accuracy depends on the PFI threshold tolerance, the V_{CC} line and the resistors.

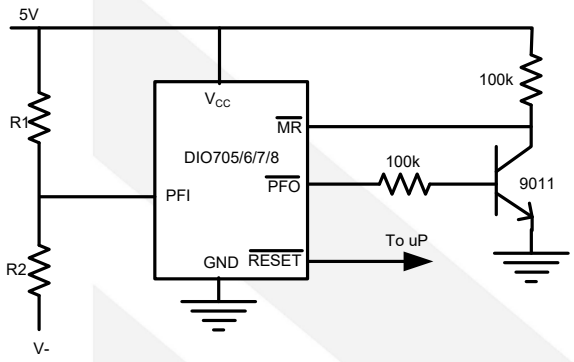


Figure 8 Monitoring A Negative Voltage

Interfacing to uPs with Bidirectional Reset Pins

uPs with bi-directional reset pins, such as the MOTOROLA 68HC11 series, can contend with DIO705/706/707/708/813 series RESET output. For example, if the RESET output is driven high and uP wants to pull it low, indeterminate logic levels may result. To correct this, connect a 4.7KΩ resistor between the RESET output and the uP reset I/O as shown in Figure 9. Buffer the RESET output to other system components.

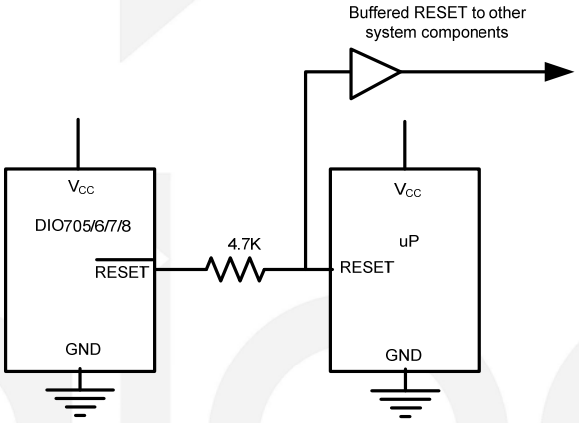


Figure 9 Interfacing to uPs with Bidirectional Reset I/O

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