USB Type-C Analog Audio Switch with Protection Function, Moisture detection and Audio Jack Detection

Features

- Power supply: 2.7 V to 5.5 V
- Version information:
  - DIO4485 default: DP_R~DP1; DN_L~DN1; SBU1~SBU1_H; SBU2~SBU2_H turn on
  - DIO4485B default: DP_R~DP1; DN_L~DN1 turn on
- USB 2.0 switch -3dB bandwidth: 1.05 GHz
- Audio switch:
  - Negative rail capability: -3.6 V to 3.6 V;
  - THD+N = -110 dB ,1V_{RMS}, f = 20 Hz~20 kHz, 32 Ω load;
  - −3dB bandwidth: 940 MHz
- UART switch -3dB bandwidth: 800 MHz
- High voltage protection:
  - +20 V DC tolerance on USB Type-C pins
  - ±25 V surge capable on USB Type-C pins
- Overvoltage protection:
  DP_R, DN_L, SBU1/SBU2/GSBU1/GSBU2 V_{TH} = 4.4 V (default), 4.4 V ~ 5.0 V configurable, 0.2V/step
- Support OMTP, CTIA and 3-pole audio jack pinout
- Built-in moisture detection function, including moisture resistor and moisture voltage mode. Support single-pin mode and multi-pin mode. Support polling mode, and polling time is I^2C configurable.
- Support 1.2 V and 1.8 V I/O logic

Applications

- Mobile phone
- Tablets

Package Information

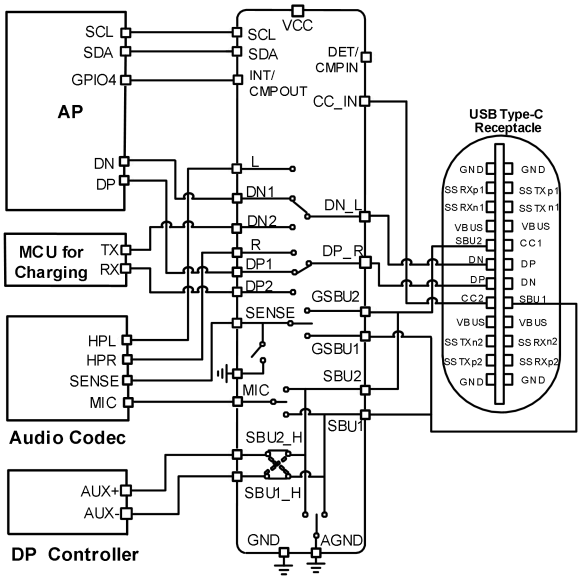
Part Number	Package	Body Size
DIO4485/B	WLCSP-25	2.24 mm × 2.28 mm

Description

The DIO4485 / DIO4485B is a high-performance USB Type-C analog switch for the use in portable multimedia devices, supporting analog audio headsets. The DIO4485 / DIO4485B can detect OMTP, CTIA, or 3-pole headsets and configure pinouts automatically. The DIO4485 / DIO4485B shares common Type-C pins to pass USB 2.0 signals and analog audio signals; the sideband uses wires and analog microphone signals. The DIO4485 / DIO4485B also supports high voltage and surge on SBUx pins and USB pins on the USB Type-C receptacle side.

The DIO4485 / DIO4485B supports the moisture detection for five pins, including CC_IN, DP_R, DN_L, SBU1 and SBU2. Moisture detection function can detect both moisture resistance and voltage. The detection mode includes single-pin mode and multi-pin mode. The multi-pin mode supports the detection polling, and the polling time can be configured through I^2C.

Simplified Schematic



Ordering Information

Ordering Part No.	Top Marking	MSL	RoHS	T_A	Package	
DIO4485WL25	D4HE	1	Green	-40 to 85°C	WLCSP-25	Tape & Reel, 3000
DIO4485BWL25	DH5B	1	Green	-40 to 85°C	WLCSP-25	Tape & Reel, 3000

If you encounter any issue in the process of using the device, please contact our customer service at marketing@dioo.com or phone us at (+86)-21-62116882. If you have any improvement suggestions regarding the datasheet, we encourage you to contact our technical writing team at docs@dioo.com. Your feedback is invaluable for us to provide a better user experience.

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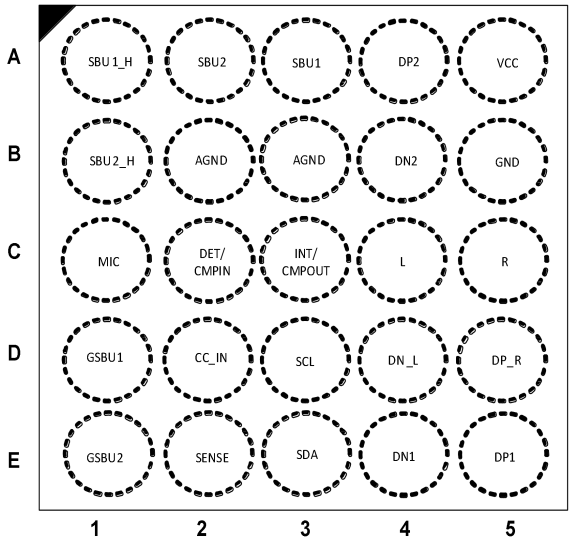


WLCSP-25 (Top view)

Pin No.	Name	Description
A5	VCC	Power supply (2.7 to 5.5 V)
B5	GND	Chip ground
D5	DP_R	USB/Audio common pin
D4	DN_L	USB/Audio common pin
E5	DP1	USB data1 (differential +)
E4	DN1	USB data1 (differential –)
C5	R	Audio – right channel
C4	L	Audio – left channel
A3	SBU1	Sideband use wire 1
A2	SBU2	Sideband use wire 2
C1	MIC	Microphone signal
B2	AGND	Audio signal ground
B3	AGND	Audio signal ground
E2	SENSE	Audio ground reference output
C3	INT/ CMPOUT	Open-drain comparator output, set as CMPOUT when 0x12h bit [4] = 1
		Open-drain output, set as INT when 0x12h bit [4] = 0. I^2C interrupt output, active low (open-drain)
D2	CC_IN	Audio accessory attachment detection input
D1	GSBU1	Audio sense path 1 to headset jack GND
E1	GSBU2	Audio sense path 2 to headset jack GND

C2	DET/ CMPIN	Comparator input, set as COMPIN when 0x12h bit [4] = 1
		Open-drain output, set as DET when 0x12h bit [4] = 0. DET is low when CC_IN > 1.5 V DET is high when CC_IN < 1.2 V
D3	SCL	I^2C clock
E3	SDA	I^2C data
B1	SBU2_H	Host side sideband use wire 2
A1	SBU1_H	Host side sideband use wire 1
A4	DP2	USB data2 (differential +)
B4	DN2	USB data2 (differential –)

2. Absolute Maximum Ratings

Exceeding the maximum ratings listed under Absolute Maximum Ratings when designing is likely to damage the device permanently. Do not design to the maximum limits because long-time exposure to them might impact the device's reliability. The ratings are obtained over an operating free-air temperature range unless otherwise specified.

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply voltage from V_{CC}		-0.5	6.5	V
V_{CC_IN}	V_{CC_IN}, to GND		-0.5	20	V
V_{SW_C}	V_{DP_R} to GND, V_{DN_L} to GND		-3.5	20	V
V_{SW_USB}	V_{DP1} to GND, V_{DN1} to GND		-0.5	6.5	V
V_{SW_Audio}	V_L to GND, V_R to GND		-3.6	6.5	V
V_{SW_UART}	V_{DP2} to GND, V_{DN2} to GND		-3.6	6.5	V
$V_{V\_SBUx/GSBUx}$	V_{SBU1} to GND, V_{SBU2} to GND, V_{GSBU1} to GND, V_{GSBU2} to GND		-0.5	20	V
V_{VSBUx_H}	V_{SBU1_H} to GND, V_{SBU2_H} to GND		-0.5	6.5	V
$V_{I/O}$	SENSE, MIC to GND		-0.5	6.5	V
V_{CNTRL}	Control input voltage	SDA, SCL	-0.5	6.5	V
$V_{comparator}$	Comparator input and output	DET/CMPIN, INT/CMPOUT	-0.5	6.5	V
I_{SW_Audio}	Switch I/O current, audio path		-250	250	mA
I_{SW_USB}	Switch I/O current, USB path			100	mA
I_{SW_MIC}	Switch I/O current, MIC to SBU1 or SBU2			50	mA
I_{SW_SBUx}	Switch I/O current, SBUx to SBUx_H			50	mA
I_{SW_SENSE}	Switch I/O current, SENSE to GSBU1 or GSBU2			100	mA
I_{SW_AGND}	Switch I/O current, AGND to SBU1 or SBU2			500	mA
I_{IK}	DC input diode current		-50		mA
T_A	Absolute maximum operating temperature		-40	85	°C
T_{STG}	Storage temperature		-65	150	°C

3. Recommended Operating Conditions

Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. The ratings are obtained over an operating free-air temperature range unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply voltage	2.7		5.5	V
V_{SW_USB}	V_{DP} to GND, V_{DN} to GND, V_{DP_R} to GND, V_{DN_L} to GND	0		3.6	V
V_{SW_Audio}	V_{DP_R} to GND, V_{DN_L} to GND, V_L to GND, V_R to GND	−3.6		3.6	V
V_{VSBU_MIC}	V_{SBU1} to GND, V_{SBU2} to GND, V_{MIC} to GND	0		3.6	V
V_{VGSBU_SEN}	V_{GSBU1} to GND, V_{GSBU2} to GND, V_{SENSE} to GND	0		3.6	V
V_{VGSBU}	V_{SBU1} to GND, V_{SBU2} to GND, V_{SBU1_H} to GND, V_{SBU2_H} to GND	0		3.6	V
V_{CC_IN}	V_{CC_IN} to GND	0		5.5	V
V_{IH}	Input voltage high	0.825		V_{CC}	V
V_{IL}	Input voltage low			0.3	V
T_A	Ambient operating temperature	−40	25	85	°C

4. ESD Ratings

When a statically-charged person or object touches an electrostatic discharge sensitive device, the electrostatic charge might be drained through sensitive circuitry in the device. If the electrostatic discharge possesses sufficient energy, damage might occur to the device due to localized overheating.

Model	Metric	Value	Unit
Human-body model (HBM)	ANSI/ESDA/JEDEC JS-001	±5000	V
Charged device model (CDM)	ANSI/ESDA/JEDEC JS-002	±2000	V
Latch-up		200	mA

5. Electrical Characteristics

5.1. DC electrical characteristics

The values are obtained under these conditions unless otherwise specified: V_{CC} = 2.7 V to 5.5 V, V_{CC} = 3.3 V (Typ.), T_A = -40°C to 85°C, and T_A = 25°C (Typ.).

Symbol	Parameter	Conditions	Power	Min	Typ	Max	Unit
I_{CC}	Supply current	USB switches on, SBUx to SBUx_H switches on	V_{CC} = 4.2 V		65		μA
		Audio switches on, MIC switch on and Audio GND switch on			63		μA
I_{CCZ}	Standby current	04H'b7 = 0			4		μA
USB/Audio common pins: DP_R, DN_L							
I_{OZ}	Off leakage current of DP_R and DN_L	DN_L, DP_R = −3 V to 3.6 V	V_{CC} = 2.7 V to 5.5 V	-3		3	μA
I_{OFF}	Power−off leakage current of DP_R and DN_L	DN_L, DP_R = 0 V to 3.6 V	Power off	-3		3	μA
V_{OV_TRIP} (1)	Input OVP lockout	Rising edge, 0x12h bit [7:6] = 00	V_{CC} = 2.7 V to 5.5 V	4.2	4.4	4.6	V
V_{OV_HYS} (1)	Input OVP hysteresis				0.24		V
Audio switch							
I_{ON}	On leakage current of audio switch	DN_L, DP_R = −3 V to 3 V, DP, DN, R, L = Float	V_{CC} = 2.7 V to 5.5 V	-4		3	μA
I_{OFF}	Power−off leakage current of L and R	L, R = 0 V to 3 V, DP_R, DN_L = Float	Power off	-1		1	μA
R_{ON}	Switch on resistance	I_{SW} = 100 mA, V_{SW} = −3 V to 3 V	V_{CC} = 2.7 V to 5.5 V		1.2		Ω
R_{SHUNT}	Pull-down resistor on R/L pin when audio switch is off	L= R = 3 V		6	10	14	kΩ
USB switch							
I_{ON}	On leakage current of USB switch	DN_L, DP_R = 0 V to 3.6 V, DP1, DN1, R, L = Float	V_{CC} = 2.7 V to 5.5 V	-3		3	μA

I_{OZ}	Off leakage current of DP and DN	DP_R to DP1, DN_L to DN1 = 0 V to 3.6 V		-3		3	μA
I_{OFF}	Power−off leakage current of DP and DN	DP_R to DP1, DN_L to DN1 = 0 V to 3.6 V	Power off	-3		3	μA
R_{ON_USB}	USB switch on resistance	I_{SW} = 8 mA, V_{SW} = 0.4 V	V_{CC} = 2.7 V to 5.5 V		4.6		Ω
UART switch							
I_{OZ}	Off leakage current of DP and DN	DP_R to DP2, DN_L to DN2 = 0 V to 3.6 V		-3		3	μA
I_{OFF}	Power−off leakage current of DP and DN	DP_R to DP2, DN_L to DN2 = 0 V to 3.6 V	Power off	-3		3	μA
R_{ON_UART}	UART switch on resistance	I_{SW} = 3 mA, V_{SW} = 0.4 V	V_{CC} = 2.7 V to 5.5 V		10		Ω
I_{ON}	On leakage current UART switch	DN_L, DP_R = 0 V to 3.6 V, DP2, DN2, R, L = Float	V_{CC} = 2.7 V to 5.5 V		1.6		μA
SENSE-AGND switch							
R_{ON}	SENSE switch on resistance	I_{OUT} = 100 mA, V_{SW} = 1.0 V	V_{CC} = 2.7 V to 5.5 V		8		Ω
SENSE switch							
I_{ON}	SENSE path leakage current	GSBUx = 0 V to 1 V, SENSE is floating	V_{CC} = 2.7 V to 5.5 V	-2		2	μA
R_{ON}	SENSE switch on resistance	I_{OUT} = 100 mA, V_{SW} = 1.0 V	V_{CC} = 2.7 V to 5.5 V		330		mΩ
I_{OFF}	Power−off leakage current of SENSE	GSBUx to SENSE = 0 V to 1.0 V	V_{CC} = 2.7 V to 5.5 V	-2		2	μA
	Power−off leakage current of GSBUx	GSBUx = 0 V to 3.6 V		-3		3	μA
V_{OV_TRIP} (1)	Input OVP lockout on GSBUx	Rising edge, 0x12h bit [7:6] = 00	V_{CC} = 2.7 V to 5.5 V	4.2	4.4	4.6	V
V_{OV_HYS} (1)	Input OVP hysteresis of GSBUx				0.24		V
SBUx pins							
I_{OZ}	Off leakage current of SBUx	SBUx = 0 V to 3.6 V	V_{CC} = 2.7 V to 5.5 V	-3		3	μA

I_{OFF}	Power−off leakage current port SBUx	SBUx = 0 V to 3.6 V	Power off	-2		10	μA
V_{OV_TRIP} (1)	Input OVP lockout	Rising edge, 0x12h bit [7:6] = 00	V_{CC} = 2.7 V to 5.5 V	4.2	4.4	4.6	V
V_{OV_HYS} (1)	Input OVP hysteresis				0.24		V
MIC switch							
I_{ON}	On leakage current of MIC switch	SBUx = 0 V to 3.6 V, MIC is floating	V_{CC} = 2.7 V to 5.5 V	-3		3	μA
I_{OZ}	Off leakage current of MIC	MIC = 0 V to 3.6 V		-1		1	μA
I_{OFF}	Power-off leakage current of MIC	MIC = 0 V to 3.6 V	Power off	-1		1	μA
R_{ON}	MIC switch on resistance	V_{SW} = 3.6 V, I_{SW} = 30 mA	V_{CC} = 2.7 V to 5.5 V		3.1		Ω
SBUx_H switch							
I_{ON}	On leakage current of SBUx_H switch	SBUx = 0 V to 3.6 V, SBUx_H is floating	V_{CC} = 2.7 V to 5.5 V	-3		3	μA
I_{OZ}	Off leakage of SBUx_H	SBUx_H = 0 V to 3.6 V		-1		1	μA
I_{OFF}	Power off leakage current of SBUx_H	SBUx_H = 0 V to 3.6 V	Power off	-1		1	μA
R_{ON}	SBUx_H switch on resistance	V_{SW} = 0 V to 3.6 V, I_{SW} = 30 mA	V_{CC} = 2.7 V to 5.5 V		2.8		Ω
Audio ground switch pin: AGND to SBUx							
R_{ON}	AGND switch on resistance	I_{SOURCE} = 100 mA on SBUx	V_{CC} = 2.7 V to 5.5 V		66		mΩ
CC_IN pin							
V_{TH_L}	Input low threshold		V_{CC} = 2.7 V to 5.5 V		1.2		V
V_{TH_H}	Input high threshold				1.5		V
I_{IN}	Input leakage of CC_IN	CC_IN = 0 V to 5.5 V				1.0	μA
SDS, SCL pins							
V_{ILI2C}	Low−level input voltage		V_{CC} = 2.7 V to 5.5 V			0.3	V

V_{IHI2C}	High−level input voltage			0.825			V
I_{I2C}	Input current of SDA and SCL pins	SCL/SDA = 0 V to 3.6 V		-5		5	μA
V_{OLSDA}	Low−level output voltage	I_{OL} = 2 mA				0.3	V
I_{OLSDA}	Low−level output current	V_{OLSDA} = 0.2 V		10			mA

Note:

(1) The OVP voltage can be adjusted by bit [7:6] for 12h: 4.4 V, 4.6 V, 4.8 V, 5 V.

(2) Specificatons subject to change without notice.

5.2. AC electrical characteristics

The values are obtained under these conditions unless otherwise specified: V_{CC} = 2.7 V to 5.5 V, V_{CC} (Typ.) = 3.3 V, T_A = -40°C to 85°C, and T_A (Typ.) = 25°C.

Symbol	Parameter	Conditions	Power	Min	Typ	Max	Unit
Audio switch							
t_{delay}	Audio switch turn-on delay time	DP_R = DN_L = 1 V, R_L = 32 Ω	V_{CC} = 3.3 V		20		μs
t_{rise}	Audio switch turn-on rising time	DP_R = DN_L = 1 V, R_L = 32 Ω			60		μs
t_{OFF}	Audio switch turn-off time	DP_R = DN_L = 1 V, R_L = 32 Ω	V_{CC} = 3.3 V		2		μs
X_{TALK}	Cross talk (adjacent)	f = 1 kHz, R_L = 50 Ω, V_{SW} = 1 V_{RMS}			-90		dB
BW	−3 dB bandwidth	R_L = 50 Ω			940		MHz
O_{IRR}	Off isolation	f = 1 kHz, R_L = 50 Ω, C_L = 0 pF, V_{SW} = 1 V_{RMS}			-110		dB
THD+N	Total harmonic distortion + noise performance with A−weighting filter	R_L = 600 Ω, f = 20 Hz ~ 20 kHz, V_{SW} = 2 V_{RMS}			-110		dB
		R_L = 32 Ω, f = 20 Hz ~ 20 kHz, V_{SW} = 1 V_{RMS}			-110		dB
		R_L = 16 Ω, f = 20 Hz ~ 20 kHz, V_{SW} = 0.5 V_{RMS}			-108		dB
USB switch							
t_{ON} (1)	USB switch turn−on time	DP_R = DN_L = 1.5 V, R_L = 50 Ω	V_{CC} = 3.3 V		32		μs

t_{OFF}	USB switch turn−off time	DP_R = DN_L = 1.5 V, R_L = 50 Ω			2		μs
BW	−3 dB bandwidth	R_L = 50 Ω			1.05		GHz
O_{IRR}	Off isolation between DP, DN and common node pins	f = 1 kHz, R_L = 50 Ω, C_L = 0 pF, V_{SW} = 1 V_{RMS}			-110		dB
t_{OVP}	DP_R and DN_L pins OVP response time	V_{SW} = 3.5 V to 5.5 V			0.4		μs
UART switch							
BW	−3 dB bandwidth	R_L = 50 Ω	V_{CC} = 3.3 V		800		MHz
MIC / Audio ground switch							
t_{delay_MIC}	MIC switch turn-on delay time	SBUx = 1 V, R_L = 50 Ω	V_{CC} = 3.3 V		70		μs
t_{rise_MIC}	MIC switch turn-on rising time				120		
t_{delay_AGND}	AGND switch turn-on time	SBUx pulled to 0.5 V by 16 Ω, AGND connect to GND			1.6		ms
t_{rise_AGND}	AGND switch turn-on rising time				1		ms
t_{OFF_MIC}	MIC switch turn-off time	SBUx = 2.5 V, R_L = 50 Ω			2		μs
$t_{OFF\_Audio\ GND}$	AGND switch turn-off time	SBUx: I_{SOURCE} = 10 mA, clamp to 2.5 V			50		μs
BW	MIC switch bandwidth	R_L = 50 Ω			52		MHz
SBUx_H switch							
t_{ON}	SBUx_H switch turn-on time	SBUx = 2.5 V, R_L = 50 Ω	V_{CC} = 3.3 V		45		μs
t_{OFF}	SBUx_H switch turn-off time				2		μs
BW	Bandwidth	R_L = 50 Ω			45		MHz
t_{OVP}	SBUx pins OVP response time	V_{SW} = 3.5 V to 5.5 V			0.4		μs

Note:

(1) The Turn-on timing can be adjusted by the I^2C register.

(2) Specifications subject to change without notice.

5.3. Comparator electrical characteristics

The values are obtained under these conditions unless otherwise specified: T_A = 25°C, V_{CC} = 2.7 V to 5 V, C_L = 15 pF.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Offset voltage						
V_{REF}	Reference voltage	T_A = 25°C to 65°C	218.5	225	231.5	mV
V_{HYS}	Hysteresis			30	40	mV
dV_{OS}/dT	Input offset voltage drift	T_A = -40°C to 85°C			±70	μV/°C
Input voltage range						
V_{CM}	Common-mode voltage range	T_A = -40°C to 85°C	-0.1		V_{CC} + 0.1	V
Input bias current (1)						
I_B	Input bias current	T_A = 25°C		30	100	pA
		T_A = -40°C to 85°C			20	nA
I_{OS}	Input offset current			8		pA
C_{LOAD}	Capacitive load drive			60		pF
Output type		Open-drain				

Note:

(1) Guaranteed by design.

(2) Specifications subject to change without notice.

5.4. Capacitance

The values are obtained under these conditions unless otherwise specified: V_{CC} (Typ.) = 3.3 V, T_A = -40°C to 85°C, and T_A (Typ.) = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{ON\_USB/Audio}$(1)	On capacitance (common port)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias		8		pF
$C_{OFF\_USB/Audio}$ (1)	Off capacitance (common port)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias		6.5		pF
C_{OFF_USB} (1)	Off capacitance (non−common ports)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias		2.6		pF
$C_{ON\_SENSE\_SW}$(1)	On capacitance (common ports)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias		55		pF
$C_{OFF\_SENSE\_SW}$(1)	Off capacitance (common ports)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias		88		pF
$C_{ON\_MIC\_SW}$(1)	On capacitance (common ports)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias		170		pF

$C_{OFF\_MIC\_SW}$(1)	Off capacitance (common ports)	f = 1 MHz, 100 mV_{PK-PK}, 100 mV DC bias		10		pF
$C_{ON\_AGND\_SW}$(1)	On capacitance (common port)	f = 1 MHz, 100 mV_{PK-PK}, 100mV DC bias		125		pF
$C_{ON\_SBUx\_H\_SW}$(1)	On capacitance (common port)	f = 1 MHz, 100 mV_{PK-PK},100 mV DC bias		160		pF

Note:

(1) Guaranteed by design.

(2) Specifications subject to change without notice.

5.5. I²C specification

The values are obtained under these conditions unless otherwise specified: V_{CC} = 2.7 V to 5.5 V, V_{CC} = 3.3 V (Typ.), T_A = -40°C to 85°C, and T_A (Typ.) = 25°C.

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	I²C_SCL clock frequency			400	kHz
$t_{HD;\ STA}$	Hold time (repeated) START condition	0.6			μs
t_{LOW}	Low period of I²C_SCL clock	1.3			μs
t_{HIGH}	High period of I²C_SCL clock	0.6			μs
$t_{SU;\ STA}$	Set−up time for repeated START condition	0.6			μs
$t_{HD;\ DAT}$ (1)	Data hold time	0		0.9	μs
$t_{SU;\ DAT}$ (2)	Data set−up time	100			ns
t_r (2)	Rising time of I²C_SDA and I²C_SCL signals	20 + 0.1 C_b		300	ns
t_f (2)	Falling time of I²C_SDA and I²C_SCL signals	20 + 0.1 C_b		300	ns
$t_{SU;\ STO}$	Set−up time for STOP condition	0.6			μs
t_{BUF}	Bus−free time between STOP and START conditions	1.3			μs
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	0		50	ns

Note:

(1) Guaranteed by characterization. Not production tested.

(2) A fast−mode I²C−bus device can be used in a standard−mode I²C−bus system, but the requirement $t_{SU;DAT}$ ≥ ±250 ns must be met. This is automatically the case if the device does not stretch the LOW period of the I²C_SCL signal. If such a device does stretch the LOW period of the I²C_SCL signal, it must output the next data bit to the I²C_SDA line t_{r_max} + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the standard-mode I²C bus specification) before the I²C_SCL line is released.

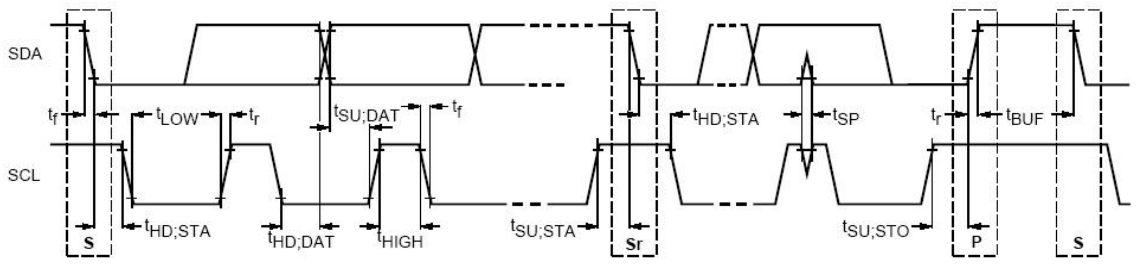
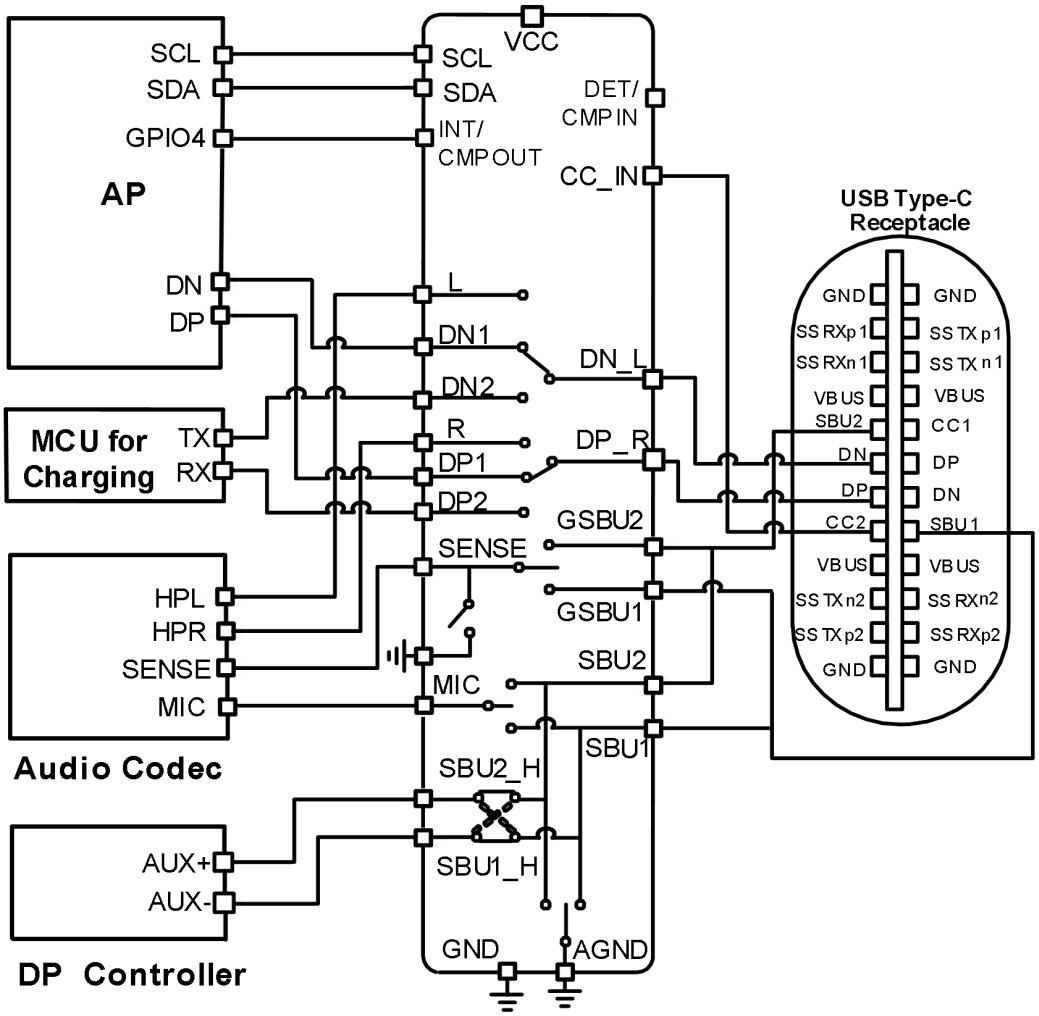


Figure 1. Definition of timing for full−speed mode devices on the I²C bus

6. Block Diagram



7. Application Information

Important notice: Validation and testing are the most reliable ways to confirm system functionality. The application information is not part of the specification and is for reference purposes only.

7.1. Overvoltage protection

The DIO4485/DIO4485B features an overvoltage protection (OVP) on receptacle side pins that turns off the internal signal routing path if the voltage exceeds the OVP threshold. If an OVP is occurred, flag register 0x02h and 0x03h will indicate which pin had the OVP event. OVP threshold voltage is configurable by 0x12h, bit [7:6].

7.2. Watchdog timer

The function of watchdog is to continuously monitor I^2C communication. A timer will start as long as the watchdog is enabled. The watchdog receives either read or write command from the master to be reset with I^2C communication.

In case there's no I^2C communication detected after the timer counting down to zero, DIO4485/DIO4485B will control Register 0x04h, 0x05h and 0x12h bit[1] to their default value by transmitting an interrupt and reset switch setting and moisture detection enable/disable signals. Watchdog timer can be programmed through Register 0x20h.

7.3. Headset detection

The DIO4485/DIO4485B integrates headset unplug detection function by detecting the CC_IN voltage. The function will be active when device is enabled. Register 0x11h,bit [1:0] Output can indicate if CC_IN is low (CC_IN < 1.2 V) or high (CC_IN > 1.5 V).

	0x11h, bit [1]	0x11h, bit [0]
CC_IN < 1.2 V	0	1
CC_IN > 1.5 V	1	0

7.4. MIC switch auto−off function

The function is active during control bit 0x12h bit [2] = 1. When CC_IN is changed from low to high, and L, R, and AGND switches are on, the MIC switch will be off and receptacle side pin will be pulled to ground for 50 μs first. Then it shows high−Z status under MIC switch is set on status.

7.5. Audio jack detection and configuration

The function is active when control bit 0x12h bit [0] = 1. When the headset is inserted, the DIO4485 / DIO4485B can detect OMTP, CTIA or 3-pole headset and configurate pinout automatically. During detection and configuration, the R, L, Sense, MIC and Audio ground switches will be off. After detection and configuration, R, L, MIC, Sense and AGND switches will turn on according to detection results and timing control setting.

7.6. I²C interface

The DIO4485 / DIO4485B includes a full I²C slave controller. The I²C slave fully complies with the I²C specification version 2.1 requirements. This block is designed for fast mode, 400 kHz, signals. Examples of an I²C write and read sequence are shown in below figures respectively.

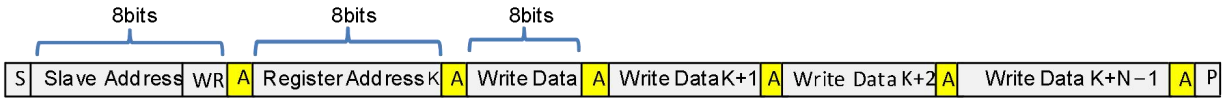


Figure 2. I²C write example

Note: Single-byte read is initiated by the master with P immediately following the first data byte.

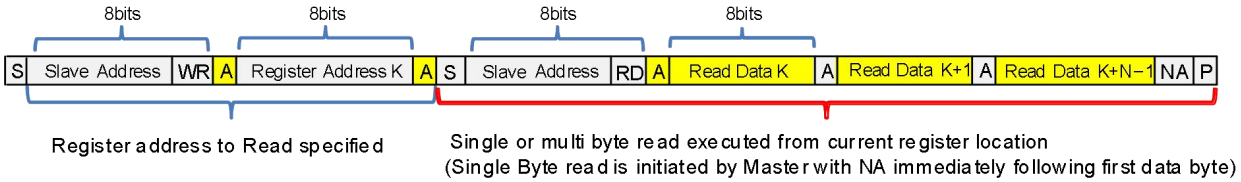


Figure 3. I²C read example

Note: If the register is not specified, the master will begin reading from the current register. In this case only sequence showing in the red bracket is needed

7.7. Moisture detection

The DIO4485 / DIO4485B can detect moisture in type-C connector. When moisture detection is enabled, all the related channels will be closed. The voltage can be measured from the selected pin with current source enabled or disabled according to 0×13h bit [3]. Leakage between the selected pins and GND/VBUS can be detected by comparing the measured results with pre-set thresholds, and it will pull down 'INT', when moisture is found. The related channels will be recovered when the pin detection is completed.

An internal current source will be applied to the pin first during detection of the leakage between GND and pin CC_IN, DP_R, DN_L, SBU1 or SBU2. After getting the result reflecting the resistance from this pin to GND, the result will be stored to corresponding register.

The voltage from the pin without current source will be measured during detection of the leakage between VBUS and pin CC_IN, DP_R, DN_L, SBU1 or SBU2. For the leakage from VBUS and the voltage drop from this pin to ground, they will be detected by the measurement when the moisture detection is performed. The moisture detection has single-pin mode and multi-pin mode.

7.7.1. Single-pin mode

In single-pin mode, the moisture detection result would be stored separately in register 0×14h (with current source enabled) or 0×30h (with current source disabled).

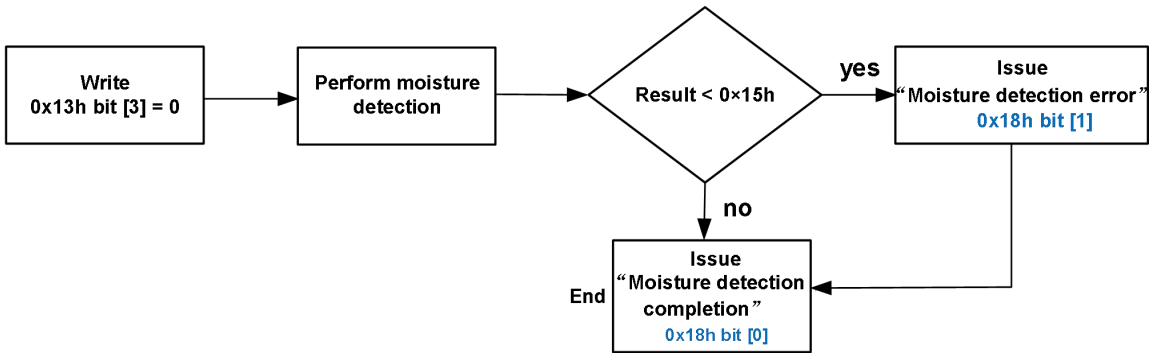


Figure 4. Single-pin mode (with current source enabled)

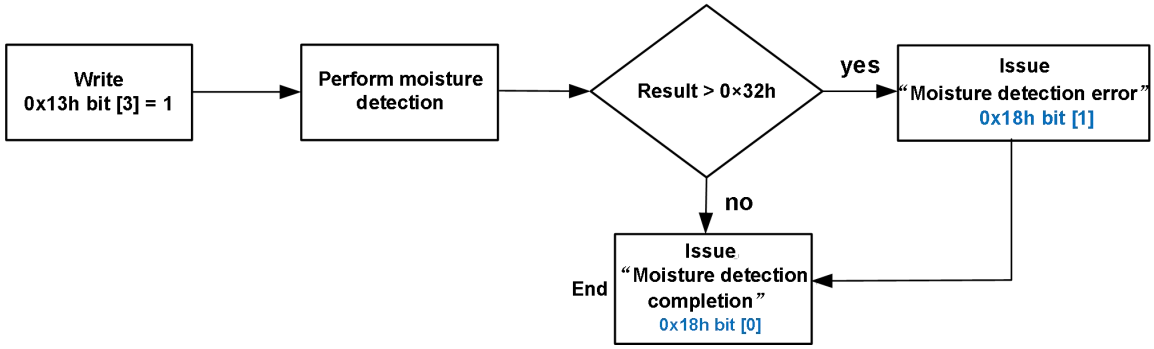


Figure 5. Single-pin mode (with current source disabled)

7.7.2. Multi-pin mode

In multi-pin mode, if all pins are selected, the turn of moisture detecting sequence will be CC_IN, DP_R, DN_L, SBU1, SBU2. In case some pins are not selected, the detection will ignore the unselected pins and performed on the next selected pins. For example, if the pin CC_IN, DP_L are not selected, the moisture detection will be performed on DP_R first, then SBU1 and SBU2 in turn.

As soon as the detection starts, whether the setup of the current source or pin selection would be ignored. And all the related channels would be forced off during the whole round detection (from the 1st pin to the last pin). The related channels will be recovered after the detection for all pins are completed.

If moisture error is detected in some pins (result > 0×32h for detection with current source disabled , or the result < 0×15h with current source enabled), DIO4485 / 4485B will complete the whole round, and then stop moisture detection and indicate the flag of “Moisture detection completion”.

0×31h bit [5] will select the blank time between two adjacent detections.

It’s shown in figure 6, figure 7 as below.

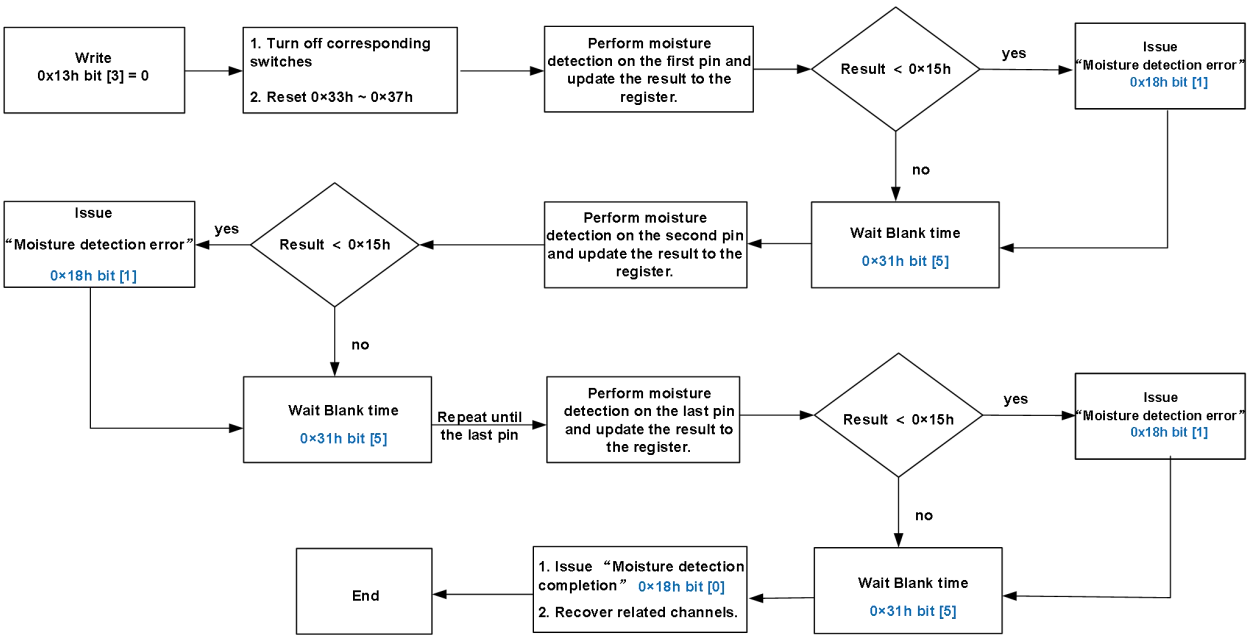


Figure 6. Multi-pin mode (with current source enabled)

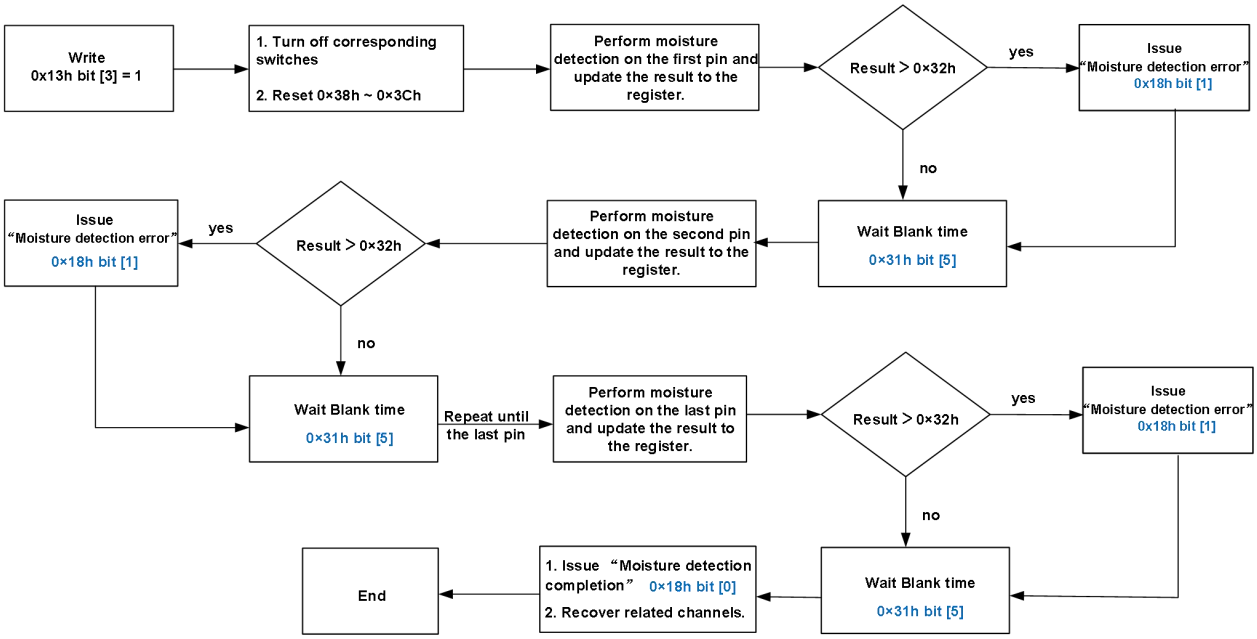


Figure 7. Multi-pin mode (with current source disabled)

7.7.3. Polling

With 0×16h bit [1:0] = 1, DIO4485 / 4485B can also repeatedly perform moisture detection on its own. A list of scenarios with the combination set of 0×16h bit [1:0] is shown as below.

In single-pin mode, when there's no moisture detected (result <= 0×32h for detection with current source disabled, or result >= 0×15h with current source enabled), the moisture detection will be restarted after a period set by 0×16h bit [1:0].

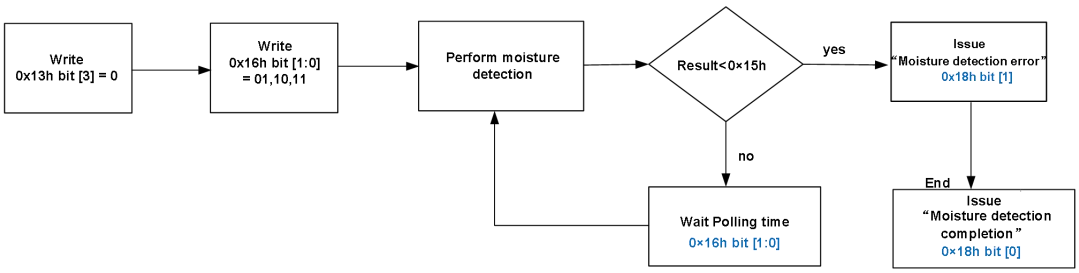


Figure 8. Single-pin polling mode (with current source enabled)

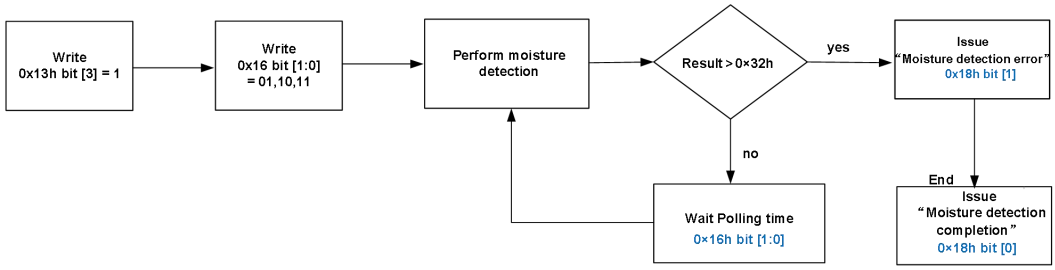


Figure 9. Single-pin polling mode (with current source disabled)

In multi-pin mode, when the measured result is ok after one round detection for selected pins, a new round will be restart after the period set by Polling time.

In the polling period, any attempt of changing the setup of current source or selecting the pins will be noticed in preparation of the next new round.

During the detection, all the related channels will be closed as soon as the first pin detection starts and the channels will not be recover until the last pin detection finishes, which means this round detection is completed. To exit polling immediately, there are two situations: one situation is writing 0×13h bit [7] = 1, the other one is an OVP event detected.

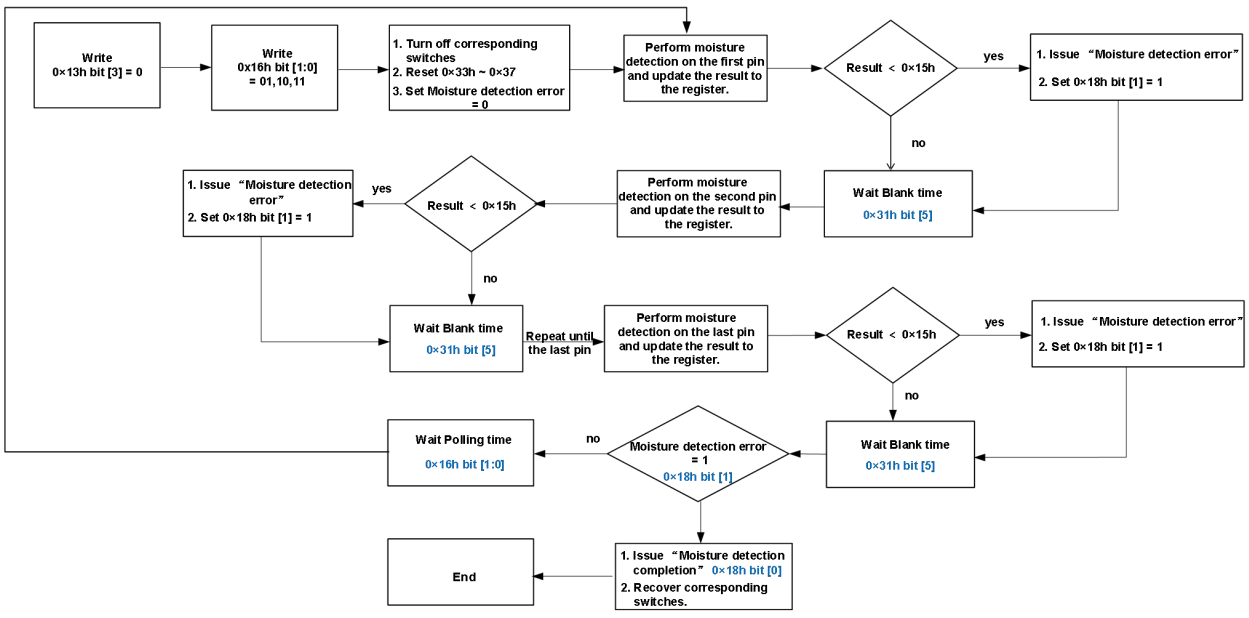


Figure 10. Multi-pin polling mode (with current source enabled)

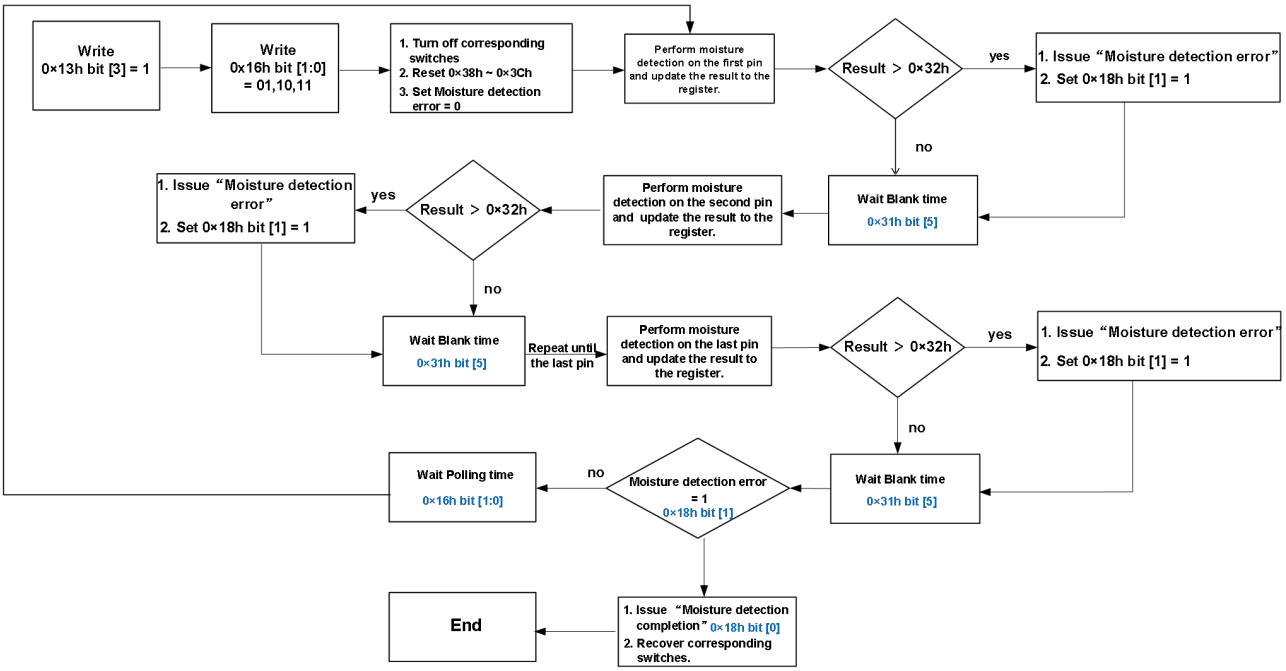


Figure 11. Multi-pin polling mode (with current source disabled)

8. Register Maps

ADDR	Register Name	Type	Reset Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00H	Device ID	R	0XF6	1	1	1	1	0	1	0	1
02H	OVP interrupt flag	R/C	0x00	Reserved	Reserved	OVP/ DP_R	OVP/ DN_L	OVP/ SBU1,SBU2		OVP/ GSBU1	OVP/ GSBU2
03H	OVP status	R	0x00	Reserved [7:6]		OVP/ DP_R	OVP/ DN_L	OVP/ SBU1, SBU2 [3:2]		OVP/ GSBU1	OVP/ GSBU2
04H	Switch settings enable	R/W	4485: 0xF8 4485B: 0x98	Device enable	SBU1_H to SBUx switches	SBU2_H to SBUx switches	DN_L to DN or L switches	DP_R to DP or R switches	Sense to GSBUx switches	MIC to SBUx switches	AGND to SBUx switches
05H	Switch select	R/W	0x18	USB2 switch select	SBU1_H switches	SBU2_H switches	DN_L to DN1 or L switches	DP_R to DP1 or R switches	Sense to GSBUx switches	MIC to SBUx switches	AGND to SBUx switches
06H	Switch status0	R	0x05	Reserved [7:6]		Sense switch status [5:4]		DP_R switch status [3:2]		DN_L switch status [1:0]	
07H	Switch status1	R	4485: 0x23 4485B: 0x00	Reserved [7:6]		SBU2 switch status [5:3]			SBU1 switch status [2:0]		
08H	Audio switch left channel turn-on control	R/W	0x01	Audio switch left channel slow control							
09H	Audio switch right channel turn-on control	R/W	0x01	Audio switch right channel slow control							
0AH	MIC switch turn-on control	R/W	0x01	MIC switch slow control							
0BH	Sense switch turn-on control	R/W	0x01	Sense switch slow control							
0CH	Audio ground switch turn-on control	R/W	0x01	Audio ground switch slow control							
0DH	Timing delay between R switch enable and switch on order	R/W	0x00	Timing delay between R switch enable and switch on order control							

0EH	Timing delay between MIC switch enable and switch on order	R/W	0x00	Timing delay between MIC switch enable and switch on order control						
0FH	Timing delay between Sense switch enable and switch on order	R/W	0x00	Timing delay between sense switch enable and switch on order control						
10H	Timing delay between Audio ground switch enable and switch on order	R/W	0x00	Timing delay between audio ground switch enable and switch on order control						
11H	Audio accessory status	R	0x01	Reserved [7:2]					CC_IN	Reserved
12H	Function enable	R/W	0x00	OVP threshold voltage configuration [7:6]	Current source for resistance detection	Role of Pin C2 and C3	Slow turn on control enable	MIC auto break out control enable	Moisture detection enable	Audio jack detection and configurati -on enable
13H	Detection control0	R/W	0x00	Moisture detection force off control	Reserved [6:4]			Current source for moisture detection	Select the pin for moisture detection in single-pin mode [2:0]	
14H	Single-pin mode resistor detection results	R	0×FF	Moisture detection result in single-pin mode with current source enabled						
15H	Moisture resistor detection threshold	R/W	0×16	Threshold moisture detection with current source enabled						
16H	Function control1	R/W	0x00	Reserved [7:3]				Select moisture detection mode	Set the time span between two moisture detections [1:0]	
17H	MIC detection status	R	0x01	Reserved [7:4]			4 pole	4 pole	3 pole	No audio

18H	System flag	R/C	0x00	Reserved [7:4]	Watchdog timeout	Audio jack detection & Configur -ation	Moisture detection error	Detection completion
19H	System mask	R/W	0×00	Reserved [7:4]	Watchdog timeout	Audio jack detection and configura -tion	Moisture detection error mask	Moisture detection completion mask
1CH	MIC detection threshold data0	R/W	0x20	MIC detection threshold data0				
1DH	MIC detection threshold data1	R/W	0xFF	MIC detection threshold data1				
1EH	I^2C reset	W/C	0x00	Reserved [7:1]				I^2C reset
1FH	Bias current setting	R/W	0x07	Reserved [7:3]			Bias current setting [2:0]	
20H	Watchdog setting	R/W	0x03	Watchdog enable	Reserved [6:3]		Watchdog timer [2:0]	
21H	Timing delay setting	R/W	0x00	Timing delay between L switch enable and switch on order				
30H	Detection data1	R	0x00	Moisture detection result in single-pin mode with current source disabled				
31H	Detection control1	R/W	0x00	Reserved [7:6]	Multi-pin mode moisture detection blank time	Select pin (CC_IN)	Select pin (DP_R)	Select pin (DN_L)	Select pin (SBU1)	Select pin (SBU2)
32H	Moisture voltage detection threshold	R/W	0x00	Threshold for moisture detection with current source disabled				
33H	Multi-pin mode resistor detection result of CC_IN	R	0xFF	Moisture detection result in multi-pin mode with current source enabled				
34H	Multi-pin mode resistor detection result of DP_R	R	0xFF	Moisture detection result in multi-pin mode with current source enabled				

35H	Multi-pin mode resistor detection result of DN_L	R	0xFF	Moisture detection result in multi-pin mode with current source enabled
36H	Multi-pin mode resistor detection result of SBU1	R	0xFF	Moisture detection result in multi-pin mode with current source enabled
37H	Multi-pin mode resistor detection result of SBU2	R	0xFF	Moisture detection result in multi-pin mode with current source enabled
38H	Multi-pin mode voltage detection result of CC_IN	R	0x00	Moisture detection result in multi-pin mode with current source disabled
39H	Multi-pin mode voltage detection result of DP_R	R	0x00	Moisture detection result in multi-pin mode with current source disabled
3A	Multi-pin mode voltage detection result of DN_L	R	0x00	Moisture detection result in multi-pin mode with current source disabled
3B	Multi-pin mode voltage detection result of SBU1	R	0x00	Moisture detection result in multi-pin mode with current source disabled
3C	Multi-pin mode voltage detection result of SBU2	R	0x00	Moisture detection result in multi-pin mode with current source disabled

8.1. I²C slave address

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1	0	0	0	0	1	0	R/W

8.2. Register definition

8.2.1. Device ID

Address: 00h

Reset Value: 8'b 1111_0110

Type: Read

Bits	Name	Size	Description
[7:6]	Vendor ID	2	Vendor ID
[5:3]	Version ID	3	Device version ID
[2:0]	Revision ID	3	Revision history ID

8.2.2. OVP interrupt flag

Address: 02h

Reset Value: 8'b 0000_0000

Type: Read Clear

Bits	Name	Size	Description
[7:6]	Reserved	2	Do not use
5	DP_R OVP	1	0: OVP event has not occurred 1: OVP event has occurred
4	DN_L OVP	1	0: OVP event has not occurred 1: OVP event has occurred
[3:2]	SBU1 || SBU2 OVP	2	0: OVP event has not occurred 1: At least one of SBU1 or SBU2 OVP event has occurred
1	GSBU1 OVP	1	0: OVP event has not occurred 1: OVP event has occurred
0	GSBU2 OVP	1	0: OVP event has not occurred 1: OVP event has occurred

8.2.3. OVP status

Address: 03h

Reset Value: 8'b 0000_0000

Type: Read

Bits	Name	Size	Description
[7:6]	Reserved	2	Do not use
5	OVP on DP_R PIN	1	0: OVP event has not occurred 1: OVP event has occurred
4	OVP on DN_L PIN	1	0: OVP event has not occurred 1: OVP event has occurred

[3:2]	SBU1 || SBU2 OVP	2	0: OVP event has not occurred 1: At least one of SBU1 or SBU2 OVP event has occurred
1	OVP on GSBU1 PIN	1	0: OVP event has not occurred 1: OVP event has occurred
0	OVP on GSBU2 PIN	1	0: OVP event has not occurred 1: OVP event has occurred

8.2.4. Switching setting enable

Address: 04h

Reset Value: DIO4485: 8’ b 1111_1000

DIO4485B: 8’b 1001_1000

Type: Read/Write

Bits	Name	Size	Description
7	Device enable	1	1: Device enable. 0: Device disable; L, R pull down by 10 kΩ and other switch nodes will be high−Z for positive input.
6	SBU1_H to SBUx switches	1	0: Switch disable; SBU1_H will be high−Z for positive input 1: Switch enable
5	SBU2_H to SBUx switches	1	0: Switch disable; SBU2_H will be high−Z for positive input 1: Switch enable
4	DN_L to DN1/2 or L switches	1	0: Switch disable; DN_L, DN1/2 will be high−Z for positive input. L pull down by 10 kΩ 1: Switch enable
3	DP_R to DP1/2 or R switches	1	0: Switch disable; DP_R, DP1/2 will be high−Z for positive input. R pull down by 10 kΩ 1: Switch enable
2	Sense to GSBUx switches	1	0: Switch disable; Sense, GSBU1 and GSBU2 will be high−Z for positive input 1: Switch enable
1	MIC to SBUx switches	1	0: Switch disable: MIC will be high−Z for positive input. 1: Switch enable
0	AGND to SBUx switches	1	0: Switch disable: AGND will be high−Z for positive input. 1: Switch enable

8.2.5. Switch select

Address: 05h

Reset Value: 8’b 0001_1000

Type: Read/Write

Bits	Name	Size	Description
7	USB2 switch select	1	0: USB2 off. USB1 or Audio switch depend on 05h, bit [4:3] and 04h,bit [4:3] 1: DP/R~DP2, DN/L~DN2 switches ON, if 04h, bit [4:3] = ‘11’ and 05h, bit [4:3] = ‘11’

6	SBU1_H switches	1	0: SBU1_H to SBU1 switch ON 1: SBU1_H to SBU2 switch ON
5	SBU2_H switches	1	0: SBU2_H to SBU2 switch ON 1: SBU2_H to SBU1 switch ON
4	DN_L to DN1 or L switches	1	0: DN_L to L switch ON 1: DN_L to DN1 switch ON
3	DP_R to DP1 or R switches	1	0: DP_R to R switch ON 1: DP_R to DP1 switch ON
2	Sense to GSBUx switches	1	0: Sense to GSBU1 switch ON 1: Sense to GSBU2 switch ON
1	MIC to SBUx switches	1	0: MIC to SBU2 switch ON 1: MIC to SBU1 switch ON
0	AGND to SBUx switches	1	0: AGND to SBU1 switch ON 1: AGND to SBU2 switch ON

Note: If want to change to USB2 mode, you must first write 0x05h = 0x98h, then write 0x04h = 0x98h

8.2.6. Switch status0

Address: 06h

Reset Value: 8'b 0000_0101

Type: Read

Bits	Name	Size	Description
[7:6]	Reserved	2	Do not use
[5:2]	Sense switch status	2	00: Sense switch is Open / Not Connected 01: Sense connected to GSBU1 10: Sense connected to GSBU2 11: Not valid
[3:2]	DP_R switch status	2	00: DP_R Switch Open / Not Connected 01: DP_R connected to DP1 10: DP_R connected to R 11: DP_R connected to DP2
[1:0]	DN_L switch status	2	00: DN_L Switch Open / Not Connected 01: DN_L connected to DN1 10: DN_L connected to L 11: DN_L connected to DN2

8.2.7. Switch status1

Address: 07h

Reset Value: DIO4485: 8’b 0010_0011

DIO4485B: 8’b 0000_0000

Type: Read

Bits	Name	Size	Description
[7:6]	Reserved	2	Do not use
[5:3]	SBU2 switch status	3	000: SBU2 switch is Open / Not Connected 001: SBU2 connected to MIC 010: SBU2 connected to AGND 011: SBU2 connected to SBU1_H 100: SBU2 connected to SBU2_H 101: SBU2 connected both SBU1_H and SBU2_H 110…111: Do not use
[2:0]	SBU1 switch status	3	000: SBU1 switch is Open / Not Connected 001: SBU1 connected to MIC 010: SBU1 connected to AGND 011: SBU1 connected to SBU1_H 100: SBU1 connected to SBU2_H 101: SBU1 connected both SBU1_H and SBU2_H 110…111: Do not use

8.2.8. Audio switch left channel slow turn-on

Address: 08h

Reset Value: 8’b 0000_0001

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Switch turn on rising time setting	8	11111111: 25600 μs
			…
			00000001: 200 μs
			00000000: 100 μs

8.2.9. Audio switch right channel slow turn-on

Address: 09h

Reset Value: 8’b 0000_0001

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Switch turn on rising time setting	8	11111111: 25600 μs
			…
			00000001: 200 μs
			00000000: 100 μs

8.2.10. MIC switch slow turn-on

Address: 0Ah

Reset Value: 8'b 0000_0001

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Switch turn on rising time setting	8	11111111: 25700 μs
			…
			00000010: 350 μs
			00000001: 250 μs
			00000000: not valid

8.2.11. Sense switch slow turn-on

Address: 0Bh

Reset Value: 8'b 0000_0001

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Switch turn-on rising time setting	8	11111111: 25600 μs
			…
			00000001: 200 μs
			00000000: 100 μs

8.2.12. Audio ground switch slow turn-on

Address: 0Ch

Reset Value: 8'b 0000_0001

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Switch turn-on rising time setting	8	11111111: 179000 μs
			…
			00000001: 1400 μs
			00000000: 700 μs

8.2.13. Timing delay between R switch enable and switch on order

Address: 0Dh

Reset Value: 8'b 0000_0000

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Delay timing setting	8	11111111: 102 ms
			11111110: 101.6 ms
			…
			00000001: 400 μs
			00000000: 0 μs

8.2.14. Timing delay between MIC switch enable and switch on order

Address: 0Eh

Reset Value: 8'b 0000_0000

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Delay timing setting	8	11111111: 102 ms
			11111110: 101.6 μs
			…
			00000001: 400 μs
			00000000: 0 μs

8.2.15. Timing delay between sense switch enable and switch on order

Address: 0Fh

Reset Value: 8'b 0000_0000

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Delay timing setting	8	11111111: 102 ms
			11111110: 101.6 ms
			…
			00000001: 400 μs
			00000000: 0 μs

8.2.16. Timing delay between audio ground switch enable and switch on order

Address: 10h

Reset Value: 8'b 0000_0000

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Delay timing setting	8	11111111: 102 ms
			11111110: 101.6 ms
			…
			00000001: 400 μs
			00000000: 0 μs

8.2.17. Audio accessory status

Address: 11h

Reset Value: 8'b 0000_0001

Type: Read

Bits	Name	Size	Description
[7:2]	Reserved	6	Do not use
1	CC_IN	1	0: CC_IN < 1.2 V 1: CC_IN > 1.5 V
0	Reserved	1	Do not use

8.2.18. Function enable

Address: 12h

Reset Value: 8'b 0000_0000

Type: Read/Write

Bits	Name	Size	Description
[7:6]	OVP threshold voltage configuration	2	00: 4.4 V 01: 4.6 V 10: 4.8 V 11: 5.0 V
5	Current source for resistance detection	1	If 0×13h bit [3] = 0. 0: 4.5 μA 1: 0.9 μA
4	Role of pin C2 and C3	1	0: Set C2 as DET and C3 as INT 1: Set C2 as COMPIN and C3 as COMPOUT
3	Slow turn on control enable	1	1: Enable 0: Disable
2	MIC auto break out control enable	1	1: Enable 0: Disable
1	Moisture detection enable	1	1: Enable. It would return to '0' after the detection was finished. 0: Disable （This bit can be reset by POR, I^2C or WTD）
0	Audio jack detection and configuration enable	1	1: Enable; will be changed to '0' after audio jack detection and configuration 0: Disable

8.2.19. Detection control0

Address:13h

Reset Value:8'b 0000_0000

Type: R/W

Bits	Name	Size	Description
7	Moisture detection force off control	1	0: Moisture detection on and off control would follow 0×12h bit [1]. 1: Moisture detection would be turned off forcibly.
[6:4]	Reserved	3	Do not use.
3	Current source for moisture detection	1	0: Enable 1: Disable
[2:0]	Select the pin for moisture detection in single-pin mode	3	000: CC_IN 001: DP_R 010: DN_L 011: SBU1 100: SBU2 101...111: Reserved

8.2.20. Single-pin mode resistor detection results

Address: 14h

Reset Value: 11111111

Type: Read

Bits	Name	Size	Description
[7:0]	Moisture detection result in single-pin mode with current source enabled	8	0x00 ~ 0xFF: 2 kΩ * Bits, with 0×12h bit [5] = 0; 10 kΩ * Bits, with 0×12h bit [5] = 1.

8.2.21. Moisture resistor detection threshold

Address: 15h

Reset Value: 8'b 0000_0000

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Threshold for moisture detection with current source enabled.	8	DIO4485/4485B would issue 'Moisture detection error' once any contents from 0×14h (in single pin mode) or 0×33h ~ 0×37h (in multi-pin mode) is lower than this threshold.

8.2.22. Function control1

Address: 16h

Reset Value: 8'b 0000_0001

Type: Read/Write

Bits	Name	Size	Description
[7:3]	Reserved	5	Do not use.
2	Select moisture detection mode	1	0: Single-pin mode, will perform moisture on single pin. 1: Multi-pin mode, will perform moisture on multiple pins.
[1:0]	Set the time span between two moisture detections	2	00: No polling. In single-pin mode, perform single detection for the selected pin (0×13h bit [2:0]). In multi-pin mode, perform single detection for all selected pins (0×31h bit [4:0]). 01: Polling with 100 ms time span 10: Polling with 1s time span 11: Polling with 10s time span

8.2.23. MIC detection status

Address: 17h

Reset Value: 8'b 0000_0001

Type: Read

Bits	Name	Size	Description
[7:4]	Reserved	4	Do not use

3	4 pole	1	1: 4 Pole SBU2 to MIC, SBU1 to audio ground 0: others
2	4 pole	1	1: 4 Pole SBU1 to MIC, SBU2 to audio ground 0: others
1	3 pole	1	1: 3 pole 0: others
0	No audio accessory	1	1: No audio accessory 0: Audio accessory attached

8.2.24. System flag

Address: 18h

Reset Value: 8'b 0000_0000

Type: Read Clear

Bits	Name	Size	Description
[7:4]	Reserved	4	Do not use
3	Watchdog timeout	1	0: Watchdog timeout has not occurred 1: Watchdog timeout has occurred
2	Audio jack detection and configuration	1	0: Audio jack detection and configuration has not completed. 1: Audio jack detection and configuration is completed.
1	Moisture detection error	1	0: Moisture occurs. For resistance detection, result(s) ≥ TH0 For voltage detection, result(s) ≤ TH1 1: Moisture doesn't occur. For resistance detection, result(s) < TH0 For voltage detection, result(s) > TH1
0	Moisture detection completion	1	0: Moisture detection has been not completed 1: Moisture detection is completed.

8.2.25. System mask

Address: 19h

Reset Value: 8'b 0000_0000

Type: Read/Write

Bits	Name	Size	Description
[7:4]	Reserved	4	Do not use.
3	Watchdog timeout mask	1	0: "Watchdog timeout" bit is not masked. 1: "Watchdog timeout" bit is masked.
2	Audio jack detection and configuration mask	1	0: "Audio jack detection and configuration" bit is not masked. 1: "Audio jack detection and configuration" bit is masked.
1	Moisture detection error mask	1	0: "Moisture detection error" bit is not masked. 1: "Moisture detection error" bit is masked.
0	Moisture detection completion mask	1	0: "Moisture detection completion" bit is not masked. 1: "Moisture detection completion" bit is masked.

8.2.26. MIC detection threshold data0

Address: 1Ch

Reset Value: 8'b 0010_0000

Type: Write

Bits	Name	Size	Description
[7:0]	MIC detection threshold data0	8	MIC detection threshold data0.

8.2.27. MIC detection threshold data1

Address: 1Dh

Reset Value: 8'b 1111_1111

Type: Read/Write

Bits	Name	Size	Description
[7:0]	MIC detection threshold data1	8	MIC detection threshold data1.

8.2.28. I²C reset

Address: 1Eh

Reset Value: 8'b 0000_0000

Type: W/C

Bits	Name	Size	Description
[7:1]	Reserved	7	Reserved
0	I²C reset	1	0: default 1: I²C reset

8.2.29. Bias current setting

Address: 1Fh

Reset Value: 8'b 0000_0111

Type: Read/Write

Bits	Name	Size	Description
[7:3]	Reserved	4	Do not use
[2:0]	Bias current setting	4	Setting bias current for audio jack detection. 0000 ~ 1111: Bits × 100 μA

8.2.30. Watchdog setting

Address: 20h

Reset Value: 8'b 0000_0011

Type: Read/Write

Bits	Name	Size	Description
7	Watchdog enable	1	0: Watchdog disabled 1: Watchdog enabled
[6:3]	Reserved	4	Do not use

[2:0]	Watchdog timer	3	000: 0.5 s 001: 1 s 010: 2 s 011: 5 s 100: 10 s 101: 30 s 110: 60 s 111: 5 min

8.2.31. Timing delay between L switch enable and switch on order

Address: 21h

Reset Value: 8'b 0000_0000

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Delay timing setting	8	11111111: 102 ms 11111110: 101.6 ms … 00000001: 400 μs 00000000: 0 μs

8.2.32. Detection data1

Address: 30h

Reset Value: 8'b 0000_0000

Type: Read

Bits	Name	Size	Description
[7:0]	Detection data1	8	Moisture detection result in single-pin mode with current source disabled: 0x00 ~ 0xFF: Bits × 9 × 0.001 [Unit: V]

8.2.33. Detection control1

Address: 31h

Reset Value: 8'b 0000_0000

Type: Read/Write

Bits	Name	Size	Description
[7:6]	Reserved	2	Do not use.
5	Multi-pin mode moisture detection blank time	1	In multi-pin mode, set blank time between detections for different pins. 0: 10 ms 1: 100 ms
4	Select pin (CC_IN)	1	Select pin for moisture detection in multi-pin mode. 0: not selected 1: selected

3	Select pin (DP_R)	1	Select pin for moisture detection in multi-pin mode. 0: not selected 1: selected
2	Select pin (DN_L)	1	Select pin for moisture detection in multi-pin mode. 0: not selected 1: selected
1	Select pin (SBU1)	1	Select pin for moisture detection in multi-pin mode. 0: not selected 1: selected
0	Select pin (SBU2)	1	Select pin for moisture detection in multi-pin mode. 0: not selected 1: selected

8.2.34. Moisture voltage detection threshold

Address: 32h

Reset Value: 8'b 0000_0000

Type: Read/Write

Bits	Name	Size	Description
[7:0]	Threshold for moisture detection with current source disabled	8	Threshold for moisture detection with current source disabled. DIO4485/DIO4485B would issue "Moisture detection error" as soon as any contents from 0×30h (in single-pin mode) or 0×38h ~ 0×3Ch (in multi-pin mode) is higher than this threshold.

8.2.35. Multi-pin mode resistor detection result of CC_IN

Address: 33h

Reset Value: 8'b 1111_1111

Type: Read

Bits	Name	Size	Description
[7:0]	Moisture detection in multi-pin mode (CC_IN)	8	Moisture detection result in multi-pin mode with current source enabled: 0x00 ~ 0xFF: 2 kΩ * Bits, with 0×12h bit [5] = 0; 10 kΩ * Bits,, with 0×12h bit [5] = 1.

8.2.36. Multi-pin mode resistor detection result of DP_R

Address: 34h

Reset Value: 8'b 1111_1111

Type: Read

Bits	Name	Size	Description
[7:0]	Moisture detection in multi-pin mode (DP_R)	8	Moisture detection result in multi-pin mode with current source enabled: 0x00 ~ 0xFF: 2 kΩ * Bits, with 0×12h bit [5] = 0; 10 kΩ* Bits, with 0×12h bit [5] = 1.

8.2.37. Multi-pin mode resistor detection result of DN_L

Address: 35h

Reset Value: 8'b 1111_1111

Type: Read

Bits	Name	Size	Description
[7:0]	Moisture detection in multi-pin mode (DN_L)	8	Moisture detection result in multi-pin mode with current source enabled: 0x00 ~ 0xFF: 2 kΩ * Bits, with 0×12h bit [5] = 0; 10 kΩ * Bits, with 0×12h bit [5] = 1.

8.2.38. Multi-pin mode resistor detection result of SBU1

Address: 36h

Reset Value: 8'b 1111_1111

Type: Read

Bits	Name	Size	Description
[7:0]	Moisture detection in multi-pin mode (SBU1)	8	Moisture detection result in multi-pin mode with current source enabled: 0x00 ~ 0xFF: 2 kΩ * Bits, with 0×12h bit [5] = 0; 10 kΩ * Bits, with 0×12h bit [5] = 1.

8.2.39. Multi-pin mode resistor detection result of SBU2

Address: 37h

Reset Value: 8'b 1111_1111

Type: Read

Bits	Name	Size	Description
[7:0]	Moisture detection in multi-pin mode (SBU2)	8	Moisture detection result in multi-pin mode with current source enabled: 0x00 ~ 0xFF: 2 kΩ * Bits, with 0×12h bit [5] = 0; 10 kΩ * Bits, with 0×12h bit [5] = 1.

8.2.40. Multi-pin mode voltage detection result of CC_IN

Address: 38h

Reset Value: 8'b 0000_0000

Type: Read

Bits	Name	Size	Description
[7:0]	Moisture detection in multi-pin mode (CC_IN)	8	Moisture detection result in multi-pin mode with current source disabled. 0x00 ~ 0xFF: Bits × 9 × 0.001 [unit: V]

8.2.41. Multi-pin mode voltage detection result of DP_R

Address: 39h

Reset Value: 8'b 0000_0000

Type: Read

Bits	Name	Size	Description
[7:0]	Moisture detection in multi-pin mode (DP_R)	8	Moisture detection result in multi-pin mode with current source disabled. 0x00 ~ 0xFF: Bits × 9 × 0.001 [unit: V]

8.2.42. Multi-pin mode voltage detection result of DN_L

Address: 3A

Reset Value: 8'b 0000_0000

Type: Read

Bits	Name	Size	Description
[7:0]	Moisture detection in multi-pin mode (DN_L)	8	Moisture detection result in multi-pin mode with current source disabled. 0x00 ~ 0xFF: Bits × 9 × 0.001 [unit: V]

8.2.43. Multi-pin mode voltage detection result of SBU1

Address: 3B

Reset Value: 8'b 0000_0000

Type: Read

Bits	Name	Size	Description
[7:0]	Moisture detection in multi-pin mode (SBU1)	8	Moisture detection result in multi-pin mode with current source disabled. 0x00 ~ 0xFF: Bits × 9 × 0.001 [unit: V]

8.2.44. Multi-pin mode voltage detection result of SBU2

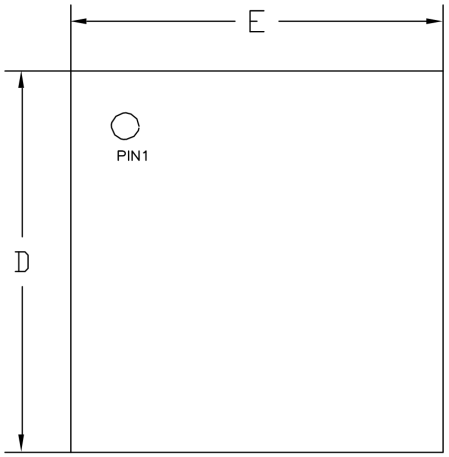
Address: 3C

Reset Value: 8'b 0000_0000

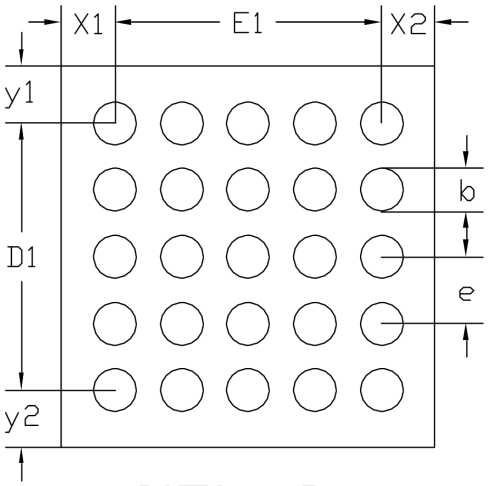
Type: Read

Bits	Name	Size	Description
[7:0]	Moisture detection in multi-pin mode (SBU2)	8	Moisture detection result in multi-pin mode with current source disabled. 0x00 ~ 0xFF: Bits × 9 × 0.001 [unit: V]

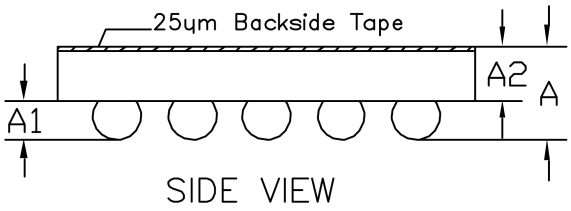
9. Physical Dimensions: WLCSP-25



TOP VIEW
(MARK SIDE)



BOTTOM VIEW
(BALL SIDE)



SIDE VIEW

Common Dimensions (Units of measure = Millimeter)			
Symbol	**Min**	**Nom**	**Max**
A	0.541	0.586	0.631
A1	0.190	0.210	0.230
A2	0.351	0.376	0.401
D	2.250	2.280	2.310
D1	1.600 BSC		
E	2.210	2.240	2.270
E1	1.600 BSC		
b	0.238	0.258	0.278
e	0.400 BSC		
x1	0.320 REF		
x2	0.320 REF		
y1	0.340 REF		
y2	0.340 REF		

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