

CMS46N03V8-HF

N-Channel
RoHS Device
Halogen Free

Features

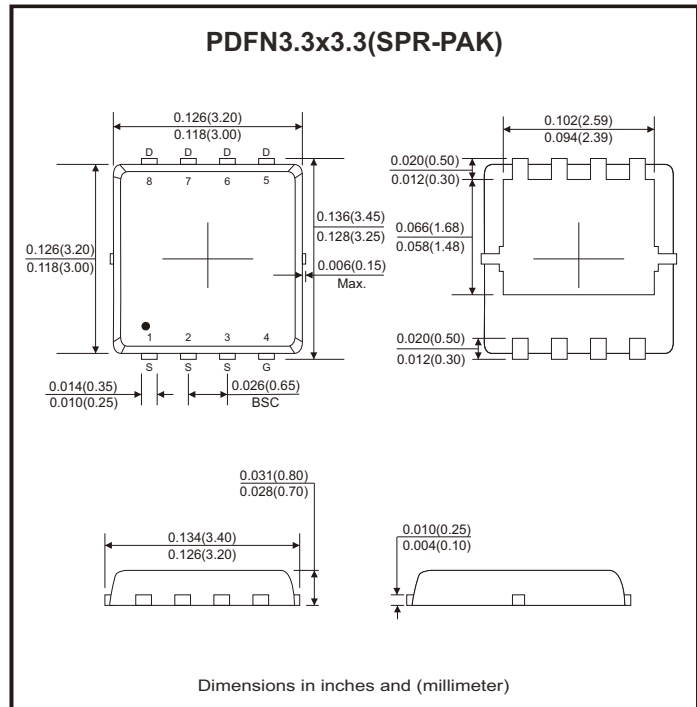
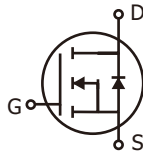
- Advanced high cell density trench technology.
- Super low gate charge.
- Excellent cdv/dt effect decline.
- Green device available.
- 100% EAS guaranteed.

Mechanical data

- Case: PDFN3.3x3.3/SPR-PAK standard package, molded plastic.

Circuit Diagram

- G : Gate
- S : Source
- D : Drain



Maximum Ratings

Parameter	Conditions	Symbol	Value	Unit
Drain-source voltage		V_{DS}	30	V
Gate-source voltage		V_{GS}	± 20	V
Continuous drain current (Note 1, 4)	$T_C = 25^\circ\text{C}$	I_D	46	A
Continuous drain current (Note 1)	$T_C = 100^\circ\text{C}$	I_D	29	
Pulsed drain current (Note 1, 2)		I_{DM}	92	A
Continuous drain current	$T_A = 25^\circ\text{C}$	I_D	11	A
	$T_A = 70^\circ\text{C}$	I_D	9	
Total power dissipation (Note 4)	$T_C = 25^\circ\text{C}$	P_D	29	W
	$T_A = 25^\circ\text{C}$	P_D	1.67	
Single pulse avalanche energy, $L=0.1\text{mH}$ (Note 3)		E_{AS}	57.8	mJ
Single pulse avalanche current, $L=0.1\text{mH}$ (Note 3)		I_{AS}	34	A
Operating junction and storage temperature range		T_J, T_{STG}	-55 to +150	$^\circ\text{C}$
Thermal resistance junction-ambient (Note 1)	Steady state	$R_{\theta JA}$	75	$^\circ\text{C/W}$
Thermal resistance junction-case (Note 1)	Steady state	$R_{\theta JC}$	4.3	$^\circ\text{C/W}$

Notes: 1. The data tested by surface mounted on a 1 inch² FR-4 board with 2 oz copper.

2. The data tested by pulsed, pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.

3. The EAS data shows max. rating. The test condition is $V_{DD}=25\text{V}$, $V_{GS}=10\text{V}$, $L=0.1\text{mH}$, $I_{AS}=34\text{A}$.

4. The power dissipation is limited by 150°C junction temperature. Package limitation current is 40A.

Company reserves the right to improve product design , functions and reliability without notice.

REV:A

Electrical Characteristics (at $T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source breakdown voltage	BV _{DSS}	V _{GS} = 0V, I _D = 250μA	30			V
Gate threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1.0		2.5	
Gate-source leakage current	I _{GSS}	V _{GS} = ±20V			±100	nA
Drain-source leakage current (T _J =25°C)	I _{DSS}	V _{DS} = 24V, V _{GS} = 0V			1	μA
Drain-source leakage current (T _J =55°C)		V _{DS} = 24V, V _{GS} = 0V			5	
Static drain-source on-resistance (Note 2)	R _{DS(on)}	V _{GS} = 10V, I _D = 15A			9	mΩ
		V _{GS} = 4.5V, I _D = 10A			15	
Total gate charge (Note 2)	Q _g	I _D = 12A, V _{DS} = 20V, V _{GS} = 4.5V		12.8		nC
Gate-source charge	Q _{gs}			3.3		
Gate-drain ("miller") charge	Q _{gd}			6.5		
Turn-on delay time (Note 2)	t _{d(on)}	V _{DS} = 12V, I _D = 5A V _{GS} = 10V, R _G = 3.3Ω		4.5		nS
Rise time	t _r			10.8		
Turn-off delay time	t _{d(off)}			25.5		
Fall time	t _f			9.6		
Input capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = 15V, f = 1MHz		1317		pF
Output capacitance	C _{oss}			163		
Reverse transfer capacitance	C _{rss}			131		
Gate resistance	R _g	f = 1MHz		1.7		Ω
Source-drain diode						
Diode forward voltage (Note 2)	V _{SD}	I _S = 15A, V _{GS} = 0V, T _J =25°C			1.2	V
Continuous source current (Note 1, 4)	I _S	V _G = V _D = 0V, Force current			40	A
Pulsed source current (Note 2, 4)	I _{SM}				80	A
Guaranteed avalanche characteristics						
Single pulse avalanche energy (Note 3)	EAS	V _{DD} = 25V, L = 0.1mH, I _{AS} = 20A	20			mJ

Notes: 1. The data tested by surface mounted on a 1 inch² FR-4 board with 2 oz copper.

2. The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.

3. The min. value is 100% EAS tested guarantee.

4. The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

Rating and Characteristic Curves (CMS46N03V8-HF)

Fig.1 - Typical Output Characteristics

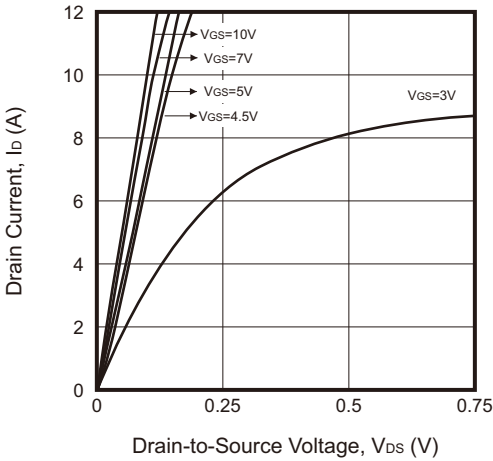


Fig.2 - On-Resistance vs. G-S Voltage

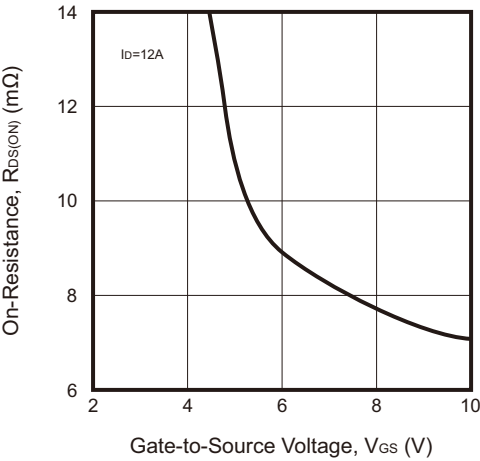


Fig.3 - Normalized $V_{GS(th)}$ vs. T_J

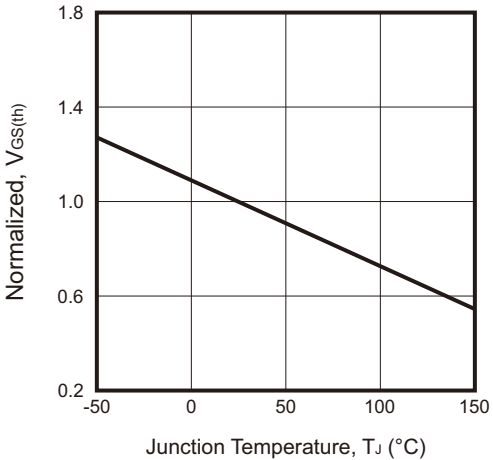


Fig.4 - Normalized $R_{DS(ON)}$ vs. T_J

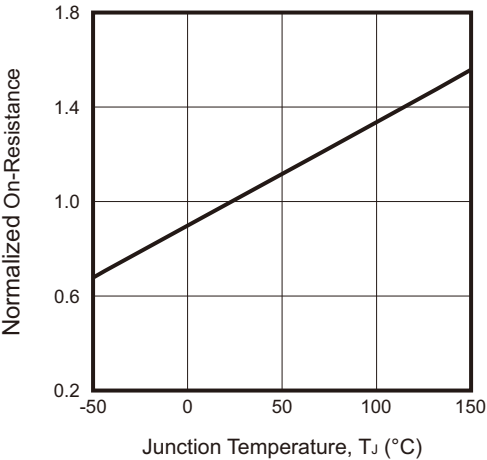


Fig.5 - Safe Operating Area

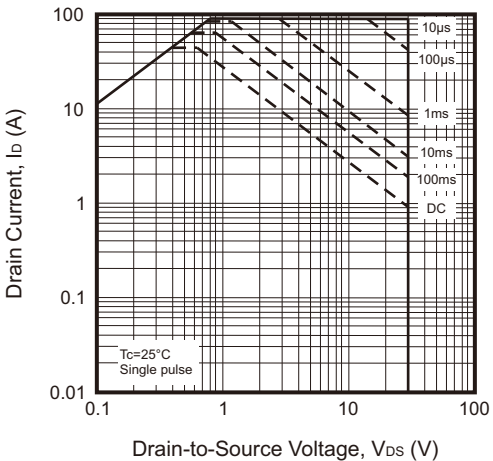
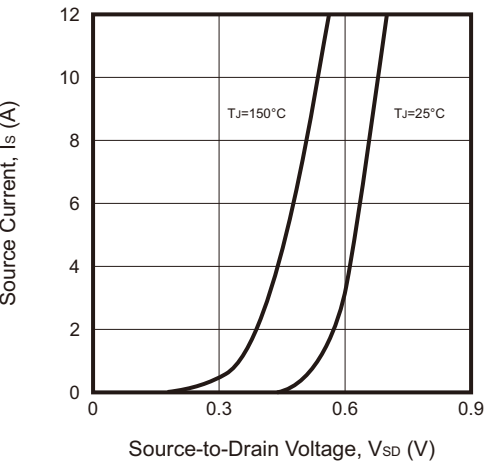


Fig.6 - Forward Characteristics of Reverse



Rating and Characteristic Curves (CMS46N03V8-HF)

Fig.7 - Gate Charge Characteristics

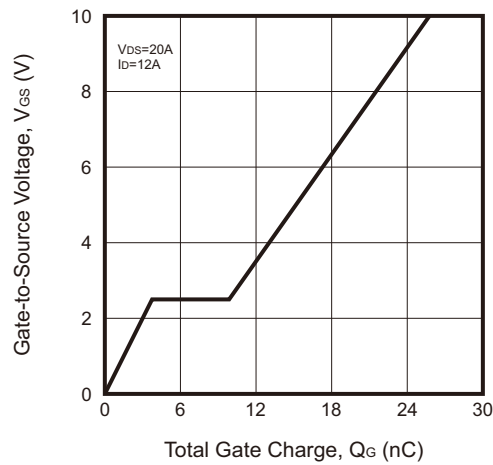
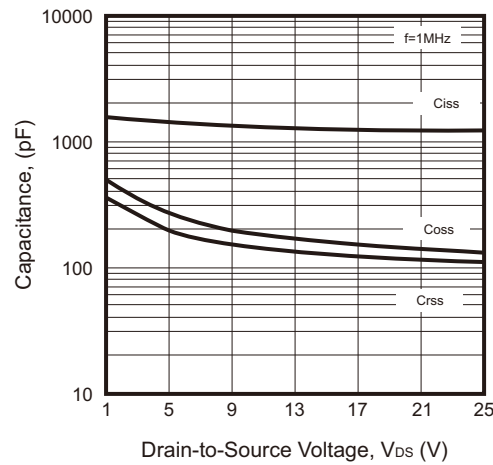
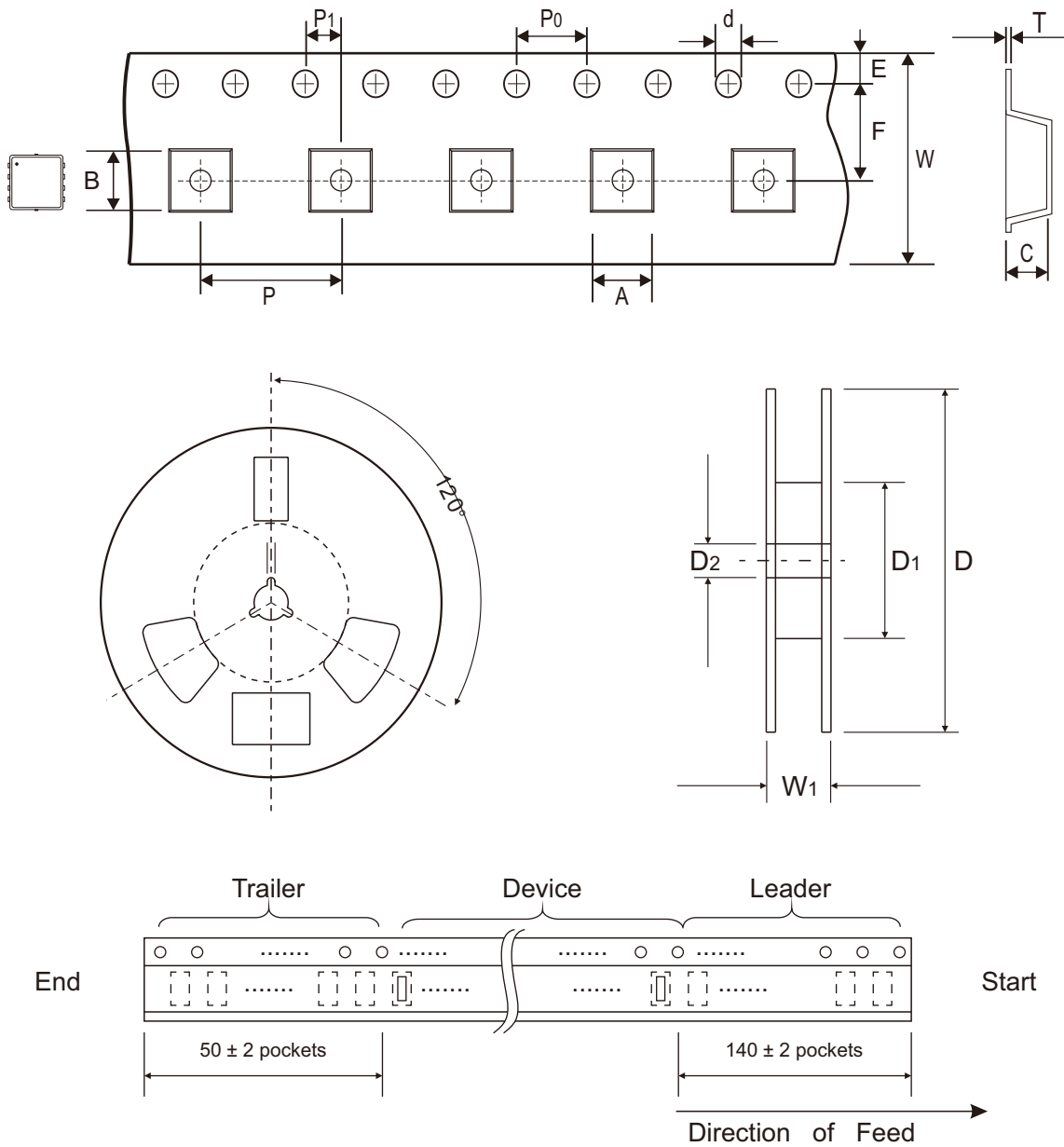


Fig.8 - Capacitance Characteristics



Reel Taping Specification

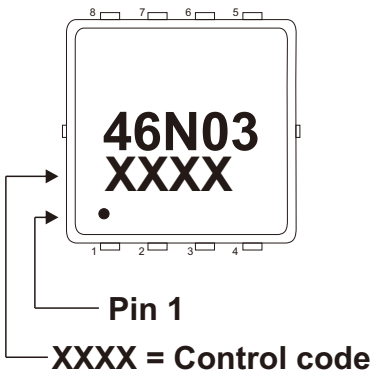


	SYMBOL	A	B	C	d	D	D1	D2
SPR-PAK	(mm)	3.55 ± 0.10	3.55 ± 0.10	1.10 + 0.10 - 0.05	1.50 + 0.10 - 0.00	330.00 ± 1.00	178.00 + 0.00 - 2.00	13.00 min.
	(inch)	0.140 ± 0.004	0.140 ± 0.004	0.043 + 0.004 - 0.002	0.059 + 0.004 - 0.000	12.992 ± 0.039	7.008 + 0.000 - 0.079	0.512 min.

	SYMBOL	E	F	P	P ₀	P ₁	T	W	W ₁
SPR-PAK	(mm)	1.75 ± 0.10	5.50 ± 0.05	8.00 ± 0.10	4.00 ± 0.10	2.00 ± 0.05	0.30 ± 0.05	12.00 + 0.30 - 0.10	18.40 ref.
	(inch)	0.069 ± 0.004	0.217 ± 0.002	0.315 ± 0.004	0.157 ± 0.004	0.079 ± 0.002	0.012 ± 0.002	0.472 + 0.012 - 0.004	0.724 ref.

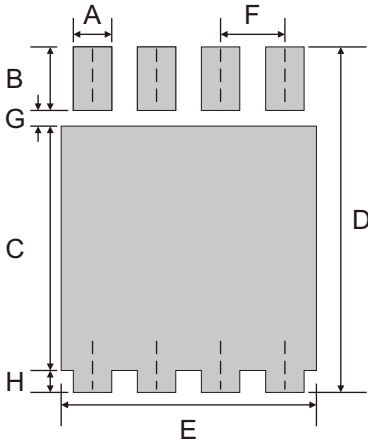
Marking Code

Part Number	Marking Code
CMS46N03V8-HF	46N03 XXXX



Suggested PAD Layout

SIZE	SPR-PAK (PDFN3.3x3.3)	
	(mm)	(inch)
A	0.40	0.016
B	0.60	0.024
C	2.35	0.093
D	3.55	0.140
E	2.80	0.110
F	0.65	0.026
G	0.35	0.014
H	0.25	0.010



Note: 1. The pad layout is for reference purposes only.

Standard Packaging

Case Type	REEL PACK	
	REEL (pcs)	Reel Size (inch)
SPR-PAK (PDFN3.3x3.3)	3,000	13

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