GENERAL DESCRIPTION

The ALD212900A/ALD212900 precision N-Channel EPAD® MOSFET array is precision matched at the factory using ALD’s proven EPAD® CMOS technology. These dual monolithic devices are enhanced additions to the ALD110900A/ALD110900 EPAD® MOSFET Family, with increased forward transconductance and output conductance, particularly at very low supply voltages. Intended for low voltage, low power small signal applications, the ALD212900A/ALD212900 features Zero-Threshold™ voltage, which enables circuit designs with input/output signals referenced to GND at enhanced operating voltage ranges. With these devices, a circuit with multiple cascading stages can be built to operate at extremely low supply/bias voltage levels. For example, a nanopower input amplifier stage operating at less than 0.2V supply voltage has been successfully built with these devices.

ALD212900A EPAD MOSFETs feature exceptional matched pair device electrical characteristics of Gate Threshold Voltage VGS(th) set precisely at 0.00V ±0.01V, IDSS = +20uA @ VDS = 0.1V, with a typical offset voltage of only ±0.001V (1mV). Built on a single monolithic chip, they also exhibit excellent temperature tracking characteristics. These precision devices are versatile as design components for a broad range of analog small signal applications such as basic building blocks for current mirrors, matching circuits, current sources, differential amplifier input stages, transmission gates, and multiplexers. They also excel in limited operating voltage applications, such as very low level voltage-clamps and nano-power normally-on circuits.

In addition to precision matched-pair electrical characteristics, each individual EPAD MOSFET also exhibits well controlled manufacturing characteristics, enabling the user to depend on tight design limits from different production batches. These devices are built for minimum voltage offset and differential thermal response, and they can be used for switching and amplifying applications in +0.1V to +10V (±0.05V to ±5V) powered systems where low input bias current, low input capacitance, and fast switching speed are desired. At VGS > 0.00V, the device exhibits enhancement mode characteristics whereas at VGS < 0.00V the device operates in the subthreshold voltage region and exhibits conventional depletion mode characteristics, with well controlled turn-off and sub-threshold levels that operate the same as standard enhancement mode MOSFETs.

The ALD212900A/ALD212900 features high input impedance (2.5 x 10^10 Ω) and high DC current gain (>10^8). A sample calculation of the DC current gain at a drain output current of 30mA and input current of 300pA at 25°C is 30mA/300pA = 100,000,000, which translates into a dynamic operating current range of about eight orders of magnitude. A series of four graphs titled “Forward Transfer Characteristics”, with the 2nd and 3rd sub-titled “expanded (subthreshold)” and the 4th sub-titled “low voltage”, illustrates the wide dynamic operating range of these devices.

Generally it is recommended that the V+ pin be connected to the most positive voltage and the V- and IC (internally-connected) pins to the most negative voltage in the system. All other pins must have voltages within these voltage limits at all times. Standard ESD protection facilities and handling procedures for static sensitive devices are highly recommended when using these devices.

ORDERING INFORMATION ("L" suffix denotes lead-free (RoHS))

<table>
<thead>
<tr>
<th>Operating Temperature Range *</th>
<th>0°C to +70°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>8-Pin SOIC Package</td>
<td>8-Pin Plastic Dip Package</td>
</tr>
<tr>
<td>ALD212900ASAL ALD212900PAL</td>
<td>ALD212900APAL ALD212900PAL</td>
</tr>
</tbody>
</table>

*Contact factory for industrial temp. range or user-specified threshold voltage values.

FEATURES & BENEFITS

- Zero Threshold™ VGS(th) = 0.00V ±0.01V
- VGS (VGS(th) match) to 2mV/10mA match.
- Sub-threshold voltage (nano-power) operation
- < 100nA min. operating current
- < 1nW min. operating power
- > 100,000,001:1 operating current ranges
- High transconductance and output conductance
- Low RDS(ON) of 14Ω
- Output current >50mA
- Matched and tracked tempco
- Tight lot-to-lot parametric control
- Positive, zero, and negative VGS(th) tempco
- Low input capacitance and leakage currents

APPLICATIONS

- Low overhead current mirrors and current sources
- Zero Power Normally-On circuits
- Energy harvesting circuits
- Very low voltage analog and digital circuits
- Zero power fail-safe circuits
- Backup battery circuits & power failure detectors
- Extremely low level voltage-clamps
- Extremely low level zero-crossing detector
- Matched source followers and buffers
- Precision current mirrors and current sources
- Matched capacitive probes and sensor interfaces
- Charge detectors and charge integrators
- High gain differential amplifier input stage
- Matched peak-detectors and level-shifters
- Multiple Channel Sample-and-Hold switches
- Precision Current multipliers
- Discrete matched analog switches/multiplexers
- Nanopower discrete voltage comparators

PIN CONFIGURATION

<table>
<thead>
<tr>
<th>IC*</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
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</thead>
<tbody>
<tr>
<td>V+</td>
<td>5</td>
<td>6</td>
<td>7</td>
<td>8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V-</td>
<td>4</td>
<td>5</td>
<td>6</td>
<td>7</td>
<td>8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V-</td>
<td>1</td>
<td>2</td>
<td>3</td>
<td>4</td>
<td></td>
<td>IC*</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*IC pins are internally connected, connect to V-.

SAL, PAL PACKAGES

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## OPERATING ELECTRICAL CHARACTERISTICS

\( V^+ = +5V \quad V^- = GND \quad TA = 25^\circ C \) unless otherwise specified

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>ALD212900A</th>
<th>ALD212900</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate Threshold Voltage</td>
<td>( V_{GS(th)} )</td>
<td>-0.02</td>
<td>0.00</td>
<td>0.02 V</td>
<td>( VDS = 20\mu A, VDS = 0.1V )</td>
</tr>
<tr>
<td>Offset Voltage</td>
<td>( V_{OS} )</td>
<td>1.8</td>
<td>3.8</td>
<td>2 mV/°C</td>
<td></td>
</tr>
<tr>
<td>Offset Voltage Tempco</td>
<td>( T_{CV_{OS}} )</td>
<td>5</td>
<td></td>
<td>5 ( \mu V/°C )</td>
<td></td>
</tr>
<tr>
<td>Gate Threshold Voltage Tempco</td>
<td>( T_{CV_{GS(th)}} )</td>
<td>-1.7</td>
<td>0.0</td>
<td>+0.6 ( mV/°C )</td>
<td></td>
</tr>
<tr>
<td>On Drain Current</td>
<td>( I_{DS(ON)} )</td>
<td>79</td>
<td>79</td>
<td>mA</td>
<td>( VGS = +3.0V, VDS = +3V )</td>
</tr>
<tr>
<td>Forward Transconductance</td>
<td>( G_{FS} )</td>
<td>38</td>
<td>38</td>
<td>mmho</td>
<td>( VGS = +3.0V, VDS = +3V )</td>
</tr>
<tr>
<td>Transconductance Mismatch</td>
<td>( \Delta G_{FS} )</td>
<td>1.8</td>
<td>1.8</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Output Conductance</td>
<td>( G_{OS} )</td>
<td>2.3</td>
<td>2.3</td>
<td>mmho</td>
<td>( VGS = +3.0V, VDS = +3V )</td>
</tr>
<tr>
<td>Drain Source On Resistance</td>
<td>( R_{DS(ON)} )</td>
<td>14</td>
<td>14</td>
<td>( \Omega )</td>
<td>( VGS = +5.0V, VDS = +0.1V )</td>
</tr>
<tr>
<td>Drain Source On Resistance</td>
<td>( R_{DS(ON)} )</td>
<td>5</td>
<td>1.18</td>
<td>( \K\Omega )</td>
<td>( VGS = +5.0V, VDS = +0.1V )</td>
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<tr>
<td>Drain Source On Resistance Tolerance</td>
<td>( \Delta R_{DS(ON)} )</td>
<td>1.8</td>
<td>1.8</td>
<td>%</td>
<td>( VGS = +5.0V, VDS = +0.1V )</td>
</tr>
<tr>
<td>Drain Source On Resistance Mismatch</td>
<td>( \Delta R_{DS(ON)} )</td>
<td>0.6</td>
<td>0.6</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Drain Source Breakdown Voltage</td>
<td>( V_{DSX} )</td>
<td>10</td>
<td>10</td>
<td>V</td>
<td>( V^- = VGS = -1.0V ) ( I_{DS} = 10\mu A )</td>
</tr>
<tr>
<td>Drain Source Leakage Current(^1)</td>
<td>( I_{DS(OFF)} )</td>
<td>10</td>
<td>400</td>
<td>( pA )</td>
<td>( V^- = VGS = -1.0V ) ( I_{DS} = 10\mu A )</td>
</tr>
<tr>
<td>Gate Leakage Current(^1)</td>
<td>( I_{GSS} )</td>
<td>5</td>
<td>200</td>
<td>( pA )</td>
<td>( V^- = VGS = +5V, VDS = 0 ) ( TA = 125^\circ C )</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>( C_{ISS} )</td>
<td>30</td>
<td>30</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>Transfer Reverse Capacitance</td>
<td>( C_{RSS} )</td>
<td>2</td>
<td>2</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>Turn-on Delay Time</td>
<td>( t_{on} )</td>
<td>10</td>
<td>10</td>
<td>ns</td>
<td>( V^+ = 5V, RL = 5\K\Omega )</td>
</tr>
<tr>
<td>Turn-off Delay Time</td>
<td>( t_{off} )</td>
<td>10</td>
<td>10</td>
<td>ns</td>
<td>( V^+ = 5V, RL = 5\K\Omega )</td>
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<tr>
<td>Crosstalk</td>
<td></td>
<td>60</td>
<td>60</td>
<td>dB</td>
<td>( f = 100\KHz )</td>
</tr>
</tbody>
</table>

Notes: \(^1\) Consists of junction leakage currents
ALD2108xx/ALD2129xx/ALD2148xx/ALD2169xx high precision monolithic quad/dual N-Channel MOSFET arrays are enhanced versions of the ALD1108xx/ALD1109xx EPAD® MOSFET family, with increased forward transconductance and output conductance, intended for operation at very low power supply voltages. These devices are also capable of sub-threshold operation with less than 1nA of operating supply currents and at the same time delivering higher output drive currents (typ. > 50mA). They feature precision Gate Offset Voltages, V_{OS}, defined as the difference in V_{GS(th)} between MOSFET pairs M1 and M2 or M3 and M4.

ALD's Electrically Programmable Analog Device (EPAD®) technology provides the industry's only family of matched MOSFET transistors with a range of precision gate-threshold voltage values. All members of this family are designed and actively programmed for exceptional matching of device electrical and temperature characteristics. Gate Threshold Voltage V_{GS(th)} values range from -3.50V Depletion Mode to +3.50V Enhancement Mode devices, including standard products with V_{GS(th)} specified at -3.50V, -1.30V, -0.80V, +0.00V, +0.20V, +0.40V, +0.80V, +1.40V, and +3.30V. ALD can also provide any customer-desired V_{GS(th)} between -3.50V and +3.50V on a special order basis.

This ALD2108xx/ALD2129xx/ALD2148xx/ALD2169xx EPAD MOSFET Array product family (EPAD MOSFET) is available in three separate categories, each providing a distinctly different set of electrical specifications and characteristics. The first category is the ALD210800/ALD212900 Zero-Threshold™ mode EPAD MOSFETs. The second is the ALD2108xx/ALD2129xx enhancement mode EPAD MOSFETs. The third category includes the ALD2148xx/ALD2169xx depletion mode EPAD MOSFETs. (The suffix "xx" denotes threshold voltage in 0.1V steps, for example, xx=08 denotes 0.80V). For each device there is a zero-tempco bias current and bias voltage point. When a design utilizes such a feature, then the gate-threshold voltage is temperature stable, greatly simplifying certain designs where stability of certain circuit parameters over a temperature range is desired.

The ALD210800A/ALD212900A/ALD212900/ALD212900A Zero-Threshold MOSFETs in which the individual gate-threshold voltage of each MOSFET is set at zero; V_{GS(th)} = 0.00V at I_{DS(ON)} = 10µA @ V_{DS(ON)} = +0.1V (I_{DS(ON)} = 20µA for the dual ALD212900A/ALD212900). Zero-Threshold MOSFETs operate in the enhancement region when operated above threshold voltage (V_{GS} > 0.00V and I_{DS} > 10µA) and subthreshold region when operated at or below threshold voltage (V_{GS} ≤ 0.00V and I_{DS} < 10µA). These devices, along with other low V_{GS(th)} members of the product family, enable ultra low supply voltage analog or digital operation and nanopower circuit designs, thereby reducing or eliminating the use of very high valued (expensive) resistors in many cases.

The ALD2108xx/ALD2129xx (quad/dual) product family features precision matched enhancement mode EPAD MOSFET devices, which require a positive gate bias voltage V_{GS} to turn on. Precision V_{GS(th)} values at +3.30V, +1.40V, +0.80V, +0.40V and +0.20V are offered. No conductive channel exists between the source and drain at zero applied gate voltage (V_{GS} = 0.00V) for +3.30V, +1.40V and +0.80V versions. The +0.40V and the +0.20V versions have a sub-threshold current at about 1nA and 100nA for the ALD2108xx (2nA and 200nA for the ALD2129xx) respectively at zero applied gate voltage. They are also capable of delivering lower R_{DS(ON)} and higher output currents greater than 68mA (see specifications).

The ALD2148xx/ALD2169xx (quad/dual) features Depletion Mode EPAD MOSFETs, which are normally-on devices at zero applied gate voltage. The V_{GS(th)} is set at a negative voltage level (V < V_{GS(th)} < V_{GS}) at which the EPAD MOSFET turns off. Without a supply voltage and/or with V_{GS} = V = 0.00V = Ground, the EPAD MOSFET device is already turned on and exhibits a defined and controlled on-resistance R_{DS(ON)}. An EPAD MOSFET may be turned off when a negative voltage is applied to V-pin and V_{GS} set more negative than its V_{GS(th)}. These Depletion Mode EPAD MOSFETs are different from most other depletion mode MOSFETs and JFETs in that they do not exhibit high gate leakage currents and channel/junction leakage currents, while they stay controlled, modulated and turned off at precise voltages. The same MOSFET device equations as those for enhancement mode devices apply.

**KEY APPLICATION ENVIRONMENTS**

EPAD MOSFETs are ideal for circuits requiring low V_{OS} and low operating currents with tracked differential thermal responses. They feature low input bias currents (less than 200pA max.), low input capacitance and fast switching speed. These and other operating characteristics offer unique solutions in one or more of the following operating environments:

* Low supply voltage: 0.1V to 10V (±0.05V to ±5V)
* Ultra low supply voltage: < 210mV to ±0.1V
* Nanopower operation: voltage x current = nW or µW
* Precision V_{OS} characteristics
* Matching and tracking of multiple MOSFETs
* Matching across multiple packages

**ELECTRICAL CHARACTERISTICS**

The turn-on and turn-off electrical characteristics of the EPAD MOSFET products are shown in the I_{DS(ON)} vs. V_{DS(ON)} and I_{DS(ON)} vs. V_{GS(th)} graphs. Each graph shows I_{DS(ON)} versus V_{DS(ON)} and I_{DS(ON)} vs. V_{GS(th)} characteristics as a function of V_{GS} in a different operating region under different bias conditions, while I_{DS(ON)} at a given gate input voltage is controlled and predictable. A series of four graphs titled “Forward Transfer Characteristics”, with the 2nd and 3rd sub-titled “expanded (subthreshold)”, and the 4th sub-titled “low voltage”, illustrates the wide dynamic operating range of these devices.

Classic MOSFET equations for an N-channel MOSFET also apply to EPAD MOSFETs.

The drain current in the linear region (V_{DS(ON)} < V_{GS} - V_{GS(th)}) is given by:

\[ I_{DS(ON)} = u \cdot COX \cdot W \cdot L \cdot \left[ V_{GS} - V_{GS(th)} - \frac{V_{DS(ON)}}{2} \right] \cdot V_{DS(ON)} \]

where:

\[ u = \text{Mobility} \]
\[ COX = \text{Capacitance / unit area of Gate electrode} \]
\[ V_{GS} = \text{Gate to Source Voltage} \]
\[ V_{GS(th)} = \text{Gate Threshold (Turn-on)Voltage} \]
\[ V_{DS(ON)} = \text{Drain to Source On Voltage} \]
\[ W = \text{Channel width} \]
\[ L = \text{Channel length} \]

In this region of operation the I_{DS(ON)} value is proportional to the V_{DS(ON)} value and the device can be used as a gate-voltage controlled resistor.

For higher values of V_{DS(ON)} where V_{DS(ON)} > V_{GS} - V_{GS(th)}, the saturation current I_{DS(SAT)} is now given by (approx.):

\[ I_{DS(SAT)} = u \cdot COX \cdot W \cdot L \cdot \left( V_{GS} - V_{GS(th)} \right)^2 \]
SUB-THRESHOLD REGION OF OPERATION

The gate threshold (turn-on) voltage, $V_{GS(th)}$, of the EPAD MOSFET is a voltage below which the MOSFET conduction channel rapidly turns off. For analog designs, this gate threshold voltage directly affects the operating signal voltage range and the operating bias current levels.

At a voltage below $V_{GS(th)}$, an EPAD MOSFET exhibits a turn-off characteristic in an operating region called the subthreshold region. This is when the EPAD MOSFET conduction channel rapidly turns off as a function of decreasing applied gate voltage. The conduction channel, induced by the gate voltage on the gate electrode, decreases exponentially and causes the drain current to decrease exponentially as well. However, the conduction channel does not shut off abruptly with decreasing gate voltage, but rather decreases at a fixed rate of about $10 \text{ mV}$ per decade of drain current decrease. For example, for the ALD2108xx device, if the gate threshold voltage is $+0.20 \text{ V}$, the drain current is $10 \mu \text{A}$ at $V_{GS} = +0.20 \text{ V}$. At $V_{GS} = +0.096 \text{ V}$, the drain current would decrease to $1 \mu \text{A}$. Extrapolating from this, the drain current is about $0.1 \mu \text{A}$ at $V_{GS} = 0.00 \text{ V}$, $1 \mu \text{A}$ at $V_{GS} = -0.216 \text{ V}$, and so forth. This subthreshold characteristic extends all the way down to current levels below $1 \mu \text{A}$ and is limited by junction leakage currents.

At a drain current of “zero current” as defined and selected by the user, the $V_{GS}$ voltage at that zero current can now be estimated. Note that using the above example, with $V_{GS(th)} = +0.20 \text{ V}$, the drain current still hovers around $100 \text{ nA}$ when the gate is at ground voltage. With a device that has $V_{GS(th)} = +0.40 \text{ V}$(part number ALD210804), the drain current is about $2 \text{ nA}$ when the gate is at ground potential. Thus, in this case an input signal referenced to ground can operate with a natural drain current of only $2 \text{ nA}$ internal bias current, dissipating nano-watts of power.

LOW POWER AND NANOPower

When supply voltages decrease, the power consumption of a given load resistor decreases as the square of the supply voltage. Thus, one of the benefits is reducing supply voltage dependency. While decreasing power supply voltages and power consumption go hand-in-hand with decreasing useful AC bandwidth and increased noise effects in the circuit, a circuit designer can make the necessary tradeoffs and adjustments in any given circuit design and bias the circuit accordingly for optimal performance.

With EPAD MOSFETs, a circuit that performs any specific function can be designed so that power consumption of that circuit is minimized. These circuits operate in low power mode where the power consumed is measured in mW, $\mu \text{W}$, and nW (nano-watt) region and still provide a useful and controlled circuit function operation.

ZERO TEMPERATURE COEFFICIENT (ZTC) OPERATION

For an EPAD MOSFET in this product family, operating points exist where the various factors that cause the current to increase as a function of temperature balance out those that cause the current to decrease, thereby canceling each other, and resulting in a net temperature coefficient of near zero. An example of this temperature stable operating point is obtained at a ZTC voltage bias condition, which is $0.38 \text{ V}$ above $V_{GS(th)}$, when $V_{DS(th)} = +0 \text{ V}$, resulting in a temperature stable current level of about $380 \mu \text{A}$ for the ALD2108xx and $760 \mu \text{A}$ for the ALD2129xx devices.
OUTPUT CHARACTERISTICS

LOW VOLTAGE OUTPUT CHARACTERISTICS

FORWARD TRANSFER CHARACTERISTICS

FORWARD TRANSFER CHARACTERISTICS EXPANDED (SUBTHRESHOLD)

FORWARD TRANSFER CHARACTERISTICS LOW VOLTAGE

FORWARD TRANSFER CHARACTERISTICS FURTHER EXPANDED (SUBTHRESHOLD)
TYPICAL PERFORMANCE CHARACTERISTICS (cont.)

LOW LEVEL OUTPUT CONDUCTANCE vs. AMBIENT TEMPERATURE

LOW LEVEL OUTPUT CONDUCTANCE vs. GATE THRESHOLD VOLTAGE

HIGH LEVEL OUTPUT CONDUCTANCE vs. AMBIENT TEMPERATURE

HIGH LEVEL OUTPUT CONDUCTANCE vs. GATE THRESHOLD VOLTAGE

TRANSCONDUCTANCE vs. AMBIENT TEMPERATURE

TRANSCONDUCTANCE vs. GATE THRESHOLD VOLTAGE
TYPICAL PERFORMANCE CHARACTERISTICS (cont.)

OUTPUT CHARACTERISTICS

DRAIN SOURCE ON VOLTAGE - V_{DS(ON)} (V)

V_{GS} = V_{GS(th)} + 3V

DRAIN SOURCE ON CURRENT - I_{DS(ON)} (mA)

V_{GS} - V_{GS(th)} (V)

V_{+} = V_{DS} = +5V

V_{DS(th)} = 0.8V

V_{GS(th)} = -1.4V

ZERO TEMPERATURE COEFFICIENT (ZTC)

DRAIN SOURCE ON CURRENT vs. GATE SOURCE OVERDRIVE VOLTAGE

V_{DS} = +0.1V

V_{GS} - V_{GS(th)} (V)

Zero Temperature Coefficient (ZTC)

GATE SOURCE OVERDRIVE VOLTAGE vs. DRAIN SOURCE ON CURRENT

V_{DS} = +1.0V

GATE SOURCE OVERDRIVE VOLTAGE - V_{GS(th)} (V)

V_{+} = V_{DS} = +5V

GATE THRESHOLD VOLTAGE vs. AMBIENT TEMPERATURE

V_{DS} = +0.1V

I_{D} = 20µA

V_{GS(th)} = 0.8V

-1.0

V_{GS(th)} = -1.4V

-2.0

-50 -25 0 +25 +50 +100 +125

AMBIENT TEMPERATURE - T_{A} (°C)
TYPICAL PERFORMANCE CHARACTERISTICS (cont.)

DRAIN OFF LEAKAGE CURRENT $I_{DS(OFF)}$ vs. AMBIENT TEMPERATURE

OFFSET VOLTAGE vs. AMBIENT TEMPERATURE

$V_{OS} = V_{GS(th)M1} - V_{GS(th)M2}$

REPRESENTATIVE UNITS

$V_{OS}$ (mV)
TYPICAL APPLICATIONS

CURRENT SOURCE MIRROR

\[
\text{ISource} = \text{Iset} = \frac{V^+ - V_t}{R_{\text{set}}}
\]

where \( V_t = V_{GS} - V_{GS(th)} = V_{DS} \)

M1, M2: N-Channel MOSFET
M3, M4: P-Channel MOSFET

CURRENT SOURCE WITH GATE CONTROL

Digital Logic Control of Current Source

ON

OFF

M1: 1/2 ALD1101, 1/2 ALD1116, 1/2 ALD1109xx, 1/2 ALD1109xx, 1/2 ALD2129xx, 1/2 ALD1195, 1/2 ALD1105, 1/2 ALD1105, 1/2 ALD1106, 1/4 ALD1106, 1/4 ALD1108xx, or 1/4 ALD2108xx
M3, M4: ALD1102, ALD1117, 1/2 ALD1103, 1/2 ALD1105, 1/2 ALD1107, or 1/2 ALD3107xx

DIFFERENTIAL AMPLIFIER

PMOS PAIR
M1
M2
M3
M4
VOUT
VIN-
VIN+

NMOS PAIR

M1, M2: N-Channel MOSFET
M3, M4: P-Channel MOSFET

CURRENT SOURCE MULTIPLICATION

\[
\text{ISource} = \text{Iset} \times N
\]

MSET, M1..MN: N x ALD1101, N x ALD1116, N x ALD1109xx, N x ALD1109xx, N x ALD2129xx, N x ALD1103, N x ALD1105, N x ALD1105, N x ALD1106, N x ALD1106, N x ALD1108xx, or N x ALD2108xx

MSET, M1..MN: N x ALD1101, N x ALD1116, N x ALD1109xx, N x ALD1109xx, N x ALD2129xx, N x ALD1103, N x ALD1105, N x ALD1105, N x ALD1106, N x ALD1106, N x ALD1108xx, or N x ALD2108xx

MSET, M1..MN: N x ALD1101, N x ALD1116, N x ALD1109xx, N x ALD2129xx, N x ALD1103, N x ALD1105, N x ALD1106, N x ALD1108xx, or N x ALD2108xx

All M's in the set are from the same part number.
TYPICAL APPLICATIONS (cont.)

BASIC CURRENT SOURCES

N-CHANNEL CURRENT SOURCE

\[ I_{\text{SOURCE}} = I_{\text{SET}} = \frac{V^+ - V_{\text{t}}}{R_{\text{SET}}} \]

where \( V_{\text{t}} = V_{GS} - V_{GS(\text{th})} = V_{DS} \)

P-CHANNEL CURRENT SOURCE

\[ I_{\text{SOURCE}} = I_{\text{SET}} = \frac{V^+ - 2V_{\text{t}}}{R_{\text{SET}}} \]

where \( V_{\text{t}} = V_{GS} - V_{GS(\text{th})} = V_{DS} \)

M1, M2 : N-Channel MOSFET

M3, M4 : P-Channel MOSFET

CASCODE CURRENT SOURCES

M1, M2, M3, M4 : N-Channel MOSFET

where M1 and M2 is a matched pair and M3 and M4 is a second matched pair.

M1, M2, M3, M4 : P-Channel MOSFET

where M1 and M2 is a matched pair and M3 and M4 is a second matched pair.
SOIC-8 PACKAGE DRAWING

8 Pin Plastic SOIC Package

<table>
<thead>
<tr>
<th>Dim</th>
<th>Millimeters</th>
<th>Inches</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>1.35 – 1.75</td>
<td>0.053 – 0.069</td>
</tr>
<tr>
<td>A1</td>
<td>0.10 – 0.25</td>
<td>0.004 – 0.010</td>
</tr>
<tr>
<td>b</td>
<td>0.35 – 0.45</td>
<td>0.014 – 0.018</td>
</tr>
<tr>
<td>C</td>
<td>0.18 – 0.25</td>
<td>0.007 – 0.010</td>
</tr>
<tr>
<td>D-8</td>
<td>4.69 – 5.00</td>
<td>0.185 – 0.196</td>
</tr>
<tr>
<td>E</td>
<td>3.50 – 4.05</td>
<td>0.140 – 0.160</td>
</tr>
<tr>
<td>e</td>
<td>1.27 BSC</td>
<td>0.050 BSC</td>
</tr>
<tr>
<td>H</td>
<td>5.70 – 6.30</td>
<td>0.224 – 0.248</td>
</tr>
<tr>
<td>L</td>
<td>0.60 – 0.937</td>
<td>0.024 – 0.037</td>
</tr>
<tr>
<td>Ø</td>
<td>0° – 8°</td>
<td>0° – 8°</td>
</tr>
<tr>
<td>S</td>
<td>0.25 – 0.50</td>
<td>0.010 – 0.020</td>
</tr>
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8 Pin Plastic DIP Package

<table>
<thead>
<tr>
<th>Dim</th>
<th>Millimeters</th>
<th>Inches</th>
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<tbody>
<tr>
<td>A</td>
<td>3.81  - 5.08</td>
<td>0.105  - 0.200</td>
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<tr>
<td>A1</td>
<td>0.38  - 1.27</td>
<td>0.015  - 0.050</td>
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<tr>
<td>A2</td>
<td>1.27  - 2.03</td>
<td>0.050  - 0.080</td>
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<tr>
<td>b</td>
<td>0.89  - 1.65</td>
<td>0.035  - 0.065</td>
</tr>
<tr>
<td>b1</td>
<td>0.38  - 0.51</td>
<td>0.015  - 0.020</td>
</tr>
<tr>
<td>c</td>
<td>0.20  - 0.30</td>
<td>0.008  - 0.012</td>
</tr>
<tr>
<td>D-8</td>
<td>9.40  - 11.68</td>
<td>0.370  - 0.460</td>
</tr>
<tr>
<td>E</td>
<td>5.59  - 7.11</td>
<td>0.220  - 0.280</td>
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<tr>
<td>E1</td>
<td>7.62  - 8.26</td>
<td>0.300  - 0.325</td>
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<tr>
<td>e</td>
<td>2.29  - 2.79</td>
<td>0.090  - 0.110</td>
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<tr>
<td>e1</td>
<td>7.37  - 7.87</td>
<td>0.290  - 0.310</td>
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<tr>
<td>L</td>
<td>2.79  - 3.81</td>
<td>0.110  - 0.150</td>
</tr>
<tr>
<td>S-8</td>
<td>1.02  - 2.03</td>
<td>0.040  - 0.080</td>
</tr>
<tr>
<td>Ø</td>
<td>0° - 15°</td>
<td>0° - 15°</td>
</tr>
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Click to View Pricing, Inventory, Delivery & Lifecycle Information:

**Advanced Linear Devices:**

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
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<tbody>
<tr>
<td>ALD212900APAL</td>
<td>ALD212900ASAL</td>
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