RICOH R5602L

Li-ion / Li-polymer Battery Management Analog Front-End IC

No.EA-531-210401

OVERVIEW

The R5602 is an analog front-end IC for 4-cell to 7-cell Li-ion / Li-polymer battery management. This IC provides cell voltage monitor, bidirectional current monitor based-on monitoring the voltage across an external sense resistor, two input pin for temperature monitoring by external NTC thermistors, Die temperature monitor, overcurrent protection, high-side NMOSFET control, a voltage regulator, cell balancing switches, switch for open-wire detection and I^{2}C/SPI interface. The IC has a built-in A/D converter and an MCU can read each monitor value as a digital value.

KEY BENEFITS

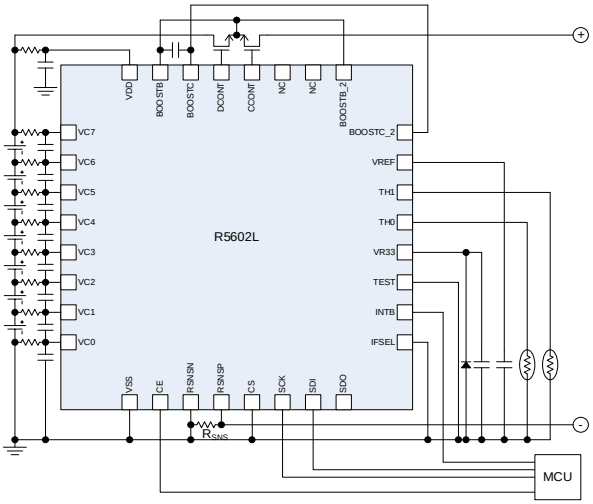
- High accuracy voltage monitoring and low power consumption - for saving battery life.
- Control High-side NMOSFET - for ease of treatment and cost reduction of BOM.
- No limitation in cell connection sequence - for cost reduction of battery pack assembling.

KEY SPECIFICATIONS

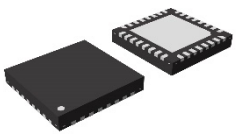
- Absolute Maximum Rating: 40 V
- Power Consumption
  Active: Typ. 150 µA
  Standby: Max. 1.0 µA
- Built-in 12-bit A/D Converter
- Cell Voltage Monitor:
  Input Range: 1.5 V to 4.5 V
  Accuracy: +/-30mV(1)
- Current monitor based-on monitoring voltage across sense resistor
  Gain: x2.5, x10, x20
- Temperature monitoring by two external NTC thermistors
- Die temperature monitoring and high temperature alert.
- Monitoring Speed: less than 1ms/1monitor (Max)
- Overcurrent Protection by Detectors: Overcharge, overdischarge, and short-circuit
- Voltage Regulator Output: Typ.3.4 V
- High-side NMOSFET Control
- Built-in Cell Balancing Switch: Cell Balancing Current depends on external resistor (up to 20mA)
- Built-in switch for Open-wire detection
- No limitation in cell connection sequence when CE = Low
- I^{2}C / SPI interface with/without CRC

TYPICAL APPLICATION

7-cell Connection Diagram with I^{2}C Interface



PACKAG



QFN0505-32C

5mm x 5mm x 0.8mm

APPLICATIONS

- Power Tool, Power Storage, Cordless/Robot Cleaner, Pedelec, E-bike, Drone

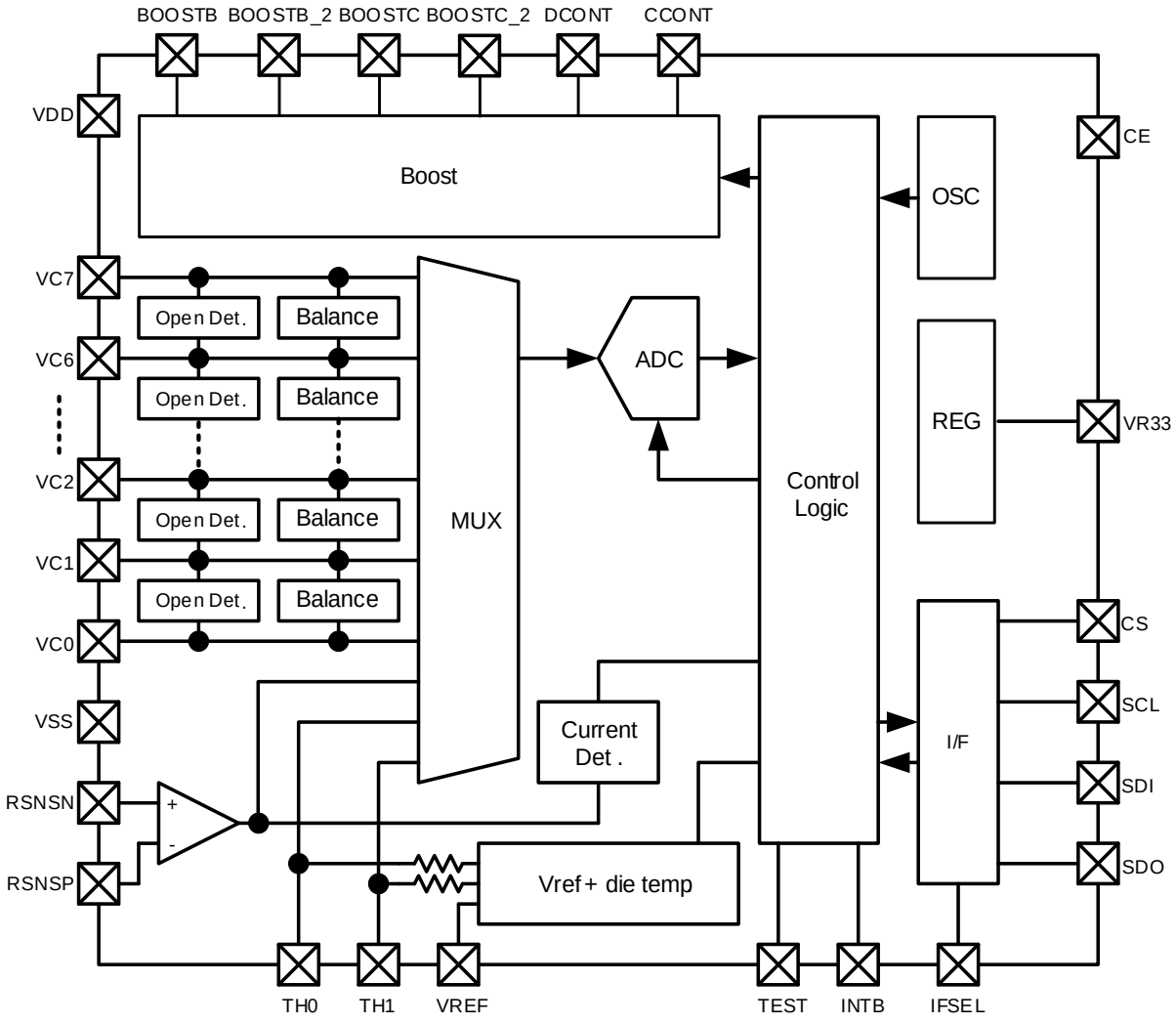
(1) −20°C ≤ Ta ≤ 85°C, V_{VCIN} = 3 V to 4.2 V, V_{DD} ≥ 6.0 V. Cell voltages are balanced.

SELECTION GUIDE

Selection Guide

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R5602L001AA-E2	QFN0505-32C	5,000 pcs	Yes	Yes

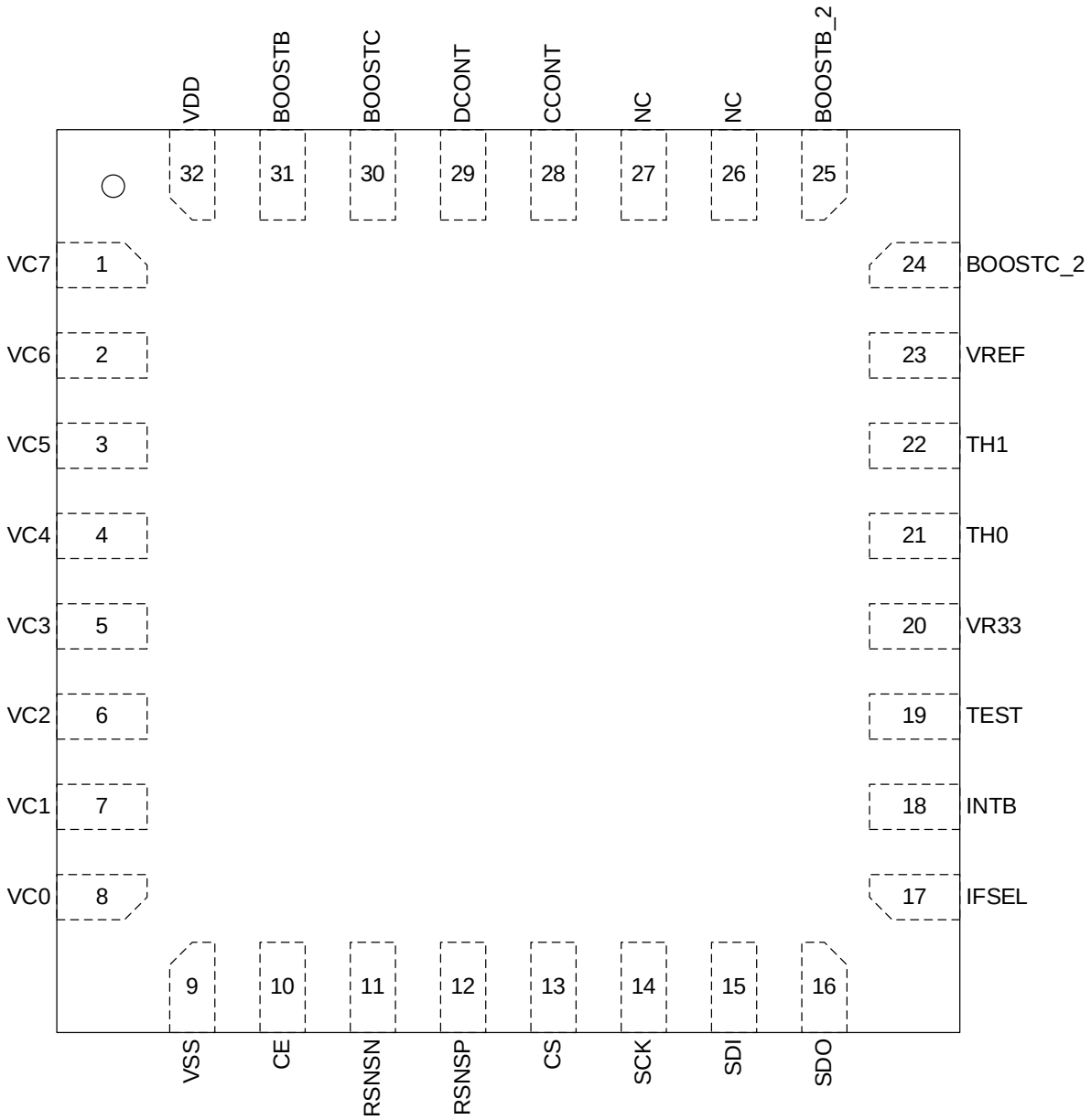
BLOCK DIAGRAM



R5602L Block Diagram

PIN DESCRIPTION

Top View



R5602L (QFN0505-32C) Pin Configuration

R5602L Pin Description

Pin No.	Pin Name	I/O	D/A	Description
1	VC7	I	A/P/G	Positive Pin for Cell 7
2	VC6	I	A/P/G	Positive Pin for Cell 6
3	VC5	I	A/P/G	Positive Pin for Cell 5
4	VC4	I	A/P/G	Positive Pin for Cell 4
5	VC3	I	A/P/G	Positive Pin for Cell 3
6	VC2	I	A/P/G	Positive Pin for Cell 2
7	VC1	I	A/P/G	Positive Pin for Cell 1
8	VC0	I	A/P/G	Negative Pin for Cell 1
9	VSS	-	G	Ground Pin
10	CE	I	D	Chip Enable Pin
11	RSNSN	I	A	R_{SENS} Negative Input Pin
12	RSNSP	I	A	R_{SENS} Positive Input Pin
13	CS	I	D	SPI Chip Select Pin
14	SCK	I	D	Clock Input Pin in Common to SPI and I^2C
15	SDI	IO	D	Input Pin for SPI Data, Input / Output Pin for I^2C Data
16	SDO	O	D	Output Pin for SPI Data
17	IFSEL	I	D	SPI / I^2C Switching Pin (High: SPI, Low: I^2C)
18	INTB	O	D	Interrupt Output Pin (Nch Open-drain Output)
19	TEST	I	D	Connect to GND
20	VR33	O	A	Capacitor and Clamp Diode Connecting Pin for Power Supply
21	TH0	I	A	Thermistor Connecting Pin 0
22	TH1	I	A	Thermistor Connecting Pin 1
23	VREF	O	A	Reference Voltage Capacitor Pin for Internal Use Only
24	BOOSTC_2	I	A	Boost Voltage Input Pin
25	BOOSTB_2	I	A	Boost Reference Voltage Input Pin
26	NC	-	-	Non-Connection
27	NC	-	-	Non-Connection
28	CCONT	O	A	FET Control Pin for Charger, High Potential SPI Chile Select Pin
29	DCONT	O	A	FET Control Pin for Discharger
30	BOOSTC	O	A	Boost Voltage Pin
31	BOOSTB	-	P	Boost Reference Voltage Pin
32	VDD	-	P	Power Supply Pin

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings (Ta = 25°C, V_{SS} = 0 V)

Symbol	Parameter	Pin	Rating	Unit
Power Supply Voltage				
V_{PS1}	Power Supply Voltage1	VDD	− 0.3 to 40	V
			V_{IN1_6} − 0.3 to V_{IN1_6} + 6	V
V_{PS2}	Power Supply Voltage2	BOOSTB	− 0.3 to 40	V
Input Voltage Range				
V_{IN1_n}	Input Voltage Range 1	VCn	$V_{IN1\_(n-1)}$ − 0.3 to $V_{IN1\_(n-1)}$ + 6.0	V
V_{IN2}	Input Voltage Range 2	VC0	V_{SS} − 0.3 to V_{SS} + 0.3	V
V_{IN3}	Input Voltage Range 3	RSENSN, RSNSP	V_{SS} − 0.3 to V_{OUT1} + 0.3	V
V_{IN4}	Input Voltage Range 4	TH0, TH1	V_{SS} − 0.3 to V_{OUT1} + 0.3	V
V_{IN5}	Input Voltage Range 5	CE	V_{SS} − 0.3 to 6.0	V
V_{IN6}	Input Voltage Range 6	CS, TEST, IFSEL	V_{SS} − 0.3 to V_{OUT1} + 0.3	V
V_{IN7}	Input Voltage Range 7	SDI, SCK(SPI)	V_{SS} − 0.3 to V_{OUT1} + 0.3	V
		SDI(I/O), SCK(I^2C)	V_{SS} − 0.3 to 6.0	V
V_{IN8}	Input Voltage Range 8	BOOSTB_2	V_{PS2}	V
V_{IN9}	Input Voltage Range 9	BOOSTC_2	V_{OUT5}	V
Output Voltage Range				
V_{OUT1}	Output Voltage Range 1	VR33	V_{SS} − 0.3 to 6.0	V
V_{OUT2}	Output Voltage Range 2	VREF	V_{SS} − 0.3 to V_{OUT1} + 0.3	V
V_{OUT3}	Output Voltage Range 3	INTB	V_{SS} − 0.3 to 6.0	V
V_{OUT4}	Output Voltage Range 4	SDO	V_{SS} − 0.3 to V_{OUT1} + 0.3	V
V_{OUT5}	Output Voltage Range 5	BOOSTC	V_{PS2} − 0.3 to V_{PS2} + 6	V
V_{OUT6}	Output Voltage Range 6	CCONT, DCONT	V_{PS2} – 0.3 to V_{OUT5} + 0.3	V
ESD				
CDM	Charged Device Model		± 0.5	kV
Power Dissipation				
P_D	Power Dissipation	Refer to Appendix “Power Dissipation”.		
Temperature Range				
Tj	Junction Temperature Range		− 40 to 125	°C
Tstg	Storage Temperature Range		− 55 to 125	°C

(n: 1 to 7)

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

RECOMMENDED OPERATING CONDITIONS

Recommended Operating Conditions

Symbol	Parameter	Rating	Unit
V_{DD}	Power Supply Voltage	6.0 to 31.5	V
V_{BSTB}	Boost Reference Supply Voltage	0 to V_{DD}	V
V_{VCIN}	Cell Voltage Input Range (V_{Cn} –V_{Cn-1})	1.5 to 4.5	V
V_{C0}	Negative Pin for Cell 1 Voltage	0	V
V_{RSNSN}	R_{SENS} Negative Input Pin Voltage	0	V
V_{RSNSP}	R_{SENS} Positive Input Pin Voltage	-0.35 / [IS_GAIN] (1) to 1.65 / [IS_GAIN]	V
V_{THERM}	TH0 and TH1 Input Pin Voltage	0.25 to 2.25	V
Ta	Operating Temperature Range	−20 to 85	°C

(n: 1 to 7)

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

(1) [IS_GAIN] is set to 2.5, 10, or 20 by register.

ELECTRICAL CHARACTERISTICS

DC Characteristics **(Ta = 25°C)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Cell Balancing						
I_{CBn}	Cell Balancing Current	$V_{Cn} - V_{C(n-1)}$ = 4.0 V 100Ω input-resistor			20	mA
I_{LVCn} (1)	Input leakage Current of middle Cell	$V_{Cn} - V_{C(n-1)}$ = 4.5 V, CE: High, Cell Balancing: OFF, Cell Voltage Monitor: OFF			0.5	µA
Cell Voltage Monitor (A/D Converter: ADC)						
V_{VCIN}	Cell Voltage Input Range	$V_{Cn} - V_{C(n-1)}$	1.5		4.5	V
V_{VCA}	Monitoring Accuracy for Cell Voltage	Ta = 25°C, V_{VCIN} = 4.0 V, Cell voltages are balanced.	-15		15	mV
		−20°C ≤ Ta ≤ 85°C, 1.5 V ≤ V_{VCIN} < 2.5 V, Cell voltages are balanced.	-40		40	mV
		−20°C ≤ Ta ≤ 85°C, 2.5 V ≤ V_{VCIN} < 3 V, Cell voltages are balanced.	-35		35	mV
		−20°C ≤ Ta ≤ 85°C, 3 V ≤ V_{VCIN} ≤ 4.2 V, Cell voltages are balanced.	-30		30	mV
		−20°C ≤ Ta ≤ 85°C, 4.2V < V_{VCIN} ≤ 4.5 V, Cell voltages are balanced.	-35		35	mV
Input Current Monitoring (ADC)						
I_{CUR}	Monitoring Ranges for Input Current	R_{SNS} = 5mΩ, [IS_GAIN] = 20	-3.5		16.5	A
		R_{SNS} = 1mΩ, [IS_GAIN] = 2.5	-140		660	A
I_{CUA}	Monitoring Accuracy for Input Current	R_{SNS} = 5mΩ, [IS_GAIN] = 20	-1		1	A
		R_{SNS} = 5mΩ, [IS_GAIN] = 10	-1.4		1.4	A
		R_{SNS} = 5mΩ, [IS_GAIN] = 2.5	-2.4		2.4	A

(n: 1 to 7)

(1) n: 1 to 6 for 7-cell

DC Characteristics (Continued) (Ta = 25°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Current Protection						
R_{SNS}	Resistance Range for SENSE Pin		1		5	mΩ
I_{SHORT}	Setting of Short-circuit Current (1)	[S_{SHORT}] = 2.4, R_{SNS} = 5mΩ [IS_GAIN] = 20		18		A
I_{CUAS}	Short-circuit Current Detection Accuracy		-10		+10	%
I_{DOC}	Setting of Discharge Overcurrent (2)	[S_{DOC}] = 1.4, R_{SNS} = 5mΩ [IS_GAIN] = 20		8		A
I_{CUAD}	Discharge Overcurrent Detection Accuracy		-20		+20	%
I_{COC}	Setting of Charge Overcurrent (3)	[S_{COC}] = 0.05, R_{SNS} = 5mΩ [IS_GAIN] = 20		-5.5		A
I_{CUAC}	Charge Overcurrent Detection Accuracy		-25		+25	%
Voltage Regulator						
V_{VR33}	Output Voltage	−20°C ≤ Ta ≤ 85°C, V_{DD} ≥ 6.0V I_{OUT} ≤ 10mA	3.2	3.4	3.5	V
I_{LIM}	Output Current Limit		10			mA
Die Temperature Detection						
T_{SDD}	Abnormal Detection Temperature at Die High-temperature			150		°C
T_{SDR}	Abnormal Release Temperature at Die High-temperature			125		°C
NTC (Negative Temperature Coefficient) Thermistor for Monitoring						
R_{THn}	NTC Pulled-up Resistance			10		kΩ
Boost Voltage for BOOSTC Pin						
V_{BSTC}	Voltage Boost		V_{BSTB} +4.3	V_{BSTB} +5		V
FET Controller for DCONT, CCONT Pin						
V_{FETH}	FET (DCONT, CCONT) Pin Output Voltage, High	I_{OUT} = 0		V_{BSTC}		V
V_{FETL}	FET (DCONT, CCONT) Pin Output Voltage, Low	I_{OUT} = 0		V_{BSTB}		V
I_{FETIL}	FET (DCONT, CCONT) Pin Output Current, Low	V_{FET} = V_{BSTC} = V_{BSTB} + 6V,		2		mA

(1) [S_{SHORT}] = 2.1, 2.2, 2.3 or 2.4, I_{SHORT} = ([S_{SHORT}] – 0.6) / [IS_GAIN] / R_{SNS}
(2) [S_{DOC}] = 1.1, 1.2, 1.3 or 1.4, I_{DOC} = ([S_{DOC}] – 0.6) / [IS_GAIN] / R_{SNS}
(3) [S_{COC}] = 0.05, 0.1, 0.15 or 0.2, I_{COC} = ([S_{COC}] – 0.6) / [IS_GAIN] / R_{SNS}

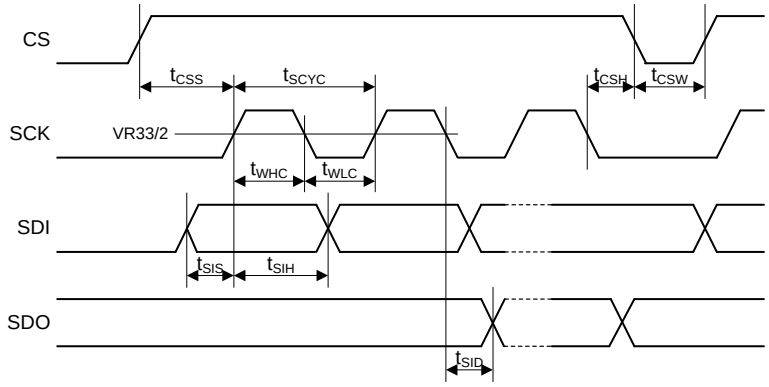
DC Characteristics (Continued) (Ta = 25°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Input Voltage for CS / CE / IFSEL Pin						
V_{CSH}	CS Pin Input Voltage, High		V_{VR33}×0.8			V
V_{CSL}	CS Pin Input Voltage, Low				V_{VR33}×0.2	V
V_{IFSEL}	IFSEL Pin Input Voltage, High		V_{VR33}×0.8			V
V_{IFSEL}	IFSEL Pin Input Voltage, Low				V_{VR33}×0.2	V
V_{CEH}	CE Pin Input Voltage, High		3.0		5.5	V
V_{CEL}	CE Pin Input Voltage, Low		-0.3		0.3	V
Output Voltage for INTB Pin (Nch Open-drain Output)						
V_{INTBL}	INTB Pin Output Voltage, Low	I_{OL} = 3 mA			0.4	V
Current Consumption						
I_{CC}	Current Consumption	Active (1)		150	300	µA
		Standby			1.0	µA
Serial Interface						
SCK: CMOS Input Pin (Schmitt Input)						
V_{IH}	Input Voltage, High		V_{VR33}×0.7			V
V_{IL}	Input Voltage, Low				V_{VR33}×0.3	V
V_{HIS}	Schmitt Hysteresis Voltage		V_{VR33}×0.05			V
SDI: CMOS Input Pin (Schmitt Input / Nch Open-drain Output)						
V_{IH}	Input Voltage, High		V_{VR33}×0.7			V
V_{IL}	Input Voltage, Low				V_{VR33}×0.3	V
V_{HIS}	Schmitt Hysteresis Voltage		V_{VR33}×0.05			V
V_{OL}	Output Voltage, Low	I_{OL} = 3 mA			0.4	V
SDO: CMOS Output Pin						
V_{OH}	Output Voltage, High	I_{OH} = -3 mA	V_{VR33} - 0.4			V
V_{OL}	Output Voltage, Low	I_{OL} = 3 mA			0.4	V

(1) 7-cell (V_{C_TIME} = 80µs) every 2ms. Alert and FET control OFF.

AC Characteristics (Ta = 25°C)

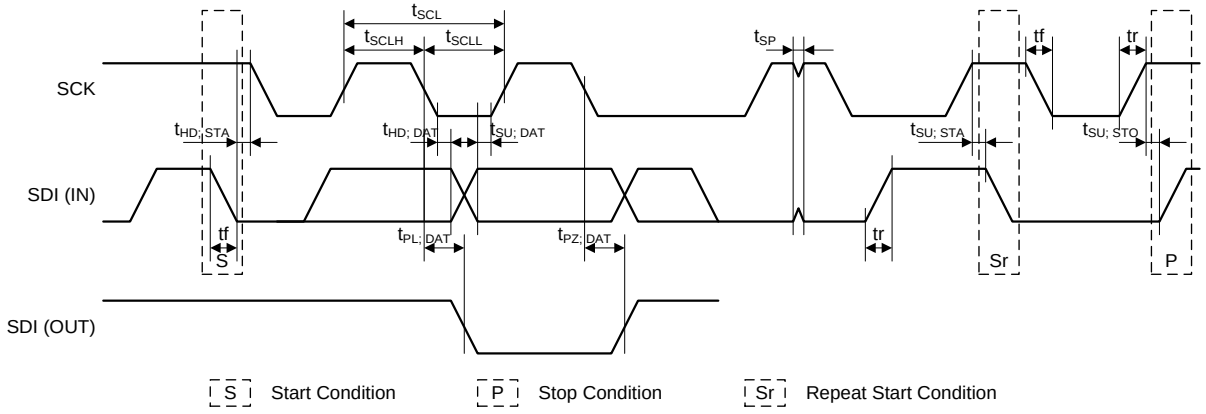
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Single/Sequential Read and Detection Delay Time						
t_{AC}	Time Accuracy		-20		30	%
SPI Communication						
t_{SCYC}	SCK Clock Cycle Time		1			µs
t_{WHC}	SCK Clock Cycle Time, High		400			ns
t_{WLC}	SCK Clock Cycle Time, Low		400			ns
t_{SIS}	Serial Data Set-up Time		100			ns
t_{SIH}	Serial Data Hold Time		100			ns
t_{CSW}	Setup Time for Transmission and Reception		3			µs
t_{CSS}	Setup Time for Chip Enable		200			ns
t_{CSH}	Hold Time for Chip Enable		200			ns
t_{SID}	Delay Time for Serial Data				200	ns



SPI Bus Timing Diagram

AC Characteristics (Continued) (Ta = 25°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I²C Communication						
f_{CLK}	SCK Clock Frequency				400	kHz
t_{SCL}	SCK Clock Cycle		2.5			µs
t_{SCLL}	SCK Clock, Low		1.3			µs
t_{SCLH}	SCK Clock, High		0.6			µs
$t_{SU:STA}$	Start Condition Setup Time		0.6			µs
$t_{SU:DAT}$	Data Setup Time		200			ns
$t_{SU:STO}$	Stop Condition Setup Time		0.6			µs
$t_{HD:STA}$	Start Condition Hold Time		0.6			µs
$t_{HD:DAT}$	Data Hold Time		0			ns
t_r	Rising Time for SDI and SCK				300	ns
t_f	Falling Time for SDI and SCK				300	ns
$t_{PL:DAT}$	Falling Time required for SDI output Low	After falling of SCK			0.9	µs
$t_{PZ:DAT}$	Rising Time required for SDI output High	After falling of SCK			0.9	µs
t_{SP}	Removal Spike Width by Input Filters				50	ns
C_B	Capacitive Load for SDI and SCK Bus lines				50	pF



I²C Bus Timing Diagram

THEORY OF OPERATION

Internal 12-bit ADC

The R5602L has a 12-bit high-accuracy analog-digital converter (ADC), and it can measure cell voltages for the VCn pins, the voltage between the RSNSP and the RSNSN pins generated by charge/discharge current, a voltage divided by an external NTC and an internal resistor, and an internal voltage to monitor the die temperature. While measuring one voltage, the R5602L is impossible to measure another voltage.

Cell Voltage Monitoring

After the analog-to-digital converting by order of the micro-controller unit (MCU), the data for cell voltages $V_{Cn} – V_{C(n-1)}$ (n: 1 to 7) is stored into the internal registers. The MCU can read each cell voltage from the register.

Current Monitoring

The R5602L can read a current that flows via the RSENS resistor between the RSNSN and the RSNSP pins. By following the MCU, the R5602L measures the difference voltage between the RSNSN pin and the RSNSP pin to multiply it by a gain and stores it into the internal register.
The MCU can read the measured voltage from the internal register with the three-step selectable gain of 2.5 / 10 / 20 times.

Temperature Monitoring

[Outside]

By connecting a 10 kΩ NTC thermistor between VSS and TH0 / TH1 pin, the R5602L can supervise the temperatures for external two points of the device. The TH0 and the TH1 pins are pulled-up to the reference voltage 2.5 V with 10 kΩ resistor connected internally to each pin.

[Inside]

By following the MCU's supervising order, the R5602L can measure the voltage met the temperature sensed in the internal temperature-monitoring circuit. The MCU can read the voltage from the register. When the internal temperature is high, an alert signal can be output via the INTB pin.

Sequential Read

The R5602L can monitor the following data of items in sequence.

1. VC7 → VC6 → VC5 → VC4 → VC3 → VC2 → VC1
2. Current via Charger / Discharger path
3. Die Temperature
4. TH1 Temperature
5. Th0 Temperature

When using six-cell or less, the connected cell only can be selected to monitor its voltage. The MCU can control above items of 2 to 5 regardless of the cell voltage.

Overcurrent Detection

Overcurrent Detection is a function to detect overcurrent by the current monitoring. After detection, this function is reset by the external MCU. The overcurrent detection voltage and the overcurrent detection delay time are settable for each of charge and discharge.

High-side NMOSFET Control

By following the MCU's order, the R5602L can control outputs of the CCONT and the DCONT pins that control High-side NMOSFETs. Outputs of the CCONT and the DCONT pins become a CMOS output with the BOOSTC voltage that was risen up as reference to the BOOSTB voltage. Setting the pin to Low can turn off the FET, setting it to High can turn on the FET. When the MCU enable current protection, the CCONT pin becomes Low if detected charge overcurrent, the DCONT pin becomes Low if detected discharge overcurrent or detected short. When the MCU disable current protection, the MCU should turn NMOSFET off at the overcurrent.

Cell Balancing

When the MCU controls the cell balancing switch, the R5602L can flow the discharge current for each cell into the IC. The discharge current value is set with the external resistor. Select external components with due consideration for the power dissipation of the device and external components.

Open-wire Detection

By flowing the discharge current for each cell into the internal resistor of the device, the R5602L monitors the cell voltage and the MCU can detect an open-wire.

INTB Pin Output

When the R5602L detects an event such as the followings, the INTB pin outputs Low. As the output type of the INTB pin is NMOSFET open-drain, pull up it with external resistors.

- Abnormal detection at die high-temperature
- Completion of start-up
- Low-voltage detection VR33 pin output
- CRC error detection
- Completion of ADC read
- Discharge overcurrent detection
- Charge overcurrent detection
- Short-circuit detection

.

Standby Mode

When the CE pin is Low, the R5602L is in the Standby state and registers become initial settings. Usually, setting the CE pin to High goes to the Normal state.

Serial Communication Interfaces

As for communication method to the MCU, the R5602L can select either of two kinds of serial interfaces, SPI or I^2C.

Method	Control Pin	Pin Name
SPI (IFSEL: High)	CS (Chip Select)	CS
	SCK (Serial Clock)	SCK
	MISO (Master In Slave Out)	SDO
	MOSI (Master Out Slave In)	SDI
I^2C (IFSEL: Low)	SCL (Serial Clock)	SCK
	SDA (Serial Data)	SDI

When using the I^2C interface, set the CS pin to VSS.

■ SPI Communication

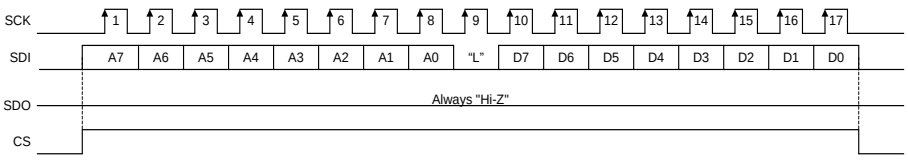
Setting the IFSEL pin to High enables the communication with the SPI interface. This interface has four pins of serial clock (SCK), serial data input pin (SDI), serial data output pin (SDO), and chip-select input pin (CS). The following Write / Read processing is shown as viewed from the master. On the data transferring, Master must transfer from the most significant bit (MSB) of the byte data, first. Likewise, on the data receiving, Slave (R5602L) must transfer from MSB of the byte data first.

[Write Processing]

1. The data is loaded into the internal shift-register at rising edge of SCK (SCK Frequency: Max.1MHz).

2. During the CS pin of High, the data receiving becomes enabled (Active-High). However, the write processing does not work if fixing to High.

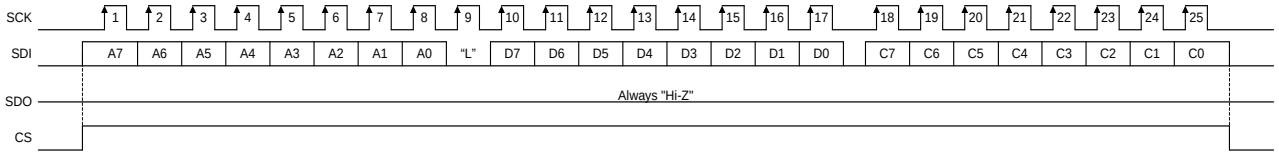
3. The loaded data is transferred from the SDI pin, in order of 8-bit address data, one bit for Low data, and 8-bit control command data in the control register.



Write Timing (No CRC)

4. Setting the CRC_EN register to “1” enables to transfer the data including CRC data (Initial value of [CRC_EN] is "0"). In the case of the data including CRC, 8-bit packet error code (PEC) is transferred after the above transferring. The CRC is calculated over the 8-bit address data, one bit for Low data, and 8-bit control command data. The CRC data is given by the following polynomial.

$$C(x) = X^8 + X^2 + X^1 + 1$$



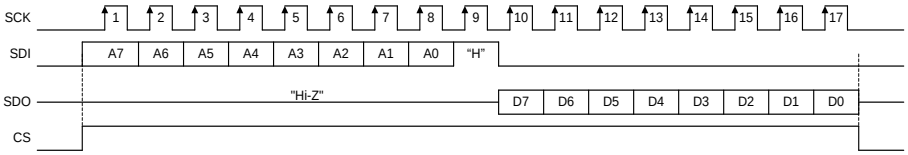
Write Timing (Including CRC)

[Read Processing]

1. The data is loaded into the internal shift-register at rising edge of SCK (SCK Frequency: Max.1MHz).

2. During the CS pin of High, the data receiving and transferring becomes enabled (Active-High). However, the read processing does not work if fixing to High.

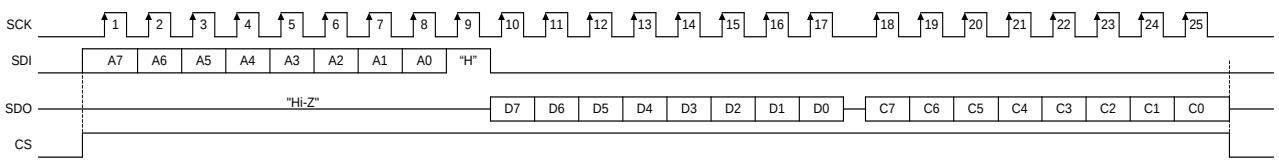
3. After 8-bit address data and one bit for High data is transferred from the SDI pin, 8-bit control register specified is transferred from the SDO pin.



Read Timing (No CRC)

4. Setting the CRC_EN register to “1” enables to transfer the data including CRC data (Initial value of [CRC_EN] is "0"). In the case of the data including CRC, 8-bit packet error code (PEC) is transferred after the above transferring. The CRC is calculated over the 8-bit address data, one bit for High data, and 8-bit read data. The CRC data is given by the following polynomial.

$$C(x) = X^8 + X^2 + X^1 + 1$$



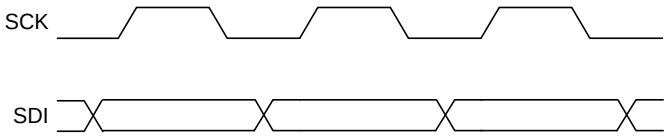
Read Timing (Including CRC)

■ I²C Interface Communication

Setting the IFSEL pin to Low enables the communication with the I²C interface. Each of the SCK and the SDI pins equates to the SCL and the SDA pins in the SPI interface.

Availability of Data

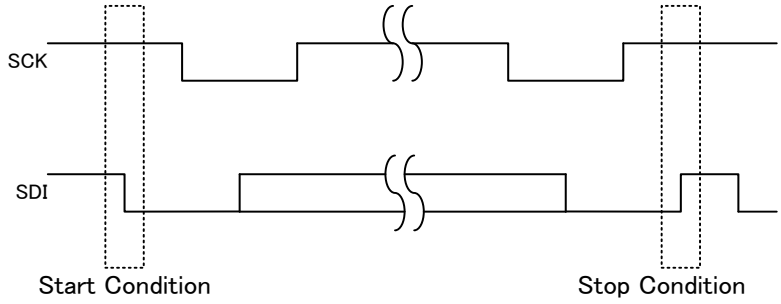
During the SCK pin of High for the data transferring duration, the SDI data of I²C-bus must be maintained constant. The SDI can change between High and Low states only when the SCK pin is Low except Start and Stop conditions.



SDI Timing Chart

Start and Stop Conditions

The SCK and the SDI pins are pulled up to High except for the data transferring duration. The start condition is met when being pulled the SDI pin down from High to Low, and the start and the stop conditions are generated by master only.

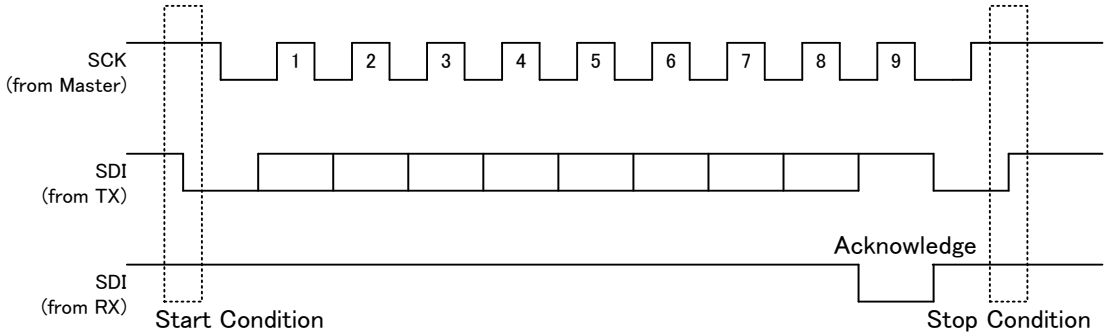


Start and Stop Conditions

Data Transfer Method

After the start condition is generated, the data transferring is done every one-byte from the MSB of a byte. An acknowledge signal is sent from the receiver to the sender at the end of transferring one-byte data.

After transferring a byte data, the master as sender makes the SDI signal Open (= High) and the slave (R5602L) makes the SDI signal Low as acknowledge signal. On the other hand, the slave as sender makes the SDI signal Open (= High). If maintaining to receive the acknowledge signal without interruption, the master makes the SDI signal Low. The master can indicate the end of the data transferring to the slave by making the SDI signal Open (= High).



Data Transfer when Master is Sender

Format for Data Transfer

The format to transfer data via the I^2C bus is as follows. Be sure to begin with start condition and finish with stop condition. On the data transferring, Master must transfer from the most significant bit (MSB) of the byte data, first. Likewise, on the data receiving, Slave (R5602L) must transfer from MSB of the byte data first.

[Write Processing]

The format for write processing after the start condition consists as shown in the following figure.

1st byte: Slave address (32h = 0110010b) + Write instruction

2nd byte: Address for internal register to write the data.

3rd byte: Data to write in the second byte.

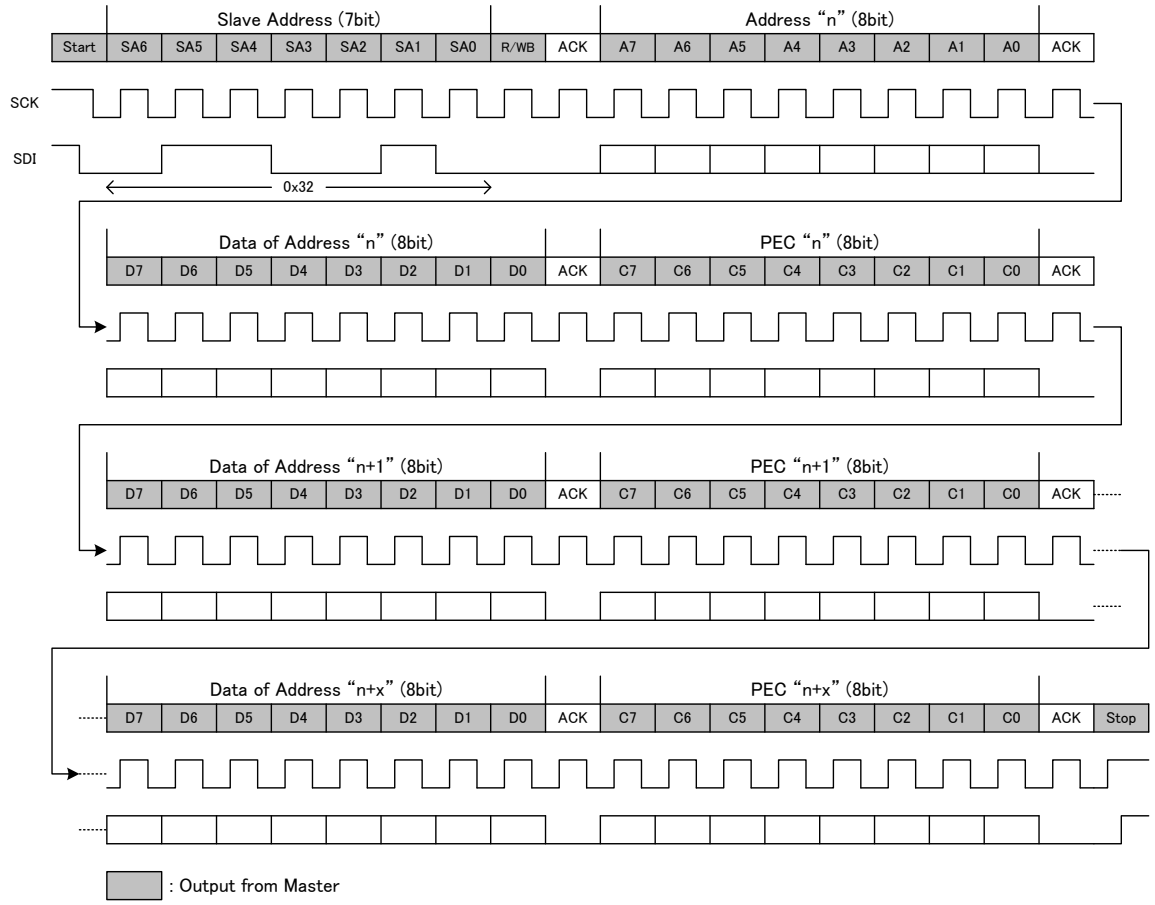
4th byte: Packet error code (PEC) if including the Cyclic Redundancy Check (CRC) data.

The PEC is an 8-bit data to indicate the result of the CRC error detection. The CRC data is given by the following polynomial.

$$C(x) = X^8 + X^2 + X^1 + 1$$

The CRC is calculated for the slave address, register address, and data. When burst write transaction, the CRC for subsequent data bytes is calculated for the data byte only.

An example of the burst write format is as follows:



Write Timing Chart (with CRC, Continuous writing)

[Read Processing]

The format for read processing after the start condition consists as shown in the following figure.

1st byte: Slave address (32h = 0110010b) + Write instruction

2nd byte: Address for the internal register to read the data.

3rd byte: Slave address + Read instruction

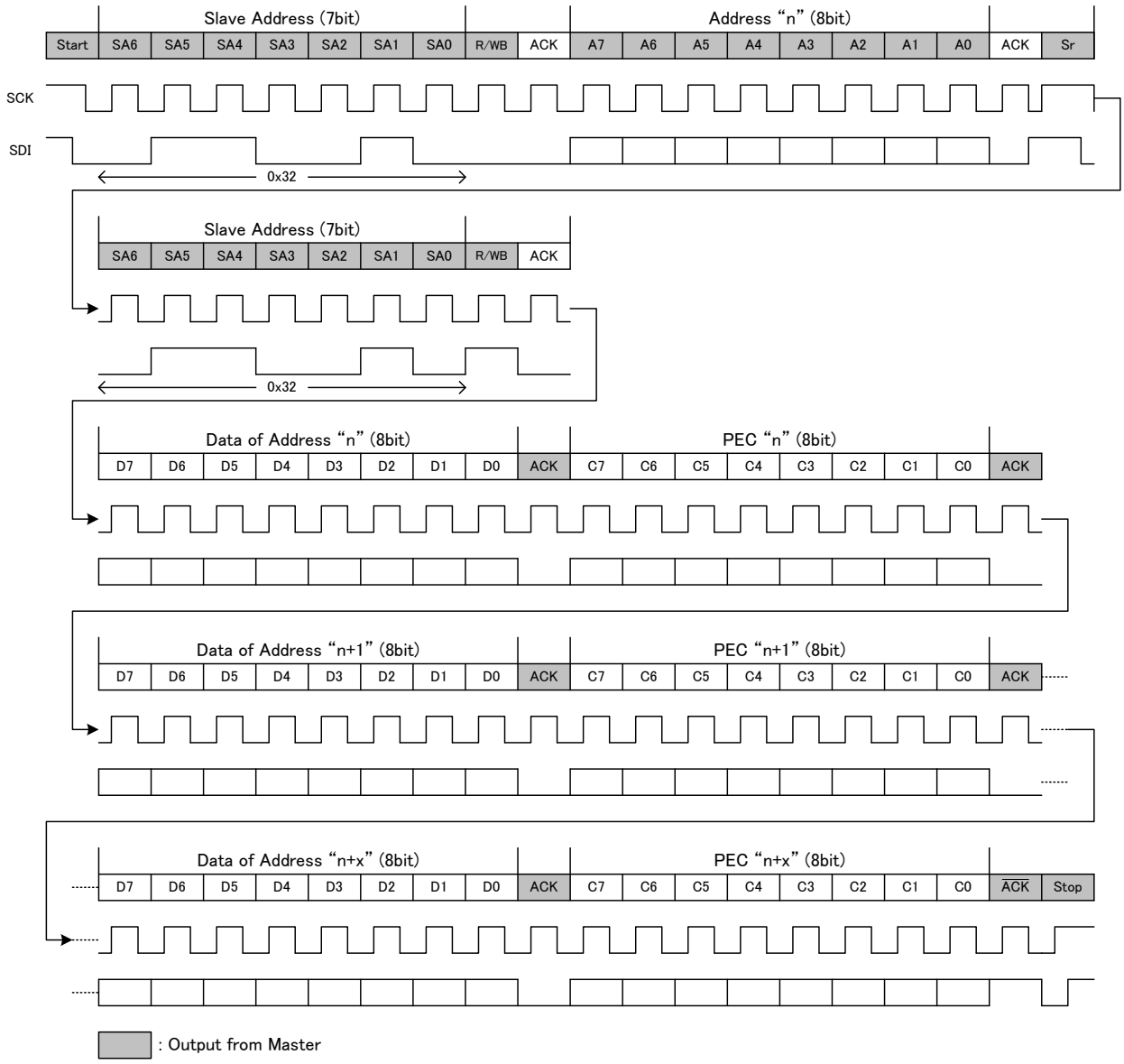
4th byte: Data read out from the address specified in the second byte.

5th byte: Packet error code (PEC) only when including the CRC data

The PEC is an 8-bit data to indicate the result of the CRC error detection. The CRC is calculated after the second start and uses the slave address and data byte. When burst write transaction, the CRC for subsequent data bytes is calculated over the data byte only.

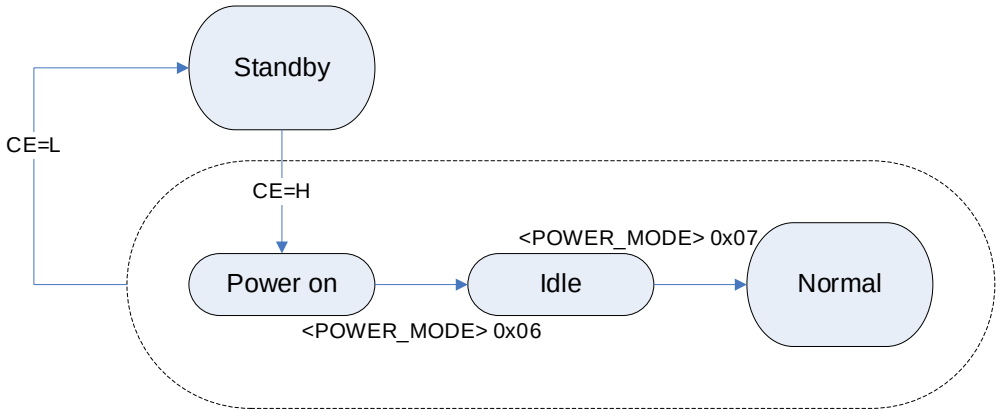
$$C(x) = X^8 + X^2 + X^1 + 1$$

An example of the burst read format is as follows:



Read Timing Chart (with CRC, Continuous reading)

Power on Sequence

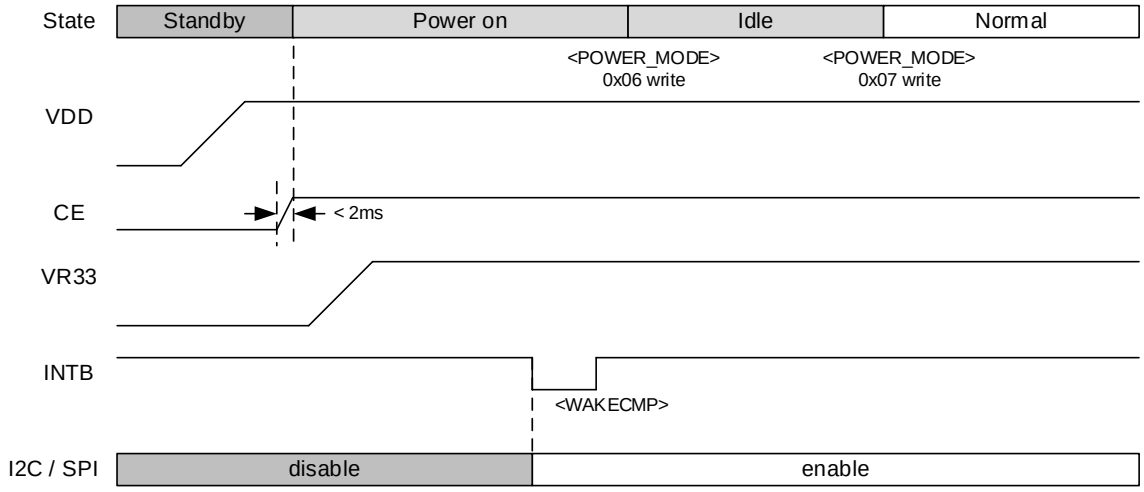


Power Mode Transition Diagram

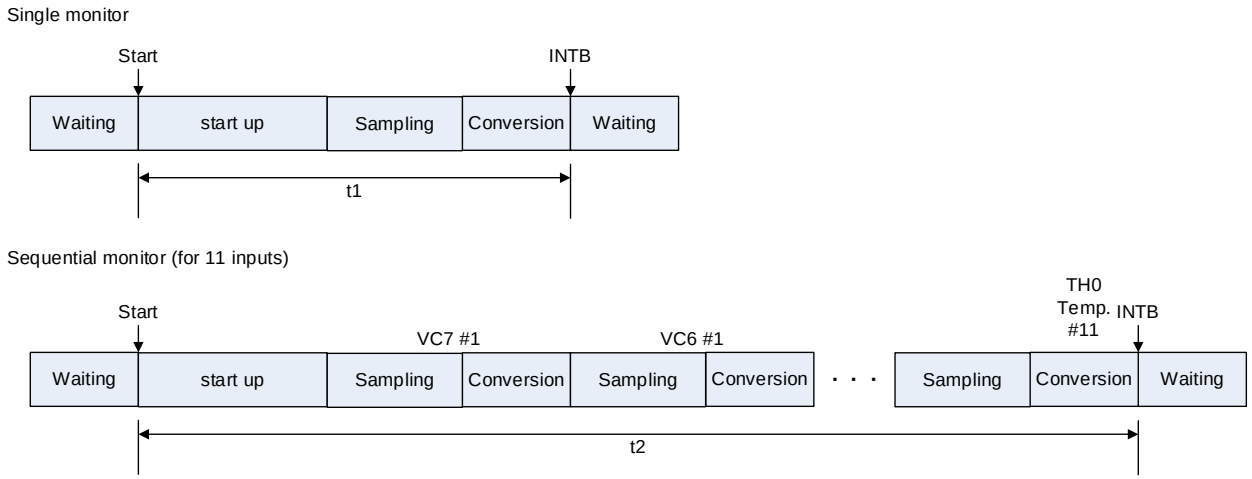
The 5602L enters in Standby state by the CE pin being Low when connecting with a battery. Even if having connected with the battery, the R5602L enters in Standby state by the CE pin being Low. The Standby state goes to the Normal state by the CE pin being High.

In the Normal state, setting the register enables a sequential reading for voltage, current, and temperature. In addition, the Cell Balancing, and the open-wire detection registers can be set individually.

The sequence is shown below.



Single and Sequential Read Status

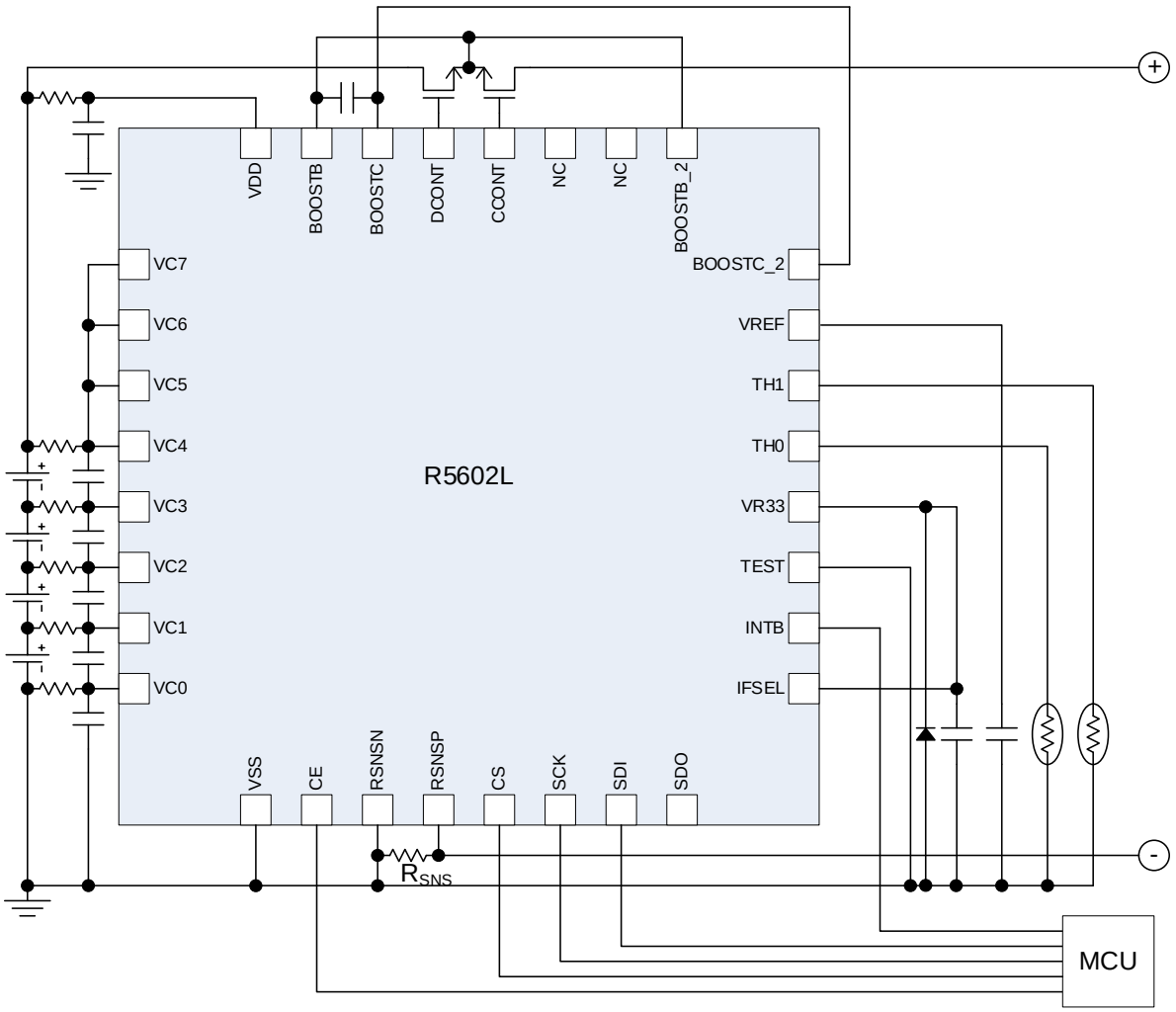


Monitoring Timing Diagram

The ADC monitors in fixed order as shown in above timing charts. The sequential read setting is possible to skip monitoring unassigned VCn pins. The start-up time is 60us, the conversion time is 30µs. t1 and t2 are is specified by the sampling time set registers and the averaged read time set registers.
Minimum sampling time settings are 80µs for VCn at 3 V ≤ V_{VCIN} ≤ 4.5 V, 400µs for VCn at 1.5 V ≤ V_{VCIN} < 3 V, 40us for the others, respectively. (n: 1 to 7)

Battery Connection

The R5602L can support from four- to seven-cell. When using six-cell or less as shown the below diagram, contiguous lower input pins (VC0 to VC4) must be connected with a battery in order of lower voltage, and contiguous upper input pins (VC5 to VC7) must be shorted to VC4 that is a highest potential input pin of used input pins.



4-cell Connection with SPI Interface Diagram(1)

(1) A clamp diode is required for VR33 pin. Recommended V_F < 0.4V@100mA

PD-QFN0505-32-(85125)-JE-A

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51.

Measurement Conditions

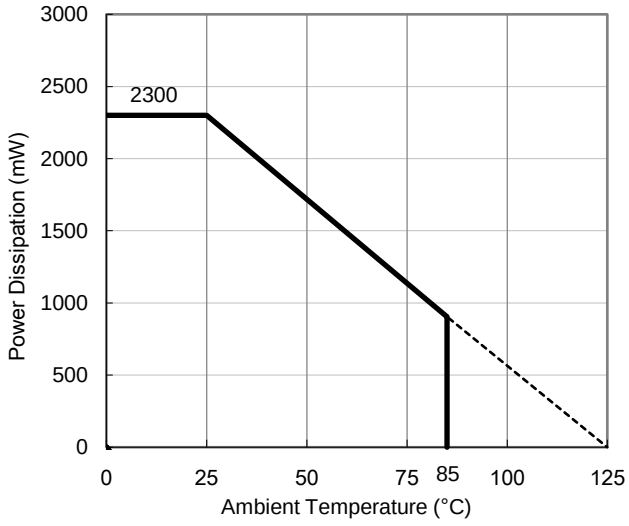
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 1.6 mm
Copper Ratio	Outer Layer (First Layer): Less than 10% Inner Layers (Second and Third Layers): Approx. 100% of 74.2 mm Square Outer Layer (Fourth Layer): Less than 10%
Through-holes	ϕ 0.3 mm × 9pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

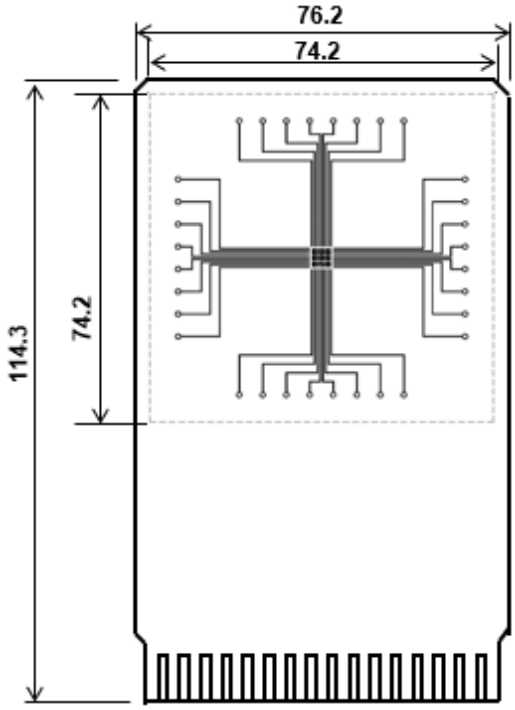
Item	Measurement Result
Power Dissipation	2300mW
Thermal Resistance (θja)	θja = 43°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 16°C/W

θja: Junction-to-Ambient Thermal Resistance

ψjt: Junction–to-top of package thermal characterization parameter



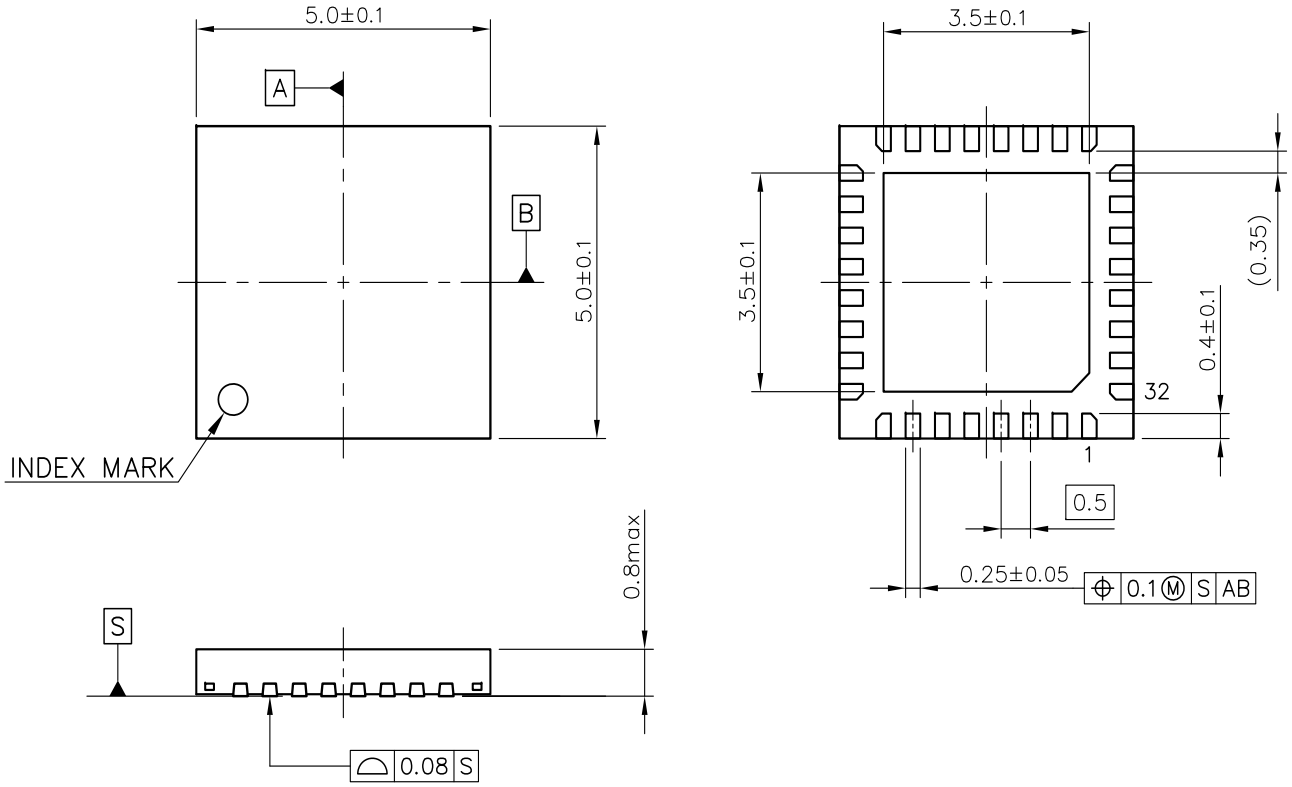
Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

RICOH

DM-QFN0505-32C-JE-A



QFN0505-32C Package Dimensions (Unit: mm)

RICOH

1. The products and the product specifications described in this document are subject to change or discontinuation of production without notice for reasons such as improvement. Therefore, before deciding to use the products, please refer to Ricoh sales representatives for the latest information thereon.
2. The materials in this document may not be copied or otherwise reproduced in whole or in part without prior written consent of Ricoh.
3. Please be sure to take any necessary formalities under relevant laws or regulations before exporting or otherwise taking out of your country the products or the technical information described herein.
4. The technical information described in this document shows typical characteristics of and example application circuits for the products. The release of such information is not to be construed as a warranty of or a grant of license under Ricoh's or any third party's intellectual property rights or any other rights.
5. The products listed in this document are intended and designed for use as general electronic components in standard applications (office equipment, telecommunication equipment, measuring instruments, consumer electronic products, amusement equipment etc.). Those customers intending to use a product in an application requiring extreme quality and reliability, for example, in a highly specific application where the failure or misoperation of the product could result in human injury or death (aircraft, spacevehicle, nuclear reactor control system, traffic control system, automotive and transportation equipment, combustion equipment, safety devices, life support system etc.) should first contact us.
6. We are making our continuous effort to improve the quality and reliability of our products, but semiconductor products are likely to fail with certain probability. In order to prevent any injury to persons or damages to property resulting from such failure, customers should be careful enough to incorporate safety measures in their design, such as redundancy feature, fire containment feature and fail-safe feature. We do not assume any liability or responsibility for any loss or damage arising from misuse or inappropriate use of the products.
7. Anti-radiation design is not implemented in the products described in this document.
8. The X-ray exposure can influence functions and characteristics of the products. Confirm the product functions and characteristics in the evaluation stage.
9. WLCSP products should be used in light shielded environments. The light exposure can influence functions and characteristics of the products under operation or storage.
10. There can be variation in the marking when different AOI (Automated Optical Inspection) equipment is used. In the case of recognizing the marking characteristic with AOI, please contact Ricoh sales or our distributor before attempting to use AOI.
11. Please contact Ricoh sales representatives should you have any questions or comments concerning the products or the technical information.

RoHS Compliant
Halogen Free

Ricoh is committed to reducing the environmental loading materials in electrical devices with a view to contributing to the protection of human health and the environment.
Ricoh has been providing RoHS compliant products since April 1, 2006 and Halogen-free products since April 1, 2012.

RICOH ELECTRONIC DEVICES CO., LTD.

Official website
https://www.n-redc.co.jp/en/
Contact us
https://www.n-redc.co.jp/en/buy/

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Ricoh Electronics:

R5602L001AA-E2