R1243S001C050-EV

30 V Input 2 A Buck DC/DC Converter Evaluation Board

NO.EEV-206-S001C050-200708

R1243S001C050-EV is the evaluation board for R1243 which has the below features. benefits and specifications.

OUTLINE

The R1243S is a CMOS-based step-down DC/DC converter with internal Nch high-side Tr. (0.175Ω) , which can provide the maximum 2 A output current. Internally, the R1243S consists of an oscillator, a PWM control circuit, a reference voltage unit, an error amplifier, phase compensation circuits, a slope circuit, a soft-start circuit, protection circuits, internal voltage regulators and a switch for bootstrap circuit. A step-down DC/DC converter can be configured by only adding an inductor, resistors, a diode and capacitors to the R1243S. The R1243S is a current mode operating type DC/DC converter that does not require external current sense resistor. It has high-speed response time and is high efficiency and compatible with ceramic capacitors. The oscillator frequency of the R1243S001C is fixed 330 kHz. The R1243S has a cycle-by-cycle peak current limit function, a short protection function, a thermal shutdown function and an UVLO as protection features. The R1243S001C has a latch protection with 2 ms delay time. The R1243S has a built-in soft-start time (Typ. 0.4 ms). In addition to this, the soft-start time is adjustable by adding an external capacitor. The R1243S has the FLG pin, which mainly monitors the FB pin voltage and gives a flag output by the Nch open drain if the abnormal condition is detected.

FEATURES

•	Operating Voltage Range	. 4.5 V to 30 V
•	Standby Current	
•	Supply Current	
•	Output Voltage	
•	Feedback Voltage	. 0.5 V with 1.4% accuracy
•	Output Current	. Max. 2 A ⁽¹⁾
•	Peak Current Limiting	
•	Internal Nch MOSFET Driver	. Typ. 175 mΩ
•	Maximum Duty Cycle	. Min. 85%
•	Oscillator Frequency	. 330 kHz
•	Latch Type Protection	. Typ. 2 ms
•	Internal Soft-start Time	. Typ. 0.4 ms, TSS = Open
•	External Soft-start Time	. Typ. 12 ms, Css = 0.1 μF
•	Flag Output	. Typ. 0.25 ms, FLG "OFF" delay time
•	UVLO Released Voltage	. Typ. 4.0 V
•	Thermal Shutdown	. Typ. 160°C, Hysteresis = 35°C
•	Package	. HSOP-8E
•	For more details on R1243 IC, please refer to	
	https://www.n-redc.co.jp/en/pdf/datasheet/r124	13-ea.pdf

⁽¹⁾ This is an approximate value, because output current depends on conditions and external parts.

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PART NUMBER INFORMATION

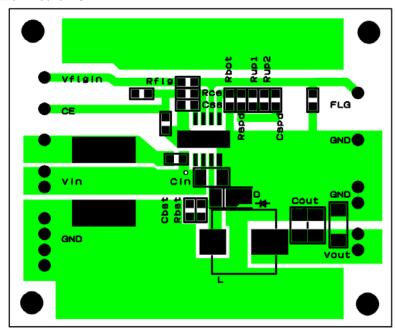
Product Name	Package
R1243S001C050	HSOP-8E

001C: 300 kHz, Fixed Frequency / Latch Type (2 ms)

050: 5.0 V, Output Voltage

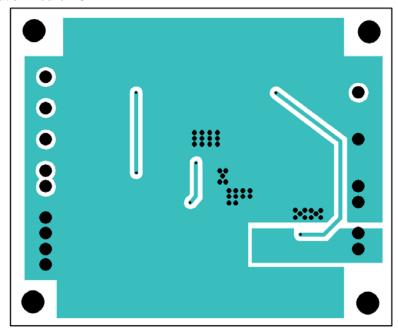
PCB LAYOUT

R1243S001C Evaluation Board TOP VIEW

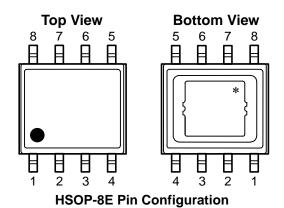


(The broad land of Lx section enables a connection with large inductors and diodes).

R1243S001C Evaluation Board TOP VIEW



PIN DESCRIPTION



* The tab is substrate level (GND). It must be connected to the GND level.

R1243S Pin Description

Pin No	Symbol	Pin Description
1	BST	Bootstrap Pin
2	VIN	Power Supply Pin
3	LX	LX Switching Pin
4	GND	Ground Pin
5	FB	Feedback Pin
6	FLG	Flag Output Pin
7	CE	Chip Enable Pin, Active with "H"
8	TSS	Soft-start Pin

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings

(GND = 0 V)

Symbol	Parameter		Rating		Unit
VIN	Input Voltage	-0.:	3 V to 32 V		V
V _{BST}	Boost Pin Voltage	V _L x −0.3	3 V to V _{LX} + 6 V		V
V_{LX}	LX Pin Voltage	-0.3	V to V _{IN} + 0.3		V
Vce	CE Pin Input Voltage	-0.3	V to V _{IN} + 0.3		V
V_{FB}	VFB Pin Voltage	-0.3 V to 6 V		V	
V _{FLG}	FLG Pin Voltage	-0.3 V to 6 V		V	
V _{TSS}	TSS Pin Voltage	-0.	-0.3 V to 6 V		V
P_D	Power Dissipation ⁽¹⁾	HSOP-8E	JEDEC STD. 51-7	2900	mW
Tj	Junction Temperature Range	-,	40 to 125		°C
Tstg	Storage Temperature Range	-!	55 to 125		°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings are not assured.

RECOMMENDED OPERATING CONDITIONS

Recommended Operating Conditions

Recommended Operating Conditions				
Symbol	Parameter	Rating	Unit	
VIN	Operating Input Voltage	4.5 to 30	V	
Та	Operating Temperature Range	−40 to 85	°C	

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

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⁽¹⁾ Refer to DATASHEET POWER DISSIPATION for detailed information.

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ELECTRICAL CHARACTERISTICS

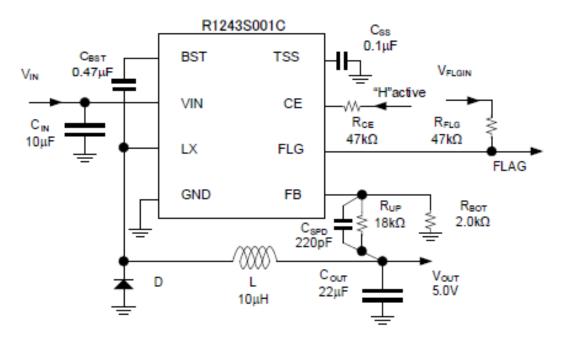
 $V_{IN} = 12 \text{ V}$, unless otherwise noted.

Electrical Characteristics

(Ta = 25°C)

					(' '	<u> </u>
Symbol	Parameter	Test Conditions/Comments	Min.	Тур.	Max.	Unit
Istandby	Standby Current	V _{IN} = 30 V, V _{CE} = 0 V		0	10	μА
Iss	Supply Current	V _{IN} = 30 V, V _{FB} = 1.0 V		0.7	1.0	mA
V _{UVLO1}	UVLO Detector Threshold	Falling	3.6	3.8	4.0	V
V _{UVLO2}	UVLO Released Voltage	Rising	3.8	4.0	4.2	V
Vuvlohys	UVLO Hysteresis	V _{UVLO2} – V _{UVLO1}		0.2		V
V_{FB}	Feedback Voltage		0.493	0.500	0.507	V
ΔV _{FB} /ΔTa	Feedback Voltage Temperature Coefficient	-40°C ≤ Ta ≤ 85°C		±100		ppm /ºC
fosc	Oscillator Frequency		290	330	370	kHz
Maxduty	Oscillator Maximum Duty Cycle	V _{IN} = 6 V	85	90	95	%
I _{TSS}	TSS Pin Current	V _{TSS} = 0 V		4.0		μΑ
t _{SS1}	Soft-start Time 1	TSS = open	0.2	0.4	0.8	ms
t _{SS2}	Soft-start Time 2	Css = 0.1 µF	6	12	18	ms
t _{DLY}	Latch Protection Delay Time	V _{IN} = 5.0 V		2.0		ms
I _{LXHOFF}	Highside Switch Leakage Current	$V_{IN} = 30 \text{ V}, V_{CE} = 0 \text{ V}$		0	10	μΑ
R_{LXH}	Highside Switch ON Resistance	$V_{BST} - V_{LX} = 4.5 \text{ V}$		175		mΩ
ILIMLXH	Highside Switch Limited Current	$V_{BST} - V_{LX} = 4.5 \text{ V}$	2.8	3.8		Α
Vceh	CE "H" Input Voltage	V _{IN} = 30 V	1.4			V
Vcel	CE "L" Input Voltage	V _{IN} = 30 V			0.4	V
Ісен	CE "H" Input Current	$V_{IN} = 30 \text{ V}, V_{CE} = 30 \text{ V}$	-1.0	0	1.0	μΑ
ICEL	CE "L" Input Current	V _{IN} = 30 V, V _{CE} = 0 V	-1.0	0	1.0	μΑ
I _{FBH}	FB "H" Input Current	V _{FB} = 2.0 V	-1.0	0	1.0	μА
I _{FBL}	FB "L" Input Current	V _{FB} = 0 V	-1.0	0	1.0	μА
T _{TSD}	Thermal Shutdown Detect Temperature	Hysteresis 35°C		160		°C
V _{FLGL}	FLG "L" Voltage	I _{FLG} = 1 mA			0.4	V
I _{FLGOFF}	FLG "OFF" Current	V _{FLG} = 5.5 V		0.0	1.0	μА
trlgoff	FLG "OFF" Delay Time		0.05	0.25	0.60	ms
Vovd	Overvoltage Detection Voltage	V _{FB}	0.55	0.60	0.65	V
V _{UVD}	Undervoltage Detection Voltage	V _{FB}	0.35	0.40	0.45	V

APPLICATION INFORMATION



R1243S001C050 Typical Application

R1243S001C050 Recommended External Components(1)

C _{IN} [μF]	Соυт [μF]	C _{BST} [μF]	C _{SPD} [pF]	Css [μF]	L [μH]	D [V / A]
10	22	0.47	220	0.1	10	40 / 3
Rce [kΩ]	R _{FLG} [kΩ]	Rup[kΩ]	R вот [kΩ]			
47.0	47.0	18.0	2.0			

⁽¹⁾The bill of materials will be attached on the shipment of each purchased evaluation board.

TECHNICAL NOTES ON PCB LAYOUT PATTERN

- The exposed pad on the bottom of the package enhances the thermal performance and is electrically connected to GND inside the package. It is recommended that the exposed pad be connected to the ground plane on the board with thermal vias if possible.
- 2. Connect shortest possible: "a wiring between the V_{IN} pin of input capacitor (C_{IN}) and the V_{IN} pin of IC" and "a wiring between the GND pin of input capacitor (C_{IN}) and the GND pin of IC".
 - Connect as short as possible: "a wiring among the Lx pin of IC, the Lx pin of diode, the GND pin of diode, and the GND pin of input capacitor (C_{IN})".
 - These are recommended to wire without intermediary of a through hole.
- 3. Wire the Lx pin short so that the parasitic capacitance would not be provided. It is recommended to implement without intermediary of a through hole.
- 4. Connect between the GND pin of C_{OUT} and the GND pin of diode as short as possible. It is recommended to wire without intermediary of a through hole.
- 5. The FB pin side of R_{UP}, R_{BOT}, C_{SPD}, and R_{SPD} should be designed to keep a distance from inductor, BST pin, and Lx pin in order to avoid the high impedance and noise effect. These can be wired via through hole.
- 6. For V_{OUT} wiring to R_{UP}, the feed-back must be made as close as possible from the output capacitor (C_{OUT}). This can be wired via through hole.
- 7. For the GND wiring to the soft-start time adjusting capacitor (C_{SS}), avoid the current path of parts including input capacitors (C_{IN}) and diodes. This can be wired via through hole.



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