100-Pin TQFP
Commercial Temp
Industrial Temp

2M x 18, 1M x 32, 1M x 36 36Mb Sync Burst SRAMs

400 MHz–150 MHz
2.5 V or 3.3 V V_{DD}
2.5 V or 3.3 V I/O

Features

- $\overline{\text{FT}}$ pin for user-configurable flow through or pipeline operation
- Single Cycle Deselect (SCD) operation
- 2.5 V or 3.3 V +10%/–10% core power supply
- 2.5 V or 3.3 V I/O supply
- $\overline{\text{LBO}}$ pin for Linear or Interleaved Burst mode
- Internal input resistors on mode pins allow floating mode pins
- Default to Interleaved Pipeline mode
- Byte Write ($\overline{\text{BW}}$) and/or Global Write ($\overline{\text{GW}}$) operation
- Internal self-timed write cycle
- Automatic power-down for portable applications
- RoHS-compliant 100-lead TQFP package

Functional Description

Applications

The GS832018/32/36AGT is a 37,748,736-bit high performance synchronous SRAM with a 2-bit burst address counter. Although of a type originally developed for Level 2 Cache applications supporting high performance CPUs, the device now finds application in synchronous SRAM applications, ranging from DSP main store to networking chip set support.

Controls

Addresses, data I/Os, chip enables ($\overline{\text{E1}}$, E2, $\overline{\text{E3}}$), address burst control inputs ($\overline{\text{ADSP}}$, $\overline{\text{ADSC}}$, $\overline{\text{ADV}}$), and write control inputs ($\overline{\text{Bx}}$, $\overline{\text{BW}}$, $\overline{\text{GW}}$) are synchronous and are controlled by a positive-edge-triggered clock input (CK). Output enable ($\overline{\text{G}}$) and power down control (ZZ) are asynchronous inputs. Burst cycles can be initiated with either $\overline{\text{ADSP}}$ or $\overline{\text{ADSC}}$ inputs. In Burst mode, subsequent burst addresses are generated internally and are controlled by $\overline{\text{ADV}}$. The burst address counter may be configured to count in either linear or interleave order with the Linear Burst Order ($\overline{\text{LBO}}$) input. The Burst function need not be used. New addresses can be loaded on every cycle with no degradation of chip performance.

Flow Through/Pipeline Reads

The function of the Data Output register can be controlled by the user via the $\overline{\text{FT}}$ mode pin (Pin 14). Holding the $\overline{\text{FT}}$ mode pin low places the RAM in Flow Through mode, causing output data to bypass the Data Output Register. Holding $\overline{\text{FT}}$ high places the RAM in Pipeline mode, activating the rising-edge-triggered Data Output Register.

Byte Write and Global Write

Byte write operation is performed by using Byte Write enable ($\overline{\text{BW}}$) input combined with one or more individual byte write signals ($\overline{\text{Bx}}$). In addition, Global Write ($\overline{\text{GW}}$) is available for writing all bytes at one time, regardless of the Byte Write control inputs.

Sleep Mode

Low power (Sleep mode) is attained through the assertion (High) of the ZZ signal, or by stopping the clock (CK). Memory data is retained during Sleep mode.

Core and Interface Voltages

The GS832018/32/36AGT operates on a 3.3 V or 2.5 V power supply. All input are 3.3 V and 2.5 V compatible. Separate output power (V_{DDQ}) pins are used to decouple output noise from the internal circuits and are 3.3 V and 2.5 V compatible.

Parameter Synopsis

		-400	-375	-333	-250	-200	-150	Unit
Pipeline 3-1-1-1	t_{KQ}	2.5	2.5	2.5	2.5	3.0	3.8	ns
	tCycle	2.5	2.66	3.3	4.0	5.0	6.7	ns
	Curr (x18)	395	390	355	280	240	205	mA
	Curr (x32/x36)	475	455	415	335	280	230	mA
Flow Through 2-1-1-1	t_{KQ}	4.0	4.2	4.5	5.5	6.5	7.5	ns
	tCycle	4.0	4.2	4.5	5.5	6.5	7.5	ns
	Curr (x18)	290	275	260	235	200	190	mA
	Curr (x32/x36)	335	320	305	270	240	220	mA

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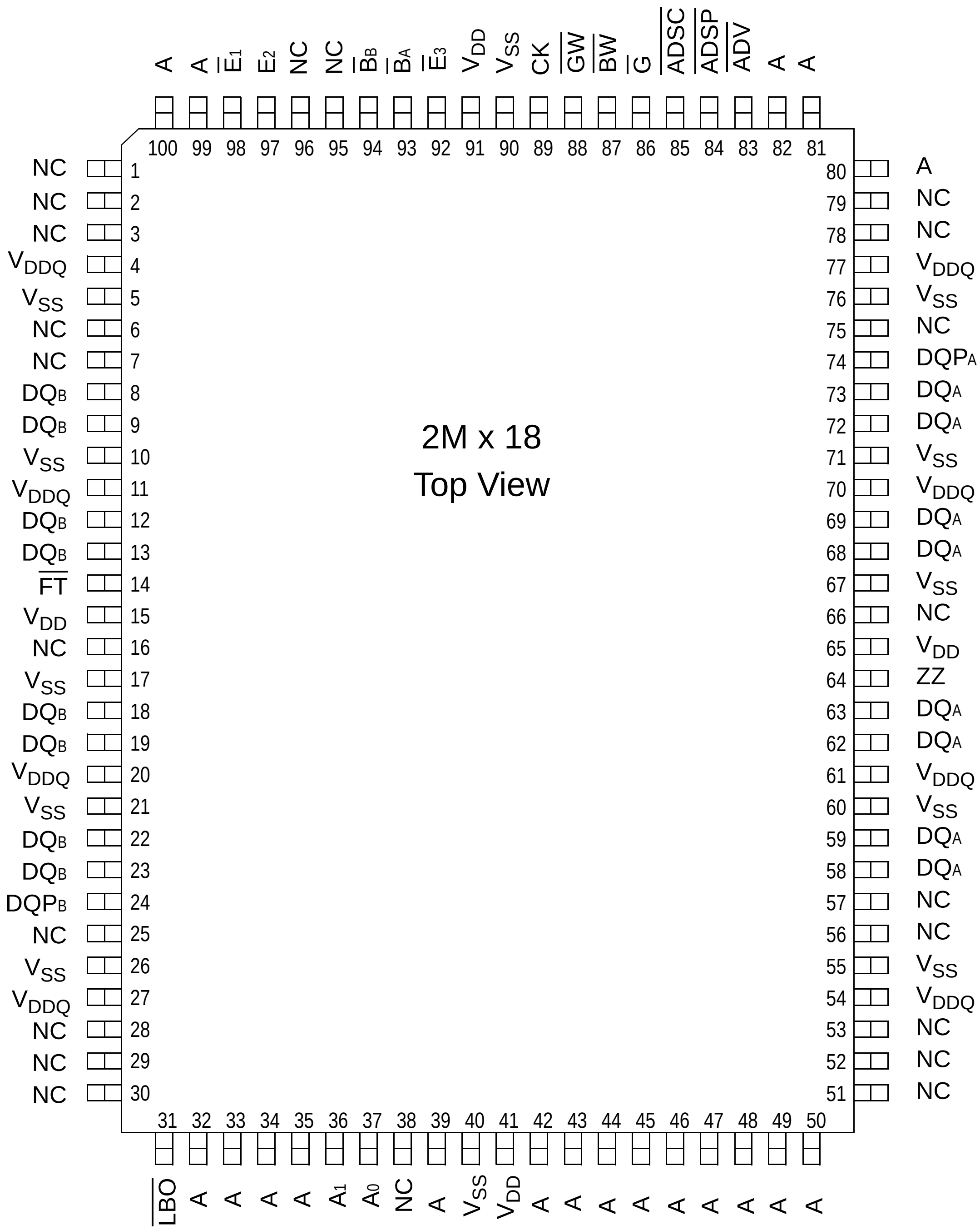
GS832018AGT 100-Pin TQFP Pinout



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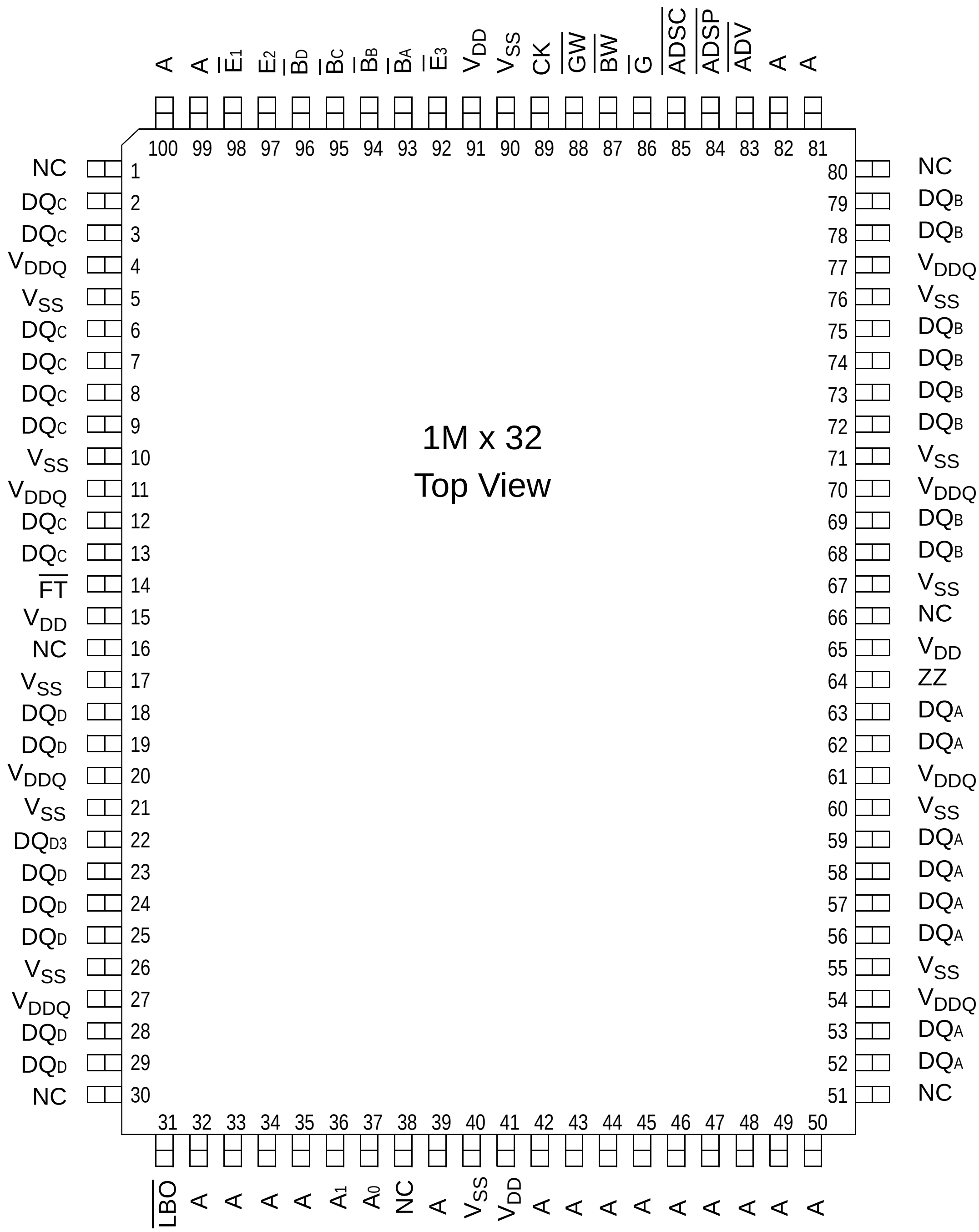
GS832032AGT 100-Pin TQFP Pinout



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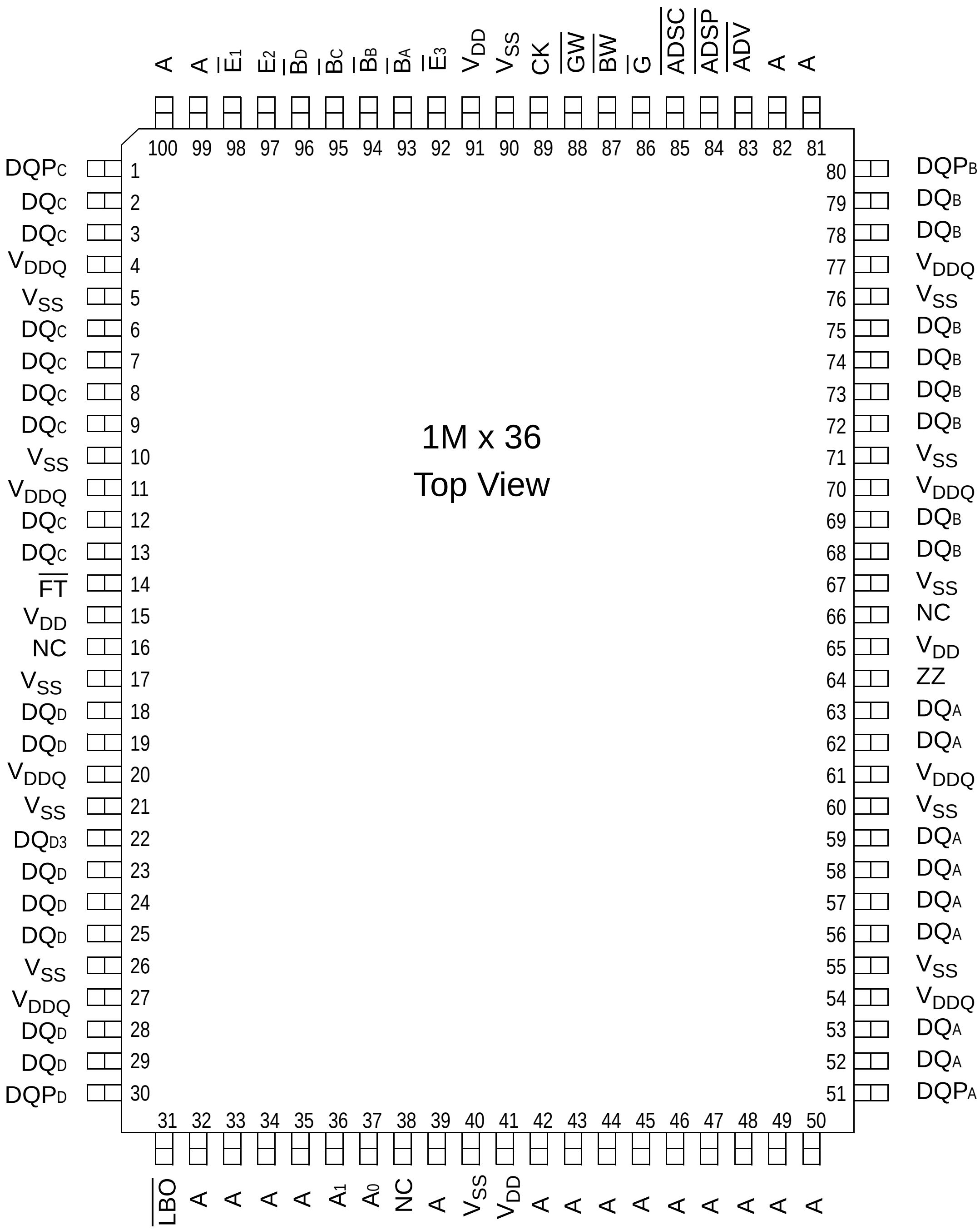
GS832036AGT 100-Pin TQFP Pinout



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TQFP Pin Description

Symbol	Type	Description
A_0, A_1	I	Address field LSBs and Address Counter preset Inputs
A	I	Address Inputs
DQ_A DQ_B DQ_C DQ_D	I/O	Data Input and Output pins
$\overline{BW}$	I	Byte Write—Writes all enabled bytes; active low
$\overline{B}_A$, $\overline{B}_B$	I	Byte Write Enable for DQ_A, DQ_B Data I/Os; active low
$\overline{B}_C$, $\overline{B}_D$	I	Byte Write Enable for DQ_C, DQ_D Data I/Os; active low
CK	I	Clock Input Signal; active high
$\overline{GW}$	I	Global Write Enable—Writes all bytes; active low
$\overline{E}_1$, $\overline{E}_3$	I	Chip Enable; active low
E_2	I	Chip Enable; active high
$\overline{G}$	I	Output Enable; active low
$\overline{ADV}$	I	Burst address counter advance enable; active low
$\overline{ADSP}$, $\overline{ADSC}$	I	Address Strobe (Processor, Cache Controller); active low
ZZ	I	Sleep Mode control; active high
$\overline{FT}$	I	Flow Through or Pipeline mode; active low
$\overline{LBO}$	I	Linear Burst Order mode; active low
V_{DD}	I	Core power supply
V_{SS}	I	I/O and Core Ground
V_{DDQ}	I	Output driver power supply
NC		No Connect

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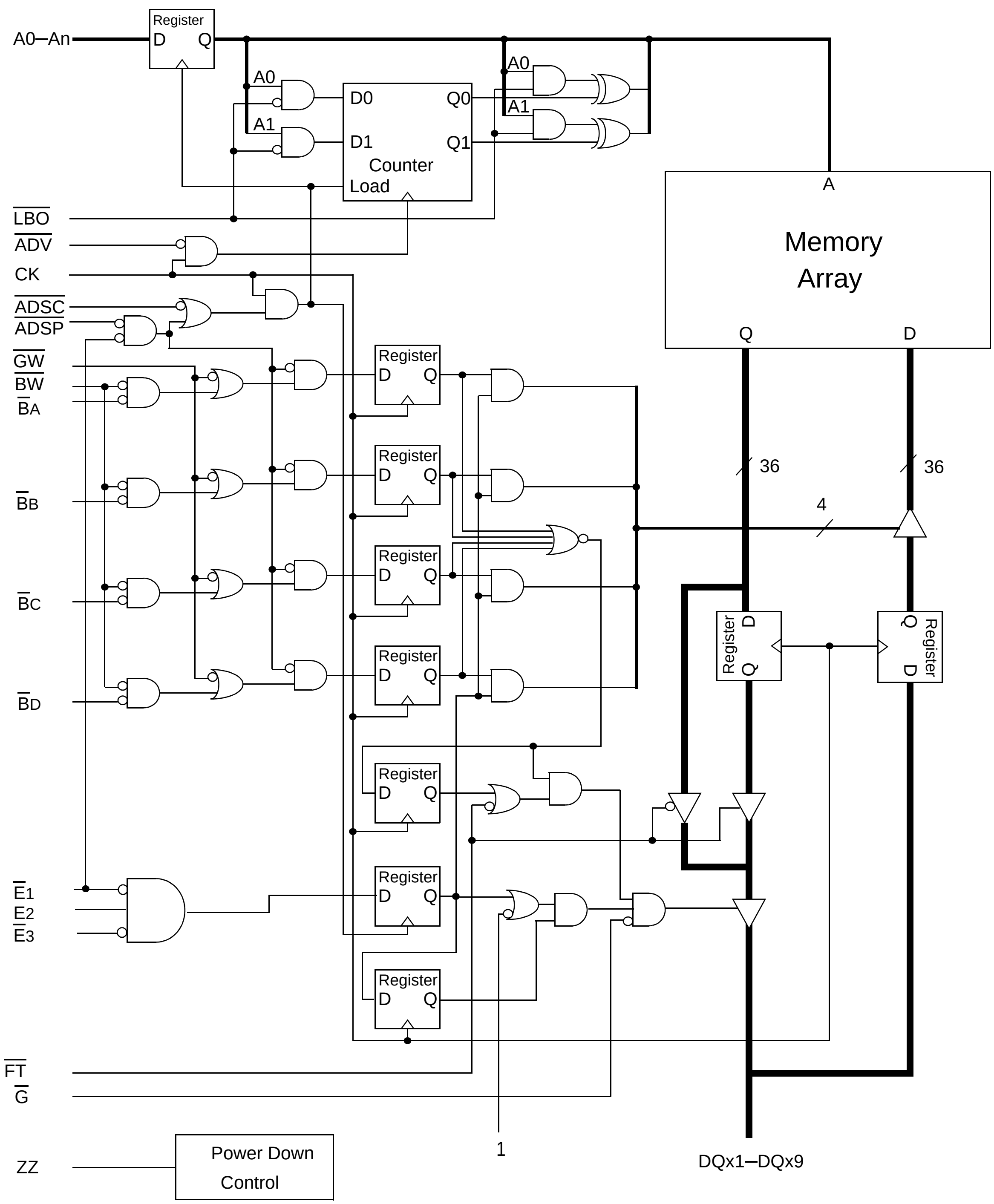
GS832018/32/36AGT Block Diagram



Note: Only x36 version shown for simplicity.

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Mode Pin Functions

Mode Name	Pin Name	State	Function
Burst Order Control	$\overline{LBO}$	L	Linear Burst
		H	Interleaved Burst
Output Register Control	$\overline{FT}$	L	Flow Through
		H or NC	Pipeline
Power Down Control	ZZ	L or NC	Active
		H	Standby, $I_{DD} = I_{SB}$

Note:
There is a pull-up device on the $\overline{FT}$ pin and a pull-down device on the ZZ pin , so this input pin can be unconnected and the chip will operate in the default states as specified in the above tables.

Burst Counter Sequences

Linear Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	10	11	00
3rd address	10	11	00	01
4th address	11	00	01	10

Note:
The burst counter wraps to initial state on the 5th clock.

Interleaved Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	00	11	10
3rd address	10	11	00	01
4th address	11	10	01	00

Note:
The burst counter wraps to initial state on the 5th clock.

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Byte Write Truth Table

Function	$\overline{GW}$	$\overline{BW}$	$\overline{B_A}$	$\overline{B_B}$	$\overline{B_C}$	$\overline{B_D}$	Notes
Read	H	H	X	X	X	X	1
Write No Bytes	H	L	H	H	H	H	1
Write byte a	H	L	L	H	H	H	2, 3
Write byte b	H	L	H	L	H	H	2, 3
Write byte c	H	L	H	H	L	H	2, 3, 4
Write byte d	H	L	H	H	H	L	2, 3, 4
Write all bytes	H	L	L	L	L	L	2, 3, 4
Write all bytes	L	X	X	X	X	X	

Notes:
1. All byte outputs are active in read cycles regardless of the state of Byte Write Enable inputs, $\overline{B_A}$, $\overline{B_B}$, $\overline{B_C}$ and/or $\overline{B_D}$.
2. Byte Write Enable inputs $\overline{B_A}$, $\overline{B_B}$, $\overline{B_C}$ and/or $\overline{B_D}$ may be used in any combination with $\overline{BW}$ to write single or multiple bytes.
3. All byte I/Os remain High-Z during all write operations regardless of the state of Byte Write Enable inputs.
4. Bytes “C” and “D” are only available on the x32 and x36 versions.

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Synchronous Truth Table

Operation	Address Used	State Diagram Key	$\overline{E1}$	E2	$\overline{E3}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{W}$	DQ[3]
Deselect Cycle, Power Down	None	X	L	X	H	X	L	X	X	High-Z
Deselect Cycle, Power Down	None	X	L	L	X	X	L	X	X	High-Z
Deselect Cycle, Power Down	None	X	L	X	H	L	X	X	X	High-Z
Deselect Cycle, Power Down	None	X	L	L	X	L	X	X	X	High-Z
Deselect Cycle, Power Down	None	X	H	X	X	X	L	X	X	High-Z
Read Cycle, Begin Burst	External	R	L	H	L	L	X	X	X	Q
Read Cycle, Begin Burst	External	R	L	H	L	H	L	X	F	Q
Write Cycle, Begin Burst	External	W	L	H	L	H	L	X	T	D
Read Cycle, Continue Burst	*Next*	*CR*	*X*	*X*	*X*	*H*	*H*	*L*	*F*	*Q*
Read Cycle, Continue Burst	Next	CR	H	X	X	X	H	L	F	Q
Write Cycle, Continue Burst	*Next*	*CW*	*X*	*X*	*X*	*H*	*H*	*L*	*T*	*D*
Write Cycle, Continue Burst	Next	CW	H	X	X	X	H	L	T	D
Read Cycle, Suspend Burst	Current		X	X	X	H	H	H	F	Q
Read Cycle, Suspend Burst	Current		H	X	X	X	H	H	F	Q
Write Cycle, Suspend Burst	Current		X	X	X	H	H	H	T	D
Write Cycle, Suspend Burst	Current		H	X	X	X	H	H	T	D

Notes:
1. X = Don't Care, H = High, L = Low
2. E = T (True) if E_2 = 1 and $\overline{E}_1 = \overline{E}_3$ = 0; E = F (False) if E_2 = 0 or $\overline{E}_1$ = 1 or $\overline{E}_3$ = 1
3. $\overline{W}$ = T (True) and F (False) is defined in the Byte Write Truth Table preceding.
4. $\overline{G}$ is an asynchronous input. $\overline{G}$ can be driven high at any time to disable active output drivers. $\overline{G}$ low can only enable active drivers (shown as "Q" in the Truth Table above).
5. All input combinations shown above are tested and supported. Input combinations shown in gray boxes need not be used to accomplish basic synchronous or synchronous burst operations and may be avoided for simplicity.
6. Tying $\overline{ADSP}$ high and $\overline{ADSC}$ low allows simple non-burst synchronous operations. See **BOLD** items above.
7. Tying $\overline{ADSP}$ high and $\overline{ADV}$ low while using $\overline{ADSC}$ to load new addresses allows simple burst operations. See *ITALIC* items above.

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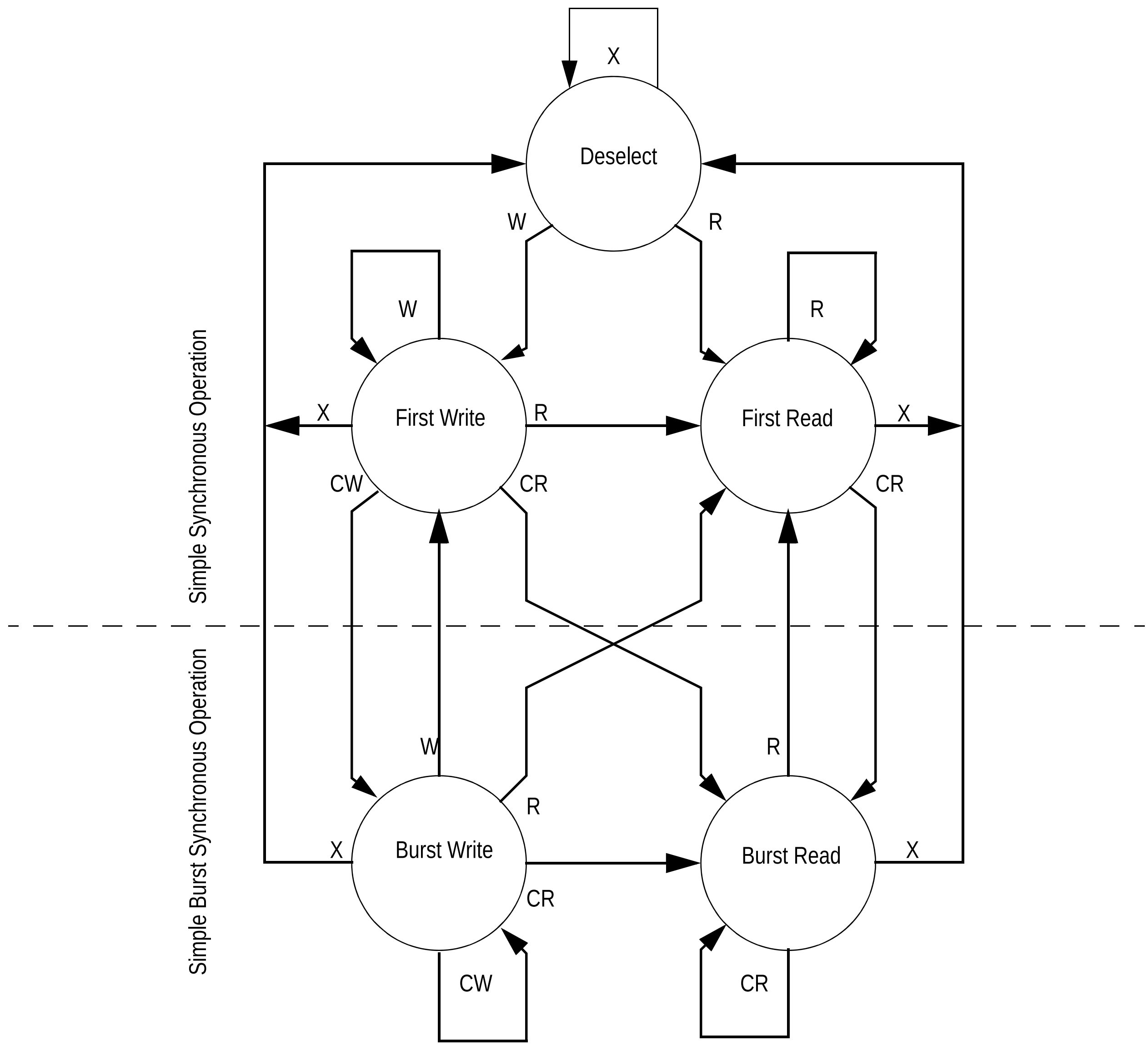
Simplified State Diagram



Notes:

1. The diagram shows only supported (tested) synchronous state transitions. The diagram presumes $\overline{\mathrm{G}}$ is tied low.
2. The upper portion of the diagram assumes active use of only the Enable ($\overline{\mathrm{E1}}$, E2, and $\overline{\mathrm{E3}}$) and Write ($\overline{\mathrm{B_A}}$, $\overline{\mathrm{B_B}}$, $\overline{\mathrm{B_C}}$, $\overline{\mathrm{B_D}}$, $\overline{\mathrm{BW}}$, and $\overline{\mathrm{GW}}$) control inputs, and that $\overline{\mathrm{ADSP}}$ is tied high and $\overline{\mathrm{ADSC}}$ is tied low.
3. The upper and lower portions of the diagram together assume active use of only the Enable, Write, and $\overline{\mathrm{ADSC}}$ control inputs, and assumes $\overline{\mathrm{ADSP}}$ is tied high and $\overline{\mathrm{ADV}}$ is tied low.

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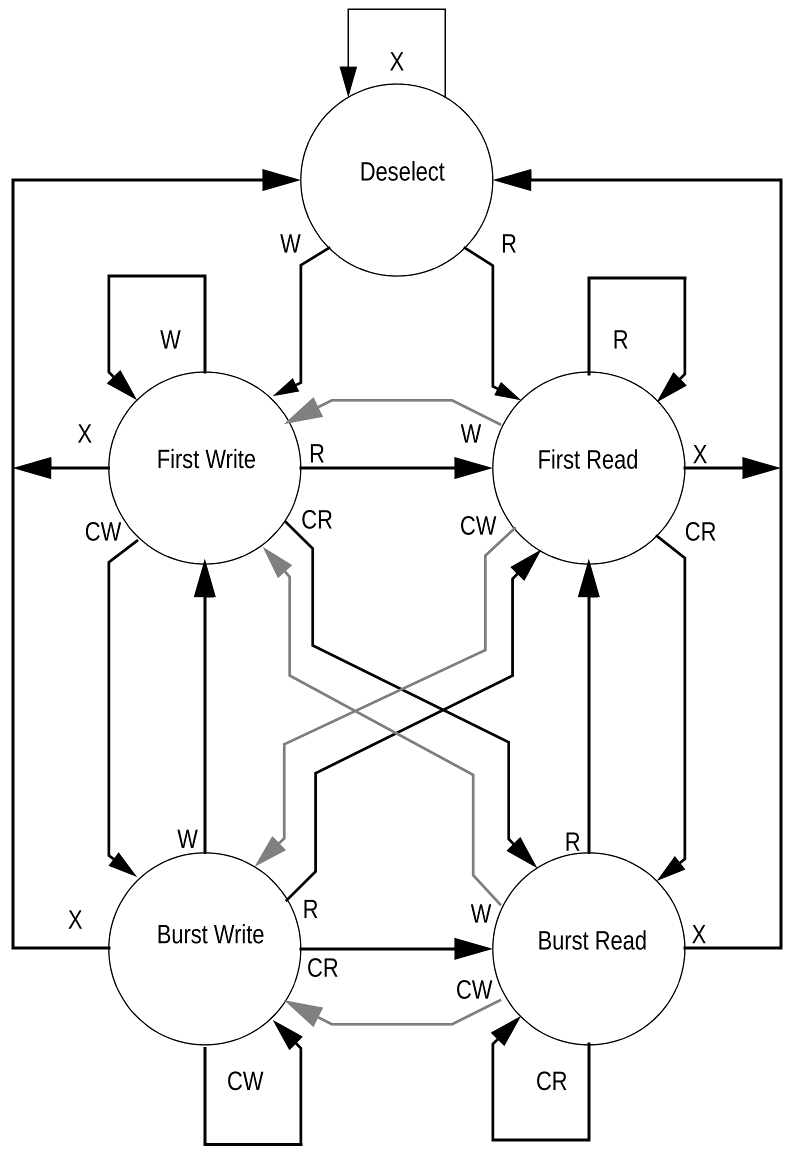
Simplified State Diagram with $\overline{G}$



Notes:

1. The diagram shows supported (tested) synchronous state transitions plus supported transitions that depend upon the use of $\overline{G}$.
2. Use of "Dummy Reads" (Read Cycles with $\overline{G}$ High) may be used to make the transition from Read cycles to Write cycles without passing through a Deselect cycle. Dummy Read cycles increment the address counter just like normal read cycles.
3. Transitions shown in gray tone assume $\overline{G}$ has been pulsed high long enough to turn the RAM's drivers off and for incoming data to meet Data Input Set Up Time.

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Absolute Maximum Ratings
(All voltages reference to V_{SS})

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	–0.5 to 4.6	V
V_{DDQ}	Voltage in V_{DDQ} Pins	–0.5 to V_{DD}	V
$V_{I/O}$	Voltage on I/O Pins	–0.5 to V_{DD} +0.5 (≤ 4.6 V max.)	V
V_{IN}	Voltage on Other Input Pins	–0.5 to V_{DD} +0.5 (≤ 4.6 V max.)	V
I_{IN}	Input Current on Any Pin	+/–20	mA
I_{OUT}	Output Current on Any I/O Pin	+/–20	mA
P_D	Package Power Dissipation	1.5	W
T_{STG}	Storage Temperature	–55 to 125	^oC
T_{BIAS}	Temperature Under Bias	–55 to 125	^oC

Note:
Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Absolute Maximum Ratings, for an extended period of time, may affect reliability of this component.

Power Supply Voltage Ranges

Parameter	Symbol	Min.	Typ.	Max.	Unit
3.3 V Supply Voltage	V_{DD3}	3.0	3.3	3.6	V
2.5 V Supply Voltage	V_{DD2}	2.3	2.5	2.7	V
3.3 V V_{DDQ} I/O Supply Voltage	V_{DDQ3}	3.0	3.3	3.6	V
2.5 V V_{DDQ} I/O Supply Voltage	V_{DDQ2}	2.3	2.5	2.7	V

V_{DD3} Range Logic Levels

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	2.0	—	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	–0.3	—	0.8	V

Notes:
1. V_{IH} (max) must be met for any instantaneous value of V_{DD}.
2. V_{DD} needs to power-up before or at the same time as V_{DDQ} to make sure V_{IH} (max) is not exceeded.

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V_{DD2} Range Logic Levels

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	$0.6*V_{DD}$	—	$V_{DD} + 0.3$	V
Input Low Voltage	V_{IL}	–0.3	—	$0.3*V_{DD}$	V

Notes:
1. V_{IH} (max) must be met for any instantaneous value of V_{DD}.
2. V_{DD} needs to power-up before or at the same time as V_{DDQ} to make sure V_{IH} (max) is not exceeded.

Operating Temperature

Parameter	Symbol	Min.	Typ.	Max.	Unit
Junction Temperature (Commercial Range Versions)	T_J	0	25	85	°C
Junction Temperature (Industrial Range Versions)*	T_J	–40	25	100	°C

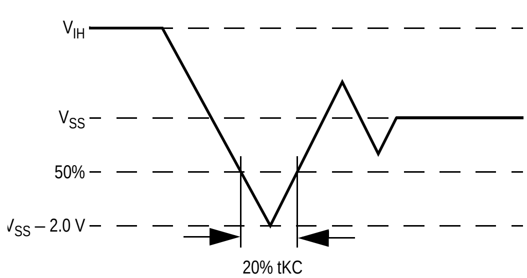
Note:
* The part numbers of Industrial Temperature Range versions end with the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.

Thermal Impedance

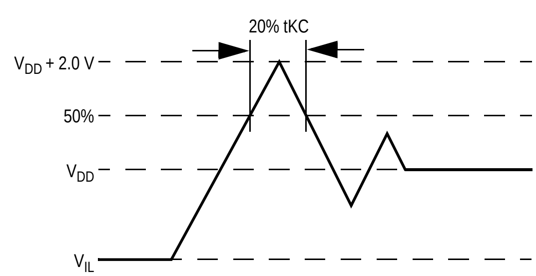
Package	Test PCB Substrate	θ JA (C°/W) Airflow = 0 m/s	θ JA (C°/W) Airflow = 1 m/s	θ JA (C°/W) Airflow = 2 m/s	θ JB (C°/W)	θ JC (C°/W)
100 TQFP	4-layer	28.7	23.8	22.3	15.1	6.5

Notes:
1. Thermal Impedance data is based on a number of of samples from mulitple lots and should be viewed as a typical number.
2. Please refer to JEDEC standard JESD51-6.
3. The characteristics of the test fixture PCB influence reported thermal characteristics of the device. Be advised that a good thermal path to the PCB can result in cooling or heating of the RAM depending on PCB temperature.

Undershoot Measurement and Timing



Overshoot Measurement and Timing



Note:
Input Under/overshoot voltage must be –2 V > Vi < V_{DDn}+2 V not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tKC.

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Capacitance

(T_A = 25°C, f = 1 MHz, V_{DD} = 2.5 V)

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	4	5	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT} = 0 V	6	7	pF

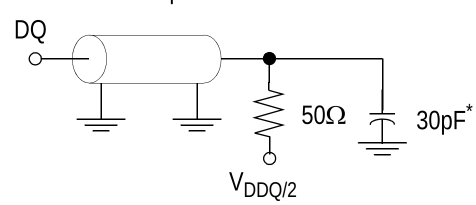
Note:
These parameters are sample tested.

AC Test Conditions

Parameter	Conditions
Input high level	V_{DD} – 0.2 V
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	V_{DD}/2
Output reference level	V_{DDQ}/2
Output load	Fig. 1

Notes:
1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted.
3. Device is deselected as defined by the Truth Table.

Output Load 1



* Distributed Test Jig Capacitance

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DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current (except mode pins)	I_{IL}	V_{IN} = 0 to V_{DD}	–1 uA	1 uA
ZZ Input Current	I_{IN1}	$V_{DD} \geq V_{IN} \geq V_{IH}$ $0\text{ V} \leq V_{IN} \leq V_{IH}$	–1 uA –1 uA	1 uA 100 uA
$\overline{FT}$ Input Current	I_{IN2}	$V_{DD} \geq V_{IN} \geq V_{IL}$ $0\text{ V} \leq V_{IN} \leq V_{IL}$	–100 uA –1 uA	1 uA 1 uA
Output Leakage Current	I_{OL}	Output Disable, V_{OUT} = 0 to V_{DD}	–1 uA	1 uA
Output High Voltage	V_{OH2}	I_{OH} = –8 mA, V_{DDQ} = 2.375 V	1.7 V	—
Output High Voltage	V_{OH3}	I_{OH} = –8 mA, V_{DDQ} = 3.135 V	2.4 V	—
Output Low Voltage	V_{OL}	I_{OL} = 8 mA	—	0.4 V

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Operating Currents

Parameter	Test Conditions	Mode		Symbol	-400		-375		-333		-250		-200		-150		Unit
					0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	
Operating Current	Device Selected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Output open	(x32/ x36)	Pipeline	I_{DD} I_{DDQ}	395 80	415 80	380 75	400 75	345 70	365 70	285 50	305 50	240 40	260 40	200 30	220 30	mA
			Flow Through	I_{DD} I_{DDQ}	285 50	305 50	270 50	290 50	260 45	280 45	230 40	250 40	205 35	225 35	190 30	210 30	mA
		(x18)	Pipeline	I_{DD} I_{DDQ}	355 40	375 40	350 40	370 40	320 35	340 35	255 25	275 25	220 20	240 20	190 15	210 15	mA
			Flow Through	I_{DD} I_{DDQ}	265 25	285 25	250 25	270 25	235 25	255 25	215 20	235 20	185 15	205 15	175 15	195 15	mA
Standby Current	$ZZ \geq V_{DD} - 0.2$ V	—	Pipeline	I_{SB}	55	75	55	75	55	75	55	75	55	75	55	75	mA
			Flow Through	I_{SB}	55	75	55	75	55	75	55	75	55	75	55	75	mA
Deselect Current	Device Deselected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$	—	Pipeline	I_{DD}	100	120	100	120	100	120	100	120	100	120	100	120	mA
			Flow Through	I_{DD}	100	120	100	120	100	120	100	120	100	120	100	120	mA

Notes:
1. I_{DD} and I_{DDQ} apply to any combination of V_{DD3}, V_{DD2}, V_{DDQ3}, and V_{DDQ2} operation.
2. All parameters listed are worst case scenario.

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AC Electrical Characteristics

	Parameter	Symbol	-400 Min	-400 Max	-375 Min	-375 Max	-333 Min	-333 Max	-250 Min	-250 Max	-200 Min	-200 Max	-150 Min	-150 Max	Unit
Pipeline	Clock Cycle Time	tKC	2.5	—	2.66	—	3.3	—	4.0	—	5.0	—	6.7	—	ns
	Clock to Output Valid	tKQ	—	2.5	—	2.5	—	2.5	—	2.5	—	3.0	—	3.8	ns
	Clock to Output Invalid	tKQX	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Clock to Output in Low-Z	tLZ[1]	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Setup time	tS	0.9	—	0.9	—	1.0	—	1.2	—	1.4	—	1.5	—	ns
	Hold time	tH	0.1	—	0.1	—	0.1	—	0.2	—	0.4	—	0.5	—	ns
Flow Through	Clock Cycle Time	tKC	4.0	—	4.2	—	4.5	—	5.5	—	6.5	—	7.5	—	ns
	Clock to Output Valid	tKQ	—	4.0	—	4.2	—	4.5	—	5.5	—	6.5	—	7.5	ns
	Clock to Output Invalid	tKQX	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
	Clock to Output in Low-Z	tLZ[1]	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
	Setup time	tS	1.2	—	1.2	—	1.3	—	1.5	—	1.5	—	1.5	—	ns
	Hold time	tH	0.2	—	0.2	—	0.3	—	0.5	—	0.5	—	0.5	—	ns
	Clock HIGH Time	tKH	0.9	—	0.9	—	1.0	—	1.3	—	1.3	—	1.5	—	ns
	Clock LOW Time	tKL	1.1	—	1.1	—	1.2	—	1.5	—	1.5	—	1.7	—	ns
	Clock to Output in High-Z	tHZ[1]	1.5	2.5	1.5	2.5	1.5	2.5	1.5	2.5	1.5	3.0	1.5	3.8	ns
	$\overline{G}$ to Output Valid	tOE	—	2.5	—	2.5	—	2.5	—	2.5	—	3.0	—	3.8	ns
	$\overline{G}$ to output in Low-Z	tOLZ[1]	0	—	0	—	0	—	0	—	0	—	0	—	ns
	$\overline{G}$ to output in High-Z	tOHZ[1]	—	2.5	—	2.5	—	2.5	—	2.5	—	3.0	—	3.8	ns
	ZZ setup time	tZZS[2]	5	—	5	—	5	—	5	—	5	—	5	—	ns
	ZZ hold time	tZZH[2]	1	—	1	—	1	—	1	—	1	—	1	—	ns
	ZZ recovery	tZZR	20	—	20	—	20	—	20	—	20	—	20	—	ns

Notes:
1. These parameters are sampled and are not 100% tested.
2. ZZ is an asynchronous signal. However, in order to be recognized on any given clock cycle, ZZ must meet the specified setup and hold times as specified above.

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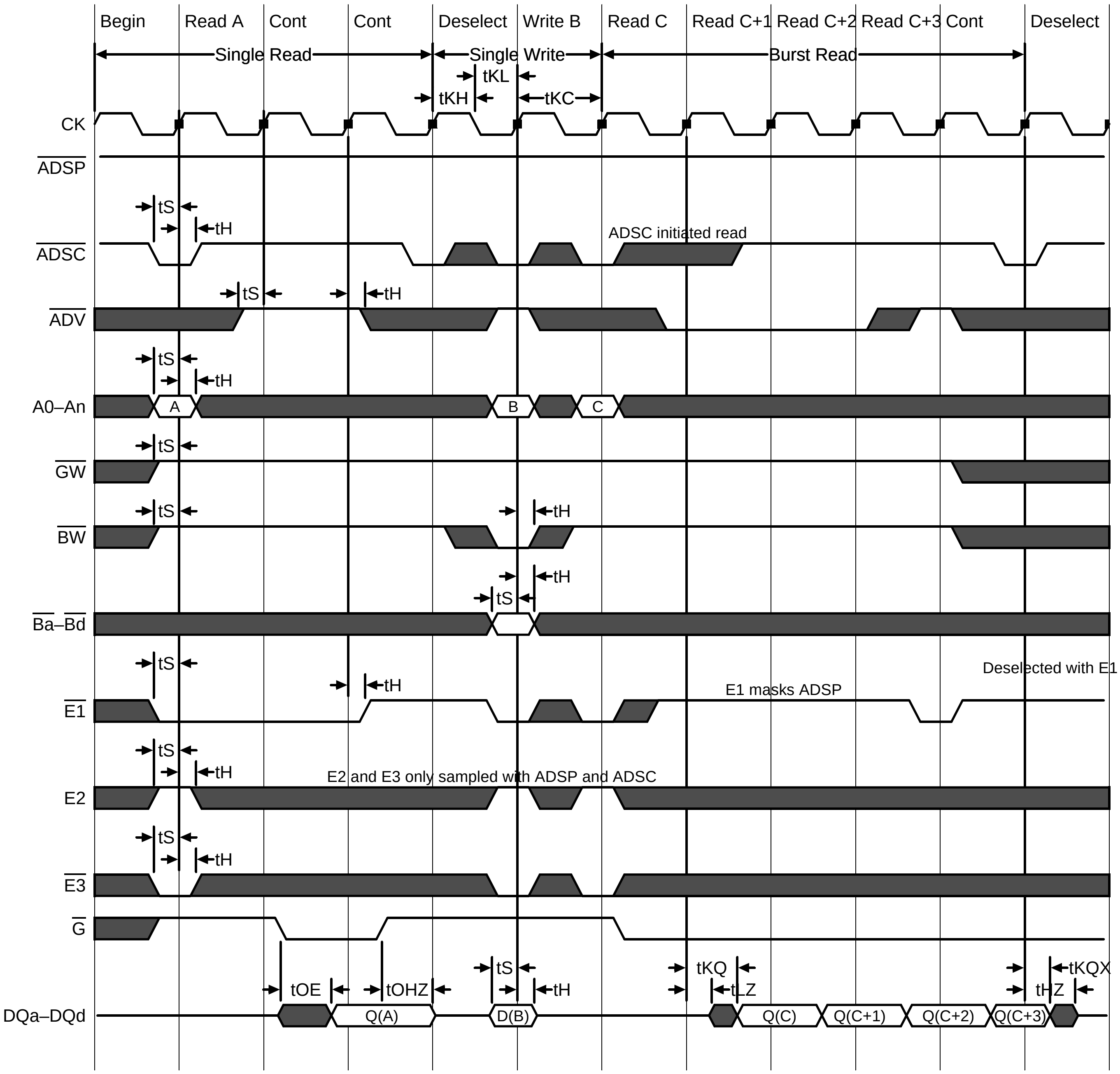
Pipeline Mode Timing



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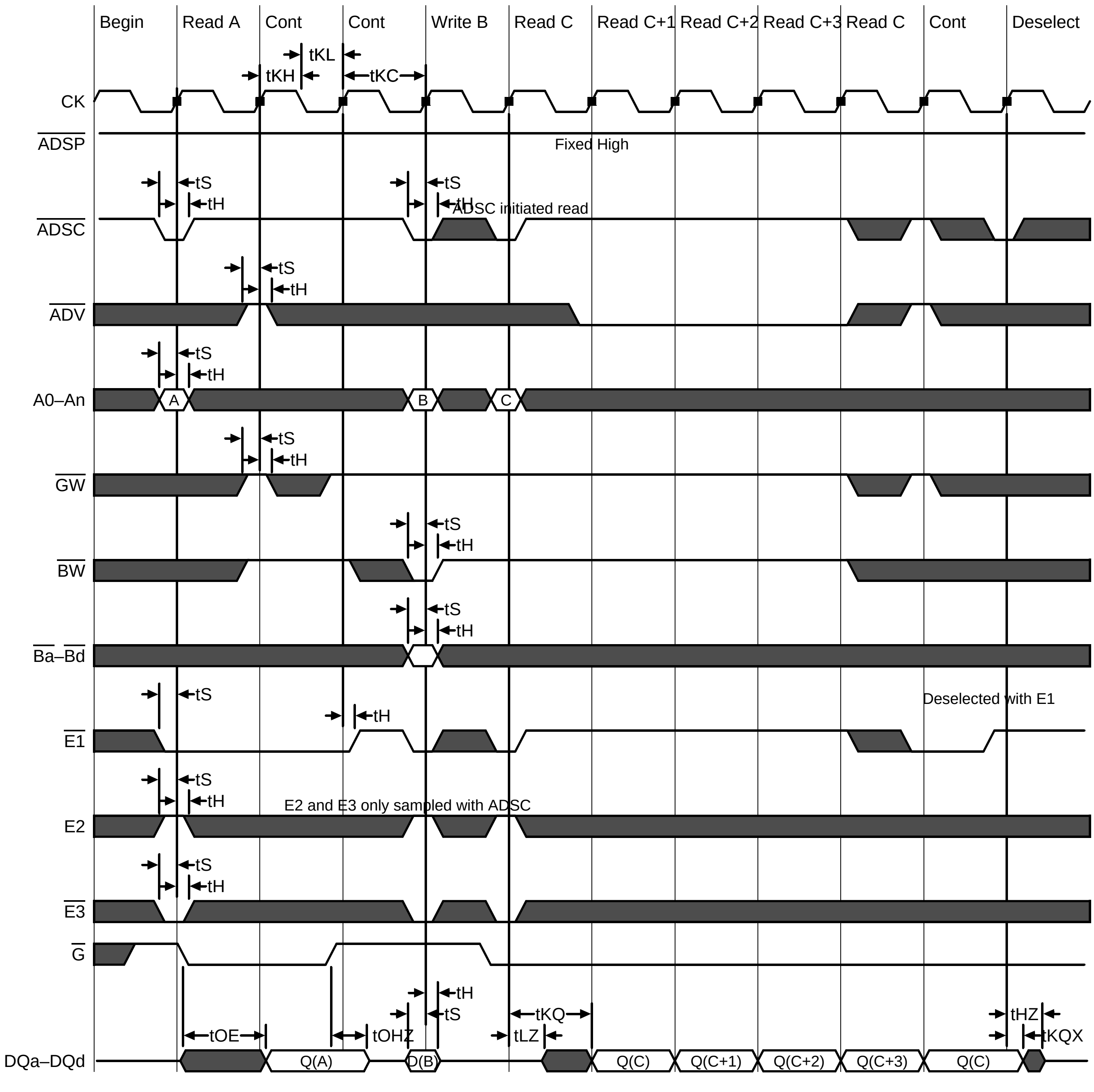
Flow Through Mode Timing



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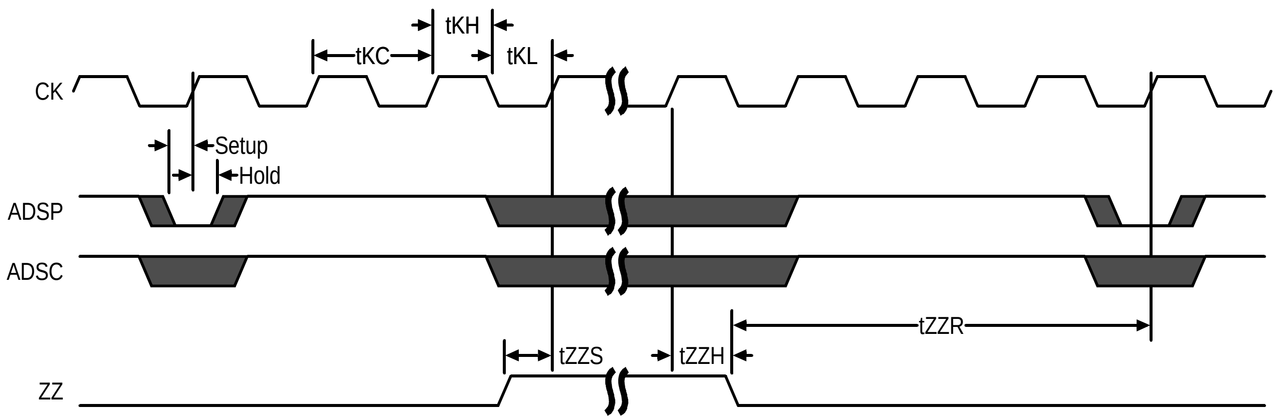
Sleep Mode

During normal operation, ZZ must be pulled low, either by the user or by its internal pull down resistor. When ZZ is pulled high, the SRAM will enter a Power Sleep mode after 2 cycles. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM operates normally after 2 cycles of wake up time.

Sleep mode is a low current, power-down mode in which the device is deselected and current is reduced to $I_{SB}2$. The duration of Sleep mode is dictated by the length of time the ZZ is in a High state. After entering Sleep mode, all inputs except ZZ become disabled and all outputs go to High-Z The ZZ pin is an asynchronous, active high input that causes the device to enter Sleep mode. When the ZZ pin is driven high, $I_{SB}2$ is guaranteed after the time tZZI is met. Because ZZ is an asynchronous input, pending operations or operations in progress may not be properly completed if ZZ is asserted. Therefore, Sleep mode must not be initiated until valid pending operations are completed. Similarly, when exiting Sleep mode during tZZR, only a Deselect or Read commands may be applied while the SRAM is recovering from Sleep mode.

Sleep Mode Timing Diagram



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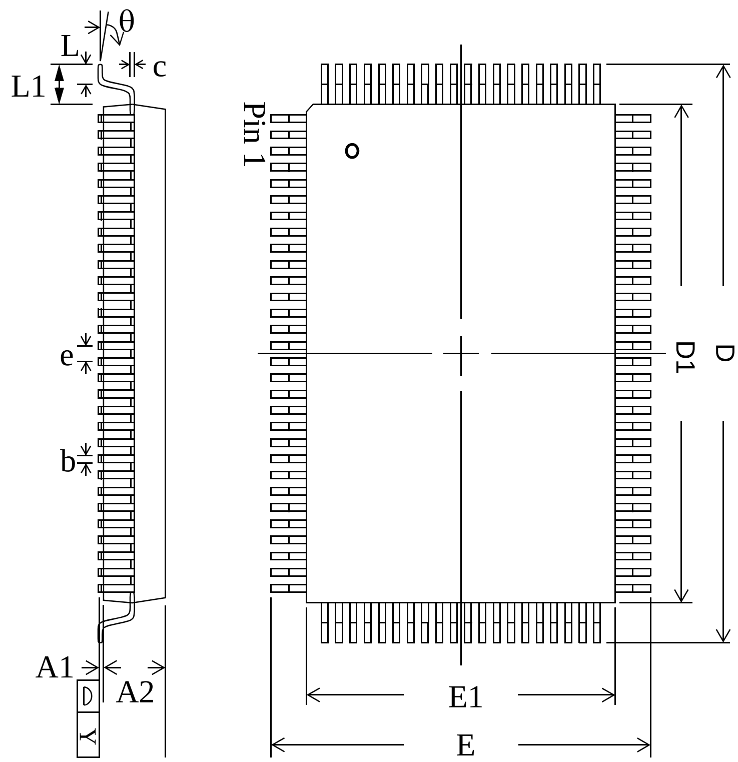
TQFP Package Drawing (Package GT)

Symbol	Description	Min.	Nom.	Max
A1	Standoff	0.05	0.10	0.15
A2	Body Thickness	1.35	1.40	1.45
b	Lead Width	0.20	0.30	0.40
c	Lead Thickness	0.09	—	0.20
D	Terminal Dimension	21.9	22.0	22.1
D1	Package Body	19.9	20.0	20.1
E	Terminal Dimension	15.9	16.0	16.1
E1	Package Body	13.9	14.0	14.1
e	Lead Pitch	—	0.65	—
L	Foot Length	0.45	0.60	0.75
L1	Lead Length	—	1.00	—
Y	Coplanarity			0.10
θ	Lead Angle	0°	—	7°



Notes:
1. All dimensions are in millimeters (mm).
2. Package width and length do not include mold protrusion.

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Ordering Information for GSI Synchronous Burst RAMs

Org	Part Number[1]	Type	Package	Speed[2] (MHz/ns)	T_J[3]
2M x 18	GS832018AGT-400	Pipeline/Flow Through	RoHS-compliant TQFP	400/4.0	C
2M x 18	GS832018AGT-375	Pipeline/Flow Through	RoHS-compliant TQFP	375/4.2	C
2M x 18	GS832018AGT-333	Pipeline/Flow Through	RoHS-compliant TQFP	333/4.5	C
2M x 18	GS832018AGT-250	Pipeline/Flow Through	RoHS-compliant TQFP	250/5.5	C
2M x 18	GS832018AGT-200	Pipeline/Flow Through	RoHS-compliant TQFP	200/6.5	C
2M x 18	GS832018AGT-150	Pipeline/Flow Through	RoHS-compliant TQFP	150/7.5	C
1M x 32	GS832032AGT-400	Pipeline/Flow Through	RoHS-compliant TQFP	400/4.0	C
1M x 32	GS832032AGT-375	Pipeline/Flow Through	RoHS-compliant TQFP	375/4.2	C
1M x 32	GS832032AGT-333	Pipeline/Flow Through	RoHS-compliant TQFP	333/4.5	C
1M x 32	GS832032AGT-250	Pipeline/Flow Through	RoHS-compliant TQFP	250/5.5	C
1M x 32	GS832032AGT-200	Pipeline/Flow Through	RoHS-compliant TQFP	200/6.5	C
1M x 32	GS832032AGT-150	Pipeline/Flow Through	RoHS-compliant TQFP	150/7.5	C
1M x 36	GS832036AGT-400	Pipeline/Flow Through	RoHS-compliant TQFP	400/4.0	C
1M x 36	GS832036AGT-375	Pipeline/Flow Through	RoHS-compliant TQFP	375/4.2	C
1M x 36	GS832036AGT-333	Pipeline/Flow Through	RoHS-compliant TQFP	333/4.5	C
1M x 36	GS832036AGT-250	Pipeline/Flow Through	RoHS-compliant TQFP	250/5.5	C
1M x 36	GS832036AGT-200	Pipeline/Flow Through	RoHS-compliant TQFP	200/6.5	C
1M x 36	GS832036AGT-150	Pipeline/Flow Through	RoHS-compliant TQFP	150/7.5	C
2M x 18	GS832018AGT-400I	Pipeline/Flow Through	RoHS-compliant TQFP	400/4.0	I
2M x 18	GS832018AGT-375I	Pipeline/Flow Through	RoHS-compliant TQFP	375/4.2	I
2M x 18	GS832018AGT-333I	Pipeline/Flow Through	RoHS-compliant TQFP	333/4.5	I
2M x 18	GS832018AGT-250I	Pipeline/Flow Through	RoHS-compliant TQFP	250/5.5	I
2M x 18	GS832018AGT-200I	Pipeline/Flow Through	RoHS-compliant TQFP	200/6.5	I
2M x 18	GS832018AGT-150I	Pipeline/Flow Through	RoHS-compliant TQFP	150/7.5	I
1M x 32	GS832032AGT-400I	Pipeline/Flow Through	RoHS-compliant TQFP	400/4.0	I
1M x 32	GS832032AGT-375I	Pipeline/Flow Through	RoHS-compliant TQFP	375/4.2	I

Notes:

1. Customers requiring delivery in Tape and Reel should add the character “T” to the end of the part number. Example: GS832018AGT-150IT.
2. The speed column indicates the cycle frequency (MHz) of the device in Pipeline mode and the latency (ns) in Flow Through mode. Each device is Pipeline/Flow Through mode-selectable by the user.
3. C = Commercial Temperature Range. I = Industrial Temperature Range.
4. GSI offers other versions this type of device in many different configurations and with a variety of different features, only some of which are covered in this data sheet. See the GSI Technology web site (www.gsitechnology.com) for a complete listing of current offerings.

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Ordering Information for GSI Synchronous Burst RAMs

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1M x 32	GS832032AGT-200I	Pipeline/Flow Through	RoHS-compliant TQFP	200/6.5	I
1M x 32	GS832032AGT-150I	Pipeline/Flow Through	RoHS-compliant TQFP	150/7.5	I
1M x 36	GS832036AGT-400I	Pipeline/Flow Through	RoHS-compliant TQFP	400/4.0	I
1M x 36	GS832036AGT-375I	Pipeline/Flow Through	RoHS-compliant TQFP	375/4.2	I
1M x 36	GS832036AGT-333I	Pipeline/Flow Through	RoHS-compliant TQFP	333/4.5	I
1M x 36	GS832036AGT-250I	Pipeline/Flow Through	RoHS-compliant TQFP	250/5.5	I
1M x 36	GS832036AGT-200I	Pipeline/Flow Through	RoHS-compliant TQFP	200/6.5	I
1M x 36	GS832036AGT-150I	Pipeline/Flow Through	RoHS-compliant TQFP	150/7.5	I

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36Mb Sync SRAM Datasheet Revision History

File Name	Types of Changes Format or Content	Page;Revisions;Reason
8320xxA_r1		• Creation of new datasheet • (Rev1.00a: Removed all non-RoHS-compliant TQFP references; updated speed bins)
8320xxA_r1_01	Content	• Updated Absolute Maximum Ratings • Added thermal information
8320xxA_r1_02	Content	• Updated to reflect MP status
8320xxA_r1_03	Content	• Updated Op Current numbers

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