

**FP-BGA**  
**Commercial Temp**  
**Industrial Temp**

**256K x 16**  
**4Mb Asynchronous SRAM**

**8, 10, 12 ns**  
**3.3 V  $V_{DD}$**   
**Center  $V_{DD}$  and  $V_{SS}$**

## Features

- Fast access time: 8, 10, 12 ns
- CMOS low power operation: 130/105/95 mA at minimum cycle time
- Single 3.3 V power supply
- All inputs and outputs are TTL-compatible
- Byte control
- Fully static operation
- Industrial Temperature Option:  $-40^{\circ}$  to  $85^{\circ}\text{C}$
- Package:
  - X: 6 mm x 10 mm Fine Pitch Ball Grid Array package
  - GX: Pb-Free 6 mm x 10 mm Fine Pitch Ball Grid Array package

## Description

The GS74117A is a high speed CMOS Static RAM organized as 262,144 words by 16 bits. Static design eliminates the need for external clocks or timing strobes. The GS operates on a single 3.3 V power supply and all inputs and outputs are TTL-compatible. The GS74117A is available in a 6 x 10 mm Fine Pitch BGA package.

## Fine Pitch BGA 256K x 16 Bump Configuration

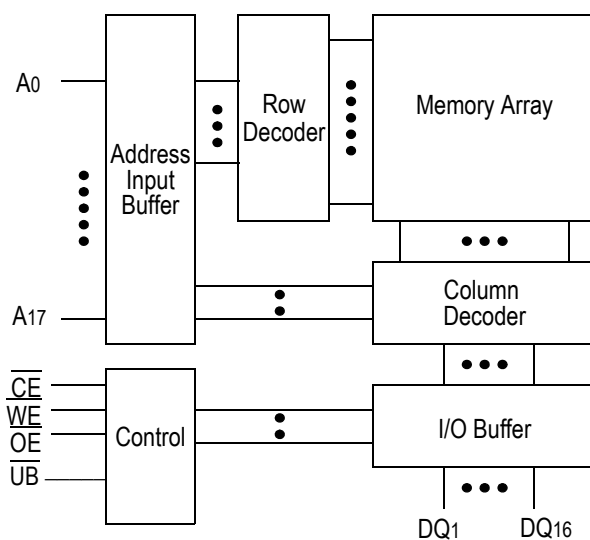
|   | 1                      | 2                      | 3   | 4   | 5                      | 6    |
|---|------------------------|------------------------|-----|-----|------------------------|------|
| A | $\overline{\text{LB}}$ | $\overline{\text{OE}}$ | A0  | A1  | A2                     | NC   |
| B | DQ1                    | $\overline{\text{UB}}$ | A3  | A4  | $\overline{\text{CE}}$ | DQ16 |
| C | DQ3                    | DQ2                    | A5  | A6  | DQ15                   | DQ14 |
| D | VSS                    | DQ4                    | A17 | A7  | DQ13                   | VDD  |
| E | VDD                    | DQ5                    | NC  | A16 | DQ12                   | VSS  |
| F | DQ6                    | DQ7                    | A8  | A9  | DQ10                   | DQ11 |
| G | DQ8                    | NC                     | A10 | A11 | $\overline{\text{WE}}$ | DQ9  |
| H | NC                     | A12                    | A13 | A14 | A15                    | NC   |

Package X  
 6 x 10 mm Substrate  
 Top View

## Pin Descriptions

| Symbol                 | Description                              |
|------------------------|------------------------------------------|
| A0–A17                 | Address input                            |
| DQ1–DQ16               | Data input/output                        |
| $\overline{\text{CE}}$ | Chip enable input                        |
| $\overline{\text{LB}}$ | Lower byte enable input<br>(DQ1 to DQ8)  |
| $\overline{\text{UB}}$ | Upper byte enable input<br>(DQ9 to DQ16) |
| $\overline{\text{WE}}$ | Write enable input                       |
| $\overline{\text{OE}}$ | Output enable input                      |
| $V_{DD}$               | +3.3 V power supply                      |
| $V_{SS}$               | Ground                                   |
| NC                     | No connect                               |

Block Diagram



Truth Table

| $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | $\overline{LB}$ | $\overline{UB}$ | DQ1 to DQ8        | DQ9 to DQ16       | VDD Current |
|-----------------|-----------------|-----------------|-----------------|-----------------|-------------------|-------------------|-------------|
| H               | X               | X               | X               | X               | Not Selected      | Not Selected      | ISB1, ISB2  |
| L               | L               | H               | L               | L               | Read              | Read              | IDD         |
|                 |                 |                 | L               | H               | Read              | High Z            |             |
|                 |                 |                 | H               | L               | High Z            | Read              |             |
| L               | X               | L               | L               | L               | Write             | Write             |             |
|                 |                 |                 | L               | H               | Write             | Not Write, High Z |             |
|                 |                 |                 | H               | L               | Not Write, High Z | Write             |             |
| L               | H               | H               | X               | X               | High Z            | High Z            |             |
| L               | X               | X               | H               | H               | High Z            | High Z            |             |

X: "H" or "L"

### Absolute Maximum Ratings

| Parameter                   | Symbol    | Rating                                         | Unit |
|-----------------------------|-----------|------------------------------------------------|------|
| Supply Voltage              | $V_{DD}$  | -0.5 to +4.6                                   | V    |
| Input Voltage               | $V_{IN}$  | -0.5 to $V_{DD} + 0.5$<br>( $\leq 4.6$ V max.) | V    |
| Output Voltage              | $V_{OUT}$ | -0.5 to $V_{DD} + 0.5$<br>( $\leq 4.6$ V max.) | V    |
| Allowable power dissipation | PD        | 0.7                                            | W    |
| Storage temperature         | $T_{STG}$ | -55 to 150                                     | °C   |

#### Note:

Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation shall be restricted to Recommended Operating Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

### Recommended Operating Conditions

| Parameter                                | Symbol   | Min  | Typ | Max            | Unit |
|------------------------------------------|----------|------|-----|----------------|------|
| Supply Voltage for -8/-10/-12            | $V_{DD}$ | 3.0  | 3.3 | 3.6            | V    |
| Input High Voltage                       | $V_{IH}$ | 2.0  | —   | $V_{DD} + 0.3$ | V    |
| Input Low Voltage                        | $V_{IL}$ | -0.3 | —   | 0.8            | V    |
| Ambient Temperature,<br>Commercial Range | $T_{Ac}$ | 0    | —   | 70             | °C   |
| Ambient Temperature,<br>Industrial Range | $T_{AI}$ | -40  | —   | 85             | °C   |

#### Notes:

1. Input overshoot voltage should be less than  $V_{DD} + 2$  V and not exceed 20 ns.
2. Input undershoot voltage should be greater than -2 V and not exceed 20 ns.

## Capacitance

| Parameter          | Symbol           | Test Condition         | Max | Unit |
|--------------------|------------------|------------------------|-----|------|
| Input Capacitance  | C <sub>IN</sub>  | V <sub>IN</sub> = 0 V  | 5   | pF   |
| Output Capacitance | C <sub>OUT</sub> | V <sub>OUT</sub> = 0 V | 7   | pF   |

### Notes:

1. Tested at T<sub>A</sub> = 25°C, f = 1 MHz
2. These parameters are sampled and are not 100% tested.

## DC I/O Pin Characteristics

| Parameter              | Symbol          | Test Conditions                                          | Min   | Max   |
|------------------------|-----------------|----------------------------------------------------------|-------|-------|
| Input Leakage Current  | I <sub>IL</sub> | V <sub>IN</sub> = 0 to V <sub>DD</sub>                   | -1 µA | 1 µA  |
| Output Leakage Current | I <sub>LO</sub> | Output High Z<br>V <sub>OUT</sub> = 0 to V <sub>DD</sub> | -1 µA | 1 µA  |
| Output High Voltage    | V <sub>OH</sub> | I <sub>OH</sub> = -4 mA                                  | 2.4   | —     |
| Output Low Voltage     | V <sub>OL</sub> | I <sub>LO</sub> = +4 mA                                  | —     | 0.4 V |

## Power Supply Currents

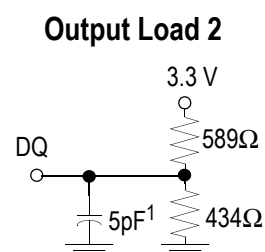
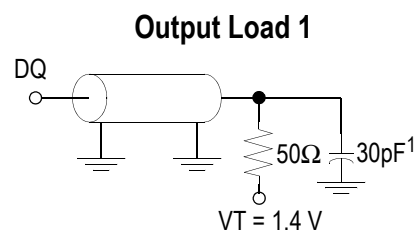
| Parameter                | Symbol           | Test Conditions                                                                                                              | 0 to 70°C |       |       | -40 to 85°C |       |       | Unit |
|--------------------------|------------------|------------------------------------------------------------------------------------------------------------------------------|-----------|-------|-------|-------------|-------|-------|------|
|                          |                  |                                                                                                                              | 8 ns      | 10 ns | 12 ns | 8 ns        | 10 ns | 12 ns |      |
| Operating Supply Current | I <sub>DD</sub>  | $\overline{CE} \leq V_{IL}$<br>All other inputs $\geq V_{IH}$ or $\leq V_{IL}$<br>Min. cycle time<br>I <sub>OUT</sub> = 0 mA | 130       | 105   | 90    | 140         | 115   | 100   | mA   |
| Standby Current          | I <sub>SB1</sub> | $\overline{CE} \geq V_{IH}$<br>All other inputs $\geq V_{IH}$ or $\leq V_{IL}$<br>Min. cycle time                            | 30        | 25    | 22    | 40          | 35    | 32    | mA   |
| Standby Current          | I <sub>SB2</sub> | $\overline{CE} \geq V_{DD} - 0.2 V$<br>All other inputs $\geq V_{DD} - 0.2 V$ or $\leq 0.2 V$                                | 10        |       |       | 20          |       |       | mA   |

## AC Test Conditions

| Parameter              | Conditions               |
|------------------------|--------------------------|
| Input high level       | $V_{IH} = 2.4 \text{ V}$ |
| Input low level        | $V_{IL} = 0.4 \text{ V}$ |
| Input rise time        | $t_r = 1 \text{ V/ns}$   |
| Input fall time        | $t_f = 1 \text{ V/ns}$   |
| Input reference level  | 1.4 V                    |
| Output reference level | 1.4 V                    |
| Output load            | <b>Fig. 1 &amp; 2</b>    |

### Notes:

1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted.
3. Output load 2 for  $t_{LZ}$ ,  $t_{HZ}$ ,  $t_{OLZ}$  and  $t_{OHZ}$



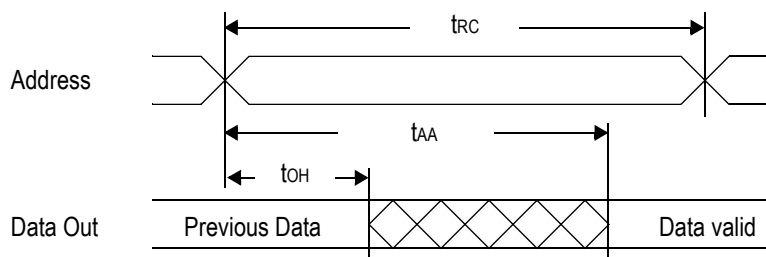
## AC Characteristics

### Read Cycle

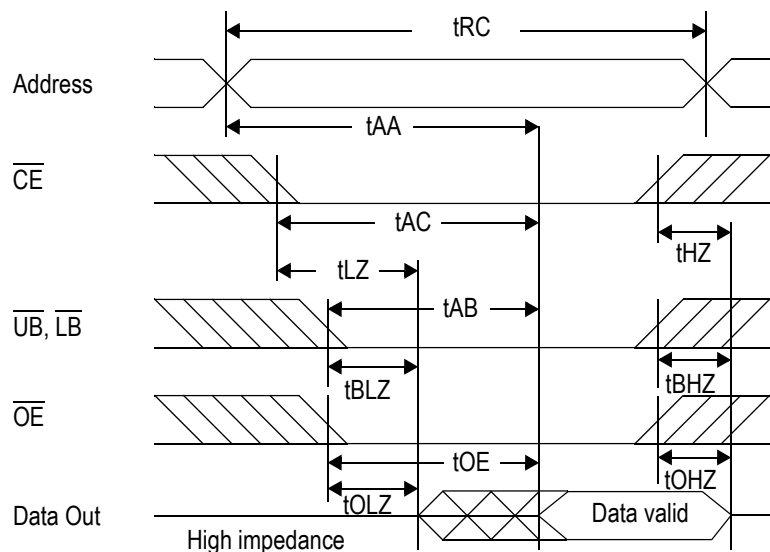
| Parameter                                                              | Symbol      | -8  |     | -10 |     | -12 |     | Unit |
|------------------------------------------------------------------------|-------------|-----|-----|-----|-----|-----|-----|------|
|                                                                        |             | Min | Max | Min | Max | Min | Max |      |
| Read cycle time                                                        | $t_{RC}$    | 8   | —   | 10  | —   | 12  | —   | ns   |
| Address access time                                                    | $t_{AA}$    | —   | 8   | —   | 10  | —   | 12  | ns   |
| Chip enable access time ( $\overline{CE}$ )                            | $t_{AC}$    | —   | 8   | —   | 10  | —   | 12  | ns   |
| Byte enable access time ( $\overline{UB}$ , $\overline{LB}$ )          | $t_{AB}$    | —   | 3.5 | —   | 4   | —   | 5   | ns   |
| Output enable to output valid ( $\overline{OE}$ )                      | $t_{OE}$    | —   | 3.5 | —   | 4   | —   | 5   | ns   |
| Output hold from address change                                        | $t_{OH}$    | 3   | —   | 3   | —   | 3   | —   | ns   |
| Chip enable to output in low Z ( $\overline{CE}$ )                     | $t_{LZ}^*$  | 3   | —   | 3   | —   | 3   | —   | ns   |
| Output enable to output in low Z ( $\overline{OE}$ )                   | $t_{OLZ}^*$ | 0   | —   | 0   | —   | 0   | —   | ns   |
| Byte enable to output in low Z ( $\overline{UB}$ , $\overline{LB}$ )   | $t_{BLZ}^*$ | 0   | —   | 0   | —   | 0   | —   | ns   |
| Chip disable to output in High Z ( $\overline{CE}$ )                   | $t_{HZ}^*$  | —   | 4   | —   | 5   | —   | 6   | ns   |
| Output disable to output in High Z ( $\overline{OE}$ )                 | $t_{OHZ}^*$ | —   | 3.5 | —   | 4   | —   | 5   | ns   |
| Byte disable to output in High Z ( $\overline{UB}$ , $\overline{LB}$ ) | $t_{BHZ}^*$ | —   | 3.5 | —   | 4   | —   | 5   | ns   |

\* These parameters are sampled and are not 100% tested.

**Read Cycle 1:  $\overline{CE} = \overline{OE} = V_{IL}$ ,  $\overline{WE} = V_{IH}$ ,  $\overline{UB}$  and, or  $\overline{LB} = V_{IL}$**



### Read Cycle 2: $\overline{WE} = V_{IH}$

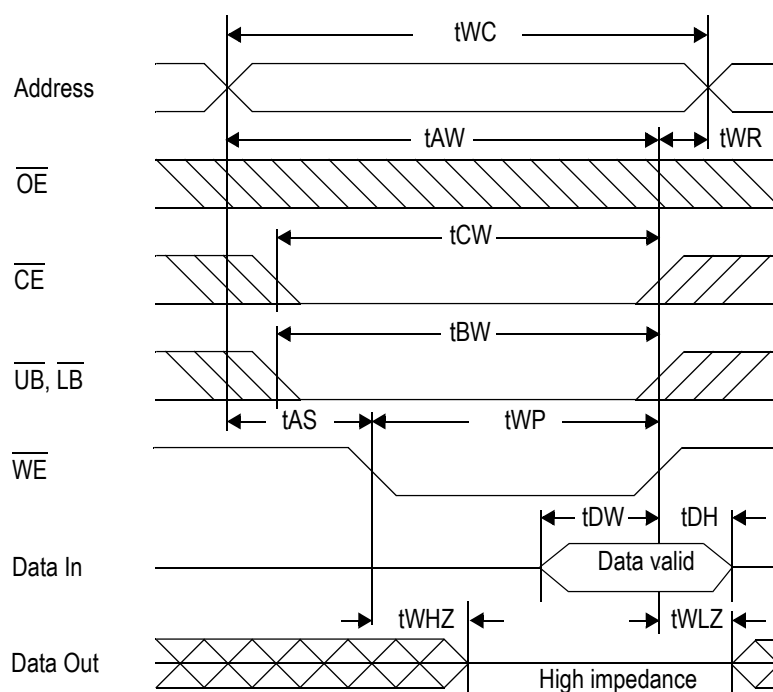


### Write Cycle

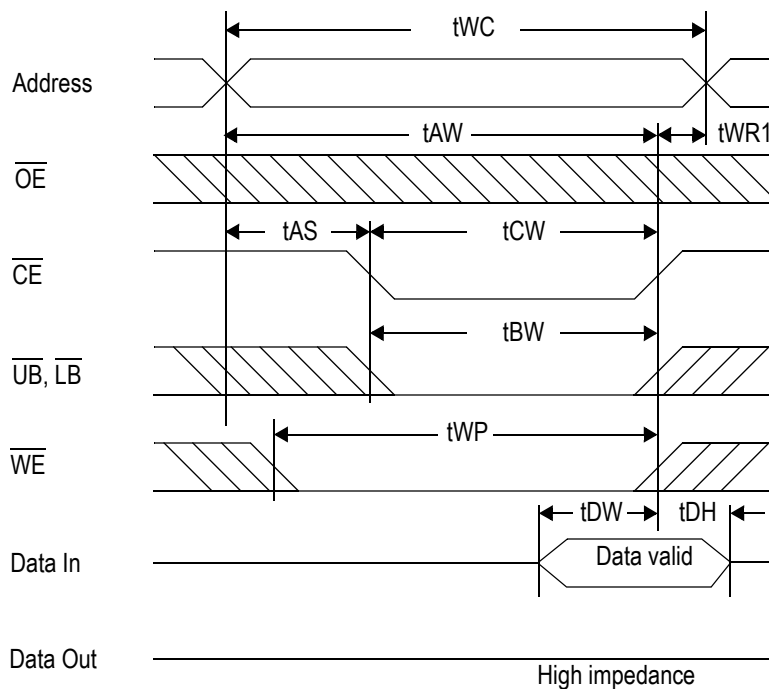
| Parameter                               | Symbol | -8  |     | -10 |     | -12 |     | Unit |
|-----------------------------------------|--------|-----|-----|-----|-----|-----|-----|------|
|                                         |        | Min | Max | Min | Max | Min | Max |      |
| Write cycle time                        | tWC    | 8   | —   | 10  | —   | 12  | —   | ns   |
| Address valid to end of write           | tAW    | 5.5 | —   | 7   | —   | 8   | —   | ns   |
| Chip enable to end of write             | tCW    | 5.5 | —   | 7   | —   | 8   | —   | ns   |
| Byte enable to end of write             | tBW    | 5.5 | —   | 7   | —   | 8   | —   | ns   |
| Data set up time                        | tDW    | 4   | —   | 4.5 | —   | 6   | —   | ns   |
| Data hold time                          | tDH    | 0   | —   | 0   | —   | 0   | —   | ns   |
| Write pulse width                       | tWP    | 5.5 | —   | 7   | —   | 8   | —   | ns   |
| Address set up time                     | tAS    | 0   | —   | 0   | —   | 0   | —   | ns   |
| Write recovery time ( $\overline{WE}$ ) | tWR    | 0   | —   | 0   | —   | 0   | —   | ns   |
| Write recovery time ( $\overline{CE}$ ) | tWR1   | 0   | —   | 0   | —   | 0   | —   | ns   |
| Output Low Z from end of write          | tWLZ*  | 3   | —   | 3   | —   | 3   | —   | ns   |
| Write to output in High Z               | tWHZ*  | —   | 3.5 | —   | 4   | —   | 5   | ns   |

\* These parameters are sampled and are not 100% tested.

### Write Cycle 1: $\overline{WE}$ control

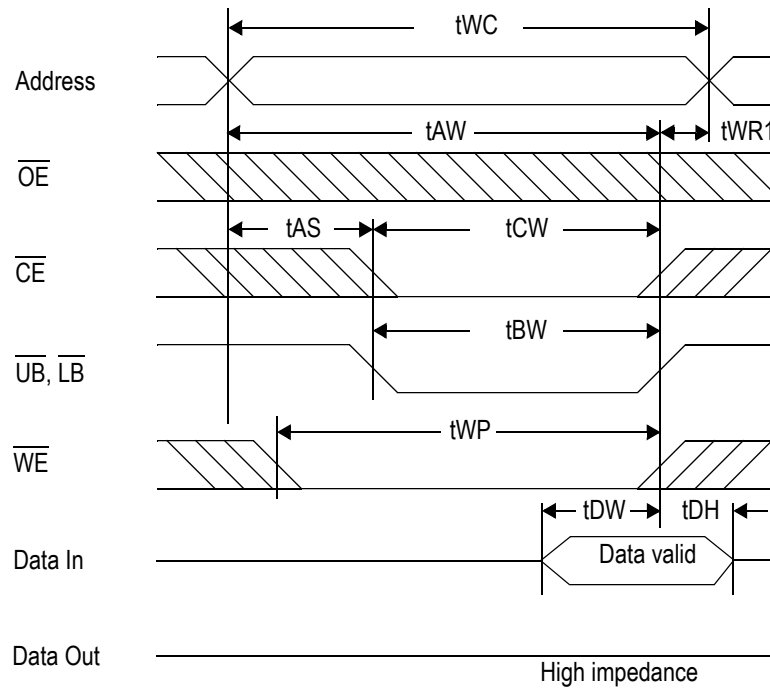


### Write Cycle 2: $\overline{CE}$ control

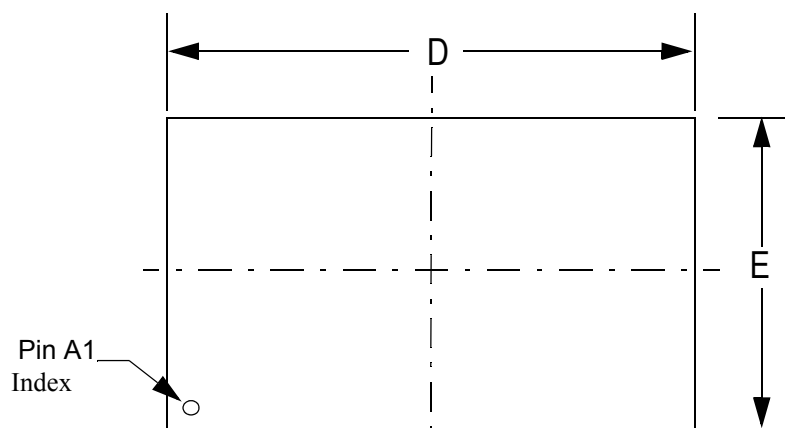




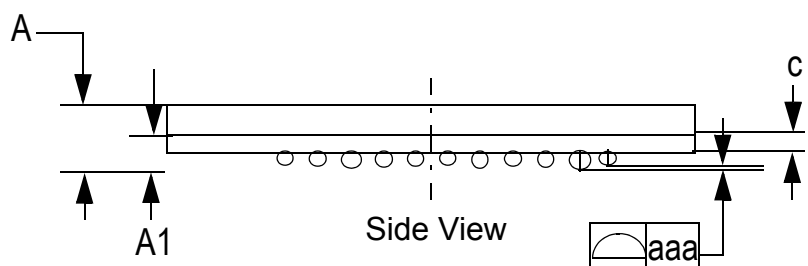
### Write Cycle 3: $\overline{UB}$ , $\overline{LB}$ control



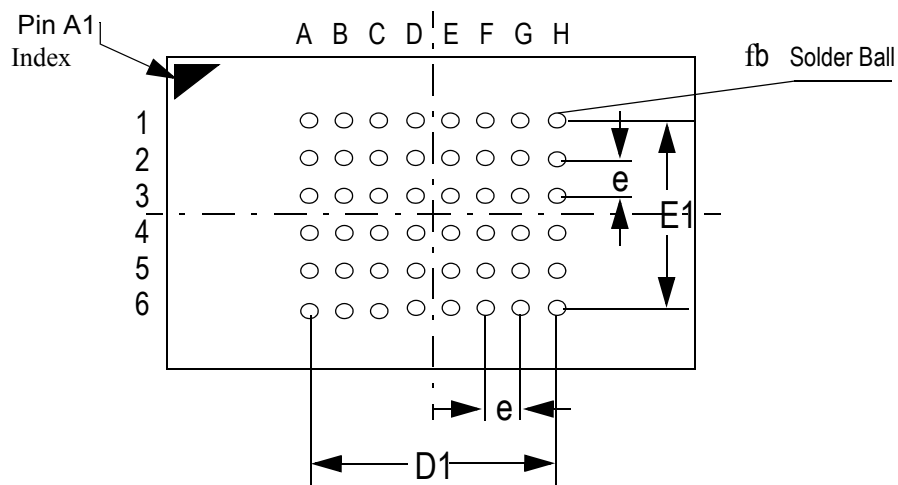
## Package X—6 mm x 10 mm FP-BGA



Top View



Side View



Bottom View

| Symbol | Unit: mm   |
|--------|------------|
| A      | 1.10±0.10  |
| A1     | 0.20~0.30  |
| fb     | f0.30~0.40 |
| c      | 0.36(TYP)  |
| D      | 10.0±0.05  |
| D1     | 5.25       |
| E      | 6.0±0.05   |
| E1     | 3.75       |
| e      | 0.75(TYP)  |
| aaa    | 0.10       |

**Ordering Information**

| <b>Part Number *</b> | <b>Package</b>           | <b>Access Time</b> | <b>Temp. Range</b> |
|----------------------|--------------------------|--------------------|--------------------|
| GS74117AX-8          | 6 mm x 10 mm BGA         | 8 ns               | Commercial         |
| GS74117AX-10         | 6 mm x 10 mm BGA         | 10 ns              | Commercial         |
| GS74117AX-12         | 6 mm x 10 mm BGA         | 12 ns              | Commercial         |
| GS74117AX-8I         | 6 mm x 10 mm BGA         | 8 ns               | Industrial         |
| GS74117AX-10I        | 6 mm x 10 mm BGA         | 10 ns              | Industrial         |
| GS74117AX-12I        | 6 mm x 10 mm BGA         | 12 ns              | Industrial         |
| GS74117AGX-8         | Pb-free 6 mm x 10 mm BGA | 8 ns               | Commercial         |
| GS74117AGX-10        | Pb-free 6 mm x 10 mm BGA | 10 ns              | Commercial         |
| GS74117AGX-12        | Pb-free 6 mm x 10 mm BGA | 12 ns              | Commercial         |
| GS74117AGX-8I        | Pb-free 6 mm x 10 mm BGA | 8 ns               | Industrial         |
| GS74117AGX-10I       | Pb-free 6 mm x 10 mm BGA | 10 ns              | Industrial         |
| GS74117AGX-12I       | Pb-free 6 mm x 10 mm BGA | 12 ns              | Industrial         |

\* Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. For example: GS74117AX-8T

#### 4Mb Asynchronous Datasheet Revision History

| Rev. Code: Old;<br>New     | Types of Changes<br>Format or Content | Page #/Revisions/Reason                                                                                                                                                                                            |
|----------------------------|---------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 74117A_r1                  | Format/Content                        | • Creation of new datasheet                                                                                                                                                                                        |
| 74117A_r1; 74117A_r1_01    | Content                               | • Updated Recommended Operating Conditions table on page 3<br>• Updated Read Cycle and Write Cycle AC Characteristics tables                                                                                       |
| 74117A_r1_01; 74117A_r1_02 | Content                               | • Removed 6 ns speed bin from entire document                                                                                                                                                                      |
| 74117A_r1_02; 74117A_r1_03 | Content                               | • Removed 7 ns speed bin from entire document                                                                                                                                                                      |
| 74117A_r1_03; 74117A_r1_04 | Format                                | • Updated format                                                                                                                                                                                                   |
| 74117A_r1_04; 74117A_r1_05 | Content                               | • Added Pb-free information for FP-BGA package<br>• (Rev1.05a: Removed empty status column on ordering information table)<br>• (Rev1.05b: Changed 6 x 10 mm Ball Pitch reference on page 1 to 6 x 10 mm Substrate) |

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[GS74117AGX-12I](#) [GS74117AGX-12](#) [GS74117AX-12I](#) [GS74117AX-8I](#) [GS74117AGX-10](#) [GS74117AX-12](#)  
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