High Efficiency 1A/2A Current-Mode Synchronous Buck Converter, 1MHz

TRIUNE PRODUCTS

Features

- Fixed output voltage choices: 1.5V, 1.8V, 2.5V, 3.3V, and 5V with +/- 2% output tolerance
- Adjustable version output voltage range: 0.9V to (VCC - 1V) with +/- 1.5% reference
- Wide input voltage range: 4.5V to 40V (42V Abs Max)
- 1MHz +/- 10% fixed switching frequency
- Continuous output current: 1A (TS30041), 2A (TS30042)
- High efficiency up to 95%
- Current mode PWM control with PFM mode for improved light load efficiency
- Voltage supervisor for VOUT reported at the Power Good (PG) pin
- Input supply under voltage lockout
- Soft start for controlled startup with no overshoot
- Full protection for over-current, over-temperature, and VOUT over-voltage
- SYNC function on EN/SYNC pin to control switching frequency
- Less than 10uA in standby mode
- Low external component count

Applications

- On-card switching regulators
- Set-top box, DVD, LCD, LED supply
- Industrial power supplies

Description

The TS30041 (1A) and TS30042 (2A) are DC/DC synchronous switching regulators with fully integrated power switches, internal compensation, and full fault protection. The switching frequency of 1MHz enables the use of small filter components resulting in minimal board space and reduced BOM costs.

The TS30041/42 utilizes current mode feedback in normal regulation PWM mode. When the regulator is placed in standby (EN is low), the device draws less than 10uA quiescent current.

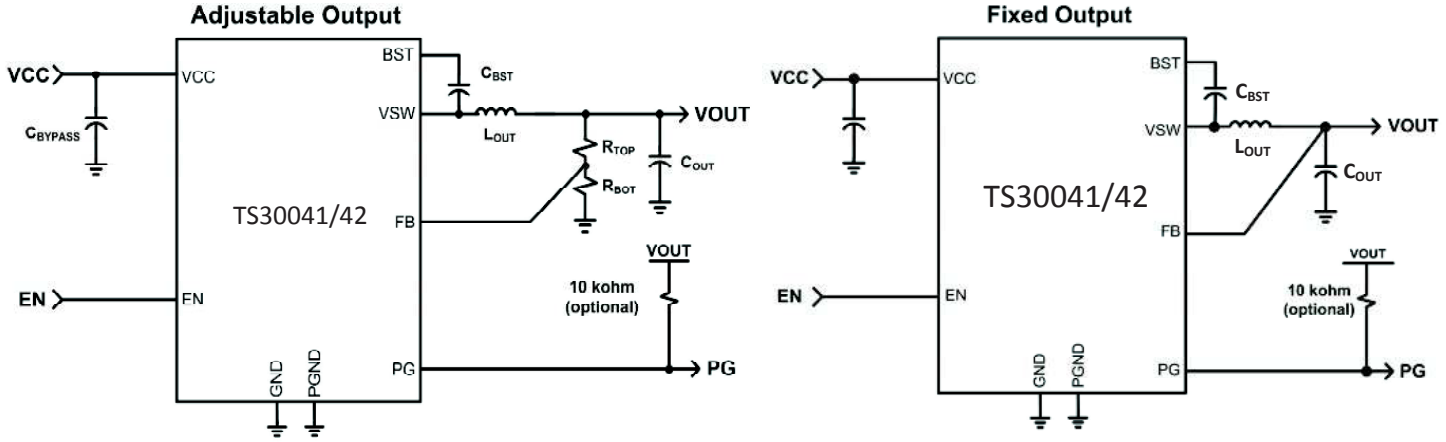
The TS30041/42 integrates a wide range of protection circuitry including input supply under-voltage lockout, output voltage soft start, current limit, and thermal shutdown.

The TS30041/42 includes supervisory reporting through the PG (Power Good) open drain output to interface other components in the system.

Summary Specification

- Junction operating temperature -40 °C to 125 °C
- Packaged in a 16pin QFN (3x3)
- ROHS: "Product is lead-free, Halogen Free, RoHS/WEEE compliant"

Typical Application Circuit



Pin Configuration

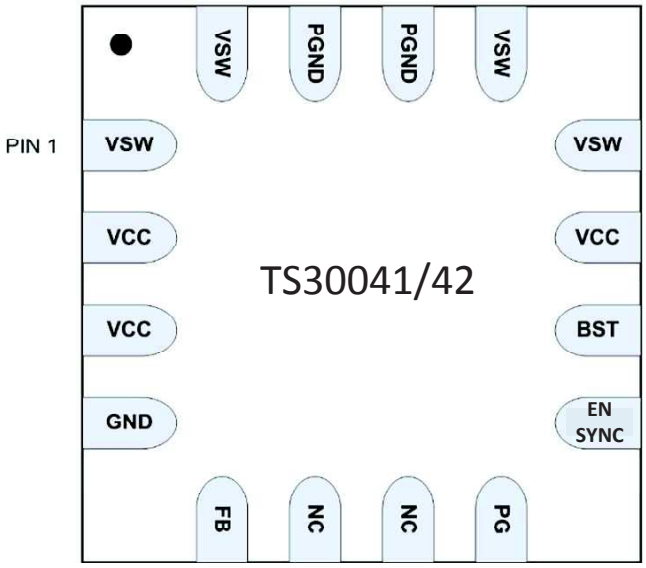


Figure 1: 16 Lead 3x3 QFN, Top View

Pin Description

Pin #	Pin Symbol	Function	Description
1	VSW	Switching Voltage Node	Connected to 4.7uH (typical) inductor
2	VCC	Input Voltage	Input voltage
3	VCC	Input Voltage	Input voltage
4	GND	GND	Primary ground for the majority of the device except the low-side power FET
5	FB	Feedback Input	Regulator FB Voltage. Connects to VOUT for fixed mode and the output resistor divider for adjustable mode
6	NC	No Connect	Not Connected
7	NC	No Connect	Not Connected
8	PG	Power Good Output	Open-drain output
9	EN/SYNC	Enable & Sync Input	Above 2.2V the device is enabled. GND the pin to put device in standby mode. Includes internal pull-up. Also used for SYNC function
10	BST	Bootstrap Capacitor	Bootstrap capacitor for the high-side FET gate driver. A ceramic capacitor in the range 15 nF - 200 nF from BST pin to VSW pin
11	VCC	Input Voltage	Input Voltage
12	VSW	Switching Voltage Node	Connected to 4.7uH (typical) inductor
13	VSW	Switching Voltage Node	Connected to 4.7uH (typical) inductor
14	PGND	Power GND	GND supply for internal low-side FET/integrated diode
15	PGND	Power GND	GND supply for internal low-side FET/integrated diode
16	VSW	Switching Voltage Node	Connected to 4.7uH (typical) inductor
17	PAD	Power PAD	Power GND

Functional Block Diagrams

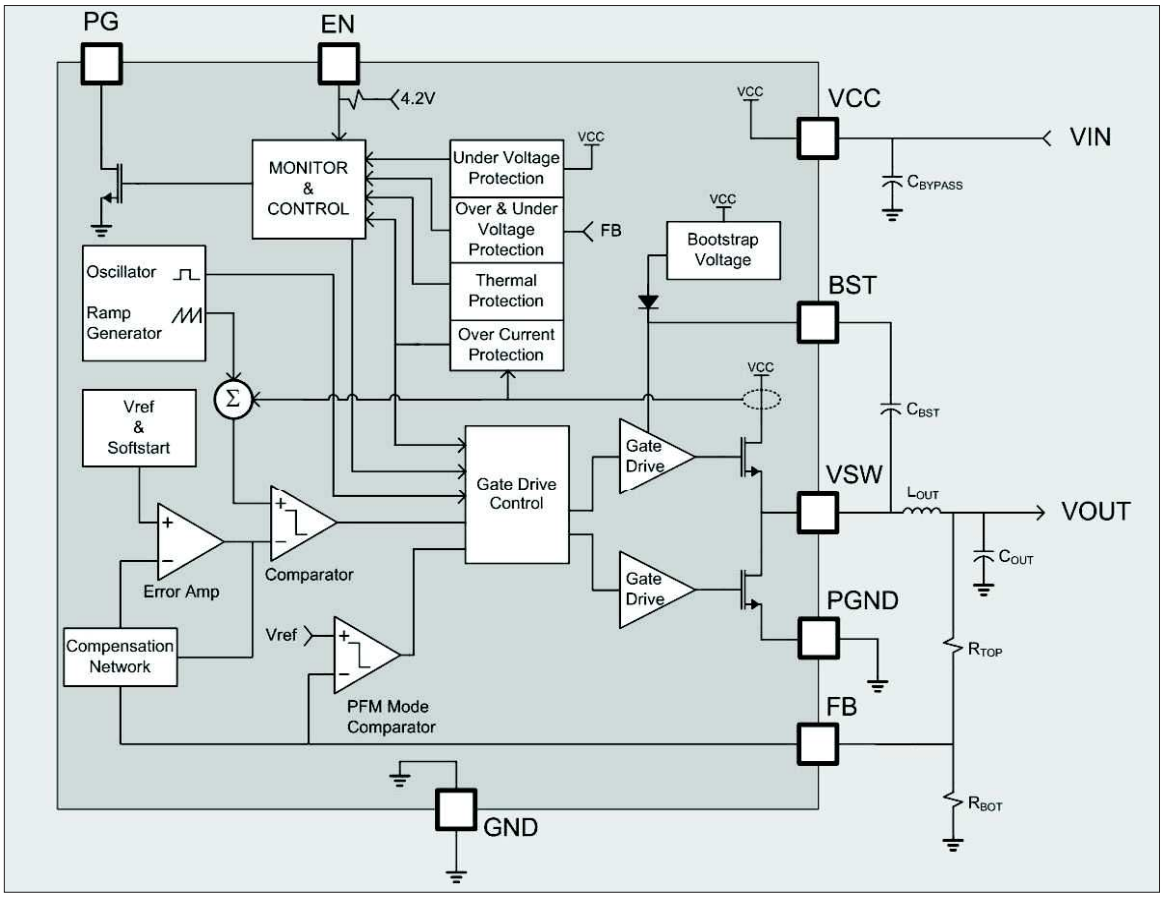


Figure 2: TS30041/42 Block Diagram

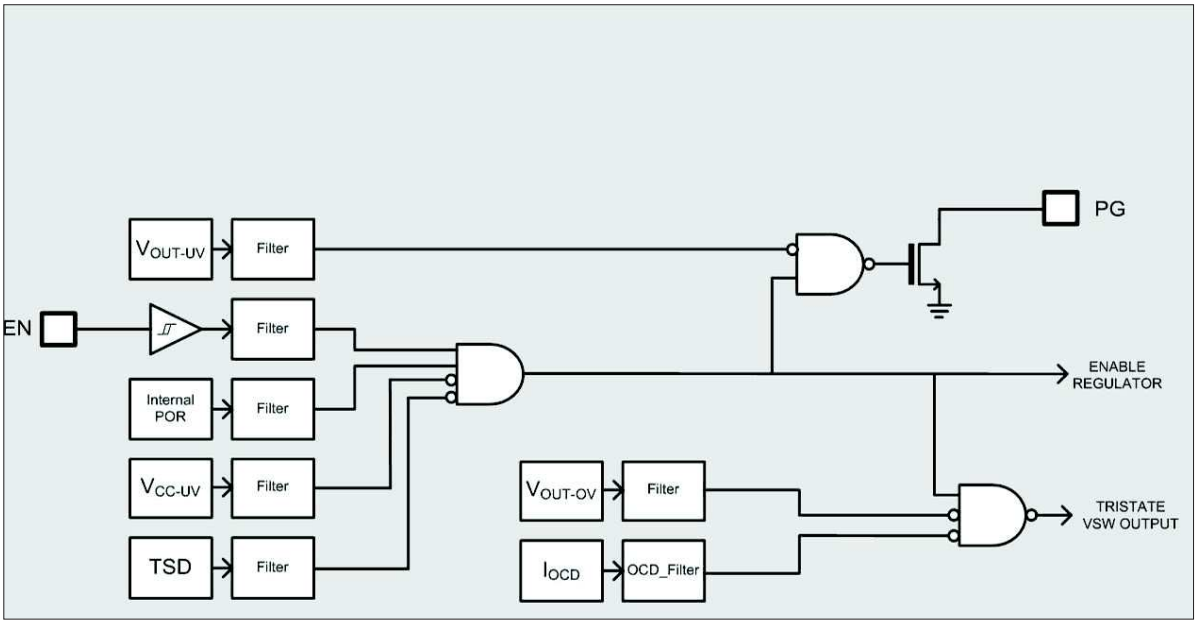


Figure 3: Monitor & Control Logic Functionality

Absolute Maximum Ratings

Over operating free–air temperature range unless otherwise noted(1,2,3)

Parameter	Value	Unit
VCC	-0.3 to 42	V
BST	-0.3 to (VCC+6)	V
VSW	-1 to 42	V
EN, PG,FB	-0.3 to 6	V
Electrostatic Discharge – Human Body Model	+/-2k	V
Electrostatic Discharge – Charge Device Model	+/-500	V
Lead Temperature (soldering, 10 seconds)	260	^{O}C

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

Note 2: All voltage values are with respect to network ground terminal.

Note 3: MOSFETs minimum breakdown voltage is 48V.

Thermal Characteristics

Over operating free–air temperature range unless otherwise noted(1,2)

Symbol	Parameter	Value	Unit
θ_{JA}	Thermal Resistance Junction to Air (Note 1)	34.5	°C/W
θ_{JC}	Thermal Resistance Junction to Case (Note 1)	2.5	°C/W
T_{STG}	Storage Temperature Range	-65 to 150	°C
$T_{J\ MAX}$	Maximum Junction Temperature	150	°C
T_J	Operating Junction Temperature Range	-40 to 125	°C

Note 1: Assumes 16LD 3x3 QFN with hi-K JEDEC board and 13.5 inch2 of 1 oz Cu and 4 thermal vias connected to PAD.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
VCC	Input Operating Voltage	4.5	12	40	V
C_{BST}	Bootstrap Capacitor	15	22	200	nF
L_{OUT}	Output Filter Inductor Typical Value (Note 1)	3.76	4.7	5.64	uH
C_{OUT}	Output Filter Capacitor Typical Value (Note 2)	33	44 (2 x 22)		uF
$C_{OUT-ESR}$	Output Filter Capacitor ESR	2		100	mΩ
C_{BYPASS}	Input Supply Bypass Capacitor Typical Value (Note 3)	8	10		uF

Note 1: For best performance, an inductor with a saturation current rating higher than the maximum VOUT load requirement plus the inductor current ripple.

Note 2: For best performance, a low ESR ceramic capacitor should be used.

Note 3: For best performance, a low ESR ceramic capacitor should be used. If CBYPASS is not a low ESR ceramic capacitor, a 0.1uF ceramic capacitor should be added in parallel to C_{BYPASS}

Electrical Characteristics

Electrical Characteristics, T_J = -40C to 125C, VCC = 12V (unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
VCC Supply Voltage						
Input Supply Voltage	V_{CC}		4.5		40	V
Quiescent current Normal Mode	$I_{CC-NORM}$	VCC = 12V, I_{LOAD} = 0A		3.6		mA
Quiescent current Normal Mode – Non-switching	$I_{CC-NOSWITCH}$	VCC=12V, I_{LOAD}=0A, Non-switching		2.5		mA
Quiescent current Standby Mode	$I_{CC-STBY}$	VCC = 12V, EN = 0V		5	10	uA
VCC Under Voltage Lockout						
Input Supply Under Voltage Threshold	V_{CC-UV}	V_{CC} Increasing		4.3	4.5	V
Input Supply Under Voltage Threshold Hysteresis	V_{CC-UV_HYST}			350		mV
OSC						
Oscillator Frequency (Internal)	f_{OSC}		0.9	1	1.1	MHz
SYNC Frequency(1)	f_{SYNC}		0.3		2.2	MHz
PG Open Drain Output						
PG Release Timer	t_{PG}			10		ms
High-Level Output Leakage	I_{OH-PG}	V_{PG} = 5V		0.5		uA
Low-Level Output Voltage	V_{OL-PG}	I_{PG} = -0.3mA			0.01	V
EN/Sync Input Voltage Thresholds						
High Level Input Voltage	V_{IH-EN}		2.2			V
Low Level Input Voltage	V_{IL-EN}				0.8	V
Input Hysteresis	$V_{HYST-EN}$			480		mV
Input Leakage	I_{IN-EN}	V_{EN}=5V		3.5		uA
		V_{EN}=0V		-1.5		uA
Thermal Shutdown						
Thermal Shutdown Junction Temperature	TSD	Note: not tested in production	150	170		°C
TSD Hysteresis	TSD_{HYST}	Note: not tested in production		10		°C

Note 1: SYNC frequency range is tested with a square wave. Operation with a 200ns minimum high pulse is required.

Regulator Characteristics

Electrical Characteristics, TJ = -40C to 125C (unless otherwise noted)

Parameter	Symbol	Condition	Min	Type	Max	Units
Switch Mode Regulator: L=4.7uH and C=2 x 22uF						
Output Voltage Tolerance in PWM Mode	$V_{OUT-PWM}$	I_{LOAD} =1A	V_{OUT} – 2%	V_{OUT}	V_{OUT} + 2%	V
Output Voltage Tolerance in PFM Mode	$V_{OUT-PFM}$	I_{LOAD} = 0A	V_{OUT} – 1%	V_{OUT} + 1%	V_{OUT} + 3.5%	V
High Side Switch On Resistance	R_{DSON}	I_{VSW} = -1A (Note 1)		180		mΩ
Low Side Switch On Resistance		I_{VSW} = 1A (Note 1)		120		mΩ
Output Current	I_{OUT}	TS30042 (Note 4)			2	A
		TS30041 (Note 4)			1	A
Over Current Detect (High Side Switch Current)	I_{OCD}	TS30042	2.4	2.8	3.4	A
		TS30041	1.4	1.8	2.4	A
Feedback Reference (Adjustable Mode)	FB_{TH}	(Note 3)	0.886	0.9	0.914	V
Feedback Reference Tolerance	FB_{TH-TOL}	(Note 3)	-1.5		1.5	%
Soft start Ramp Time	T_{SS}	Guaranteeed by Design		4		ms
PFM Mode FB Comparator Threshold	FB_{TH-PFM}			V_{OUT} + 1%		V
VOUT Under Voltage Threshold	V_{OUT-UV}		91% V_{OUT}	93% V_{OUT}	95% V_{OUT}	
VOUT Under Voltage Hysteresis	V_{OUT-UV_HYST}			1.5% V_{OUT}		
VOUT Over Voltage Threshold	V_{OUT-OV}			103% V_{OUT}		
VOUT Over Voltage Hysteresis	V_{OUT-OV_HYST}			1% V_{OUT}		
Max Duty Cycle	$DUTY_{MAX}$	(Note 2)	95%	97%	99%	
Minimum On Time	T_{0N-MIN}	Not tested in production		100		ns

Note 1: R_{DSON} is characterized at 1A and tested at lower current in production.
Note 2: Regulator VSW pin is forced off for 240ns every 16 cycles to ensure the BST cap is replenished.
Note 3: For the adjustable version, the ratio of VCC/Vout cannot exceed 16.
Note 4: Based on Over Current Detect testing

Typical Performance Characteristics

T_J = -40C to 125C, VCC = 12V (unless otherwise noted)

Figure 4. Startup Response

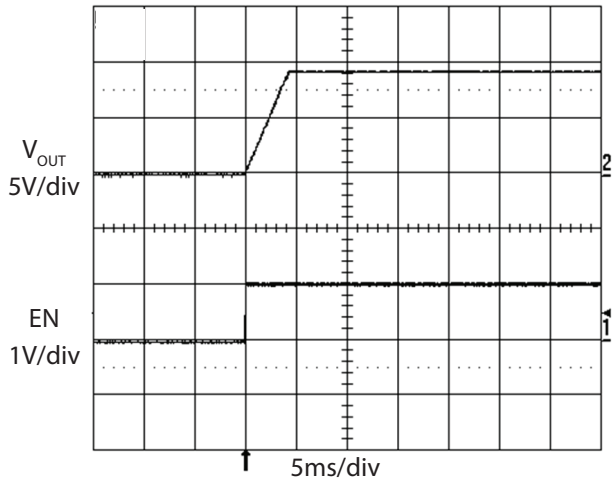


Figure 5. 100mA to 1A Load Step (V_{CC}=12V, V_{OUT}=3.3V)

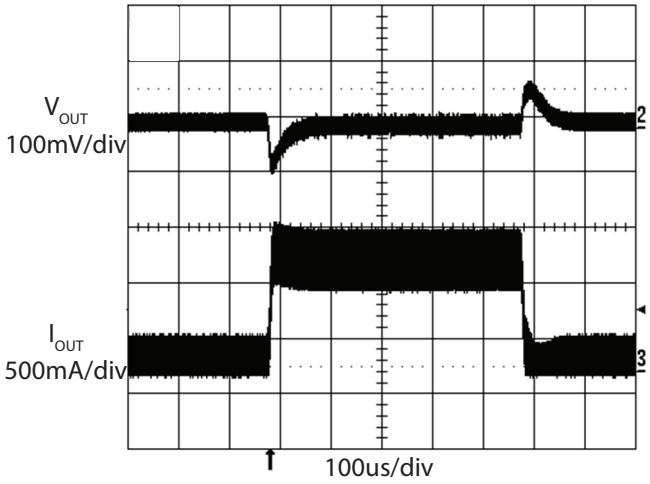


Figure 6. 100mA to 2A Load (V_{CC}=12V, V_{OUT}=3.3V)

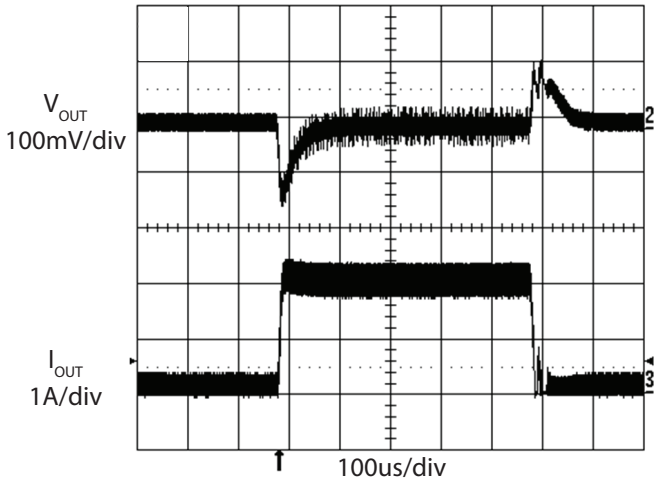


Figure 7. 100mA to 1A Load Step (V_{CC}=12V, V_{OUT}=1.8V)

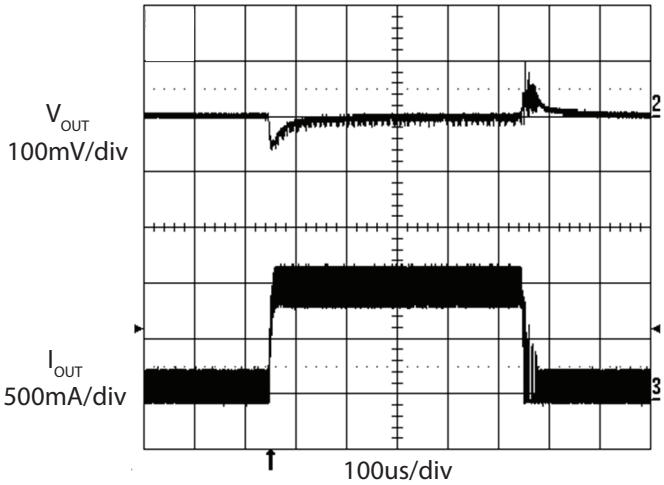


Figure 8. 100mA to 2A Load Step (V_{CC}=12V, V_{OUT}=1.8V)

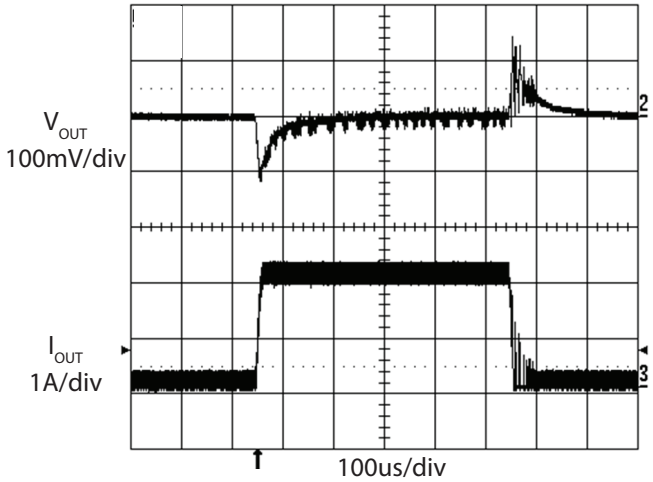
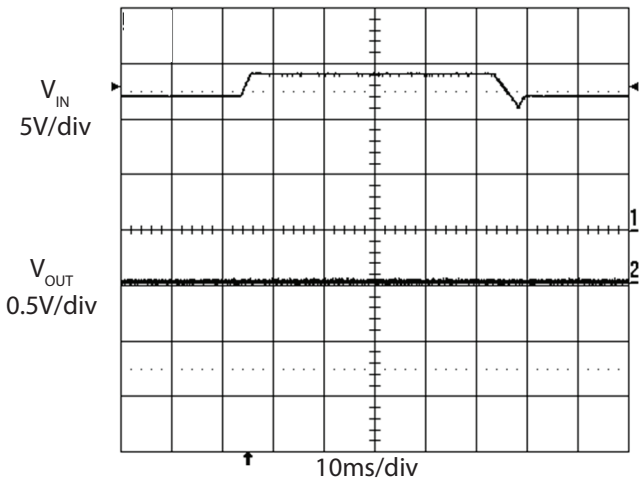


Figure 9. Line Transient Response (V_{CC}=12V, V_{OUT}=3.3V)



Typical Performance Characteristics continued

T_J = -40C to 125C, VCC = 12V (unless otherwise noted)

Figure 10. Load Regulation

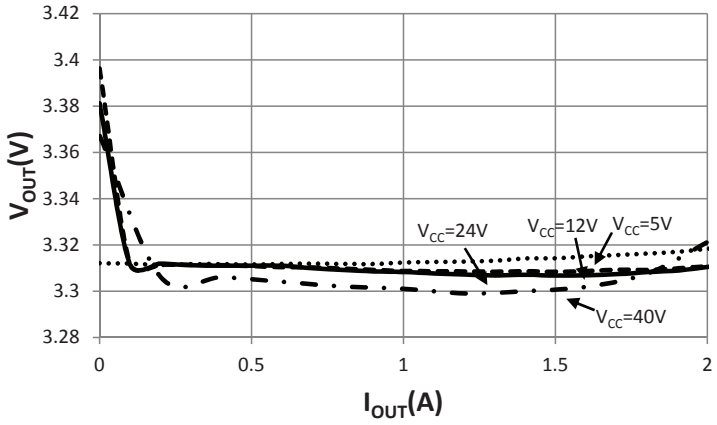


Figure 11. Line Regulation (I_{OUT}=1A)

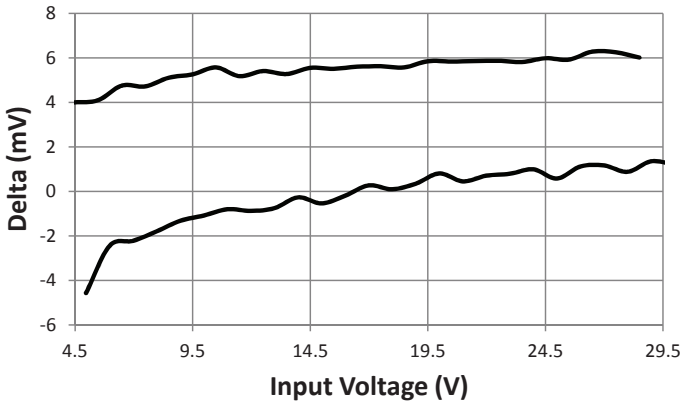


Figure 12. Efficiency vs. Output Current (V_{OUT} = 3.3V)

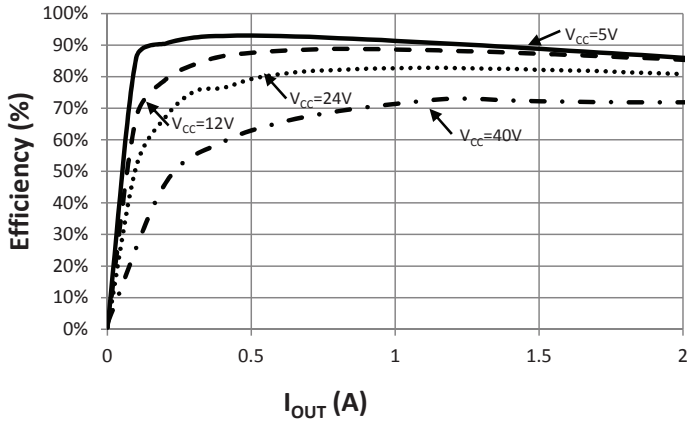


Figure 13. Efficiency vs. Output Current (V_{OUT} = 5V)

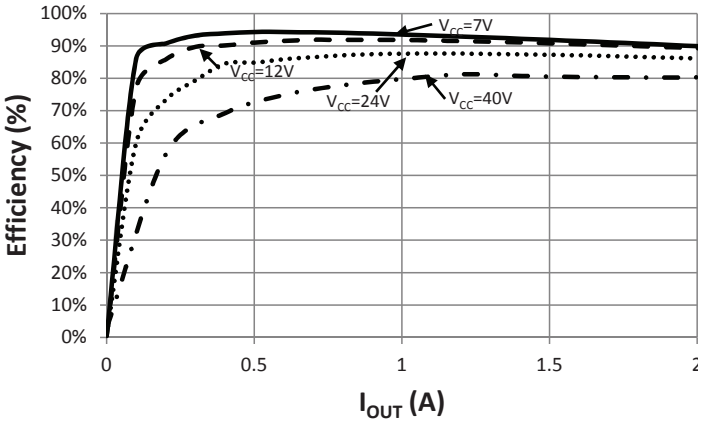


Figure 14. Efficiency vs. Output Current (V_{OUT} = 1.8V)

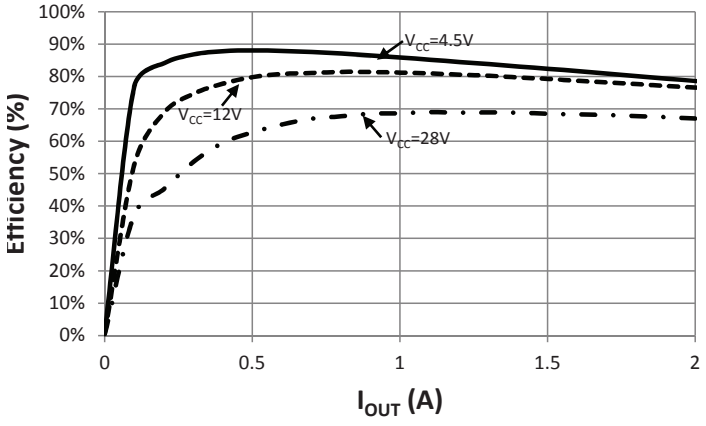
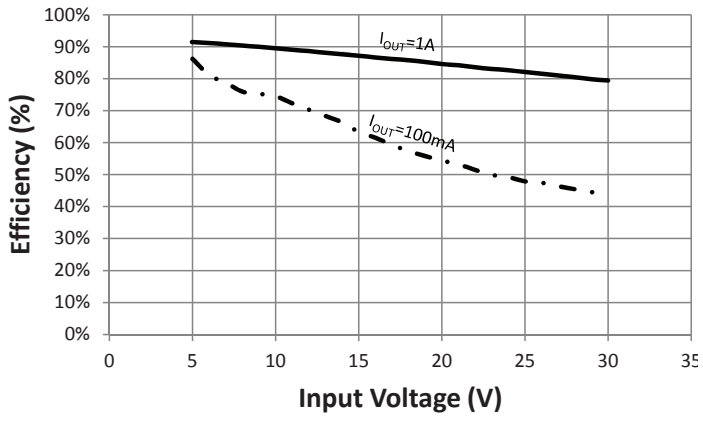


Figure 15. Efficiency vs. Input Voltage (V_{OUT} = 3.3V)



Typical Performance Characteristics continued

T_J = -40C to 125C, VCC = 12V (unless otherwise noted)

Figure 16. Standby Current vs. Input Voltage

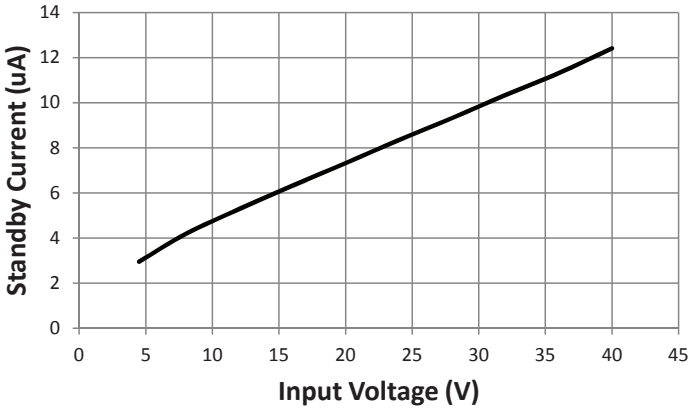


Figure 17. Standby Current vs. Temperature

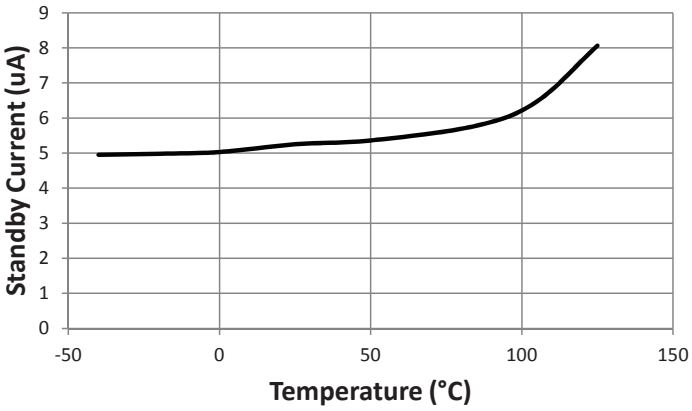


Figure 18. Output Voltage vs. Temperature

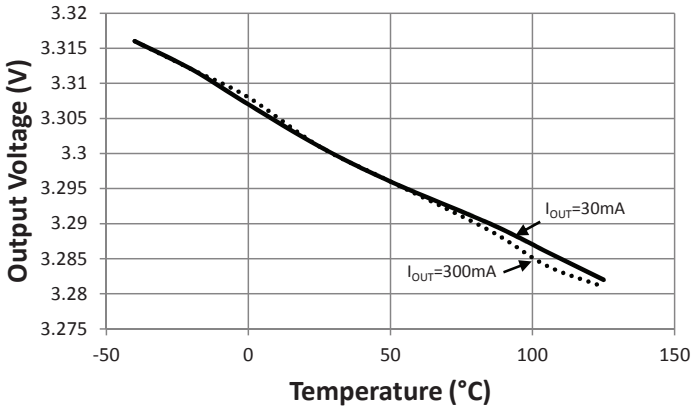


Figure 19. Oscillator Frequency vs. Temperature (I_{OUT}=300mA)

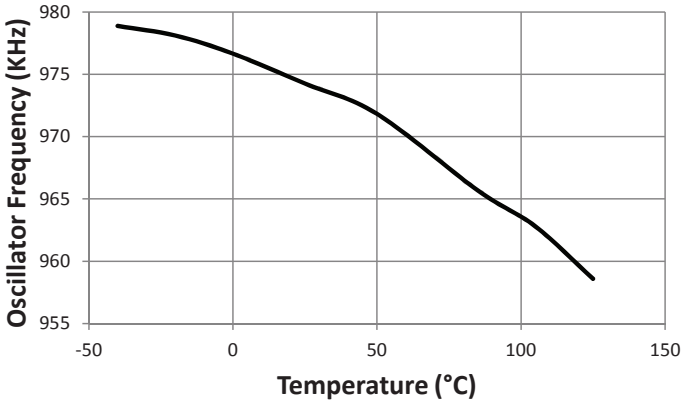
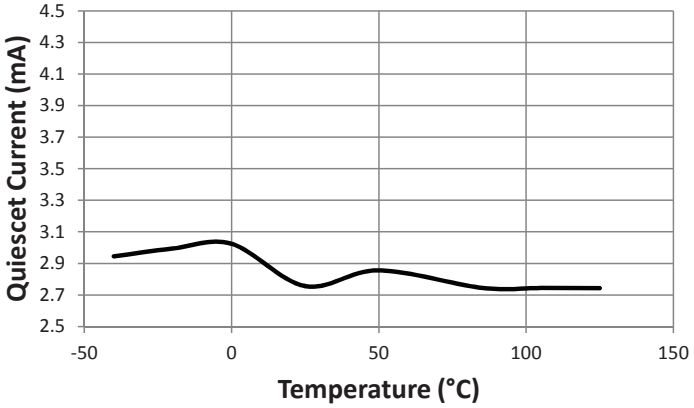


Figure 20. Quiescent Current vs. Temperature (No load)



Functional Description

The TS30041/42 current-mode synchronous step-down power supply product is ideal for use in the commercial, industrial, and automotive market segments. It includes flexibility to be used for a wide range of output voltages and is optimized for high efficiency power conversion with low RDSON integrated synchronous switches. A 1MHz internal switching frequency facilitates low cost LC filter combinations. Additionally, the fixed output versions enable a minimum external component count to provide a complete regulation solution with only 4 external components: an input bypass capacitor, an inductor, an output capacitor, and the bootstrap capacitor. The regulator automatically transitions between PFM and PWM mode to maximize efficiency for the load demand.

The TS30041/42 was designed to provide these system benefits:

- Reduced board real estate
- Lower system cost
  - Lower cost inductor
  - Low external parts count
- Ease of design
  - Bill of Materials and suggested board layout provided
  - Power Good output
  - Integrated compensation network
  - Wide input voltage range
- Robust solution
  - Over current, over voltage and over temperature protection

Detailed Pin Description

Unregulated input, VCC

This terminal is the unregulated input voltage source for the IC. It is recommended that a 10uF bypass capacitor be placed close to the device for best performance. Since this is the main supply for the IC, good layout practices need to be followed for this connection.

Bootstrap control, BST

This terminal will provide the bootstrap voltage required for the upper internal NMOS switch of the buck regulator. An external ceramic capacitor placed between the BST input terminal and the VSW pin will provide the necessary voltage for the upper switch. In normal operation the capacitor is re-charged on every low side synchronous switching action. In the case of where the switch mode approaches 100% duty cycle for the high side FET, the device will automatically reduce the duty cycle switch to a minimum off time on every 16th cycle to allow this capacitor to re-charge.

Sense feedback, FB

This is the input terminal for the output voltage feedback.

For the fixed mode versions, this should be hooked directly to VOUT. The connection on the PCB should be kept as short as possible, and should be made as close as possible to the capacitor. The trace should not be shared with any other connection. (Figure 22)

For adjustable mode versions, this should be connected to the external resistor divider. To choose the resistors, use the following equation:

$$V_{OUT} = 0.9\ (1 + R_{TOP}/R_{BOT})$$

The input to the FB pin is high impedance, and input current should be less than 100nA. As a result, good layout practices are required for the feedback resistors and feedback traces. When using the adjustable version, the feedback trace should be kept as short as possible and minimum width to reduce stray capacitance and to reduce the injection of noise.

For the adjustable version, the ratio of VCC/Vout cannot exceed 16.

Switching output, VSW
This is the switching node of the regulator. It should be connected directly to the 4.7uH inductor with a wide, short trace and to one end of the Bootstrap capacitor. It is switching between VCC and PGND at the switching frequency.

Ground, GND
This ground is used for the majority of the device including the analog reference, control loop, and other circuits.

Power Ground, PGND
This is a separate ground connection used for the low side synchronous switch to isolate switching noise from the rest of the device. (Figure 22)

Enable/Synchronize, high-voltage, EN/SYNC
This is the input terminal to activate the regulator. The input threshold is TTL/CMOS compatible. It also has an internal pull-up to ensure a stable state if the pin is disconnected.
After a sequence of three rising edge pulses having a frequency greater than or equal to FSync-Min, the switcher synchronizes to the frequency of the signal provided on the EN/SYNC pin. SYNC frequency range is tested with a square wave and a high pulse of minimum 200ns duration is required for proper operation. For highier frequencies of operation a 2.2uH inductor and for lower frequencies of operation a 10uH inductor is recommended.

Power Good Output, PG
This is an open drain, active low output. The switched mode output voltage is monitored and the PG line will remain low until the output voltage reaches the VOUT-UV threshold. Once the internal comparator detects the output voltage is above the desired threshold, an internal delay timer is activated and the PG line is de-asserted to high once this delay timer expires. In the event the output voltage decreases below VOUT-UV, the PG line will be asserted low and remain low until the output rises above VOUT-UV and the delay timer times out. See Figure 3 for the circuit schematic for the PG signal.

Internal Protection Details

Internal Current Limit
The current through the high side FET is sensed on a cycle by cycle basis and if current limit is reached, it will abbreviate the cycle. In addition, the device senses the FB pin to identify hard short conditions and will direct the VSW output to skip 4 cycles if current limit occurs when FB is low. This allows current built up in the inductor during the minimum on time to decay sufficiently. Current limit is always active when the regulator is enabled. Soft start ensures current limit does not prevent regulator startup.

Under extended over current conditions (such as a short), the device will automatically disable. Once the over current condition is removed, the device returns to normal operation automatically. (Alternately the factory can configure the device's NVM to shutdown the regulator if an extended over current event is detected and require a toggle of the Enable pin to return the device to normal operation.)

Thermal Shutdown
If the temperature of the die exceeds 170°C (typical), the VSW outputs will tri-state to protect the device from damage. The PG and all other protection circuitry will stay active to inform the system of the failure mode. Once the device cools to 160°C (typical), the device will start up again, following the normal soft start sequence. If the device reaches 170°C, the shutdown/restart sequence will repeat.

Reference Soft Start
The reference in this device is ramped at a rate of 4ms to prevent the output from overshoot during startup. This ramp restarts whenever there is a rising edge sensed on the Enable pin. This occurs in both the fixed and adjustable versions. During the soft start ramp, current limit is still active, and will still protect the device in case of a short on the output.

Output Overvoltage
If the output of the regulator exceeds 103% of the regulation voltage, the VSW outputs will tri-state to protect the device from damage. This check occurs at the start of each switching cycle. If it occurs during the middle of a cycle, the switching for that cycle will complete, and the VSW outputs will tri-state at the beginning of the next cycle.

VCC Under-Voltage Lockout
The device is held in the off state until VCC reaches 4.3V (typical). There is a 350mV hysteresis on this input, which requires the input to fall below 4.0V (typical) before the device will disable.

Transient Response

TS30041/42 has been designed to work under a wide range of input and output voltages, supporting different values and types of output capacitance. By design, TS30041/42 adjustable output version has lower bandwidth than fixed version. For adjustable output version designs, with a high slew rate load requirement using a 10nF feed-forward capacitor in parallel with the R_{TOP} feedback resistor is recommended.

Typical Application Schematic

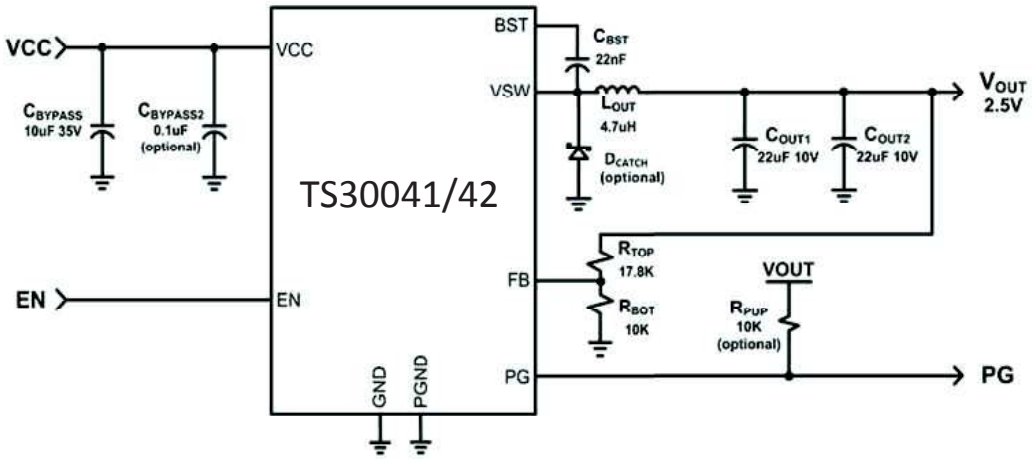


Figure 21: TS30041/42 Application Schematic

A minimal schematic suitable for most applications is shown on page 1. Figure 21 includes optional components that may be considered to address specific issues as listed in the External Component Selection section.

PCB Layout

For proper operation and minimum EMI, care must be taken during PCB layout. An improper layout can lead to issues such as poor stability and regulation, noise sensitivity and increased EMI radiation. (Figure 22) The main guidelines are the following:

- provide low inductive and resistive paths for loops with high di/dt,
- provide low capacitive paths with respect to all the other nodes for traces with high di/dt,
- sensitive nodes not assigned to power transmission should be referenced to the analog signal ground (GND) and be always separated from the power ground (PGND).

The negative ends of CBYPASS, COUT and the Schottky diode DCATCH (optional) should be placed close to each other and connected using a wide trace. Vias must be used to connect the PGND node to the ground plane. The PGND node must be placed as close as possible to the TS30041/42 PGND pins to avoid additional voltage drop in traces.

The bypass capacitor CBYPASS (optionally paralleled to a 0.1µF capacitor) must be placed close to the VCC pins of TS30041/42.

The inductor must be placed close to the VSW pins and connected directly to COUT in order to minimize the area between the VSW pin, the inductor, the COUT capacitor and the PGND pins. The trace area and length of the switching nodes VSW and BST should be minimized.

For the adjustable output voltage version of the TS30041/42, feedback resistors R_{BOT} and R_{TOP} are required for Vout settings greater than 0.9V and should be placed close to the TS30041/42 in order to keep the traces of the sensitive node FB as short as possible and away from switching signals. R_{BOT} should be connected to the analog ground pin (GND) directly and should never be connected to the ground plane. The analog ground trace (GND) should be connected in only one point to the power ground (PGND). A good connection point is under the TS30041/42 package to the exposed thermal pad and vias which are connected to PGND. RTOP will be connected to the V_{OUT} node using a trace that ends close to the actual load.

For fixed output voltage versions of the TS30041/42, R_{BOT} and R_{TOP} are not required and the FB pin should be connected directly to the Vout.

The exposed thermal pad must be soldered to the PCB for mechanical reliability and to achieve good power dissipation. Vias must be placed under the pad to transfer the heat to the ground plane.

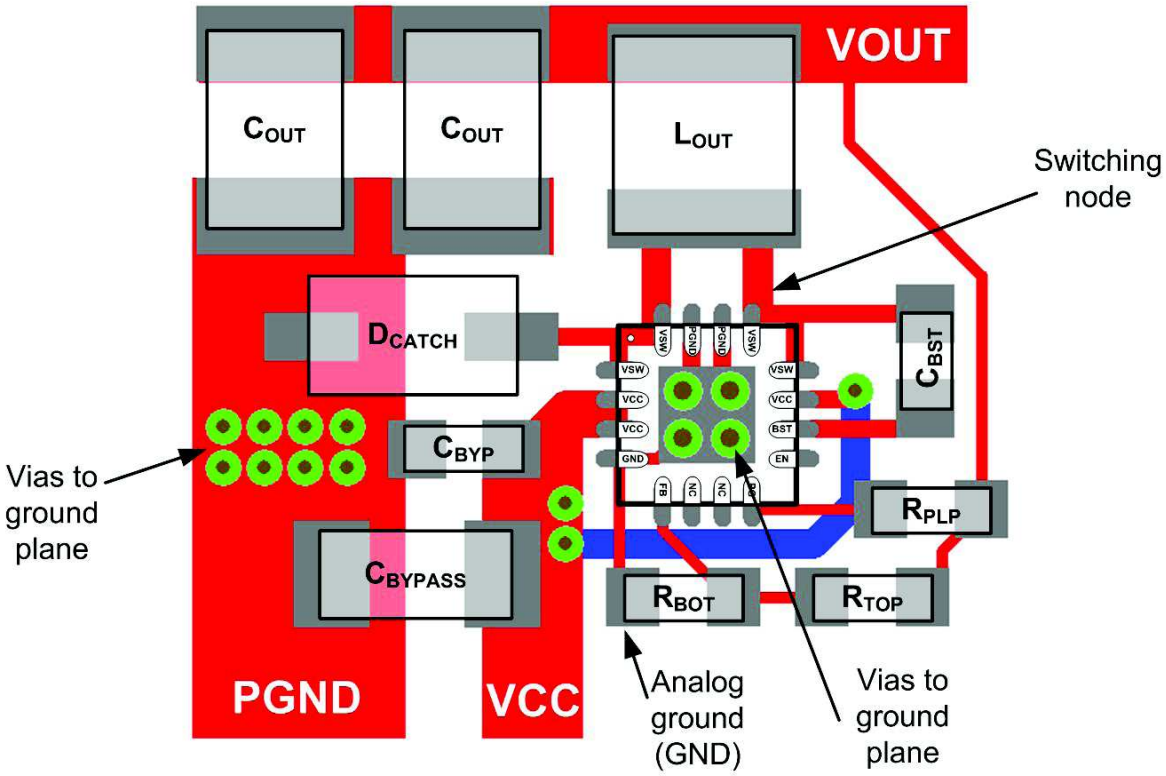


Figure 22: TS30041/42 PCB Layout, Top View

External Component Bill of Material

Designator	Function	Description	Suggested Manufacturer	Manufacturer Code	Qty
C_{BYPASS}	Input Supply Bypass Capacitor	10uF 10% 50V			1
C_{OUT}	Output Filter Capacitor	22uF 10% 10V	TDK Wurth	C2012X5R1A226K125AB 885 012 208 019	2
L_{OUT}	Output Filter Inductor (1A)	4.7uH 2A	TDK	SLF7045T-4R7M2R0-PF 7447745047	
L_{OUT}	Output Filter Inductor (2A)	4.7uH 3A	TDK Wurth	VLC5045T-4R7M 744774047	1
C_{BST}	Boost Capacitor	22nF 10V	TDK Wurth	C1005X7R1C223K 885 012 205 033	1
R_{TOP}	Voltage Feedback Resistor (optional)	17.8K (Note 1)			1
R_{BOT}	Voltage Feedback Resistor (optional)	10K (Note 1)			1
R_{PLP}	PG Pin Pull-up Resistor (optional)	10K			1
D_{CATCH}	Catch Diode (optional, 1A)	30V 2A SOD-123FL	On Semiconductor	MBR230LSFT1G	1
D_{CATCH}	Catch Diode (optional, 2A)	40V 3A SOD-123	NXP Semiconductors	PMEG4030ER,115	1

Note 1: The voltage divider resistor values are calculated for an output voltage of 2.5V. For fixed output versions, the FB pin is connected directly to V_{OUT}

External Component Selection

The 1MHz internal switching frequency of the TS30041/42 facilitates low cost LC filter combinations. Additionally, the fixed output versions enable a minimum external component count to provide a complete regulation solution with only 4 external components: an input bypass capacitor, an inductor, an output capacitor, and the bootstrap capacitor. The internal compensation is optimized for a 44uF output capacitor and a 4.7uH inductor.

For best performance, a low ESR ceramic capacitor should be used for CBYPASS. If CBYPASS is not a low ESR ceramic capacitor, a 0.1uF ceramic capacitor should be added in parallel to CBYPASS.

The minimum allowable value for the output capacitor is 33uF. To keep the output ripple low, a low ESR (less than 35mOhm) ceramic is recommended. Multiple capacitors can be paralleled to reduce the ESR.

The inductor range is 4.7uH +/-20%. For optimal over-current protection, the inductor should be able to handle up to the regulator current limit without saturation. Otherwise, an inductor with a saturation current rating higher than the maximum IOUT load requirement plus the inductor current ripple should be used.

For high current modes, the optional Schottky diode will improve the overall efficiency and reduce the heat. It is up to the user to determine the cost/benefit of adding this additional component in the user's application. The diode is typically not needed.

For the adjustable output version of the TS30041/42, the output voltage can be adjusted by sizing RTOP and RBOT feedback resistors. The equation for the output voltage is

$$Vout = 0.9 \cdot \left(1 + \left(\frac{R_{TOP}}{R_{BOT}}\right)\right)$$

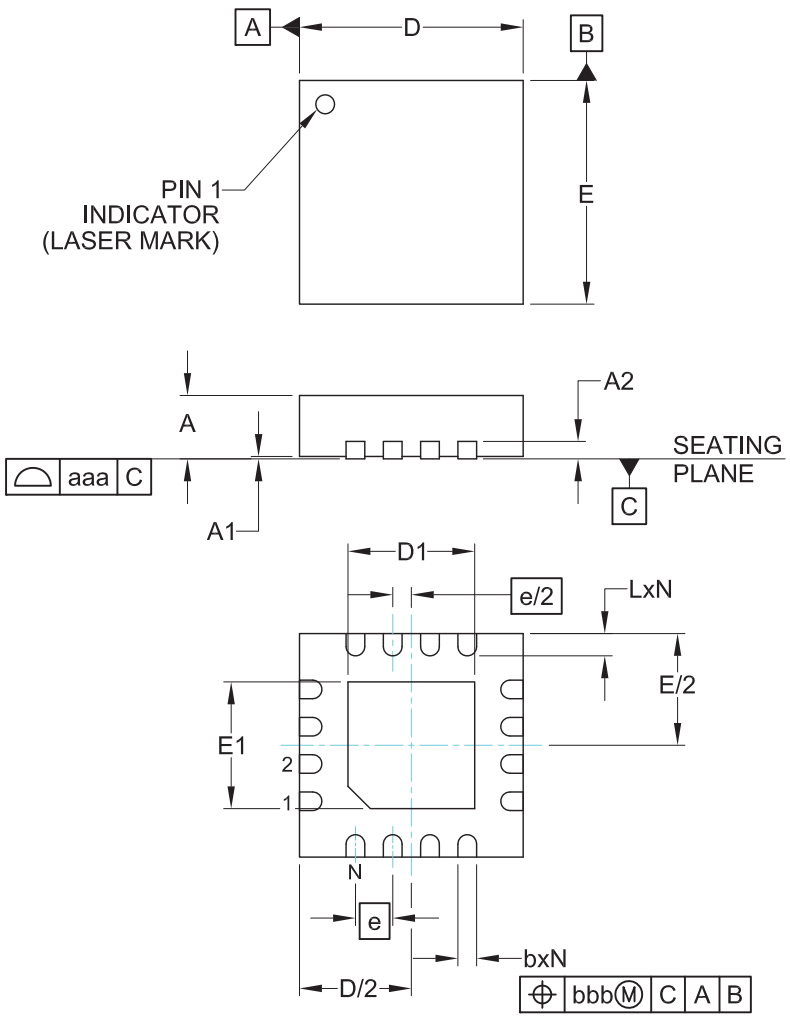
For the adjustable version, the ratio of VCC/Vout cannot exceed 16.

R_{PUP} is only required when the Power Good signal (PG) is utilized.

Thermal Information

TS30041/42 is designed for a maximum operating junction temperature Tj of 125°C. The maximum output power is limited by the power losses that can be dissipated over the thermal resistance given by the package and the PCB structures. The PCB must provide heat sinking to keep the TS30041/42 cool. The exposed metal on the bottom of the QFN package must be soldered to a ground plane. This ground should be tied to other copper layers below with thermal vias. Adding more copper to the top and the bottom layers and tying this copper to the internal planes with vias can reduce thermal resistance further. For a hi-K JEDEC board and 13.5 square inch of 1 oz Cu, the thermal resistance from junction to ambient can be reduced to θ_{JA} = 34.5°C/W. The power dissipation of other power components (catch diode, inductor) cause additional copper heating and can further increase what the TS30041/42 sees as ambient temperature.

Package Mechanical Drawings (all dimensions in mm)

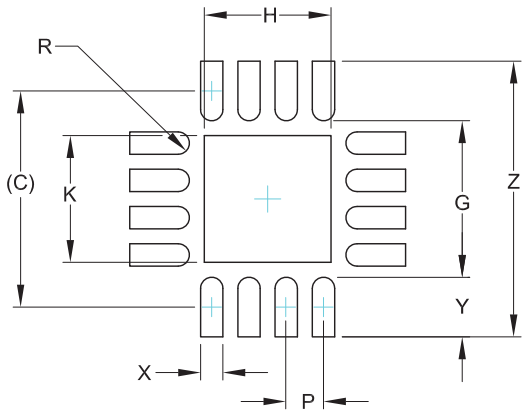


DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2	-	(0.20)	-
b	0.18	0.25	0.30
D	2.90	3.00	3.10
D1	1.55	1.70	1.80
E	2.90	3.00	3.10
E1	1.55	1.70	1.80
e	0.50 BSC		
L	0.20	0.30	0.40
N	16		
aaa	0.08		
bbb	0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Recommended PCB Land Pattern



DIMENSIONS	
DIM	MILLIMETERS
C	(2.90)
G	2.10
H	1.70
K	1.70
P	0.50
R	0.15
X	0.30
Y	0.80
Z	3.70

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

Marking and Ordering Information

Part Number	Voltage Assign	Marking Code
TS30041-M000QFNR	ADJ V	41M00
TS30041-M015QFNR	1.5 V	41M15
TS30041-M018QFNR	1.8 V	41M18
TS30041-M025QFNR	2.5 V	41M25
TS30041-M033QFNR	3.3 V	41M33
TS30041-M050QFNR	5.0 V	41M50

Tape & Reel (3300 parts/reel)

Marking for the 3 x 3mm MLPQ 16 Lead package:

nnnnn= Part Number (Example: 41Mnn)
yyww = Date Code (Example: 1652)
xxxx = Semtech Lot No. (Example: E901)

Part Number	Voltage Assign	Marking Code
TS30042-M000QFNR	ADJ V	42M00
TS30042-M015QFNR	1.5 V	42M15
TS30042-M018QFNR	1.8 V	42M18
TS30042-M025QFNR	2.5 V	42M25
TS30042-M033QFNR	3.3 V	42M33
TS30042-M050QFNR	5.0 V	42M50

Tape & Reel (3300 parts/reel)

Marking for the 3 x 3mm MLPQ 16 Lead package:

nnnnn= Part Number (Example: 42Mnn)
yyww = Date Code (Example: 1652)
xxxx = Semtech Lot No. (Example: E901)

Contact Information

Semtech Corporation
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111, Fax: (805) 498-3804
www.semtech.com

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Semtech:
TS30042-M025QFNR TS30041-M015QFNR TS30042-M015QFNR TS30041-M025QFNR TS30041-M050QFNR TS30041-M000QFNR TS30042-M000QFNR TS30042-M018QFNR TS30041-M033QFNR TS30041-M018QFNR TS30042-M050QFNR TS30042-M033QFNR