

## PROTECTION PRODUCTS

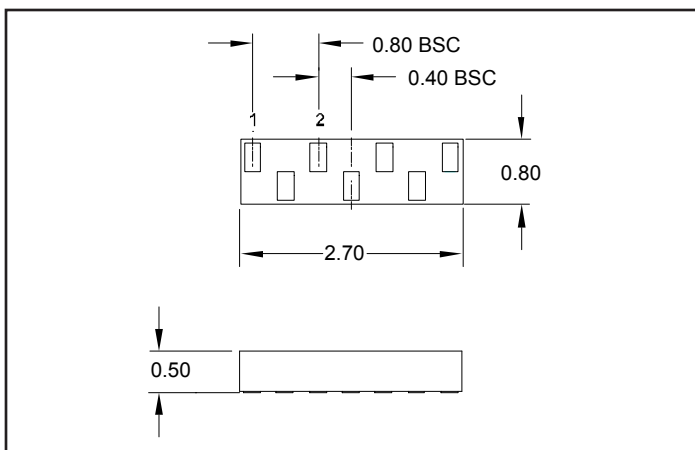
### Description

The RClamp®3346P provides ESD protection for high-speed data interfaces. It features a high maximum ESD withstand voltage of  $\pm 17\text{kV}$  contact and  $\pm 20\text{kV}$  air discharge per IEC 61000-4-2. RClamp3346P is designed to minimize both the ESD peak clamping and the TLP clamping. Package inductance is reduced at each pin resulting in lower peak ESD clamping voltage. The dynamic resistance is among the industry's lowest at 0.15 Ohms (typical). Maximum capacitance on each line to ground is 0.65pF allowing the RClamp3346P to be used in applications operating in excess of 5GHz without signal attenuation. Each device will protect up to six lines (three high-speed pairs).

The RClamp3346P is in a 7-pin SGP2708N7 package measuring 2.7 x 0.8mm with a nominal height of 0.50mm. The leads have a nominal pin-to-pin pitch of 0.40mm. Flow-through package design simplifies PCB layout and maintains signal integrity on high-speed lines.

The combination of low peak ESD clamping, low dynamic resistance, and innovative package design enables this device to provide the highest level of ESD protection for applications such as USB 3.0, eSATA, and DisplayPort.

### Package Dimension



### Features

- ESD protection for high-speed data lines to
  - ♦ **IEC 61000-4-2 (ESD)  $\pm 17\text{kV}$  (Contact),  $\pm 20\text{kV}$  (Air)**
  - ♦ **IEC 61000-4-5 (Lightning) 5A (8/20  $\mu\text{s}$ )**
  - ♦ **IEC 61000-4-4 (EFT) 40A (5/50ns)**
- Package design optimized for high speed lines
- Flow-Through design
- Protects six high-speed lines
- Low capacitance: 0.65pF Maximum (I/O to Ground)
- Low ESD clamping voltage
- Low dynamic resistance: 0.15 Ohms (Typical)
- Solid-state silicon-avalanche technology

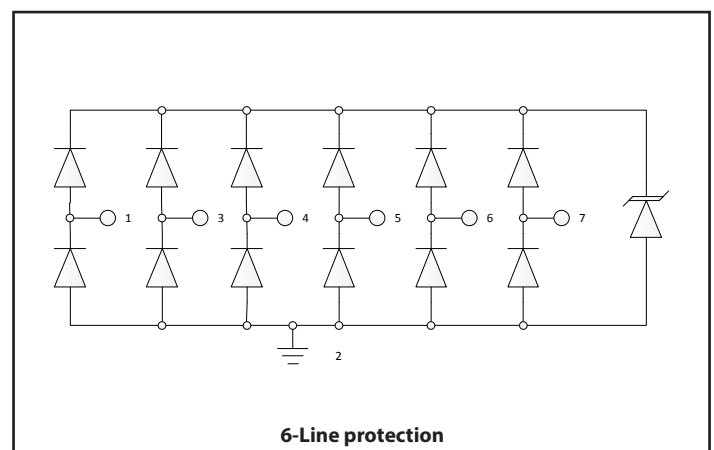
### Mechanical Characteristics

- SGP2708N7 7-pin package (2.7 x 0.8 x 0.50mm)
- Pb-Free, Halogen Free, RoHS/WEEE compliant
- Lead Pitch: 0.4mm (intra-pair)
- Lead Finish: NiPdAu
- Marking: Marking code
- Packaging: Tape and Reel

### Applications

- USB 3.0
- eSATA
- Display Port
- LVDS

### Schematic & Pin Configuration



## Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Current ( $t_p = 8/20\mu s$ )	$I_{PP}$	4.5	A
ESD per IEC 61000-4-2 (Air) <sup>(1)</sup> ESD per IEC 61000-4-2 (Contact) <sup>(1)</sup>	$V_{ESD}$	$\pm 20$ $\pm 17$	kV
Operating Temperature	$T_J$	-40 to +125	°C
Storage Temperature	$T_{STG}$	-55 to +150	°C

## Electrical Characteristics (T=25°C unless otherwise specified)

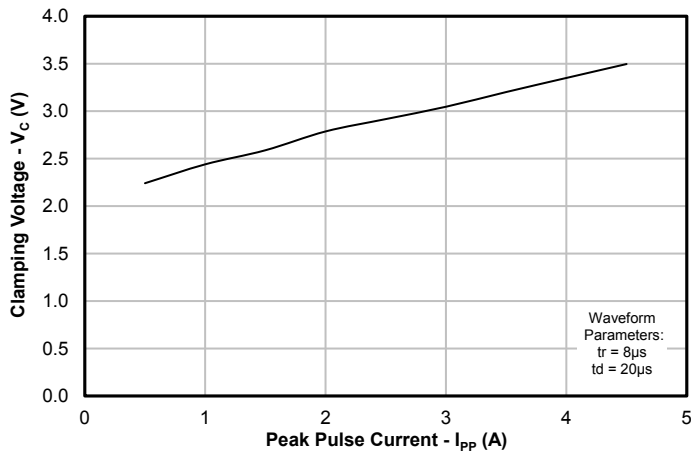
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	$V_{RWM}$	Any I/O to GND			3.3	V
Reverse Breakdown Voltage	$V_{BR}$	$I_{BR} = 10\mu A$	7	8	9	V
Reverse Leakage Current	$I_R$	$V_{RWM} = 3.3V$ Any I/O to GND	$T = 25^\circ C$	0.01	0.05	$\mu A$
			$T = 125^\circ C$		0.150	
Clamping Voltage	$V_C$	$t_p = 8/20\mu s$ Any I/O to GND	$I_{PP} = 1A$	2.5	3.5	V
			$I_{PP} = 4.5A$	3.5	4.5	
ESD Clamping Voltage <sup>2</sup>	$V_C$	$t_p = 0.2/100ns$	$I_{PP} = 16A$	5.5		V
			$I_{PP} = -16A$	-3		
Dynamic Resistance (positive) <sup>2,3</sup>	$R_{DYN}$	$t_p = 0.2/100ns$		0.15		$\Omega$
Dynamic Resistance (negative) <sup>2,3</sup>	$R_{DYN}$	$t_p = 0.2/100ns$		0.14		
Junction Capacitance	$C_J$	$V_R = 0V, f = 1MHz, \text{Any I/O to GND}$		0.60	0.65	pF
		$V_R = 0V, f = 1MHz, \text{Between I/O pins}$		0.30	0.40	

### Notes

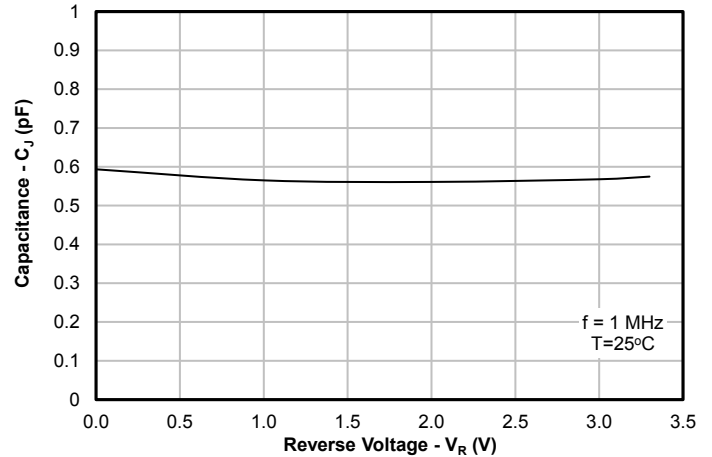
- 1) Measured with a 20dB attenuator, 50 Ohm scope input impedance, 2GHz bandwidth. ESD gun return path connected to ESD ground plane.
- 2) Transmission Line Pulse Test (TLP) Settings:  $t_p = 100ns$ ,  $t_r = 0.2ns$ ,  $I_{TLP}$  and  $V_{TLP}$  averaging window:  $t_1 = 70ns$  to  $t_2 = 90ns$ .
- 3) Dynamic resistance calculated from  $I_{TLP} = 4A$  to  $I_{TLP} = 16A$

# Typical Characteristics

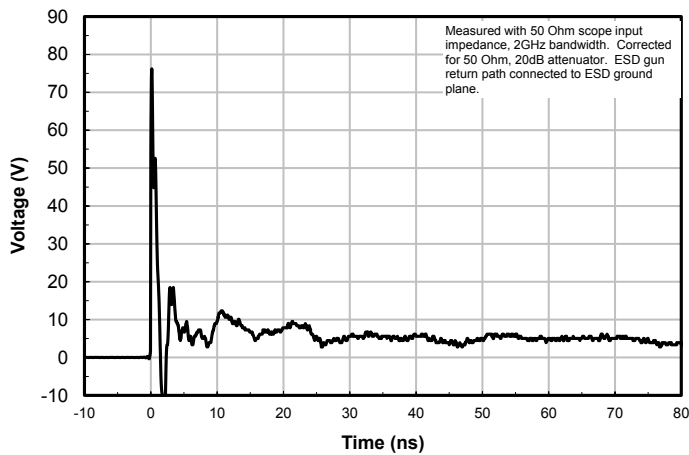
**Clamping Voltage vs. Peak Pulse Current  
(Between any I/O and Ground)**



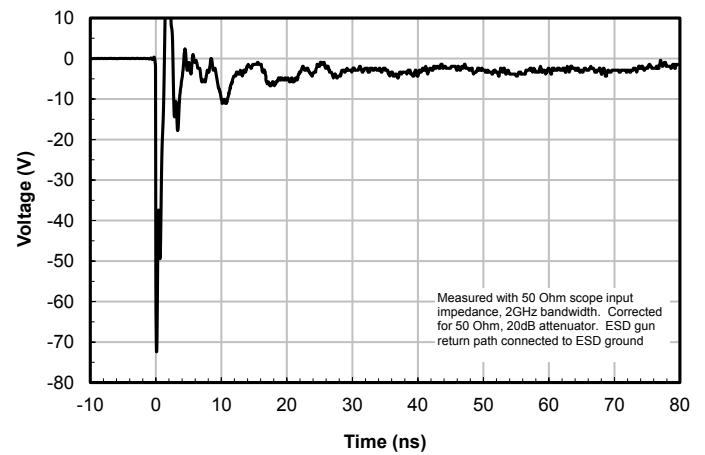
**Junction Capacitance vs. Reverse Voltage  
(Between any I/O and Ground)**



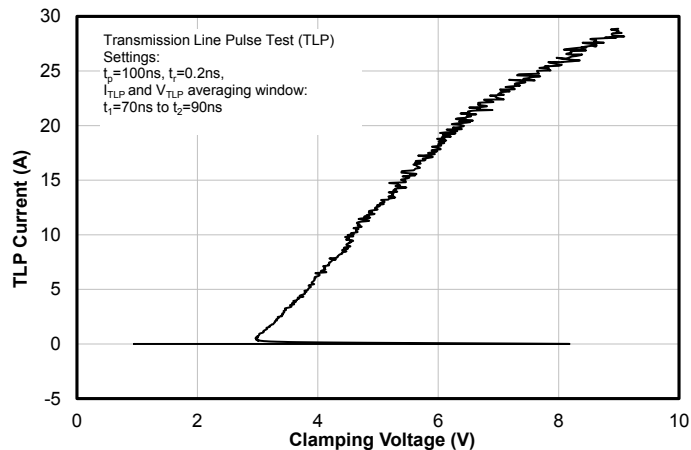
**ESD Clamping (+8kV Contact per IEC 61000-4-2)  
(Between any I/O and Ground)**



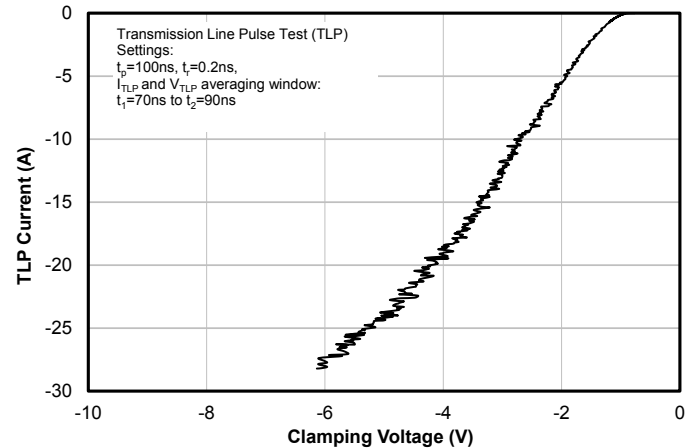
**ESD Clamping (-8kV Contact per IEC 61000-4-2)  
(Between any I/O and Ground)**



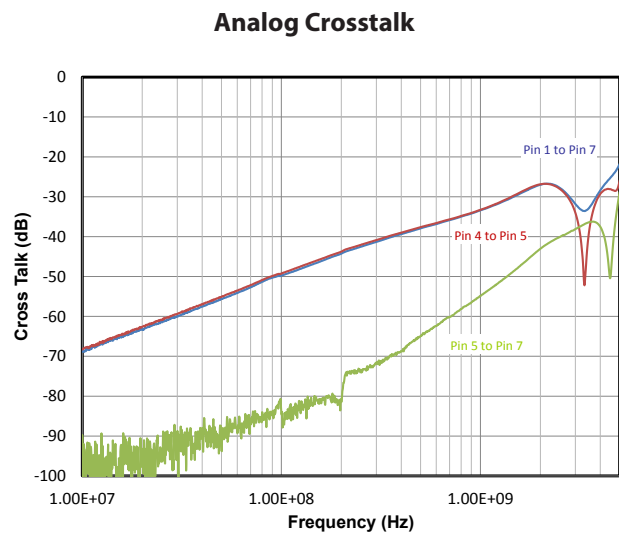
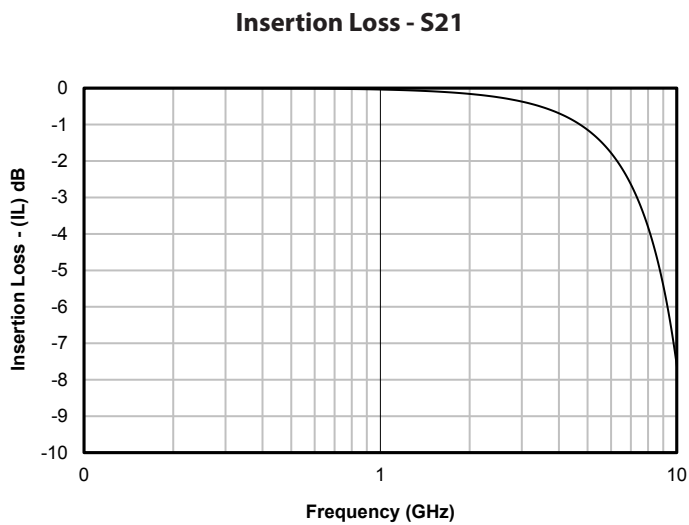
**TLP Characteristic (Positive)**



**TLP Characteristic (Negative)**



# Typical Characteristics (Continued)



# Application Information

## Protecting USB 3.0 Ports

RClamp3346P is designed to protect all six USB 3.0 SuperSpeed and high speed differential lines. PCB traces enter and exit each I/O pin and ground is connected at pin 2. For best results, it is recommended that the ground connection be made using a filled via-in-pad. The via should be filled with a conductive paste. This technique saves board space and reduces parasitic inductance in the ground path. Figures 2 and 3 are examples of how to route high speed differential traces through the RClamp3346P. Differential impedance of each pair can easily be controlled for USB 3.0 (85 Ohms +/- 15%).

The RClamp3346P should be placed as close to the connector as possible for optimum ESD performance. Internal construction of the RClamp3346P has been optimized to minimize series inductance within the package. This helps to reduce the ESD peak clamping voltage. Dynamic resistance is extremely low (typically 0.15 Ohms) further reducing the ESD clamping voltage.

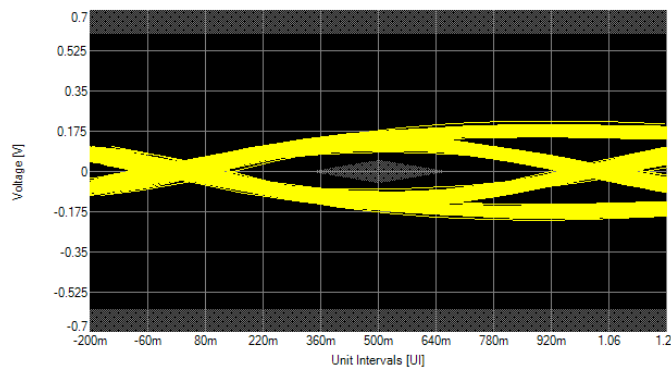


Figure 1 - USB 3.0 Eye Diagram with RClamp3346P

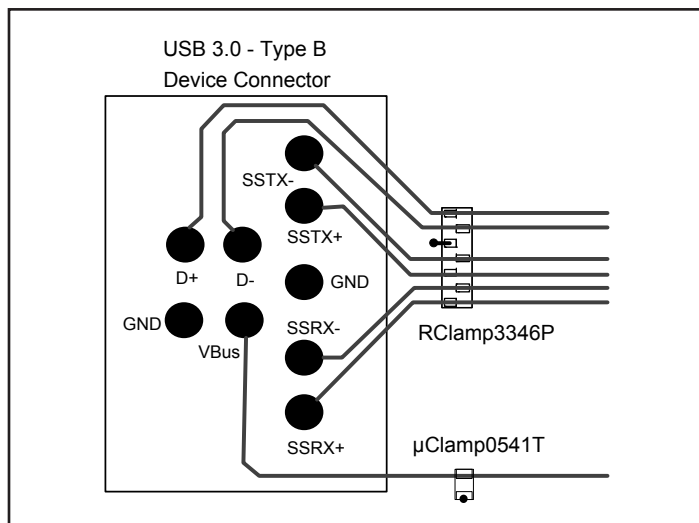


Figure 2 - Example USB 3.0 Layout  
(Type B Device Connector)

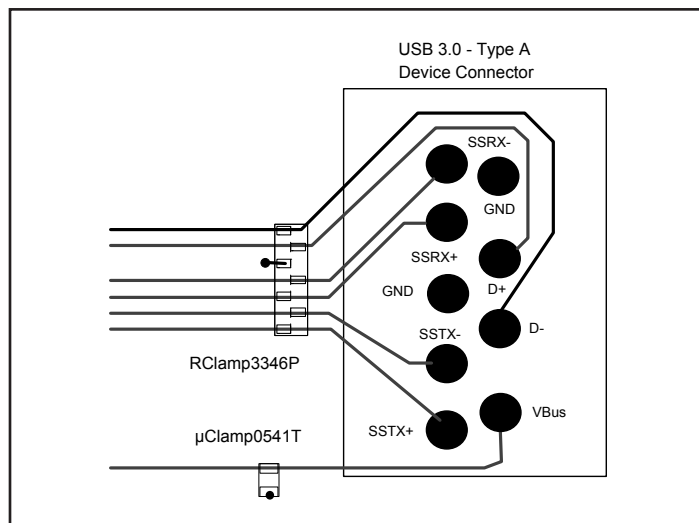


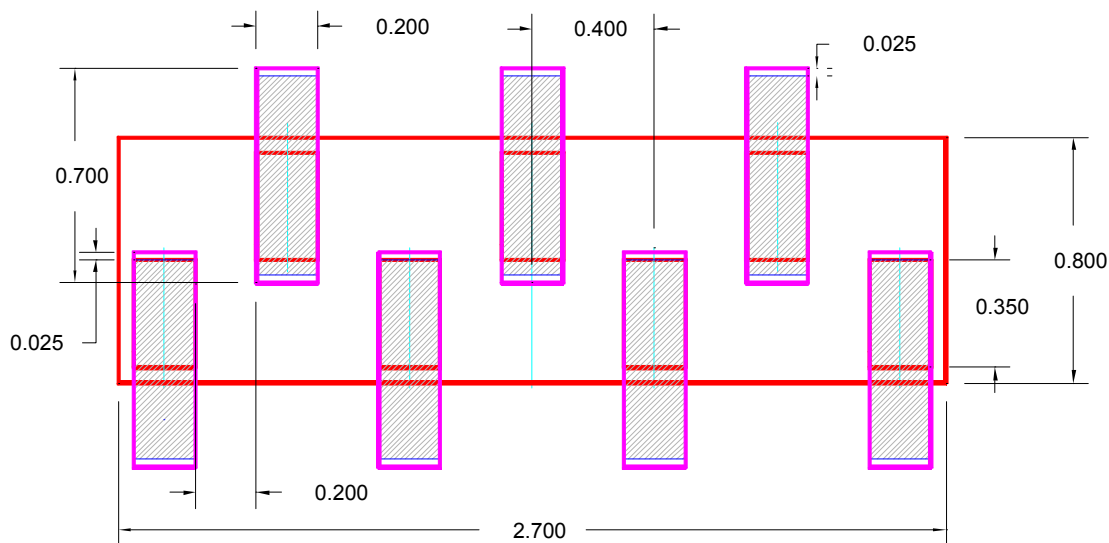
Figure 3 - Example USB 3.0 Layout  
(Type A Device Connector)

# Application Information

## Assembly Guidelines

The small size of this device means that some care must be taken during the mounting process to insure reliable solder joint. Semtech’s recommended assembly guidelines for mounting this device are shown in the Table 1. Figure 4 details Semtech’s recommended aperture. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. Exact manufacturing parameters will require some experimentation to get the desired solder application.

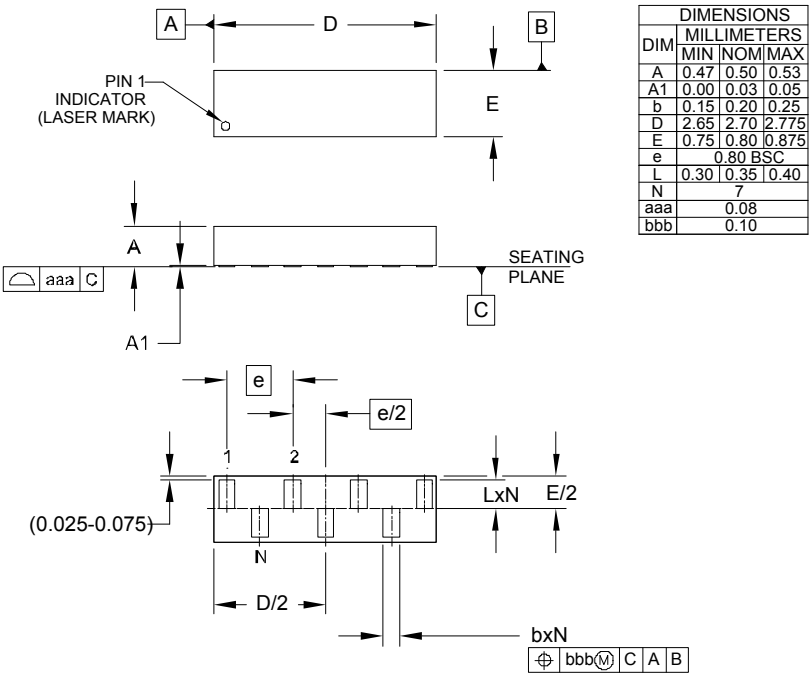
Assembly Parameter	Recommendation
Solder Stencil Design	Laser cut, Electro-Polished
Aperture shape	Rectangular with rounded corners
Solder Stencil Thickness	0.100 mm (0.004")
Solder Paste Type	Type 4 size sphere or smaller
Solder Reflow Profile	Per JEDEC J-STD-020
PCB Solder Pad Design	Non-Solder mask defined
PCB Pad Finish	OSP OR NiAu



All Dimensions are in mm.

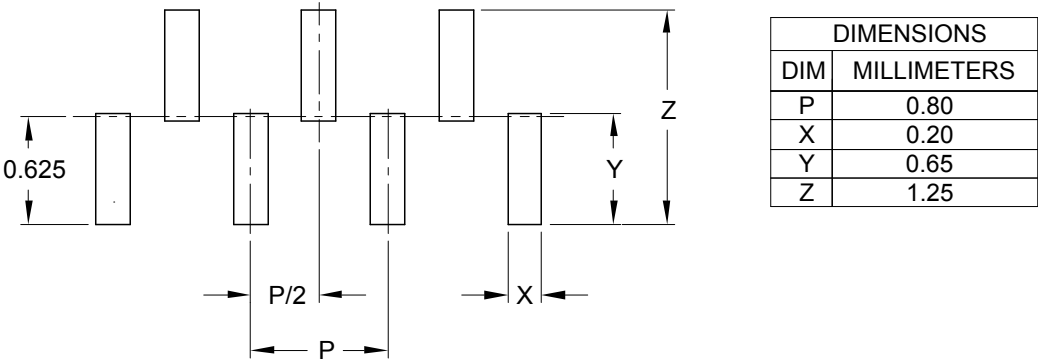
Land Pad. Stencil opening Component

# Outline Drawing - SGP2708N7



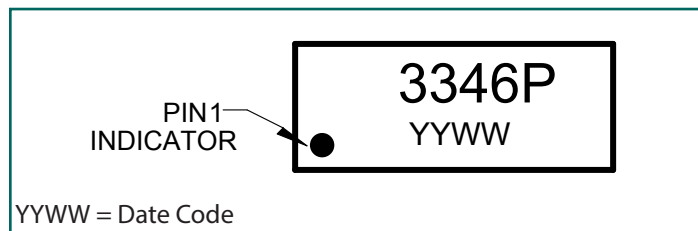
- NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

# Land Pattern - SGP2708N7

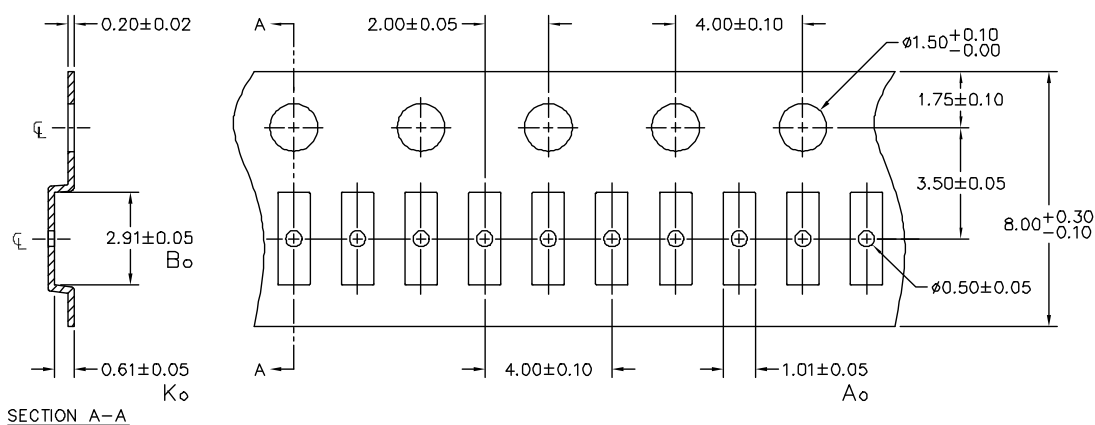


- NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
  2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.  
CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

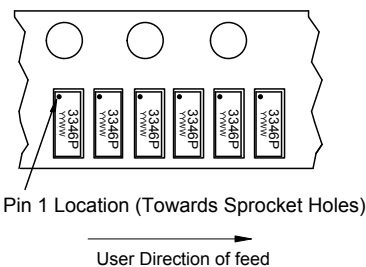
## Marking Code



## Tape and Reel Specification



NOTES: 1.) ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.



## Ordering Information

Part Number	Qty per Reel	Reel Size
RClamp3346P.TNT	10,000	7"





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