TS80000

High Efficiency Transmitter Controller for Wireless Power Systems

POWER PRODUCTS

Features

- Supports Qi®, PMA and proprietary charging applications
- Power outputs up to 40W+
- Support for single and multi-coil applications
- Support for half and full-bridge power sections
- Support for variable voltage, variable frequency and variable duty cycle architectures
- Integrated controller and flash for communications and control
- High precision data converters
- Precise control of bridge duty cycle and frequency
- Low external component count
- RISC-based controller core with flash and SRAM memory
- Two 12-bit A/D converters
- DMA controller
- Three 16-bit timers, each with up to 4 IC/OC/PWM or pulse counter
- Dual 16-bit PWM timers with dead-time generation
- 3 AGPIO and 5 GPIO for application customization
- I2C or UART interface
- USB interface
- 36 pin 6x6 QFN

Description

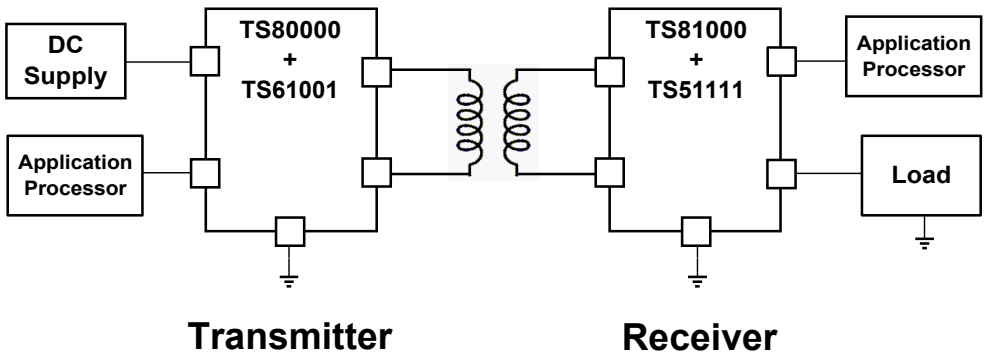
The TS80000 is a power transmitter communications and control unit for wireless charging applications. The TS80000 can support power outputs up to 40W+, and supports Qi® compliant, PMA compliant and proprietary applications. The TS80000 can be configured to drive single or multi-coil applications, in half and full-bridge systems.

The TS80000 performs the necessary decode of packets from the secondary side device and adjusts the control accordingly. An integrated PID filter provides the necessary compensation for the loop for high-precision control of duty cycle, frequency, and or bridge voltage.

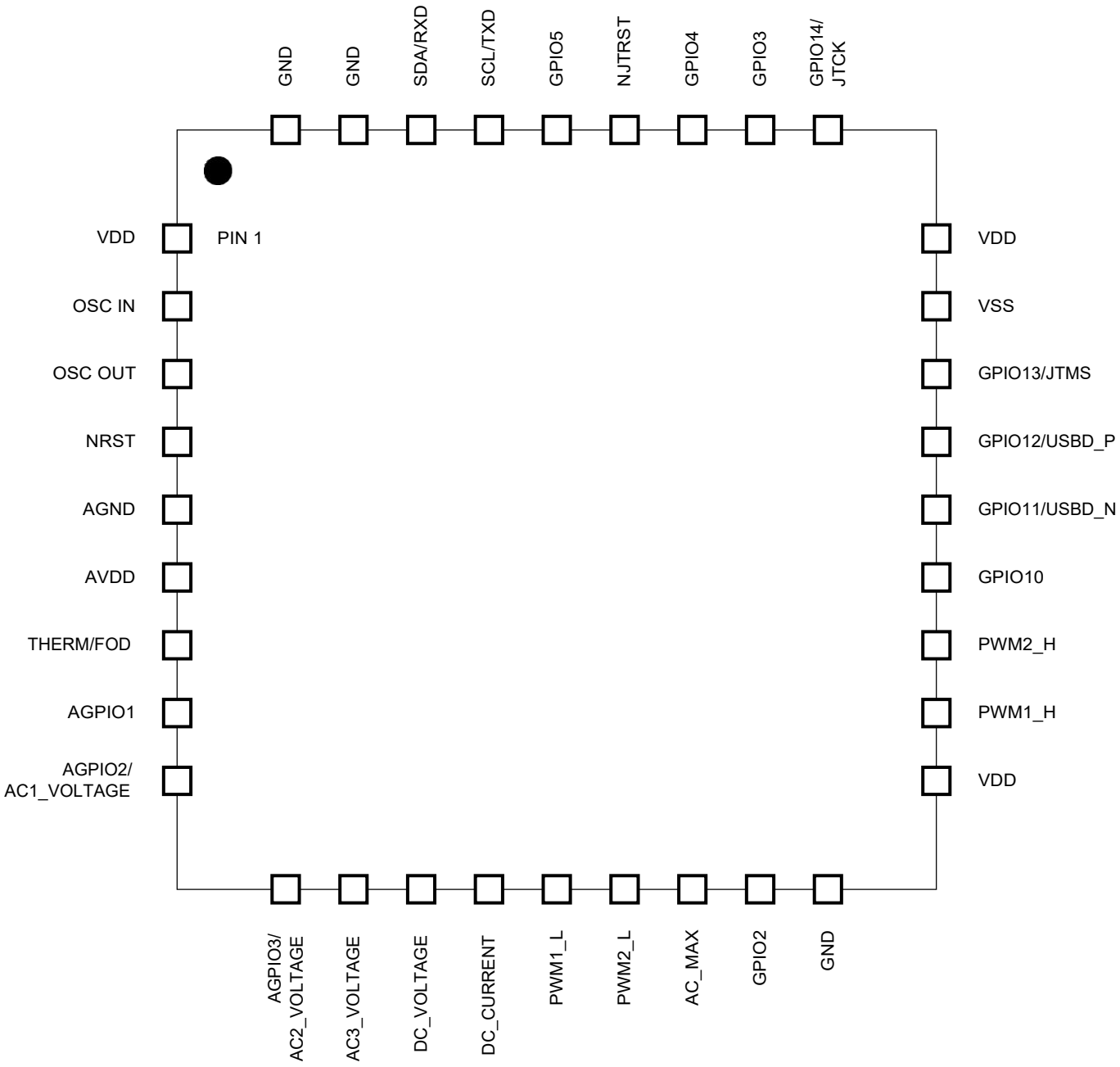
Applications

- Qi® and non-standard wireless chargers for:
  - Cell Phones and Smartphones
  - GPS Devices
  - Digital Cameras
  - Tablets and eReaders
  - Portable Lighting
  - Industrial applications

Typical Application Circuit



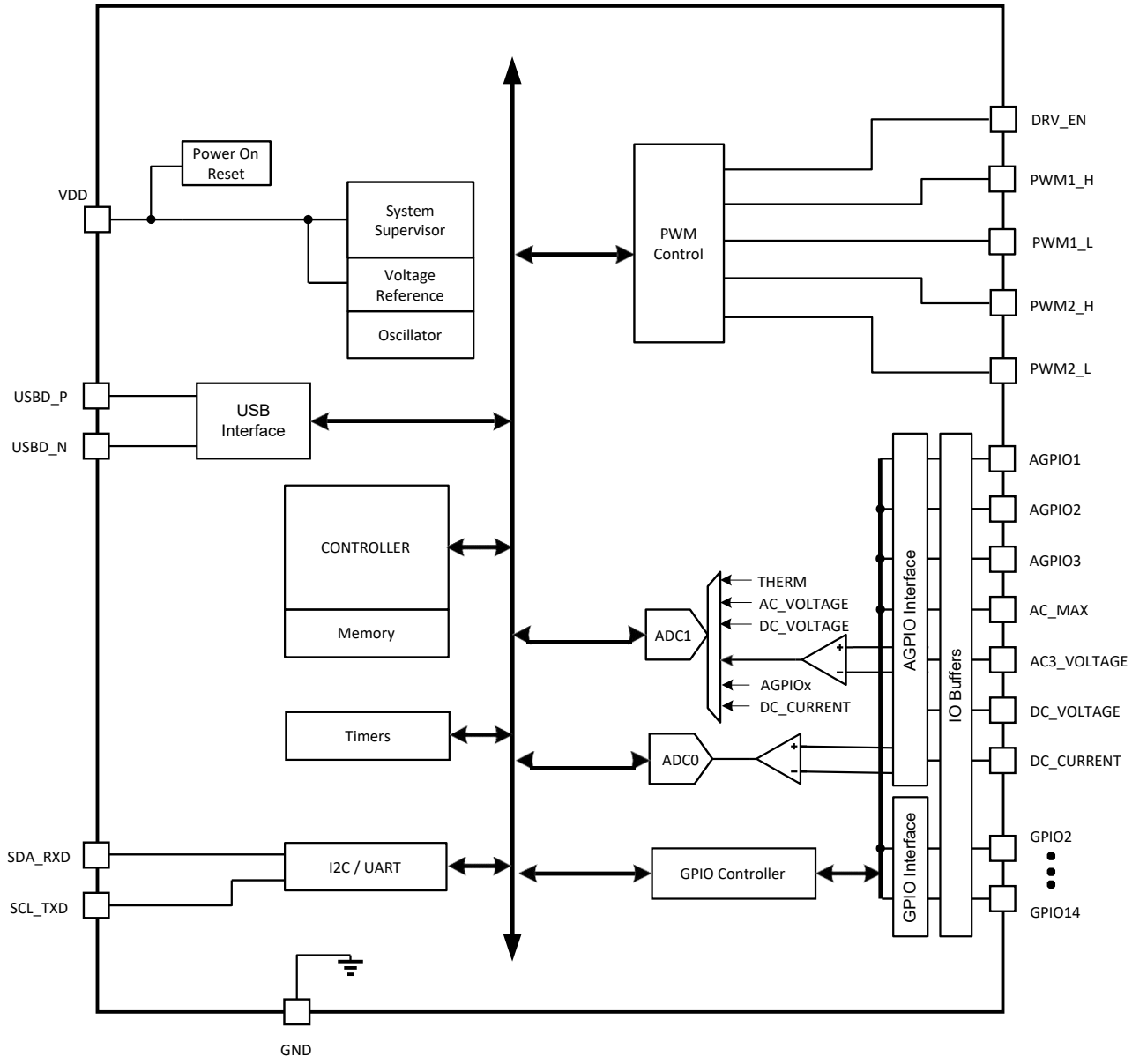
Pinout(Top View)



Pin Description

Pin #	Pin Name	Pin Function	Description
1	VDD	Input power	Input power supply
2	OSC_IN	Oscillator input	Oscillator input
3	OSC_OUT	Oscillator output	Oscillator output
4	NRST	Reset	Reset input
5	AGND	Analog GND	Analog GND
6	AVDD	Analog power	Analog power supply
7	THERM/FOD	Thermistor/FOD	Thermistor input or FOD calibration input
8	AGPIO1	Analog GPIO	Analog GPIO1
9	AGPIO2/ AC1_VOLTAGE	Analog GPIO	Analog GPIO2 or AC coil voltage for coil #1 in a three-coil system
10	AGPIO3/ AC2_VOLTAGE	Analog GPIO	Analog GPIO3 or AC coil voltage for coil #2 in a three-coil system
11	AC3_VOLTAGE	Analog GPIO	AC coil voltage for a single-coil system or AC coil voltage for coil #3 in a three-coil system
12	DC_VOLTAGE	Analog GPIO	DC input voltage measurement
13	DC_CURRENT	Analog GPIO	DC input current measurement
14	PWM1_L	PWM output	PWM1 low-side control
15	PWM2_L	PWM output	PWM2 low-side control
16	AC_MAX	Analog GPIO	Communication demodulator input
17	DRV_EN	Drive enable	FET driver enable
18	GND	Power GND	Power GND
19	VDD	Input power	Input power supply
20	PWM1_H	PWM	PWM1 high-side control
21	PWM2_H	PWM	PWM2 high-side control
22	GPIO10	GPIO	GPIO10
23	GPIO11/USBD_N	GPIO/USB data	GPIO11 or USB data input (D-)
24	GPIO12/USBD_P	GPIO/USB data	GPIO12 or USB data input (D+)
25	GPIO13/JTMS	GPIO/JTAG	GPIO13 or JTAG state machine control
26	GND	Power GND	Power GND
27	VDD	Input power	Input power supply
28	GPIO14/JTCK	GPIO/JTAG	GPIO14 or JTAG clock
29	GPIO15	GPIO	GPIO15
30	GPIO3	GPIO	GPIO3
31	GPIO4	GPIO	GPIO4
32	GPIO5	GPIO	GPIO5
33	SCL/TXD	I2C/UART	I2C clock or UART output
34	SDA/RXD	I2C/UART	I2C data or UART input
35	GND	Power GND	Power GND
36	GND	Power GND	Power GND

Functional Block Diagram



Absolute Maximum Rating

Over operating free–air temperature range unless otherwise noted [1,2,3]

Parameter	Min	Max	Unit
VDD, AVDD, GND, AGND (supply voltage)	-0.3	4.0	V
OSC_IN, OSC_OUT, DRV_EN, PWM1_H, PWM2_H, GPIO10, GPIO11/USBD_N, GPIO12/ USBD_P, GPIO13/JTMS, GPIO3, GPIO4, SCL/TXD, SDA/RXD	GND - 0.3	VDD + 4.0	V
NRST, THERM/FOD, AGPIO1, AGPIO2/AC1_VOLTAGE, AGPIO3/AC2_VOLTAGE, AC3_ VOLTAGE, DC_VOLTAGE, DC_CURRENT, PWM1_L, PWM2_L, AC_MAX, GPIO14/JTCK, GPIO15, GPIO5	GND - 0.3	4.0	V
Operating Junction Temperature Range, TJ	-40	125	°C
Storage Temperature Range, TSTG	-65	150	°C
Electrostatic Discharge – Human Body Model		±2k	V
IR Reflow Temperature (soldering, 10 seconds)		260	°C

Notes:

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Input Operating Voltage	VDD / AVDD	2.0	3.3	3.6	V
Oscillator Frequency	F_{OSC}		8.0		MHz
Analog Supply decoupling capacitor values	AVDD		100		nF
			4.7		nF
			4.7		uF
Digital Supply decoupling capacitor values	VDD		3 x 100		nF
			4.7		
Operating Free Air Temperature	T_A	-40			uF
Operating Junction Temperature	T_J	-40		85	°C
				105	°C

Communication Interfaces

The Applications Processor can interrogate the TS8000x using the I2C or UART interface. The two interfaces share the same pins. Only one interface is active at any time.

I2C

I/O Pins

ALERT pin (optional):

- Driven high when an event is active in the internal STATUS register
- Driven low when all the internal events are cleared

Note: The ALERT pin is provided to help with I2C communication, i.e. to signal events to the App. MCU so the App. MCU can interrogate the TS80000 via I2C to see what changed on the wireless interface. The use of the ALERT pin is not mandatory in the application.

SCL pin:

- Clock pin for the I2C interface.
- Open-drain with weak pull-ups. Needs stronger external pull-ups for full-speed operation.

SDA pin:

- Data pin for the I2C interface.
- Open-drain with weak pull-ups. Needs stronger external pull-ups for full-speed operation.

I2C Protocol

The TS80000 Wireless Power Transmitter Controller acts as an I2C slave peripheral to allow communication with an application microcontroller. The slave address (7 bit) is 0x50. The Application MCU is an I2C master and initiates every data transfer.

The TS80000 implements a set of registers available from the I2C bus. It also implements a set of API functions that receive parameters and return values using the I2C bus. Four transfer types are possible:

- Write Register
- Read Register
- Run API Function
- Read API Function Return Buffer

Write Register Operations				Description
START				Start of the I2C transfer.
M➔S	Slave Address (7 bits)	0 (1 bit)	Slave ACK	Slave address + R/nW bit (0xA0 as 8-bit)
M➔S	Register n address (8 bits)		Slave ACK	Address of the first register
M➔S	Register n Data (8 bits)		Slave ACK	Write the first register
M➔S	Register n+1 Data (8 bits)		Slave ACK	Optionally write the following registers
	…			
M➔S	Register n+k Data (8 bits)		Slave ACK	
STOP				Stop of the I2C transfer

Read Register Operations				Description
START				Start of the I2C transfer.
M➔S	Slave Address (7 bits)	0 (1 bit)	Slave ACK	Slave address + 0 as R/nW bit (0xA0 as 8-bit)
M➔S	Register n address (8 bits)		Slave ACK	Address of the first register
START				Repeated Start
M➔S	Slave Address (7 bits)	1 (1 bit)	Slave ACK	Slave address + 1 as R/nW bit (0xA1 as 8-bit)
S➔M	Register n Data (8 bits)		Master ACK	Read the first register
S➔M	Register n+1 Data (8 bits)		Master ACK	Optionally read the following registers
	…			
S➔M	Register n+k Data (8 bits)		Master nACK	The master should send a nACK after the last data byte was received.
STOP				Stop of the I2C transfer

Run API Function				Description
START				Start of the I2C transfer
M➔S	Slave Address (7 bits)	0 (1 bit)	Slave ACK	Slave address + R/nW bit (0xA0 as 8-bit
M➔S	API number (8 bits)		Slave ACK	API number
M➔S	API input buffer length m (8 bits)		Slave ACK	API input buffer length. Equal to 0 if no input buffer data is required by the API
M➔S	Input buffer data[0] (8 bits)		Slave ACK	First byte of the input buffer (optional)
M➔S	Input buffer data[1] (8 bits)		Slave ACK	Second byte of the input buffer (optional)
	…			
M➔S	Input buffer data[m-1] (8 bits)		Slave ACK	Last byte of the input buffer (optional)
STOP				Stop of the I2C transfer and execute the API function

Read API Function Return Buffer				Description
START				Start of the I2C transfer.
M➔S	Slave Address (7 bits)	0 (1 bit)	Slave ACK	Slave address + 0 as R/nW bit (0xA0 as 8-bit)
M➔S	API number (8 bits)		Slave ACK	API number.
START				Repeated Start
M➔S	Slave Address (7 bits)	1 (1 bit)	Slave ACK	Slave address + 1 as R/nW bit (0xA1 as 8-bit)
S➔M	API number (8 bits)		Master ACK	API number for the following return buffer
S➔M	API return buffer length n (8 bits)		Master ACK	API return buffer length
S➔M	Output buffer data[0] (8 bits)		Master ACK	Read the first byte in the output buffer
S➔M	Output buffer data[1] (8 bits)		Master ACK	Optionally read the following bytes
	…			
S➔M	Output buffer data[n-1] (8 bits)		Master nACK	The master should send a nACK after the last data byte was received.
STOP				Stop of the I2C transfer

Internal Registers

Addresss	Name	Type	Access Mode (bits)	Description
General Registers				
0x00	BOOTFW_REV_L	R	8 / 16	Bootloader Firmware Revision (L)
0x01	BOOTFW_REV_H	R	8 / 16	Bootloader Firmware Revision (H)
0x02	FW_REV_L	R	8 / 16	Firmware Revision (L)
0x03	FW_REV_H	R	8 / 16	Firmware Revision (H)
0x04	MODE_L	R	8 / 16	Operating Mode (L)
0x05	MODE_H	R	8 / 16	Operating Mode (H)
0x06	RESET_L	R/W	8 / 16	Reset Register (L)
0x07	RESET_H	R/W	8 / 16	Reset Register (H)
0x08	STATUS0	R	8	Status0 Register
0x09	STATUS1	R	8	Status1 Register
0x0A	STATUS2	R	8	Status2 Register
0x0B	STATUS3	R	8	Status3 Register
0x0C	RESERVED			
Bootloader Mode				
0x0D	BLOCK_SIZE	R	8	Block Size
0x0E	FW_SIZE_L	R	8 / 16	Firmware Size (L)
0x0F	FW_SIZE_H	R	8 / 16	Firmware Size (H)
0x10	CONFIG_SIZE_L	R	8 / 16	Configuration Size (L)
0x11	CONFIG_SIZE_H	R	8 / 16	Configuration Size (H)
0x12	CALIBRATION_SIZE_L	R	8 / 16	Calibration Size (L)
0x13	CALIBRATION_SIZE_H	R	8 / 16	Calibration Size (H)
0x14	FW_FLAGS_L	R	8 / 16	Firmware Flags (L)
0x15	FW_FLAGS_H	R	8 / 16	Firmware Flags (H)
0x16-0x7F	RESERVED			
Transmitter Mode				
0x0D	CHANNEL_COUNT	R	8	Channel Count
0x0E	CHANNEL_SELECT	R/W	8	Channel Selection Register
0x0F	COIL_COUNT	R	8	Coil Count
0x10	FREQ_MIN_LIMIT_L	R/W	16	Limit for the Minimum Frequency (L)
0x11	FREQ_MIN_LIMIT_H	R/W	16	Limit for the Minimum Frequency (H)
0x12	FREQ_MAX_LIMIT_L	R/W	16	Limit for the Maximum Frequency (L)
0x13	FREQ_MAX_LIMIT_H	R/W	16	Limit for the Maximum Frequency (H)
0x14	DC_CURRENT_LIMIT_L	R/W	16	DC Current Limit (L)
0x15	DC_CURRENT_LIMIT_H	R/W	16	DC Current Limit (H)
0x16	AC_VOLTAGE_LIMIT_L	R/W	16	AC Voltage Limit (L)
0x17	AC_VOLTAGE_LIMIT_H	R/W	16	AC Voltage Limit (H)
0x18	TEMP_COIL_LIMIT_L	R/W	16	Coil Temperature Limit (L)
0x19	TEMP_COIL_LIMIT_H	R/W	16	Coil Temperature Limit (H)
0x1A	TEMP_DIE_LIMIT_L	R/W	16	Die Temperature Limit (L)
0x1B	TEMP_DIE_LIMIT_H	R/W	16	Die Temperature Limit (H)
0x1C	FAN_TEMP_MIN	R/W	8	Minimum Temperature for Fan Control
0x1D	FAN_TEMP_MAX	R/W	8	Maximum Temperature for Fan Control
0x1E	FAN_DTC_MIN	R/W	8	Minimum Duty Cycle for Fan Control
0x1F	FAN_DTC_MAX	R/W	8	Maximum Duty Cycle for Fan Control
0x20	SUPPORTED_STANDARDS	R/W	8	Supported Standards
0x21	MAX_POWER_WPC	R/W	8	Maximum Power in WPC Mode
0x22	MAX_POWER_PMA	R/W	8	Maximum Power in PMA Mode
0x23	MAX_POWER_A4WP	R/W	8	Maximum Power in A4WP Mode
0x24-0x3F	RESERVED			
0x40	ACTIVE_COIL	R	8	Active Coil
0x41	POWER_STATE_TX	R	8	Transmitter Power State
0x42	STANDARD	R	8	Wireless Power Standard
0x43	POWER_LEVEL	R	8	Power Level
0x44	FOD_TYPE	R	8	Foreign Object Detection Type

Internal Registers

Addresss	Name	Type	Access Mode (bits)	Description
Transmitter Mode continues...				
0x45	POWER_STATE_RX	R	8	Receiver Power State
0x46	PWM_FREQUENCY_L	R	16	PWM Frequency (L)
0x47	PWM_FREQUENCY_H	R	16	PWM Frequency (H)
0x48	PWM_DTC_L	R	16	PWM Duty Cycle (L)
0x49	PWM_DTC_H	R	16	PWM Duty Cycle (H)
0x4A	DC_VOLTAGE_L	R	16	Bridge DC Voltage (L)
0x4B	DC_VOLTAGE_H	R	16	Bridge DC Voltage (H)
0x4C	DC_CURRENT_L	R	16	Bridge DC Current (L)
0x4D	DC_CURRENT_H	R	16	Bridge DC Current (H)
0x4E	AC_VOLTAGE_L	R	16	Coil AC voltage (L)
0x4F	AC_VOLTAGE_H	R	16	Coil AC Voltage (H)
0x50	AC_CURRENT_L	R	16	Coil AC Current (L)
0x51	AC_CURRENT_H	R	16	Coil AC Current (H)
0x52	TEMP_COIL_L	R	16	Temperature at the Coil Thermistor (L)
0x53	TEMP_COIL_H	R	16	Temperature at the Coil Thermistor (H)
0x54	TEMP_DIE_L	R	16	Die Temperature (L)
0x55	TEMP_DIE_H	R	16	Die Temperature (H)
0x56	POWER_DC_IN_L	R	16	DC Power at the Bridge Input (L)
0x57	POWER_DC_IN_H	R	16	DC Power at the Bridge Input (H)
0x58	POWER_TX_L	R	16	TX Power into the Magnetic Field (L)
0x59	POWER_TX_H	R	16	TX Power into the Magnetic Field (H)
0x5A	POWER_RX_L	R	8	Received Power Reported by the RX (L)
0x5B	POWER_RX_H	R	8	Received Power Reported by the RX (H)
0x5C	BATT_CHARGE_LEVEL_RX	R	8	Receiver Battery Charge Level
0x5D	LED_STATE	R	8	LED State
0x5E	ERROR_L	R	16	Error Code and Parameter (L)
0x5F	ERROR_H	R	16	Error Code and Parameter (H)
0x60-0x6F	RESERVED			
0x70	CONTROL_POWER_L	R/W	16	Power Control Register (L)
0x71	CONTROL_POWER_H	R/W	16	Power Control Register (H)
0x72	CONTROL_DEBUG_L	R/W	16	Debug Control Register (L)
0x73	CONTROL_DEBUG_H	R/W	16	Debug Control Register (H)
0x74	DEBUG_MASK0	R/W	8	Debug Mask Register 0
0x75	DEBUG_MASK1	R/W	8	Debug Mask Register 1
0x76	DEBUG_MASK2	R/W	8	Debug Mask Register 2
0x77	DEBUG_MASK3	R/W	8	Debug Mask Register 3
0x78	INTERRUPT_MASK0	R/W	8	Interrupt Mask Register 0
0x79	INTERRUPT_MASK1	R/W	8	Interrupt Mask Register 1
0x7A	INTERRUPT_MASK2	R/W	8	Interrupt Mask Register 2
0x7B	INTERRUPT_MASK3	R/W	8	Interrupt Mask Register 3
0x7C-0x7F	RESERVED			

Bootloader Firmware Revision Register (BOOTFW_REV_H:BOOTFW_REV_L)

Address: 0x00

Reset value: Major and Minor version number of the bootloader firmware

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REV_H[7:0]								REV_L[7:0]							
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bits 15:8 REV_H[7:0]: Major Bootloader Firmware Revision

These bits contain the major version number of the bootloader firmware.

Bits 7:0 REV_L[7:0]: Minor Bootloader Firmware Revision

These bits contain the minor version number of the bootloader firmware.

Firmware Revision Register (FW_REV_H:FW_REV_L)

Address: 0x02

Reset value: Major and Minor version number of the transmitter firmware

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REV_H[7:0]								REV_L[7:0]							
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bits 15:8 REV_H[7:0]: Major Firmware Revision

These bits contain the major version number of the transmitter firmware.

Bits 7:0 REV_L[7:0]: Minor Firmware Revision

These bits contain the minor version number of the transmitter firmware.

Operating Mode Register (MODE_H:MODE_L)

Address: 0x04

Reset value: Depends on the bootloader mode and the firmware type

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															BOOT LDR
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bits 16:1 Reserved

Bit 0 BOOTLDR: Bootloader mode

0: The transmitter firmware is running

1: The controller is in bootloader mode

Reset Register (RESET_H:RESET_L)

Address: 0x06

Reset value: 0x00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET_KEY[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 15:0 RESET_KEY[15:0]: Reset Key

0xAA55: generate a system reset

0xA5A5: generate a system reset and enter bootloader mode

Any other value: a system reset is not generated

The reset sequence takes about 20 milliseconds. During this time the communication interfaces are not available.

After reset the MODE register can be used to check if the system is in bootloader mode or is running the transmitter firmware.

Status0 Register(STATUS0)

Address: 0x08

Reset value: 0xC0

7	6	5	4	3	2	1	0
CTS	CTS_API	CTS_IF	CTS_API_IF	STATUS3	STATUS2	STATUS1	Res
r	r	r	r	r	r	r	

Bit 7 CTS: Clear To Send

This bit indicates if a new read/write register access can be issued to the controller. This bit is not reset by hardware when read.

0: The controller is busy processing a previous register access. New commands should not be sent to the controller.

1: The controller can accept a new register access command over the communication interface.

Bit 6 CTS_API: Clear to Send for API

This bit indicates if a new API call or API read request can be issued to the controller. This bit is not reset by hardware when read.

0: The controller is busy processing a previous API call. New API calls should not be sent to the controller.

1: The controller can accept a new API call over the communication interface.

Bit 5 CTS_IF: Clear To Send Event Interrupt Flag

0: No event is signaled for the CTS bit or the corresponding bit in the INTERRUPT_MASK0 register is cleared.

1: The CTS bit has been set and the corresponding bit in the INTERRUPT_MASK0 register is set. Reset to 0 by hardware when the STATUS0 register is read.

Bit 4 CTS_API_IF: Clear to Send for API Event Interrupt Flag

0: No event is signaled for the CTS_API bit.

1: The CTS_API bit has been set and the corresponding bit in the INTERRUPT_MASK0 register is set. Reset to 0 by hardware when the STATUS0 register is read.

Bit 3 STATUS3_IF: STATUS1 Event Interrupt Flag

0: No event is signaled in the STATUS3 register or the corresponding bit in the INTERRUPT_MASK0 register is cleared.

1: An event is signaled in the STATUS3 register and the corresponding bit in the INTERRUPT_MASK3 register is set. Reset to 0 by hardware when the STATUS3 register is read.

Bit 2 STATUS2_IF: STATUS2 Event Interrupt Flag

0: No event is signaled in the STATUS2 register or the corresponding bit in the INTERRUPT_MASK0 register is cleared.

1: An event is signaled in the STATUS2 register and the corresponding bit in the INTERRUPT_MASK2 register is set. Reset to 0 by hardware when the STATUS2 register is read.

Bit 1 STATUS1_IF: STATUS1 Event Interrupt Flag

0: No event is signaled in the STATUS1 register or the corresponding bit in the INTERRUPT_MASK0 register is cleared.

1: An event is signaled in the STATUS1 register and the corresponding bit in the INTERRUPT_MASK1 register is set. Reset to 0 by hardware when the STATUS1 register is read.

Bit 0 Reserved

Status1 Register(STATUS1)

Address: 0x09

Reset value: 0x00

7	6	5	4	3	2	1	0
Res		RX_EOC	RX_CHG	RX_CONFIG	RX_ID	RX_RMV	RX_DET
		r	r	r	r	r	r

Bits 7:4 Reserved

Bit 5 RX_EOC: RX End of Charge Received
0: No RX End of Charge command has been received since the last read.
1: The RX End of Charge command has been received. Reset to 0 by hardware when read.

Bit 4 RX_CHG: RX Charge Level Received
0: No RX charge level has been received since the last read.
1: The RX charge level has been received. Reset to 0 by hardware when read.

Bit 3 RX_CONFIG: RX Configuration Received
0: No RX configuration data has been received since the last read.
1: The RX configuration phase has completed. Reset to 0 by hardware when read.

Bit 2 RX_ID: RX Identification Received
0: No RX identification data has been received since the last read.
1: The RX identification phase has completed. Reset to 0 by hardware when read.

Bit 1 RX_RMV: RX Removed
0: No RX removal event has occurred since the last read.
1: The RX device has been removed from the TX surface. Reset to 0 by hardware when read.

Bit 0 RX_DET: RX Detected
0: No RX detection event has occurred since the last read.
1: A RX device has been detected on the transmitter surface. Reset to 0 by hardware when read.

Status2 Register(STATUS2)

Address: 0x0A

Reset value: 0x00

7	6	5	4	3	2	1	0
Res						LED	ERROR
						r	r

Bits 7:2 Reserved

Bit 1 LED: LED Status Changed
0: No change in the LED state has occurred since the last read.
1: A change in the LED state has occurred. Reset to 0 by hardware when read.

Bit 0 ERROR: Error Condition Detected
0: No error has occurred since the last read.
1: An error has occurred. Reset to 0 by hardware when read.

Status3 Register(STATUS3)

Address: 0x0B

Reset value: 0x00

7	6	5	4	3	2	1	0
Res						LED	ERROR
						r	r

Bits 7:2 Reserved

Bit 1 TEST: Test Event
0: No test event has occurred since the last read.
1: A test event has occurred. Reset to 0 by hardware when read.

Bit 0 DEBUG: Debug Event
0: No debug event has occurred since the last read.
1: A debug event has occurred. Reset to 0 by hardware when read.

Block Size Register (BLOCK_SIZE)

Address: 0x0D

Reset value: 0x40

7	6	5	4	3	2	1	0
BLOCK_SIZE[7:0]							
r	r	r	r	r	r	r	r

Bits 7:0 BLOCK_SIZE[7:0]: FLASH Block Size

This field reports the length of the FLASH block size in bytes.

The following FLASH API functions should use a BLOCK_DATA field with a size that is equal to BLOCK_SIZE (or optionally for USB communication, a multiple of BLOCK_SIZE):

- BOOTLOADER_WRITE_BLOCK
- BOOTLOADER_WRITE_CONFIGURATION
- BOOTLOADER_READ_CONFIGURATION
- BOOTLOADER_WRITE_CALIBRATION
- BOOTLOADER_READ_CALIBRATION
- BOOTLOADER_TRIM
- BOOTLOADER_READ_TRIM

Firmware Size Register (FW_SIZE_H:FW_SIZE_L)

Address: 0x0E

Reset value: Size of the firmware image segment (unit: number of blocks)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FW_SIZE[15:0]															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bits 15:0 FW_SIZE[15:0]: Size of the firmware image segment (blocks)

These bits contain size of the firmware image segment in FLASH measured as a number of BLOCK_SIZE byte long blocks.

Example: if BLOCK_SIZE = 64 and the firmware image segment is 51KB (52224 bytes) then FW_SIZE is 52224 / 64 =816.

Configuration Size Register (CONFIG_SIZE_H:CONFIG_SIZE_L)

Address: 0x10

Reset value: Size of the configuration image segment (unit: number of blocks)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONFIG_SIZE[15:0]															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bits 15:0 CONFIG_SIZE[15:0]: Size of the configuration image segment (blocks)

These bits contain size of the configuration image segment in FLASH measured as a number of BLOCK_SIZE byte long blocks (see the FW_SIZE for details).

Calibration Size Register (CAL_SIZE_H:CAL_SIZE_L)

Address: 0x12

Reset value: Size of the configuration image segment (unit: number of blocks)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAL_SIZE[15:0]															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bits 15:0 CAL_SIZE[15:0]: Size of the calibration image segment (blocks)

These bits contain size of the calibration image segment in FLASH measured as a number of BLOCK_SIZE byte long blocks (see the FW_SIZE for details).

Firmware Flags Register (FW_FLAGS_H:FW_FLAGS_L)

Address: 0x14

Reset value: Firmware flags

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bits 15:0 Reserved

Channel Count Register (CHANNEL_COUNT)

Address: 0x0D

Reset value: From the configuration data

7	6	5	4	3	2	1	0
CHANNEL_COUNT[7:0]							
r	r	r	r	r	r	r	r

Bits 7:0 CHANNEL_COUNT[7:0]: Number of independent transmitter channels

A transmitter has multiple channels if it can transfer power through multiple coils at the same time.

Channel Selection Register (CHANNEL_SELECT)

Address: 0x0E

Reset value: 0x00

7	6	5	4	3	2	1	0
CHANNEL_SELECT[7:0]							
rw	rw	rw	rw	rw	rw	rw	rw

Bits 7:0 CHANNEL_SELECT[7:0]: Number of independent transmitter channels
For transmitters with a single channel this register has no effect.
For transmitters with more than one channel this field associates all the other registers with one of the channels:
0x00: Channel 0 selected
0x01: Channel 1 selected
0x02: Channel 2 selected

Coil Count Register (COIL_COUNT)

Address: 0x0F

Reset value: From the configuration data

7	6	5	4	3	2	1	0
CHANNEL_COUNT[7:0]							
r	r	r	r	r	r	r	r

Bits 7:0 COIL_COUNT[7:0]: Number of coils in the transmitter channel:
0x01: 1 coil
0x02: 2 coils
.....
0x07: 7 coils

Limit for the Minimum Frequency Register (FREQ_MIN_LIMIT_H:FREQ_MIN_LIMIT_L)

Address: 0x10

Reset value: From the configuration data

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FREQ_MIN_LIMIT[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 15:0 FREQ_MIN_LIMIT[15:0]: Minimum frequency allowed for the transmitter channel (100 Hz)
The transmitter doesn't allow its operating frequency to go below this limit. The unit is 100 Hz.
If a value higher than the transmitter operating frequency is written to this register, the transmitter adjusts its operating frequency so it falls within the correct boundaries. This mechanism can be used for automotive applications to force the transmitter to avoid certain frequency ranges when other wireless devices are used.

Example: To limit the transmitter frequency to 150 kHz or higher, a value of 1500 is written to the FREQ_MIN_LIMIT register.

Limit for the Maximum Frequency Register (FREQ_MAX_LIMIT_H:FREQ_MAX_LIMIT_L)

Address: 0x12

Reset value: From the configuration data

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FREQ_MIN_LIMIT[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 15:0 FREQ_MAX_LIMIT[15:0]: Maximum frequency allowed for the transmitter channel (100 Hz)
The transmitter doesn't allow its operating frequency to go above this limit. The unit is 100 Hz.
If a value lower than the transmitter operating frequency is written to this register, the transmitter adjusts its operating frequency so it falls within the correct boundaries.

Example: To limit the transmitter frequency to 180 kHz or lower, a value of 1800 is written to the FREQ_MAX_LIMIT register.

DC Current Limit Register (DC_CURRENT_LIMIT_H:DC_CURRENT_LIMIT_L)

Address: 0x14

Reset value: From the configuration data

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DC_CURRENT_LIMIT[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 15:0 DC_CURRENT_LIMIT[15:0]: Maximum DC current allowed into the transmitter bridge (mA)
The transmitter stops the power transfer and reports an error if the bridge current goes above this limit.
A value of 0x0000 disables the limit checking.

Example: To limit the bridge current to 2A, a value of 2000 is written to the DC_CURRENT_LIMIT register.

AC Voltage Limit Register (AC_VOLTAGE_LIMIT_H:AC_VOLTAGE_LIMIT_L)

Address: 0x16

Reset value: From the configuration data

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AC_VOLTAGE_LIMIT[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 15:0 AC_VOLTAGE_LIMIT[15:0]: Maximum AC voltage amplitude allowed at the resonant circuit (10 mV)
The transmitter stops the power transfer and reports an error if the AC voltage amplitude measured at the sensing point of the AC resonant circuit goes above this limit. The unit is 10 mV.
A value of 0x0000 disables the limit checking.

Example: To limit the AC voltage amplitude to 200V, a value of 20000 is written to the AC_VOLTAGE_LIMIT register.

Coil Temperature Limit Register (TEMP_COIL_LIMIT_H:TEMP_COIL_LIMIT_L)

Address: 0x18

Reset value: From the configuration data

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEMP_COIL_LIMIT[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 15:0 TEMP_COIL_LIMIT[15:0]: Maximum coil temperature allowed (degrees C)
The transmitter stops the power transfer and reports an error if the coil temperature measured by an optional external thermistor goes above this limit.
A value of 0x0000 disables the limit checking.

Example: To limit the coil temperature to 85 degrees C, a value of 85 is written to the TEMP_ COIL_LIMIT register.

Die Temperature Limit Register (TEMP_DIE_LIMIT_H:TEMP_DIE_LIMIT_L)

Address: 0x1A

Reset value: From the configuration data

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEMP_DIE_LIMIT[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 15:0 TEMP_DIE_LIMIT[15:0]: Maximum die temperature allowed (0.01 degrees C)
The transmitter stops the power transfer and reports an error if the TS80000 die temperature measured internally goes above this limit. The unit is 0.01 deg. C.
A value of 0x0000 disables the limit checking.

Example: To limit the die temperature to 85 degrees C, a value of 8500 is written to the TEMP_DIE_LIMIT register.

Minimum Temperature for Fan Control Register (FAN_TEMP_MIN)

Address: 0x1C

Reset value: From the configuration data

7	6	5	4	3	2	1	0
Res							
rw	rw	rw	rw	rw	rw	rw	rw

Bits 7:0 Reserved

Maximum Temperature for Fan Control Register (FAN_TEMP_MAX)

Address: 0x1D

Reset value: From the configuration data

7	6	5	4	3	2	1	0
Res							
rw	rw	rw	rw	rw	rw	rw	rw

Bits 7:0 Reserved

Minimum Duty Cycle for Fan Control Register (FAN_DTC_MIN)

Address: 0x1E

Reset value: From the configuration data

7	6	5	4	3	2	1	0
Res							
rw	rw	rw	rw	rw	rw	rw	rw

Bits 7:0 Reserved

Maximum Duty Cycle for Fan Control Register (FAN_DTC_MAX)

Address: 0x1F

Reset value: From the configuration data

7	6	5	4	3	2	1	0
Res							
rw	rw	rw	rw	rw	rw	rw	rw

Bits 7:0 Reserved

Supported Standards Register (SUPPORTED_STANDARDS)

Address: 0x20

Reset value: From the configuration data

7	6	5	4	3	2	1	0
Res			A4WP	PMA	WPCRES	WPCMP	WPC
			rw	rw	rw	rw	rw

Bits 7:5 Reserved

Bit 4 A4WP: A4WP Resonant Technology
Read:
0: A4WP not supported by hardware.
1: A4WP supported.
Write:
0: A4WP is not allowed.
1: A4WP is allowed if supported by the hardware.

Bit 3 PMA: Power Matters Alliance Inductive Technology
Read:
0: PMA not supported by hardware.
1: PMA supported.
Write:
0: PMA is not allowed.
1: PMA is allowed if supported by the hardware.

Bit 2 WPCRES: WPC 1.2 Resonant Technology
Read:
0: WPC 1.2 not supported by hardware.
1: WPC 1.2 supported.
Write:
0: WPC 1.2 is not allowed.
1: WPC 1.2 is allowed if supported by the hardware.

Bit 1 WPCMP: WPC Medium Power Inductive Technology
Read:
0: WPC Medium Power not supported by hardware.
1: WPC Medium Power supported.
Write:
0: WPC Medium Power is not allowed.
1: WPC Medium Power is allowed if supported by the hardware.

Bit 0 WPC: WPC Inductive Technology
Read:
0: WPC not supported by hardware.
1: WPC supported.
Write:
0: WPC is not allowed.
1: WPC is allowed if supported by the hardware.

Maximum Power in WPC Mode Register (MAX_POWER_WPC)

Address: 0x21

Reset value: From the configuration data

7	6	5	4	3	2	1	0
MAX_POWER[7:0]							
rw	rw	rw	rw	rw	rw	rw	rw

Bits 7:0 MAX_POWER[7:0]: Maximum power in WPC mode (W)
Read:
Maximum power in WPC mode supported by the hardware.
Write:
Maximum power in WPC mode that is to be allowed.

Maximum Power in PMA Mode Register (MAX_POWER_PMA)

Address: 0x22

Reset value: From the configuration data

7	6	5	4	3	2	1	0
MAX_POWER[7:0]							
rw	rw	rw	rw	rw	rw	rw	rw

Bits 7:0 MAX_POWER[7:0]: Maximum power in PMA mode (W)

Read:

Maximum power in PMA mode supported by the hardware.

Write:

Maximum power in PMA mode that is to be allowed.

Maximum Power in A4WP Mode Register (MAX_POWER_A4WP)

Address: 0x23

Reset value: From the configuration data

7	6	5	4	3	2	1	0
MAX_POWER[7:0]							
rw	rw	rw	rw	rw	rw	rw	rw

Bits 7:0 MAX_POWER[7:0]: Maximum power in A4WP mode (W)

Read:

Maximum power in A4WP mode supported by the hardware.

Write:

Maximum power in A4WP mode that is to be allowed.

Active Coil Register (ACTIVE_COIL)

Address: 0x40

Reset value: 0x00

7	6	5	4	3	2	1	0
ACTIVE_COIL[7:0]							
r	r	r	r	r	r	r	r

Bits 7:0 ACTIVE_COIL[7:0]: Active coil during power transfer

0x00: Coil 0 is active

0x01: Coil 1 is active

.....

0x06: Coil 6 is active

Transmitter Power State Register (POWER_STATE_TX)

Address: 0x41

Reset value: 0x00

7	6	5	4	3	2	1	0
ACTIVE_COIL[7:0]							
r	r	r	r	r	r	r	r

Bits 7:0 POWER_STATE_TX[7:0]: Transmitter state

0x00: Standby (low-power mode, no pinging)

0x01: Test mode

0x02: Hardware Error (voltage, current, temperature, self-test errors)

0x03: Selection (pinging, searching for a receiver)

0x04: Identification (receiver found, negotiating power transfer)

0x05: Power Transfer

0x06: End of Charge (power stopped, waiting for the RX to be removed)

Wireless Power Standard Register (STANDARD)

Address: 0x42

Reset value: 0x00

7	6	5	4	3	2	1	0
STANDARD[7:0]							
r	r	r	r	r	r	r	r

Bits 7:0 STANDARD[7:0]: Wireless power standard used for power transfer

0x00: Not determined

0x01: WPC 1.0.3 or WPC 1.1.2

0x02: WPC Medium Power

0x03: WPC 1.2

0x04: PMA

0x05: A4WP

Power Level Register (POWER_LEVEL)

Address: 0x43

Reset value: 0x00

7	6	5	4	3	2	1	0
POWER_LEVEL[7:0]							
r	r	r	r	r	r	r	r

Bits 7:0 POWER_LEVEL[7:0]: Maximum power for the current operating mode (W)

These bits contain the maximum power level that was negotiated with the receiver when the power transfer was initiated.

Foreign Object Detection Type Register (FOD_TYPE)

Address: 0x44

Reset value: 0x00

7	6	5	4	3	2	1	0
Res				ANALOG	TEMP	FOD_RX	PMOD_RX
				r	r	r	r

Bits 7:4 Reserved

Bit 3 ANALOG: Analog methods

0: No analog methods are used for FOD.

1: Foreign objects are detected using analog methods based on voltages and currents.

Bit 2 TEMP: Surface temperature

0: The surface temperature is not used for FOD.

1: The surface temperature is used for FOD.

Bit 1 FOD_RX: Received Power packets from the RX

0: Received Power packets from the RX are not used for FOD.

1: Received Power packets from the RX are used for FOD (WPC 1.1.2, WPC Medium Power, WPC 1.2, PMA).

Bit 0 PMOD_RX: Parasitic Metal Object Detection

0: Rectified Power Packets from the RX are not used for FOD.

1: Rectified Power Packets from the RX are used for FOD (WPC 1.0.3).

Receiver Power State Register (POWER_STATE_RX)

AAddress: 0x45

Reset value: 0x00

7	6	5	4	3	2	1	0
Res							
r	r	r	r	r	r	r	r

Bits 7:0 Reserved

PWM Frequency Register (PWM_FREQUENCY_H:PWM_FREQUENCY_L)

Address: 0x46

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWM_FREQUENCY[15:0]															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bits 15:0 PWM_FREQUENCY[15:0]: Operating frequency (100 Hz)
Transmitter operating frequency. The unit is 100 Hz.

Example: If the transmitter is operating at 145640 kHz, a value of 1456 is read from the PWM_FREQUENCY register.

PWM Duty Cycle Register(PWM_DTC_H:PWM_DTC_L)

Address: 0x48

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWM_DTC[15:0]															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bits 15:0 PWM_DTC[15:0]: Operating duty cycle (0.01%)
Transmitter operating duty cycle. The unit is 0.01%. In half-bridge mode the duty cycle is between 0 and 5000. In full-bridge mode the duty cycle is between 0 and 10000.

Example: If the transmitter is operating at 50% duty cycle, a value of 5000 is read from the PWM_DTC register.

Bridge DC Voltage Register (DC_VOLTAGE_H:DC_VOLTAGE_L)

Address: 0x4A

Reset value: 0x0000

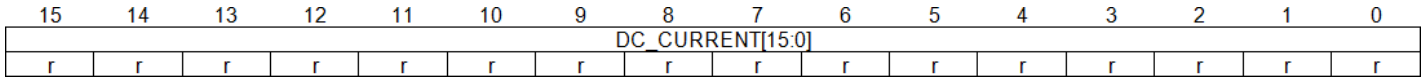
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DC_VOLTAGE[15:0]															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

BBits 15:0 DC_VOLTAGE[15:0]: Bridge voltage measurement (mV)
DC voltage measurement across the bridge.

Bridge DC Current Register (DC_CURRENT_H:DC_CURRENT_L)

Address: 0x4C

Reset value: 0x0000

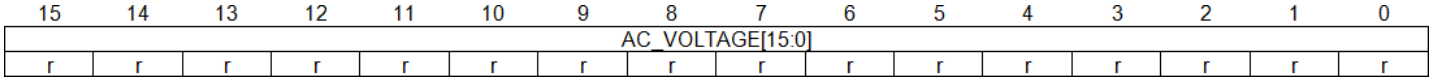


Bits 15:0 DC_CURRENT[15:0]: Bridge current measurement (mA)
DC current flowing into the bridge.

Coil AC Voltage Register (AC_VOLTAGE_H:AC_VOLTAGE_L)

Address: 0x4E

Reset value: 0x0000



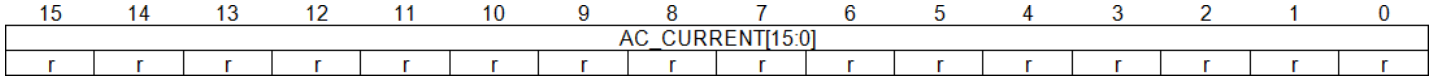
Bits 15:0 AC_VOLTAGE[15:0]: AC voltage amplitude measurement (10 mV)
Amplitude of the AC voltage across the coil. The unit is 10 mV.

Example: If the coil peak voltage is 80V, a value of 8000 is read from the AC_VOLTAGE register.

Coil AC Current Register (AC_CURRENT_H:AC_CURRENT_L)

Address: 0x50

Reset value: 0x0000



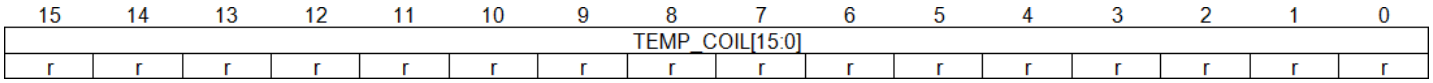
Bits 15:0 AC_CURRENT[15:0]: AC current measurement (mA RMS)
RMS value of the AC current through the coil.

Example: If the coil current is 2A RMS, a value of 2000 is read from the AC_CURRENT register.

Temperature at the Coil Thermistor Register (TEMP_COIL_H:TEMP_COIL_L)

Address: 0x52

Reset value: 0x0000



Bits 15:0 TEMP_COIL[15:0]: Coil temperature measurement (0.01 degrees C)
Coil temperature measurement using an external thermistor. The unit is 0.01 deg. C.

Example: If the coil temperature to 85 degrees C, a value of 8500 is read from the TEMP_COIL register.

Die Temperature Register (TEMP_DIE_H:TEMP_DIE_L)

Address: 0x54

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEMP_DIE[15:0]															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bits 15:0 TEMP_DIE[15:0]: Die temperature measurement (0.01 degrees C)
Die temperature measurement using an internal sensing element. The unit is 0.01 deg. C.

Example: If the die temperature to 85 degrees C, a value of 8500 is read from the TEMP_DIE register.

DC Power at the Bridge Input Register (POWER_DC_IN_H:POWER_DC_IN_L)

Address: 0x56

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POWER_DC_IN[15:0]															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bits 15:0 POWER_DC_IN[15:0]: DC power supplied at the bridge input (10 mW)
DC power measurement at the input of the bridge. The unit is 10 mW.

Example: If the input power into the bridge is 6W, a value of 600 is read from the POWER_DC_IN register.

TX Power into the Magnetic Field Register (POWER_TX_H:POWER_TX_L)

Address: 0x58

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POWER_TX[15:0]															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bits 15:0 POWER_TX[15:0]: Power supplied into the magnetic field (10 mW)
Estimate of the amount of power transferred into the magnetic field. The unit is 10 mW.

Received Power Reported by the RX Register (POWER_RX_H:POWER_RX_L)

Address: 0x5A

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POWER_RX[15:0]															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bits 15:0 POWER_RX[15:0]: RX reported received power (10 mW)
Value of the power received from the magnetic field as reported by the RX using Received Power or Rectified Power packets. The unit is 10 mW.

Receiver Battery Charge Level Register (BATT_CHARGE_LEVEL_RX)

Address: 0x5C

Reset value: 0x00

7	6	5	4	3	2	1	0
CHARGE_LEVEL[7:0]							
r	r	r	r	r	r	r	r

Bits 7:0 CHARGE_LEVEL[7:0]: Battery charge level (%)

These bits contain the battery charge level as reported by the RX using the Charge Status packet.

LED State Register (LED_STATE)

Address: 0x5D

Reset value: 0x00

7	6	5	4	3	2	1	0
Res				LED_STATE[3:0]			
r	r	r	r	r	r	r	r

Bits 7:4 Reserved

Bits 3:0 LED_STATE[3:0]: LED state

These bits contain the state of the LEDs to facilitate an easy implementation of a user interface without having to interpret the contents of other registers.

0x00: Standby, waiting for RX to be placed
0x01: Power Transfer
0x02: Power Transfer, Battery Status 100%
0x03: End of Charge without Error, RX still present
0x04: RX reported error, RX still present
0x05: TX error, RX still present
0x06: FOD error, RX still present
0x07-0xFF: Reserved

Error Code and Parameter Register (ERROR_H:ERROR_L)

Address: 0x5E

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERROR_PARAM[7:0]								ERROR_CODE[7:0]							
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

7	6	5	4	3	2	1	0
ERROR_CODE[7:0]							
r	r	r	r	r	r	r	r

Bits 15:8 **ERROR_PARAM[7:0]**: Error parameter

These bits contain an optional error parameter associated to the error reported in the ERROR_CODE field.

ERROR_CODE = 0x00

0x00-0xFF: Reserved

ERROR_CODE = 0x01

0x00-0xFF: Reserved

ERROR_CODE = 0x02

0x00-0xFF: Reserved

ERROR_CODE = 0x03

0x00-0xFF: Reserved

ERROR_CODE = 0x04

0x00-0xFF: Reserved

ERROR_CODE = 0x05

0x00-0xFF: Reserved

ERROR_CODE = 0x06

0x00-0xFF: Reserved

ERROR_CODE = 0x07

0x00: Generic error
0x01: Supply voltage too low
0x02: Supply voltage too high
0x03: DC bridge current limit reached
0x04: AC voltage limit reached
0x05: Coil temperature limit reached
0x06: Die temperature limit reached
0x07-0xFF: Reserved

ERROR_CODE = 0x08

0x00: Unknown reason
0x01: Charge complete (not an error)
0x02: Internal fault
0x03: Over temperature
0x04: Over Voltage
0x05: Over Current
0x06: Battery failure
0x07: Reserved
0x08: No response
0x09-0x0F: Reserved
0x10: Battery fully charged (not an error)
0x11: No load (not an error)
0x12: Host EOP request (not an error)
0x13: Incompatible power class
0x14-0x16: Reserved
0x17: Over Dec
0x18: Alternate supply connected
0x19-0x1A: Reserved
0x1B: Communication error
0x1C-0xFF: Reserved

Bits 7:0 **ERROR_CODE[7:0]:** Error code

These bits contain the last error code that was generated by the transmitter during power transfer.

0x00: No error has occurred
0x01: Insufficient software resources
0x02: Incorrect RX packet timing
0x03: Incorrect RX packet sequence
0x04: Incorrect RX packet data
0x05: RX packet timeout during power transfer
0x06: FOD error
0x07: Limit exceeded (temperature, voltage, current)
0x08: End Power Transfer packet received
0x09-0xFF: Reserved

Interrupt Mask 0 Register (INTERRUPT_MASK0)

Address: 0x78

Reset value: 0x00

7	6	5	4	3	2	1	0
Res		CTS_IF	CTS_API_IF	STATUS3	STATUS2	STATUS1	Res
		r	r	r	r	r	

Bits 7:6 Reserved

Bit 5 CTS_IF: Clear To Send

0: A transition from 0 to 1 of the CTS bit in the STATUS0 register doesn't cause an interrupt.

1: A transition from 0 to 1 of the CTS bit in the STATUS0 register causes an interrupt.

Bit 4 CTS_API_IF: Clear to Send for API

0: A transition from 0 to 1 of the CTS_API bit in the STATUS0 register doesn't cause an interrupt.

1: A transition from 0 to 1 of the CTS_API bit in the STATUS0 register causes an interrupt.

Bit 3 STATUS3_IF: STATUS1 Event

0: A transition from 0 to 1 of the STATUS3_IF bit in the STATUS0 register doesn't cause an interrupt.

1: A transition from 0 to 1 of the STATUS3_IF bit in the STATUS0 register causes an interrupt.

Bit 2 STATUS2_IF: STATUS2 Event

0: A transition from 0 to 1 of the STATUS2_IF bit in the STATUS0 register doesn't cause an interrupt.

1: A transition from 0 to 1 of the STATUS2_IF bit in the STATUS0 register causes an interrupt.

Bit 1 STATUS1_IF: STATUS1 Event

0: A transition from 0 to 1 of the STATUS1_IF bit in the STATUS0 register doesn't cause an interrupt.

1: A transition from 0 to 1 of the STATUS1_IF bit in the STATUS0 register causes an interrupt.

Bit 0 Reserved

Interrupt Mask 1 Register (INTERRUPT_MASK1)

Address: 0x79

Reset value: 0x00

7	6	5	4	3	2	1	0
Res		RX_EOC	RX_CHG	RX_CONFIG	RX_ID	RX_RMV	RX_DET

Bits 7:6 Reserved

Bit 5 RX_EOC: RX End of Charge Received

0: A value of 1 of this bit in the STATUS1 register doesn't cause the STATUS1 event flag to be set in the STATUS0 register.

1: A value of 1 of this bit in the STATUS1 register causes the STATUS1 event flag to be set in the STATUS0 register.

Bit 4 RX_CHG: RX Charge Level Received

0: A value of 1 of this bit in the STATUS1 register doesn't cause the STATUS1 event flag to be set in the STATUS0 register.

1: A value of 1 of this bit in the STATUS1 register causes the STATUS1 event flag to be set in the STATUS0 register.

Bit 3 RX_CONFIG: RX Configuration Received

0: A value of 1 of this bit in the STATUS1 register doesn't cause the STATUS1 event flag to be set in the STATUS0 register.

1: A value of 1 of this bit in the STATUS1 register causes the STATUS1 event flag to be set in the STATUS0 register.

Bit 2 RX_ID: RX Identification Received

0: A value of 1 of this bit in the STATUS1 register doesn't cause the STATUS1 event flag to be set in the STATUS0 register.

1: A value of 1 of this bit in the STATUS1 register causes the STATUS1 event flag to be set in the STATUS0 register.

Bit 1 RX_RMV: RX Removed

0: A value of 1 of this bit in the STATUS1 register doesn't cause the STATUS1 event flag to be set in the STATUS0 register.

1: A value of 1 of this bit in the STATUS1 register causes the STATUS1 event flag to be set in the STATUS0 register.

Bit 0 RX_DET: RX Detected

0: A value of 1 of this bit in the STATUS1 register doesn't cause the STATUS1 event flag to be set in the STATUS0 register.

1: A value of 1 of this bit in the STATUS1 register causes the STATUS1 event flag to be set in the STATUS0 register.

Interrupt Mask 2 Register (INTERRUPT_MASK2)

Address: 0x7A

Reset value: 0x00

7	6	5	4	3	2	1	0
Res						LED	ERROR
						rw	rw

Bits 7:2 Reserved

Bit 1 LED: LED Status Changed

0: A value of 1 of this bit in the STATUS2 register doesn't cause the STATUS2 event flag to be set in the STATUS0 register.

1: A value of 1 of this bit in the STATUS2 register causes the STATUS2 event flag to be set in the STATUS0 register.

Bit 0 ERROR: Error Condition Detected

0: A value of 1 of this bit in the STATUS2 register doesn't cause the STATUS2 event flag to be set in the STATUS0 register.

1: A value of 1 of this bit in the STATUS2 register causes the STATUS2 event flag to be set in the STATUS0 register.

Interrupt Mask 3 Register (INTERRUPT_MASK3)

Address: 0x7B

Reset value: 0x00

7	6	5	4	3	2	1	0
Res						TEST	DEBUG
						rw	rw

Bits 7:2 Reserved

Bit 1 TEST: Test Event

0: A value of 1 of this bit in the STATUS3 register doesn't cause the STATUS3 event flag to be set in the STATUS0 register.

1: A value of 1 of this bit in the STATUS3 register causes the STATUS3 event flag to be set in the STATUS0 register.

Bit 0 DEBUG: Debug Event

0: A value of 1 of this bit in the STATUS3 register doesn't cause the STATUS3 event flag to be set in the STATUS0 register.

1: A value of 1 of this bit in the STATUS3 register causes the STATUS3 event flag to be set in the STATUS0 register.

API Functions

API Number	API Name	Description
0x80	BOOTLOADER_UNLOCK_FLASH	Allow changes to the FLASH memory
0x81	BOOTLOADER_WRITE_BLOCK	Write a page of the firmware into the FLASH memory
0x82	BOOTLOADER_CRC_CHECK	Check the CRC of the transmitter firmware
0x83	RESERVED	R
0x84	BOOTLOADER_WRITE_CONFIGURATION	Write a page of the configuration block into the FLASH memory
0x85	BOOTLOADER_READ_CONFIGURATION	Read a page of the configuration block from the FLASH memory
0x86	BOOTLOADER_WRITE_CALIBRATION	Write a page of the calibration block into the FLASH memory
0x87	BOOTLOADER_READ_CALIBRATION	Read a page of the calibration block from the FLASH memory
0x88	BOOTLOADER_TRIM	Execute the trim procedure and store the result in FLASH memory
0x89	BOOTLOADER_READ_TRIM	Read the trim block from the FLASH memory
0x8A-0x8F	RESERVED	
0x90	WRITE_CONFIGURATION	Write to the TX channel configuration
0x91	READ_CONFIGURATION	Read from the TX channel configuration
0x92	READ_RX_CONFIG	Read the RX power contract parameters
0x93	READ_RX_ID	Read the RX ID
0x94	WRITE_TX_ID	Write the TX ID
0x95	READ_TX_ID	Read the TX ID
0x96	READ_DEBUG	Read the next oldest debug block from the debug queue
0x97-0xFE	RESERVED	
0xFF	API_ERROR	Value returned in the API field when a Read API Function Return Buffer command is issued and the API function called previously has generated an error.

Bootloader Unlock Flash (BOOTLOADER_UNLOCK_FLASH)

API number: 0x80
Input buffer size: 16
Output buffer size: 1

Buffer	Parameter	Length (bytes)	Description
Input buffer	Nonce	16	Firmware authentication string.
Return data buffer	ERROR_CODE	1	
Note: The firmware authentication string is obtained from the header of the Triune Systems firmware image file.			

Bootloader Write Block (BOOTLOADER_WRITE_BLOCK)

API number: 0x81
Input buffer size: 66
Output buffer size: 1

Buffer	Parameter	Length (bytes)	Description
Input buffer	Block Number	2	Block index. The first block has an index of 0.
	Block Data	64	
Return data buffer	ERROR_CODE	1	

Bootloader CRC Check (BOOTLOADER_CRC_CHECK)

API number: 0x82
Input buffer size: 0
Output buffer size: 3

Buffer	Parameter	Length (bytes)	Description
Return data buffer	ERROR_CODE	1	CRC check error code for the firmware block.
	ERROR_CODE	1	CRC check error code for the configuration block.
	ERROR_CODE	1	CRC check error code for the calibration block.

Read RX ID (READ_RX_ID)

API number: 0x93
Input buffer size: 0
Output buffer size: 6

Buffer	Parameter	Length (bytes)	Description
	Block Data	64	
Return data buffer	RXID	6	RXID data.

Write TX ID (WRITE_TX_ID)

API number: 0x94
Input buffer size: 6
Output buffer size: 1

Buffer	Parameter	Length (bytes)	Description
	Block Data	64	
Input buffer	TXID	6	TXID data.
Return data buffer	ERROR_CODE	1	

Read TX ID (READ_TX_ID)

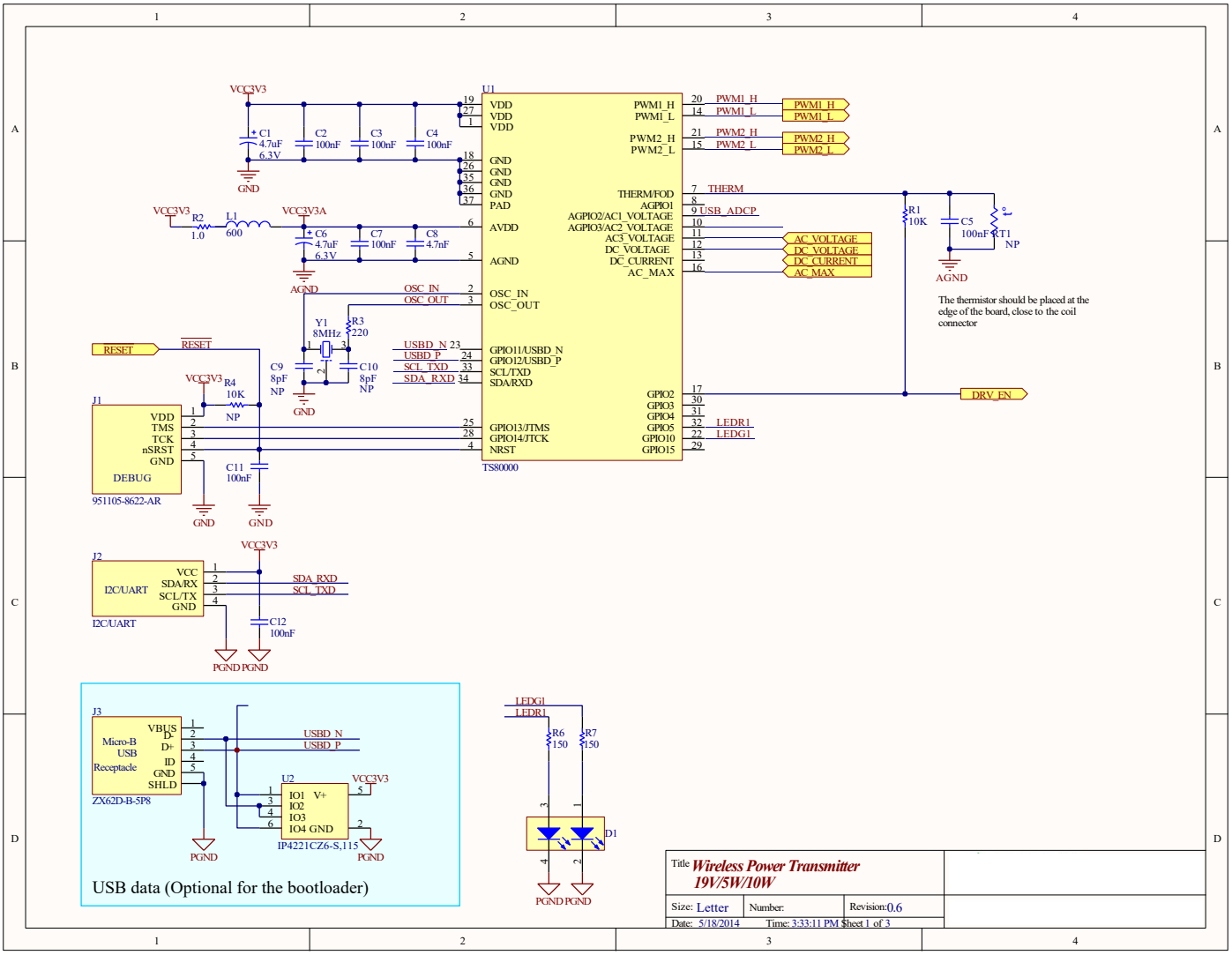
API number: 0x95
Input buffer size: 0
Output buffer size: 6

Buffer	Parameter	Length (bytes)	Description
	Block Data	64	
Return data buffer	TXID	6	TXID data.

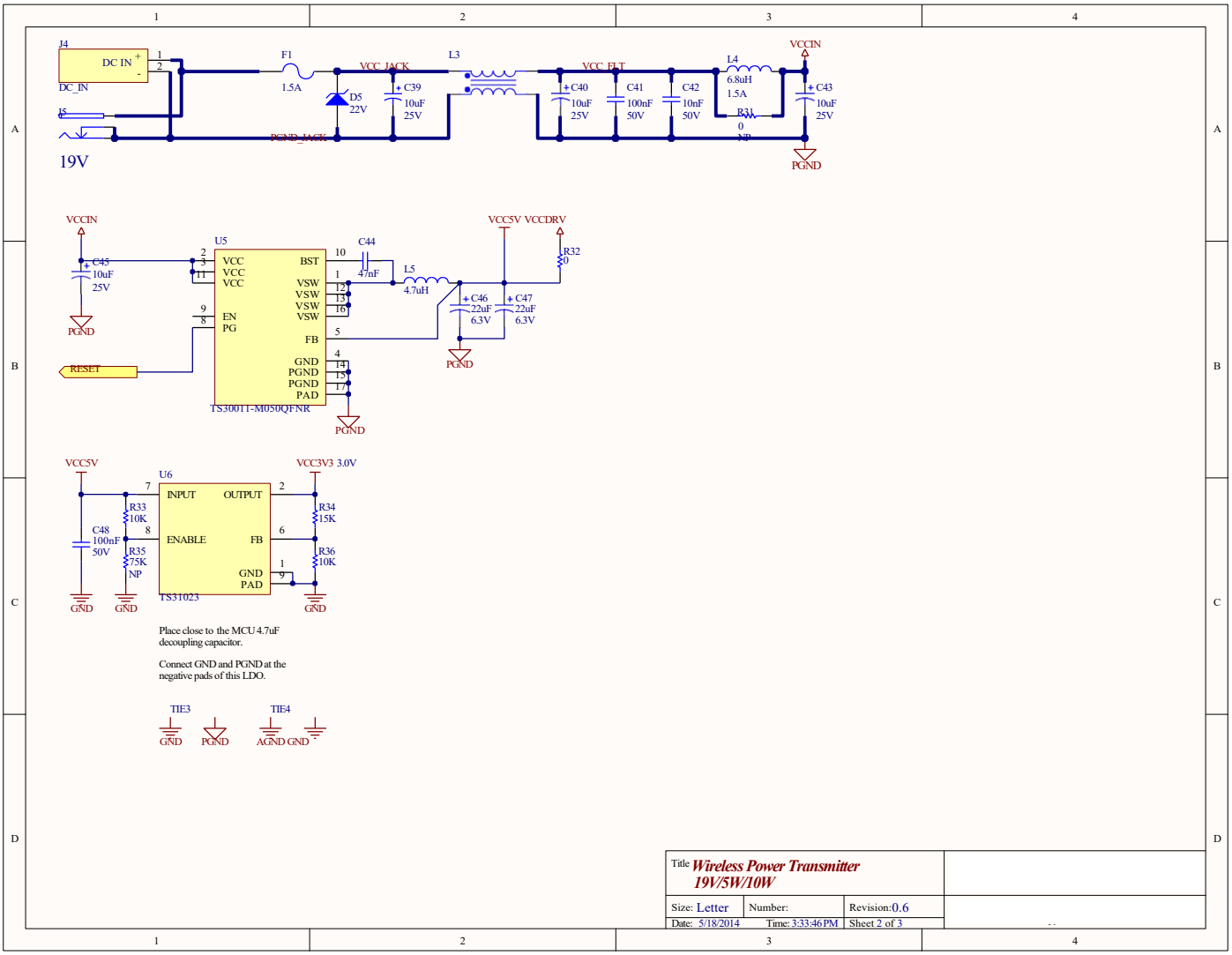
API Error Codes

Error Code	Error Code Name	Description
0x00	ERROR_GENERIC	Generic error.
0x01	ERROR_OK	Operation succeeded. This is not indicating an error.
0x02	ERROR_INVALID_CRC	CRC error.
0x03	ERROR_FLASH_UNLOCK_FAILED	FLASH unlocking has failed.
0x04	ERROR_API_NOT_IMPLEMENTED	The API number is not implemented.
0x05	ERROR_API_DATA_OVERFLOW	The API input buffer has been filled with more data than its length.
0x06	ERROR_API_INVALID_PARAMETERS	At least one of the API parameters is invalid.
0x07	ERROR_FLASH_ERASE_FAILED	FLASH erase has failed.
0x08	ERROR_FLASH_PROGRAM_FAILED	FLASH programming has failed.
0x09	ERROR_API_DATA_NOT_READY	The API data is not available yet.
0x0A-0xFF	RESERVED. Will be defined later.	

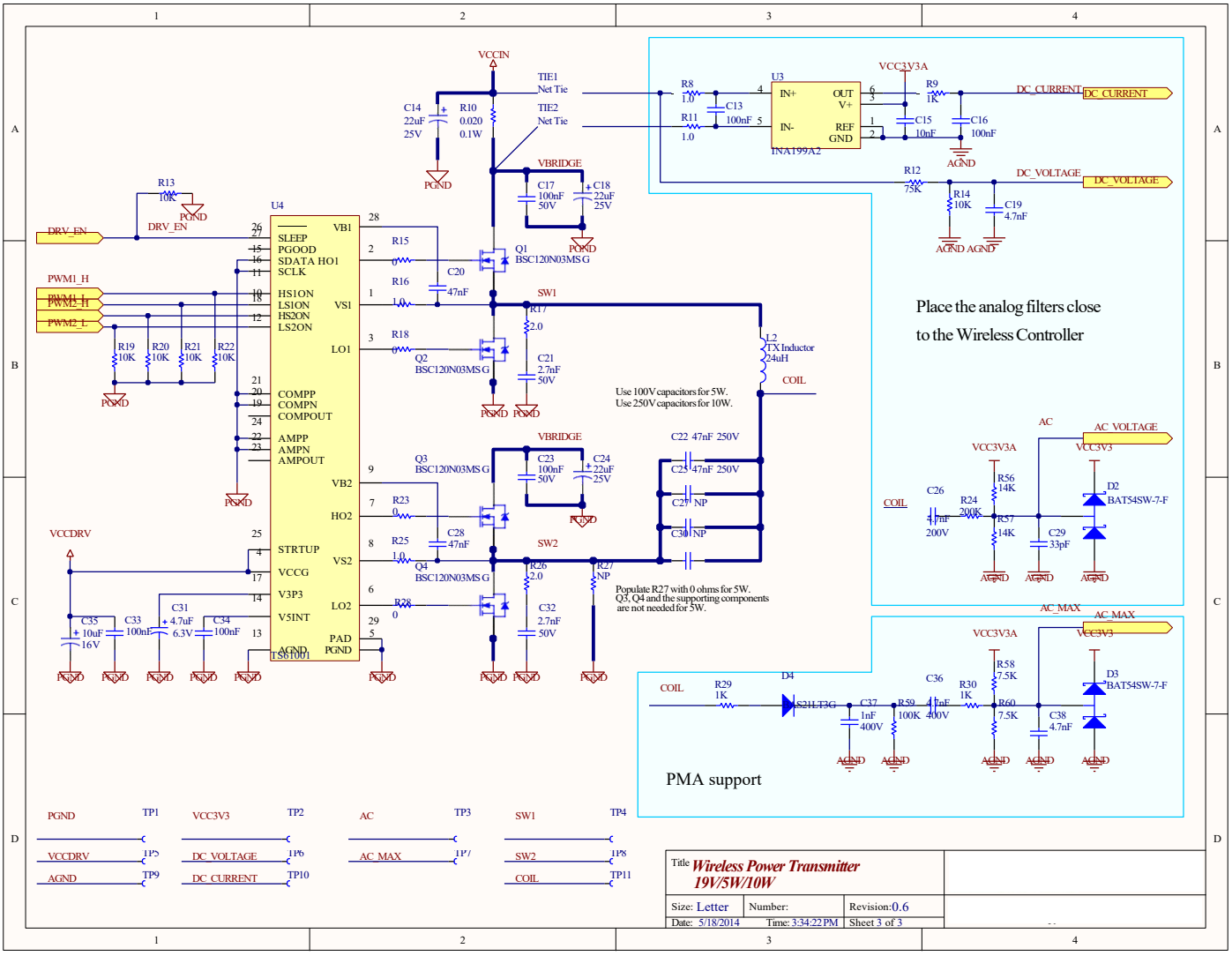
Application Schematics



Application Schematics



Application Schematics



Package Dimensions

Figure 41. VFQFPN36 6 x 6 mm, 0.5 mm pitch, package outline(1)

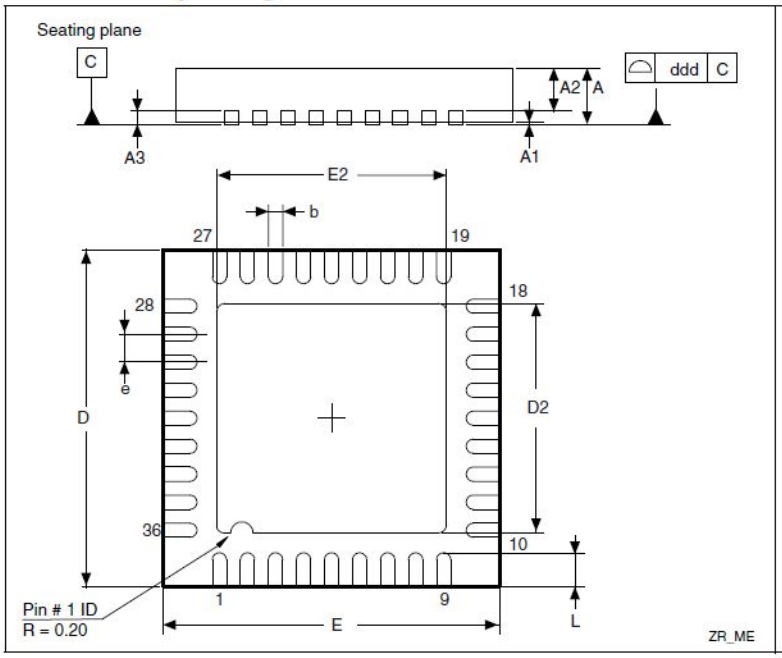
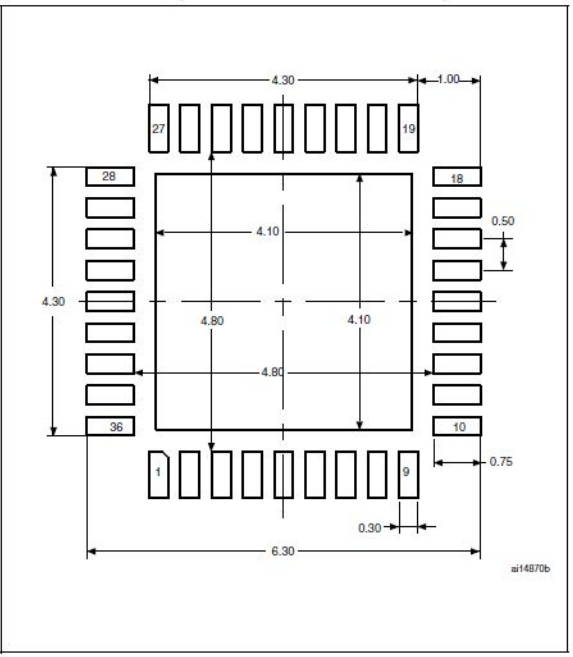


Figure 42. Recommended footprint (dimensions in mm)(1)(2)



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead solder joint life.

Table 51. VFQFPN36 6 x 6 mm, 0.5 mm pitch, package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.800	0.900	1.000	0.0315	0.0354	0.0394
A1		0.020	0.050		0.0008	0.0020
A2		0.650	1.000		0.0256	0.0394
A3		0.250			0.0098	
b	0.180	0.230	0.300	0.0071	0.0091	0.0118
D	5.875	6.000	6.125	0.2313	0.2362	0.2411
D2	1.750	3.700	4.250	0.0689	0.1457	0.1673
E	5.875	6.000	6.125	0.2313	0.2362	0.2411
E2	1.750	3.700	4.250	0.0689	0.1457	0.1673
e	0.450	0.500	0.550	0.0177	0.0197	0.0217
L	0.350	0.550	0.750	0.0138	0.0217	0.0295
ddd		0.080			0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Ordering Information

Part Number	Description	Reel quantity
TS80000-QFNR	Bootloader programmed device. Ready for firmware programming	3,000 pcs
TS80000-916203QFNR	Device programmed with a custom firmware	3,000 pcs

RoHS and Reach Compliance

Triune Systems is fully committed to environmental quality. All Triune Systems materials and suppliers are fully compliant with RoHS (European Union Directive 2011/65/EU), REACH SVHC Chemical Restrictions (EC 1907/2006), IPC-1752 Level 3 materials declarations, and their subsequent amendments. Triune Systems maintains certified laboratory reports for all product materials, from all suppliers, which show full compliance to restrictions on the following:

- Cadmium (Cd)
- Chlorofluorocarbons (CFCs)
- Chlorinate Hydrocarbons (CHCs)
- Halons (Halogen free)
- Hexavalent Chromium (CrVI)
- Hydrobromofluorocarbons (HBFCs)
- Hydrochlorofluorocarbons (HCFCs)
- Lead (Pb)
- Mercury (Hg)
- Perfluorocarbons (PFCs)
- Polybrominated biphenyls (PBB)
- Polybrominated Diphenyl Ethers (PBDEs)

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