

### ADVANCED COMMUNICATIONS & SENSING

### DATASHEET

#### GENERAL DESCRIPTION

The SX8650 is an ultra low power 4-wire resistive touchscreen controller optimized for portable equipment where power and board-space are at a premium.

It incorporates a highly accurate 12-bit ADC for data conversion and operates from a single 1.65 to 3.7V supply voltage.

The SX8650 features a built-in preprocessing algorithm for data measurements, which greatly reduces the host processing overhead and bus activity. This complete touchscreen solution includes four user-selectable operation modes which offer programmability on different configurations such as conversion rate and settling time, thus enable optimization in throughput and power consumption for a wide range of touch sensing applications.

The touch screen inputs have been specially designed to provide robust on-chip ESD protection of up to  $\pm 15\text{kV}$  in both HBM and Contact Discharge, and eliminates the need for external protection devices.

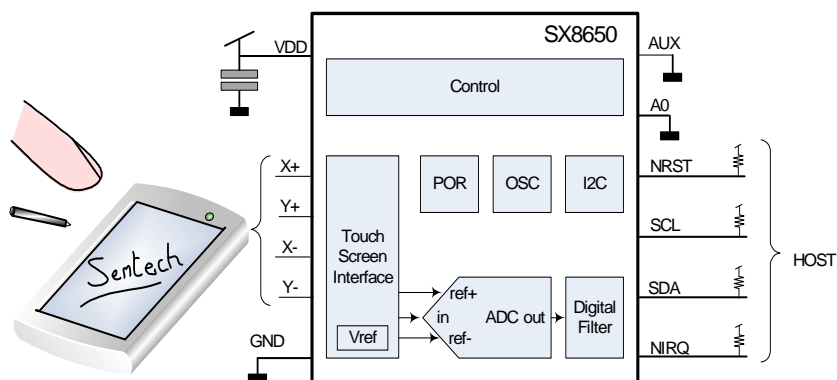
The SX8650 supports the Fast-mode I<sup>2</sup>C (400kbit/s) serial bus data protocol and includes 2 user-selectable slave addresses. A custom I2C address is possible on request.

The SX8650 is offered in two tiny packages: 3.0 mm x 3.0 mm DFN and a 1.5 mm x 2.0 mm wafer-level chip-scale package (WLCSP).

#### APPLICATIONS

- ◆ Portable Equipment
- ◆ Mobile Communication Devices
- ◆ Cell phone, PDA, MP3, GPS, DSC
- ◆ Touch Screen Monitors

#### Block Diagram



#### KEY PRODUCT FEATURES

- ◆ Extremely Low Power Consumption: 23uA@1.8V 8kSPS
- ◆ Superior On-chip ESD Protection
  - ⇒  $\pm 15\text{kV}$  HBM (X+, X-, Y+, Y-)
  - ⇒  $\pm 2\text{kV}$  CDM
  - ⇒  $\pm 25\text{kV}$  Air Gap Discharge
  - ⇒  $\pm 15\text{kV}$  Contact Discharge
  - ⇒  $\pm 300\text{V}$  MM
- ◆ Single 1.65V to 3.7V Supply/Reference
- ◆ Integrated Preprocessing Block to Reduce Host Loading and Bus Activity
- ◆ Four User Programmable Operation Modes provides Flexibility to address Different Application Needs
  - ⇒ Manual, Automatic, Pen Detect, Pen Trigger
- ◆ High Precision 12-bit Resolution
- ◆ Low Noise Ratiometric Conversion
- ◆ Selectable Polling or Interrupt Modes
- ◆ Touch Pressure Measurement
- ◆ 400kHz Fast-Mode I<sup>2</sup>C Interface
- ◆ Hardware Reset & I<sup>2</sup>C Software Reset
- ◆ -40°C to 85°C Operation
- ◆ 12-LD (3.0 mm x 3.0 mm) DFN Package
- ◆ 12-Ball (1.5 mm x 2.0 mm) WLCSP Package
- ◆ Pin-compatible with SX8651
- ◆ Pb-Free, Halogen Free, RoHS/WEEE compliant product
- ◆ Windows CE 6.0, Linux Driver Support Available

#### ORDERING INFORMATION

| Part Number               | Package                           |
|---------------------------|-----------------------------------|
| SX8650ICSTRT <sup>1</sup> | 12 - Ball WLCSP (1.5 mm x 2.0 mm) |
| SX8650IWLTRT <sup>1</sup> | 12 - Lead DFN (3.0 mm x 3.0 mm)   |

1. 3000 Units / reel

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## 1. General Description

### 1.1. DFN Pinout Diagram and Marking Information (Top View)

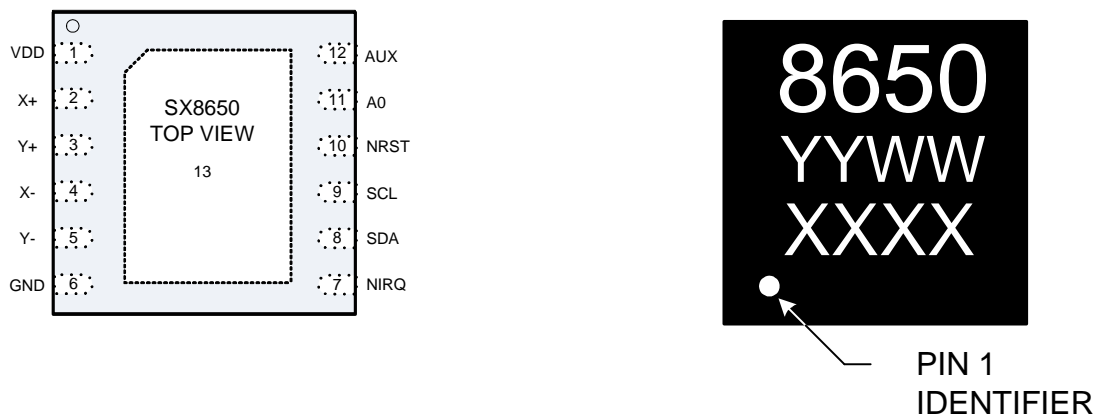


Figure 1. SX8650 DFN Top View, Pad on Bottom Side

YYWW : date code

XXXXX: Lot Number

### 1.2. WLCSP Pinout Diagram and Marking Information (Top View)

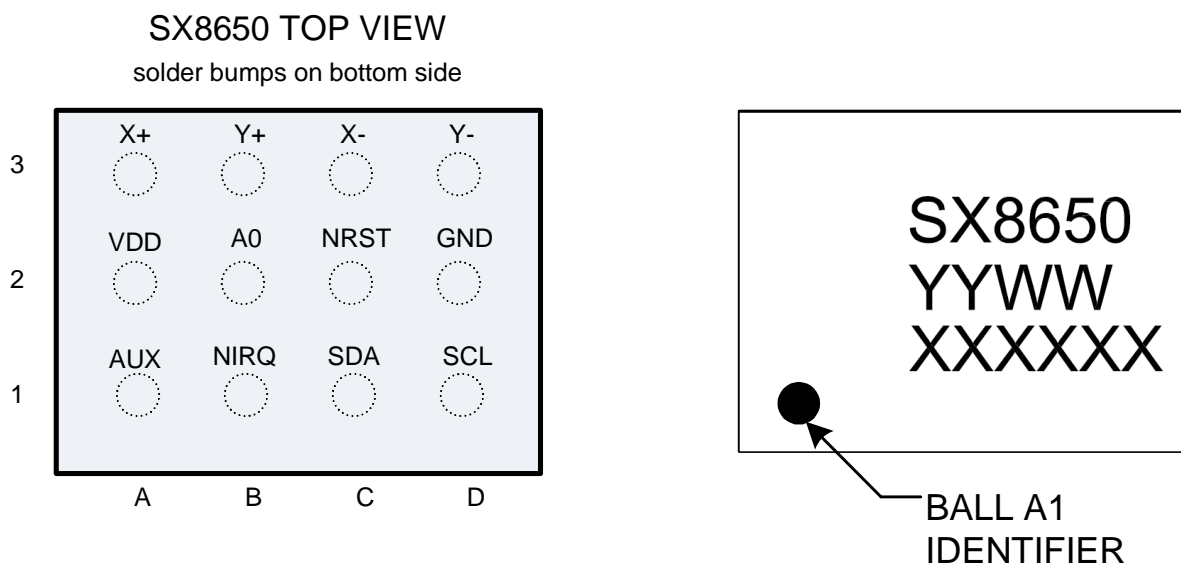


Figure 2. SX8650 WLCSP Top View, Solder Bumps on Bottom Side

YYWW : date code

XXXXX: Lot Number

### 1.3. Pin Description

| Pin Number # |       | Name | Type                               | Description  |
|--------------|-------|------|------------------------------------|--|
| DFN          | WLCSP |      |                                    |  |
| 1            | A2    | VDD  | Power                              | Input power supply connect to a 0.1uF capacitor to GND       |
| 2            | A3    | X+   | Analog                             | X+ channel input   |
| 3            | B3    | Y+   | Analog                             | Y+ channel input   |
| 4            | C3    | X-   | Analog                             | X- channel input   |
| 5            | D3    | Y-   | Analog                             | Y- channel input   |
| 6            | D2    | GND  | Ground                             | Ground   |
| 7            | B1    | NIRQ | Digital Output / Open Drain Output | Interrupt output, active low. Need external pull-up resistor |
| 8            | C1    | SDA  | Digital Input / Open Drain Output  | I2C data input/output  |
| 9            | D1    | SCL  | Digital Input / Open Drain Output  | I2C clock, input/output                                      |
| 10           | C2    | NRST | Digital Input / Output             | Reset Input, active low. Need external 50k pull-up resistor  |
| 11           | B2    | A0   | Digital Input                      | I2C slave address selection input                            |
| 12           | A1    | AUX  | Digital Input/Analog Input         | Analog auxiliary input or conversion synchronization         |
| 13           |       | GND  | Ground                             | Die attach paddle, connect to Ground                         |

Table 1 Pin description

### 1.4. Simplified Block Diagram

The SX8650 simplified block diagram is shown in Figure 3.

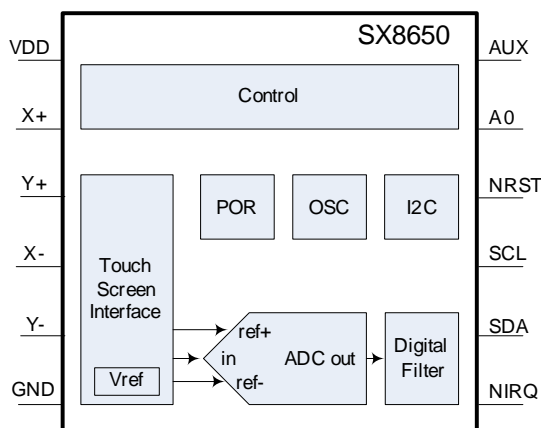


Figure 3. Simplified block diagram of the SX8650

## 2. Electrical Characteristics

Stresses above the values listed in “Absolute Maximum Ratings” may cause permanent damage to the device.

This is a stress rating only and functional operation of the device at these, or any other conditions beyond the “Recommended Operating Conditions”, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Parameter                       | Symbol  | Min.              | Max.           | Unit |
|---------------------------------|---|-------------------|----------------|------|
| Supply Voltage                  | $V_{DDABS}$   | -0.5              | 3.9            | V    |
| Input voltage (non-supply pins) | $V_{IN}$  | -0.5              | 3.9            | V    |
| Input current (non-supply pins) | $I_{IN}$  |                   | 10             | mA   |
| Operating Junction Temperature  | $T_{JCT}$   |                   | 125            | °C   |
| Reflow temperature              | $T_{RE}$  |                   | 260            | °C   |
| Storage temperature             | $T_{STOR}$  | -50               | 150            | °C   |
| ESD HBM<br>(Human Body Model)   | High ESD pins: X+, X-, Y+, Y-                                   | $ESD_{HBM1}$      | $\pm 15^{(i)}$ | kV   |
|                                 |   |                   | $\pm 8^{(ii)}$ | kV   |
|                                 | All pins except high ESD pins:<br>AUX, A0, NRST, NIRQ, SDA, SCL | $ESD_{HBM2}$      | $\pm 2$        | kV   |
| ESD (Contact Discharge)         | High ESD pins: X+, X-, Y+, Y-                                   | $ESD_{CD}$        | $\pm 15$       | kV   |
| Latchup                         | $I_{LU}$  | $\pm 100^{(iii)}$ |                | mA   |

Table 2. Absolute Maximum Ratings

(i) Tested to TLP (10A)

(ii) Tested to JEDEC standard JESD22-A114

(iii) Tested to JEDEC standard JESD78

### 2.1. Recommended Operating Conditions

| Parameter                 | Symbol   | Min.  | Max | Unit |
|---------------------------|----------|-------|-----|------|
| Supply Voltage            | $V_{DD}$ | 1.65V | 3.7 | V    |
| Ambient Temperature Range | $T_A$    | -40   | 85  | °C   |

### 2.2. Thermal Characteristics

| Parameter  | Symbol        | Min. | Max | Unit |
|--|---------------|------|-----|------|
| Thermal Resistance with DFN package - Junction to Ambient <sup>(i)</sup>   | $\theta_{JA}$ |      | 39  | °C/W |
| Thermal Resistance with WLCSP package - Junction to Ambient <sup>(i)</sup> | $\theta_{JA}$ |      | 65  | °C/W |

(iii)  $\theta_{JA}$  is calculated from a package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under exposed pad (if applicable) per JESD51 standards.

### 2.3. Electrical Specifications

| Parameter  | Symbol                           | Conditions   | Min.                        | Typ | Max                | Unit |
|--|----------------------------------|--|-----------------------------|-----|--------------------|------|
| <b>Current consumption</b>   |                                  |  |                             |     |                    |      |
| Manual   | $I_{pwd}$                        | Manual (converter stopped, pen detection off, I2C listening, OSC stopped)  |                             | 0.4 | 0.75               | uA   |
| Pen Detect   | $I_{pndt}$                       | Pen detect mode (converter stopped, pen detection activated, device will generate interrupt upon detection, I2C listening, OSC stopped).   |                             | 0.4 | 0.75               | uA   |
| Pen Trigger  | $I_{pntr}$                       | Pen trigger mode (converter stopped, pen detection activated, device will start conversion upon pen detection. I2C listening, OSC stopped) |                             | 0.4 | 0.75               | uA   |
| Automatic  | $I_{wt}$                         | Automatic (converter stopped, pen detection off, I2C listening, OSC and timer on, device is waiting for timer expiry)                      |                             | 1.5 |                    | uA   |
| Operation @8kSPS, VDD=1.8V   | $I_{opl}$                        | X,Y Conv. RATE=4kSPS, $N_{filt}=1$<br>PowDly=0.5us, SetDly=0.5us   |                             | 23  | 50                 | uA   |
| Operation @42kSPS, VDD=3.3V  | $I_{oph}$                        | X,Y Conv. RATE=3kSPS, $N_{filt}=7$<br>PowDly=0.5us, SetDly=0.5us   |                             | 105 | 140                | uA   |
| <b>Digital I/O</b>   |                                  |  |                             |     |                    |      |
| High-level input voltage <sup>1</sup>                                    | $V_{IH}$                         |  | $0.7V_{DD}$                 |     | $V_{DD}+0.5$       | V    |
| Low-level input voltage  | $V_{IL}$                         |  | $V_{SS}-0.3$                |     | $0.3V_{DD}$        | V    |
| SDA / SCL Hysteresis of Schmitt trigger inputs<br>VDD > 2 V<br>VDD < 2 V | $V_{hys}$                        |  | $0.05V_{DD}$<br>$0.1V_{DD}$ |     |                    | V    |
| Low-level output voltage   | $V_{OL}$                         | $I_{OL}=3mA, V_{DD}>2V$<br>$I_{OL}=3mA, V_{DD}<2V$   | 0<br>0                      |     | 0.4<br>$0.2V_{DD}$ | V    |
| Input leakage current  | $I_I$                            | CMOS input   |                             |     | ±1                 | uA   |
| <b>AUX</b>   |                                  |  |                             |     |                    |      |
| Input voltage range  | $V_{IAUX}$                       |  | 0                           |     | $V_{DD}$           | V    |
| Input capacitance  | $C_{X+}, C_{X-}, C_{Y+}, C_{Y-}$ |  |                             | 50  |                    | pF   |
|  | $C_{AUX}$                        |  |                             | 5   |                    | pF   |

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| Parameter                  | Symbol         | Conditions                                   | Min. | Typ       | Max | Unit |
|----------------------------|----------------|--|------|-----------|-----|------|
| Input leakage current      | $I_{IAUX}$     |  | -1   |           | 1   | uA   |
|                            |                |  |      |           |     |      |
| <b>Startup</b>             |                |  |      |           |     |      |
| Power-up time<br>(Delay)   | $t_{POR}$      | Time between rising edge VDD and rising NIRQ |      |           | 1   | ms   |
|                            |                |  |      |           |     |      |
| <b>Reset</b>               |                |  |      |           |     |      |
| Reset low time             | $t_{NRST}$     |  | 50   |           |     | ns   |
|                            |                |  |      |           |     |      |
| <b>ADC</b>                 |                |  |      |           |     |      |
| Resolution                 | $A_{res}$      |  | 12   |           |     | bits |
| Offset                     | $A_{off}$      |  |      | $\pm 1$   |     | LSB  |
| Gain error                 | $A_{ge}$       | At full scale                                |      | 0.5       |     | LSB  |
| Differential nonlinearity  | $A_{dnl}$      |  |      | $\pm 1$   |     | LSB  |
| Integral nonlinearity      | $A_{inl}$      |  |      | $\pm 1.5$ |     | LSB  |
|                            |                |  |      |           |     |      |
| <b>Resistors</b>           |                |  |      |           |     |      |
| X+, X-, Y+, Y- resistance  | $R_{chn}$      | Touch Pad Biasing Resistance                 |      | 5         |     | Ohm  |
| Pen detect resistance      | $R_{PNDT\_00}$ | $R_{PNDT} = 0$                               |      | 100       |     | kOhm |
|                            | $R_{PNDT\_01}$ | $R_{PNDT} = 1$                               |      | 200       |     | kOhm |
|                            | $R_{PNDT\_10}$ | $R_{PNDT} = 2$                               |      | 50        |     | kOhm |
|                            | $R_{PNDT\_11}$ | $R_{PNDT} = 3$                               |      | 25        |     | kOhm |
|                            |                |  |      |           |     |      |
| <b>External components</b> |                | <b>recommendations</b>                       |      |           |     |      |
| Capacitor between VDD, GND | $C_{vdd}$      | Type 0402, tolerance +/-50%                  |      | 0.1       |     | uF   |

1. SCL, SDA, NRST and NIRQ can be pulled up to a potential higher than the chip VDD but must not exceed the maximum voltage of 3.7V.

All values are valid within the recommended operating conditions unless otherwise specified.



## 2.4. Host Interface Specifications

| Parameter   | Symbol       | Condition | Min | Typ | Max | Unit |
|---|--------------|-----------|-----|-----|-----|------|
| <b>I2C TIMING SPECIFICATIONS <sup>(i)</sup></b>                   |              |           |     |     |     |      |
| SCL clock frequency   | $f_{SCL}$    |           | 0   |     | 400 | kHz  |
| SCL low period  | $t_{LOW}$    |           | 1.3 |     |     | us   |
| SCL high period   | $t_{HIGH}$   |           | 0.6 |     |     | us   |
| Data setup time   | $t_{SU;DAT}$ |           | 100 |     |     | ns   |
| Data hold time  | $t_{HD;DAT}$ |           | 0   |     |     | ns   |
| Repeated start setup time   | $t_{SU;STA}$ |           | 0.6 |     |     | us   |
| Start condition hold time   | $t_{HD;STA}$ |           | 0.6 |     |     | us   |
| Stop condition setup time   | $t_{SU;STO}$ |           | 0.6 |     |     | us   |
| Bus free time between stop and start                              | $t_{BUF}$    |           | 1.3 |     |     | us   |
| Data valid time   | $t_{VD;DAT}$ |           |     |     | 0.9 | us   |
| Data valid ack time   | $t_{VD;ACK}$ |           |     |     | 0.9 | us   |
| Pulse width of spikes that must be suppressed by the input filter | $t_{SP}$     |           |     |     | 50  | ns   |
| <b>I2C BUS SPECIFICATIONS</b>                                     |              |           |     |     |     |      |
| Capacitive Load on each bus line SCL, SDA                         | $C_b$        |           |     |     | 400 | pF   |

**Table 3** Host Interface Specifications

**Notes:**

- (i) All timing specifications refer to voltage levels ( $V_{IL}$ ,  $V_{IH}$ ,  $V_{OL}$ ) defined in Table 3 unless otherwise mentioned.

## 2.5. Host Interface Timing Waveforms

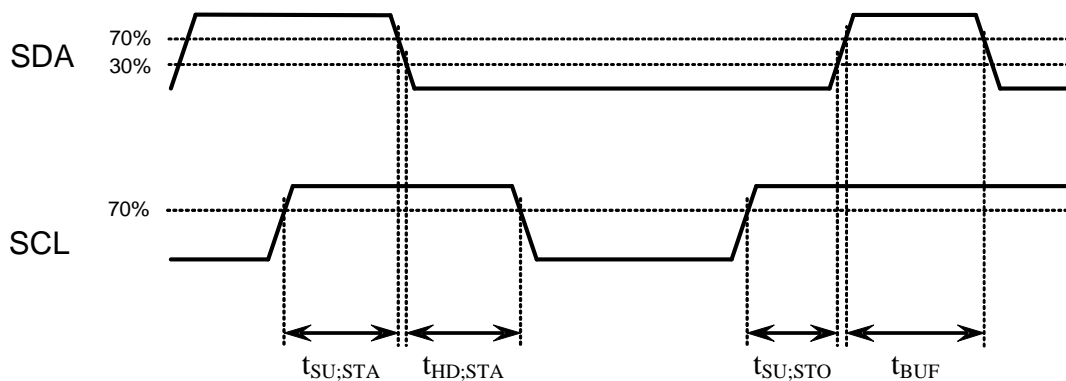


Figure 4. I2C Start and Stop timing

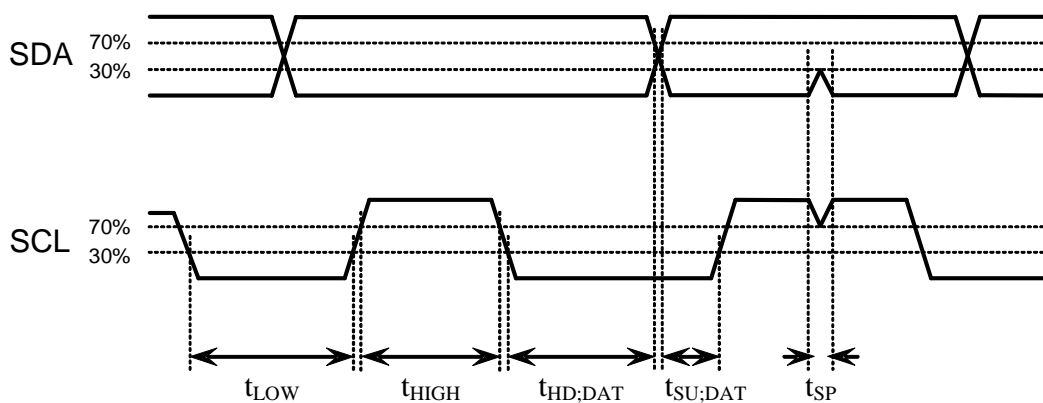
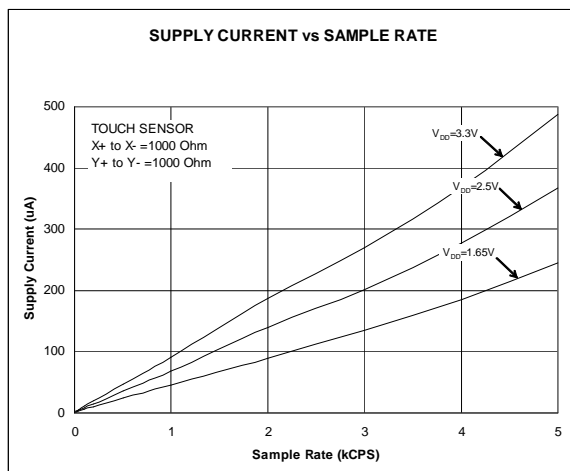
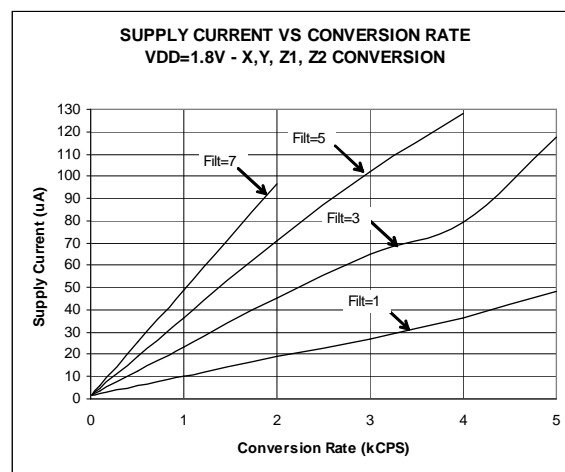
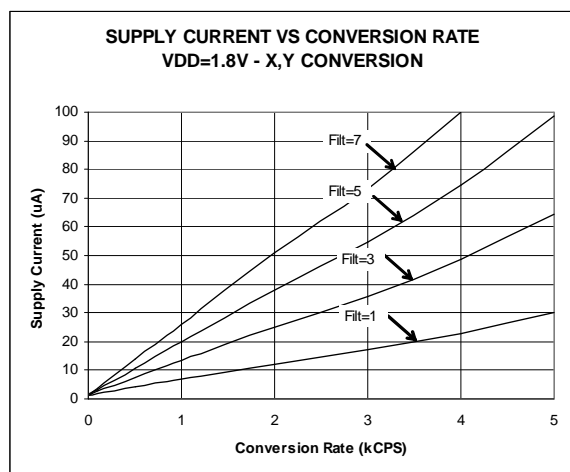
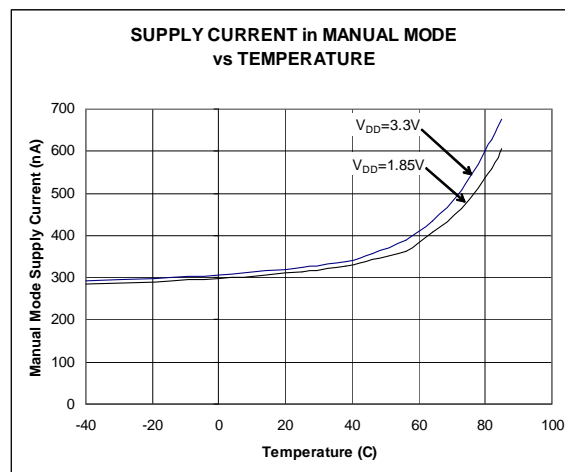
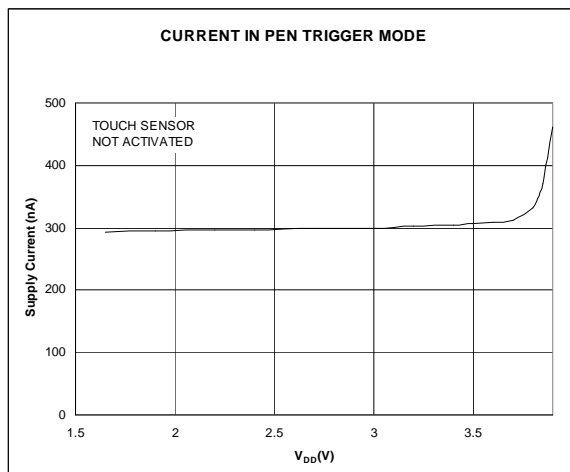


Figure 5. I2C Data timing

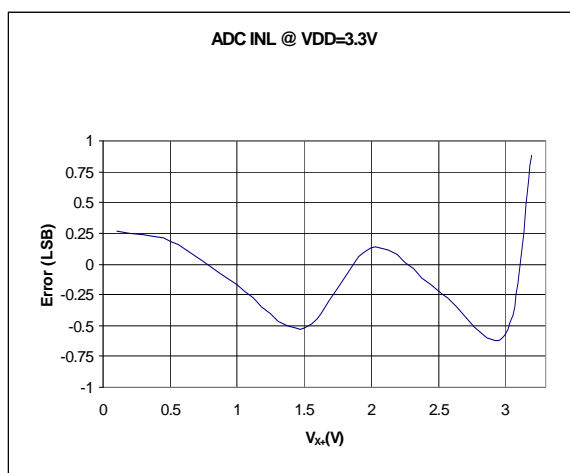
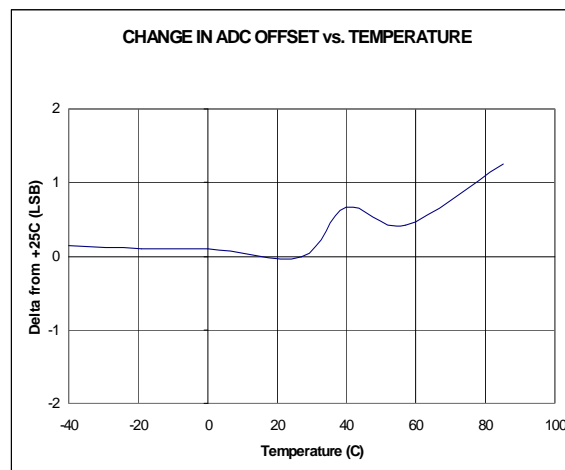
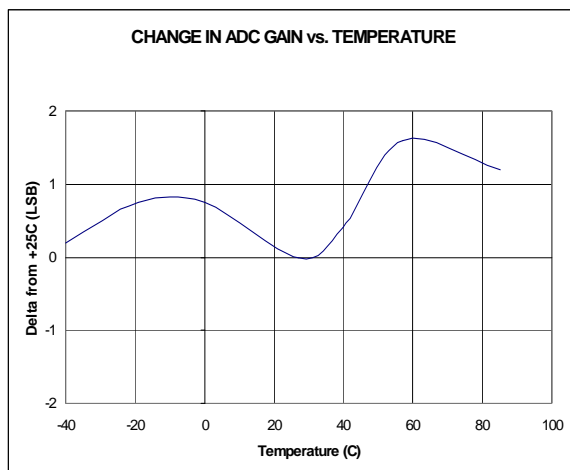
## 2.6. Typical Operating Characteristics

At  $T_a = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{DD} = 1.7\text{V}$  to  $3.7\text{V}$ ,  $\text{PowDly} = 0.5\text{ us}$ ,  $\text{SetDly} = 0.5\text{ us}$ ,  $\text{Filt} = 1$ , Resistive touch screen sensor current not taking in account, unless otherwise noted.



### Typical Operating Characteristics (continued)

At  $T_a = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{DD} = 1.7\text{V}$  to  $3.7\text{V}$ ,  $\text{PowDly} = 0.5\text{ us}$ ,  $\text{SetDly} = 0.5\text{us}$ ,  $\text{Filt} = 1$ , Resistive touch screen sensor current not taking in account, unless otherwise noted.



### 3. Functional Description

#### 3.1. General Introduction

This section provides an overview of the SX8650 architecture, device pinout and a typical application.

The SX8650 is designed for 4-wire resistive touch screen applications (Figure 6). The touch screen or touch panel is the resistive sensor and can be activated by either a finger or stylus. The touch screen coordinates and touch pressure are converted into I2C format by the SX8650 for transfer to the host.

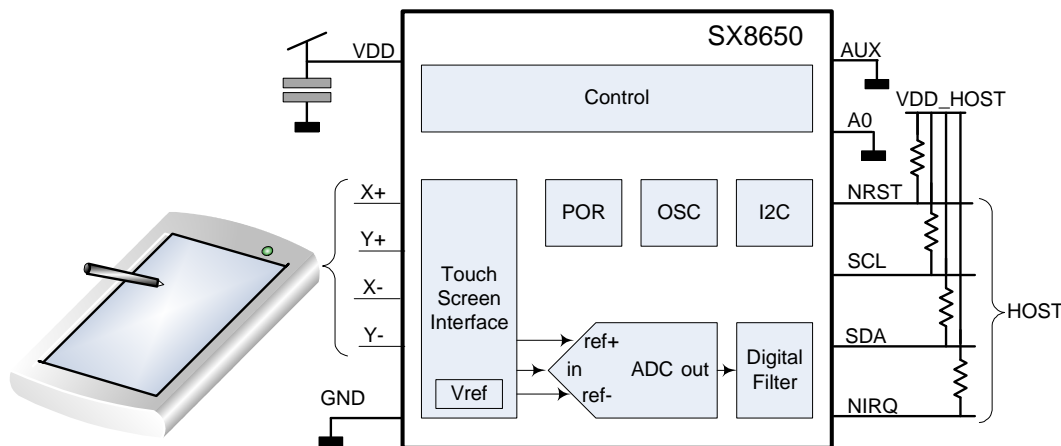


Figure 6. SX8650 with screen

#### 3.2. Channel Pins

##### 3.2.1. X+, X-, Y+, Y-

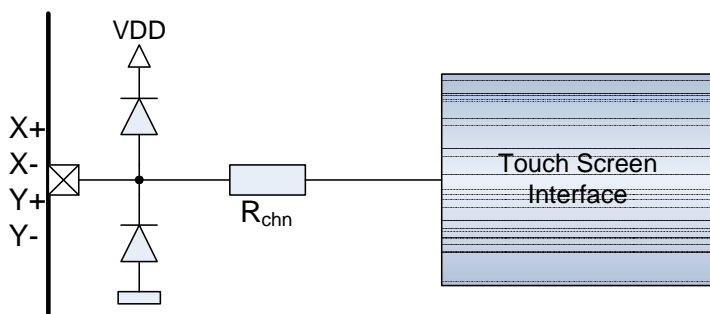


Figure 7. Simplified diagram of X+, X-, Y+, Y- pins

The SX8650's channel pins (X+, X-, Y+, Y-) directly connect to standard touch screen X and Y resistive layers. The SX8650 separately biases each of these layers and converts the resistive values into (X,Y) coordinates.

The channel pins are protected to VDD and GROUND.

Figure 7 shows the simplified diagram of the X+, X-, Y+, Y- pins.

##### 3.2.2. AUX

The SX8650 interface includes an AUX pin that serves two functions: an ADC input; and a start of conversion trigger. When used as an ADC, the single ended input range is from GND to VDD, referred to GND. When the AUX input is configured to start conversions, the AUX input can be further configured as a rising and / or falling edge trigger.

The AUX is protected to VDD and GROUND.

Figure 8 shows a simplified diagram of the AUX pin.

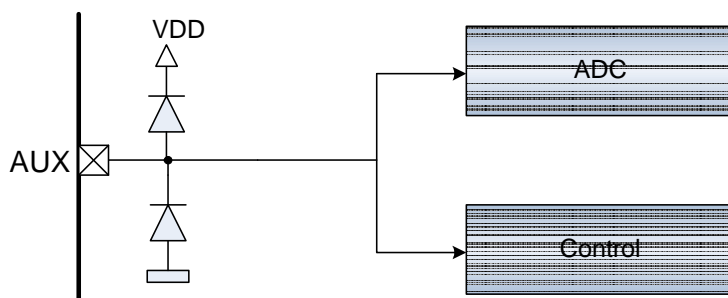
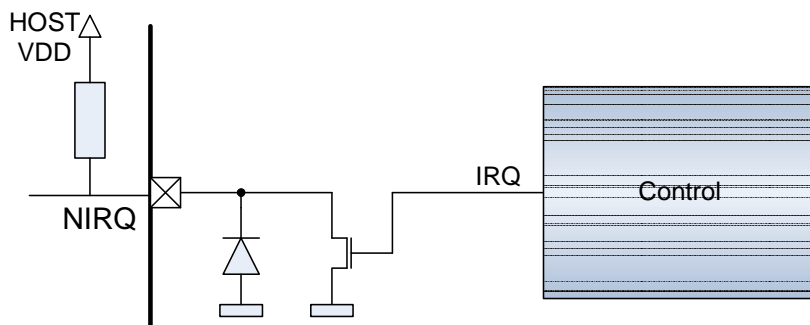


Figure 8. Simplified diagram of AUX

### 3.3. Host Interface and Control Pins

The SX8650 host and control interface consists of: NIRQ, I2C pins SCL and SDA, A0, and NRST.

#### 3.3.1. NIRQ



The NIRQ pin is an active low, open drain output to facilitate interfacing to different supply voltages and thus requires an external pull-up resistor (1-10 kOhm). The NIRQ pin does not have protection to VDD.

The NIRQ function is designed to provide an interrupt to the host processor. Interrupts may occur when a pen is detected, or when channel data is available.

Figure 9 shows a simplified diagram of the NIRQ pin.

Figure 9. Simplified diagram of NIRQ

#### 3.3.2. SCL

The SCL pin is a high-impedance input and open-drain output pin. The SCL pin does not have protection to VDD to conform to I2C slave specifications. An external pull-up resistor (1-10 kOhm) is required.

Figure 10 shows the simplified diagram of the SCL pin.

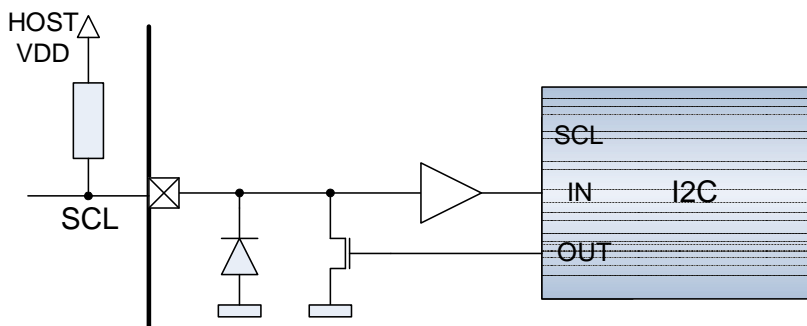
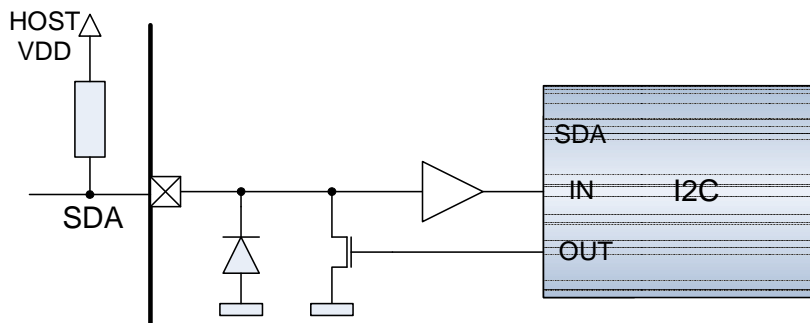


Figure 10. Simplified diagram of SCL

#### 3.3.3. SDA



SDA is an I/O pin. It can be used as an open-drain output (with external pull-up resistor) or as an input. An external pull-up resistor (1-10 kOhm) is required.

The SDA I/O pin does not have protection to VDD to conform to I2C slave specifications.

Figure 11 shows a simplified diagram of the SDA pin.

Figure 11. Simplified diagram of SDA

### 3.3.4. A0

The A0 pin is connected to the I2C address select control circuitry and is used to modify the device I2C address.

The A0 pin is protected to GROUND.

Figure 12 shows a simplified diagram of the A0 pin.

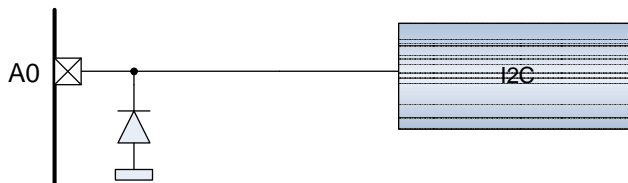


Figure 12. Simplified diagram of A0

### 3.3.5. NRST

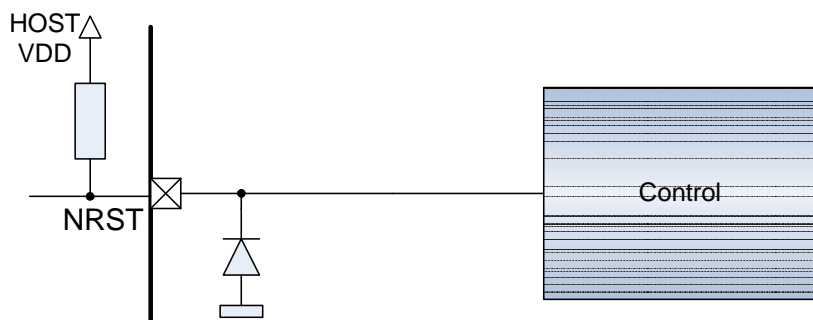


Figure 13. Simplified diagram of NRST

The NRST pin is an active low input that provides a hardware reset of the SX8650's control circuitry.

The NRST pin is protected GROUND to enable interfacing with devices at a different supply voltages.

Figure 13 shows a simplified diagram of the NRST pin.

## 3.4. Power Management Pins

The SX8650's power management input consists of the following Power and Ground pins.

### 3.4.1. VDD

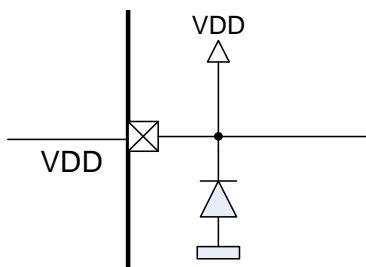


Figure 14. Simplified diagram of VDD

The VDD is a power pin and is the power supply for the SX8650.

The VDD has ESD protection to GROUND.

Figure 14 shows a simplified diagram of the VDD pin.

### 3.4.2. GND

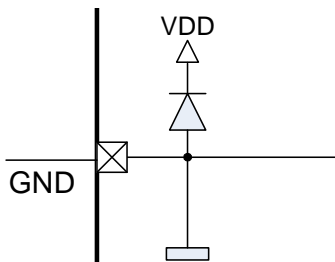


Figure 15. Simplified diagram of GND

The SX8650 has one power management ground pin, GND.

(The die attach paddle on DFN is also connected to GND.)

The GND has ESD protection to VDD.

Figure 15 shows a simplified diagram of the GND pin.

## 4. Detailed Description

### 4.1. Touch Screen Operation

A resistive touch screen consists of two (resistive) conductive sheets separated by an insulator when not pressed. Each sheet is connected through 2 electrodes at the border of the sheet (Figure 16). When a pressure is applied on the top sheet, a connection with the lower sheet is established. Figure 17 shows how the Y coordinate can be measured. The electrode plates are connected through terminals X+, X-, Y+, Y- to an analog to digital converter (ADC) and a reference voltage. The resistance between the terminals X+ and X- is defined by  $R_{xtot}$ .  $R_{xtot}$  will be split in 2 resistors, R1 and R2, in case the screen is touched. The resistance between the terminals Y+ and Y- is represented by R3 and R4. The connection between the top and bottom sheet is represented by the touch resistance ( $R_T$ ).

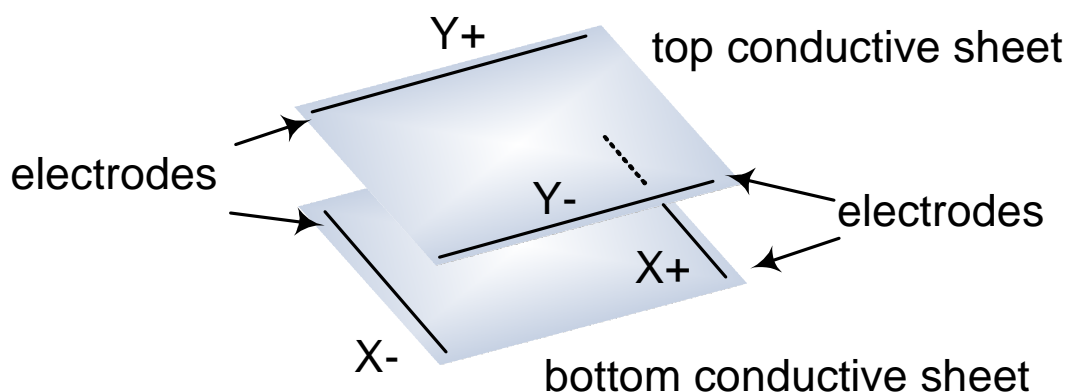


Figure 16. 4-wire Touch Screen

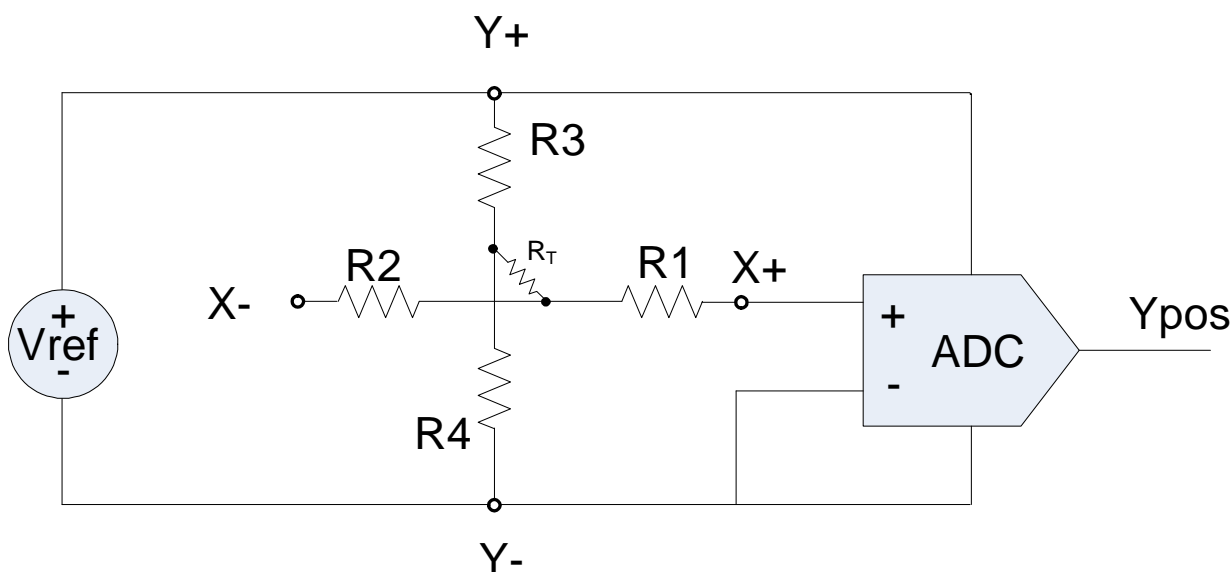


Figure 17. Touch Screen Operation ordinate measurement (Y)



## 4.2. Coordinates Measurement

The top resistive sheet (Y) is biased with a voltage source. Resistors R3 and R4 determine a voltage divider proportional to the Y position of the contact point. Since the converter has a high input impedance, no current flows through R1 so that the voltage X+ at the converter input is given by the voltage divider created by R3 and R4.

The X coordinate is measured in a similar fashion with the bottom resistive sheet (X) biased to create a voltage divider by R1 and R2, while the voltage on the top sheet is measured through R3. Figure 18 shows the coordinates measurement setup. The resistance  $R_T$  is the resistance obtained when a pressure is applied on the screen.  $R_T$  is created by the contact area of the X and Y resistive sheet and varies with the applied pressure.

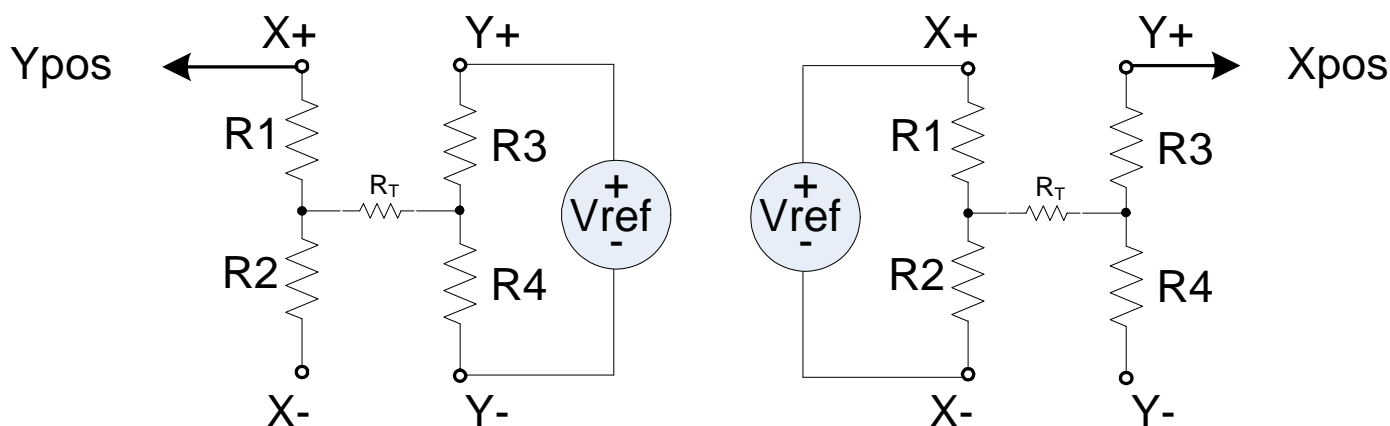


Figure 18. Ordinate (Y) and abscissa (X) coordinates measurement setup

The X and Y position are found by:  $Xpos = 4095 \cdot \frac{R2}{R1 + R2}$      $Ypos = 4095 \cdot \frac{R4}{R3 + R4}$

## 4.3. Pressure Measurement

The pressure measurement consists of two additional setups: z1 and z2 (see Figure 19).

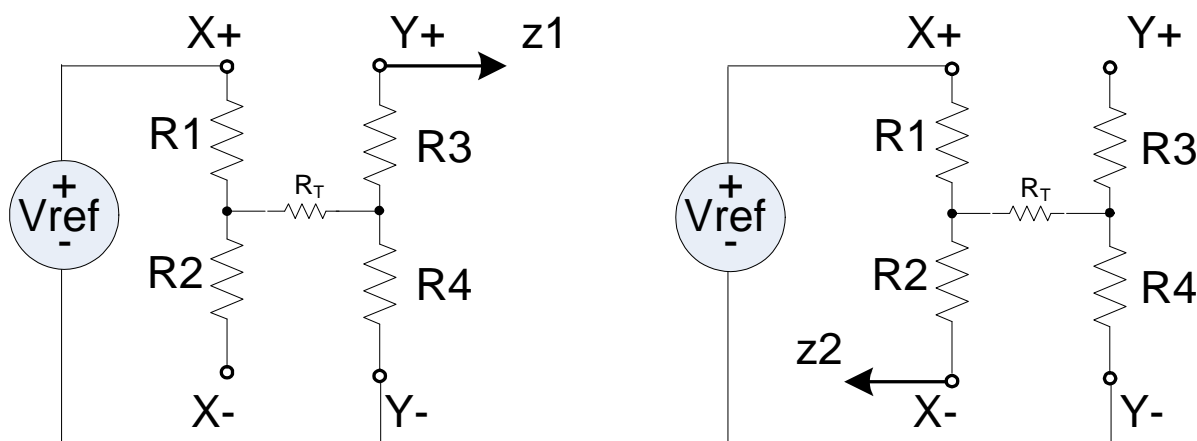


Figure 19. z1 and z2 pressure measurement setup

The corresponding equations for the pressure:  $z1 = 4095 \cdot \frac{R4}{R1 + R4 + R_T}$      $z2 = 4095 \cdot \frac{R4 + R_T}{R1 + R4 + R_T}$

The X and Y total sheet resistance ( $R_{xtot}$ ,  $R_{ytot}$ ) are known from the touch screen supplier.

$R_4$  is proportional to the Y coordinate.

The  $R_4$  value is given by the total Y plate resistance multiplied by the fraction of the Y position over the full coordinate range.

By re-arranging  $z_1$  and  $z_2$  one obtains

$$R_{xtot} = R_1 + R_2$$

$$R_{ytot} = R_3 + R_4$$

$$R_4 = R_{ytot} \cdot \frac{Y_{pos}}{4095}$$

$$R_T = R_4 \cdot \left[ \frac{z_2}{z_1} - 1 \right]$$

$$R_T = R_{ytot} \cdot \frac{Y_{pos}}{4095} \cdot \left[ \frac{z_2}{z_1} - 1 \right]$$

Which results in:

The touch resistance calculation above requires three channel measurements ( $Y_{pos}$ ,  $z_2$  and  $z_1$ ) and one specification data ( $R_{ytot}$ ). An alternative calculation method is using  $X_{pos}$ ,  $Y_{pos}$ , one z channel and both  $R_{xtot}$  and  $R_{ytot}$  shown in the next calculations

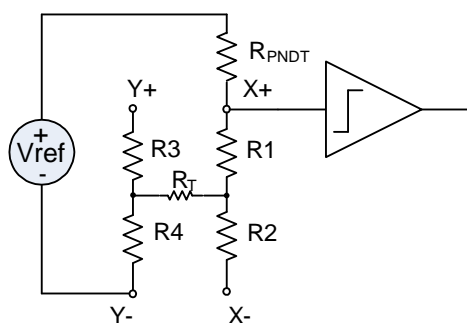
$R_1$  is inverse proportional to the X coordinate.

$$R_1 = R_{xtot} \cdot \left[ 1 - \frac{X_{pos}}{4095} \right]$$

Substituting  $R_1$  and  $R_4$  into  $z_1$  and rearranging terms gives:

$$R_T = \frac{R_{ytot} \cdot Y_{pos}}{4095} \cdot \left[ \frac{4095}{z_1} - 1 \right] - R_{xtot} \cdot \left[ 1 - \frac{X_{pos}}{4095} \right]$$

#### 4.4. Pen Detection



The pen detection circuitry is used both to detect a user action and generate an interrupt or start an acquisition in PENDET and PENTRG mode respectively. Doing a pen detection prior to conversion avoids feeding the host with dummy data and saves power.

If the touchscreen is powered between  $X+$  and  $Y-$  through a resistor  $R_{PNDT}$ , no current will flow so long as pressure is not applied to the surface (see Figure 20). When some pressure is applied, a current path is created and brings  $X+$  to the level defined by the resistive divider determined by  $R_{PNDT}$  and the sum of  $R_1$ ,  $R_T$  and  $R_4$ .

The level is detected by a comparator.

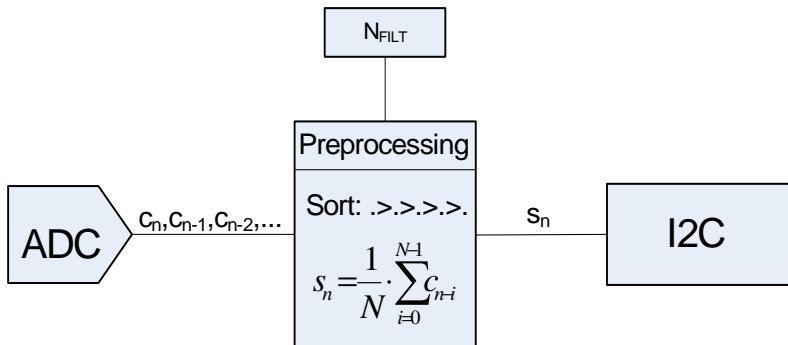
Figure 20. Pen detection

$R_{PNDT}$  should be set to the greatest value 200 kOhm for optimal detection (see Table 6). Increasing PowDly settings can also improve the detection on panel with high resistance.

The pen detection will set the PENIRQ bit of the RegStat register.

In PENDET mode, the pen detection will set NIRQ low. The PENIRQ bit will be cleared and the NIRQ will be de-asserted as soon as the host reads the status register.

## 5. Data Processing



The SX8650 offers 4 types of data processing which allows the user to make trade-offs between data throughput, power consumption and noise rejection.

The parameter FILT is used to select the filter order  $N_{\text{filt}}$ . The noise rejection will be improved with a high order to the detriment of the power consumption. The K coefficient in Table 4 is a filter constant. Its value is  $K=4079/4095$ .

Figure 21. Filter structure

| FILT | $N_{\text{filt}}$ | Processing   |
|------|-------------------|--|
| 0    | 1                 | $s_n = c_n$<br>No average.   |
| 1    | 3                 | $= \frac{1}{3} \cdot \frac{4079}{4095} (c_n + c_{n-1} + c_{n-2})$<br>3 ADC samples are averaged  |
| 2    | 5                 | $= \frac{1}{5} \cdot \frac{4079}{4095} (c_n + c_{n-1} + c_{n-2} + c_{n-3} + c_{n-4})$<br>5 ADC samples are averaged  |
| 3    | 7                 | $c_{\text{max}1} \geq c_{\text{max}2} \geq c_a \geq c_b \geq c_c \geq c_{\text{min}1} \geq c_{\text{min}2}$<br>$= \frac{1}{3} \cdot \frac{4079}{4095} (c_a + c_b + c_c)$<br>7 ADC samples are sorted and the 3 center samples are averaged |

Table 4. Filter order

### 5.1. Host Interface and Control

The host interface consists of I2C (SCL and SDA) and the NIRQ, A0, NRST signals.

The I2C implemented on the SX8650 is compliant with:

- ◆ Standard Mode (100 kbit/s) & Fast Mode (400 kbit/s)
- ◆ Slave mode
- ◆ 7 bit slave address

#### 5.1.1. I2C Address

Pin A0 defines the LSB of the I2C address. It is shown on Figure 22.

$$\text{SX8650 Slave Address}(7:1) = \begin{cases} 1001000 & \text{with pin A0 connected to ground} \\ 1001001 & \text{with pin A0 connected to VDD} \end{cases}$$

Figure 22. I2C slave address

Upon request of the customer, a custom I2C address can be burned in the NVM.

The host uses the I2C to read and write data and commands to the configuration and status registers. During a conversion, the I2C clock can be stretched until the end of the processing.

Channel data read is done by I2C throughput optimized formats.

The supported I2C access formats are described in the next sections:

- ◆ I2C Write Registers
- ◆ I2C Read Registers
- ◆ I2C Host Commands
- ◆ I2C Read Channels

### 5.1.2. I2C Write Registers

The format for I2C write is given in Figure 23.

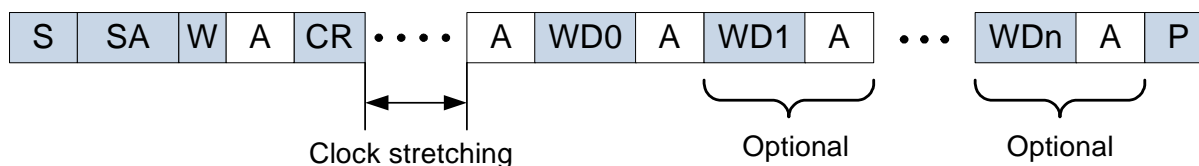
After the start condition [S], the SX8650 slave address (SA) is sent, followed by an eighth bit (W='0') indicating a Write.

The SX8650 then Acknowledges [A] that it is being addressed, and the host sends 8-bit Command and Register address consisting of the command bits '000' followed by the SX8650 Register Address (RA).

The SX8650 Acknowledges [A] and the host sends the appropriate 8-bit Data Byte (WD0) to be written.

Again the SX8650 Acknowledges [A].

In case the host needs to write more data, a succeeding 8-bit Data Byte will follow (WD1), acknowledged by the slave [A]. This sequence will be repeated until the host terminates the transfer with the Stop condition [P].



S: Start condition  
SA: SX8650 Slave Address(7:1)  
W: '0'  
A: Acknowledge  
CR: '000' + Register Address(4:0)  
WDn: Write Data byte(7:0), 0...n  
P: Stop condition



 From host to SX8650  
 From SX8650 to host

Figure 23. I2C write register

The register address increments automatically when successive register data (WD1...WDn) is supplied by the host. This automatic increment can be used for the first 4 register addresses (see Table 6).

The correct sampling of the screen by the SX8650 and the host I2C bus traffic are events that might occur simultaneously. The SX8650 will synchronize these events by the use of clock stretching if that is required. The stretching occurs directly after the last received command bit (see Figure 23).

### 5.1.3. I2C Read Registers

The format for incremental I2C read for registers is given in Figure 24. The read has to start with a write of the read address.

After the start condition [S], the SX8650 Slave Address (SA) is sent, followed by an eighth bit (W='0') indicating a Write. The SX8650 then Acknowledges [A] that it is being addressed, and the host responds with a 8-bit CR Data consisting of '010' followed by the Register Address (RA). The SX8650 responds with an Acknowledge [A] and the host sends the Repeated Start Condition [Sr]. Once again, the SX8650 Slave Address (SA) is sent, followed by an eighth bit (R='1') indicating a Read.

The SX8650 responds with an Acknowledge [A] and the read Data byte (RD0). If the host needs to read more data it will acknowledge [A] and the SX8650 will send the next read byte (RD1). This sequence can be repeated until the host terminates with a NACK [N] followed by a stop [P].

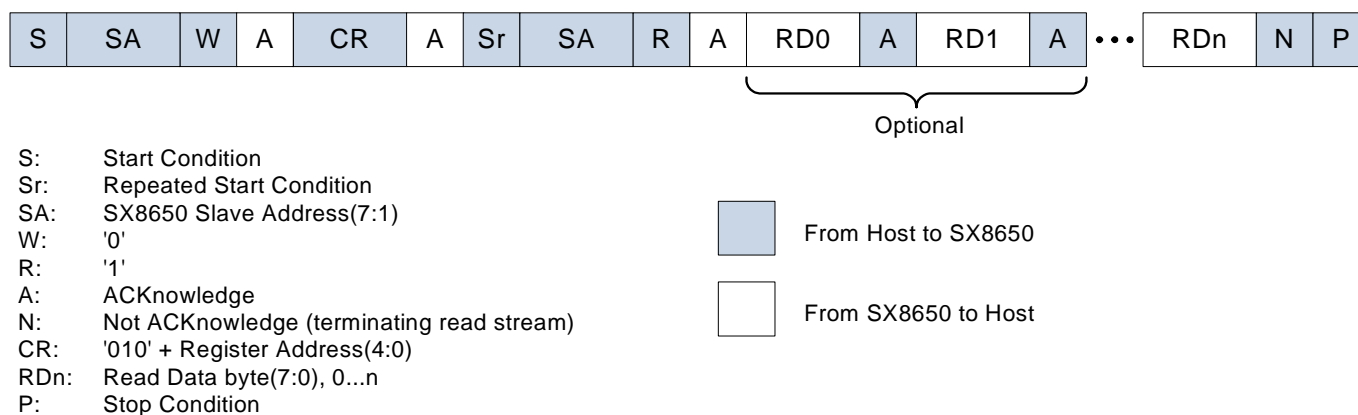


Figure 24. I2C read registers

The I2C read register format of Figure 24 is maintained until the Stop Condition. After the Stop Condition the SX8650 is performing succeeding reads by the compact read format of the I2C read channels described in the next section.

No clock stretching will occur for the I2C read registers.

### 5.1.4. I2C Host Commands

The format for I2C commands is given in Figure 25.

After the start condition [S], the SX8650 Slave Address (SA) is sent, followed by an eighth bit (W='0') indicating a Write. The SX8650 then Acknowledges [A] that it is being addressed, and the host responds with an 8-bit Data consisting of a '1' + command(6:0). The SX8650 Acknowledges [A] and the host sends a stop [P].

The exact definition of command(6:0) can be found in Table 8.

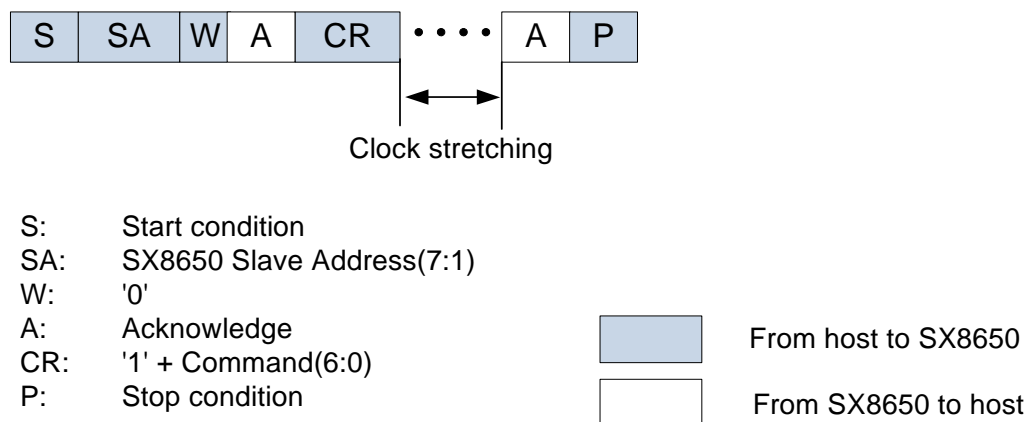


Figure 25. I2C host command

The sampling of the screen by the SX8650 and the host I2C bus traffic are events that might occur simultaneously. The SX8650 will synchronize these events by the use of clock stretching if that is required. The stretching occurs directly after the last received command bit (see Figure 25).

### 5.1.5. I2C Read Channels

The host is able to read the channels with a high throughput, by the format shown in Figure 26.

After the start condition [S], the SX8650 Slave Address (SA) is sent, followed by an eighth bit (R='1') indicating a read. The SX8650 responds with an Acknowledge [A] and the Read Data byte (RD0). The host sends an Acknowledge [A] and the SX8650 responds with the Read Data byte (RD1). If the host needs to read more data, it will acknowledge [A] and the SX8650 will send the next read bytes. This sequence can be repeated until the host terminates with a NACK [N] followed immediately by a stop [P]. The NACK [N] releases the NIRQ line. The stop [P] must occur before the end of the conversion.

The channel data that can be read is defined by the last conversion sequence.

A maximum number of 10 data bytes is passed when all channels (X, Y, z1, z2 and AUX) are activated in the "I2CRegChanMsk".

The channel data is sent with the following order: X, Y, Z1, Z2, AUX. The first byte of the data contains the channel information as shown in Figure 27.

Typical applications require only X and Y coordinates, thus only 4 bytes of data will be read.

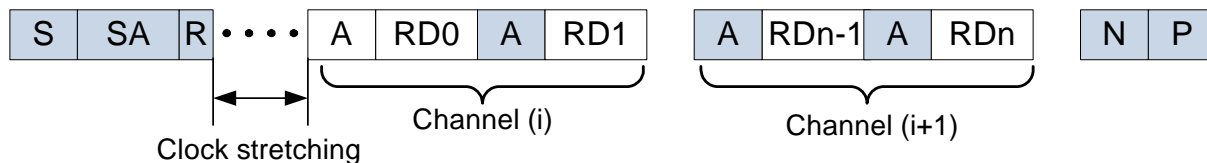


Figure 26. I2C read channels

The sampling of the screen by the SX8650 and the host I2C bus traffic are events that might occur simultaneously. The SX8650 will synchronize these events by the use of clock stretching if that is required. The stretching occurs directly after the address and read bit have been sent for the I2C read channels command (see Figure 26).

### 5.1.6. Data Channel Format

Channel data is coded on 16 bits as shown in Figure 27

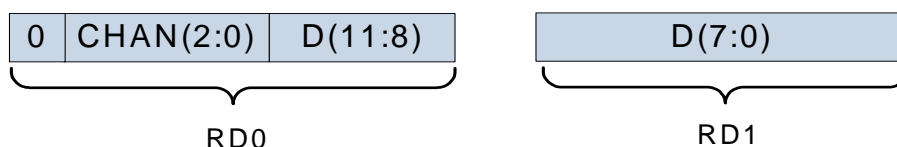


Figure 27. data channel format

The 3 bits CHAN(2:0) are defined in Table 9 and show which channel data is referenced. The channel data D(11:0) is of unsigned format and corresponds to a value between 0 and 4095.

### 5.1.7. Invalid Qualified Data

The SX8650 will return 0xFFFF data in case of invalid qualified data.

This occurs:

- ◆ when the SX8650 converted channels and the host channel readings do not correspond. E.g. the host converts X and Y and the host tries to read X, Y and z1 and z2.
- ◆ when a conversion is done without a pen being detected.

## 5.2. I2C Register Map

| I2C register address RA(4:0) | Register        | Description |
|------------------------------|-----------------|-------------|
| 0 0000                       | I2CRegCtrl0     | Write, Read |
| 0 0001                       | I2CRegCtrl1     | Write, Read |
| 0 0010                       | I2CRegCtrl2     | Write, Read |
| 0 0100                       | I2CRegChanMsk   | Write, Read |
| 0 0101                       | I2CRegStat      | Read        |
| 1 1111                       | I2CRegSoftReset | Write       |

Table 5. I2C Register address

The details of the registers are described in the next sections.

### 5.3. Host Control Writing

The host control writing allows the host to change SX8650 settings. The control data goes from the host towards the SX8650 and may be read back for verification.

| register    | bits | default | description |   |
|-------------|------|---------|-------------|---|
| I2CRegCtrl0 | 7:4  | 0000    | RATE        | Set rate in coordinates per sec (cps) ( $\pm 20\%$ )<br>If RATE equals zero then Manual mode.<br>if RATE is larger than zero then Automatic mode  |
|             |      |         |             | <div> <div>0000: Timer disabled -Manual mode</div> <div>0001: 10 cps</div> <div>0010: 20 cps</div> <div>0011: 40 cps</div> <div>0100: 60 cps</div> <div>0101: 80 cps</div> <div>0110: 100 cps</div> <div>0111: 200 cps</div> </div> <div> <div>1000: 300 cps</div> <div>1001: 400 cps</div> <div>1010: 500 cps</div> <div>1011: 1k cps</div> <div>1100: 2k cps</div> <div>1101: 3k cps</div> <div>1110: 4k cps</div> <div>1111: 5k cps</div> </div> |
|             | 3:0  | 0000    | POWDLY      | Settling time ( $\pm 10\%$ ): The channel will be biased for a time of POWDLY before each channel conversion  |
|             |      |         |             | <div> <div>0000: Immediate (0.5 us)</div> <div>0001: 1.1 us</div> <div>0010: 2.2 us</div> <div>0011: 4.4 us</div> <div>0100: 8.9 us</div> <div>0101: 17.8 us</div> <div>0110: 35.5 us</div> <div>0111: 71.0 us</div> </div> <div> <div>1000: 0.14 ms</div> <div>1001: 0.28 ms</div> <div>1010: 0.57 ms</div> <div>1011: 1.14 ms</div> <div>1100: 2.27 ms</div> <div>1101: 4.55 ms</div> <div>1110: 9.09 ms</div> <div>1111: 18.19 ms</div> </div>   |
| I2CRegCtrl1 | 7:6  | 00      | AUXAQC      | <div>00: AUX is used as an analog input</div> <div>01: On rising AUX edge, wait POWDLY and start acquisition</div> <div>10: On falling AUX edge, wait POWDLY and start acquisition</div> <div>11: On rising and falling AUX edges, wait POWDLY and start acquisition</div>  |
|             |      |         |             | The AUX trigger requires the manual mode.   |
|             | 5    | 1       | CONDIRQ     | Enable conditional interrupts<br>0: interrupt always generated at end of conversion cycle. If no pen is detected the data is set to 'invalid qualified'.<br>1: interrupt generated when pen detect is successful  |
|             | 4    | 0       | reserved    |   |
|             | 3:2  | 00      | RPDNT       | Select the Pen Detect Resistor<br>00: 100 KOhm<br>01: 200 KOhm<br>10: 50 KOhm<br>11: 25 KOhm  |
|             | 1:0  | 00      | FILT        | Digital filter control<br>00: Disable<br>01: 3 sample averaging<br>10: 5 sample averaging<br>11: 7 sample acquisition, sort, average 3 middle samples   |

Table 6. I2C registers



| register        | bits  | default | description   |   |   |
|-----------------|---|---------|---|---|---|
| I2CRegCtrl2     | 7:4   | 0       | reserved  |   |   |
|                 | 3:0   | 0000    | SETDLY  | Settling time while filtering (± 10%)<br>When filtering is enabled, the channel will initially bias for a time of POWDLY for the first conversion, and for a time of SETDLY for each subsequent conversion in a filter set. |   |
|                 |   |         |   | 0000: Immediate (0.5 us)<br>0001: 1.1 us<br>0010: 2.2 us<br>0011: 4.4 us<br>0100: 8.9 us<br>0101: 17.8 us<br>0110: 35.5 us<br>0111: 71.0 us   | 1000: 0.14 ms<br>1001: 0.28 ms<br>1010: 0.57 ms<br>1011: 1.14 ms<br>1100: 2.27 ms<br>1101: 4.55 ms<br>1110: 9.09 ms<br>1111: 18.19 ms |
| I2CRegChanMsk   | 7   | 1       | XCONV   | 0: no sample<br>1: sample, report X channel   |   |
|                 | 6   | 1       | YCONV   | 0: no sample<br>1: sample, report Y channel   |   |
|                 | 5   | 0       | Z1CONV  | 0: no sample<br>1: sample, report Z1 channel  |   |
|                 | 4   | 0       | Z2CONV  | 0: no sample<br>1:sample, report Z2 channel   |   |
|                 | 3   | 0       | AUXCONV   | 0: no sample<br>1: sample, report AUX channel   |   |
|                 | 0   | 0       | reserved  |   |   |
|                 | 0   | 0       | reserved  |   |   |
|                 | 0   | 0       | reserved  |   |   |
| I2CRegStat      | The host status reading allows the host to read the status of the SX8650. The data goes from the SX8650 towards the host. Host writing to this register is ignored. |         |   |   |   |
|                 | 7   | 0       | CONVIRQ   | 0: no IRQ pending<br>1: End of conversion sequence IRQ pending<br>IRQ is cleared by the I2C channel reading   |   |
|                 | 6   | 0       | PENIRQ  | operational in pen detect mode<br>0: no IRQ pending<br>1: Pen detected IRQ pending<br>IRQ is cleared by the I2C status reading  |   |
|                 | 5:0   | 000000  | reserved  |   |   |
| I2CRegSoftReset | 7:0   | 0x00    | If the host writes the value 0xDE to this register, then the SX8650 will be reset.<br>Any other data will not affect the SX8650 |   |   |

*Table 6. I2C registers*

## 5.4. Host Commands

The host can write to and read from registers of the SX8650 by the write and read commands as defined in Table 7.

| W/R command name | CR(7:0) |   |   |         |   |   |   |   | Function                            |
|------------------|---------|---|---|---------|---|---|---|---|-------------------------------------|
|                  | 7       | 6 | 5 | 4       | 3 | 2 | 1 | 0 |                                     |
| WRITE(RA)        | 0       | 0 | 0 | RA(4:0) |   |   |   |   | Write register (see Table 5 for RA) |
| READ(RA)         | 0       | 1 | 0 | RA(4:0) |   |   |   |   | Read register (see Table 5 for RA)  |

Table 7. I2C W/R commands

The host can issue commands to change the operation mode or perform manual actions as defined in Table 8.

| command name  | CR(7:0) |   |   |   |   |           |   |   | Function   |
|---------------|---------|---|---|---|---|-----------|---|---|--|
|               | 7       | 6 | 5 | 4 | 3 | 2         | 1 | 0 |  |
| SELECT(CHAN)  | 1       | 0 | 0 | 0 | x | CHAN(2:0) |   |   | Bias channel (see Table 9 for CHAN)  |
| CONVERT(CHAN) | 1       | 0 | 0 | 1 | x | CHAN(2:0) |   |   | Bias channel (see Table 9 for CHAN)<br>Wait POWDLY settling time<br>Run conversion |
| MANAUTO       | 1       | 0 | 1 | 1 | x | x         | x | x | Enter manual or automatic mode.  |
| PENDET        | 1       | 1 | 0 | 0 | x | x         | x | x | Enter pen detect mode.   |
| PENTRG        | 1       | 1 | 1 | 0 | x | x         | x | x | Enter pen trigger mode.  |

Table 8. I2C commands

The channels are defined as in Table 9.

| Channel  | CHAN(2:0) |   |   | Function   |
|----------|-----------|---|---|--|
|          | 2         | 1 | 0 |  |
| X        | 0         | 0 | 0 | X channel  |
| Y        | 0         | 0 | 1 | Y channel  |
| Z1       | 0         | 1 | 0 | First channel for pressure measurement                                   |
| Z2       | 0         | 1 | 1 | Second channel for pressure measurement                                  |
| AUX      | 1         | 0 | 0 | Auxiliary channel  |
| reserved | 1         | 0 | 1 |  |
| reserved | 1         | 1 | 0 |  |
| SEQ      | 1         | 1 | 1 | Channel sequentially selected from I2CRegChanMsk register, (see Table 8) |

Table 9. channel definition

## 5.5. Power-Up

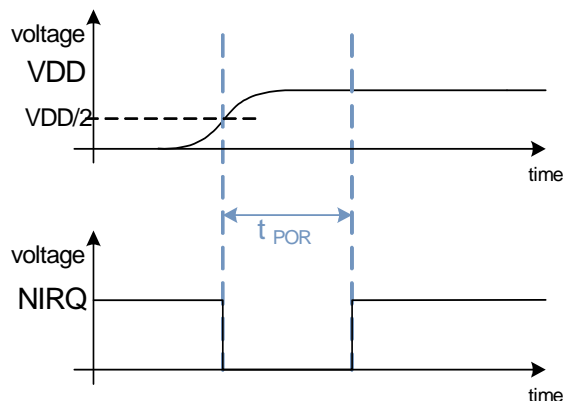


Figure 28. Power-up, NIRQ

## 5.6. Reset

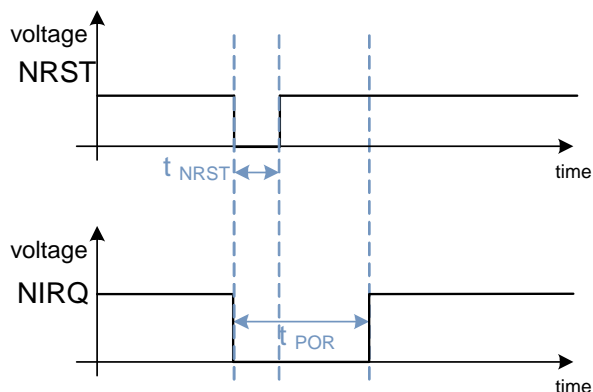


Figure 29. Reset

The NIRQ pin is kept low during SX8650 power-up.

During power-up, the SX8650 is not accessible and I2C communications are ignored.

As soon as NIRQ rises, the SX8650 is ready for I2C communication.

After startup, the host must wait  $t_{por}$  before any communication with the SX8650.

The POR of the SX8650 will reset all registers and states of the SX8650 at power-up.

Additionally the host can reset the SX8650 by asserting the NRST pin (active low) and also via the I2C bus.

If NRST is driven LOW, then NIRQ will be driven low by the SX8650. When NRST is released (or set to high) then NIRQ will be released by the SX8650.

The circuit has also a soft reset capability. When writing the code 0xDE to the register RegSoftReset, the circuit will be reset.

## 6. Modes of Operation

The SX8650 has four operation modes that are configured using the I2C commands as defined in Table 8 and Table 6. These 4 modes are:

- ◆ manual (command 'MANAUTO' and RATE=0),
- ◆ automatic (command 'MANAUTO' and RATE>0),
- ◆ pen detect (command 'PENDET'),
- ◆ pen trigger mode (command 'PENTRG').

At startup the SX8650 is set in manual mode.

In the manual mode the SX8650 is entirely stopped except for the I2C peripheral which accepts host commands. This mode requires RATE equal to be zero (RATE = 0, see Table 6).

In the automatic mode the SX8650 will sequence automatic channel conversions. This mode requires RATE to be larger than zero (RATE > 0, see Table 6).

In the PENDET mode the pen detection is activated. The SX8650 will generate an interrupt (NIRQ) upon pen detection and set the PENIRQ bit in the I2C status register. To quit the PENDET mode the host needs to configure the manual mode.

In the PENTRG mode the pen detection is activated and a channel conversion will start after the detection of a pen. The SX8650 will generate an interrupt (NIRQ) upon pen detection and set the CONVIRQ bit in the I2C status register. To quit the PENTRG mode the host needs to configure the manual mode. The PENTRG mode offers the best compromise between power consumption and coordinate throughput.

### 6.1. Manual Mode

In manual mode (RATE=0) single actions are triggered by the I2C commands described in Table 10.

When a command is received, the SX8650 executes the associated task and waits for the next command. It is up to the host to sequence all actions.

| Command       | Action  |
|---------------|---|
| CONVERT(CHAN) | Select and bias a channel<br>Wait for the programmed settling time (POWDLY)<br>Start conversion |
| SELECT(CHAN)  | Select and bias a channel   |

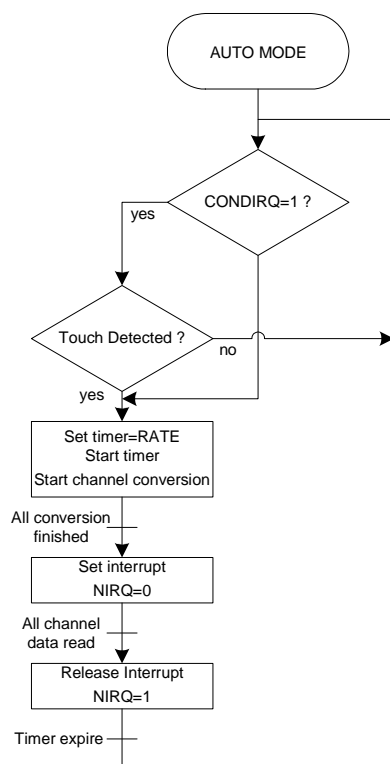
*Table 10 CONVERT and SELECT command*

The channel can be biased for an arbitrary amount of time by first sending a SELECT command and then a CONVERT command once the settling time requirement is met.

The SELECT command can be omitted if the large range of POWDLY settings cover the requirements. In the latter case, the CONVERT command alone is enough to perform an acquisition.

With CHAN=SEQ, multiple channels are sampled. This requires programming the POWDLY field in register RegCTRL0. The selected channel will be powered during POWDLY before a conversion is started. The channel bias is automatically removed after the conversion has completed.

## 6.2. Automatic mode



In automatic mode ( $RATE > 0$ ), SX8650 will automatically decide when to start acquisition, sequence all the acquisitions and alerts the host if data is available for download with a NIRQ. The host will read the channels and the SX8650 will start again with the next conversion cycle.

The fastest coordinate rate is obtained if the host reads the channels immediately after the NIRQ.

To not loose data, the SX8650 will not begin conversion before the host read the channels. If after the NIRQ a delay superior to the sampling period is made by the host to read the channels a slower coordinate rate is obtained.

When the control CONDIRQ bit (see register I2CRegStat Table 6) is set to '1' then the interrupts will only be generated if the pen detect occurred. This result in a regular interrupt stream, as long as the host performs the read channel commands, and the screen is touched. When the screen is not touched, interrupts does not occur.

If the control CONDIRQ bit is cleared to '0', the interrupts will always be generated. In case there is no pen detected on the screen then the coordinate data will be qualified as invalid, see section [5.1.7]. This result in a regular interrupt stream, as long as the host performs the read channel commands, independent of the screen being touched or not.

This working is illustrated in Figure 30.

Figure 30. AUTO Mode Flowchart

Figure 31 shows the I2C working in automatic mode. After the first sentence send throught the I2C to make the initialization, traffic is reduced as only reads are required.

The processing time is the necessary time for the SX8650 to makes the pendetection, the settling time (POWDLY) and the conversion. This time increases with the number of channel selected and the filter used. All succeeding conversions notifies the host by an interrupt signal and the host only needs to issue the I2C read command.

The reads occur at the RATE interval.

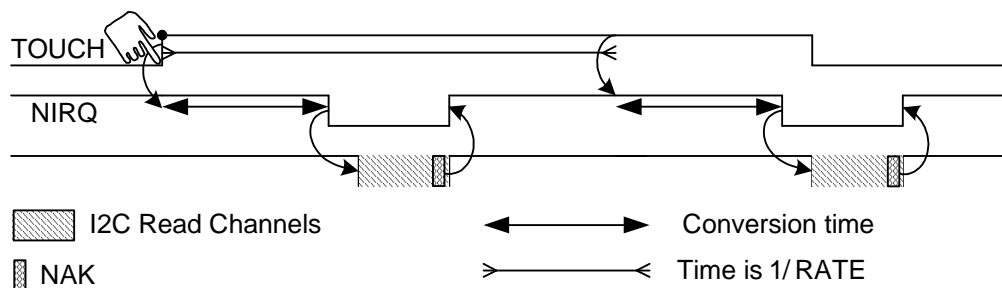
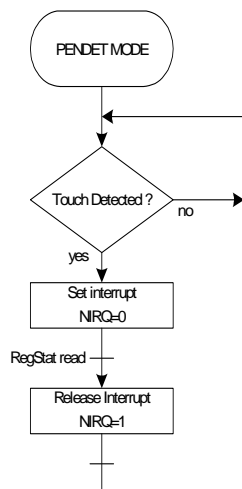


Figure 31. I2C working in AUTO mode

### 6.3. PENDET Mode



The PENDET mode can be used if the host only needs to know if the screen has been touched or not and take from that information further actions. When pen detect circuitry is triggered the interrupt signal NIRQ will be generated and the status register bit 'PENIRQ' will be set. The bit is cleared by reading the status register RegStat.

Figure 32. PENDET Mode Flowchart

### 6.4. PENTRIG Mode

The PENTRIG mode offers the best compromise between power consumption and coordinate throughput.

In this mode the SX8650 will wait until a pen is detected on the screen and then starts the coordinate conversions. The host will be signalled only when the screen is touched and coordinates are available.

The coordinate rate in pen trigger mode is determined by the speed of the host reading the channels and the conversion times of the channels. The host performs the minimum number of I2C commands in this mode.

The host has to wait for the NIRQ interrupt to make the acquisition of the datas.

The flowchart and the I2C working is illustrated in Figure 33.

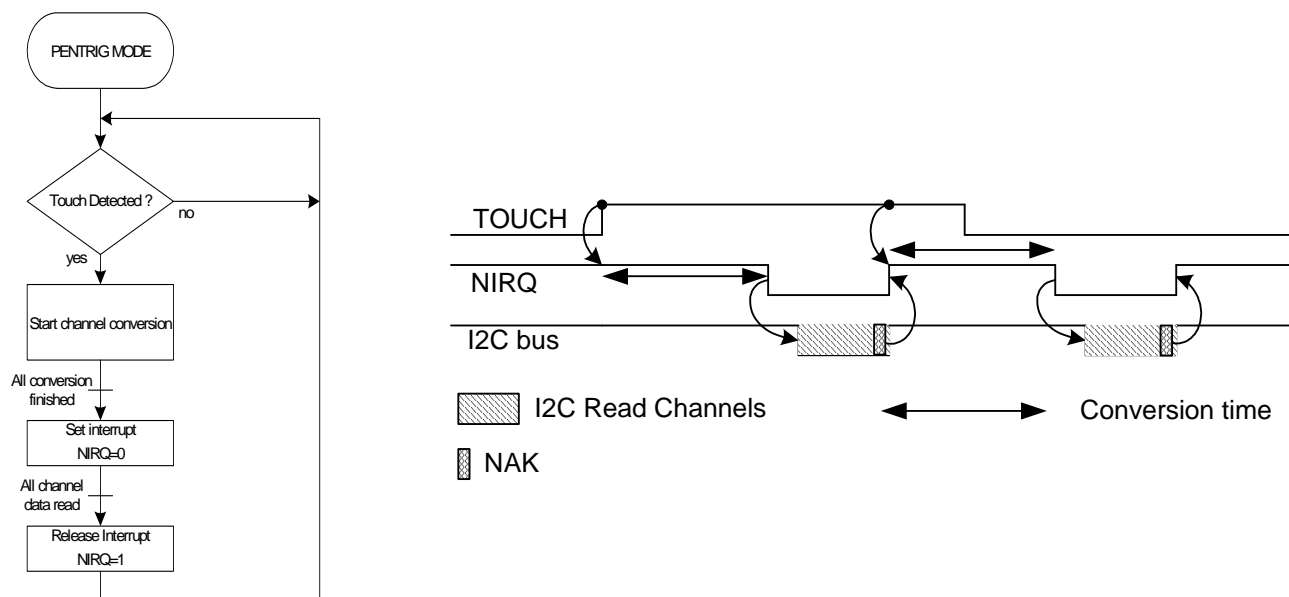


Figure 33. PENTRIG Mode Flowchart and I2C working in PENTRIG mode

## 7. Application Information

This section describes in more detail application oriented data.

### 7.1. Acquisition Setup

Prior to an acquisition, the SX8650 can be setup by writing the control registers. Registers are written by issuing the register write command. They can be read by issuing the read command. Please refer to the section [5.3].

If no registers are written, the circuit will start in manual mode.

### 7.2. Channel Selection

The SX8650 can be setup to start a single channel conversion or to convert several channels in sequence. For a single conversion, the channel to be converted is determined from the CHAN(2:0) field in the command word (defined in Table 9). Several channels can be acquired sequentially by setting the CHAN(2:0) field to SEQ. The channels will be sampled in the order defined by register RegChanMsk from MSB to LSB.

If a “one” is written in a channel mask, the corresponding channel will be sampled, in the opposite case, it is ignored and the next selected channel is chosen.

### 7.3. Noise Reduction

A noisy environment can decrease the performance of the controller. For example, an LCD display located just under the touch screen can add a lot of noise on the high impedance A/D converter inputs.

#### 7.3.1. POWDLY

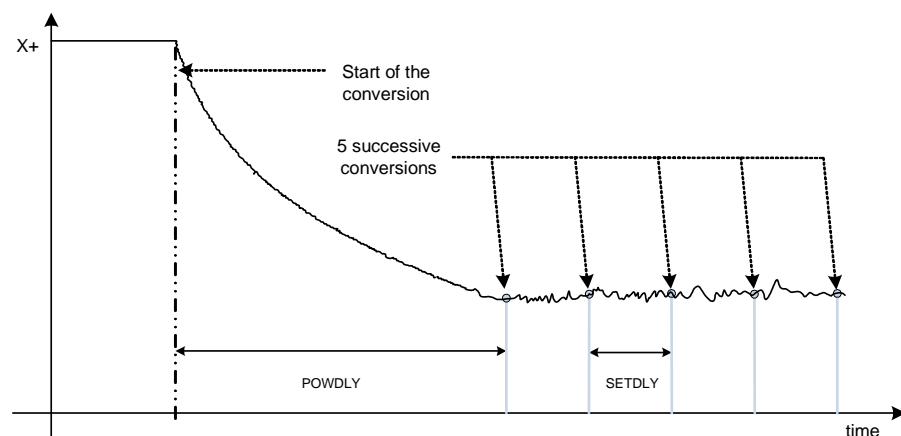
In order to perform correct coordinates acquisition properly, some time must be given for the touch screen to reach a proper level. It is a function of the PCB trace resistance connecting the SX8650 to the touchscreen and also the capacitance of the touchscreen. If tau is this RC time constant then POWDLY duration must be programmed to 10 tau to reach 12 bit accuracy.

Adding a capacitor from the touch screen drivers to ground is a solution to minimize external noise. A low-pass filter created by the capacitor may increase settling time. Therefore, use POWDLY to stretch the acquisition period. POWDLY can be estimated by the following formula :  $PowDly = 10 \times R_{touch} \times C_{touch}$

$R_{touch}$  is the sum of the panel resistances plus any significant series input resistance,  $R_{xtot} + R_{ytot} + R_i$ .

$C_{touch}$  is the sum of the touch panel capacitance plus any noise filtering and routing capacitances.

### 7.3.2. SETDLY



A second method of noise filtering uses an averaging filter as described in section [5] (Data processing). In this case, the chip will sequence up to 7 conversions on each channel. The parameter SETDLY sets the settling time between the consecutive conversions.

In most applications, SETDLY can be set to 0. In some particular applications, where accuracy of 1LSB is required and  $C_{touch}$  is less than 100nF a specific value should be determined.

Figure 34. POWDLY and SETDLY timing with FILT=2

### 7.3.3. AUX Input

An alternate conversion trigger method can be used if the host system provides additional digital signals that indicate noisy or noise-free periods. The SX8650 can be set up to start conversions triggered by the AUX pin. A rising edge, a falling edge or both can trigger the conversion. To enter this mode, AUXACQ must be set to a different value than '00' as defined in Table 6. The AUX edge will first trigger the bias delay (POWDLY). Following the programmed delay, the channel acquisition takes place.

## 7.4. Interrupt Generation

An interrupt (NIRQ=0) will be generated:

- ◆ During the power-up phase or after a reset
- ◆ After completion of a conversion in MANUAL, PENTRIG or AUTO mode. CONVIRQ (bit [7] of RegStat) will be set at the same time.
- ◆ After a touch on the panel is detected in PENDET mode. PENIRQ (bit [6] of RegStat) will be set at the same time.

The NIRQ will be released and pulled high (NIRQ=1) by the external pull-up resistor:

- ◆ When the power-up phase is finished
- ◆ When the host read all channels data that were previously converted by the SX8650 in MANUAL, PENTRIG or AUTO mode. CONVIRQ will be cleared at the same time.
- ◆ When the host read the status register in PENDET mode. PENIRQ, will be cleared at the same time.

An active NIRQ (low) needs to be cleared before any new conversions will occur.

## 7.5. Coordinate Throughput Rate

The coordinate throughput rate depends on the following factors:

- ◆ The I2C communication time :  $T_{com}$
- ◆ The conversion time :  $T_{conv}$

The coordinate rate is the frequency to get the X, Y, Z1 and Z2 coordinate:  $CoordRate = \frac{1}{T_{com} + T_{conv}}$



### 7.5.1. I2C Communication Time

The minimum time to read the channel data in PENTRIG mode is :  $T_{com} = (8 + 16 \times N_{chan}) \times T_{SPI}$

The highest throughput will be obtained with a I2C frequency of 5MHz when the host read the channel data as quickly as possible after the NIRQ falling edge.

### 7.5.2. Conversion Time

The maximum possible throughput can be estimated with the following equation

$$T_{conv}(us) = 47 \cdot T_{osc} + N_{chan} \cdot (POWDLY + (N_{filt} - 1) \cdot SETDLY + (21N_{filt} + 1) \cdot T_{osc})$$

with:

- ◆  $N_{filt} = \{1, 3, 5, 7\}$  based on the order defined for the filter FILT (see Figure 4).
- ◆  $N_{chan} = \{1, 2, 3, 4, 5\}$  based on the number of channels defined in RegChanMsk
- ◆ POWDLY = 0.5us to 18.19ms, settling time as defined in RegCtrl0
- ◆ SETDLY = 0.5us to 18.19ms, settling time when filtering as defined in RegCtrl2
- ◆  $T_{osc}$  is the oscillator period (555ns +/- 15%)

Table 11 gives some examples of Coordinate Rate and Sample Rate for various setting in PENTRIG mode.

| Nch<br>[1..5] | Nfilt<br>[1 3 5 7] | PowDly<br>[uS] | SetDly<br>[uS] | Tconv<br>[uS] | Tcomm<br>[uS] | Total<br>[uS] | CR<br>[kCPS] | ECR<br>[kCPS] | SR<br>[kSPS] | ESR<br>[kSPS] |
|---------------|--------------------|----------------|----------------|---------------|---------------|---------------|--------------|---------------|--------------|---------------|
| 2.0           | 1.0                | 0.5            | 0.5            | 51.7          | 91.2          | 142.9         | 7.0          | 14.0          | 7.0          | 14.0          |
| 2.0           | 3.0                | 35.5           | 0.5            | 170.6         | 91.2          | 261.8         | 3.8          | 7.6           | 11.5         | 22.9          |
| 2.0           | 5.0                | 2.2            | 0.5            | 152.8         | 91.2          | 244.0         | 4.1          | 8.2           | 20.5         | 41.0          |
| 4.0           | 3.0                | 35.5           | 0.5            | 315.0         | 181.2         | 496.2         | 2.0          | 8.1           | 6.0          | 24.2          |

*Table 11 Coordinate throughput examples*

### 7.5.3. AUTO MODE

In AUTO mode, the coordinate throughput rate is the RATE set in RegCtrl0 if the host retrieve channel data at this RATE. The RATE set should be superior or equal to the CoordRate.

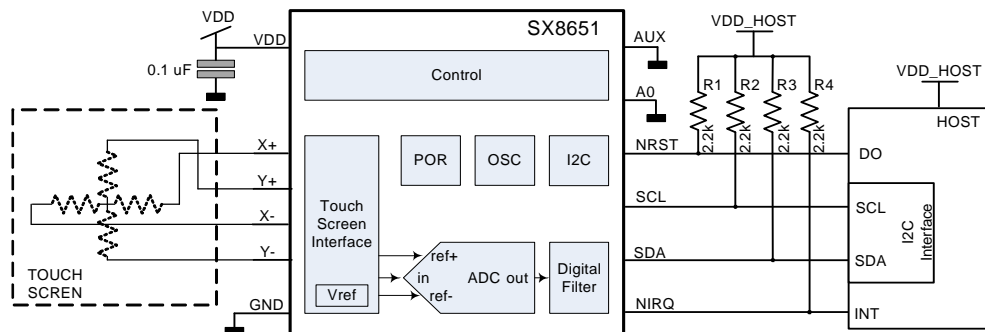
### 7.6. ESD event

In case of ESD event, the chip can reset to protect its internal circuitry. Polling a register may be used to check the chip reset event.

ESD event may trig the pen detection circuitry. In this case wrong data will be send to the host. To detect this false coordinates on 4-wire touchscreen, a pressure measurement can be done. When reading the values  $Z1 < 10$  and  $Z2 > 4070$ , the data may not be valid and indicate an ESDevent or a

## 7.7. Application Schematic

A typical application schematic is shown in Figure 35



*Figure 35. Typical application*

VDD\_HOST can be higher than VDD but must not exceed the maximum voltage of 3.7V.

The host GPIO D0 output is connected to the SX8650 NRST input to allows SX8650 hardware reset.

The host D0 may be a totem pole output. In this configuration and if the host and the SX8650 are supply with the same VDD, the R1 pull-up resistor is not required.

NIRQ pin is connected to a host interrupt pin. Once NIRQ event happens, the host read the data by a I2C read register.

## 7.8. Application Examples

### 7.8.1. Soft Keyboard



*Figure 36. Keyboard*

### 7.8.2. Slider Controls

A keyboard application can be designed with the help of the SX8650. The data are entered by tapping keys on the keyboard with a stylus. The SX8650 send the key coordinates to the microcontroller which interpret them as a symbol.

When the keyboard is not activated, the chip stays in low power mode to save power.

Every kind of controls such as rotative knob, slider, button could be emulated with a SX8650 associated to a touchscreen.

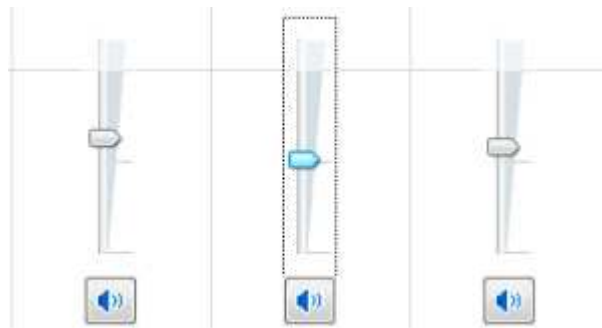


Figure 37. Slider controls

### 7.8.3. Game

Many kinds of game can be designed with touchscreen. With its high data throughput and its ability to sense pressure, SX8650 is the perfect controller for this kind of application.

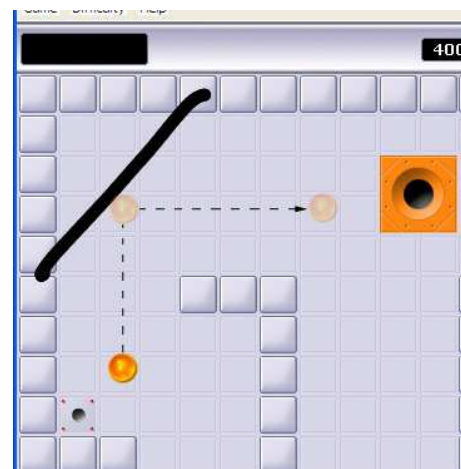
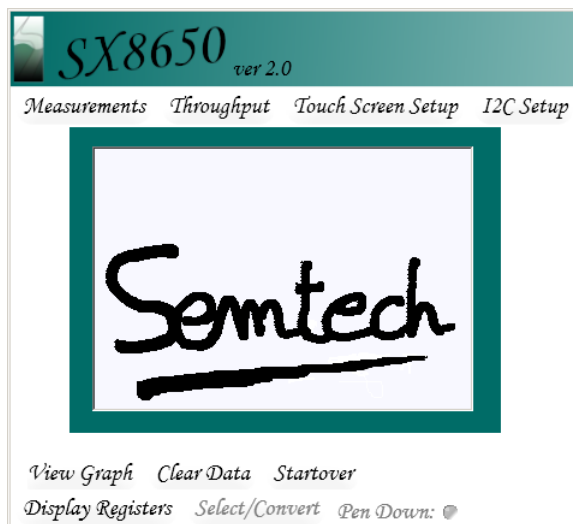


Figure 38. Game

### 7.8.4. Handwriting Application

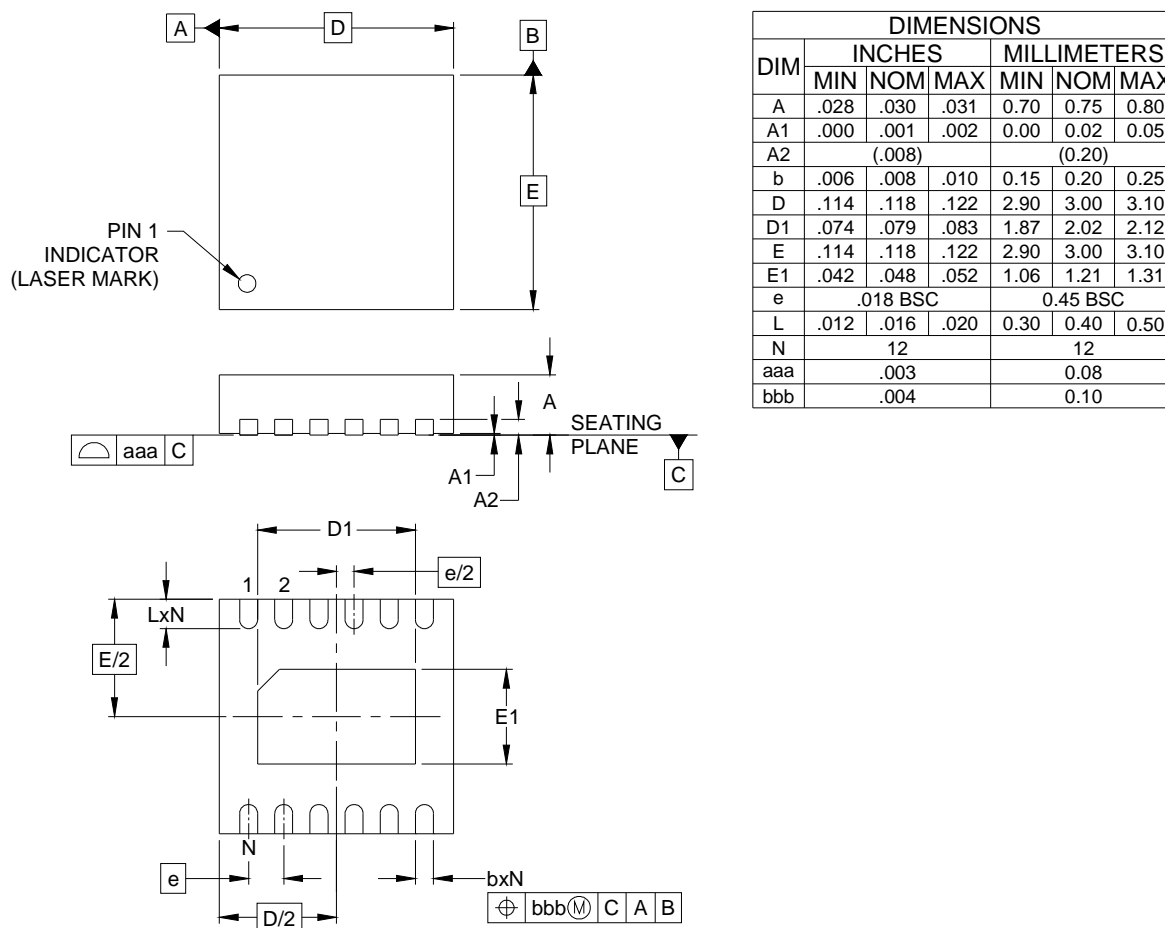


An handwriting application needs a powerful microcontroller to run recognition algorithms. The SX8650 includes a preprocessing block to reduce host activity.

Figure 39. Handwriting application

## 8. Packaging Information

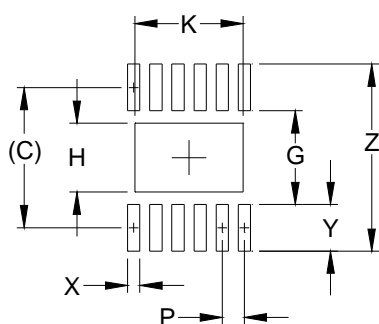
### 8.1. DFN Package



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS TERMINALS.

Figure 40. DFN Package Outline Drawing



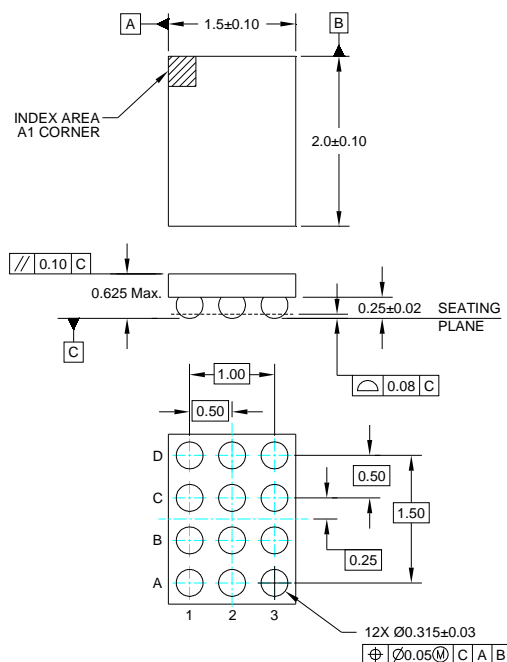
| DIMENSIONS |        |             |
|------------|--------|-------------|
| DIM        | INCHES | MILLIMETERS |
| C          | (.112) | (2.85)      |
| G          | .075   | 1.90        |
| H          | .055   | 1.40        |
| K          | .087   | 2.20        |
| P          | .018   | 0.45        |
| X          | .010   | 0.25        |
| Y          | .037   | 0.95        |
| Z          | .150   | 3.80        |

**NOTES:**

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

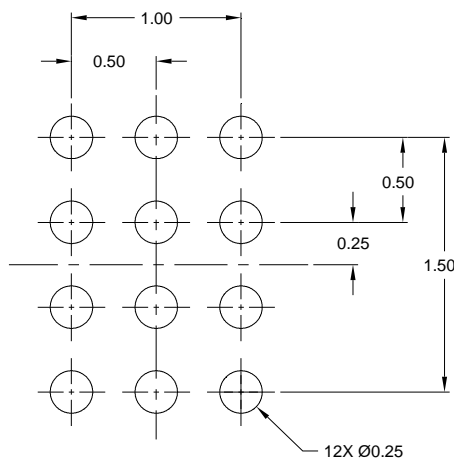
*Figure 41. DFN Package Land Pattern*

## 8.2. WLCSP Package


**NOTES:**

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS

*Figure 42. WLCSP Package Outline Drawing*


**NOTES:**

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*Figure 43. WLCSP Land Pattern*

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