SC4525F

# 18V, 3A, 350kHz Step-Down Switching Regulator

POWER MANAGEMENT

## Features

- Input Voltage Range: 3V to 18V
- 3A Output Current
- 350kHz Fixed Switching Frequency
- Precision 1V Feedback Voltage
- Peak Current-Mode Control
- Cycle-by-Cycle Current Limiting
- Hiccup Overload Protection with Frequency Foldback
- Soft-Start and Enable
- Thermal Shutdown
- Thermally Enhanced 8-pin SOIC Package
- Fully RoHS and WEEE Compliant

## Applications

- XDSL and Cable Modems
- Set Top Boxes
- Point of Load Applications
- CPE Equipment
- DSP Power Supplies
- LCD and Plasma TVs

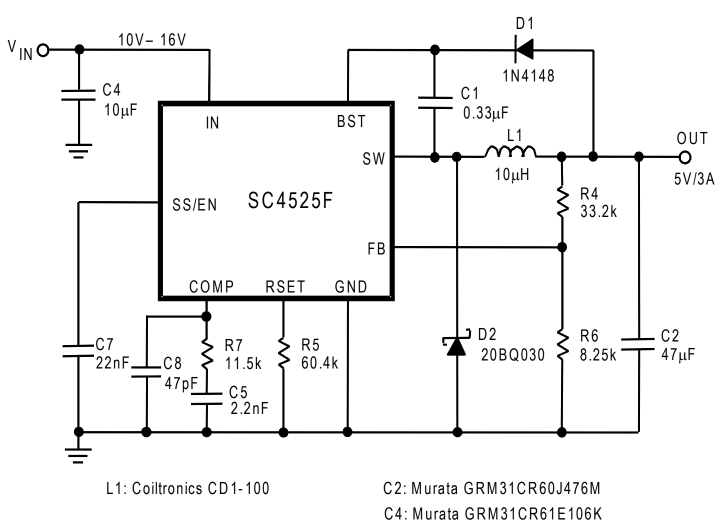
## Description

The SC4525F is a 350kHz constant frequency peak current-mode step-down switching regulator capable of producing 3A output current from an input ranging from 3V to 18V. The SC4525F is suitable for next generation XDSL modems, high-definition TVs and various point of load applications.

Peak current-mode PWM control employed in the SC4525F achieves fast transient response with simple loop compensation. Cycle-by-cycle current limiting and hiccup overload protection reduces power dissipation during output overload. Soft-start function reduces input start-up current and prevents the output from overshooting during power-up.

The SC4525F is available in SOIC-8 EDP package.

## Typical Application Circuit



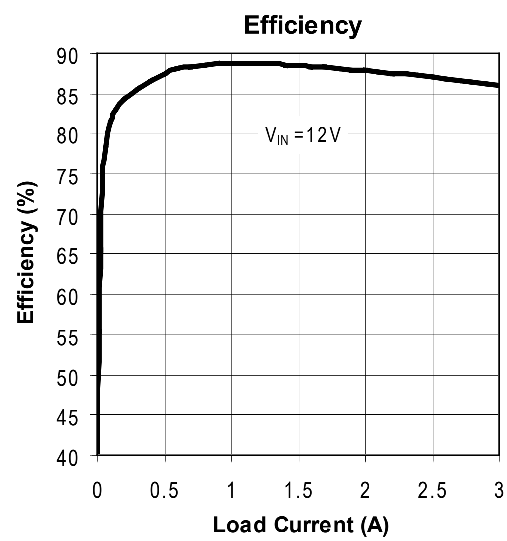
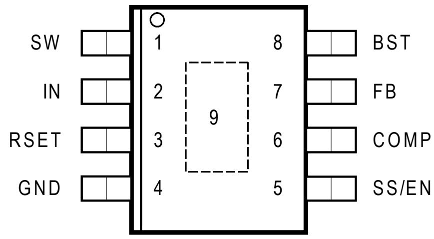




Figure 1 — 350kHz 10V - 16V to 5V/3A Step-down Converter

## Pin Configuration




(8 - Pin SOIC - EDP)

## Ordering Information

| Device | Package |
|---|---|
| SC4525FSETRT(1)(2) | SOIC-8 EDP |
| SC4525FEVB | Evaluation Board |

Notes:
(1) Available in tape and reel only. A reel contains 2,500 devices.
(2) Available in lead-free package only. Device is fully WEEE and RoHS compliant and halogen-free.

## Marking Information


yyww=Date code (Example: 0752)
xxxxx=Semtech Lot No. (Example: E9010)

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## Absolute Maximum Ratings

$V_{IN}$ Supply Voltage .................................. -0.3 to 24V

BST Voltage .................................................... 40V

BST Voltage above SW ........................................ 24V

SS Voltage .................................................-0.3 to 3V

FB Voltage ................................................ -0.3 to 7V

SW Voltage ............................................ -0.6 to $V_{IN}$

SW Transient Spikes (10ns Duration)......... -2.5V to $V_{IN}$ +1.5V

Peak IR Reflow Temperature ............................. 260°C

ESD Protection Level[2] .................................... 2000V

## Thermal Information

Junction to Ambient [1] .................................. 36°C/W

Junction to Case [1] ..................................... 5.5°C/W

Maximum Junction Temperature.......................... 150°C

Storage Temperature ............................ -65 to +150°C

Lead Temperature (Soldering) 10 sec ..................... 300°C

## Recommended Operating Conditions

Input Voltage Range ................................. 3V to 18V

Maximum Output Current .................................. 3A

Operating Ambient Temperature .............. -40 to +105°C

Operating Junction Temperature .............. -40 to +125°C

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES-

(1) Calculated from package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

(2) Tested according to JEDEC standard JESD22-A114-B.

## Electrical Characteristics

Unless otherwise noted, $V_{IN}$ = 12V, $V_{BST}$ = 15V, $V_{SS}$ = 2.2V, -40°C < $T_A$ = $T_J$ < 125°C, $R_{SET}$ = 60.4kΩ.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **Input Supply** | | | | | |
| Input Voltage Range | | 3 | | 18 | V |
| $V_{IN}$ Start Voltage | $V_{IN}$ Rising | 2.70 | 2.82 | 2.95 | V |
| $V_{IN}$ Start Hysteresis | | | 225 | | mV |
| $V_{IN}$ Quiescent Current | $V_{COMP}$ = 0 (Not Switching) | | 2 | 2.6 | mA |
| $V_{IN}$ Quiescent Current in Shutdown | $V_{SS/EN}$ = 0, $V_{IN}$ = 12V | | 40 | 52 | µA |
| **Error Amplifier** | | | | | |
| Feedback Voltage | | 0.980 | 1.000 | 1.020 | V |
| Feedback Voltage Line Regulation | $V_{IN}$ = 3V to 18V | | 0.005 | | %/V |
| FB Pin Input Bias Current | $V_{FB}$ = 1V, $V_{COMP}$ = 0.8V | | -170 | -340 | nA |
| Error Amplifier Transconductance | | | 300 | | $\mu\Omega^{-1}$ |
| Error Amplifier Open-loop Gain | | | 60 | | dB |
| COMP Pin to Switch Current Gain | | | 15.2 | | A/V |
| COMP Maximum Voltage | $V_{FB}$ = 0.9V | | 2.35 | | V |
| COMP Source Current | $V_{FB}$ = 0.8V, $V_{COMP}$ = 0.8V | | 17 | | µA |
| COMP Sink Current | $V_{FB}$ = 1.2V, $V_{COMP}$ = 0.8V | | 25 | | |
| **Internal Power Switch** | | | | | |
| Switch Current Limit | (Note 1) | 3.9 | 5.1 | 6.6 | A |
| Switch Saturation Voltage | $I_{SW}$ = -3.9A | | 380 | 600 | mV |

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## Electrical Characteristics (Cont.)

Unless otherwise noted, $V_{IN}$ = 12V, $V_{BST}$ = 15V, $V_{SS}$ = 2.2V, -40°C < $T_A$ = $T_J$ < 125°C, $R_{SET}$ = 60.4kΩ.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Minimum Switch On-time | $V_{IN}$ = 10 V, $R_{SW}$ = 10Ω | 70 | 120 | 230 | ns |
| Minimum Switch Off-time | $V_{IN}$ = 6 V, $R_{SW}$ = 6Ω | 30 | 75 | 130 | ns |
| Switch Leakage Current | | | | 10 | µA |
| Minimum Bootstrap Voltage | $I_{SW}$ = -3.9A | | 1.8 | 2.3 | V |
| BST Pin Current | $I_{SW}$ = -3.9A | | 100 | 150 | mA |
| **Oscillator** | | | | | |
| Switching Frequency | $R_{SET}$ = 60.4kΩ | 275 | 350 | 425 | kHz |
| Foldback Frequency | $R_{SET}$ = 60.4kΩ, $V_{FB}$ = 0 | 35 | 65 | 100 | kHz |
| **Soft Start and Overload Protection** | | | | | |
| SS/EN Shutdown Threshold | | 0.2 | 0.3 | 0.4 | V |
| SS/EN Switching Threshold | $V_{FB}$ = 0 V | 0.95 | 1.2 | 1.4 | V |
| Soft-start Charging Current | $V_{SS/EN}$ = 0 V | | 1.9 | | µA |
| | $V_{SS/EN}$ = 1.5 V | 1.6 | 2.4 | 3.2 | |
| Soft-start Discharging Current | | | 1.5 | | µA |
| Hiccup Arming SS/EN Voltage | $V_{SS/EN}$ Rising | | 2.15 | | V |
| Hiccup SS/EN Overload Threshold | $V_{SS/EN}$ Falling | | 1.9 | | V |
| Hiccup Retry SS/EN Voltage | $V_{SS/EN}$ Falling | 0.6 | 1.0 | 1.2 | V |
| **Over Temperature Protection** | | | | | |
| Thermal Shutdown Temperature | | | 165 | | °C |
| Thermal Shutdown Hysteresis | | | 10 | | °C |

Note 1: Switch current limit does not vary with duty cycle.

## Pin Descriptions

| SO-8 | Pin Name | Pin Function |
|---|---|---|
| 1 | SW | Emitter of the internal NPN power transistor. Connect this pin to the inductor, the freewheeling diode and the bootstrap capacitor. |
| 2 | IN | Power supply to the regulator. It is also the collector of the internal NPN power transistor. It must be closely by-passed to the ground plane with a capacitor. |
| 3 | RSET | Connect a 60.4kΩ resistor from this pin to ground. |
| 4 | GND | Ground pin |
| 5 | SS/EN | Soft-start and regulator enable pin. A capacitor from this pin to ground provides soft-start and overload hiccup functions. Hiccup can be disabled by overcoming the internal soft-start discharging current with an external pull-up resistor connected between the SS/EN and the IN pins. Pulling the SS/EN pin below 0.2V completely shuts off the regulator to low current state. |
| 6 | COMP | The output of the internal error amplifier. The voltage at this pin controls the peak switch current. A RC compensa-tion network at this pin stabilizes the regulator. |
| 7 | FB | The inverting input of the error amplifier. If $V_{FB}$ falls below 0.8V, then the switching frequency will be reduced to improve short-circuit robustness (see Applications Information for details). |
| 8 | BST | Supply pin to the power transistor driver. Tie to an external diode-capacitor bootstrap circuit to generate drive voltage higher than $V_{IN}$ in order to fully enhance the internal NPN power transistor. |
| 9 | Exposed Pad | The exposed pad serves as a thermal contact to the circuit board. While the exposed pad is electrically isolated, it is suggested to be soldered to the ground plane of the PC board. |

## Block Diagram

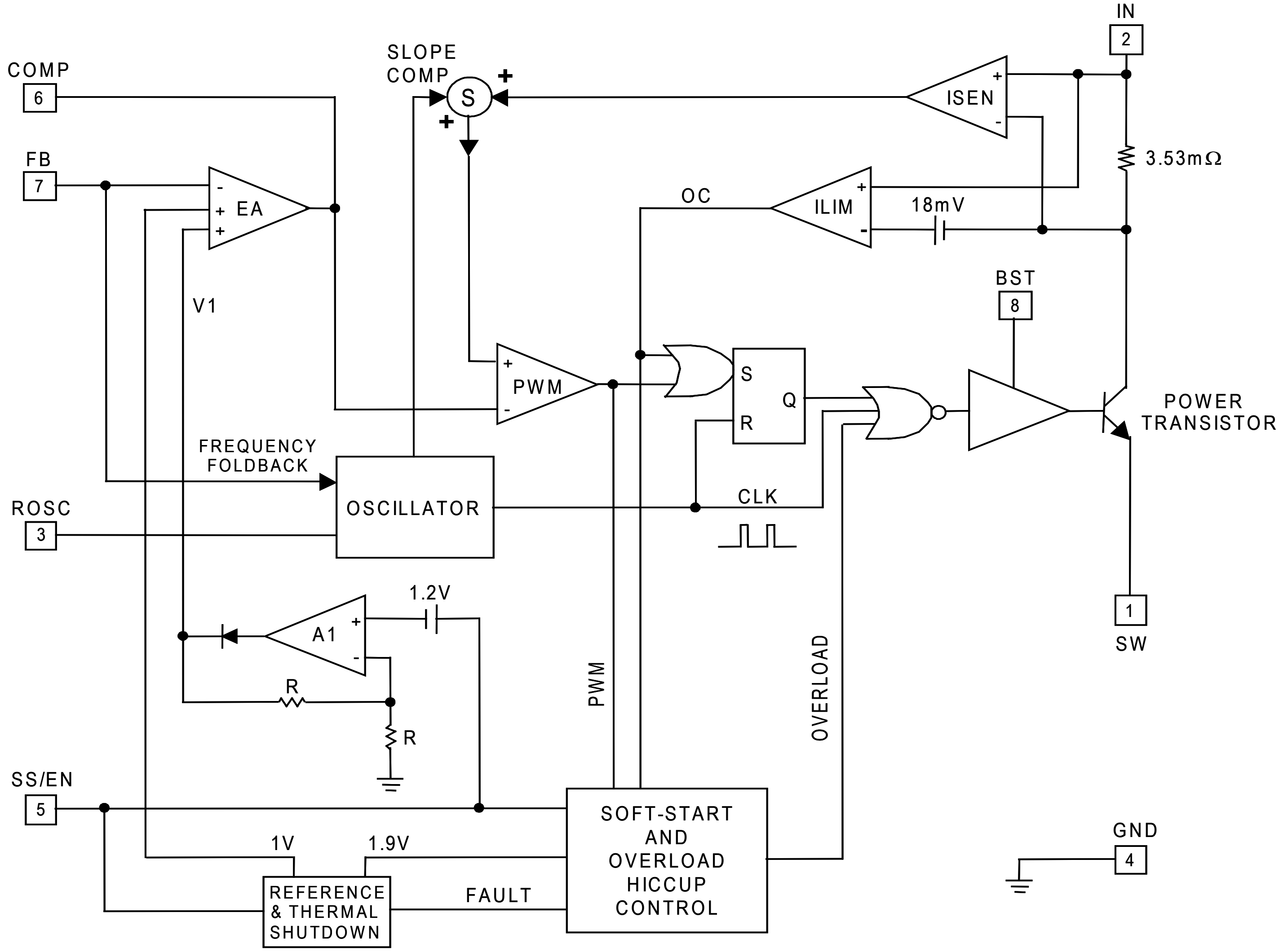


Figure 2 — SC4525F Block Diagram

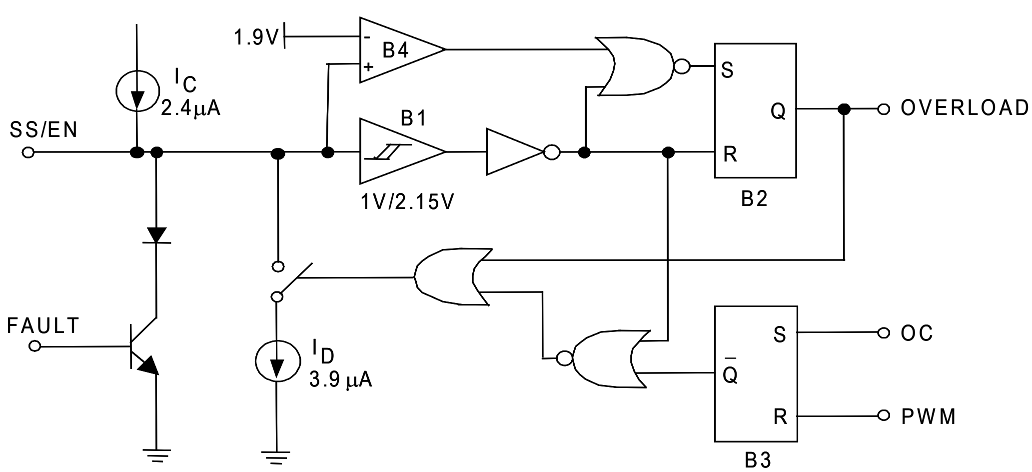


Figure 3 — Soft-start and Overload Hiccup Control Circuit

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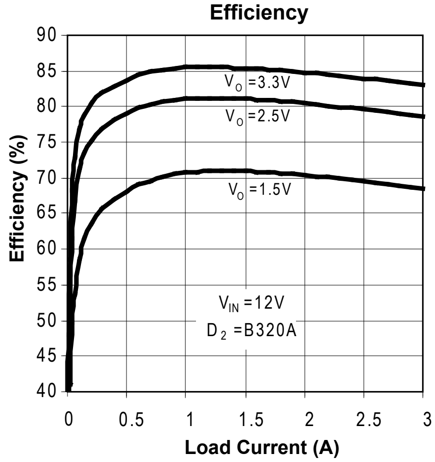
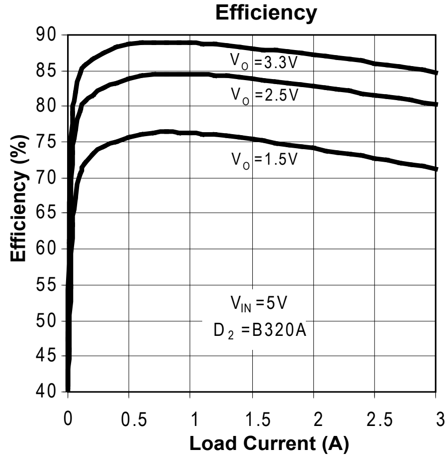
## Typical Characteristics

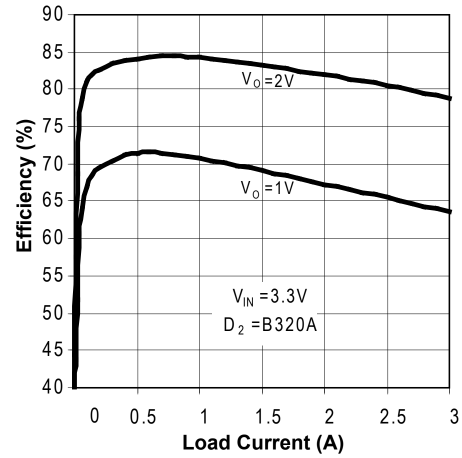
Efficiency



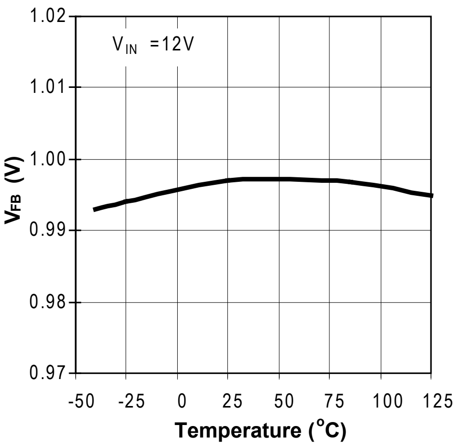

Efficiency



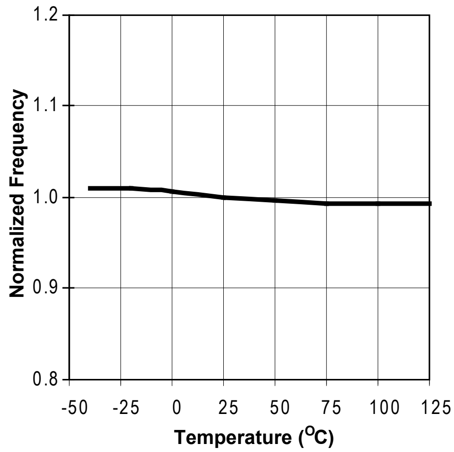

Efficiency



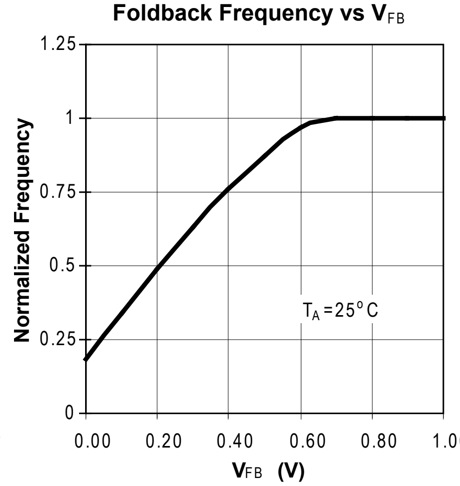

Feedback Voltage vs Temperature



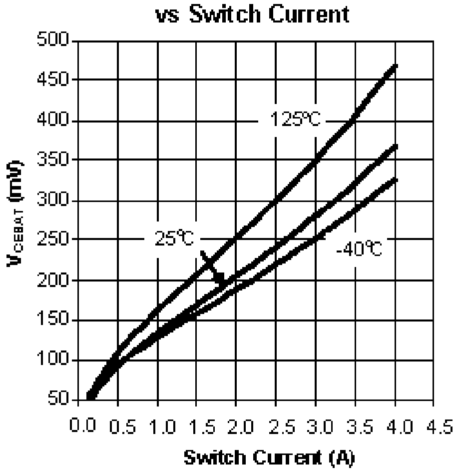

Frequency vs Temperature



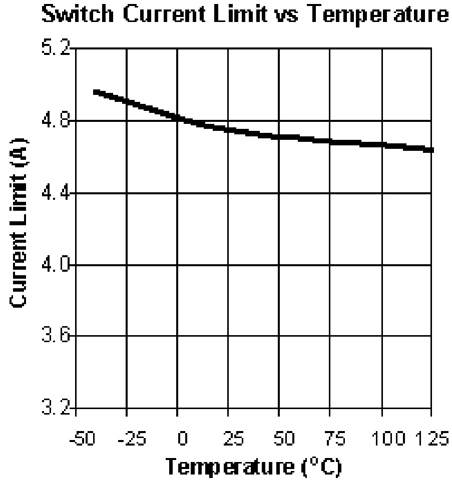

Foldback Frequency vs $V_{FB}$



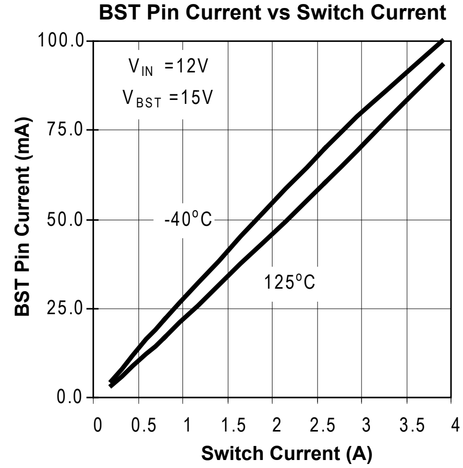

Switch Saturation Voltage vs Switch Current



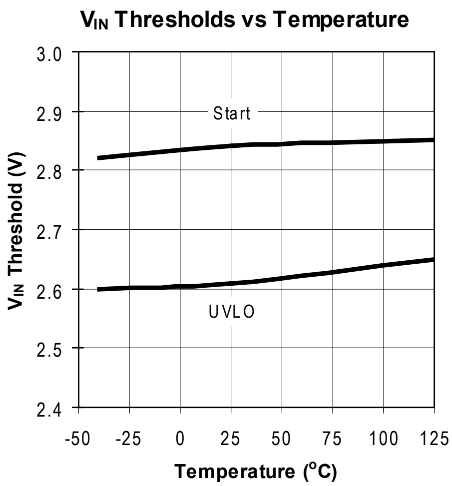

Switch Current Limit vs Temperature

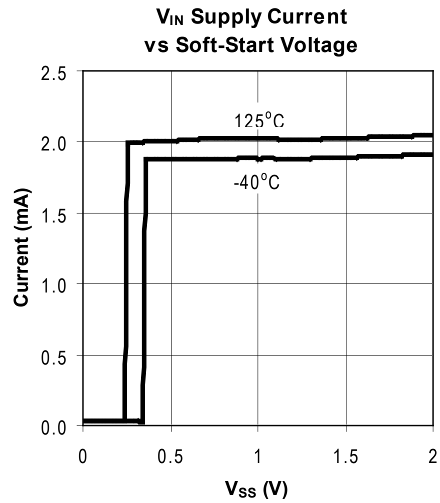


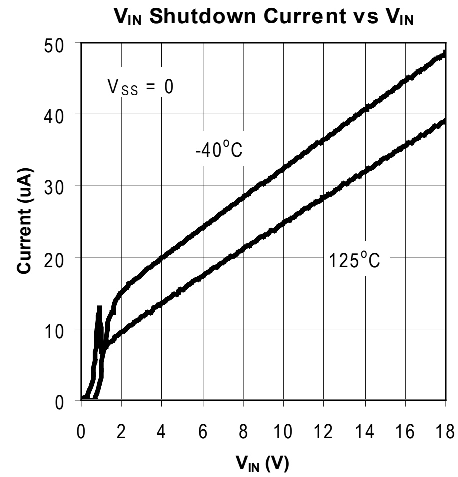

BST Pin Current vs Switch Current

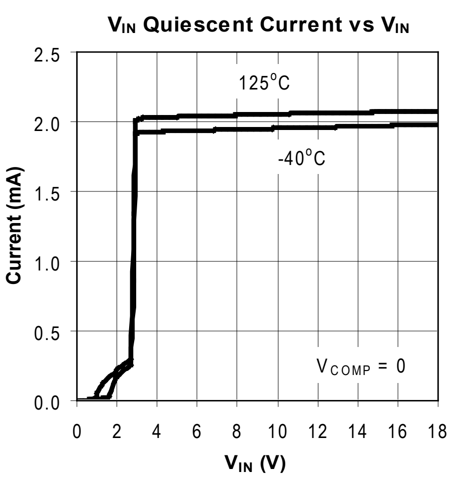


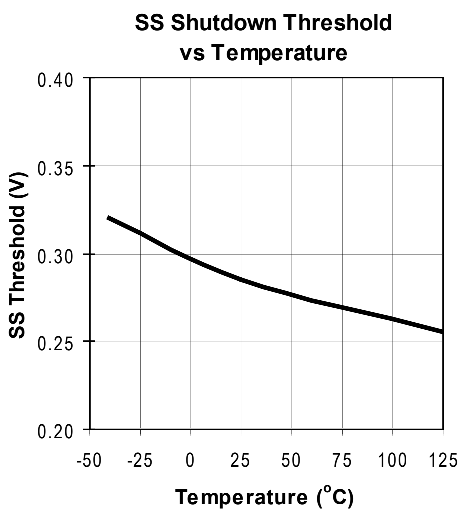
## Typical Characteristics (Cont.)

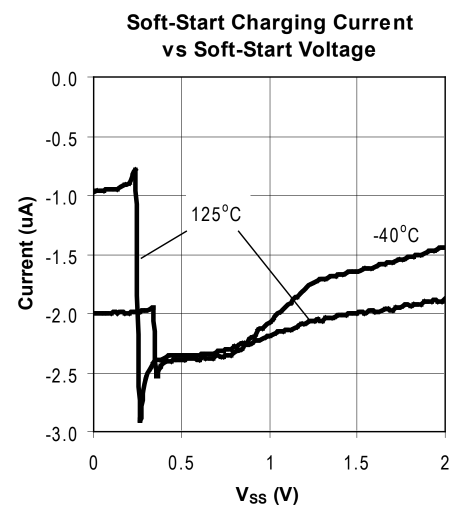


## Applications Information

### Operation

The SC4525F is a 350kHz fixed frequency, peak current-mode, step-down switching regulator with an integrated 3.9A power NPN transistor. With the peak current-mode control, the double reactive poles of the output LC filter are reduced to a single real pole by the inner current loop. This simplifies loop compensation and achieves fast transient response with a simple Type-2 compensation network.

As shown in Figure 2, the switch collector current is sensed with an integrated 3.53mΩ sense resistor. The sensed current is summed with a slope-compensating ramp before it is compared with the transconductance error amplifier (EA) output. The PWM comparator trip point determines the switch turn-on pulse width. The current-limit comparator ILIM turns off the power switch when the sensed signal exceeds the 18mV current-limit threshold.

Driving the base of the power transistor above the input power supply rail minimizes the power transistor saturation voltage and maximizes efficiency. An external bootstrap circuit (formed by the capacitor $C_1$ and the diode $D_1$ in Figure 1) generates such a voltage at the BST pin for driving the power transistor.

### Shutdown and Soft-Start

The SS/EN pin is a multiple-function pin. An external capacitor (4.7nF to 22nF) connected from the SS pin to ground sets the soft-start and overload shutoff times of the regulator (Figure 3). The effect of $V_{SS/EN}$ on the SC4525F is summarized in Table 1.

**Table 1: SS/EN operation modes**

| SS/EN | Mode | Supply Current |
|---|---|---|
| <0.2V | Shutdown | 18uA @ 5Vin |
| 0.4V to 1.2V | Not switching | 2mA |
| 1.2V to 2.15V | Switching & hiccup disabled | Load dependent |
| >2.15V | Switching & hiccup armed | |

Pulling the SS/EN pin below 0.2V shuts off the regulator and reduces the input supply current to 18µA ($V_{IN}$ = 5V). When the SS/EN pin is released, the soft-start capacitor is charged with an internal 1.9µA current source (not shown in Figure 3). As the SS/EN voltage exceeds 0.4V, the internal bias circuit of the SC4525F turns on and the SC4525F draws 2mA from $V_{IN}$. The 1.9µA charging current turns off and the 2.4µA current source $I_C$ in Figure 3 slowly charges the soft-start capacitor.

The error amplifier EA in Figure 2 has two non-inverting inputs. The non-inverting input with the lower voltage predominates. One of the non-inverting inputs is biased to a precision 1V reference and the other non-inverting input is tied to the output of the amplifier $A_1$. Amplifier $A_1$ produces an output $V_1 = 2(V_{SS/EN} - 1.2V)$. $V_1$ is zero and COMP is forced low when $V_{SS/EN}$ is below 1.2V. During start up, the effective non-inverting input of EA stays at zero until the soft-start capacitor is charged above 1.2V. Once $V_{SS/EN}$ exceeds 1.2V, COMP is released. The regulator starts to switch when $V_{COMP}$ rises above 0.4V. If the soft-start interval is made sufficiently long, then the FB voltage (hence the output voltage) will track $V_1$ during start up. $V_{SS/EN}$ must be at least 1.83V for the output to achieve regulation. Proper soft-start prevents output overshoot. Current drawn from the input supply is also well controlled.

### Overload / Short-Circuit Protection

Table 2 lists various fault conditions and their corresponding protection schemes in the SC4525F.

**Table 2: Fault conditions and protections**

| Condition | Cause of Fault | Protective Action |
|---|---|---|
| IL>ILimit, $V_{FB}$>0.8V | Over current | Cycle-by-cycle limit at programmed frequency |
| IL>ILimit, $V_{FB}$<0.8V | Over current | Cycle-by-cycle limit with frequency foldback |
| VSS/EN Falling SS/EN<1.9V | Persistent over current or short circuit | Shutdown, then retry (Hiccup) |
| Tj>160C | Over temperature | Shutdown |

As summarized in Table 1, overload shutdown is disabled during soft-start ($V_{SS/EN}$<2.15V). In Figure 3, the reset input of the overload latch $B_2$ will remain high if the SS/EN voltage is below 2.15V. Once the soft-start capacitor is charged above 2.15V, the output of the Schmitt trigger $B_1$ goes high, the reset input of $B_2$ goes low and hiccup becomes armed. As the load draws more current from the regulator, the current-limit comparator ILIM (Figure 2) will eventually limit the switch current on a cycle-by-cycle basis. The over-current signal OC goes high, setting

## Applications Information (Cont.)

the latch $B_3$. The soft-start capacitor is discharged with ($I_D$ - $I_C$) (Figure 3). If the inductor current falls below the current limit and the PWM comparator instead turns off the switch, then latch $B_3$ will be reset and $I_C$ will recharge the soft-start capacitor. If over-current condition persists or OC becomes asserted more often than PWM over a period of time, then the soft-start capacitor will be discharged below 1.9V. At this juncture, comparator $B_4$ sets the overload latch $B_2$. The soft-start capacitor will be continuously discharged with ($I_D$ - $I_C$). The COMP pin is immediately pulled to ground. The switching regulator is shut off until the soft-start capacitor is discharged below 1.0V. At this moment, the overload latch is reset. The soft-start capacitor is recharged and the converter again undergoes soft-start. The regulator will go through soft-start, overload shutdown and restart until it is no longer overloaded.

If the FB voltage falls below 0.8V because of output overload, then the switching frequency will be reduced. Frequency foldback helps to limit the inductor current when the output is hard shorted to ground.

During normal operation, the soft-start capacitor is charged to 2.4V.

### Setting the Output Voltage

The regulator output voltage, $V_O$, is set with an external resistive divider (Figure 1) with its center tap tied to the FB pin. For a given $R_6$ value, $R_4$ can be found by

$$R_4 = R_6\left(\frac{V_O}{1.0V} - 1\right)$$

### Minimum On Time Consideration

The operating duty cycle of a non-synchronous step-down switching regulator in continuous-conduction mode (CCM) is given by

$$D = \frac{V_O + V_D}{V_{IN} + V_D - V_{CESAT}}$$

where $V_{IN}$ is the input voltage, $V_{CESAT}$ is the switch saturation voltage, and $V_D$ is voltage drop across the rectifying diode.

In peak current-mode control, the PWM modulating ramp is the sensed current ramp of the power switch. This current ramp is absent unless the switch is turned on. The intersection of this ramp with the output of the voltage feedback error amplifier determines the switch pulse width. The propagation delay time required to immediately turn off the switch after it is turned on is the minimum controllable switch on time ($T_{ON(MIN)}$).

Closed-loop measurement shows that the SC4525F minimum on time is about 120ns at room temperature for 1A load current (Figure 4). If the required switch on time is shorter than the minimum on time, the regulator will either skip cycles or it will jitter.

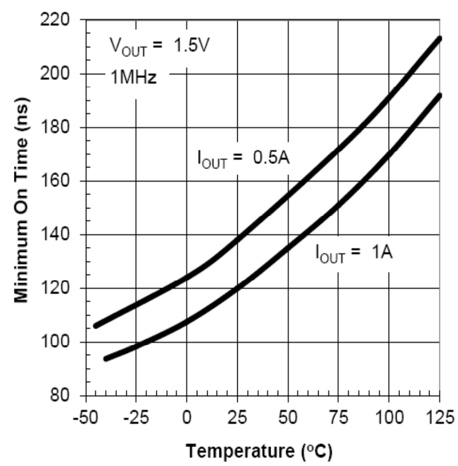



**Figure 4. Variation of Minimum On Time with Ambient Temperature**

To allow for transient headroom, the minimum operating switch on time should be at least 20% to 30% higher than the worst-case minimum on time.

### Minimum Off Time Limitation

The PWM latch in Figure 2 is reset every cycle by the clock. The clock also turns off the power transistor to refresh the bootstrap capacitor. This minimum off time limits the attainable duty cycle of the regulator at a given switching frequency. The measured minimum off time is 138ns typically. If the required duty cycle is higher than the attainable maximum, then the output voltage will not be able to reach its set value in continuous-conduction mode.

## Applications Information (Cont.)

### Inductor Selection

The inductor ripple current for a non-synchronous step-down converter in continuous-conduction mode is

$$\Delta I_L = \frac{(V_O + V_D)\cdot(1-D)}{F_{SW}\cdot L_1}$$

where $F_{SW}$ is the switching frequency (350kHz) and $L_1$ is the inductance.

An inductor ripple current between 20% to 50% of the maximum load current, $I_O$, gives a good compromise among efficiency, cost and size. Re-arranging the previous euqation and assuming 35% inductor ripple current, the inductor is given by

$$L_1 = \frac{(V_O + V_D)\cdot(1-D)}{35\%\cdot I_O\cdot F_{SW}}$$

If the input voltage varies over a wide range, then choose $L_1$ based on the nominal input voltage. Always verify converter operation at the input voltage extremes.

The peak current limit of SC4525F power transistor is at least 3.9A. The maximum deliverable load current for the SC4525F is 3.9A minus one half of the inductor ripple current.

### Input Decoupling Capacitor

The input capacitor should be chosen to handle the RMS ripple current of a buck converter. This value is given by

$$I_{RMS\_CIN} = I_O\cdot\sqrt{D\cdot(1-D)}$$

The input capacitance must also be high enough to keep input ripple voltage within specification. This is important in reducing the conductive EMI from the regulator. The input capacitance can be estimated from

$$C_{IN} > \frac{I_O}{4\cdot\Delta V_{IN}\cdot F_{SW}}$$

where $\Delta V_{IN}$ is the allowable input ripple voltage.
Multi-layer ceramic capacitors, which have very low ESR (a few mΩ) and can easily handle high RMS ripple current, are the ideal choice for input filtering. A single 4.7μF to 10μF X5R ceramic capacitor is adequate for most applications. For high voltage applications, a small ceramic (1μF or 2.2μF) can be placed in parallel with a low ESR electrolytic capacitor to satisfy both the ESR and bulk capacitance requirements.

### Output Capacitor

The output ripple voltage $\Delta V_O$ of a buck converter can be expressed as

$$\Delta V_O = \Delta I_L\cdot\left(ESR + \frac{1}{8\cdot F_{SW}\cdot C_O}\right)$$

where $C_O$ is the output capacitance.

Since the inductor ripple current $\Delta I_L$ increases as D decreases (refer to the first equation in the Inductor Selection section), the output ripple voltage is therefore the highest when $V_{IN}$ is at its maximum.

A 22μF to 47μF X5R ceramic capacitor is found adequate for output filtering in most applications. Ripple current in the output capacitor is not a concern because the inductor current of a buck converter directly feeds $C_O$, resulting in very low ripple current. Avoid using Z5U and Y5V ceramic capacitors for output filtering because these types of capacitors have high temperature and high voltage coefficients.

### Freewheeling Diode

Use of Schottky barrier diodes as freewheeling rectifiers reduces diode reverse recovery input current spikes, easing high-side current sensing in the SC4525F. These diodes should have an average forward current rating at least 3A and a reverse blocking voltage of at least a few volts higher than the input voltage. For switching regulators operating at low duty cycles (i.e. low output voltage to input voltage conversion ratios), it is beneficial to use freewheeling diodes with somewhat higher average current ratings (thus lower forward voltages). This is because the diode conduction interval is much longer than that of the transistor. Converter efficiency will be improved if the voltage drop across the diode is lower.

The 20BQ030 (International Rectifier), B320A, B330A (Diodes Inc.), SS33 (Vishay), CMSH3-20MA and CMSH3-40MA (Central-Semi.) are all suitable.

The freewheeling diode should be placed close to the SW pin of the SC4525F on the PCB to minimize ringing due to trace inductance.

## Applications Information (Cont.)

### Bootstrapping the Power Transistor

To maximize efficiency, the turn-on voltage across the internal power NPN transistors should be minimized. If these transistors are to be driven into saturation, then their bases will have to be driven from a power supply higher in voltage than $V_{IN}$. The required driver supply voltage (at least 2.3V higher than the SW voltage) is generated with a bootstrap circuit (the diode $D_1$ and the capacitor $C_1$ in Figure 6). The bootstrapped output (the common node between $D_1$ and $C_1$) is connected to the BST pin of the SC4525F.

The minimum BST to SW voltage required to fully saturate the power transistor is shown in Figure 5. The minimum required $V_{C1}$ increases as temperature decreases. The bootstrap circuit reaches equilibrium when the base charge drawn from $C_1$ during transistor on time is equal to the charge replenished during the off interval.

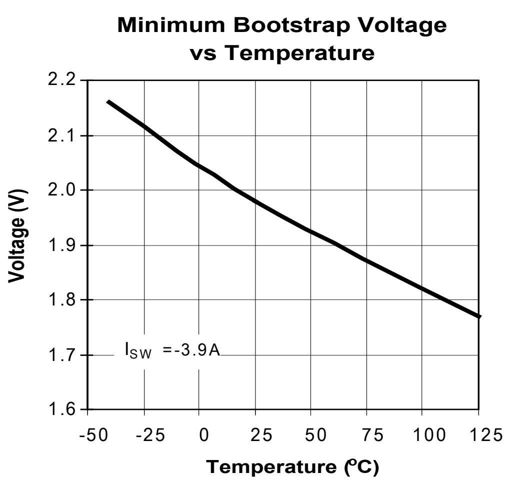



**Figure 5. Typical Minimum Bootstrap Voltage required to Saturate the Transistor ($I_{SW}$= -3.9A)**

Figure 6 summarizes various ways of bootstrapping the SC4525F. A fast switching PN diode (such as 1N4148 or 1N914) and a small (0.33µF – 0.47µF) ceramic capacitor can be used.

In Figure 6(a) the power switch is bootstrapped from the output. This is the most efficient configuration and it also results in the least voltage stress at the BST pin. The maximum BST pin voltage is about $V_{IN} + V_{OUT}$. The minimum $V_{OUT}$ required for this bootstrap configuration is 2.5V. If the output voltage is between 2.5V and 3V, then use a small Schottky diode (such as BAT54) for $D_1$ to maximize the bootstrap voltage.

The SC4525F can also be bootstrapped from the input [Figure 6(b)]. This configuration is not as efficient as Figure 6(a). However this may be the only option if the output voltage is less than 2.5V and there is no other supply with voltage higher than 2.5V. Voltage stress at the BST pin can be somewhat higher than $2V_{IN}$.

Figures 6(c) and (d) show how to bootstrap the SC4525F from a second independent power supply $V_S$.

The minimum bootstrap capacitance $C_1$ can be estimated as:

$$C_1 > \frac{I_{OUT(MAX)} \cdot D}{10 \cdot f \cdot (V_S - 2.4)}$$

where $V_S$ is the voltage applied to the anode of $D_1$.

The inductor current charges the bootstrap capacitor when it pulls the SW node low during the switch off time. If $D_1$ is connected to the converter input, then $C_1$ will be charged as soon as $V_{IN}$ is applied.

If the bootstrap diode is tied to the converter output [Fig ures 6(a)], then $C_1$ can only be charged from the regulator output through the inductor. Before the converter starts, there is no output voltage or inductor current. Hence it is necessary for the regulator to deliver some inductor current to the output before $C_1$ can be charged. If $V_{IN}$ is not much higher than the programmed $V_{OUT}$ and it ramps up very slowly, then the inductor current will not be high enough for the bootstrap circuit to run, especially at light loads. In order to have some inductor current to charge $C_1$, the converter output needs to be loaded or $V_{IN}$ needs to be increased. Using larger soft-start capacitor $C_{SS}$ will also help in starting bootstrap because there will be current in the inductor over a longer period of time. Figures 7(a) and 7(b) show the minimum input voltage required to start bootstrap and to run before dropping out as a function of the load current. The minimum start-up $V_{IN}$ decreases with higher $dV_{IN}/dt$ or larger soft-start capacitor $C_{SS}$. The lines labeled “dropout” in these graphs show that once started, the bootstrap circuit is able to sustain itself down to zero load.

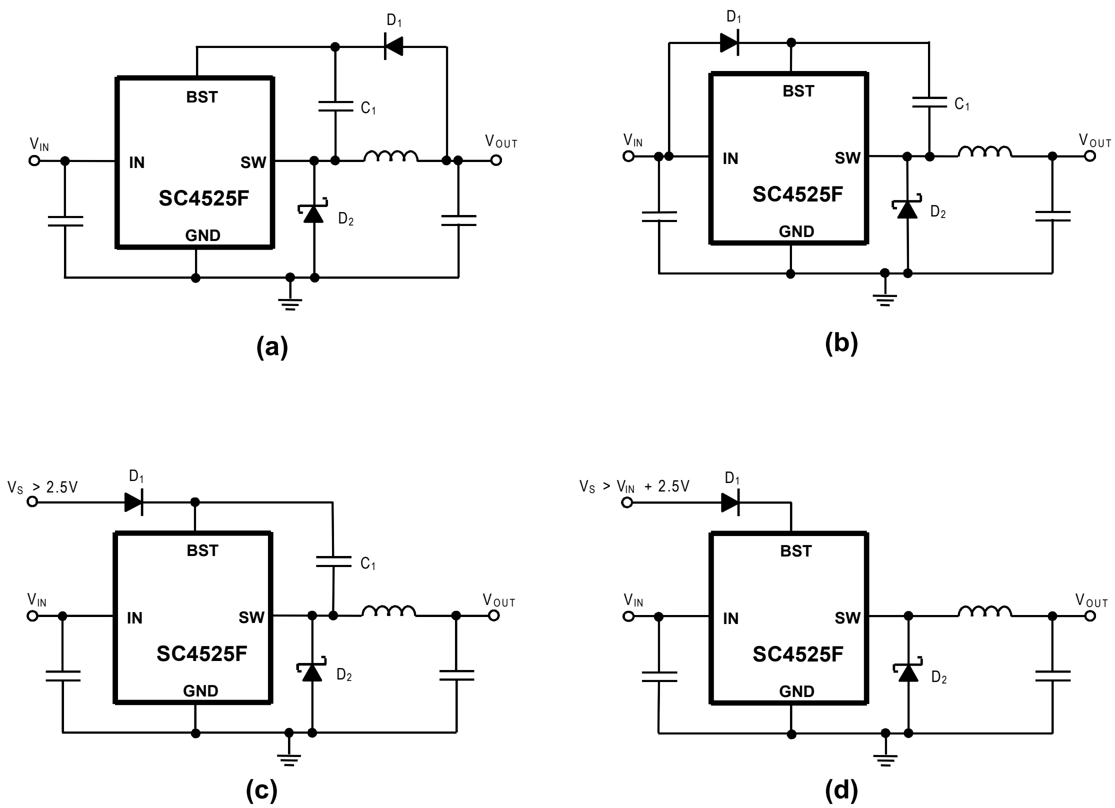



Figure 6(a)-(d). Methods of Bootstrapping the SC4525F

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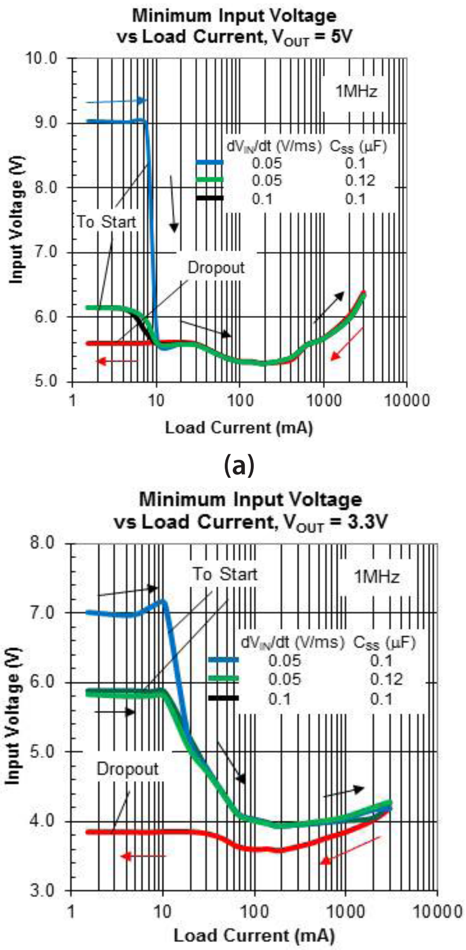
## Applications Information (Cont.)




(b)

**Figure 7. The Minimum Input Voltage to Start and to Run Before Dropout. The Regulator is Bootstrapped from its Output [Figure 6(a)]. $D_1$ is 1N4148. (a) $V_{OUT}$ = 5V (b) $V_{OUT}$ = 3.3V**

### Minimum Soft-start Capacitance Css

To ensure normal operation, the minimum soft-start capacitance $C_{SS}$ can be calculated in terms of the output capacitance $C_O$ and output load current $I_O$ according to the following equations.

$$\frac{dV_{SS}}{dt} = \frac{I_{SS}}{C_{SS}}$$

$$\frac{dV_0}{dt} = \frac{dV_1}{dt} = \frac{d}{dt}\left[2\left(V_{SS} - 1.2V\right)\right]$$

Substituting the first equation into the second equation,

$$\frac{dV_0}{dt} = \frac{2I_{SS}}{C_{SS}}$$

where $V_{SS}$ is the soft-start capacitor voltage and $I_{SS}$ is the soft-start charging current. $V_1$ is the voltage defined in Figure 2.

To ensure successful startup, the total current drawn from the output must be less than the maximum output capability of the part,

$$\frac{V_0}{R} + C_0 \times \frac{dV_0}{dt} \le 3.5A$$

Substituting the third equation of this section into the previous equation,

$$\frac{V_0}{R} + 2I_{SS} \times \frac{C_0}{C_{SS}} \le 3.5A$$

Rearranging,

$$C_{SS} \ge \frac{2I_{SS(MAX)} \times C_0}{3.5A - \left(\frac{V_0}{R}\right)}$$

Therefore the minimum $C_{SS}$ depends on the output capacitance and the load current. Larger $C_{SS}$ is necessary when starting into a heavy load (small R).

If the regulator is to be started by turning on a bench power supply, then $C_{SS}$ will be best determined empirically because the rise time of a power supply can range from a few milliseconds to a few hundred milliseconds. With the maximum load applied, the output rise is observed using a 22nF for $C_{SS}$. Adjust $C_{SS}$ until a linear $V_{OUT}$ ramp is achieved.

### Loop Compensation

The goal of compensation is to shape the frequency response of the converter so as to achieve high DC accuracy and fast transient response while maintaining loop stability.

## Applications Information (Cont.)

The block diagram in Figure 8 shows the control loops of a buck converter with the SC4525F. The inner loop (current loop) consists of a current sensing resistor ($R_s$=3.53mΩ) and a current amplifier (CA) with gain ($G_{CA}$=18.5). The outer loop (voltage loop) consists of an error amplifier (EA), a PWM modulator, and a LC filter.

Since the current loop is internally closed, the remaining task for the loop compensation is to design the voltage compensator ($C_5$, $R_7$, and $C_8$).

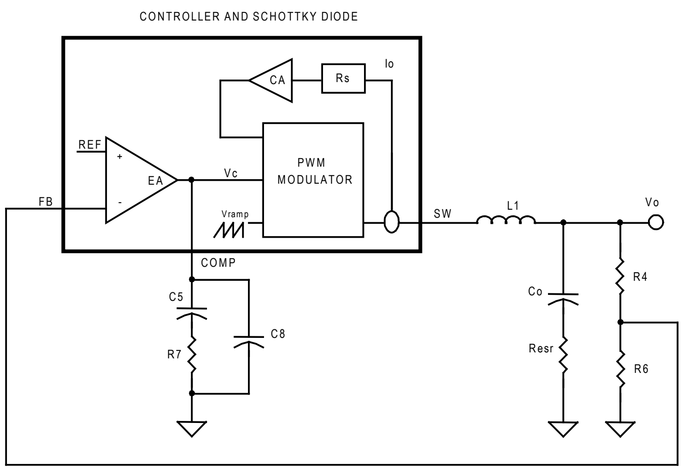



**Figure 8 — Block diagram of control loops**

For a converter with switching frequency $F_{SW}$, output inductance $L_1$, output capacitance $C_O$ and loading R, the control ($V_C$) to output ($V_O$) transfer function in Figure 8 is given by:

$$\frac{V_O}{V_C} = \frac{G_{PWM}(1+sR_{ESR}C_O)}{(1+s/\omega_p)(1+s/\omega_n Q+s^2/\omega_n^2)}$$

This transfer function has a finite DC gain

$$G_{PWM} \approx \frac{R}{G_{CA} \times R_S}$$

an ESR zero $F_Z$ at

$$\omega_Z = \frac{1}{R_{ESR}C_O}$$

It has a dominant low-frequency pole $F_P$ at

$$\omega_p \approx \frac{1}{RC_O}$$

and double poles at half the switching frequency.

Including the voltage divider ($R_4$ and $R_6$), the control to feedback transfer function is found and plotted in Figure 9 as the converter gain.

Since the converter gain has only one dominant pole at low frequency, a simple Type-2 compensation network is sufficient for voltage loop compensation. As shown in Figure 9, the voltage compensator has a low frequency integrator pole, a zero at $F_{Z1}$, and a high frequency pole at $F_{P1}$. The integrator is used to boost the gain at low frequency. The zero is introduced to compensate the excessive phase lag at the loop gain crossover due to the integrator pole (-90deg) and the dominant pole (-90deg). The high frequency pole nulls the ESR zero and attenuates high frequency noise.

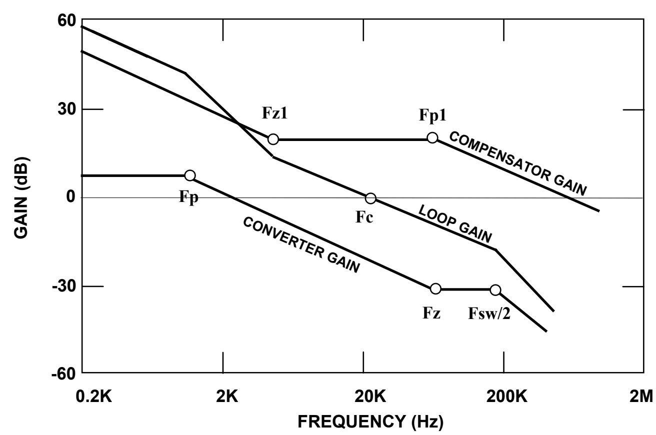



**Figure 9 — Bode plots for voltage loop design**

Therefore, the procedure of the voltage loop design for the SC4525F can be summarized as:

1. Plot the converter gain, i.e. control to feedback transfer function.
2. Select the open loop crossover frequency, $F_C$, between 10% and 20% of the switching frequency. At $F_C$, find the required compensator gain, $A_C$. In typical applications with ceramic output capacitors, the ESR zero is neglected and the required compensator gain at $F_C$ can be estimated by

$$A_C = -20 \times \log\left(\frac{1}{G_{CA}R_S} \times \frac{1}{2\pi F_C C_O} \times \frac{V_{FB}}{V_O}\right)$$

## Applications Information (Cont.)

3. Place the compensator zero, $F_{Z1}$, between 10% and 20% of the crossover frequency, $F_C$.
4. Use the compensator pole, $F_{P1}$, to cancel the ESR zero, $F_Z$.
5. Then, the parameters of the compensation network can be calculated by the following equations.

$$R_7 = \frac{10^{\frac{A_C}{20}}}{g_m}$$

$$C_5 = \frac{1}{2\pi F_{Z1} R_7}$$

$$C_8 = \frac{1}{2\pi F_{P1} R_7}$$

where gm=0.3mA/V is the EA gain of the SC4525F.

**Example:** Determine the voltage compensator for an 350kHz, 12V to 3.3V/3A converter with 47uF ceramic output capacitor.

Choose a loop gain crossover frequency of 35kHz, and place voltage compensator zero and pole at $F_{Z1}$=7kHz (20% of $F_C$), and $F_{P1}$= 677kHz. From the equation in step 2, the required compensator gain at $F_C$ is shown by the following equation.

$$A_C = -20\cdot\log\left(\frac{1}{18.5\cdot 3.53\cdot 10^{-3}}\cdot\frac{1}{2\pi\cdot 35\cdot 10^{3}\cdot 47\cdot 10^{-6}}\cdot\frac{1.0}{3.3}\right) = 7\text{dB}$$

Then the compensator parameters are

$$R_7 = \frac{10^{\frac{7}{20}}}{0.3\times 10^{-3}} = 7.4\text{k}$$

$$C_5 = \frac{1}{2\pi\times 7\times 10^3\times 7.4\times 10^3} = 3.1\text{nF}$$

$$C_8 = \frac{1}{2\pi\times 677\times 10^3\times 7.4\times 10^3} = 32\text{pF}$$

Select $R_7$=7.32k, $C_5$=3.3nF, and $C_8$= 33pF for the design.

Compensator parameters for various typical applications are listed in Table 4.

### Thermal Considerations

For the power transistor inside the SC4525F, the conduction loss $P_C$, the switching loss $P_{SW}$, and bootstrap circuit loss $P_{BST}$, can be estimated using the following.

$$P_C = D\times V_{CESAT}\times I_O$$

$$P_{SW} = \frac{1}{2}\times t_S\times V_{IN}\times I_O\times F_{SW}$$

$$P_{BST} = D\times V_{BST}\times\frac{I_O}{40}$$

where $V_{BST}$ is the BST supply voltage and $t_S$ is the equivalent switching time of the NPN transistor (see Table 3).

**Table 3 — Typical switching time**

| Input Voltage | Load Current 1A | Load Current 2A | Load Current 3A |
|---|---|---|---|
| 5V | 6.86ns | 9.71ns | 12.5ns |
| 12V | 12.5ns | 15.3ns | 18ns |

In addition, the quiescent current loss is

$$P_Q = V_{IN}\times 2\text{mA}$$

The total power loss of the SC4525F is therefore

$$P_{TOTAL} = P_C + P_{SW} + P_{BST} = P_Q$$

The temperature rise of the SC4525F is the product of the total power dissipation (previous equation) and $\theta_{JA}$ (36°C/W), which is the thermal impedance from junction to ambient for the SOIC-8 EDP package.

It is not recommended to operate the SC4525F above 125°C junction temperature.

## PCB Layout Considerations

In a step-down switching regulator, the input bypass capacitor, the main power switch and the freewheeling diode carry pulse currents (Figure 10). For jitter-free operation, the size of the loop formed by these components should be minimized. Since the power switch is already integrated within the SC4525F, connecting the anode of the freewheeling diode close to the negative terminal of the input bypass capacitor minimizes size of the switched current loop. The input bypass capacitor should be placed close to the IN pin. Shortening the traces of the SW and BST nodes reduces the parasitic trace inductance at these nodes. This not only reduces EMI but also decreases switching voltage spikes at these nodes.

The exposed pad should be soldered to a large ground plane as the ground copper acts as a heat sink for the device. To ensure proper adhesion to the ground plane, avoid using large vias directly under the device.

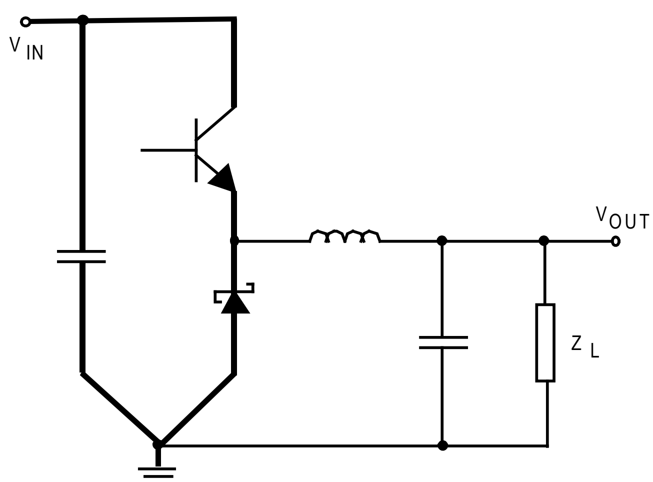



**Figure 10 — Pulse Current Loop**

Note: Heavy lines indicate the critical pulse current loop. The stray inductance of this loop should be minimized.

## Recommended Component Parameters in Typical Applications

Table 4 lists the recommended inductance ($L_1$) and compensation network ($R_7$, $C_5$, $C_8$) for common input and output voltages. The inductance is determined by assuming that the ripple current is 35% of load current $I_O$. The compensator parameters are calculated by assuming a 47μF low ESR ceramic output capacitor and a loop gain crossover frequency of $F_{SW}/10$.

**Table 4. Recommended inductance ($L_1$) and compensator ($R_7$, $C_5$, $C_8$)**

| Typical Applications | | | | Recommended Parameters | | | |
|---|---|---|---|---|---|---|---|
| **Vin(V)** | **Vo(V)** | **Io(A)** | **C2(uF)** | **L1(uH)** | **R7(k)** | **C5(nF)** | **C8(pF)** |
| 3.3 | 1.0 | 3 | 47 | 3.3 | 3.74 | 6.8 | 47 |
| | 2.0 | | | 2.2 | 6.49 | 3.3 | |
| 5 | 1.5 | | | 3.3 | 3.74 | 6.8 | |
| | 2.5 | | | 4.7 | 6.49 | 4.7 | |
| | 3.3 | | | 4.7 | 7.5 | 3.3 | 68 |
| 12 | 1.5 | | | 4.7 | 3.74 | 6.8 | 82 |
| | 2.5 | | | 6.8 | 6.98 | 4.7 | |
| | 3.3 | | | 8.2 | 8.66 | 3.3 | 68 |
| | 5 | | | 10 | 11.5 | 2.2 | 47 |
| | 7.5 | | | 10 | 18.2 | 2.2 | |

## Typical Application Schematics

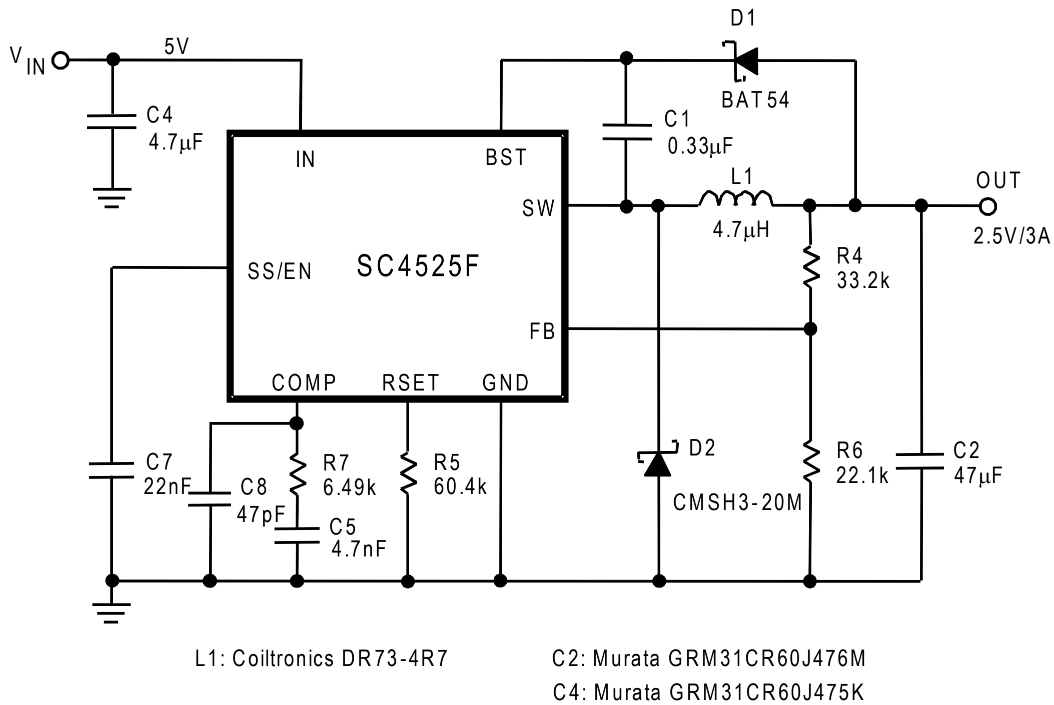



**Figure 11. 350kHz 5V to 2.5V/3A Step-down Converter**

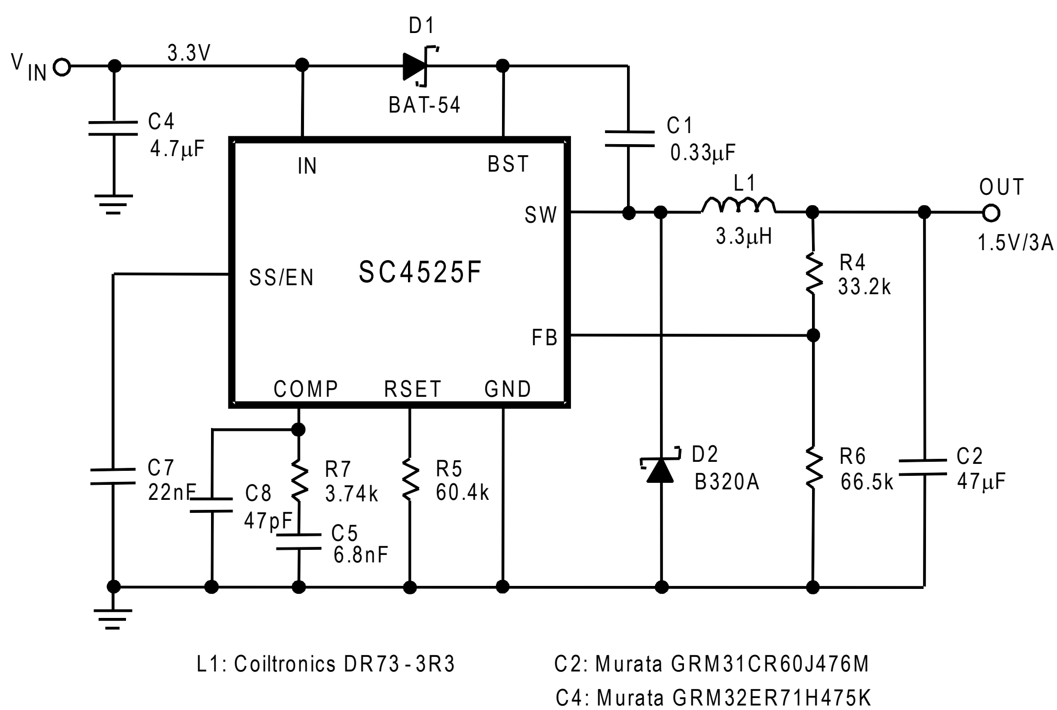
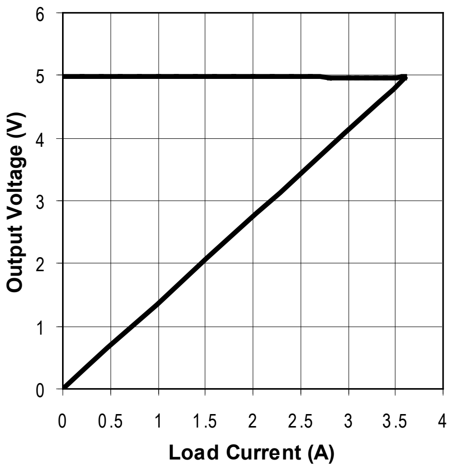


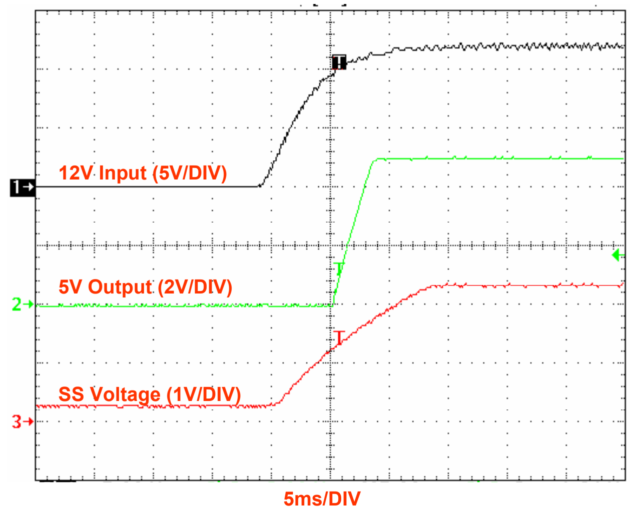

**Figure 12. 350kHz 3.3V to 1.5V/3A Step-down Converter**

## Typical Performance Characteristics

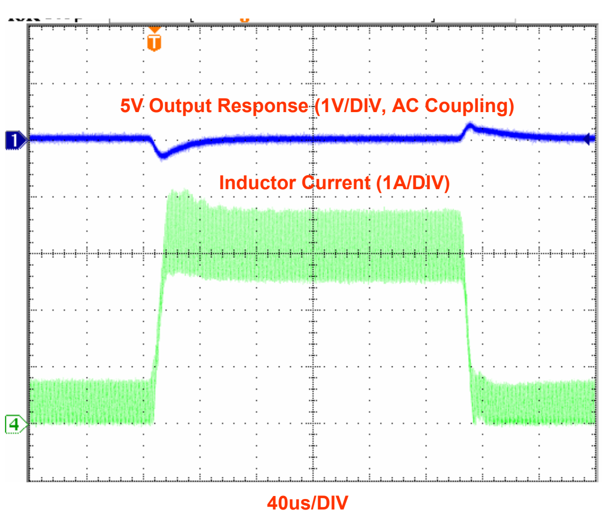
(For A 12V to 5V/3A Step-down Converter with 350kHz Switching Frequency)



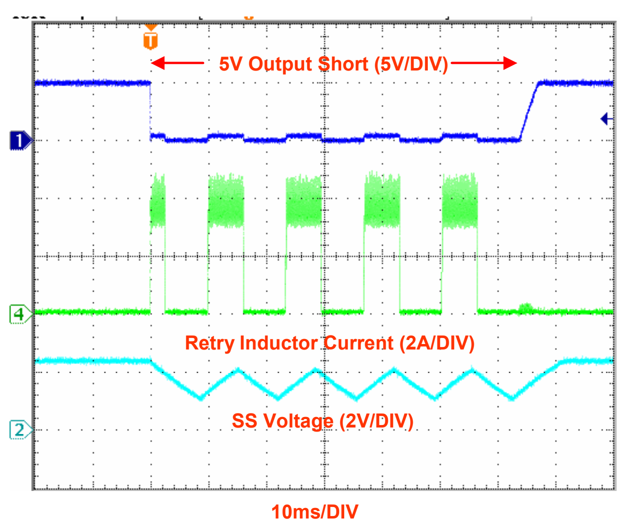

Load Characteristic




$V_{IN}$ Start up Transient ($I_O$=3A)

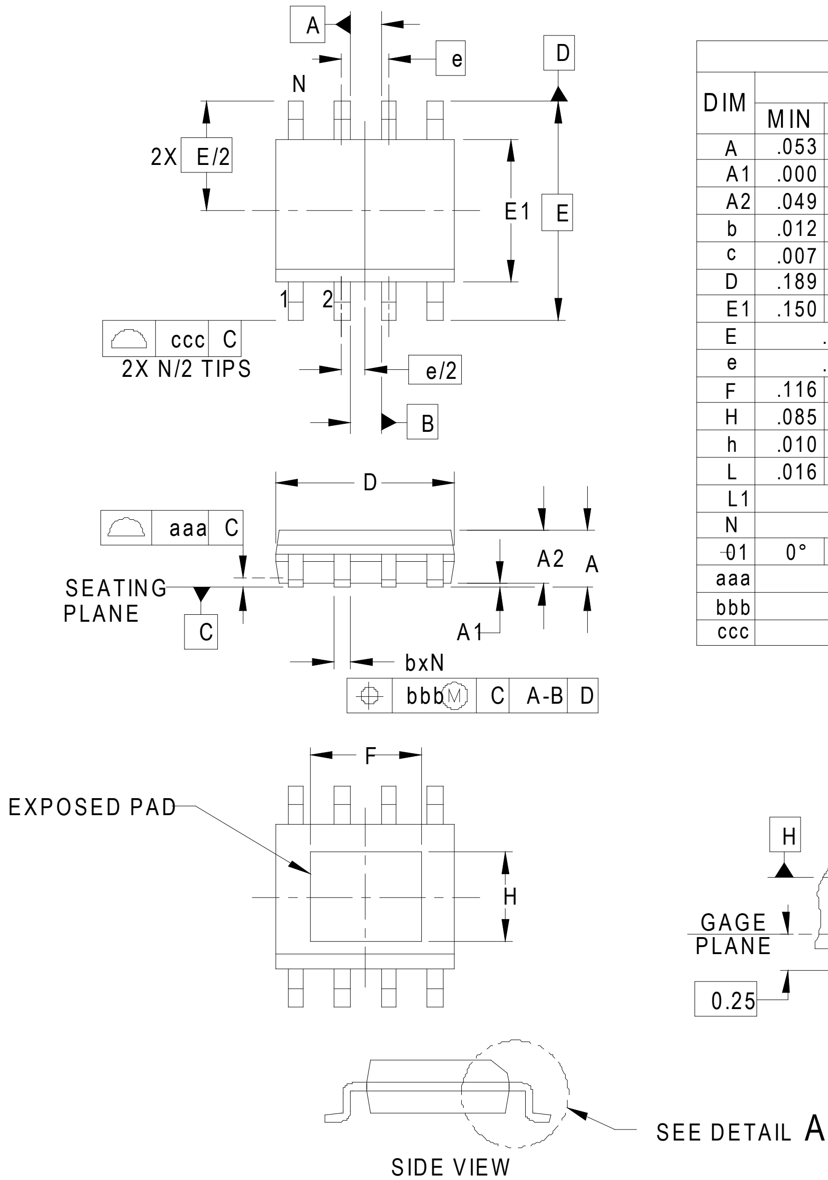



Load Transient Response ($I_O$= 0.3A to 3A)

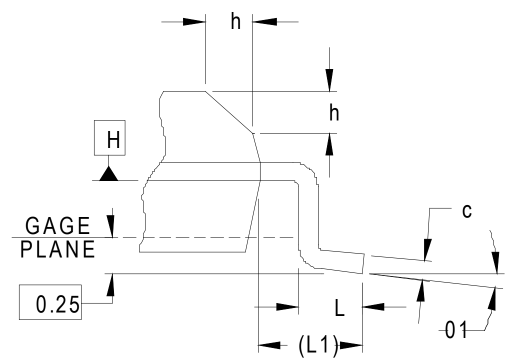



Output Short Circuit (Hiccup)

## Outline Drawing - SOIC-8 EDP




| DIM | INCHES | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | .053 | - | .069 | 1.35 | - | 1.75 |
| A1 | .000 | - | .005 | 0.00 | - | 0.13 |
| A2 | .049 | - | .065 | 1.25 | - | 1.65 |
| b | .012 | - | .020 | 0.31 | - | 0.51 |
| c | .007 | - | .010 | 0.17 | - | 0.25 |
| D | .189 | .193 | .197 | 4.80 | 4.90 | 5.00 |
| E1 | .150 | .154 | .157 | 3.80 | 3.90 | 4.00 |
| E | | .236 BSC | | | 6.00 BSC | |
| e | | .050 BSC | | | 1.27 BSC | |
| F | .116 | .120 | .130 | 2.95 | 3.05 | 3.30 |
| H | .085 | .095 | .099 | 2.15 | 2.41 | 2.51 |
| h | .010 | - | .020 | 0.25 | - | 0.50 |
| L | .016 | .028 | .041 | 0.40 | 0.72 | 1.04 |
| L1 | | (.041) | | | (1.05) | |
| N | | 8 | | | 8 | |
| θ1 | 0° | - | 8° | 0° | - | 8° |
| aaa | | .004 | | | 0.10 | |
| bbb | | .010 | | | 0.25 | |
| ccc | | .008 | | | 0.20 | |




DETAIL A

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-012, VARIATION BA.

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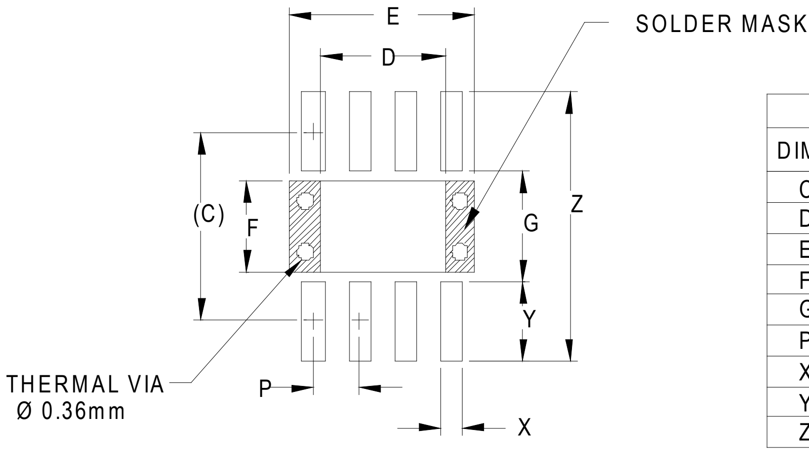
## Land Pattern - SOIC-8 EDP




| DIMENSIONS | | |
|---|---|---|
| DIM | INCHES | MILLIMETERS |
| C | (.205) | (5.20) |
| D | .134 | 3.40 |
| E | .201 | 5.10 |
| F | .101 | 2.56 |
| G | .118 | 3.00 |
| P | .050 | 1.27 |
| X | .024 | 0.60 |
| Y | .087 | 2.20 |
| Z | .291 | 7.40 |

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A, RLP NO. 300A.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

## Contact Information

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