CIRRUS LOGIC®

WM8716

High Performance 24-bit, 192 kHz Stereo DAC

DESCRIPTION

The WM8716 is a high performance stereo DAC designed for audio applications such as CD, DVD, home theatre systems, set top boxes and digital TV. The WM8716 supports data input word lengths from 16 to 24-bits and sampling rates up to 192kHz. The WM8716 consists of a serial interface port, digital interpolation filter, multi-bit sigma delta modulator and stereo DAC in a small 28-lead SSOP package. The WM8716 also includes a digitally controllable mute and attenuator function on each channel.

The internal digital filter has two selectable roll-off characteristics. A sharp or slow roll-off can be selected dependent on application requirements. Additionally, the internal digital filter can be by-passed and the WM8716 used with an external digital filter.

The WM8716 supports two connection schemes for audio DAC control. The SPI-compatible serial control port provides access to a wide range of features including on-chip mute, attenuation and phase reversal. A hardware controllable interface is also available.

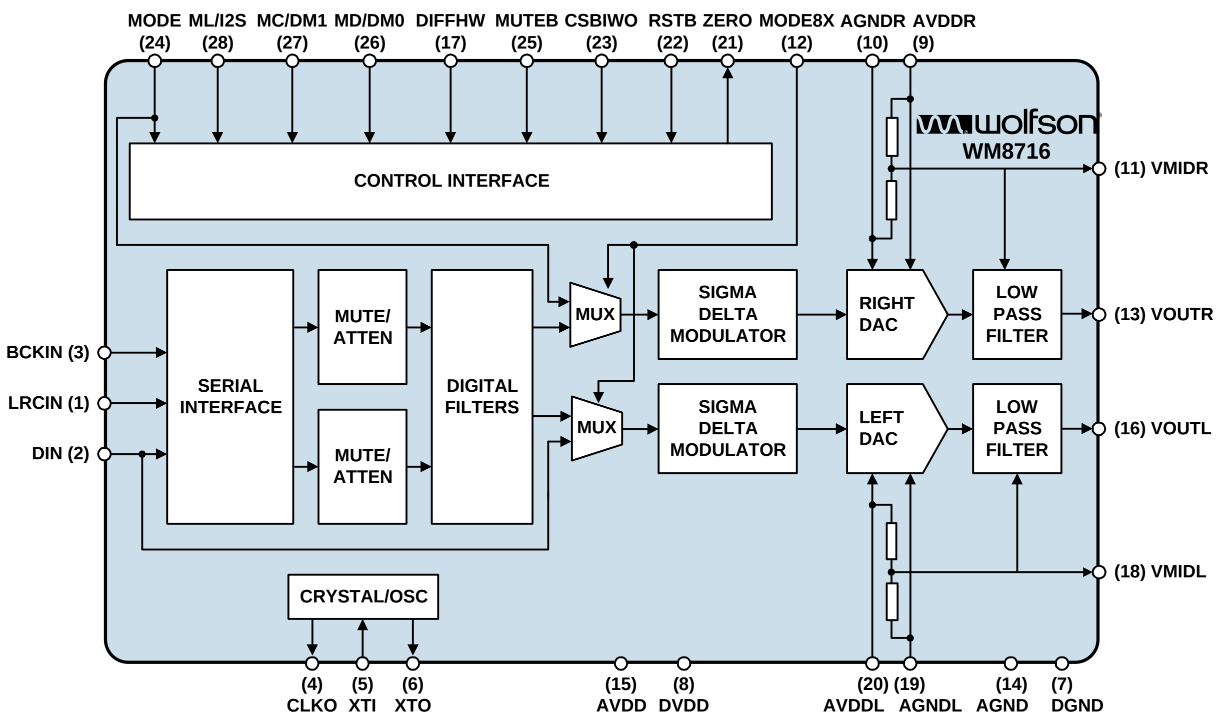
FEATURES

- 112dB SNR (‘A’ weighted @ 48kHz), THD: -97dB @ -1dB FS
- Sampling frequency: 8kHz to 192kHz
- Selectable digital filter roll-off
- Optional interface to industry standard external filters
- Differential mono mode
- Input data word: 16 to 24-bit
- Hardware or SPI compatible serial port control modes:
  - Hardware mode: mute, de-emphasis, audio format control
  - Serial mode: mute, de-emphasis, attenuation (256 steps), phase reversal
- Compatible upgrade to PCM1716

APPLICATIONS

- CD, DVD audio
- Home theatre systems
- Set top boxes
- Digital TV

BLOCK DIAGRAM



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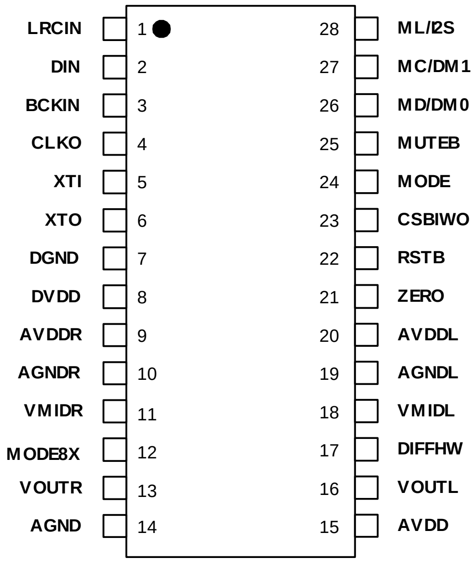
PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	PEAK SOLDERING TEMPERATURE
WM8716SEDS/V	-25 to +85°C	28-lead SSOP (Pb- free)	260°C
WM8716SEDS/RV	-25 to +85°C	28-lead SSOP (Pb- free, tape and reel)	260°C

Note:
Reel quantity = 2,000

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

CONDITION	MIN	MAX
Supply voltage	-0.3V	+7.0V
Reference input		VDD + 0.3V
Operating temperature range, T_A	-25°C	+85°C
Storage temperature	-65°C	+150°C
Voltage range digital inputs	DGND -0.3V	DVDD +0.3V
Master clock frequency		37MHz

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range	DVDD		-10%	3.3 to 5	+10%	V

Analogue supply range	AVDD		-10%	3.3 to 5	+10%	V
Ground	AGND, DGND			0		V
Difference DGND to AGND			-0.3	0	+0.3	V
Analogue supply current	AVDD = 5V			26	40	mA
Digital supply current	DVDD = 5V			22	35	mA
Analogue supply current	AVDD = 3.3V			25		mA
Digital supply current	DVDD = 3.3V			13		mA

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS

AVDD, DVDD = 5V, AGND, DGND = 0V, T_A = +25ºC, fs = 48kHz, SCKI = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC Circuit Specifications						
SNR (See Notes 1 and 2)			105	112		dB
THD (full-scale)		0dB FS		-92		dB
(See Note 2)		-1dB FS		-97		dB
Dynamic range (See Note 2)		THD @ -60dB FS	105	112		dB
Filter Characteristics (Sharp Roll-off)						
Passband		±0.0012 dB	0.4535fs			dB
Stopband		-3dB		0.491fs		
Passband ripple					±0.0012	dB
Stopband Attenuation		f > 0.5465fs	-82			dB
Delay time				30/fs		s
Filter Characteristics (Slow Roll-off)						
Passband		±0.001dB	0.274fs			
Stopband		-3dB	0.459fs			
Passband ripple					±0.001	dB
Stopband Attenuation		f > 0.732fs	-82			dB
Delay time				9/fs		s
Internal Analogue Filter						
Bandwidth		-3dB		195		kHz
Passband edge response		20kHz		-0.043		dB
Digital Logic Levels						
Input LOW level	V_{IL}				0.8	
Input HIGH level (See Note 3)	V_{IH}		2.0			V
Output LOW level	V_{OL}	I_{OL} = 2mA			DGND + 0.3V	V
Output HIGH level	V_{OH}	I_{OH} = 2mA	DVDD - 0.3V			

TEST CONDITIONS

AVDD, DVDD = 5V, AGND, DGND = 0V, T_A = +25ºC, fs = 48kHz, SCKI = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Output Levels						
Output level		Into 10kΩ, full scale 0dB, (5V supply)		1.1		V_{RMS}
		Into 10kΩ, full scale 0dB, (3.3V supply)		0.72		V_{RMS}
Minimum resistance load		To midrail or AC coupled (5V supply)		1		kΩ
		To midrail or AC coupled (3.3V supply)		600		Ω
Maximum capacitance load		5V or 3.3V		100		pF
Output DC level				AVDD/2		V
Gain mismatch channel to channel				0.5	2	%FSR
Reference Levels						
Potential divider resistance		AVDD to VMIDL/VMIDR and VMIDL/VMIDR to AGND		10		kΩ
Voltage at VMIDL/VMIDR				AVSS/2		
POR						
POR threshold				2.5V		V

Notes:

1. Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured 'A' weighted over a 20Hz to 20kHz bandwidth.
2. All performance measurements done with 20kHz low pass filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
3. Except for Pin 12 (MODE8X) and Pin 17 (DIFFHW), where V_{IH} = 2.6V min.

TERMINOLOGY

1. Signal-to-noise ratio (dB) (SNR) is a measure of the difference in level between the full-scale output and the output with no signal applied.
2. Dynamic range (dB) (DNR) is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (eg THD+N @ -60dB= -32dB, DR= 92dB).
3. THD+N (dB) is a ratio of the r.m.s. values, of (Noise + Distortion)/Signal.
4. Stop band attenuation (dB) is the degree to which the frequency spectrum is attenuated (outside audio band).
5. Channel Separation (dB) (also known as Cross-Talk) is a measure of the amount one channel is isolated from the other. Normally measured by sending a full-scale signal down one channel and measuring the other.
6. Pass-Band Ripple - Any variation of the frequency response in the pass-band region.

SIGNAL TIMING REQUIREMENTS

AUDIO INTERFACE TIMING

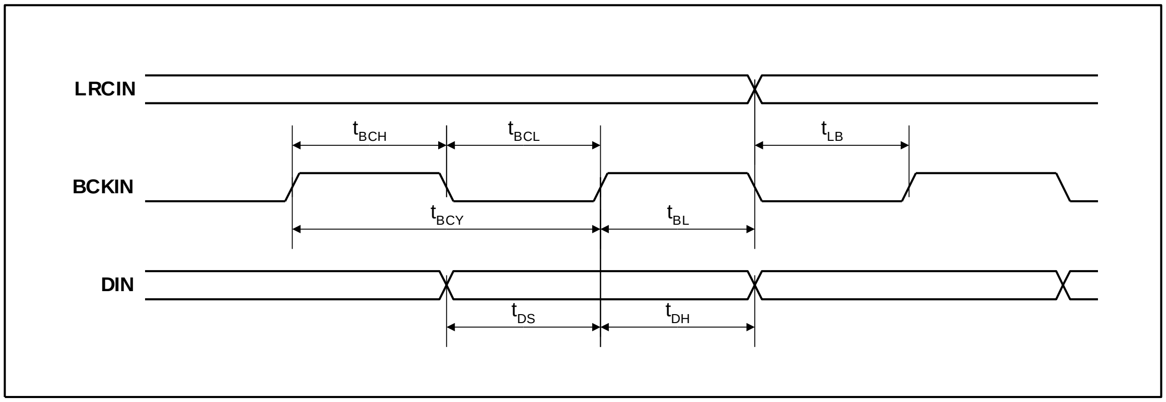


Figure 1 Audio Data Input Timing

TEST CONDITIONS

AVDD, DVDD = 5V, AGND, DGND = 0V, T_A = +25ºC, fs = 48kHz, SCKI = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
BCKIN pulse cycle time	t_{BCY}		100			ns
BCKIN pulse width high	t_{BCH}		50			ns
BCKIN pulse width low	t_{BCL}		50			ns
BCKIN rising edge to LRCIN edge	t_{BL}		30			ns
LRCIN rising edge to BCKIN rising edge	t_{LB}		30			ns
DIN setup time	t_{DS}		30			ns
DIN hold time	t_{DH}		30			ns

SYSTEM CLOCK TIMING

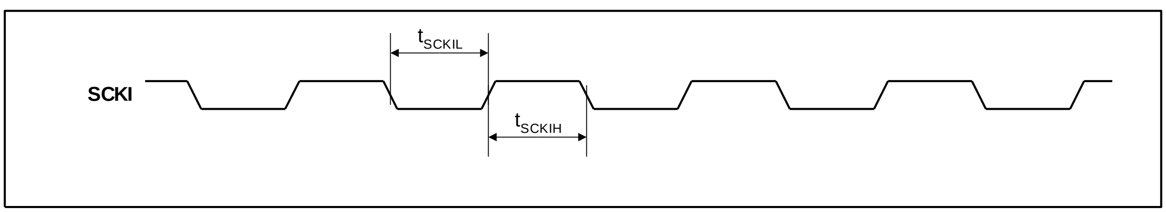


Figure 2 System Clock Timing Requirements

TEST CONDITIONS

AVDD, DVDD = 5V, AGND, DGND = 0V, T_A = +25ºC, fs = 48kHz, SCKI = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
SCKI System clock pulse width high	t_{SCKIH}		13			ns
SCKI System clock pulse width low	t_{SCKIL}		13			ns

PROGRAM REGISTER TIMING

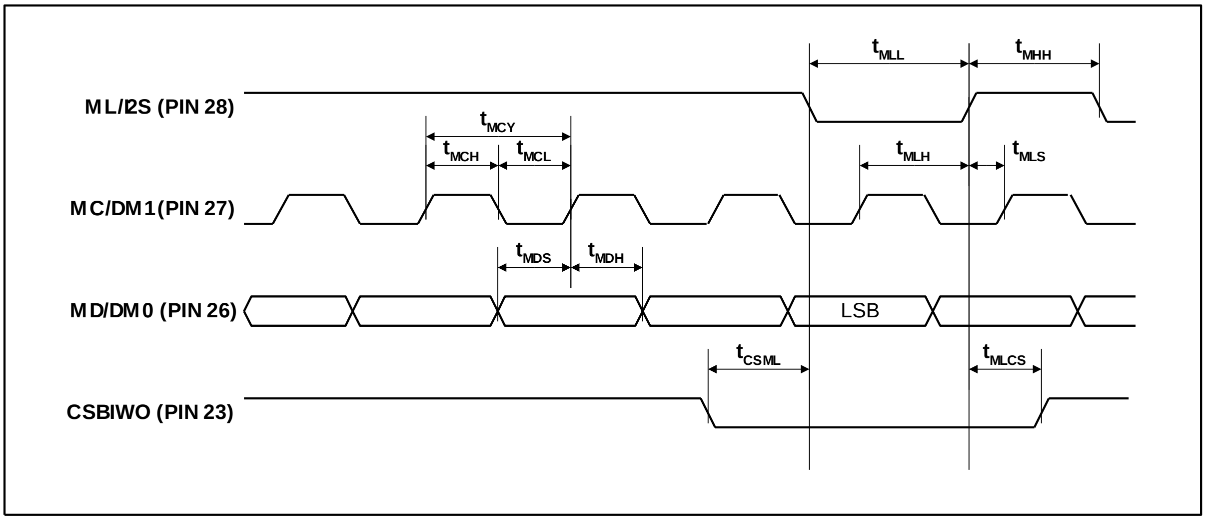


Figure 3 Program Register Input Timing

TEST CONDITIONS

AVDD, DVDD = 5V, AGND, DGND = 0V, T_A = +25ºC, fs = 48kHz, SCKI = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Program Register Input Information						
MC/DM1 Pulse cycle time	t_{MCY}		100			ns
MC/DM1 Pulse width LOW	t_{MCL}		40			ns
MC/DM1 Pulse width HIGH	t_{MCH}		40			ns
MD/DM0 Hold time	t_{MDH}		40			ns
MD/DM0 Set-up time	t_{MDS}		40			ns
ML/I2S Low level time (See Note 3)	t_{MLL}		40 + 1SYSCLK			ns
ML/I2S High level time (See Note 3)	t_{MHH}		40 + 1SYSCLK			ns
ML/I2S Hold time	t_{MLH}		40			ns
ML/I2S Set-up time	t_{MLS}		40			ns
CSBIWO Low to ML/I2S low time	t_{CSML}		10			ns
ML/I2S High to CSBIWO high time	t_{MLCS}		10			ns

Note:

3. System clock cycle.

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION			
			Hardware Mode			**Software Mode**
			Normal Mode	**Differential Mode**	**8X Mode**	
1	LRCIN	Digital input	Sample rate clock input.			
2	DIN	Digital input	Audio data serial input		DINL	Audio data serial input
3	BCKIN	Digital input	Audio data bit clock input.			
4	CLKO	Digital output	Oscillator buffered output (system clock).			
5	XTI	Analogue input	Oscillator input.			
6	XTO	Analogue output	Oscillator output.			
7	DGND	Supply	Digital ground supply.			
8	DVDD	Supply	Digital positive supply.			
9	AVDDR	Supply	Analogue positive supply.			
10	AGNDR	Supply	Analogue ground supply.			
11	VMIDR	Analogue output	Mid rail right channel.			
12	MODE8X	Digital input	Internal pull-down, active high, 8 x fs mode.			
13	VOUTR	Analogue output	Right channel DAC output.			
14	AGND	Supply	Analogue ground supply.			
15	AVDD	Supply	Analogue positive supply.			
16	VOUTL	Analogue output	Left channel DAC output.			
17	DIFFHW	Digital input	Internal pull-down, active high, differential mono mode			
18	VMIDL	Analogue output	Mid rail left channel.			
19	AGNDL	Supply	Analogue ground supply.			
20	AVDDL	Supply	Analogue positive supply.			
21	ZERO	Digital output	Infinite zero detect – active low. Open drain type output with active pull-down.			
22	RSTB	Digital input	Reset input – active low. Internal pull-up.			
23	CSBIWO	Digital input Internal pull-down	Wordlength: Low for 16-bit data. High for 20-bit (normal) or 24-bit I^{2}S data.	Wordlength: Low for 16-bit data. High for 20-bit (normal) or 24-bit I^{2}S data.	Wordlength: Low for 20-bit data. High for 24-bit data.	Low for serial interface operation.
24	MODE	Digital input Internal pull-up	Low for hardware mode.	Low for left mono mode. High for right mono mode	DINR	High for software mode.
25	MUTEB	Digital input Internal pull-up	Low to soft mute. High for normal operation. Z for automute.	Low to soft mute. High for normal operation. Z for automute.	Low to soft mute. High for normal operation. Z for automute.	Low to soft mute. High for normal operation. Z for automute.
26	MD/DM0	Digital input Internal pull-up	De-emphasis mode select bit 0.	Low for no de-emphasis. High for 44.1kHz de-emphasis.	LRP – LRCLK polarity select.	Control serial interface data signal.
27	MC/DM1	Digital input Internal pull-up	De-emphasis mode select bit 1.	Low for normal filter operation. High for filter slow roll-off.	Unused. Leave unconnected.	Control serial interface clock signal.
28	ML/I2S	Digital input Internal pull-up	Audio serial format: Low – right justified. High – I^{2}S.	Audio serial format: Low – right justified. High – I^{2}S.	Input data format: Low – right justified. High – left justified.	Control serial interface load signal.

Note: Digital input pins have Schmitt trigger input buffers except Pin 12 and Pin 17.

DEVICE DESCRIPTION

The WM8716 is a high performance 128fs oversampling rate stereo DAC employing a novel 64 level sigma delta DAC design which provides optimised signal-to-noise performance and clock jitter tolerance. It is ideally suited to high quality audio applications such as CD, DVD-audio, home theatre receivers and professional mixing consoles. The WM8716 supports sample rates from 8ks/s to 192ks/s.

The control functions of the WM8716 are either pin selected (hardware mode) or programmed via the serial interface (software mode). Control functions that are available include: data input word length and format selection (16-24 bits: I^2S, left justified or right justified): de-emphasis sample rate selection (48kHz, 44.1kHz and 32kHz); differential output modes; a software or hardware mute and independently digitally controllable attenuation on both channels.

The digital filtering may be bypassed entirely by selecting MODE8X. Data is then input directly to the DAC, bypassing the digital filters. Left and right channels are input separately, using the MODE pin as the right channel input. This mode allows the use of alternative digital filters, such as the Pacific Microsonics PMD100 HDCD filter.

In addition to the normal stereo operating mode the WM8716 may also be used in dual differential mode with either the left or right channel (selectable) being output differentially. Two WM8716s can then be used in parallel to implement a stereo channel, each supporting a single channel differentially. This mode is available in both software and hardware modes and may also be used in conjunction with MODE8X.

SYSTEM CLOCK

Sample rates from 8ks/s up to 96ks/s are available, and automatically selected, with a system clock of 256fs, 384fs, 512fs or 768fs. In addition a system clock of 128fs or 192fs may be used, with sample rates up to 192ks/s. With a 128fs or 192fs system clock 64x oversampling mode operation is automatically selected and the first stage of the digital filter is bypassed.

WM8716 has an asynchronous monitor circuit, which in the event of removal of the master system clock, resets the digital filters and analogue circuits, muting the output. Re-application of the system clock re-starts the filters from an intitialised state. Control registers are not reset under this condition.

The WM8716 is tolerant of asynchronous bit clock jitter. The internal signal processing resynchronises to the external LRCIN once the phase difference between bit clock and the system clock exceeds half an LRCIN period. During this re-synch period the interpolating filters will either miss or repeat an audio sample, minimising the audible effects of the operation. Table 1 shows the typical system clock frequency inputs for the WM8716.

SAMPLING RATE (LRCIN)	SYSTEM CLOCK FREQUENCY (MHZ)					
	128fs	192fs	256fs	384fs	512fs	768fs
32kHz	4.096	6.144	8.192	12.288	16.384	24.576
44.1kHz	5.6448	8.467	11.2896	16.9340	22.5792	33.8688
48kHz	6.114	9.216	12.288	18.432	24.576	36.864
96kHz	12.288	18.432	24.576	36.864	Unavailable	Unavailable
192kHz	24.576	36.864	Unavailable	Unavailable	Unavailable	Unavailable

Table 1 System Clock Frequencies Versus Sampling Rate

AUDIO DATA INTERFACE

Data may be input at a rate corresponding to the system clock having a rate of 256fs or 384fs or 512fs or 768fs, in which case an oversampling ratio of 128x is selected. Alternatively a rate of 128fs or 192fs may be used, in which case the first filter stage is bypassed and an oversampling ratio of 64x results. Finally, in MODE8X, data may be input at 8x the normal rate, in which case separate input pins are used to input the two stereo channels of data (unless DIFFHW mode and MODE8X are both selected, in which case only a mono channel is converted differentially). In MODE8X all filter stages are by-passed, prior to the sigma delta modulator. Data is input MSB first in all modes.

NORMAL SAMPLE RATE

In normal mode, the data is input serially on one pin for both left and right channels.

Data can be "right justified" meaning that the last 16, 20 or 24 bits (depending on chosen PCM word length) that were clocked in prior to the transition on LRCIN are valid.

Alternatively data can be "left justified" (20 and 24-bit PCM data only), where the bits are clocked in as the first 20 or 24 bits after a transition on LRCIN.

For the three I²S modes supported (16-bit, 20-bit and 24-bit PCM data), data is clocked "left justified" except with one additional preceding clock cycle.

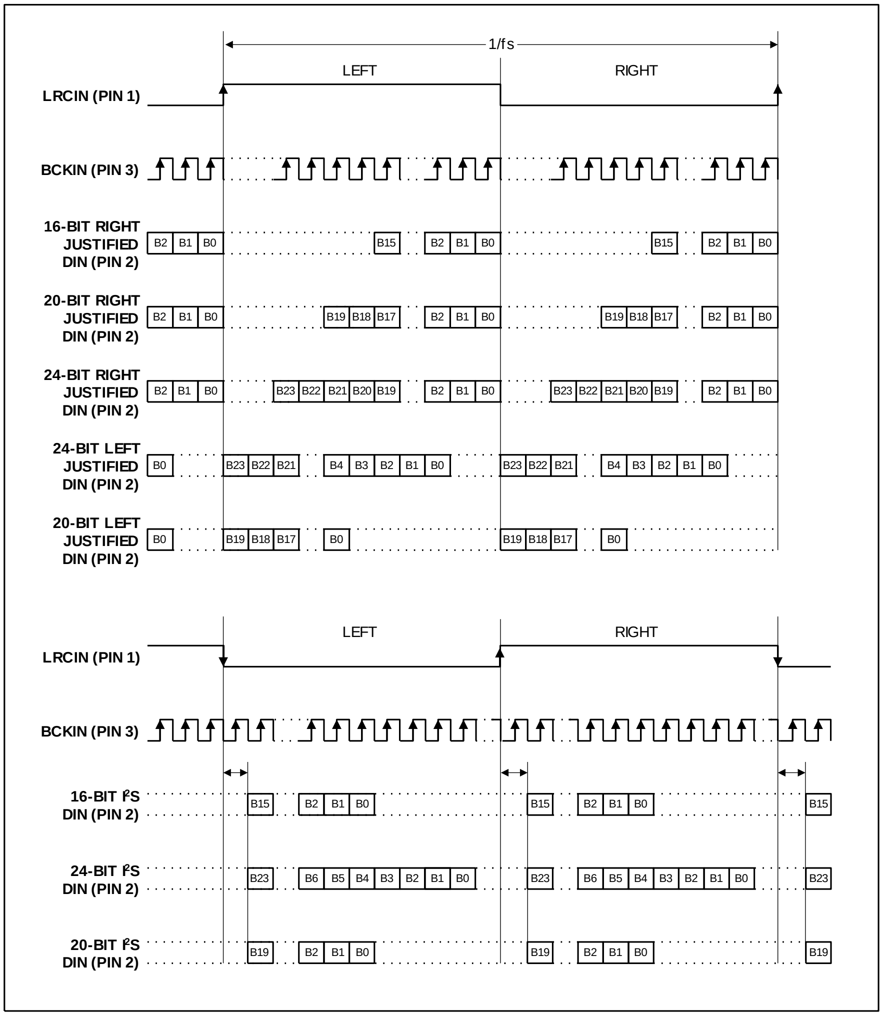


Figure 4 Audio Data Input Format

8 X FS INPUT SAMPLE RATE

Due to the higher speed of the interface in 8 x fs mode, audio data is input on two pins. The MODE pin (pin 24) is used as the second input for the right channel data and left data is input on DIN (pin 2). In this mode, software control of the device is not available. The data can be input in two formats, left or right justified, selectable by ML/I2S and two word lengths (20 or 24 bit), selectable by CSBIWO. In both modes the data is always clocked in MSB first.

For left justified data the word start is marked by the falling edge of LRCIN. The data is clocked in on the next 20/24 BCKIN rising edges. This format is compatible with devices such as the PMD100.

For right justified the data is justified to the rising edge of LRCIN and the data is clocked in on the preceding 20/24 BCKIN rising edges before the LRCIN rising edge. This format is compatible with devices such as the DF1704 or SM5842.

In both modes the polarity of LRCIN can be switched using MD/DM0.

Differential hardware mode can be used in conjunction with 8fs mode by setting the DIFFHW pin high. In differential 8fs mode the data is input on DIN and output differentially. MODE is unused and must be tied low.

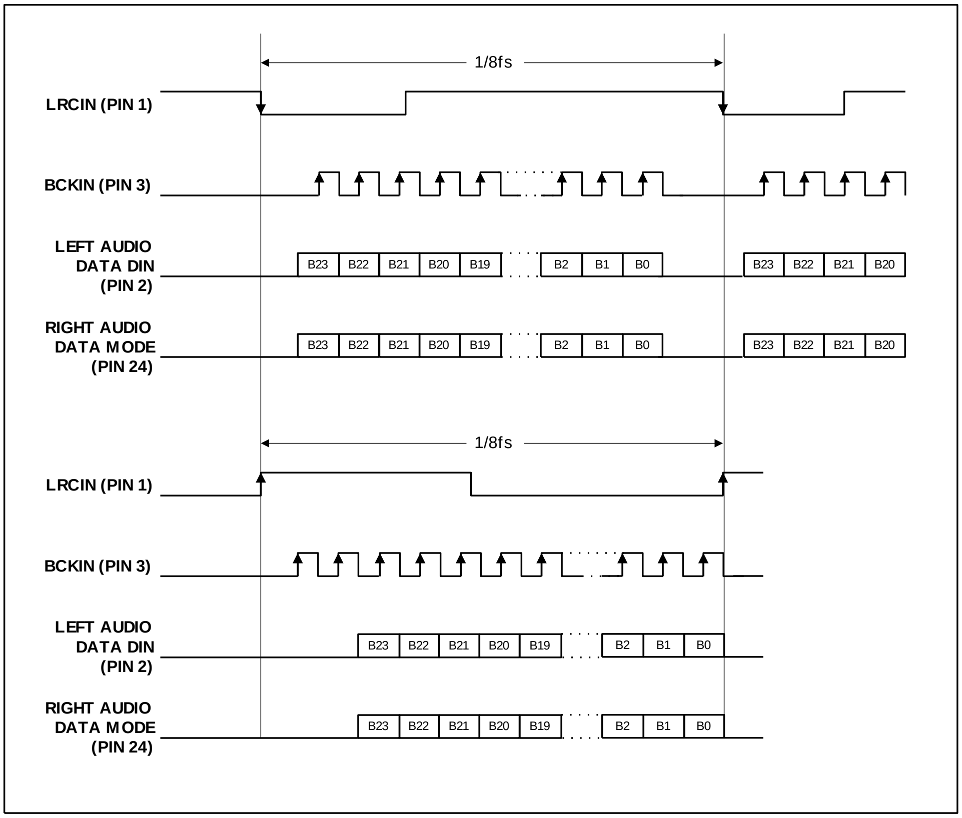


Figure 5 Audio Data Input Format (8 x fs Operation)

MODES OF OPERATION

Control of the various modes of operation is either by software control over the serial interface, or by hard-wired pin control. Selection of software or hardware mode is via MODE pin. The following functions may be controlled either via the serial control interface or by hard wiring of the appropriate pins.

HARDWARE CONTROL MODES

When the MODE pin is held 'low' the following hardware modes of operation are available. In Hardware differential mode or 8X mode some of these modes/control words are altered or unavailable.

DE-EMPHASIS CONTROL

MDDM1 PIN 27	MCDMO PIN 26	DE-EMPHASIS
L	L	Off
L	H	48kHz
H	L	44.1kHz
H	H	32kHz

Table 2 De-Emphasis Control

AUDIO INPUT FORMAT

CSBIIS PIN 28	CSBIWO PIN 23	DATA FORMAT
L	L	16 bit normal right justified
L	H	20 bit normal right justified
H	L	16 bit I^2S
H	H	24 bit I^2S

Table 3 Audio Input Format

SOFT MUTE

MUTEB PIN 25	FUNCTION
L	Mute On (no output)
Z	Automute
H	Mute Off (normal operation)

Table 4 Soft Mute

A logic low on the MUTEB pin will cause the attenuation to ramp to infinite attenuation at a rate of 128/fs seconds per 0.5dB step. Setting MUTEB high will cause the attenuation to ramp back to its previous value.

Leaving MUTEB undriven allows operation of the automute circuit in both hardware and software modes. On receiving 1024 consecutive zero value audio samples, the analogue stage output mute is asserted. This may be overdriven from the MUTEB pin to disable the automute function, or output as a weak (10kohm) output signal.

SOFTWARE CONTROL INTERFACE

The WM8716 can be controlled using a 3-wire serial interface. MD/DM0 (pin 26) is used for the program data, MC/DM1 (pin 22) is used to clock in the program data and ML/I2S (pin 28) is use to latch in the program data. The 3-wire interface protocol is shown in Figure 6. CSB/IWO (pin 23) must be low when writing.

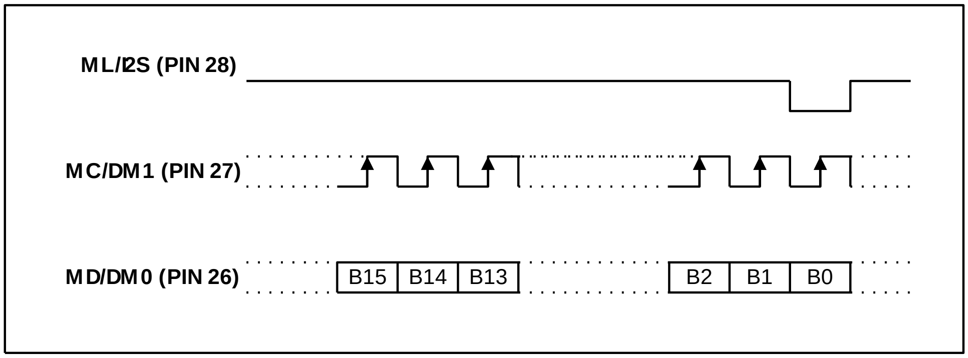


Figure 6 Three-Wire Serial Interface

REGISTER MAP

WM8716 controls the special functions using 4 program registers, which are 16-bits long. These registers are all loaded through input pin MD/DM0. After the 16 data bits are clocked in, ML/I2S is used to latch in the data to the appropriate register. Table 5 shows the complete mapping of the 4 registers. Note that in hardware differential mode and 8X modes, software control is not available. The hardware differential mode (Diff[1:0]) clock loss detector disable (CDD) can only be accessed by writing to M2[8:5] with the pattern 1111. Register M4 is then accessible by setting A[2:0] to 110.

	B15	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
M0	-	-	-	-	A2 (0)	A1(0)	A0(0)	LDL	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0
M1	-	-	-	-	A2(0)	A1(0)	A0(1)	LDR	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
M2	-	-	-	-	A2(0)	A1(1)	A0(0)	-	-	-	-	IW1	IW0	OPE	DEM	MUT
M3	-	-	-	-	A2(0)	A1(1)	A0(1)	IZD	SF1	SF0	CK0	REV	SR0	ATC	LRP	I^2S
M4	-	-	-	-	A2(1)	A1(1)	A0(0)	-	-	CDD	DIFF1	DIFF0	-	-	-	-

Table 5 Mapping of Program Registers

REGISTER	BITS	NAME	DEFAULT	DESCRIPTION
0	[7:0]	AL[7:0]	FF	Attenuation data for left channel.
	8	LDL	0	Attenuation data load control for left channel.
1	[7:0]	AR[7:0]	FF	Attenuation data for right channel.
	8	LDR	0	Attenuation data load control for right channel.
2	0	MUT	0	Left and right DACs soft mute control.
	1	DEM	0	De-emphasis control.
	2	OPE	0	Left and right DACs operation control.
	[4:3]	IW[1:0]	0	Input audio data bit select.
3	0	I2S	0	Audio data format select.
	1	LRP	0	Polarity of LRCIN select.
	2	ATC	0	Attenuator control.
	3	SR0	0	Digital filter slow roll-off select.
	4	REV	0	Output phase reverse.
	5	CKO	0	CLKO frequency select.
	[7:6]	SF[1:0]	0	Sampling rate select.
	8	IZD	0	Infinite zero detection circuit control.
4	[5:4]	DIFF	0	Differential output mode.
	6	CDD	0	Clock loss detector disable.

Table 6 Register Bit Descriptions

DAC OUTPUT ATTENUATION

The level of attenuation for eight bit code X, is given by:

$0.5 * (X - 255)$ dB, $\quad 1 \leq X \leq 255$

$-\infty$dB (mute), $\quad X = 0$

Bit 8 in register 0 (LDL) is used to control the loading of attenuation data in B[7:0]. When LDL is set to 0, attenuation data will be loaded into AL[7:0], but it will not affect the filter attenuation. LDR in register 1 has the same function for right channel attenuation. Only when LDL or LDR is set to '1' will the filter attenuation be updated. This permits left and right channel attenuation to be updated simultaneously.

Attenuation level is controlled by AL[7:0] (left channel) or AR[7:0] (right channel). Attenuation levels are given in Table 4.

X[7:0]	ATTENUATION LEVEL
00(hex)	- ∞dB (mute)
01(hex)	-127.0dB
:	:
:	:
FD(hex)	-1.0dB
FE(hex)	-0.5dB
FF(hex)	0.0dB

Table 7 Attenuation Control Level

Bit 2 in Reg3 is used to control the attenuator (ATC). When ATC is “high”, the attenuation data loaded in program register 0 is used for both the left and the right channels. When ATC is low, the attenuation data for each register is applied separately to left and right channels.

SOFT MUTE

MUT (REG2, B0)	
L	Soft Mute off (normal operation)
H	Soft Mute on (no output)

Table 8 Soft Mute

Setting MUT causes the attenuation to ramp from the current value down to 00. The values held in the attenuation registers are unchanged. When MUT is reset the attenuation will ramp back up to the previous value. The ramp rate is 128/fs s/0.5dB step.

DIGITAL DE-EMPHASIS

DEM (REG2, B1)	
L	De-emphasis off
H	De-emphasis on

Table 9 Digital De-Emphasis

DAC OPERATION ENABLE

OPE (REG2,B2)	
L	Normal operation
H	DAC output forced to bipolar zero, irrespective of input data.

Table 10 DAC Operation Enable

AUDIO DATA INPUT FORMAT

I2S (REG3, B0)	IW1 (REG2, B4)	IW0 (REG2, B3)	AUDIO INTERFACE
0	0	0	16-bit standard right justified
0	0	1	20-bit standard right justified
0	1	0	24-bit standard right justified
0	1	1	24-bit left justified (MSB first)
1	0	0	16-bit I^2S
1	0	1	24-bit I^2S
1	1	0	20-bit I^2S
1	1	1	20-bit left justified (MSB first)

Table 11 Audio Data Input Format

POLARITY OF LR INPUT CLOCK

The left channel data for a particular sample instant is always input first, then the right channel data.

LRP (REG3, B1)	
L	LR High – left channel LR Low – right channel
H	LR Low – left channel LR High – right channel

Table 12 Polarity of LR Input Clock

INDIVIDUAL OR COMMON ATTENUTATION CONTROL

ATC (REG3, B2)	
L	Individual control
H	Common control from Reg0

Table 13 Individual or Common Attenuation Control

DIGITAL FILTER ROLL-OFF SELECTION

SRO (REG3, B3)	
L	Sharp
H	Slow

Table 14 Digital Filter Roll-Off Selection

ANALOGUE OUTPUT POLARITY REVERSAL

REV (REG3, B4)	
L	Normal
H	Inverted

Table 15 Analogue Output Polarity Reversal

CLKO OUTPUT FREQUENCY

CKO (REG3, B5)	
L	XTI
H	XTI/2

Table 16 CLKO Output Frequency

DE-EMPHASIS SAMPLE RATE

SF1 (REG3, B7)	SF0 (REG3, B6)	SAMPLE RATE
0	0	No de-emphasis
0	1	48kHz
1	0	44.1kHz
1	1	32kHz

Table 17 De-Emphasis Sample Rate

INFINITE ZERO DETECT

IZD (REG3, B8)	
L	Zero detect mute off
H	Zero detect mute on

Table 18 Infinite Zero Detect

DIFFERENTIAL MONO MODE

Using bits 4 and 5, the differential output mode may be selected to be one of normal stereo, reversed stereo, mono left or mono right, as shown in Table 19.

DIFF[1:0] B[4:5])	DIFFERENTIAL OUTPUT MODE
00	Stereo
01	Stereo reverse.
10	Mono left – differential outputs. VOUTL is left channel. VOUTR is the negative of left channel.
11	Mono right – differential outputs. VOUTL is the negative right channel. VOUTR is right channel.

Table 19 Differential Output Modes

Using these controls a pair of WM8716 devices may be used to build a 'dual differential' stereo implementation with higher performance and differential output.

CLOCK LOSS DETECTOR DISABLE

CDD (REG4, B6)	
L	Clock loss detector on
R	Clock loss detector off

Table 20 Clock Loss Detector Disable

When the system clock is inactive for approximately 100μs, the clock loss detector circuit detects the loss of clock and the analogue circuitry is forced into a mute condition and the digital filters reset. Setting the CDD bit disables this behaviour.

MUTE MODES

The device has various mute modes.

	DIGITAL FILTER	ANALOGUE	
		ANRES	ANMUTE
Reg bit OPE = '1'	Unaffected		Asserted
MUTEB pin	Gain ramped to zero On release volume ramps to previous value		Asserted when gain = 0
AUTOMUTE (detect 1024 zero input samples)	Automute has no effect on digital filters		Asserted after 1024 zero input samples if IZD = 1
Reg bit MUT	As MUTEB pin		As MUTEB pin
Gain = 00 (left & right)	Gain = -∞dB		Asserted
RAM initialise	Gain initialised to 0dB		Asserted
Loss of system clock	Not running (no clock). On clock restart, filters initialised, RAM initialised. Registers unchanged	Asserted	Asserted
No LRCLK or invalid SCLK/LRCLK ratio	Filters initialised, RAM initialised. Registers unchanged	Asserted	Asserted
RB	Reset – gain initialised to 0dB	Asserted	Asserted
Power-on reset	Reset	Asserted	Asserted

Table 21 Mute Modes

- ANRES is the reset to the switched capacitor filter.
- ANMUTE is an analogue muting signal gating the analogue signal at the output (after the SC filter)
- AUTOMUTE is asserted when both the IZD register bit is asserted and the input audio data has been zero on both left and right channels for 1024 input samples. The first non-zero sample de-asserts.
- Applying a logic low to MUTEB or setting MUT in Reg2 causes the gain registers to ramp to zero. When a logic high is applied, the gain ramps slowly back up to the value held in the appropriate attenuation register (AL or AR). The ramp rate = 128/fs s/0.5dB step.

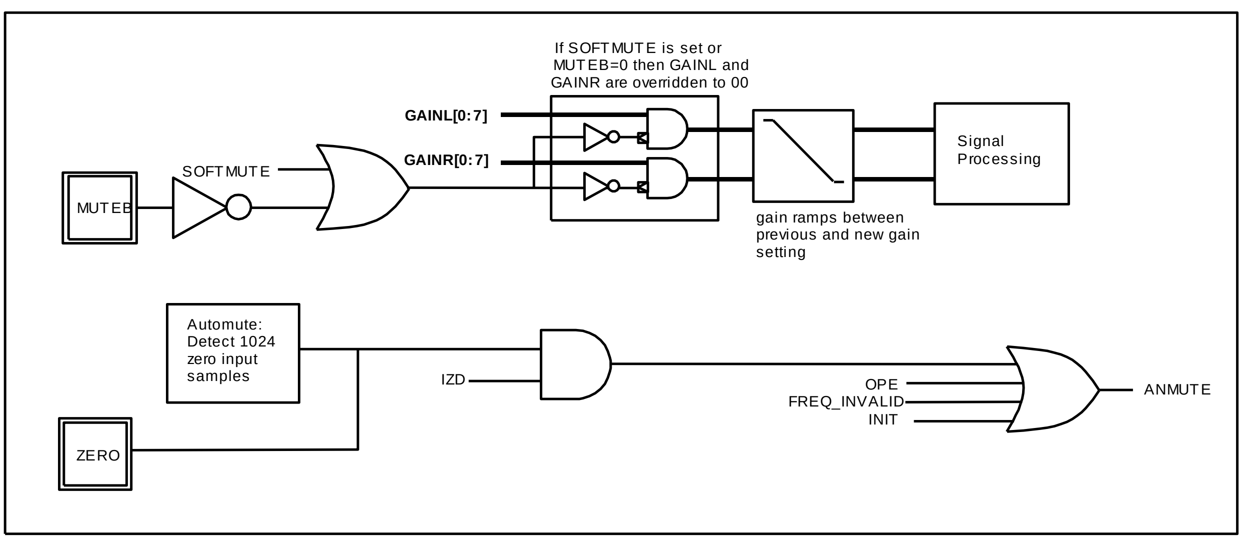


Figure 7 Mute Modes

FILTER RESPONSES

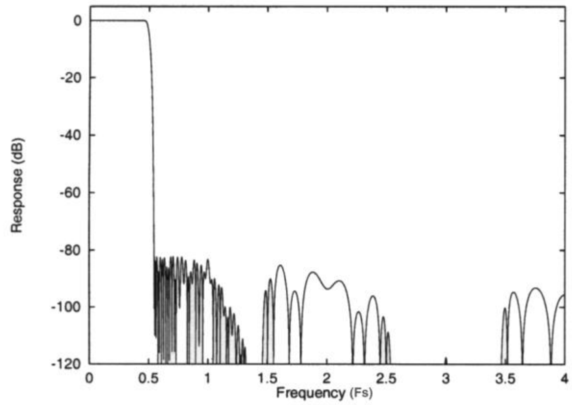


Figure 8 Digital Filter Response (Sharp Roll-off Mode)

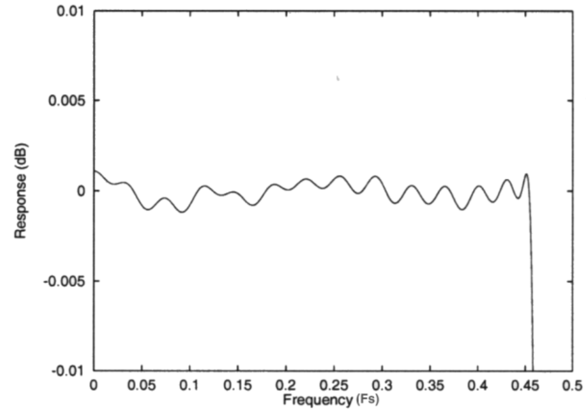


Figure 9 Digital Filter Response (Sharp Roll-off Mode)

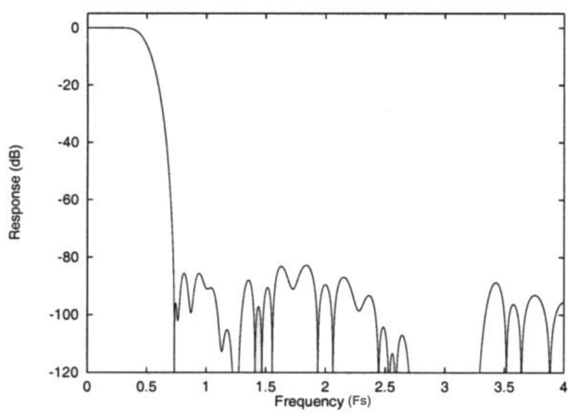


Figure 10 Digital Filter Response (Slow Roll-off Mode)

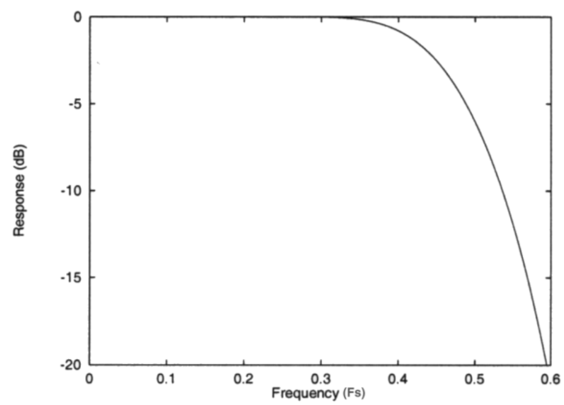


Figure 11 Digital Filter Response (Slow Roll-off Mode)

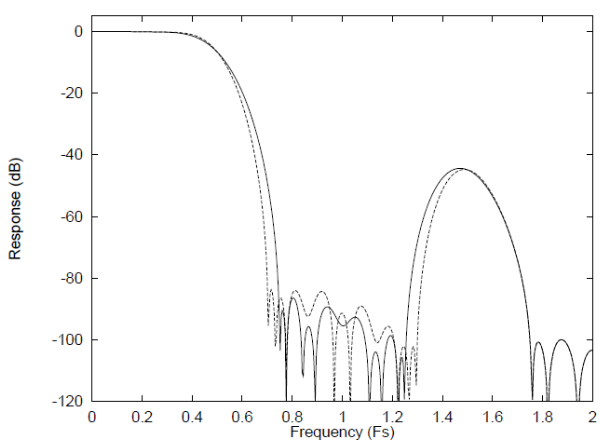


Figure 12 Digital Filter Response 128fs Mode (192kHz Sample Rate) Normal Mode – Solid, Slow Mode – Dashed

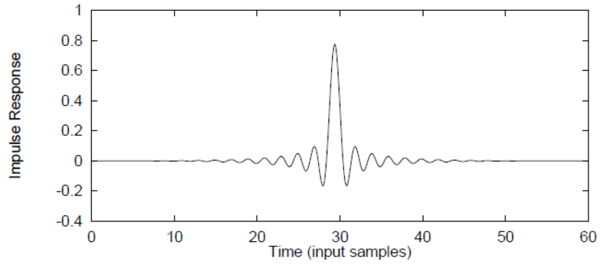


Figure 13 Impulse Response (Normal Roll-off, no De-emphasis)

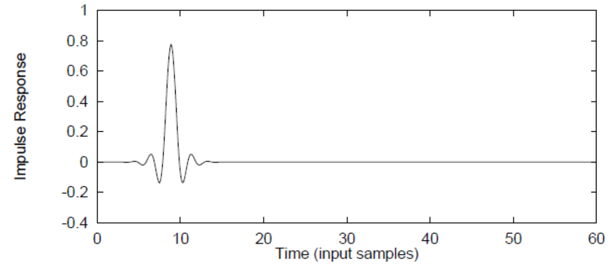


Figure 14 Impulse Response (Slow Roll-off, no De-emphasis)

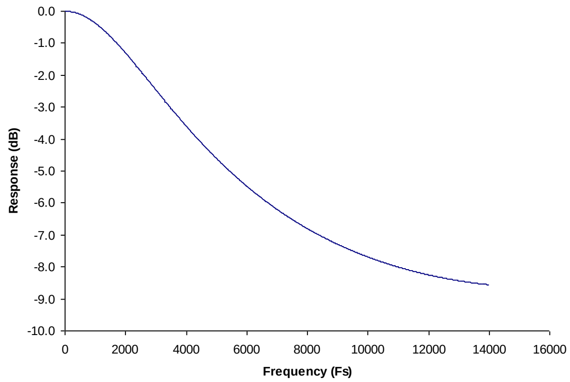


Figure 15 De-emphasis frequency response (fs=32kHz)

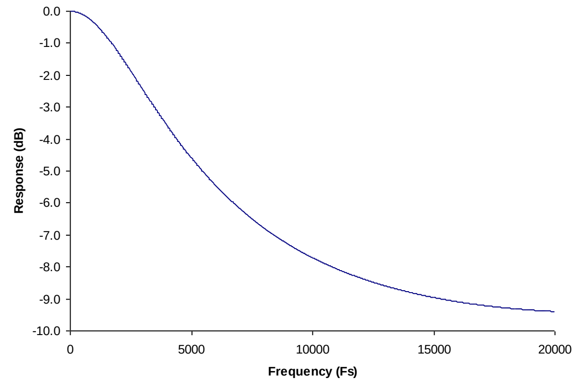


Figure 15 De-emphasis frequency response (fs=44.1kHz)

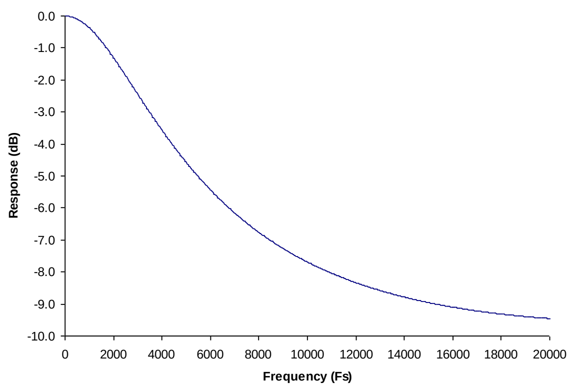


Figure 16 De-emphasis frequency response (fs=48kHz)

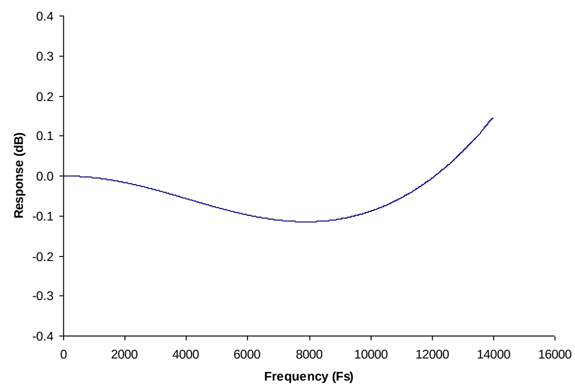


Figure 17 De-emphasis frequency response error (fs=32kHz)

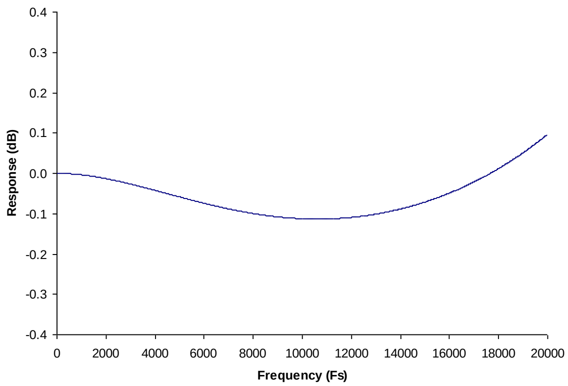


Figure 18 De-emphasis frequency response error (fs=44.1kHz)

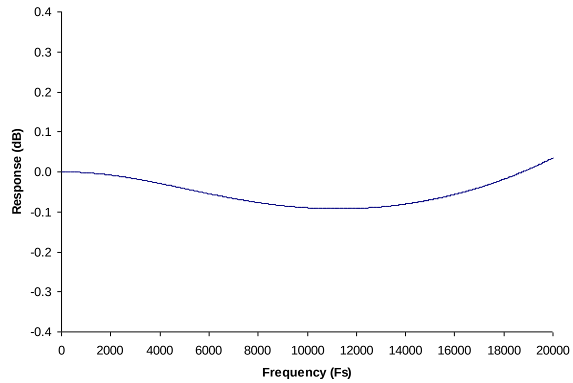
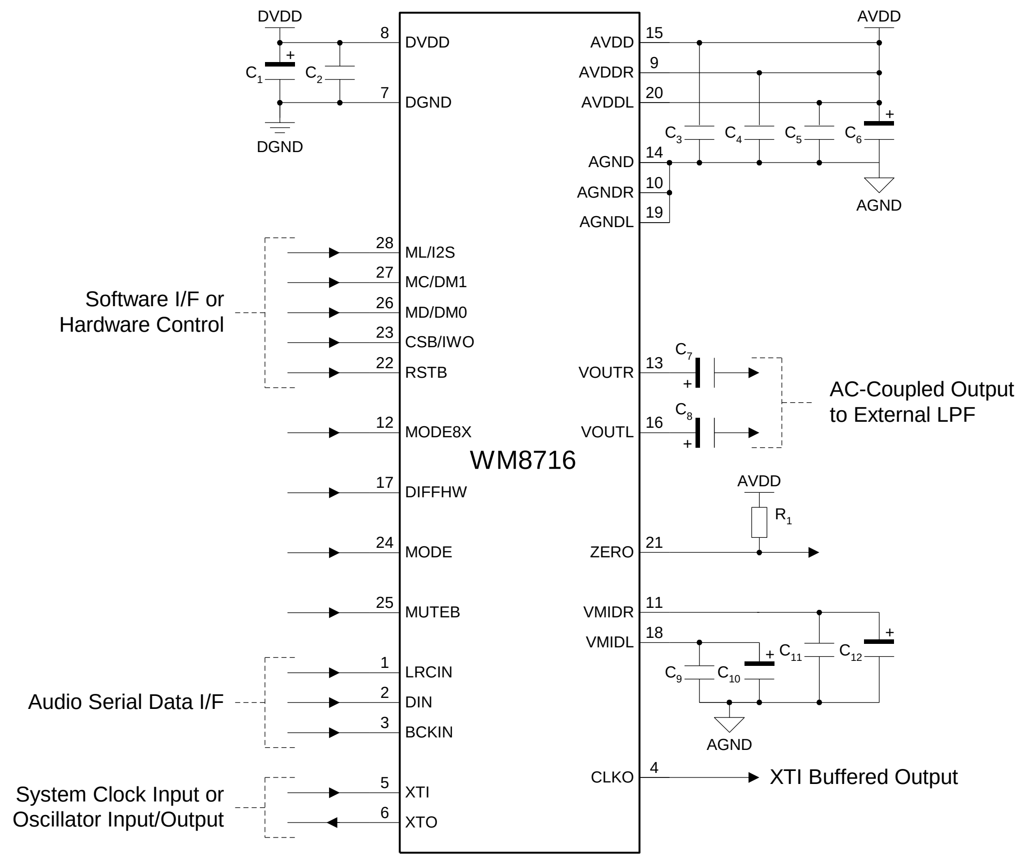


Figure 19 De-emphasis frequency response error (fs=48kHz)

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS



NOTES:

1. AGND and DGND should be connected as close to the WM8716 as possible.
2. C_2 to C_5, C_9 and C_{11} should be positioned as close to the WM8716 as possible.
3. Capacitor type used can have a big effect on device performance. It is recommended that capacitors with very low ESR are used and that ceramics are either NPO or COG type material to achieve best performance from the WM8716.

Figure 20 External Components Diagram

RECOMMENDED EXTERNAL COMPONENTS VALUES

COMPONENT REFERENCE	SUGGESTED VALUE	DESCRIPTION
C1 and C6	10µF	De-coupling for DVDD and AVDD.
C2 to C5	0.1µF	De-coupling for DVDD and AVDD.
C7 and C8	10µF	Output AC coupling caps to remove VMID DC level from outputs.
C9 and C11	0.1µF	Reference de-coupling capacitors for VMIDR and VMIDL.
C10 and C12	10µF	
R1	10kΩ	Resistor to AVDD for open drain output operation.

Table 22 External Components Description

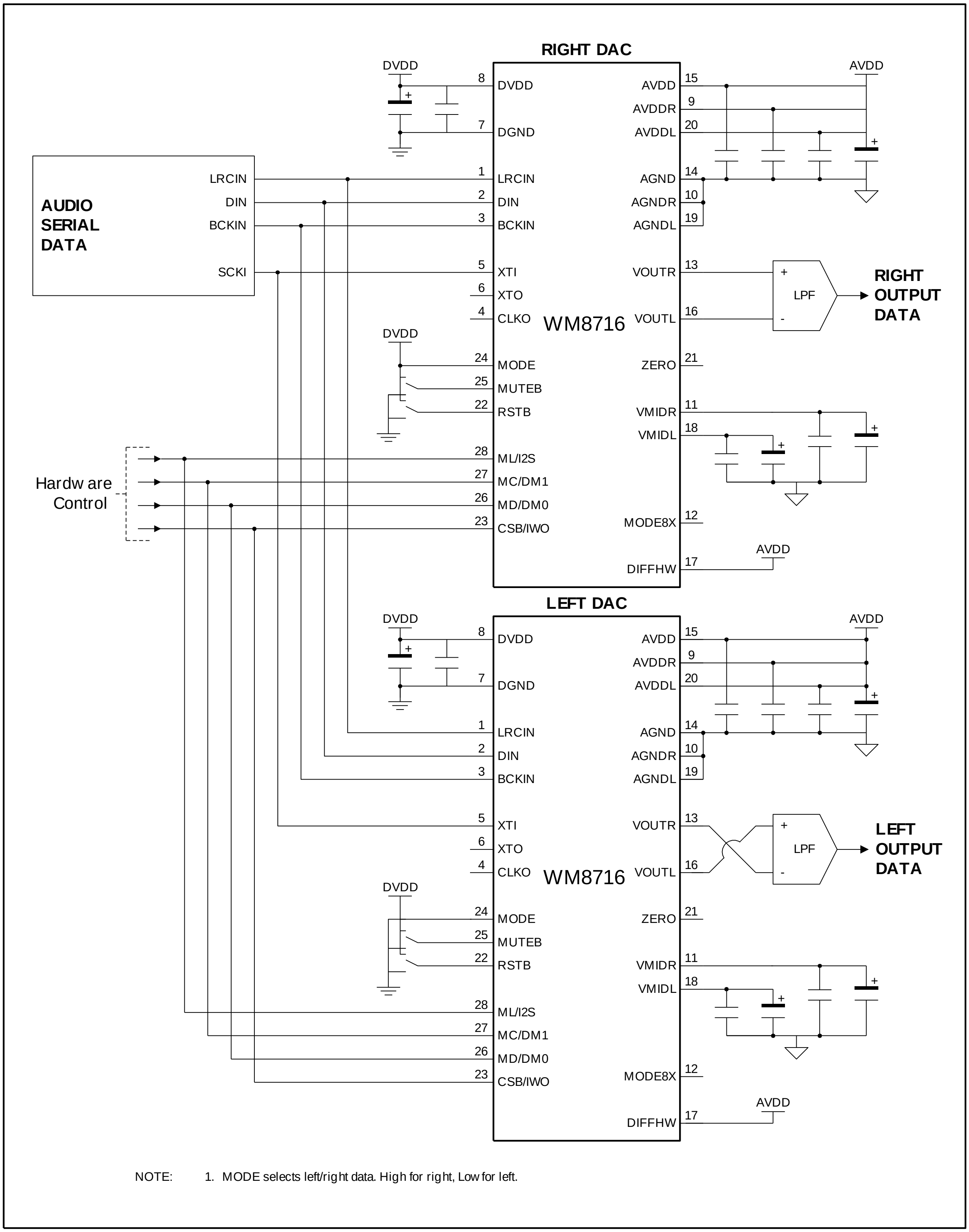


Figure 21 Example of 2 WM8716 Stereo DACs Configured in Hardware Differential Mode to Provide an Optimum Performance Stereo Output

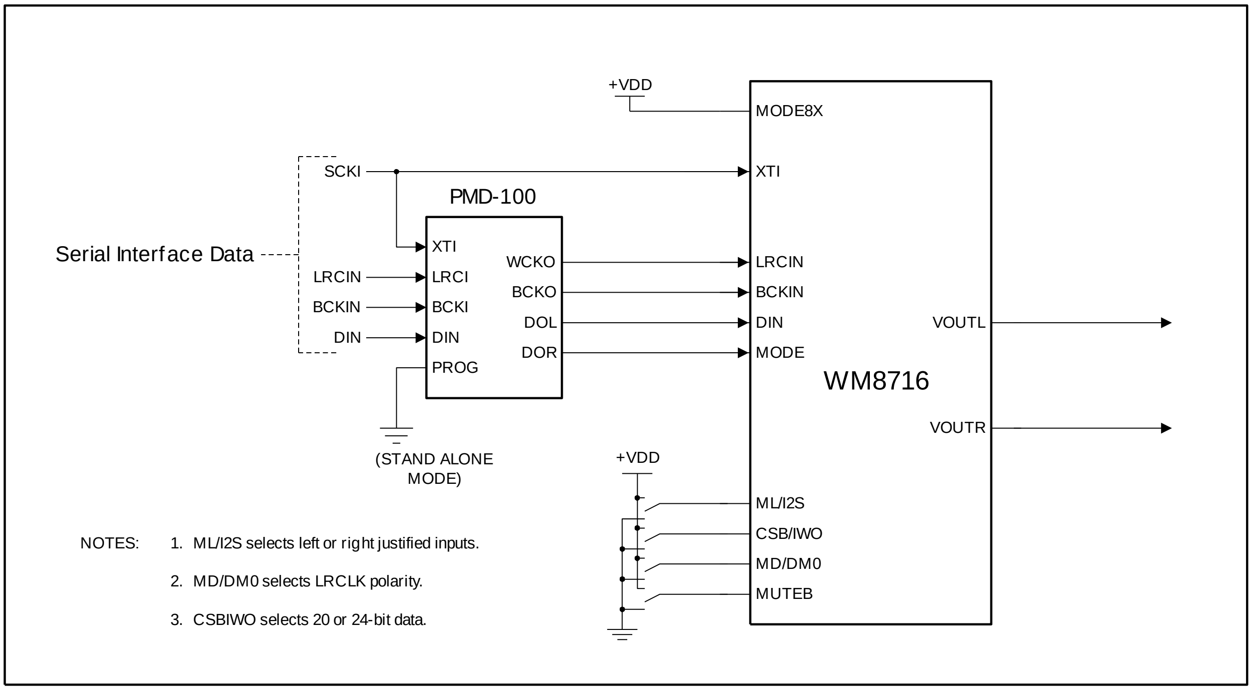
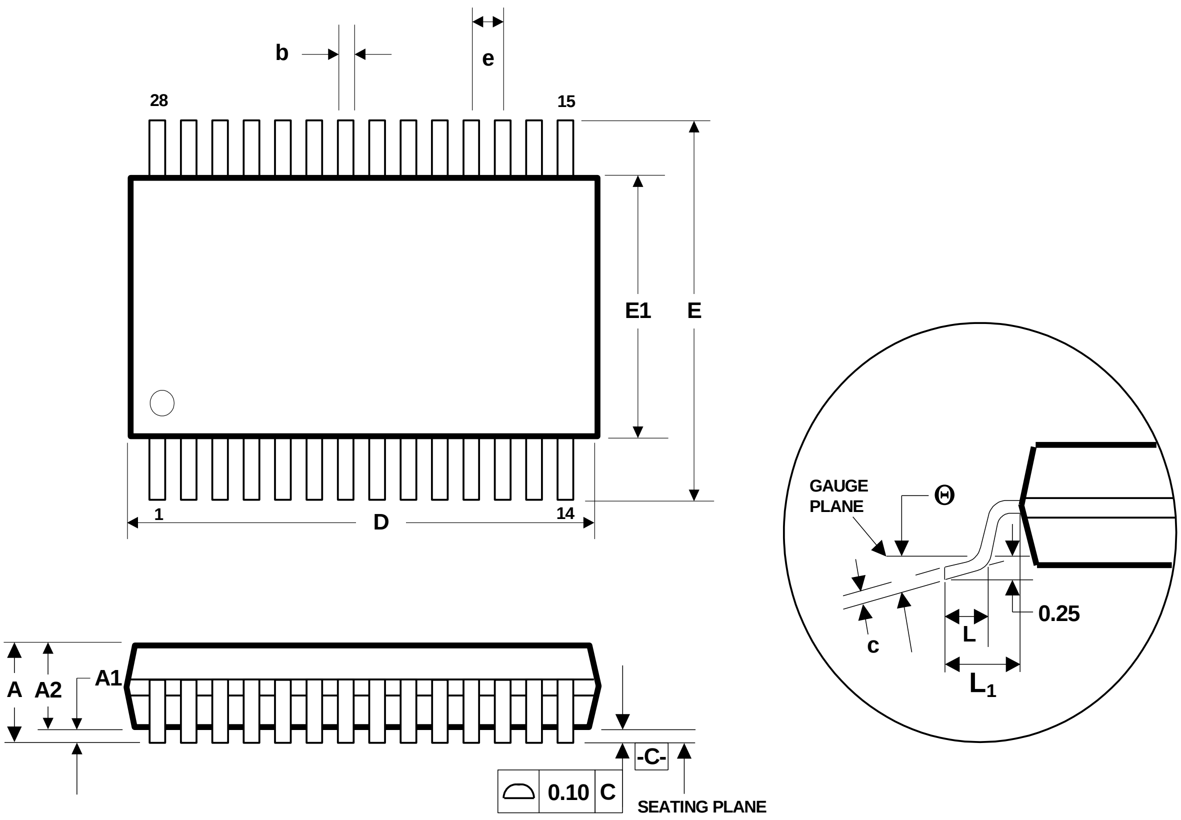


Figure 22 Example of WM8716 in MODE8X Operation

PACKAGE DIMENSIONS

DS: 28 PIN SSOP (10.2 x 5.3 x 1.75 mm) **DM007.E**



Symbols	Dimensions (mm)		
	MIN	NOM	MAX
A	-----	-----	2.0
A_1	0.05	-----	0.25
A_2	1.65	1.75	1.85
b	0.22	0.30	0.38
c	0.09	-----	0.25
D	9.90	10.20	10.50
e	0.65 BSC		
E	7.40	7.80	8.20
E_1	5.00	5.30	5.60
L	0.55	0.75	0.95
L_1	1.25 REF		
θ	0^o	4^o	8^o
REF:	JEDEC.95, MO-150		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.20MM.
D. MEETS JEDEC.95 MO-150, VARIATION = AH. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

IMPORTANT NOTICE

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com.

REVISION HISTORY

DATE	REV	ORIGINATOR	CHANGES	PAGE
13/05/04	4.0	MT	TOC added	2
			Peak Soldering Temperature added	3
			Order Codes:	
			X added to WM8716EDS/WM8716EDS/R	3
			Lead free product codes added	3
			MSL nfo added	3
			De-emphasis Filter response diagrams added	20
			Package diagram updated to DM007.D	25
27/07/06	4.1	LucyE	Updated Front page	1
			Updated footers	
			Updated ordering information- removed 2 devices and changed 28-pin to 28-lead	3
			Updated package dimensions diagram to DM007.E	25
			Updated Important Notice	26
13/09/06		CM	Voltage range digital inputs and Master clock frequency added to conditions table	4
			Changed AVDD/AVSS to DVDD/DGND in Electrical Characteristics	5
21/07/08	4.2	JMacD	Order Info: /V and /RV added to part number.	3
			MSL updated from MSL1 to MSL2	
20/01/20	4.3	PH	Ordering Information and Absolute Maximum Ratings updated – MSL information removed	3