CS5461A

Single Phase, Bi-directional Power/Energy IC

Features

- Energy Data Linearity: ±0.1% of Reading over 1000:1 Dynamic Range
- On-chip Functions:
  - Instantaneous Voltage, Current, and Power
  - I_{RMS} and V_{RMS}, Apparent and Active (Real) Power
  - Energy-to-pulse Conversion for Mechanical Counter/Stepper Motor Drive
  - System Calibrations and Phase Compensation
  - Temperature Sensor
  - Voltage Sag Detect
- Meets Accuracy Spec for IEC, ANSI, & JIS.
- Low Power Consumption
- Current Input Optimized for Sense Resistor.
- GND-referenced Signals with Single Supply
- On-chip 2.5 V Reference (25 ppm/°C typ)
- Power Supply Monitor
- Simple Three-wire Digital Serial Interface
- "Auto-boot" Mode from Serial E^2PROM.
- Power Supply Configurations:
  VA+ = +5 V; AGND = 0 V; VD+ = +3.3 V to +5 V

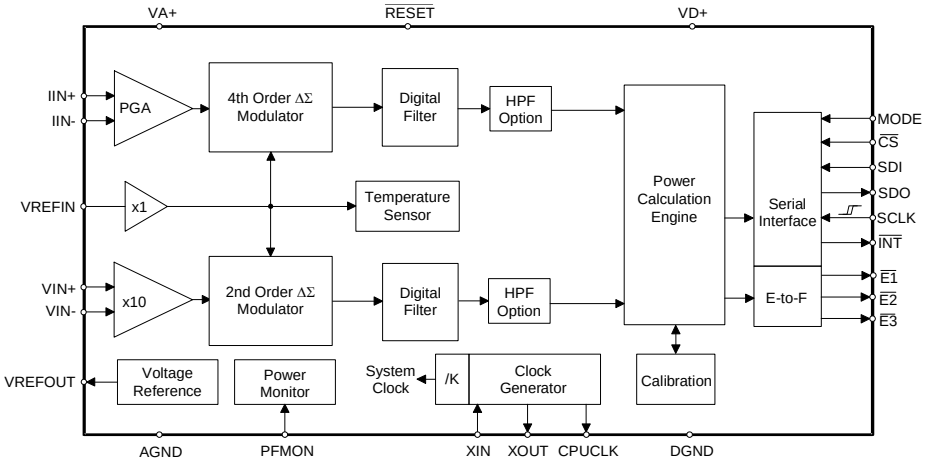
Description

The CS5461A is an integrated power measurement device which combines two ΔΣ analog-to-digital converters, power calculation engine, energy-to-frequency converter, and a serial interface on a single chip. It is designed to accurately measure instantaneous current and voltage, and calculate V_{RMS}, I_{RMS}, instantaneous power, apparent power, and active power for single-phase, 2- or 3-wire power metering applications.

The CS5461A is optimized to interface to shunt resistors or current transformers for current measurement, and to resistive dividers or potential transformers for voltage measurement.

The CS5461A features a bi-directional serial interface for communication with a processor, and a programmable energy-to-pulse output function. Additional features include on-chip functionality to facilitate system-level calibration, temperature sensor, voltage sag detection, and phase compensation.

ORDERING INFORMATION:
See Page 43.



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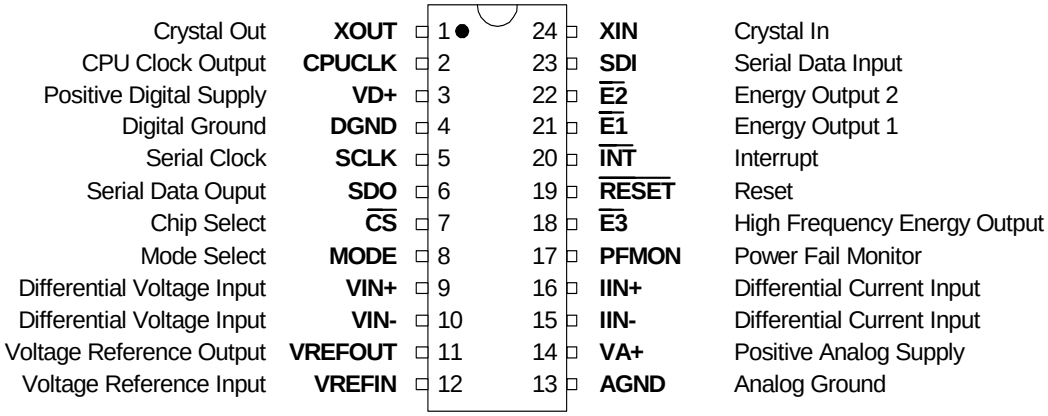
1. OVERVIEW

The CS5461A is a CMOS monolithic power measurement device with a computation engine and an energy-to-frequency pulse output. The CS5461A combines a programmable-gain amplifier, two ΔΣ analog-to-digital converters (ADCs), system calibration and a computation engine on a single chip.

The CS5461A is designed for power measurement applications and is optimized to interface to a current-sense resistor or transformer for current measurement, and to a resistive divider or potential transformer for voltage measurement. The voltage and current channels provide programmable gains to accommodate various input levels from a wide variety of sensing elements. With single +5 V supply on VA+/AGND, both of the CS5461A's input channels can accommodate common mode as well as signal levels between (AGND - 0.25 V) and VA+.

Additionally, the CS5461A is equipped with a computation engine that calculates I_{RMS}, V_{RMS}, apparent power and active (real) power. To facilitate communication to a microprocessor, the CS5461A includes a simple three-wire serial interface which is SPI™ and Microwire™ compatible. The CS5461A provides three outputs for energy registration. $\overline{E1}$ and $\overline{E2}$ are designed to directly drive a mechanical counter or stepper motor, or interface to a microprocessor. The pulse output $\overline{E3}$ is designed to assist with meter calibration.

2. PIN DESCRIPTION



Clock Generator		
Crystal Out **Crystal In**	1,24	**XOUT, XIN** - The output and input of an inverting amplifier. Oscillation occurs when connected to a crystal, providing an on-chip system clock. Alternatively, an external clock can be supplied to the XIN pin to provide the system clock for the device.
CPU Clock Output	2	**CPUCLK** - Output of on-chip oscillator which can drive one standard CMOS load.
Control Pins and Serial Data I/O		
Serial Clock Input	5	**SCLK** - A Schmitt Trigger input pin. Clocks data from the SDI pin into the receive buffer and out of the transmit buffer onto the SDO pin when $\overline{CS}$ is low.
Serial Data Output	6	**SDO** -Serial port data output pin.SDO is forced into a high impedance state when $\overline{CS}$ is high.
Chip Select	7	$\overline{\textbf{CS}}$ - Low, activates the serial port interface.
Mode Select	8	**MODE** - High, enables the “auto-boot” mode. The mode pin is pulled low by an internal resistor.
High Frequency Energy Output	18	**E3** - Active low pulses with an output frequency proportional to the active power. Used to assist in system calibration.
Reset	19	$\overline{\textbf{RESET}}$ - A Schmitt Trigger input pin. Low activates Reset, all internal registers (some of which drive output pins) are set to their default states.
Interrupt	20	$\overline{\textbf{INT}}$ - Low, indicates that an enabled event has occurred.
Energy Output	21,22	**E1,** $\overline{\textbf{E2}}$ - Active low pulses with an output frequency proportional to the active power. Indicates if the measured energy is negative.
Serial Data Input	23	**SDI** - Serial port data input pin. Data will be input at a rate determined by SCLK.
Analog Inputs/Outputs		
Differential Voltage Inputs	9,10	**VIN+, VIN-** - Differential analog input pins for the voltage channel.
Differential Current Inputs	15,16	**IIN+, IIN-** - Differential analog input pins for the current channel.
Voltage Reference Output	11	**VREFOUT** - The on-chip voltage reference output. The voltage reference has a nominal magnitude of 2.5 V and is referenced to the AGND pin on the converter.
Voltage Reference Input	12	**VREFIN** - The input to this pin establishes the voltage reference for the on-chip modulator.
Power Supply Connections		
Positive Digital Supply	3	**VD**+ - The positive digital supply.
Digital Ground	4	**DGND** - Digital Ground.
Positive Analog Supply	14	**VA+** - The positive analog supply.
Analog Ground	13	**AGND** - Analog ground.
Power Fail Monitor	17	**PFMON** - The power fail monitor pin monitors the analog supply. If PFMON’s voltage threshold is not met, a Low-Supply Detect (LSD) bit is set in the status register.

3. CHARACTERISTICS & SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Positive Digital Power Supply	VD+	3.135	5.0	5.25	V
Positive Analog Power Supply	VA+	4.75	5.0	5.25	V
Voltage Reference	VREFIN	-	2.5	-	V
Specified Temperature Range	T_A	-40	-	+85	°C

ANALOG CHARACTERISTICS

- Min / Max characteristics and specifications are guaranteed over all *Recommended Operating Conditions*.
- Typical characteristics and specifications are measured at nominal supply voltages and TA = 25 °C.
- VA+ = VD+ = 5 V ±5%; AGND = DGND = 0 V; VREFIN = +2.5 V. All voltages with respect to 0 V.
- MCLK = 4.096 MHz.

Parameter		Symbol	Min	Typ	Max	Unit
Linearity Performance						
Active Power Accuracy (All Gain Ranges) (Note 1)	Input Range 0.1% - 100%	P_{Active}	-	±0.1	-	%
Current RMS Accuracy (All Gain Ranges) (Note 1) 	Input Range 0.2% - 100% Input Range 0.1% - 0.2%	I_{RMS}	- -	±0.2 ±1.5	- -	% %
Voltage RMS Accuracy (All Gain Ranges) (Note 1)	Input Range 5% - 100%	V_{RMS}	-	±0.1	-	%
Analog Inputs (Both Channels)						
Common Mode Rejection	(DC, 50, 60 Hz)	CMRR	80	-	-	dB
Common Mode + Signal (All Gain Ranges)			-0.25	-	VA+	V
Analog Inputs (Current Channel)						
Differential Input Range [(IIN+) - (IIN-)]	(Gain = 10) (Gain = 50)	IIN	- -	500 100	- -	mV_{P-P} mV_{P-P}
Total Harmonic Distortion	(Gain = 50)	THD	80	94	-	dB
Crosstalk with Voltage Channel at Full Scale	(50, 60 Hz)		-	-115	-	dB
Input Capacitance	(Gain = 10) (Gain = 50)	IC	- -	32 52	- -	pF pF
Effective Input Impedance		EII	30	-	-	kΩ
Noise (Referred to Input)	(Gain = 10) (Gain = 50)	N_I	- -	22.5 4.5	- -	μV_{rms} μV_{rms}
Offset Drift (Without the high-pass filter)		OD	-	4.0	-	µV/°C
Gain Error	(Note 2)	GE	-	±0.4		%
Analog Inputs (Voltage Channel)						
Differential Input Range	{(VIN+) - (VIN-)}	VIN	-	500	-	mV_{P-P}
Total Harmonic Distortion		THD	65	75	-	dB
Crosstalk with Current Channel at Full Scale	(50, 60 Hz)		-	-70	-	dB
Input Capacitance	All Gain Ranges	IC	-	0.2	-	pF
Effective Input Impedance		EII	2	-	-	MΩ
Noise (Referred to Input)		N_V	-	140	-	μV_{rms}
Offset Drift (Without the high-pass Filter)		OD	-	16.0	-	µV/°C
Gain Error	(Note 2)	GE	-	±3.0		%

ANALOG CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Typ	Max	Unit
Temperature Channel					
Temperature Accuracy	T	-	±5	-	°C
Power Supplies					
Power Supply Currents (Active State) I_{A+}	PSCA	-	1.1	-	mA
I_{D+} (VA+ = VD+ = 5 V)	PSCD	-	2.9	-	mA
I_{D+} (VA+ = 5 V, VD+ = 3.3 V)	PSCD	-	1.7	-	mA
Power Consumption Active State (VA+ = VD+ = 5 V) (Note 3)	PC	-	21	28	mW
Active State (VA+ = 5 V, VD+ = 3.3 V)		-	12	16.5	mW
Stand-By State		-	8	-	mW
Sleep State		-	10	-	µW
Power Supply Rejection Ratio (DC, 50 and 60 Hz) (Note 4)					
Voltage Channel	PSRR	45	65	-	dB
Current Channel		70	75	-	dB
PFMON Low-voltage Trigger Threshold (Note 5)	PMLO	2.3	2.45	-	V
PFMON High-voltage Power-On Trip Point (Note 6)	PMHI	-	2.55	2.7	V

1. Applies when the HPF option is enabled.
2. Applies before system calibration.
3. All outputs unloaded. All inputs CMOS level.
4. Measurement method for PSRR: VREFIN tied to VREFOUT, VA+ = VD+ = 5 V, a 150 mV (zero-to-peak) (60 Hz) sinewave is imposed onto the +5 V DC supply voltage at VA+ and VD+ pins. The “+” and “-” input pins of both input channels are shorted to AGND. Then the CS5461A is commanded to continuous conversion acquisition mode, and digital output data is collected for the channel under test. The (zero-to-peak) value of the digital sinusoidal output signal is determined, and this value is converted into the (zero-to-peak) value of the sinusoidal voltage (measured in mV) that would need to be applied at the channel’s inputs, in order to cause the same digital sinusoidal output. This voltage is then defined as Veq. PSRR is then (in dB):

$$PSRR = 20 \cdot \log\left\{\frac{150}{V_{eq}}\right\}$$

5. When voltage level on PFMON is sagging, and LSD bit is at 0, the voltage at which LSD bit is set to 1.
6. If the LSD bit has been set to 1 (because PFMON voltage fell below PMLO), this is the voltage level on PFMON at which the LSD bit can be permanently reset back to 0.

VOLTAGE REFERENCE

Parameter	Symbol	Min	Typ	Max	Unit
Reference Output					
Output Voltage	VREFOUT	+2.4	+2.5	+2.6	V
Temperature Coefficient (Note 7)	TC_{VREF}	-	25	60	ppm/°C
Load Regulation (Note 8)	ΔV_R	-	6	10	mV
Reference Input					
Input Voltage Range	VREFIN	+2.4	+2.5	+2.6	V
Input Capacitance		-	4	-	pF
Input CVF Current		-	25	-	nA

Notes: 7. The voltage at VREFOUT is measured across the temperature range. From these measurements the following formula is used to calculate the VREFOUT Temperature Coefficient:.

$$TC_{VREF} = \left(\frac{(VREFOUT_{MAX} - VREFOUT_{MIN})}{VREFOUT_{AVG}}\right)\left(\frac{1}{T_{AMAX} - T_{AMIN}}\right)\left(1.0 \times 10^{6}\right)$$

8. Specified at maximum recommended output of 1 µA, source or sink.

DIGITAL CHARACTERISTICS

- Min / Max characteristics and specifications are guaranteed over all *Recommended Operating Conditions*.
- Typical characteristics and specifications are measured at nominal supply voltages and TA = 25 °C.
- VA+ = VD+ = 5V ±5%; AGND = DGND = 0 V. All voltages with respect to 0 V.
- MCLK = 4.096 MHz.

Parameter	Symbol	Min	Typ	Max	Unit
Master Clock Characteristics					
Master Clock Frequency Internal Gate Oscillator (Note 10)	MCLK	2.5	4.096	20	MHz
Master Clock Duty Cycle		40	-	60	%
CPUCLK Duty Cycle (Note 11 and 12)		40		60	%
Filter Characteristics					
Phase Compensation Range (Voltage Channel, 60 Hz)		-2.8	-	+2.8	°
Input Sampling Rate DCLK = MCLK/K		-	DCLK/8	-	Hz
Digital Filter Output Word Rate (Both Channels)	OWR	-	DCLK/1024	-	Hz
High-pass Filter Corner Frequency -3 dB		-	0.5	-	Hz
Full Scale Calibration Range (Referred to Input) (Note 13)	FSCR	25	-	100	%F.S.
Channel-to-channel Time-shift Error (Note 14)			1.0		µs
Input/Output Characteristics					
High-level Input Voltage All Pins Except XIN and SCLK and $\overline{\text{RESET}}$ XIN SCLK and $\overline{\text{RESET}}$	V_{IH}	 0.6 VD+ (VD+) - 0.5 0.8 VD+	 - - -	 - - -	 V V V
Low-level Input Voltage (VD = 5 V) All Pins Except XIN and SCLK and $\overline{\text{RESET}}$ XIN SCLK and $\overline{\text{RESET}}$	V_{IL}	 - - -	 - - -	 0.8 1.5 0.2 VD+	 V V V
Low-level Input Voltage (VD = 3.3 V) All Pins Except XIN and SCLK and $\overline{\text{RESET}}$ XIN SCLK and $\overline{\text{RESET}}$	V_{IL}	 - - -	 - - -	 0.48 0.3 0.2 VD+	 V V V
High-level Output Voltage I_{out} = +5 mA	V_{OH}	(VD+) - 1.0	-	-	V
Low-level Output Voltage I_{out} = -5 mA	V_{OL}	-	-	0.4	V
Input Leakage Current (Note 15)	I_{in}	-	±1	±10	µA
3-state Leakage Current	I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance	C_{out}	-	5	-	pF

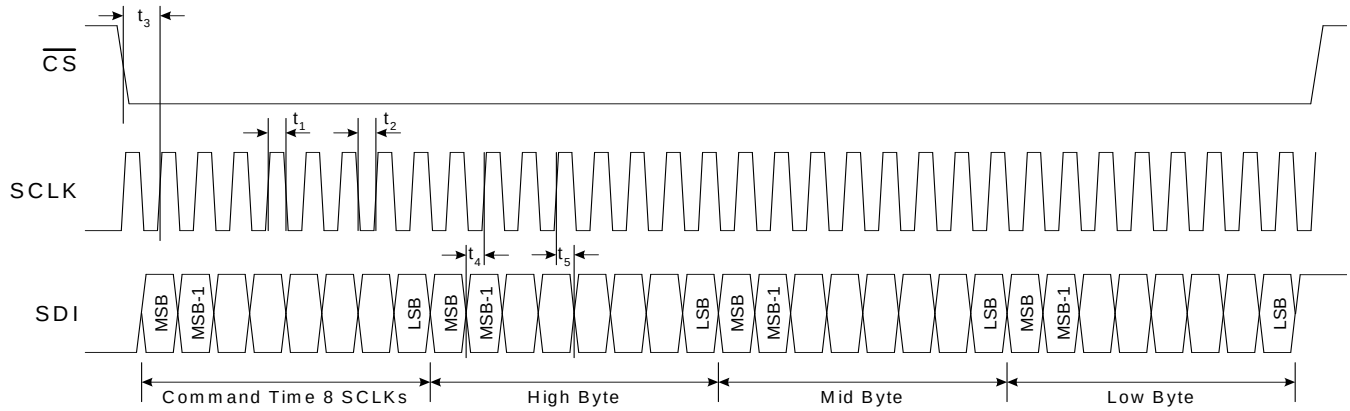
Notes:
9. All measurements performed under static conditions.
10. If a crystal is used, then XIN frequency must remain between 2.5 MHz - 5.0 MHz. If an external oscillator is used, XIN frequency range is 2.5 MHz - 20 MHz, but K must be set so that MCLK is between 2.5 MHz - 5.0 MHz.
11. If external MCLK is used, then the duty cycle must be between 45% and 55% to maintain this specification.
12. The frequency of CPUCLK is equal to MCLK.
13. The minimum FSCR is limited by the maximum allowed gain register value. The maximum FSCR is limited by the full-scale signal applied to the channel input.
14. Configuration Register bits PC[6:0] are set to “0000000”.
15. The MODE pin is pulled low by an internal resistor.

SWITCHING CHARACTERISTICS

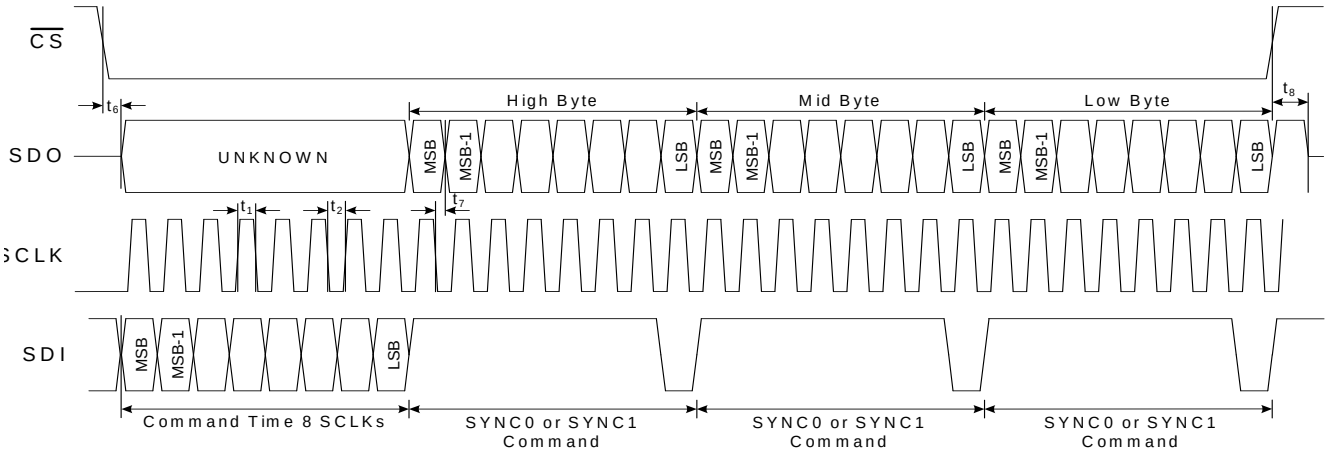
- Min / Max characteristics and specifications are guaranteed over all *Recommended Operating Conditions*.
- Typical characteristics and specifications are measured at nominal supply voltages and TA = 25 °C.
- VA+ = 5 V ±5% VD+ = 3.3 V ±5% or 5 V ±5%; AGND = DGND = 0 V. All voltages with respect to 0 V.
- Logic Levels: Logic 0 = 0 V, Logic 1 = VD+.

Parameter		Symbol	Min	Typ	Max	Unit
Rise Times (Note 16)	Any Digital Input Except SCLK SCLK Any Digital Output	t_{rise}	- - -	- - 50	1.0 100 -	µs µs ns
Fall Times (Note 16)	Any Digital Input Except SCLK SCLK Any Digital Output	t_{fall}	- - -	- - 50	1.0 100 -	µs µs ns
Start-up						
Oscillator Start-Up Time	XTAL = 4.096 MHz (Note 17)	t_{ost}	-	60	-	ms
Serial Port Timing						
Serial Clock Frequency		SCLK	-	-	2	MHz
Serial Clock	Pulse Width High Pulse Width Low	t_1 t_2	200 200	- -	- -	ns ns
SDI Timing						
$\overline{CS}$ Falling to SCLK Rising		t_3	50	-	-	ns
Data Set-up Time Prior to SCLK Rising		t_4	50	-	-	ns
Data Hold Time After SCLK Rising		t_5	100	-	-	ns
SDO Timing						
$\overline{CS}$ Falling to SDO Driving		t_6	-	20	50	ns
SCLK Falling to New Data Bit (hold time)		t_7	-	20	50	ns
$\overline{CS}$ Rising to SDO Hi-Z		t_8	-	20	50	ns
Auto-Boot Timing						
Serial Clock	Pulse Width Low Pulse Width High	t_9 t_{10}		8 8		MCLK MCLK
MODE setup time to $\overline{RESET}$ Rising		t_{11}	50			ns
$\overline{RESET}$ rising to $\overline{CS}$ falling		t_{12}	48			MCLK
$\overline{CS}$ falling to SCLK rising		t_{13}	100	8		MCLK
SCLK falling to $\overline{CS}$ rising		t_{14}		16		MCLK
$\overline{CS}$ rising to driving MODE low (to end auto-boot sequence).		t_{15}	50			ns
SDO guaranteed setup time to SCLK rising		t_{16}	100			ns

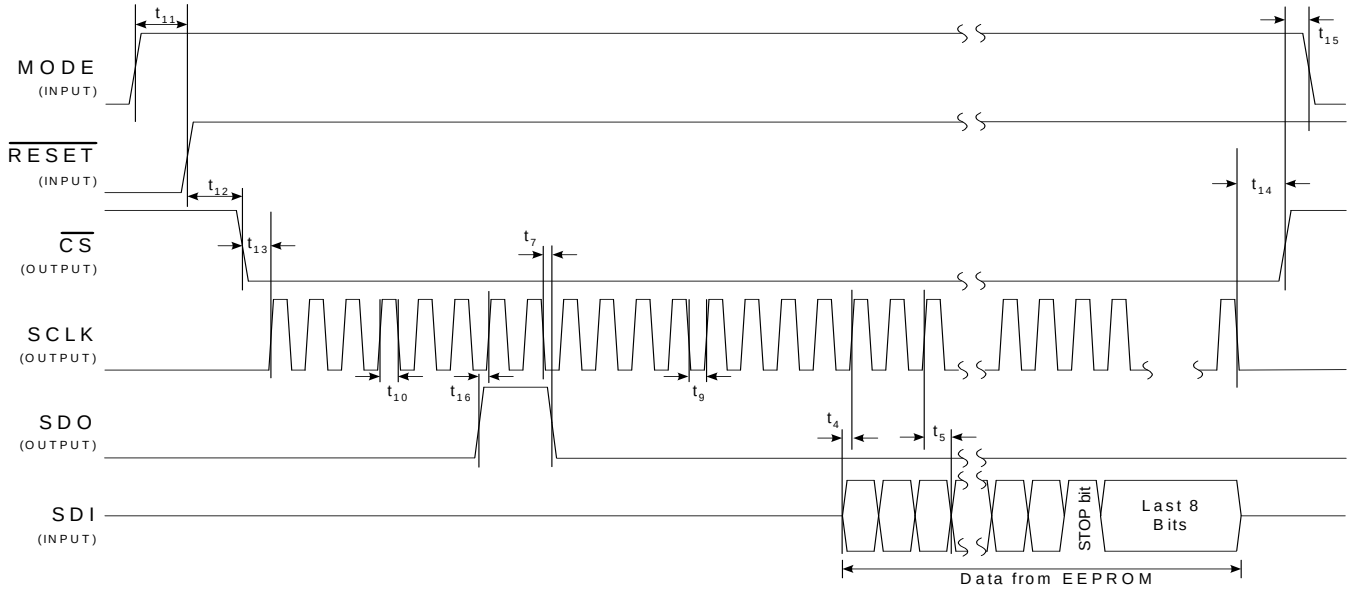
Notes: 16. Specified using 10% and 90% points on wave-form of interest. Output loaded with 50 pF.
17. Oscillator start-up time varies with crystal parameters. This specification does not apply when using an external clock source.



SDI Write Timing (Not to Scale)



SDO Read Timing (Not to Scale)



Auto-Boot Sequence Timing (Not to Scale)

Figure 1. CS5461A Read and Write Timing Diagrams

ABSOLUTE MAXIMUM RATINGS

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies	(Notes 18 and 19)					
Positive Digital		VD+	-0.3	-	+6.0	V
Positive Analog		VA+	-0.3	-	+6.0	V
Input Current, Any Pin Except Supplies	(Notes 20, 21, 22)	I_{IN}	-	-	±10	mA
Output Current, Any Pin Except VREFOUT		I_{OUT}	-	-	100	mA
Power Dissipation	(Note 23)	P_D	-	-	500	mW
Analog Input Voltage	All Analog Pins	V_{INA}	- 0.3	-	(VA+) + 0.3	V
Digital Input Voltage	All Digital Pins	V_{IND}	-0.3	-	(VD+) + 0.3	V
Ambient Operating Temperature		T_A	-40	-	85	°C
Storage Temperature		T_{stg}	-65	-	150	°C

Notes:
18. VA+ and AGND must satisfy {(VA+) - (AGND)} ≤ + 6.0 V.
19. VD+ and AGND must satisfy {(VD+) - (AGND)} ≤ + 6.0 V.
20. Applies to all pins including continuous over-voltage conditions at the analog input pins.
21. Transient current of up to 100 mA will not cause SCR latch-up.
22. Maximum DC input current for a power supply pin is ±50 mA.
23. Total power dissipation, including all input currents and output currents.

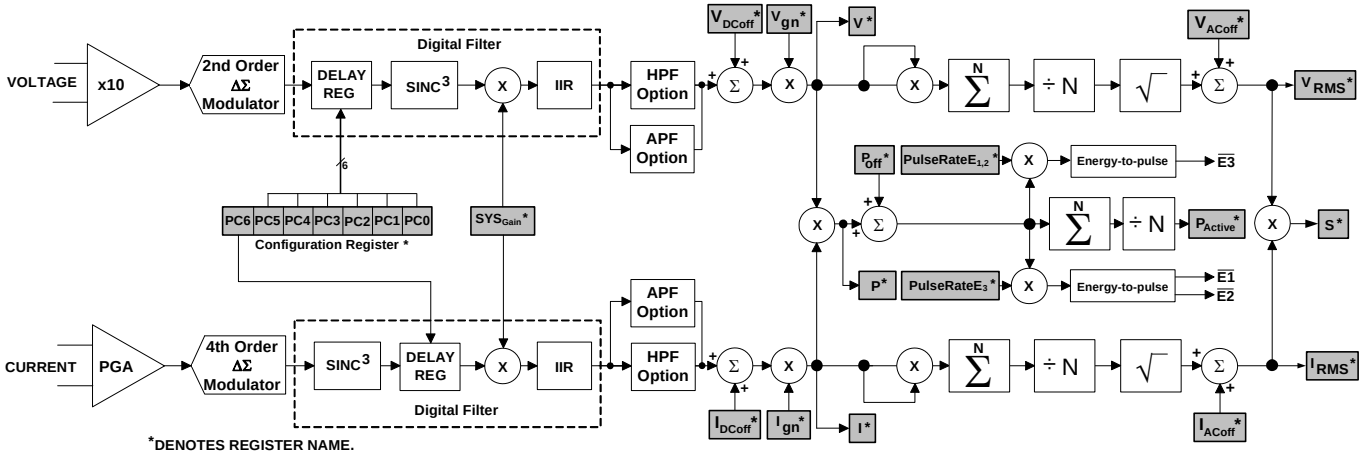


Figure 2. Data Flow.

4. THEORY OF OPERATION

The CS5461A is a dual-channel analog-to-digital converter (ADC) followed by a computation engine that performs power calculations and energy-to-pulse conversion. The flow diagram for the two data paths is depicted in Figure 2. The analog inputs are structured with two dedicated channels, voltage and current, then optimized to simplify interfacing to sensing elements.

The voltage-sensing element introduces a voltage waveform on the voltage channel input VIN± and is subject to a gain of 10x. A second-order, delta-sigma modulator samples the amplified signal for digitization.

Simultaneously, the current-sensing element introduces a voltage waveform on the current channel input IIN± and is subject to the two selectable gains of the programmable gain amplifier (PGA). The amplified signal is sampled by a fourth-order, delta-sigma modulator for digitization. Both converters sample at a rate of MCLK/8, the over-sampling provides a wide dynamic range and simplified anti-alias filter design.

4.1 Digital Filters

The decimating digital filters on both channels are $Sinc^3$ filters followed by 4th-order, IIR filters. The single-bit data is passed to the low-pass decimation filter and output at a fixed word rate. The output word is passed to the IIR filter to compensate for the magnitude roll-off of the low-pass filtering operation.

An optional digital High-pass Filter (*HPF* in Figure 2) removes any DC component from the selected signal path. By removing the DC component from the voltage and/or the current channel, any DC content will also be removed from the calculated active power as well. With both HPFs enabled, the DC component will be removed from the calculated V_{RMS} and I_{RMS} as well as the apparent power.

When the HPF option is used in only one channel, the APF (all pass filter) option can be applied to the other channel to preserve the phase match between the two channels.

4.2 Voltage and Current Measurements

The digital filter output word is then subject to a DC offset adjustment and a gain calibration (See Section 7. *System Calibration* on page 35). The calibrated measurement is available to the user by reading the instantaneous voltage and current registers.

The Root Mean Square (RMS) calculations are performed on N instantaneous voltage and current samples, V_n and I_n respectively (where N is the cycle count), using the formula:

$$I_{RMS} = \sqrt{\frac{\sum_{n=0}^{N-1} I_n}{N}}$$

and likewise for V_{RMS}, using V_n. I_{RMS} and V_{RMS} are accessible by register reads, which are updated once every cycle count (referred to as a computational cycle).

4.3 Power Measurements

The instantaneous voltage and current samples are multiplied to obtain the instantaneous power (see Figure 2). The product is then averaged over N conversions to compute active power and used to drive energy pulse outputs **E1, E2 and E3**. Output $\overline{E3}$ provides a uniform pulse stream that is proportional to the active power and is designed for system calibration.

To generate a value for the accumulated active energy over the last computation cycle, the active power can be multiplied by the time duration of the computation cycle.

The apparent power is the combination of the active power and reactive power, without reference to an impedance phase angle, and is calculated by the CS5461A using the following formula:

$$S = V_{RMS} \times I_{RMS}$$

The apparent power is registered once every computation cycle.

4.4 Linearity Performance

The linearity of the V_{RMS}, I_{RMS}, and active power measurements (before calibration) will be within ±0.1% of reading over the ranges specified, with respect to the input voltage levels required to cause full-scale readings in the I_{RMS} and V_{RMS} registers. Refer to *Linearity Performance Specifications* on page 7.

Until the CS5461A is calibrated, the *accuracy* of the CS5461A (with respect to a reference line-voltage and line-current level on the power mains) is not guaranteed to within ±0.1%. See Section 7. *System Calibration* on page 35. The accuracy of the internal calculations can often be improved by selecting a value for the *Cycle Count Register* that will cause the time duration of one computation cycle to be equal to (or very close to) a whole-number of power-line cycles (and N must be greater than or equal to 4000).

5. FUNCTIONAL DESCRIPTION

5.1 Analog Inputs

The CS5461A is equipped with two fully differential input channels. The inputs VIN± and IIN± are designated as the voltage and current channel inputs, respectively. The full-scale differential input voltage for the current and voltage channel is ±250 mV_P.

5.1.1 Voltage Channel

The output of the line-voltage resistive divider or transformer is connected to the VIN+ and VIN- input pins of the CS5461A. The voltage channel is equipped with a 10x, fixed-gain amplifier. The full-scale signal level that can be applied to the voltage channel is ±250 mV. If the input signal is a sine wave the maximum RMS voltage at a gain 10x is:

$$\frac{250mV_P}{\sqrt{2}} \cong 176.78mV_{RMS}$$

which is approximately 70.7% of maximum peak voltage. The voltage channel is also equipped with a *Voltage Gain Register*, allowing for an additional programmable gain of up to 4x.

5.1.2 Current Channel

The output of the current-sense resistor or transformer is connected to the IIN+ and IIN- input pins of the CS5461A. To accommodate different current-sensing elements, the current channel incorporates a Programmable Gain Amplifier (PGA) with two programmable input gains. *Configuration Register* bit Igain (See Table 1) defines the two gain selections and corresponding maximum input-signal level.

Igain	Maximum Input Range	
0	±250 mV	10x
1	±50 mV	50x

Table 1. Current Channel PGA Configuration

For example, if Igain=0, the current channel's PGA gain is set to 10x. If the input signals are pure sinusoids with zero phase shift, the maximum peak differential signal on the current or voltage channel is ±250 mV_P. The input-signal levels are approximately 70.7% of maximum peak voltage producing a full-scale energy pulse registration equal to 50% of absolute maximum energy pulse registration. This will be discussed further in Section 5.4 *Energy Pulse Output* on page 16.

The *Current Gain Register* also allows for an additional programmable gain of up to 4x. If an additional gain is applied to the voltage and/or current channel, the maximum input range should be adjusted accordingly.

5.2 High-pass Filters

By removing the offset from either channel, no error component will be generated at DC when computing the active power. By removing the offset from both channels, no error component will be generated at DC when computing V_{RMS}, I_{RMS}, and apparent power. *Configuration Register* bits VHPF and IHPF activate the HPF in the voltage and current channel respectively.

5.3 Performing Measurements

The CS5461A performs measurements of instantaneous voltage (V_n) and current (I_n), and calculates instantaneous power (P_n) at an Output Word Rate (OWR) of

$$OWR = \frac{(MCLK/K)}{1024}$$

where K is the clock divider setting in the *Configuration Register*.

The RMS voltage (V_{RMS}), RMS current (I_{RMS}), and active power (P_{Active}) are computed using N instantaneous samples of V_n, I_n and P_n respectively, where N is the value in the *Cycle Count Register* (N) and is referred to as a *"computation cycle"*. The apparent power (S) is the product of V_{RMS} and I_{RMS}. A computation cycle is derived from the master clock (MCLK), with frequency:

$$\text{Computation Cycle} = \frac{OWR}{N}$$

Under default conditions & with K = 1, N = 4000, and MCLK = 4.096 MHz – the OWR = 4000 Hz and the Computation Cycle = 1 Hz.

All measurements are available as a percentage of full scale. The format for *signed* registers is a two's complement, normalized value between -1 and +1. The format for *unsigned* registers is a normalized value between 0 and 1. A register value of

$$\frac{(2^{23}-1)}{2^{23}} = 0.99999988$$

represents the maximum possible value.

At each instantaneous measurement, the CRDY bit will be set (logic 1) in the *Status Register*, and the $\overline{INT}$ pin will become active if the CRDY bit is unmasked in the *Mask Register*. At the end of each computation cycle, the DRDY bit will be set in the *Status Register*, and the

$\overline{INT}$ pin will become active if the DRDY bit is unmasked in the *Mask Register*. When these bits are set, they must be cleared (logic 0) by the user before they can be asserted again.

If the *Cycle Count Register* (N) is set to 1, all output calculations are instantaneous, and DRDY, like CRDY, will indicate when instantaneous measurements are finished. Some calculations are inhibited when the cycle count is less than 2.

5.4 Energy Pulse Output

The CS5461A provides three output pins for energy registration. The $\overline{E1}$ and $\overline{E2}$ pins provide a simple interface which energy can be registered. These pins are designed to directly connect to a stepper motor or electromechanical counter. $\overline{E1}$ and $\overline{E2}$ pins can be set to one of four pulse output formats, Normal, Alternate, Stepper Motor, or Mechanical Counter. Table 2 defines the pulse output format, which is controlled by bits ALT in the *Configuration Register*, and MECH and STEP in the *Control Register.*

ALT	STEP	MECH	FORMAT
0	0	0	Normal
0	X	1	Mechanical Counter
0	1	0	Stepper Motor
1	X	1	Alternate Pulse

Table 2. E1 and E2 Pulse Output Format

The $\overline{E3}$ pin is designated for system calibration, the pulse rate can be selected to reach a frequency of 512 kHz.

The pulse output frequency of $\overline{E1}$ and $\overline{E2}$ is directly proportional to the active power calculated from the input signals. To calculate the output frequency on $\overline{E1}$ and $\overline{E2}$, the following transfer function can be utilized:

$$FREQ_E = \frac{VIN \times VGAIN \times IIN \times IGAIN \times PF \times PulseRateE_{1,2}}{VREFIN^2}$$

$FREQ_E$ = Average frequency of $\overline{E1}$ and $\overline{E2}$ pulses [Hz]
VIN = rms voltage across VIN+ and VIN- [V]
VGAIN = Voltage channel gain
IIN = rms voltage across IIN+ and IIN- [V]
IGAIN = Current channel gain
PF = Power Factor
$PulseRateE_{1,2}$ = Maximum frequency on $\overline{E1}$ and $\overline{E2}$ [Hz]
VREFIN = Voltage at VREFIN pin [V]

With MCLK = 4.096 MHz, PF = 1, and default settings, the pulses will have an average frequency equal to the frequency setting in the *$PulseRateE_{1,2}$ Register* when the input signals applied to the voltage and current channels cause full-scale readings in the instantaneous voltage and current registers. When MCLK/K is not equal to 4.096 MHz, the user should scale the *$PulseRateE_{1,2}$ Register* by a factor of 4.096 MHz/(MCLK/K) to get the actual pulse rate output.

5.4.1 Normal Format

The Normal format is the default. Figure 3 illustrates the output format on pins $\overline{E1}$ and $\overline{E2}$. The $\overline{E1}$ pin outputs active-low pulses with a frequency proportional to the active power. The $\overline{E2}$ pin is the energy direction indicator. Positive energy is represented by a pulse on the $\overline{E1}$ pin while the $\overline{E2}$ pin remains high. Negative energy is represented by synchronous pulses on both the $\overline{E1}$ pin and the $\overline{E2}$ pin.

The *$PulseRateE_{1,2}$ Register* defines the average frequency on output pin $\overline{E1}$, when full-scale input signals are applied to the voltage and current channels. The maximum pulse frequency from the $\overline{E1}$ pin

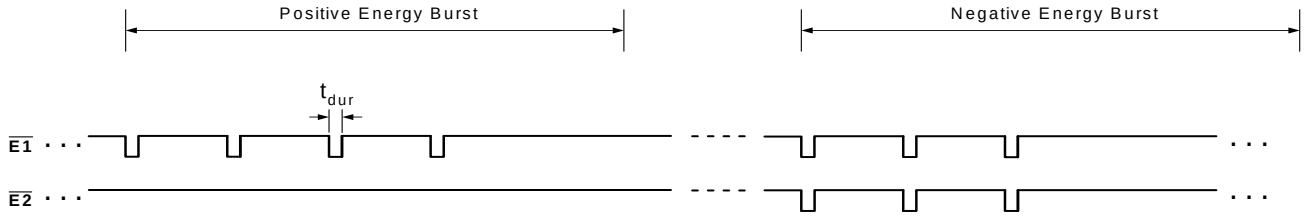


Figure 3. Normal Format on pulse outputs E1 and E2

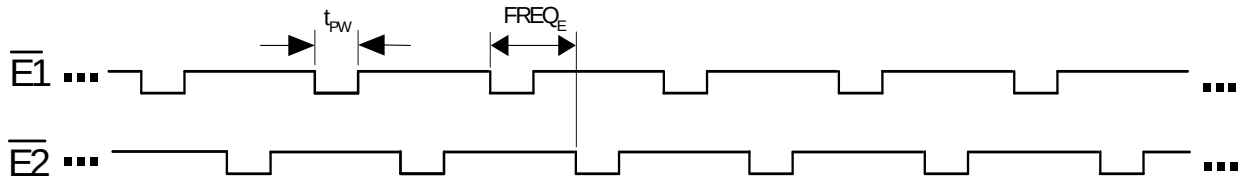


Figure 4. Alternate Pulse Format on E1 and E2

is (MCLK/K)/16. The pulse duration (t_{dur}) is an integer multiple of MCLK cycles, approximately equal to:

$$t_{dur}(sec) \cong \frac{1}{PulseRateE_{1,2} \times 8}$$

The maximum pulse duration (t_{dur}) is determined by the sampling rate and the minimum is defined by the maximum pulse frequency. The t_{dur} limits are:

$$\frac{1}{(MCLK/K)/16 \times 8} < t_{dur}(sec) < \frac{1}{(MCLK/K)/1024 \times 8}$$

The *Pulse Width Register* (PW) does not affect the normal format.

5.4.2 Alternate Pulse Format

Setting bits MECH = 1 and STEP = 0 in the *Control Register* and ALT = 1 in the *Configuration Register* configures the $\overline{E1}$ and $\overline{E2}$ pins for alternating pulse format output (see Figure 4). Each pin produces alternating active-low pulses with a pulse duration (t_{PW}) defined by the *Pulse Width Register* (PW):

$$t_{PW}(ms) = \frac{PW}{(MCLK/K)/1024}$$

If MCLK = 4.096 MHz, K = 1, and PW = 1 then t_{PW} = 0.25 ms. To ensure that pulses occur on the $\overline{E1}$ and $\overline{E2}$ output pins when full-scale input signals are applied to the voltage and current channels, then:

$$PulseRateE_{1,2} < \frac{1}{t_{PW}}$$

The pulse frequency ($FREQ_E$) is determined by the *PulseRateE$_{1,2}$ Register* and can be calculated using the transfer function. The energy direction is not defined in the alternate pulse format.

5.4.3 Mechanical Counter Format

Setting bits MECH = 1 and STEP = 0 in the *Control Register* and bit ALT = 0 in the *Configuration Register* enables $\overline{E1}$ and $\overline{E2}$ for mechanical counters and similar discrete counting instruments. When energy is negative, pulses appear on $\overline{E2}$ (see Figure 5). When energy is positive, the pulses appear on $\overline{E1}$. The pulse width is defined by the *Pulsewidth Register* and will limit the output pulse frequency ($FREQ_E$). By default, PW = 512 samples, if MCLK = 4.096 MHz and K = 1 then t_{PW} = 128 ms. To ensure that pulses will occur, the *PulseRateE$_{1,2}$ Register* must be set to an appropriate value.

5.4.4 Stepper Motor Format

Setting bits STEP = 1 and MECH = 0 in the *Control Register* and bit ALT = 0 in the *Configuration Register* configures the $\overline{E1}$ and $\overline{E2}$ pins for stepper motor format. When the accumulated active power equals the defined

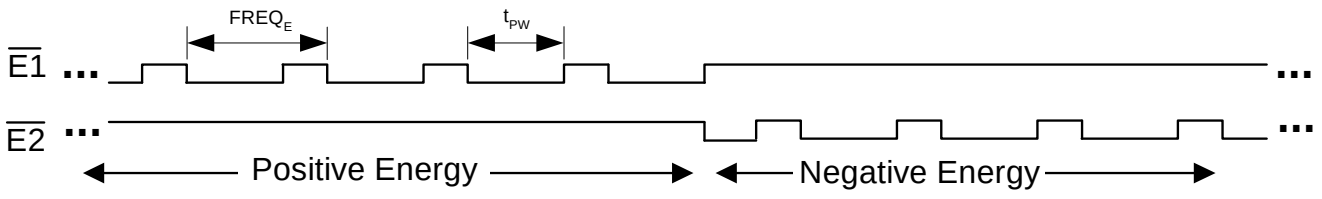


Figure 5. Mechanical Counter Format on E1 and E2

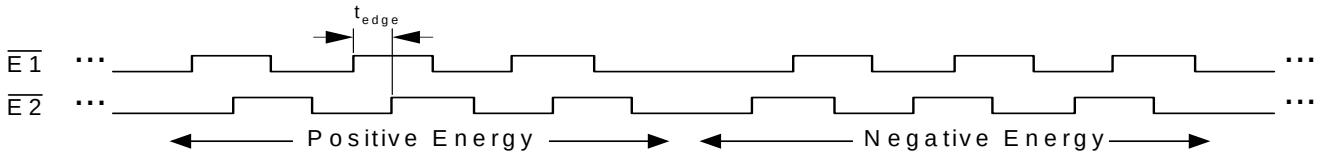


Figure 6. Stepper Motor Format on E1 and E2

energy level, the energy output pins ($\overline{E1}$ and $\overline{E2}$) alternate changing states (see Figure 6). The duration (t_{edge}) between the alternating states is defined by the transfer function:

$$t_{edge}(sec) = \frac{1}{FREQ_E}$$

The direction the motor will rotate is determined by the order of the state changes. When energy is positive, $\overline{E1}$ will lead $\overline{E2}$. When energy is negative, $\overline{E2}$ will lead $\overline{E1}$. The *Pulse Width Register* (PW) does not affect the stepper motor format.

5.4.5 Pulse Output $\overline{E3}$

The pulse output $\overline{E3}$ is designed to assist with meter calibration. The pulse-output frequency of $\overline{E3}$ is directly proportional to the active power calculated from the input signals. $\overline{E3}$ pulse frequency is derived using a simular transfer function as $\overline{E1}$, but is set by the value in the *PulseRateE$_3$ Register*.

The $\overline{E3}$ pin outputs negative and positive energy, but has no energy direction indicator.

The pulse width of $\overline{E3}$ is configurable. The *PulseWidth* register defines the pulse width of $\overline{E3}$ in units of 1/OWR or:

$$t_{pw} = \frac{PulseWidth}{((MCLK)/K)/1024}$$

The default value is 0.

5.4.6 Anti-creep for the Pulse Outputs

Anti-creep allows the measurement element to maintain an energy level, such that when the magnitude of the accumulated active power is below this level, no energy pulses are output. Anti-creep is enabled by setting bit FAC in the *Control Register* for $\overline{E3}$ and bit EAC in the *Control Register* for $\overline{E1}$ and $\overline{E2}$.

For low-frequency pulse output formats (i.e. mechanical counter and stepper motor formats), the active power is accumulated over time. When a designated energy level is reached (determined by the transfer function) a pulse is generated on $\overline{E1}$ and/or $\overline{E2}$. If active power with alternating polarity occurs during the accumulation period (e.g. random noise at zero power levels), the accuracy of the registered energy will be maintained.

For high-frequency pulse output formats (i.e. normal and alternate pulse formats), the active power is accumulated over time until a ±8x buffer is defined. Then, when the designated energy level is reached, a pulse is generated on $\overline{E1}$ and/or $\overline{E2}$. For pulse outputs with high frequencies and power levels close to zero, the extended buffer prevents random noise from being registered as active energy.

5.4.7 Design Examples

EXAMPLE #1:

The maximum rated levels for a power line meter are 250 V rms and 20 A rms. The required number of pulses per second on $\overline{E1}$ is 100 pulses per second (100 Hz), when the levels on the power line are 220 V rms and 15 A rms.

With a 10x gain on the voltage and current channel the maximum input signal is 250 mV$_P$ (see Section 5.1 *Analog Inputs* on page 15). To prevent over-driving the channel inputs, the maximum rated rms input levels will register 0.6 in V_{RMS} and I_{RMS} by design. Therefore the voltage level at the channel inputs will be 150 mV rms when the maximum rated levels on the power lines are 250 V rms and 20 A rms.

Solving for PulseRateE$_{1,2}$ using the transfer function:

$$PulseRateE_{1,2} = \frac{FREQ_E \times VREFIN^2}{VIN \times VGAIN \times IIN \times PF}$$

Therefore with PF = 1 and

$$VIN = 220V \times ((150mV)/(250V)) = 132mV$$

$$IIN = 15A \times ((150mV)/(20A)) = 112.5mV$$

the *PulseRateE$_{1,2}$ Register* is set to:

$$PulseRateE = \frac{100 \times 2.5^2}{0.132 \times 10 \times 0.1125 \times 10} = 420.8754Hz$$

EXAMPLE #2:

The required number of pulses per unit energy present on $\overline{E1}$ is specified to be 500 pulses per kWhr, given that the line voltage is 250 Vrms and the line current is 20 Arms. In such a situation, the stated line voltage and current do not determine the appropriate $PulseRateE_{1,2}$ setting. To achieve full-scale readings in the instantaneous voltage and current registers, a 250 mV, DC-level signal is applied to the channel inputs.

As in example #1, the voltage and current channel gains are 10x, and the voltage level at the channel inputs will be 150 mV rms when the levels on the power lines are 250 V rms and 20 A rms. In order to achieve 500 pulse-per-kW Hr per unit-energy, the *PulseRateE$_{1,2}$ Register* setting is determined using the following equation:

$$PulseRateE_{1,2} = \frac{500pulses}{kWHr} \times \frac{1Hr}{3600s} \times \frac{1kW}{1000W} \times \frac{250mV}{\left(\frac{150mV}{250V}\right)} \times \frac{250mV}{\left(\frac{150mV}{20A}\right)}$$

Therefor, the *PulseRateE$_{1,2}$ Register* is approximately 1.929 Hz. The *PulseRateE$_{1,2}$ Register* cannot be set to a frequency of exactly 1.929 Hz. The closest setting is 0x00003E = 1.9375 Hz.

To improve the accuracy, either gain register can be programmed to correct for the round-off error. This value would be calculated as

$$Vgn \text{ or } Ign = \frac{PulseRateE}{1.929} \cong 1.00441 = 0x404830$$

If (MCLK/K) is not equal to 4.096 MHz, the *PulseRateE$_{1,2}$ Register* must be scaled by a correction factor of:

$$\frac{4.096MHz}{(MCLK/K)} \times PulseRateE_{1,2}$$

Therefore if (MCLK/K) = 3.05856 MHz the value of *PulseRateE$_{1,2}$ Register* is

$$PulseRateE_{1,2} = \frac{4.096}{3.05856} \times 1.929Hz \cong 2.583Hz$$

5.5 Voltage Sag-detect Feature

Status bit VSAG in the *Status Register,* indicates a voltage sag occurred in the power line voltage. For a voltage sag condition to be identified, the absolute value of the instantaneous voltage must be less than the voltage sag level for more than half of the voltage sag duration (see Figure 7).

To activate Voltage Sag detect, a voltage sag level must be specified in the *Voltage Sag Level Register* (VSAGLevel), and a voltage sag duration must be specified in the *Voltage Sag Duration Register* (VSAGDuration). The voltage sag level is specified as the average of the absolute instantaneous voltage. Voltage sag duration is specified in terms of ADC cycles.

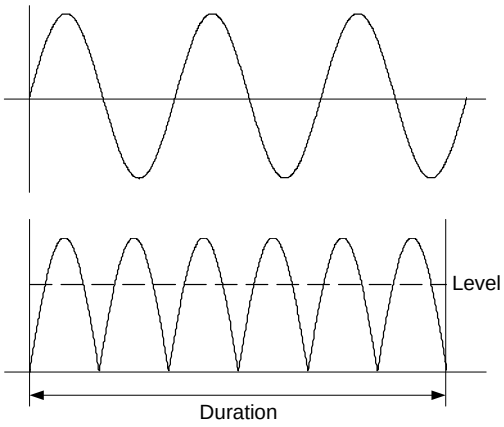


Figure 7. Voltage Sag Detect

5.6 No Load Threshold

The CS5461A includes the *LoadIntv* (No Load Detection Interval) register and the *LoadMin* register to implement the no load threshold function. When the accumulated energy measured within the time defined by the *LoadIntv* register does not reach the value in the *LoadMin* register, the pulse outputs will be disabled.

5.7 On-chip Temperature Sensor

The on-chip temperature sensor is designed to assist in characterizing the measurement element over a desired temperature range. Once a temperature characterization is performed, the temperature sensor can then be utilized to assist in compensating for temperature drift.

Temperature measurements are performed during continuous conversions and stored in the *Temperature Register*. The *Temperature Register* (T) default is Celsius scale (^{o}C). The *Temperature Gain Register* (T_{gain}) and *Temperature Offset Register* (T_{off}) are constant values allowing for temperature scale conversions.

The temperature update rate is a function of the number of ADC samples. With MCLK = 4.096 MHz and K = 1 the update rate is:

$$\frac{2240 \text{ samples}}{(MCLK/K)/1024} = 0.56 \text{ sec}$$

The *Cycle Count Register* (N) must be set to a value greater than one. Status bit TUP in the *Status Register,* indicates when the *Temperature Register* is updated.

The *Temperature Offset Register* sets the zero-degree measurement. To improve temperature measurement accuracy, the zero-degree offset should be adjusted after the CS5461A is initialized. Temperature offset calibration is achieved by adjusting the *Temperature Offset Register* (T_{off}) by the differential temperature (ΔT) measured from a calibrated digital thermometer and the CS5461A temperature sensor. A one-degree adjustment to the *Temperature Register* (T) is achieved by adding 2.737649×10^{-4} to the *Temperature Offset Register* (T_{off}). Therefore,

$$T_{off} = T_{off} + (\Delta T \times 2.737649 \cdot 10^{-4})$$

if T_{off} = -0.0951126 and ΔT = -2.0 (^{o}C), then

$$T_{off} = -0.0951126 + (-2.0 \times 2.737649 \cdot 10^{-4}) = -0.09566$$

or 0xF3C168 (2's compliment notation) is stored in the *Temperature Offset Register* (T_{off}).

To convert the *Temperature Register* (T) from a Celsius scale (^{o}C) to a Fahrenheit scale (^{o}F) utilize the formula

$$^{o}F = \frac{9}{5}(^{o}C + 17.7778)$$

Applying the above relationship to the CS5461A temperature measurement algorithm

$$T\langle^{o}F\rangle = (\frac{9}{5} \times T_{gain})[T\langle^{o}C\rangle + (T_{off} + (17.7778 \times 2.737649 \cdot 10^{-4}))]$$

If T_{off} = -0.09566 and T_{gain} = 23.507 for a Celsius scale, then the modified values are T_{off} = -0.0907935 (0xF460E1) and T_{gain} = 42.3132 (0x54A05E) for a Fahrenheit scale.

5.8 Voltage Reference

The CS5461A is specified for operation with a +2.5 V reference between the VREFIN and AGND pins. To utilize the on-chip 2.5 V reference, connect the VREFOUT pin to the VREFIN pin of the device. The VREFIN pin can be used to connect external filtering and/or references.

5.9 System Initialization

Upon powering up, the digital circuitry is held in reset until the analog voltage reaches 4.0 V. At that time, an eight-XIN-clock-period delay is enabled to allow the oscillator to stabilize. The CS5461A will then initialize.

A hardware reset is initiated when the $\overline{\text{RESET}}$ pin is asserted with a minimum pulse width of 50 ns. The $\overline{\text{RESET}}$ signal is asynchronous, with a Schmitt-trigger input. Once the $\overline{\text{RESET}}$ pin is de-asserted, an eight-XIN-clock-period delay is enabled.

A software reset is initiated by writing the command of 0x80. After a hardware or software reset, the internal registers (some of which drive output pins) will be reset to their *default* values. Status bit DRDY in the *Status Register,* indicates the CS5461A is in its *active* state and ready to receive commands.

5.10 Power-down States

The CS5461A has two power-down states, stand-by and sleep. In the stand-by state all circuitry except the voltage reference and crystal oscillator is turned off. To return the device to the active state a power-up command is sent to the device.

In sleep state all circuitry except the instruction decoder is turned off. When the power-up command is sent to the device, a system initialization is performed (see Section 5.9 *System Initialization* on page 20).

5.11 Oscillator Characteristics

The XIN and XOUT pins are the input and output of an inverting amplifier configured as an on-chip oscillator, as shown in Figure 8. The oscillator circuit is designed

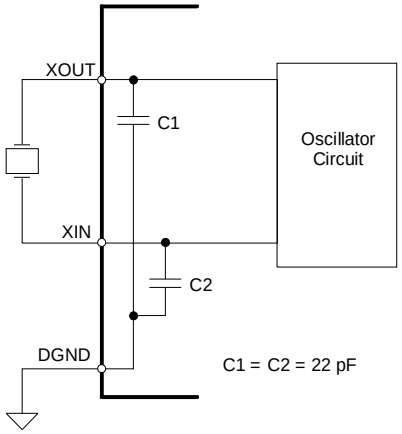


Figure 8. Oscillator Connection

to work with a quartz crystal. To reduce circuit cost, two load capacitors C1 and C2 are integrated in the device, from XIN to DGND, and XOUT to DGND. PCB trace lengths should be minimized to reduce stray capacitance. To drive the device from an external clock source, XOUT should be left unconnected while XIN is driven by the external circuitry. There is an amplifier between XIN and the digital section which provides CMOS-level signals. This amplifier works with sinusoi-

dal inputs so there are no problems with slow edge times.

The CS5461A can be driven by an external oscillator ranging from 2.5 to 20 MHz, but the K divider value must be set such that the internal MCLK will run somewhere between 2.5 MHz and 5 MHz. The K divider value is set with the K[3:0] bits in the *Configuration Register*. As an example, if XIN = MCLK = 15 MHz, and K is set to 5, then DCLK is 3 MHz, which is a valid value for DCLK.

5.12 Event Handler

The $\overline{\text{INT}}$ pin is used to indicate that an internal error or event has taken place in the CS5461A. Writing a logic 1 to any bit in the *Mask Register* allows the corresponding bit in the *Status Register* to activate the $\overline{\text{INT}}$ pin. The interrupt condition is cleared by writing a logic 1 to the bit that has been set in the *Status Register*.

The behavior of the $\overline{\text{INT}}$ pin is controlled by the IMODE and IINV bits of the *Configuration Register*.

IMODE	IINV	$\overline{\text{INT}}$ Pin
0	0	Active-low Level
0	1	Active-high Level
1	0	Low Pulse

Table 3. Interrupt Configuration

IMODE	IINV	$\overline{\text{INT}}$ Pin
1	1	High Pulse

Table 3. Interrupt Configuration

If the interrupt output signal format is set for either falling or rising edge, the duration of the $\overline{\text{INT}}$ pulse will be at least one DCLK cycle (DCLK = MCLK/K).

5.12.1 Typical Interrupt Handler

The steps below show how interrupts can be handled.

INITIALIZATION:

1) All Status bits are cleared by writing 0xFFFFFF to the Status Register.
2) The condition bits which will be used to generate interrupts are then set to logic 1 in the Mask Register.
3) Enable interrupts.

INTERRUPT HANDLER ROUTINE:

4) Read the Status Register.
5) Disable all interrupts.
6) Branch to the proper interrupt service routine.
7) Clear the Status Register by writing back the read value in step 4.
8) Re-enable interrupts.
9) Return from interrupt service routine.

5.13 Serial Port Overview

The CS5461A incorporates a serial port transmit and receive buffer with a command decoder that interprets one-byte (8 bits) commands as they are received. There are four types of commands; instructions, synchronizing, register writes and register reads (See Section 5.14 *Commands* on page 23).

Instructions are one byte in length and will interrupt any instruction currently executing. Instructions do not affect register reads currently being transmitted.

Synchronizing commands are one byte in length and only affect the serial interface. Synchronizing commands do not affect operations currently in progress.

Register writes must be followed by three bytes of data. register reads can return up to four bytes of data.

Commands and data are transferred most-significant bit (MSB) first. Figure 1 on page 11, defines the serial port timing and required sequence necessary to write to and read from the serial port receive and transmit buffer, respectively. While reading data from the serial port, commands and data can be simultaneously written. Starting a new register read command while data is being read will terminate the current read in progress. This is acceptable if the remainder of the current read data is not needed. During data reads, the serial port requires input data. If a new command and data is not sent, SYNC0 or SYNC1 must be sent.

5.13.1 Serial Port Interface

The serial port interface is a “4-wire” synchronous serial communications interface. The interface is enabled to start excepting SCLKs when $\overline{CS}$ (Chip Select) is asserted. SCLK (Serial bit-clock) is a Schmitt-trigger input that is used to strobe the data on SDI (Serial Data In) into the receive buffer and out of the transmit buffer onto SDO (Serial Data Out).

If the serial port interface becomes unsynchronized with respect to the SCLK input, any attempt to clock valid commands into the serial interface may result in unexpected operation. The serial port interface must then be re-initialized by one of the following actions:

- Drive the $\overline{CS}$ pin high, then low.
- Hardware Reset (drive $\overline{RESET}$ pin low, for at least 10 µs).
- Issue the *Serial Port Initialization Sequence*, which is 3 (or more) SYNC1 command bytes (0xFF) followed by one SYNC0 command byte (0xFE).

If a resynchronization is necessary, it is best to re-initialize the part either by hardware or software reset (0x80), as the state of the part may be unknown.

5.14 Commands

All commands are 8-bits in length. Any byte that is not listed in this section is invalid. Commands that write to registers must be followed by 3 bytes of data. Commands that read data can be chained with other commands (e.g., while reading data, a new command can be sent which can execute during the original read). All commands except register reads, register writes, and SYNC0 & SYNC1 will abort any currently executing commands.

5.14.1 Start Conversions

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	0	C3	C2	0	0

Initiates acquiring measurements and calculating results. The device has three modes of acquisition.

C[3:2] Modes of acquisition/measurement
00 = Perform a single computation cycle
01 = Not Used
10 = Perform continuous computation cycles
11 = Perform continuous computation cycles with APF enabled on the other channel

5.14.2 SYNC0 and SYNC1

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	1	1	1	1	SYNC

The serial port can be initialized by asserting $\overline{CS}$ or by sending three or more consecutive SYNC1 commands followed by a SYNC0 command. The SYNC0 or SYNC1 can also be sent while sending data out.

SYNC 0 = Last byte of a serial port re-initialization sequence.
1 = Used during reads and serial port initialization.

5.14.3 Power-Up/Halt

B7	B6	B5	B4	B3	B2	B1	B0
1	0	1	0	0	0	0	0

If the device is powered-down, Power-Up/Halt will initiate a power on reset. If the part is already powered-on, all computations will be halted.

5.14.4 Power-down and Software Reset

B7	B6	B5	B4	B3	B2	B1	B0
1	0	0	S1	S0	0	0	0

To conserve power the CS5461A has two power-down states. In stand-by state all circuitry, except the analog/digital clock generators, is turned off. In the sleep state all circuitry, except the instruction decoder, is turned off. Bringing the CS5461A out of sleep state requires more time than out of stand-by state, because of the extra time needed to re-start and re-stabilize the analog oscillator.

S[1:0] Power-down state
00 = Software Reset
01 = Halt and enter stand-by power saving state. This state allows quick power-on
10 = Halt and enter sleep power saving state.
11 = Reserved

5.14.5 Register Read/Write

B7	B6	B5	B4	B3	B2	B1	B0
0	W/R	RA4	RA3	RA2	RA1	RA0	0

The Read/Write informs the command decoder that a register access is required. During a read operation, the addressed register is loaded into an output buffer and clocked out by SCLK. During a write operation, the data is clocked into an input buffer and transferred to the addressed register upon completion of the 24th SCLK.

W/$\overline{R}$ Write/Read control
0 = Read
1 = Write

RA[4:0] Register address bits (bits 5 through 1) of the read/write command.

Address	RA[4:0]	Name	Description
0	00000	Config	Configuration
1	00001	I_{DCoff}	Current DC Offset
2	00010	I_{gn}	Current Gain
3	00011	V_{DCoff}	Voltage DC Offset
4	00100	V_{gn}	Voltage Gain
5	00101	Cycle Count	Number of A/D conversions used in one computation cycle (N)).
6	00110	$PulseRateE_{1,2}$	Sets the $\overline{E1}$ and $\overline{E2}$ energy-to-frequency output pulse rate.
7	00111	I	Instantaneous Current
8	01000	V	Instantaneous Voltage
9	01001	P	Instantaneous Power
10	01010	P_{Active}	Active (Real) Power
11	01011	I_{RMS}	RMS Current
12	01100	V_{RMS}	RMS Voltage
14	01110	P_{off}	Power Offset
15	01111	Status	Status
16	10000	I_{ACoff}	Current AC (RMS) Offset
17	10001	V_{ACoff}	Voltage AC (RMS) Offset
18	10010	$PulseRateE_3$	Sets the $\overline{E3}$ energy-to-frequency output pulse rate.
19	10011	T	Temperature
20	10100	SYS_{Gain}	System Gain
21	10101	PW	Pulse width register for mechanical counter output mode
22	10110	PulseWidth	Pulse width register for $\overline{E3}$ energy pulse output
23	10111	$VSAG_{Duration}$	Voltage Sag Duration
24	11000	$VSAG_{Level}$	Voltage Sag Level Threshold
25	11001	LoadIntv	No load threshold interval (detection window)
26	11010	Mask	Interrupt Mask
27	11011	LoadMin	No Load Threshold
28	11100	Ctrl	Control
29	11101	T_{Gain}	Temperature Sensor Gain
30	11110	T_{off}	Temperature Sensor Offset
31	11111	S	Apparent Power

Note: For proper operation, *do not* attempt to write to unspecified registers.

5.14.6 Calibration

B7	B6	B5	B4	B3	B2	B1	B0
1	1	0	CAL4	CAL3	CAL2	CAL1	CAL0

The CS5461A can perform system calibrations. Proper input signals must be applied to the current and voltage channel before performing a designated calibration.

CAL[4:0]* Designates calibration to be performed
- 01001 = Current channel DC offset
- 01010 = Current channel DC gain
- 01101 = Current channel AC offset
- 01110 = Current channel AC gain
- 10001 = Voltage channel DC offset
- 10010 = Voltage channel DC gain
- 10101 = Voltage channel AC offset
- 10110 = Voltage channel AC gain
- 11001 = Current and Voltage channel DC offset
- 11010 = Current and Voltage channel DC gain
- 11101 = Current and Voltage channel AC offset
- 11110 = Current and Voltage channel AC gain

*Values for CAL[4:0] not specified should not be used.

6. REGISTER DESCRIPTION

1. “Default” => bit status after power-on or reset
2. Any bit not labeled is Reserved. A zero should always be used when writing to one of these bits.

6.1 Configuration Register

Address: 0

23	22	21	20	19	18	17	16
PC6	PC5	PC4	PC3	PC2	PC1	PC0	Igain
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
EWA			IMODE	IINV	EPP	EOP	EDP
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ALT	VHPF	IHPF	iCPU	K3	K2	K1	K0

Default = 0x000001

PC[6:0] Phase compensation. A 2’s complement number which sets a delay in the voltage channel relative to the current channel. When MCLK = 4.096 MHz and K = 1, the phase adjustment range is approximately ±2.8 degrees with each step approximately 0.04 degrees (assuming a power line frequency of 60 Hz). If (MCLK/K) is not 4.096 MHz, the values for the range and step size should be scaled by the factor 4.096 MHz / (MCLK/K). Default setting is 0000000 = 0.0215 degree phase delay at 60 Hz (when MCLK = 4.096 MHz).

Igain Sets the gain of the current PGA.
0 = Gain is 10x (default)
1 = Gain is 50x

EWA Allows the $\overline{E1}$ and $\overline{E2}$ pins to be configured as open-collector output pins.
0 = Normal outputs (default)
1 = Only the pull-down device of the $\overline{E1}$ and $\overline{E2}$ pins are active

IMODE, IINV Interrupt configuration bits. Select the desired pin behavior for indication of an interrupt.
00 = Active-low level (default)
01 = Active-high level
10 = High-to-low pulse
11 = Low-to-high pulse

EPP Allows the $\overline{E1}$ and $\overline{E2}$ pins to be controlled by the EOP and EDP bits.
0 = Normal operation of the $\overline{E1}$ and $\overline{E2}$ pins. (default)
1 = EOP and EDP bits defines the $\overline{E1}$ and $\overline{E2}$ pins.

EOP EOP defines the value of the $\overline{E1}$ pin when EPP = 1.
0 = Logic level low (default)

EDP EDP defines the value of the $\overline{E2}$ pin when EPP = 1.
0 = Logic level low (default)

ALT Alternate pulse format, $\overline{E1}$ and $\overline{E2}$ becomes active low alternating pulses with an output frequency proportional to the active power.
0 = Normal (default), Mechanical Counter or Stepper Motor Format
1 = Alternate Pulse Format, also MECH = 1

VHPF (IHPF) Enables the high-pass filter on the voltage (current) channel.
0 = High-pass filter disabled (default)
1 = High-pass filter enabled

iCPU — Inverts the CPUCLK clock. In order to reduce the level of noise present when analog signals are sampled, the logic driven by CPUCLK should not be active during the sample edge.
0 = Normal operation (default)
1 = Minimize noise when CPUCLK is driving rising-edge logic

K[3:0] — Clock divider. A 4-bit binary number used to divide the value of MCLK to generate the internal clock DCLK. The internal clock frequency is DCLK = MCLK/K. The value of K can range between 1 and 16. A value of "0000" will set K to 16 (not zero). K = 1 at reset.

6.2 Current and Voltage DC Offset Register (I_{DCoff}, V_{DCoff})

Address: 1 (Current DC Offset); 3 (Voltage DC Offset)

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0x000000

The DC Offset registers (I_{DCoff},V_{DCoff}) are initialized to 0.0 on reset. When DC Offset calibration is performed, the register is updated with the DC offset measured over a computation cycle. DRDY will be asserted at the end of the calibration. This register may be read and stored for future system offset compensation. The value is represented in two's complement notation and in the range of $-1.0 \le I_{DCoff}, V_{DCoff} < 1.0$, with the binary point to the right of the MSB.

6.3 Current and Voltage Gain Register (I_{gn}, V_{gn})

Address: 2 (Current Gain); 4 (Voltage Gain)

MSB															LSB
2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	.....	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}

Default = 0x400000 = 1.000

The gain registers (I_{gn},V_{gn}) are initialized to 1.0 on reset. When either a AC or DC Gain calibration is performed, the register is updated with the gain measured over a computation cycle. DRDY will be asserted at the end of the calibration. This register may be read and stored for future system gain compensation. The value is in the range $0.0 \le I_{gn}, V_{gn} < 3.9999$, with the binary point to the right of the second MSB.

6.4 Cycle Count Register

Address: 5

MSB															LSB
2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	.....	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Default = 0x000FA0 = 4000

Cycle Count, denoted as N, determines the length of one *computation cycle*. During continuous conversions, the computation cycle frequency is (MCLK/K)/(1024∗N). A one second computational cycle period occurs when MCLK = 4.096 MHz, K = 1, and N = 4000.

6.5 PulseRateE$_{1,2}$ Register

Address: 6

MSB															LSB
2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	.....	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}

Default = 0xFA000 = 32000.00 Hz

PulseRateE$_{1,2}$ sets the frequency of the $\overline{E1}$ and/or $\overline{E2}$ pulses. The smallest valid frequency is 2^{-4} with 2^{-5} incremental steps. A pulse rate higher than (MCLK/K)/8 will result in a pulse rate setting of (MCLK/K)/8. The value is represented in unsigned notation, with the binary point to the right of bit 5.

6.6 Instantaneous Current, Voltage and Power Registers (I , V , P)

Address: 7 (Instantaneous Current); 8 (Instantaneous Voltage); 9 (Instantaneous Power)

MSB															LSB
$-(2^{0})$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

I and V contain the instantaneous measured values for current and voltage, respectively. The instantaneous voltage and current samples are multiplied to obtain Instantaneous Power (P). The value is represented in two's complement notation and in the range of $-1.0 \le I, V, P < 1.0$, with the binary point to the right of the MSB.

6.7 Active (Real) Power Registers (P_{Active})

Address: 10

MSB															LSB
$-(2^{0})$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

The instantaneous power is averaged over each computation cycle (N conversions) to compute Active Power (P_{Active}). The value is represented in two's complement notation and in the range of $-1.0 \le P_{Active} < 1.0$, with the binary point to the right of the MSB.

6.8 I_{RMS} and V_{RMS} Registers (I_{RMS} , V_{RMS})

Address: 11 (I_{RMS}); 12 (V_{RMS})

MSB															LSB
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	.....	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}

I_{RMS} and V_{RMS} contain the Root Mean Square (RMS) value of I and V, calculated over each computation cycle. The value is represented in unsigned binary notation and in the range of $0.0 \le I_{RMS}, V_{RMS} < 1.0$, with the binary point to the left of the MSB.

6.9 Power Offset Register (P_{off})

Address: 14

MSB															LSB
$-(2^{0})$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0x000000

Power Offset (P_{off}) is added to the instantaneous power being accumulated in the P_{active} register and can be used to offset contributions to the energy result that are caused by undesirable sources of energy that are inherent in the system. The value is represented in two's complement notation and in the range of $-1.0 \le P_{off} < 1.0$, with the binary point to the right of the MSB.

6.10 Status Register and Mask Register (Status , Mask)

Address: *15* (*Status*)*; 26 (Mask)*

23	22	21	20	19	18	17	16
DRDY			CRDY			IOR	VOR
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	IROR	VROR	EOR				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TUP	TOD		VOD	IOD	LSD	VSAG	$\overline{IC}$

Default = 0x000001 (Status Register), 0x000000 (Mask Register)

The Status Register indicates status within the chip. In normal operation, writing a '1' to a bit will cause the bit to reset. Writing a '0' to a bit will not change it's current state.

The Mask Register is used to control the activation of the $\overline{INT}$ pin. Placing a logic '1' in a Mask bit will allow the corresponding bit in the Status Register to activate the $\overline{INT}$ pin when the status bit is asserted.

DRDY — Data Ready. During conversions, this bit will indicate the end of computation cycles. For calibrations, this bit indicates the end of a calibration sequence.

CRDY — Conversion Ready. Indicates a new conversion is ready. This will occur at the output word rate.

IOR — Current Out of Range. Set when the *Instantaneous Current Register* overflows.

VOR — Voltage Out of Range. Set when the *Instantaneous Voltage Register* overflows.

IROR — I_{RMS} Out of Range. Set when the I_{RMS} *Register* overflows.

VROR — V_{RMS} Out of Range. Set when the V_{RMS} *Register* overflows.

EOR — Energy Out of Range. Set when P_{ACTIVE} overflows.

TUP — Temperature Updated. Indicates the *Temperature Register* has updated.

TOD — Modulator oscillation detected on the temperature channel. Set when the modulator oscillates due to an input above full scale.

VOD (IOD) — Modulator oscillation detected on the voltage (current) channel. Set when the modulator oscillates due to an input above full scale. The level at which the modulator oscillates is significantly higher than the voltage (current) channel's differential input voltage range.

Note: The IOD and VOD bits may be 'falsely' triggered by very brief voltage spikes from the power line. This event should not be confused with a DC overload situation at the inputs, when the IOD and VOD bits will re-assert themselves even after being cleared, multiple times.

LSD — Low Supply Detect. Set when the voltage at the PFMON pin falls below the low-voltage threshold (PMLO), with respect to AGND pin. The LSD bit cannot be reset until the voltage at PFMON pin rises back above the high-voltage threshold (PMHI).

VSAG — Indicates a voltage sag has occurred. See Section 5.5 *Voltage Sag-detect Feature* on page 19.

$\overline{IC}$ — Invalid Command. Normally logic 1. Set to logic 0 if an invalid command is received or the *Status Register* has not been successfully read.

6.11 Current and Voltage AC Offset Register (V_{ACoff} , I_{ACoff})

Address: 16 (Current AC Offset); 17 (Voltage AC Offset)

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0x000000

The AC Offset Registers (V_{ACoff}, I_{ACoff}) are initialized to zero on reset, allowing for uncalibrated normal operation. AC Offset Calibration updates these registers. This sequence lasts approximately (6N + 30) ADC cycles (where N is the value of the *Cycle Count Register*). DRDY will be asserted at the end of the calibration. These values may be read and stored for future system AC offset compensation. The value is represented in two's complement notation and in the range of $-1.0 \le V_{ACoff}, I_{ACoff} < 1.0$, with the binary point to the right of the MSB.

6.12 PulseRateE_3 Register

Address: 18

MSB															LSB
2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	.....	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}

Default = 0xFA0000 = 32000.00 Hz

PulseRateE_3 sets the frequency of the $\overline{E3}$ pulses. The register's smallest valid frequency is 2^{-4} with 2^{-5} incremental steps. A pulse rate higher than (MCLK/K)/8 will result in a pulse rate setting of (MCLK/K)/8. The value is represented in unsigned notation, with the binary point to the right of bit #5.

6.13 Temperature Register (T)

Address: 19

MSB															LSB
$-(2^7)$	2^6	2^5	2^4	2^3	2^2	2^1	2^0	.....	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}

T contains measurements from the on-chip temperature sensor. Measurements are performed during continuous conversions, with the default the Celsius scale (^oC). The value is represented in two's complement notation and in the range of $-128.0 \le T < 128.0$, with the binary point to the right of the eighth MSB.

6.14 System Gain Register (SYS_{Gain})

Address: 20

MSB															LSB
$-(2^1)$	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	.....	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}

Default = 0x500000 = 1.25

System Gain (SYS_{Gain}) determines the one's density of the channel measurements. Small changes in the modulator due to temperature can be fine adjusted by changing the system gain. The value is represented in two's complement notation and in the range of $-2.0 < SYS_{Gain} < 2.0$, with the binary point to the right of the second MSB.

6.15 Pulsewidth Register (PW)

Address: 21

MSB															LSB
2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	.....	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Default = 0x000200 = 512 sample periods

PW sets the pulsewidth of $\overline{E1}$ and $\overline{E2}$ pulses in Alternate Pulse and Mechanical Counter format. The width is a function of number of sample periods. The default corresponds to a pulsewidth of 512 samples/[(MCLK/K)/1024] = 128 msec with MCLK = 4.096 MHz and K = 1. The value is represented in unsigned notation.

6.16 E3 Pulse Width Register (PulseWidth)

Address: 22

MSB															LSB
0	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	.....	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Default = 0x000000 = Hardware-generated pulse width (up to 125 μs)

The PulseWidth register sets the pulse width of $\overline{E3}$ pulses in units of 1/OWR.

$\overline{E3}$ pulse width = $\frac{\text{PulseWidth}}{((\text{MCLK})/\text{K})/1024}$

The range of this register is from 1 to 8388607.

6.17 Voltage Sag Duration Register ($VSAG_{Duration}$)

Address: 23

MSB															LSB
0	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	.....	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Default = 0x000000

Voltage Sag Duration ($VSAG_{Duration}$) defines the number of instantaneous voltage measurements utilized to determine a voltage level sag event ($VSAG_{LEVEL}$). Setting this register to zero will disable Voltage Sag-detect. The value is represented in unsigned notation.

6.18 Voltage Sag Level Register ($VSAG_{Level}$)

Address: 24

MSB															LSB
0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0x000000

Voltage Sag Level ($VSAG_{Level}$) defines the voltage level that the magnitude of input samples, averaged over the sag duration, must fall below in order to register a sag condition. This value is represented in unsigned notation and in the range of $0 \le VSAG_{Level} < 1.0$, with the binary point to the right of the MSB.

6.19 No Load Threshold Interval Register (LoadIntv)

Address: 25

MSB															LSB
2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	.....	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Default = 0x000000 = No load threshold feature disabled

LoadMin determines the duration or interval of the no load detection window in units of 1/OWR. The range is from 1 to 16777215.

6.20 No Load Threshold (LoadMin)

Address: 27

MSB															LSB
$-(2^{0})$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0x000000 = No load threshold feature disabled

LoadMin sets the no load threshold value. LoadMin is a two's complement value in the range of $-1.0 \leq \text{LoadMin} < 1.0$ with the binary point to the right of the MSB. Negative values are not allowed.

6.21 Control Register

Register Address: 28

23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
					FAC	EAC	STOP
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	MECH		INTOD		NOCPU	NOOSC	STEP

Default = 0x000000

FAC — Determines if anti-creep is enabled for pulse output **E3**.
0 = Disable anti-creep (default)
1 = Enabled anti-creep

EAC — Determines if anti-creep is enabled for pulse output **E1 and/or E2**.
0 = Disable anti-creep (default)
1 = Enabled anti-creep

STOP — Terminates the auto-boot sequence.
0 = Normal (default)
1 = Stop sequence

MECH — Mechanical Counter Format, $\overline{E1}$ or $\overline{E2}$ becomes active low pulses with an output frequency proportional to the active power
0 = Normal (default) or Stepper Motor Format
1 = Mechanical Counter Format, also ALT = 0

INTOD — Converts **INT** output pin to an open drain output.
0 = Normal (default)
1 = Open drain

NOCPU — Saves power by disabling the CPUCLK pin.
0 = Normal (default)
1 = Disables CPUCLK

NOOSC — Saves power by disabling the crystal oscillator.
0 = Normal (default)
1 = Oscillator circuit disabled

STEP — Stepper Motor Format, $\overline{E1}$ and $\overline{E2}$ becomes active low pulses with an output frequency proportional to the active power
0 = Normal Format (default)
1 = Stepper Motor Format, also MECH = 0 and ALT = 0

6.22 Temperature Gain Register (T_{Gain})

Address: 29

MSB															**LSB**
2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}	.....	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}

Default = 0x2F02C3 = 23.5073471

Sets the temperature channel gain. Temperature gain (T_{Gain}) is utilized to convert from one temperature scale to another. The Celsius scale (^oC) is the default. Values are represented in unsigned notation and in the range of $0 \le T_{Gain} < 128$, with the binary point to the right of the seventh MSB.

6.23 Temperature Offset Register (T_{off})

Address: 30

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default = 0xF3D35A = -0.0951126

Temperature offset (T_{off}) is used to remove the temperature channel's offset at the zero degree reading. Values are represented in two's complement notation and in the range of $-1.0 \leq T_{off} < 1.0$, with the binary point to the right of the MSB.

6.24 Apparent Power Register (S)

Address: 31

MSB															LSB
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	.....	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}

Apparent power (S) is the product of the V_{RMS} and I_{RMS}. The value is represented in unsigned binary notation and in the range of $0.0 \leq S < 1.0$, with the binary point to the left of the MSB.

7. SYSTEM CALIBRATION

7.1 Channel Offset and Gain Calibration

The CS5461A provides digital DC offset and gain compensation that can be applied to the instantaneous voltage and current measurements, and AC offset compensation to the voltage and current RMS calculations.

Since the voltage and current channels have independent offset and gain registers, system offset and/or gain can be performed on either channel without the calibration results from one channel affecting the other.

The computational flow of the calibration sequences are illustrated in Figure 9. The flow applies to both the voltage channel and current channel.

7.1.1 Calibration Sequence

The CS5461A must be operating in its active state and ready to accept valid commands. Refer to Section 5.14 *Commands* on page 23. The calibration algorithms are dependent on the value N in the *Cycle Count Register* (see Figure 9). Upon completion, the results of the calibration are available in their corresponding register. The DRDY bit in the *Status Register* will be set. If the DRDY bit is to be output on the $\overline{\text{INT}}$ pin, then DRDY bit in the *Mask Register* must be set. The initial values stored in the AC gain and offset registers do affect the calibration results.

7.1.1.1 Duration of Calibration Sequence

The value of the *Cycle Count Register* (N) determines the number of conversions performed by the CS5461A during a given calibration sequence. For DC offset and gain calibrations, the calibration sequence takes at least N + 30 conversion cycles to complete. For AC offset calibrations, the sequence takes at least 6N + 30 ADC cycles to complete, (about 6 computation cycles). As N is increased, the accuracy of calibration results will increase.

7.1.2 Offset Calibration Sequence

For DC- and AC offset calibrations, the VIN± pins of the voltage and IIN± pins of the current channels should be connected to their ground-reference level.
See Figure 10.

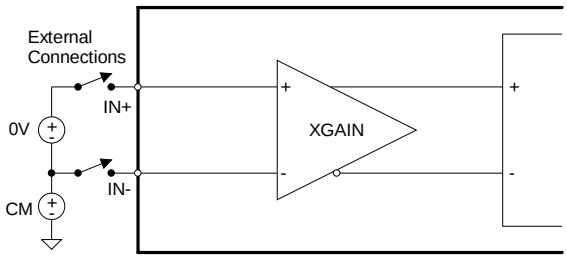


Figure 10. System Calibration of Offset.

The AC offset registers must be set to the default (0x000000).

7.1.2.1 DC Offset Calibration Sequence

Channel gain should be set to 1.0 when performing DC offset calibration. Initiate a DC offset calibration. The DC offset registers are updated with the negative of the average of the instantaneous samples taken over a computational cycle. Upon completion of the DC offset calibration the DC offset is stored in the corresponding DC offset register. The DC offset value will be added to each instantaneous measurement to cancel out the DC

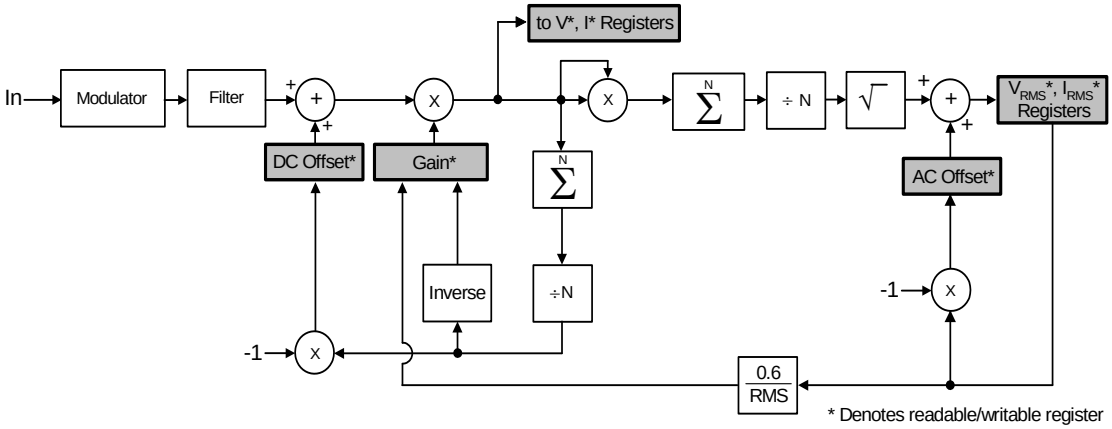


Figure 9. Calibration Data Flow

component present in the system during conversion commands.

7.1.2.2 AC Offset Calibration Sequence

Corresponding offset registers I_{ACoff} and/or V_{ACoff} should be cleared prior to initiating AC offset calibrations. Initiate an AC offset calibration. The AC offset registers are updated with an offset value that reflects the RMS output level. Upon completion of the AC offset calibration the AC offset is stored in the corresponding AC offset register. The AC offset register value is subtracted from each successive V_{RMS} and I_{RMS} calculation.

7.1.3 Gain Calibration Sequence

When performing gain calibrations, a reference signal should be applied to the VIN± pins of the voltage and IIN± pins of the current channels that represents the desired maximum signal level. Figure 11 shows the basic setup for gain calibration.

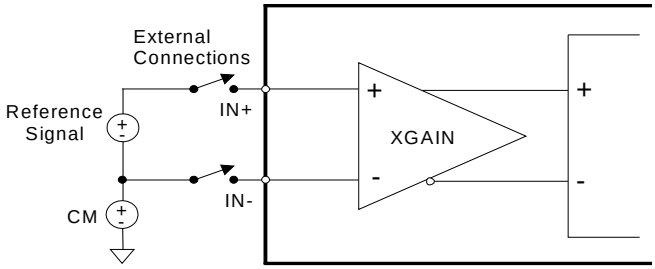


Figure 11. System Calibration of Gain

For gain calibrations, there is an absolute limit on the RMS voltage levels that are selected for the gain-calibration input signals. The maximum value that the gain registers can attain is 4. Therefore, if the signal level of the applied input is low enough that it causes the CS5461A to attempt to set either gain register higher than 4, the gain calibration result will be invalid and all CS5461A results obtained while performing measurements will be invalid.

If the channel gain registers are initially set to a gain other then 1.0, AC gain calibration should be used.

7.1.3.1 AC Gain Calibration Sequence

The corresponding gain register should be set to 1.0, unless a different initial gain value is desired. Initiate an AC gain calibration. The AC gain calibration algorithm computes the RMS value of the reference signal applied to the channel inputs. The RMS register value is then divided into 0.6 and the quotient is stored in the corresponding gain register. Each instantaneous measurement will be multiplied by its corresponding AC gain value.

A typical rms calibration value which allows for reasonable over-range margin would be 0.6 or 60% of the voltage and current channel's maximum input voltage level.

Two examples of AC gain calibration and the updated digital output codes of the channel's instantaneous data registers are shown in Figures 12 and 13. Figure 13

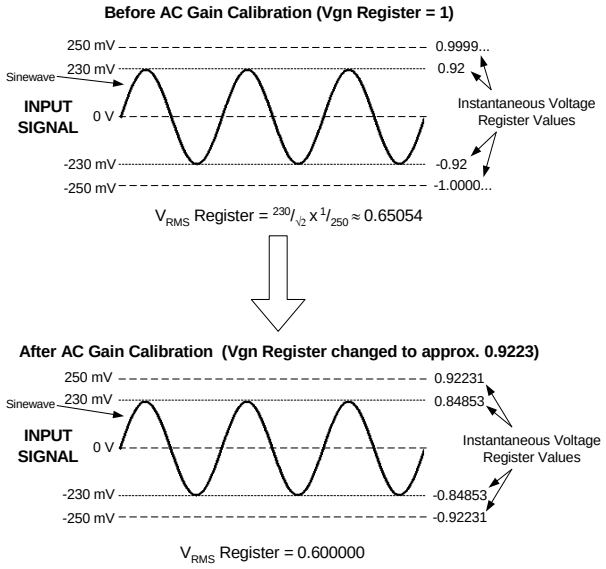


Figure 12. Example of AC Gain Calibration

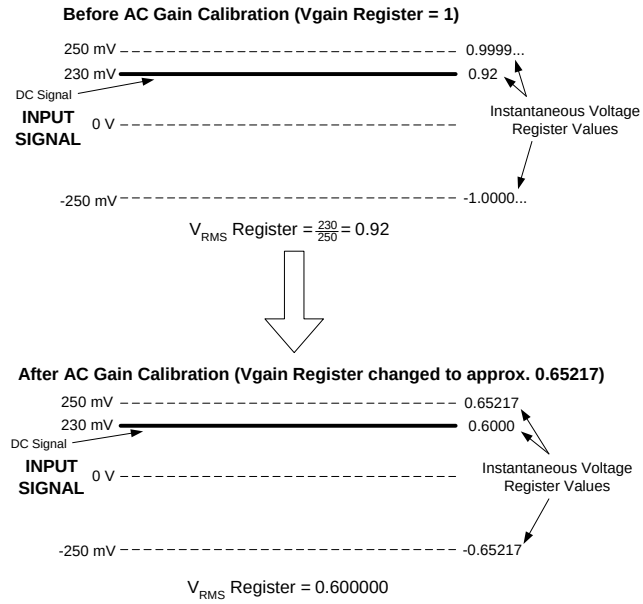


Figure 13. Another Example of AC Gain Calibration

shows that a positive (or negative), DC-level signal can be used even though an AC gain calibration is being ex-

ecuted. However, an AC signal should not be used for DC gain calibration.

7.1.3.2 DC Gain Calibration Sequence

Initiate a DC gain calibration. The corresponding gain register is restored to default (1.0). The DC gain calibration algorithm averages the channel's instantaneous measurements over one computation cycle (N samples). The average is then divided into 1.0 and the quotient is stored in the corresponding gain register

After the DC gain calibration, the instantaneous register will read at full-scale whenever the DC level of the input signal is equal to the level of the DC calibration signal applied to the inputs during the DC gain calibration.The HPF option should not be enabled if DC gain calibration is utilized.

7.1.4 Order of Calibration Sequences

1. If the HPF option is enabled, then any dc component that may be present in the selected signal path will be removed and a DC offset calibration is not required. However, if the HPF option is disabled the DC offset calibration sequence should be performed.

   When using high-pass filters, it is recommended that the DC offset register for the corresponding channel be set to zero. When performing DC offset calibration, the corresponding gain channel should be set to one.

2. If an ac offset exist, in the V_{RMS} or I_{RMS} calculation, then the AC offset calibration sequence should be performed.

3. Perform the gain calibration sequence.

4. Finally, if an AC offset calibration was performed (step 2), then the AC offset may need to be adjusted to compensate for the change in gain (step 3). This can be accomplished by restoring zero to the AC offset register and then perform an AC offset calibration sequence. The adjustment could also be done by multiplying the AC offset register value that was calculated in step 2 by the gain calculated in step 3 and updating the AC offset register with the product.

7.2 Phase Compensation

The CS5461A is equipped with phase compensation to cancel out phase shifts introduced by the measurement element. Phase Compensation is set by bits PC[6:0] in the *Configuration Register*.

The default value of PC[6:0] is zero. With MCLK = 4.096 MHz and K = 1, the phase compensation has a range of ±2.8 degrees when the input signals are 60 Hz. Under these conditions, each step of the phase compensation register (value of one LSB) is approximately 0.04 degrees. For values of MCLK other than 4.096 MHz, the range and step size should be scaled by 4.096 MHz/(MCLK/K). For power-line frequencies other than 60Hz, the values of the range and step size of the PC[6:0] bits can be determined by converting the above values from angular measurement into time-domain (seconds), and then computing the new range and step size (in degrees) with respect to the new line frequency.

7.3 Active Power Offset

The *Power Offset Register* can be used to offset system power sources that may be resident in the system, but do not originate from the power-line signal. These sources of extra energy in the system contribute undesirable and false offsets to the power and energy measurement results. After determining the amount of stray power, the Power Offset Register can be set to cancel the effects of this unwanted energy.

8. AUTO-BOOT MODE USING E²PROM

When the CS5461A MODE pin is asserted (logic 1), the CS5461A *auto-boot mode* is enabled. In auto-boot mode, the CS5461A downloads the required commands and register data from an external serial E²PROM, allowing the CS5461A to begin performing energy measurements.

8.1 Auto-Boot Configuration

A typical auto-boot serial connection between the CS5461A and a E²PROM is illustrated in Figure 14. In auto-boot mode, the CS5461A's $\overline{CS}$ and SCLK are configured as outputs. The CS5461A asserts $\overline{CS}$, provides a clock on SCLK, and sends a read command to the E²PROM on SDO. The CS5461A reads the user-specified commands and register data presented on the SDI pin. The E²PROM's programmed data is utilized by the CS5461A to change the designated registers' default values and begin registering energy.

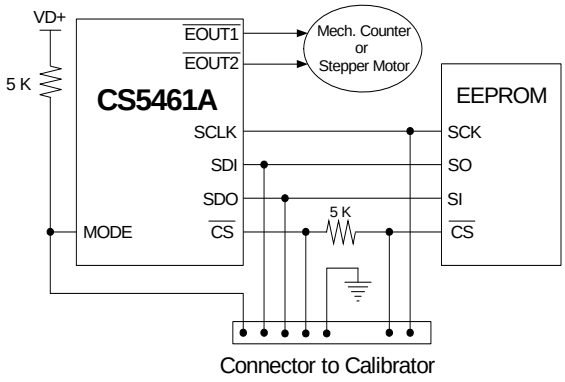


Figure 14. Typical Interface of E²PROM to CS5461A

Figure 14 also shows the external connections that would be made to a calibrator device, such as a PC or custom calibration board. When the metering system is installed, the calibrator would be used to control calibration and/or to program user-specified commands and calibration values into the E²PROM. The user-specified commands/data will determine the CS5461A's exact operation, when the auto-boot initialization sequence is running. Any of the valid commands can be used.

8.2 Auto-Boot Data for E²PROM

Below is an example code set for an auto-boot sequence. This code is written into the E²PROM by the user. The serial data for such a sequence is shown below in single-byte, hexidecimal notation:

- 40 00 00 61
  Write Configuration Register, turn high-pass filters on, set K=1.
- 44 7F C4 A9
  Write value of 0x7FC4A9 to Current Gain Register.
- 48 FF B2 53
  Write value of 0xFFB253 to Voltage Gain Register.
- 4C 00 7D 00
  Set PulseRate$E_{1,2}$ Register to 1000 Hz.
- 74 00 00 04
  Unmask bit #2 (LSD) in the Mask Register).
- E8
  Start continuous conversions
- 78 00 01 00
  Write STOP bit to Control Register, to terminate auto-boot initialization sequence.

8.3 Suggested E²PROM Devices

Several industry-standard, serial E²PROMs that will successfully run auto-boot with the CS5461A are listed below:

- Atmel AT25010, AT25020 or AT25040
- National Semiconductor NM25C040M8 or NM25020M8
- Xicor X25040SI

These types of serial E²PROMs expect a specific 8-bit command (00000011) in order to perform a memory read. The CS5461A has been hardware programmed to transmit this 8-bit command to the E²PROM at the beginning of the auto-boot sequence.

9. BASIC APPLICATION CIRCUITS

Figure 15 shows the CS5461A configured to measure power in a single-phase, 2-wire system while operating in a single-supply configuration. In this diagram, a shunt resistor is used to sense the line current and a voltage divider is used to sense the line voltage. In this type of shunt resistor configuration, the common-mode level of the CS5461A must be referenced to the line side of the power line. This means that the common-mode potential of the CS5461A will track the high-voltage levels, as well as low-voltage levels, with respect to earth ground potential. Isolation circuitry is required when an earth-ground-referenced communication interface is connected.

Figure 16 shows the same single-phase, two-wire system with complete isolation from the power lines. This isolation is achieved using three transformers: a general purpose transformer to supply the on-board DC power; a high-precision, low-impedance voltage transformer with very little roll-off/phase-delay, to measure voltage; and a current transformer to sense the line current.

Figure 17 shows a single-phase, 3-wire system. In many 3-wire residential power systems within the United States, only the two line terminals are available (neutral is not available). Figure 18 shows the CS5461A configured to meter a three-wire system with no neutral available.

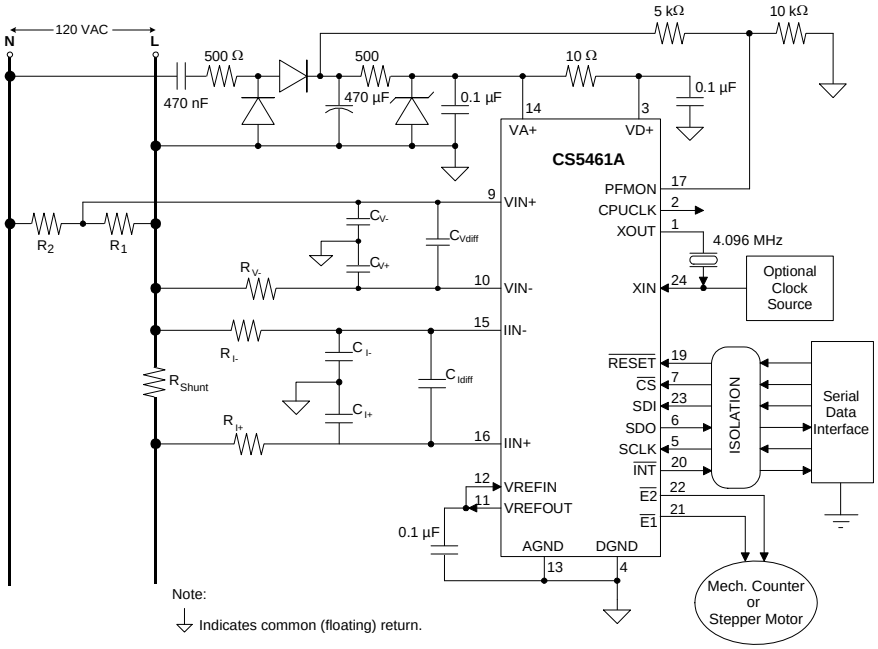


Figure 15. Typical Connection Diagram *(Single-phase, 2-wire – Direct Connect to Power Line)*

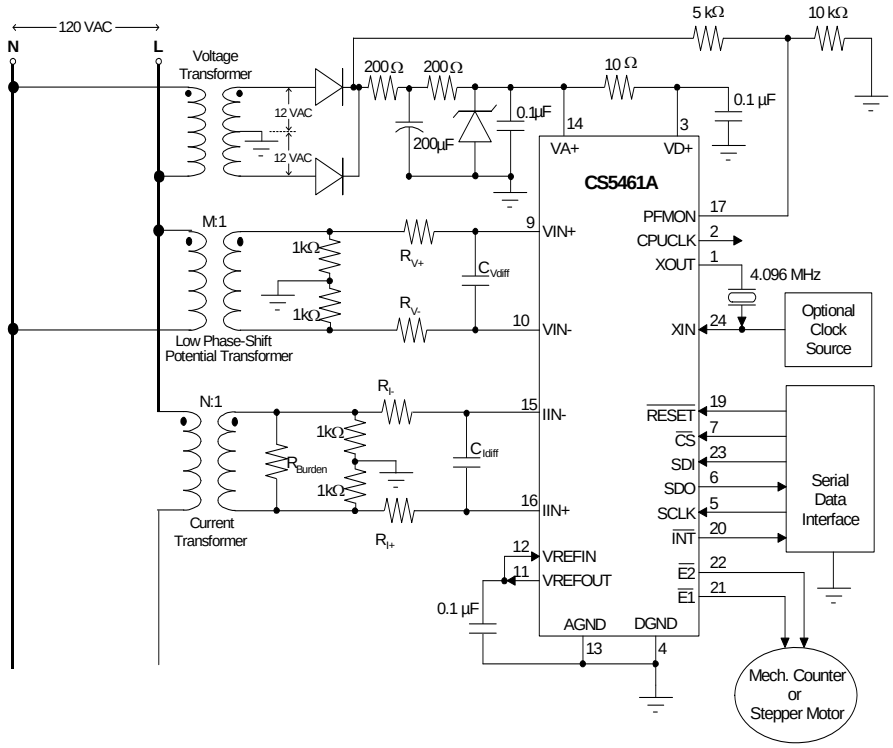


Figure 16. Typical Connection Diagram *(Single-phase, 2-wire – Isolated from Power Line)*

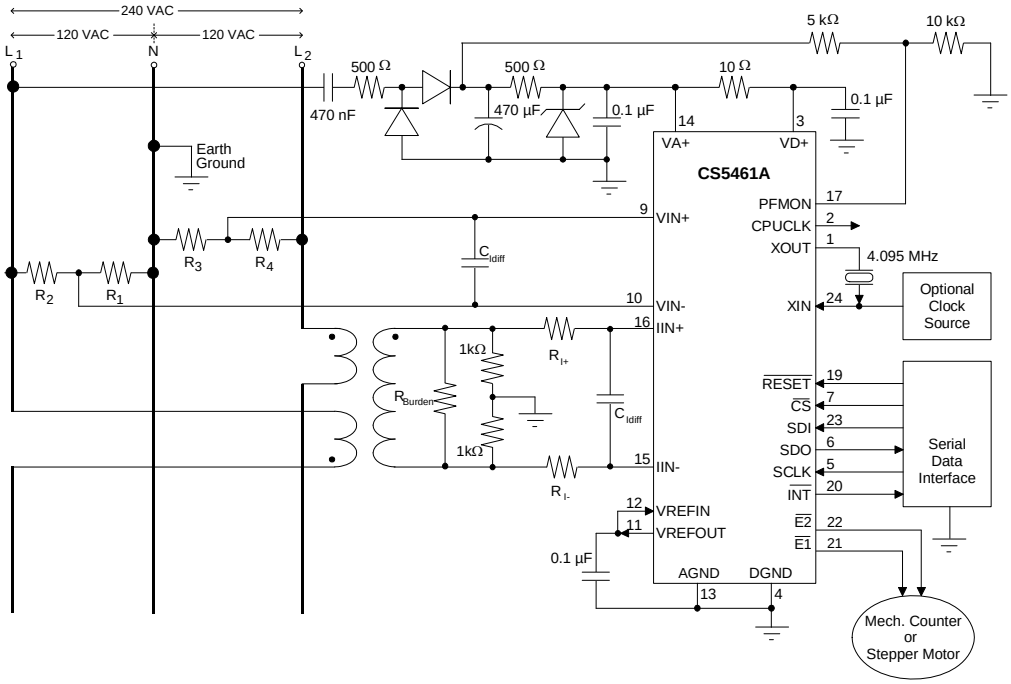


Figure 17. Typical Connection Diagram *(Single-phase, 3-wire)*

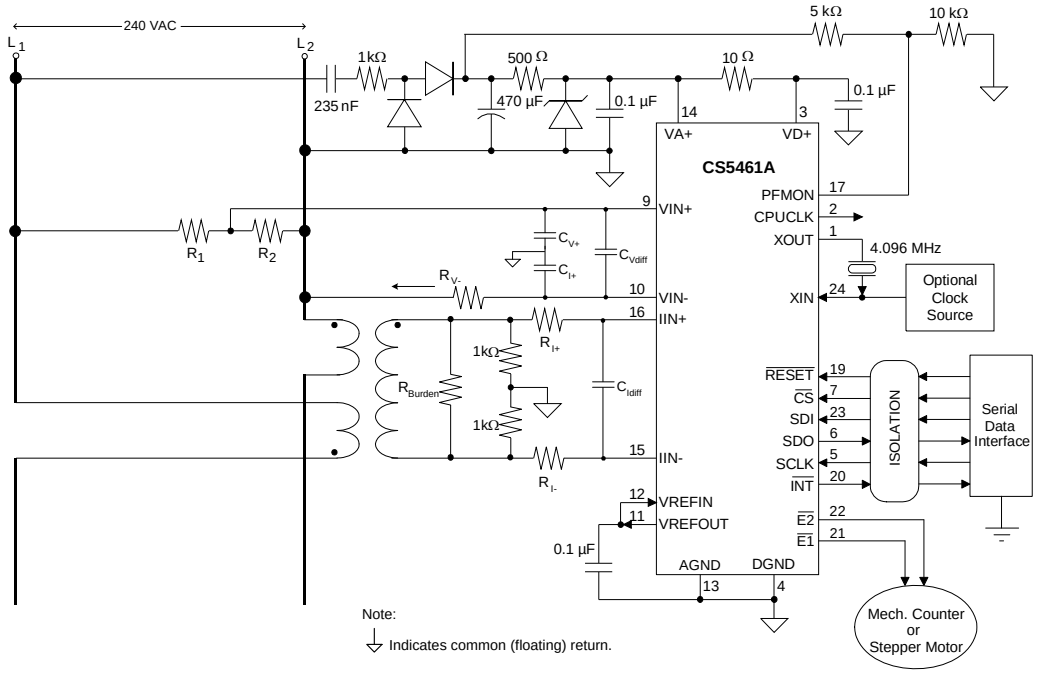
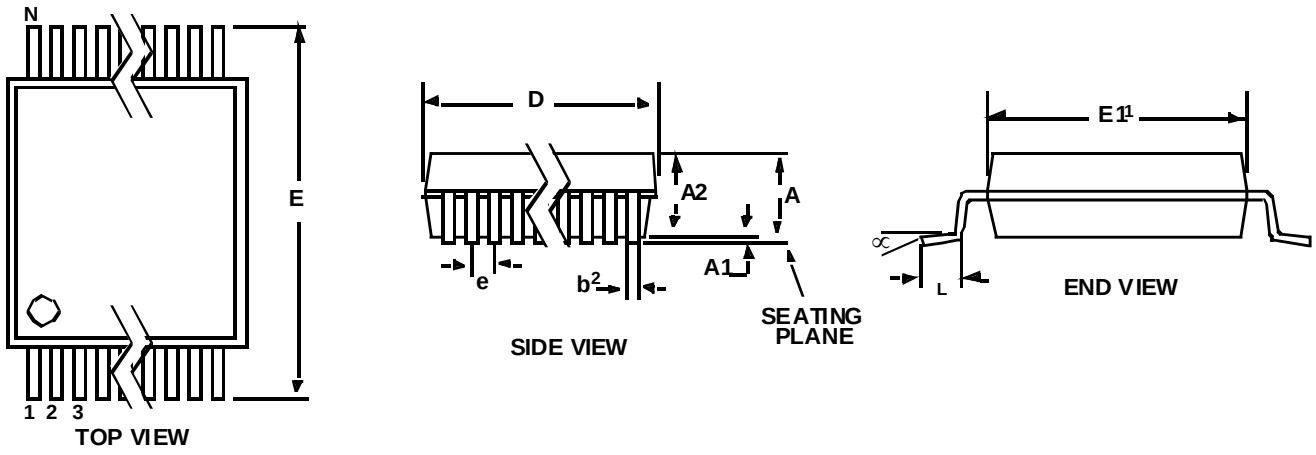


Figure 18. Typical Connection Diagram *(Single-phase, 3-wire – No Neutral Available)*

10.PACKAGE DIMENSIONS

24L SSOP PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.084	--	--	2.13	
A1	0.002	0.006	0.010	0.05	0.13	0.25	
A2	0.064	0.068	0.074	1.62	1.73	1.88	
b	0.009	--	0.015	0.22	--	0.38	2,3
D	0.311	0.323	0.335	7.90	8.20	8.50	1
E	0.291	0.307	0.323	7.40	7.80	8.20	
E1	0.197	0.209	0.220	5.00	5.30	5.60	1
e	0.022	0.026	0.030	0.55	0.65	0.75	
L	0.025	0.03	0.041	0.63	0.75	1.03	
∝	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-150

Controlling Dimension is Millimeters.

Notes:
3. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.
4. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.
5. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

11. ORDERING INFORMATION

Model	Temperature	Package
CS5461A-ISZ (lead free)	-40 to +85 °C	24-pin SSOP

12. ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

Model Number	Peak Reflow Temp	MSL Rating*	Max Floor Life
CS5461A-ISZ (lead free)	260 °C	3	7 Days

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

13. REVISION HISTORY

Revision	Date	Changes
A1	DEC 2004	Advance Release
PP1	FEB 2005	Initial Preliminary Release
F1	AUG 2005	Final version Updated with most-recent characterization data. MSL data added.
F2	APR 2008	Added *LoadIntv*, *LoadMin*, & *PulseWidth* registers. Added APF function.
F3	APR 2011	Removed lead-containing (Pb) device ordering information.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.

To find the one nearest to you go to www.cirrus.com