CS4399

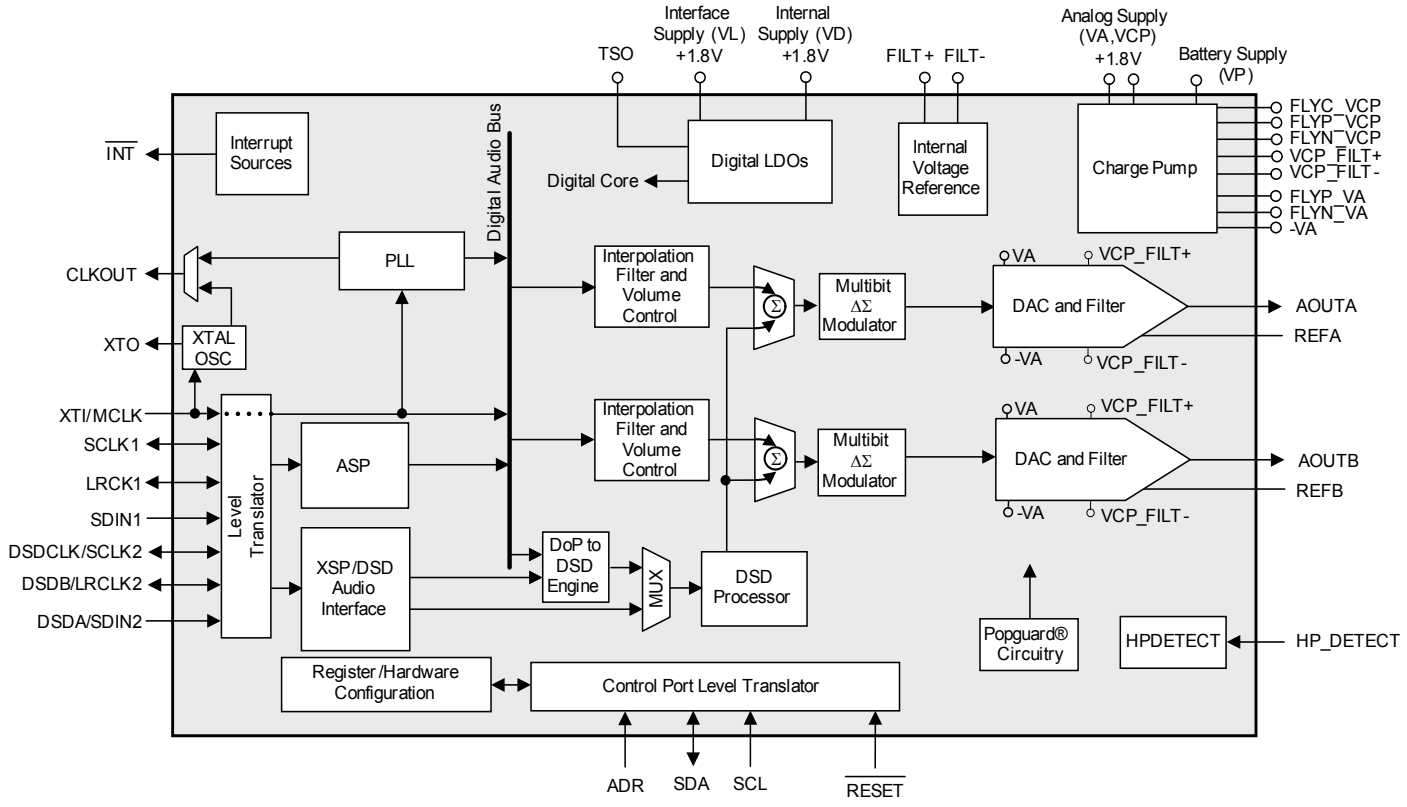
130-dB, 32-Bit High-Performance DAC

System Features

- Enhanced ΔΣ oversampling DAC architecture
  - 32-bit resolution
  - Up to 384-kHz sampling rate
  - Low clock jitter sensitivity
  - Auto mute detection
- Integrated high performance outputs
  - 130-dB dynamic range (A-weighted)
  - –108-dB total harmonic distortion + noise (THD+N)
  - 110-dB interchannel isolation
- Headphone detection
  - Headphone plug-in detection
  - Popguard® technology eliminates pop noise
- Integrated PLL
  - Support for 11.2896-/22.5792-, 12.288-/24.576-, 9.6-/19.2-, 12-/24-, and 13-/26-MHz system MCLK rates
  - Reference clock sourced from XTI/MCLK pin
  - System clock output
- Mono mode support
- I²C control—up to 1 MHz
- Direct Stream Digital (DSD®) path
  - Patented DSD processor
    - On-chip 50-kHz filter to meet Scarlet Book Super Audio Compact Disk (SACD) recommendations
    - Matched PCM and DSD analog output levels
    - Nondecimating volume control with 0.5-dB step size and soft ramp
    - DSD and Pulse-code modulation (PCM) mixing for alerts
  - Dedicated DSD and DoP pin interface
- Serial audio input path
  - Five selectable digital filter responses
    - Low-latency mode minimizes pre-echo
    - 110 dB of stopband attenuation
  - Supports sample rates from 32 to 384 kHz
  - I²S, right-justified, left-justified, TDM, and DSD-over-PCM (DoP) interface
  - Master or slave operation
  - Volume control with 0.5-dB step size and soft ramp
  - 44.1 kHz deemphasis and inverting feature
- 40-pin QFN or 42-ball CSP package option

Applications

- Smart phones, tablets, portable media players, laptops, digital headphones, powered speakers, AVR, home theater systems, Blu-ray/DVD/SACD players and pro audio



http://www.cirrus.com

General Description

The CS4399 is a high-performance, 32-bit resolution, stereo audio DAC that supports up to 384-kHz sampling frequency. The advanced 32-bit oversampled multibit modulator with mismatch shaping technology eliminates distortion due to on-chip component mismatch. Proprietary digital-interpolation filters support five selectable filter responses with pseudo-linear phase and ultralow latency to minimize pre-echos and ringing artifacts. Other features include volume control with 0.5-dB steps and digital deemphasis for 44.1-kHz sample rate.

The patented on-chip DSD processor preserves audio integrity by allowing signal processing such as volume control and 50-kHz Scarlet Book recommended filtering to be applied directly to the DSD stream without an intermediate decimation stage. Additional features like volume matching and channel mixing enable seamless transition between DSD and PCM playback paths.

The CS4399 accepts I^2S, right-justified, left-justified, and TDM-format PCM data at sample rates from 32 to 384 kHz. The industry-standard high-speed I^2C interface capable of up to 1-MHz operation provides easy configuration control. An integrated PLL allows for maximum clocking flexibility in any system. Popguard® technology eliminates output transients upon power-up or power-down events.

The CS4399 is available in a commercial-grade 42-ball WLCSP or 40-pin QFN package for operation from –10°C to +70°C.

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1 Pin Assignments and Descriptions

1.1 40-Pin QFN (Top-Down, Through-Package View)

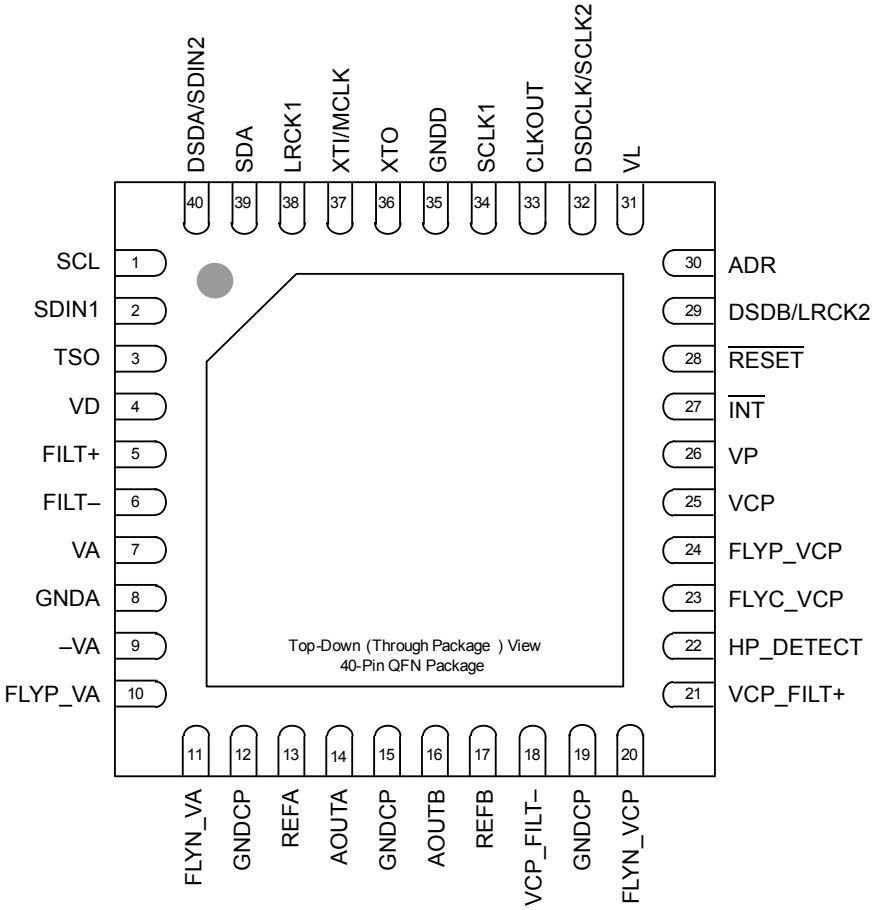


Figure 1-1. Top-Down (Through-Package) View—QFN 40-Pin Diagram

1.2 42-Ball WLCSP (Top-down, Through-Package View)

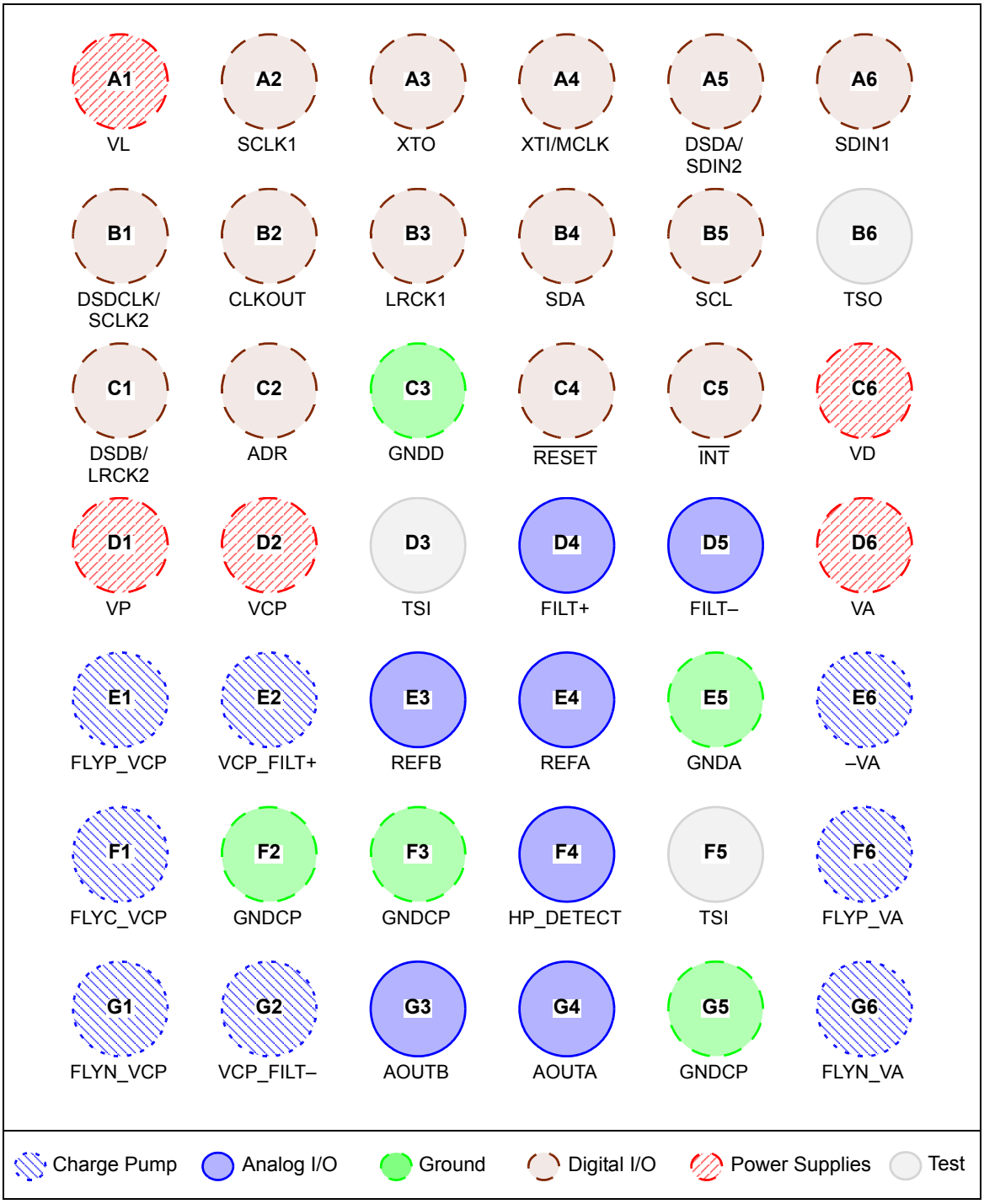


Figure 1-2. Top-Down (Through-Package) View—42-Ball WLCSP Package

1.3 Pin Descriptions

Table 1-1. Pin Descriptions

Pin Name	QFN Pin #	WLCSP Ball	Power Supply	I/O	Pin Description	Internal Connection	Digital I/O Driver	Digital I/O Receiver
					Digital I/O			
ADR	30	C2	VL	I	**Address Bit (I²C).** In I²C Mode, ADR is a chip address pin.	—	—	—
CLKOUT	33	B2	VL	O	**CLK Output.** Single-ended clock output sourced from PLL or buffered crystal.	Weak pull-down	CMOS output	—
SCLK1	34	A2	VL	I/O	**Serial Audio Input Bit Clock 1.** Serial bit clock for audio data on the SDIN pins.	Weak pull-down	CMOS output	Hysteresis on CMOS input
LRCK1	38	B3	VL	I/O	**Serial Audio Input Left/Right Clock.** Word-rate clock for the audio data on the SDIN pins.	Weak pull-down	CMOS output	Hysteresis on CMOS input
SDIN1	2	A6	VL	I	**Serial Audio Input Data Port.** Audio data serial input pin 1.	Weak pull-down	—	Hysteresis on CMOS input
DSDA/ SDIN2	40	A5	VL	I	**DSD Data Input A/Serial Data In 2.** DSD audio or PCM audio data serial input pin 2.	Weak pull-down	—	Hysteresis on CMOS input
DSDB/ LRCK2	29	C1	VL	I/O	**DSD Data Input B/Serial Audio Input Left/Right Clock 2.** DSD audio data serial input pin or word rate clock for the audio data on the SDIN2 pin.	Weak pull-down	CMOS output	Hysteresis on CMOS input
DSDCLK/ SCLK2	32	B1	VL	I/O	**DSD Clock Input/Serial Audio Input Bit Clock 2.** DSD clock input. Serial bit clock for audio data on the SDIN2 pin.	Weak pull-down	CMOS output	Hysteresis on CMOS input
$\overline{\text{INT}}$	27	C5	VP	O	**Interrupt.** When pulled up, works as system interrupt pin. Open drain, active low programmable.	—	CMOS open-drain output	—
$\overline{\text{RESET}}$	28	C4	VP	I	**System Reset.** The device enters system reset when enabled.	—	—	Hysteresis on CMOS input
SDA	39	B4	VL	I/O	**Serial Control Data I/O (I²C).** In I²C Mode, SDA is the control I/O data line.	—	CMOS open-drain output	Hysteresis on CMOS input
SCL	1	B5	VL	I	**Software Clock (I²C).** Serial control interface clock used to clock control data bits into and out of the CS4399.	—	—	Hysteresis on CMOS input
XTI/MCLK	37	A4	VL	I	**Crystal/Oscillator Input/MCLK In.** Crystal or digital clock input for the master clock.	Weak pull-down	—	Hysteresis on CMOS input
XTO	36	A3	VL	O	**Crystal/Oscillator Output.** Crystal output.	Weak pull-down	CMOS output	—
					Analog I/O			
FILT+ FILT–	5 6	D4 D5	VA	O	**Positive/Negative Voltage Reference.** Positive/negative reference voltage for DAC.	—	—	—
HP_ DETECT	22	F4	VP	I	**Headphone Detect.** Can be configured to be debounced on unplugged and plugged events before it is presented as a noninterrupt status bit (HPDETECT).	—	Hi-Z	—
AOUTB AOUTA	16 14	G3 G4	VCP_ FILT±	O	**Audio Output.** Refer to analog specification table for full-scale output level.	—	—	—
REFB REFA	17 13	E3 E4	VCP_ FILT±	I	**Output Reference.** Reference for analog output.	—	—	—
					Power Supplies			
VL	31	A1	N/A	I	**Logic Power.** Input/Output power supply, typically +1.8 V.	—	—	—
VD	4	C6	N/A	I	**Internal Digital Power.** Internal digital power supply, typically +1.8 V.	—	—	—
VA	7	D6	N/A	I	**Analog Power.** Power supply for the internal analog section.	—	—	—
VCP	25	D2	N/A	I	**Charge Pump Supply**. Provides charge pump voltage to the analog output circuit.	—	—	—
VP	26	D1	N/A	I	**Battery supply**. Provides voltage to the Class H circuit.	—	—	—

Table 1-1. Pin Descriptions *(Cont.)*

Pin Name	QFN Pin #	WLCSP Ball	Power Supply	I/O	Pin Description	Internal Connection	Digital I/O Driver	Digital I/O Receiver
					Ground			
GNDD	35	C3	N/A	I	**Digital and I/O Ground.** Ground for the I/O and core logic. GNDA, GNDCP, GNDD must be connected to a common ground area under the chip.	—	—	—
GNDA	8	E5	N/A	I	**Analog Ground.** Ground reference for the internal analog section. GNDA, GNDCP, GNDD must be connected to a common ground area under the chip.	—	—	—
GNDCP	12, 15, 19	F2, F3, G5	N/A	I	**Charge Pump Ground.** Ground reference for the charge pump section. GNDA, GNDCP, GNDD must be connected to a common ground area under the chip.	—	—	—
					Charge Pump			
VCP_FILT+ VCP_FILT–	21 18	E2 G2	VCP/ VP [1]	I/O	**Inverting Charge Pump Filter Connection.** Power supply from the inverting charge pump that provides the positive/negative rail for the analog output. When operating in external VCP_FILT mode, these pins can directly take in supply voltage.	—	—	—
–VA	9	E6	VA	O	**VA Negative Charge Pump Output.** Negative charge pump output for DAC rail. It is derived from VA.	—	—	—
FLYP_VA FLYN_VA	10 11	F6 G6	VA	O	**–VA Charge Pump Cap Positive/Negative Node.** Positive/ negative nodes for the DAC negative charge pump's flying capacitor.	—	—	—
FLYP_VCP	24	E1	VCP/ VP [1]	O	**–VCP Charge Pump Cap Positive Node.** Positive node for the analog output negative charge pump's flying capacitor.	—	—	—
FLYC_VCP	23	F1	VCP/ VP [1]	O	**–VCP Charge Pump Cap Center Node.** Center node for the analog output negative charge pump's flying capacitor.	—	—	—
FLYN_VCP	20	G1	VCP_ FILT±	O	**–VCP Charge Pump Cap Negative Node.** Negative node for the analog output negative charge pump's flying capacitor.	—	—	—
					Test			
TSO	3	B6	N/A	I/O	**Test Output.**	—	—	—
TSI	—	D3, F5			**Test Input.**	—	—	—

1. The power supply is determined by ADPT_PWR setting (see Section 4.3.1). VP is used if ADPT_PWR = 001 (VP_LDO Mode) or when necessary for ADPTPWR = 111 (Adapt-to-Signal Mode).

1.4 Electrostatic Discharge (ESD) Protection Circuitry

ESD-sensitive device. The CS4399 is manufactured on a CMOS process. Therefore, it is generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken while handling and storing this device. This device is qualified to current JEDEC ESD standards.

Fig. 1-3 provides a composite view of the ESD domains showing the ESD protection paths between each pad and the substrate (GND), as well as the interrelations between some domains. Note that this figure represents the structure for the internal protection devices and that additional protections can be implemented as part of the integration into the board.

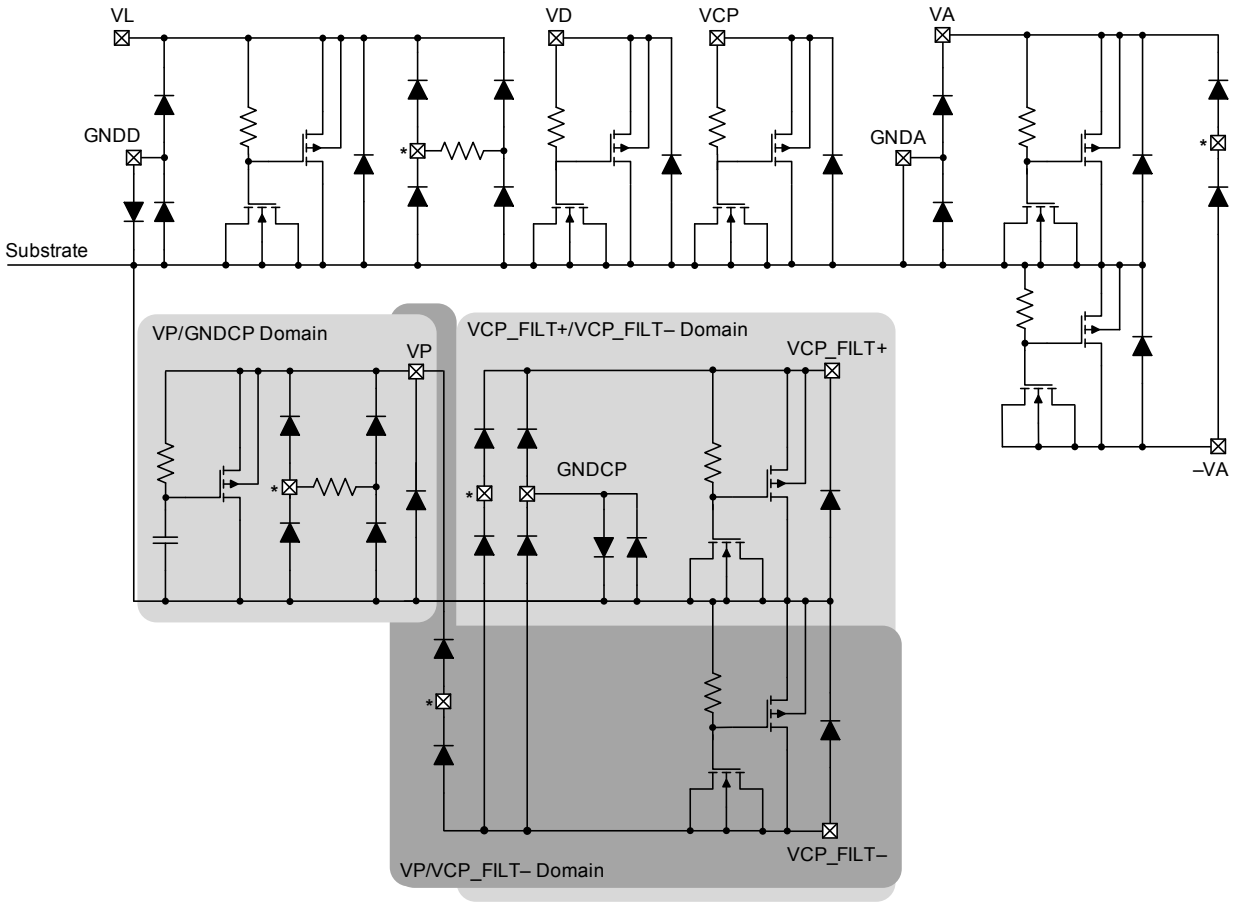


Figure 1-3. Composite ESD Topology

Table 1-2 shows the individual ESD domains and lists the pins associated with each domain.

Table 1-2. ESD Domains

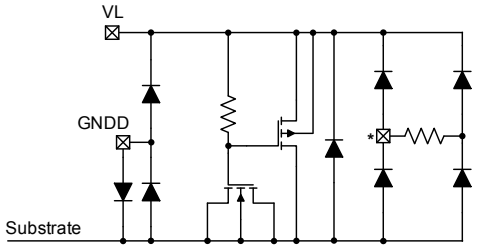
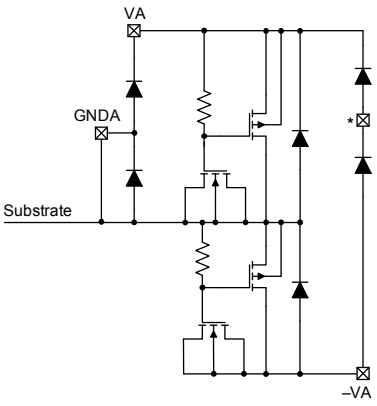
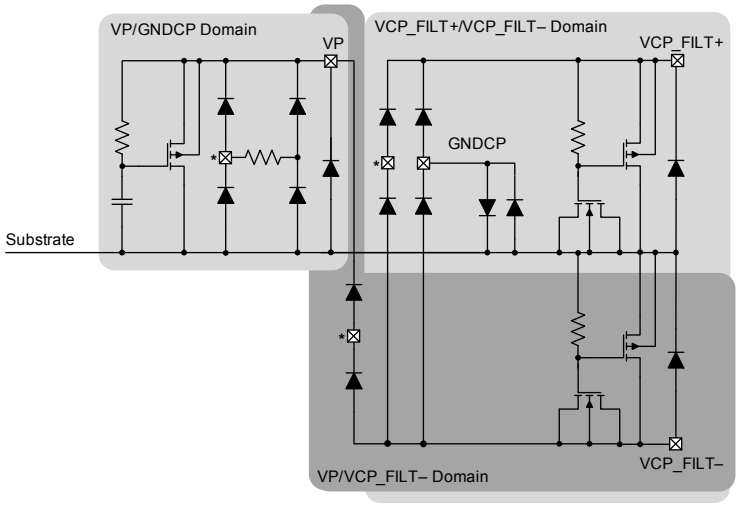
ESD Domain	Signal Name (See * in Topology Figures for Pad)	Topology
VL/GNDD	ADR DSDCLK/SCLK2 SCL SDA DSDB/LRCK2 DSDA/SDIN2 SDIN1 LRCK1 SCLK1 CLKOUT XTI/MCLK XTO	

Table 1-2. ESD Domains *(Cont.)*

ESD Domain	Signal Name (See * in Topology Figures for Pad)	Topology
VA/–VA	FLYN_VA FLYP_VA FILT+ FILT–	
VP/GNDCP	$\overline{\text{RESET}}$ $\overline{\text{INT}}$	
VP/VCP_FILT–	FLYP_VCP FLYC_VCP HP_DETECT	
VCP_FILT+/ VCP_FILT–	FLYN_VCP AOUTA AOUTB REFA REFB	

2 Typical Connection Diagram

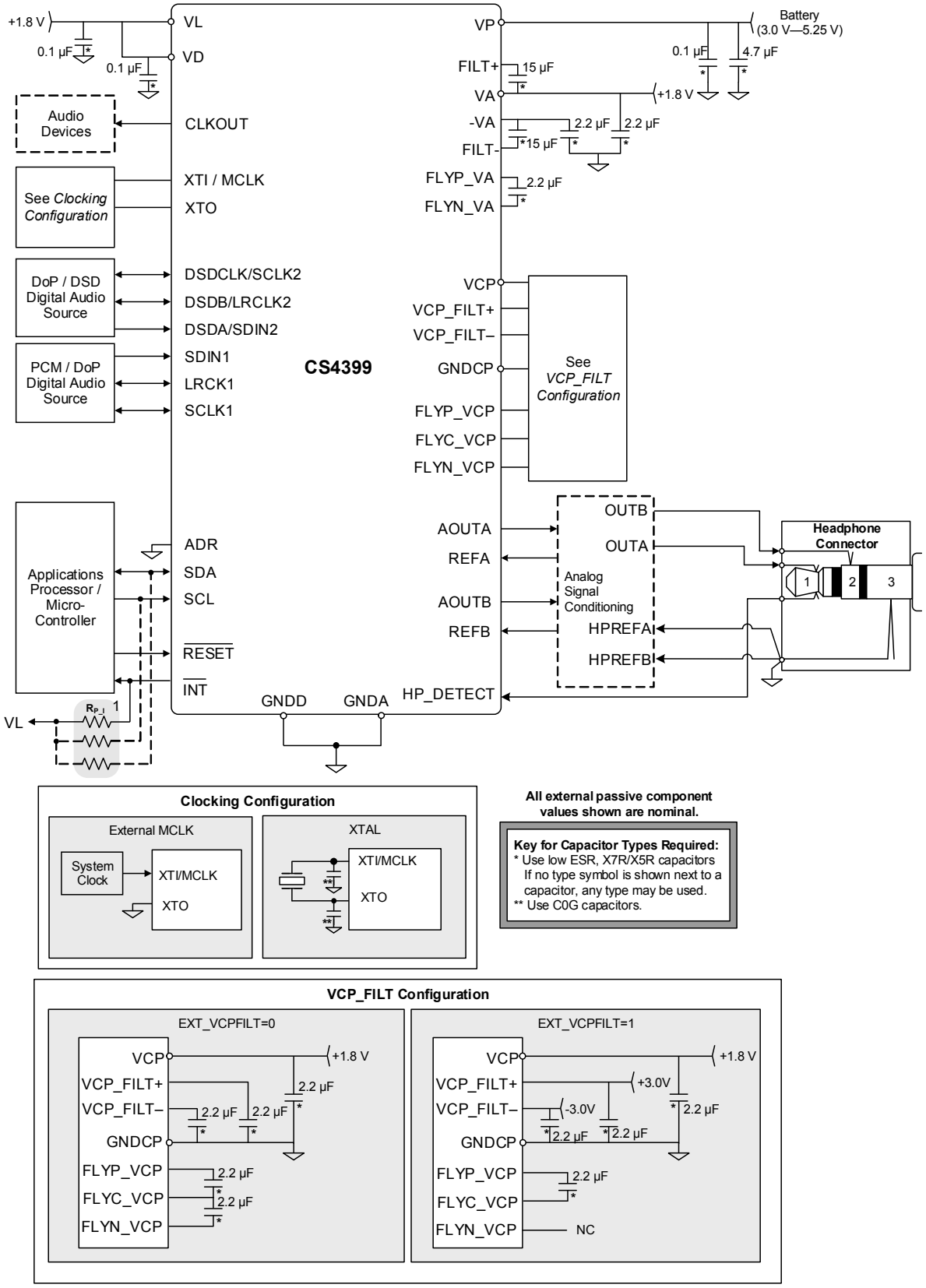


Figure 2-1. Typical Connection Diagram

Note:
1. The value for R_{P_I} can be determined by the interrupt pin specification in Table 3-8.

3 Characteristics and Specifications

Table 3-1 defines parameters as they are characterized in this section.

Table 3-1. Parameter Definitions

Parameter	Definition
Dynamic range	The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. A signal-to-noise ratio measurement over the specified bandwidth made with a –60-dB signal; 60 dB is added to resulting measurement to refer the measurement to full scale. This technique ensures that distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17–1991, and the Electronic Industries Association of Japan, EIAJ CP–307. Dynamic range is expressed in decibel units.
Gain drift	The change in gain value with temperature, expressed in ppm/°C units.
Idle channel noise	The rms value of the signal with no input applied (properly back-terminated analog input, digital zero, or zero modulation input). Measured over the specified bandwidth.
Interchannel gain mismatch	The gain difference between left and right channel pairs. Interchannel gain mismatch is expressed in decibel units.
Interchannel phase mismatch	The phase difference between left and right channel pairs at 997-Hz sine wave input. Interchannel phase mismatch is expressed in degree units (with respect to 997-Hz sine wave input).
Interchannel isolation	A measure of cross talk between the left and right channel pairs. Interchannel isolation is measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Interchannel isolation is expressed in decibel units.
Load resistance and capacitance	The recommended minimum resistance and maximum capacitance required for the internal op-amp's stability and signal integrity. The load capacitance effectively moves the band-limiting pole of the amp in the output stage. Increasing load capacitance beyond the recommended value can cause the internal op-amp to become unstable.
Output offset voltage	The DC offset voltage present at the amplifier's output when its input signal is in a mute state. The offset exists due to CMOS process limitations and is proportional to analog volume settings. When measuring the offset out of the headphone amplifier, the headphone amplifier is ON.
Total harmonic distortion + noise (THD+N)	The ratio of the rms sum of distortion and noise spectral components across the specified bandwidth (typically 20 Hz–20 kHz) relative to the rms value of the signal. THD+N is measured at –1 and –20 dBFS for the analog input and at 0 and –20 dB for the analog output, as suggested in AES17–1991 Annex A. THD+N is expressed in decibel units.
Turn-on time	Turn-on time is measured from when the PDN_HP = 0 ACK signal is received to when the signal appears on the HP output.

Table 3-2. Recommended Operating Conditions

GNDD = GNDA = 0 V, all voltages with respect to ground.

Parameters [1]			Symbol	Minimum	Maximum	Units
DC power supply	Analog		VA	1.66	1.94	V
	Charge pump		VCP	1.66	1.94	V
	Filtered charge pump	EXT_VCPFLT = 1	VCP_FILT+	2.85	3.15	V
			VCP_FILT–	–3.15	–2.85	V
	Battery supply	HV_EN = 0, EXT_VCPFILT = 0 HV_EN = 1, EXT_VCPFILT = 0 EXT_VCPFILT = 1	VP	3.0 3.3 3.3	5.25 5.25 5.25	V V V
	Digital Interface		VL	1.66	1.94	V
	Digital Internal		VD	1.66	1.94	V
External voltage applied to pin[2,3]		HP_DETECT pin VCP_FILT± domain pins [4] VL domain pins VA domain pins VP domain pins	V_{INHI} V_{VCPF} V_{VL} V_{VA} V_{VP}	–0.3 – VCP_FILT– –0.3 – VCP_FILT– –0.3 –0.3 –0.3	VP + 0.3 0.3 + VCP_FILT+ VL + 0.3 VA + 0.3 VP + 0.3	V V V V V
Ambient temperature			T_A	–10	+70	°C

1. Device functional operation is guaranteed within these limits. Functionality is not guaranteed or implied outside of these limits. Operation outside of these limits may adversely affect device reliability.
2. The maximum over/undervoltage is limited by the input current.
3. Table 1-1 lists the power supply domain in which each CS4399 pin resides.
4. VCP_FILT± is specified in Table 3-13.

Table 3-3. Absolute Maximum Ratings

GNDD = GNDA= GNDCP = 0 V; all voltages with respect to ground.

Parameters		Symbol	Minimum	Maximum	Units
DC power supply	Analog	VA	–0.3	2.33	V
	Battery	VP	–0.3	6.3	V
	Charge pump	VCP	–0.3	2.33	V
	Filtered charge pump (positive)	VCP_FILT+	–0.3	3.3	V
	Filtered charge pump (negative)	VCP_FILT–	0.3	–3.3	V
	Digital interface	VL	–0.3	2.33	V
	Digital internal	VD	–0.3	2.33	V
Input current [1]		I_{in}	—	±10	mA
Ambient operating temperature (power applied)		T_A	–50	+115	°C
Storage temperature		T_{stg}	–65	+150	°C

Caution: Stresses beyond “Absolute Maximum Ratings” levels may cause permanent damage to the device. These levels are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Table 3-2, “Recommended Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1.Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins do not cause SCR latch-up.

Table 3-4. Analog Output Characteristics (HV_EN = 1) [1]

Test conditions (unless otherwise specified): Fig. 2-1 shows CS4399 connections; input test signal is a 32-bit, full-scale 997-Hz sine wave (unless specified otherwise); GNDA = GNDCP = GNDD = 0 V; voltages are with respect to ground; ASP_M/Sb = 1; typical, min/max performance data taken with VA = VCP = 1.8 V; VL = VD = 1.8 V; VP = 3.6 V; T_A = +25°C; measurement bandwidth is 20 Hz–20 kHz; ASP_SPRATE = 0001 (LRCK = 44.1-kHz mode); PDN_XTAL = 0, MCLK_INT = 1, and MCLK_SRC_SEL = 00 (crystal frequency f_{XTAL} = 22.5792 MHz); Volume = 0 dB; when testing in DSD processor mode, DSD_ZERODB = 1; when testing noise related specifications (dynamic range, THD+N, idle channel noise), no external impedance on REFx.

PCM and DSD Processor Mode Parameter [2,3,4]				Minimum	Typical	Maximum	Units
AOUTx R_L = 10 kΩ C_L = 200 pF OUT_FS = 11 Volume = 0 dB [5], unless otherwise specified	Dynamic range (defined in Table 3-1)	24-bit, 32-bit, DSD	A-weighted	124	130	—	dB
			Unweighted	121	127	—	dB
		16-bit	A-weighted	91	97	—	dB
			Unweighted	88	94	—	dB
	THD+N (defined in Table 3-1)	24-bit, 32-bit, DSD	0 dB	—	–108	–101	dB
			–20 dB	—	–97	—	dB
			–60 dB	—	–67	–61	dB
		16-bit	0 dB	—	–94	–88	dB
			–20 dB	—	–74	—	dB
			–60 dB	—	–34	–28	dB
	Idle channel noise (A-weighted) (defined in Table 3-1)	24-bit, 32-bit, DSD		—	0.55	—	µV
	Full-scale output voltage			4.66	4.90	5.14	Vpp
	Interchannel isolation [6](defined in Table 3-1)		217 Hz	—	110	—	dB
			1 kHz	—	95	—	dB
			20 kHz	—	68	—	dB
AOUTx R_L = 600 Ω C_L = 200 pF OUT_FS = 11 Volume = 0 dB [5], unless otherwise specified	Dynamic range (defined in Table 3-1)	24-bit, 32-bit, DSD	A-weighted	124	130	—	dB
			Unweighted	121	127	—	dB
		16-bit	A-weighted	91	97	—	dB
			Unweighted	88	94	—	dB
	THD+N (defined in Table 3-1)	24-bit, 32-bit, DSD	0 dB	—	–108	–101	dB
			–20 dB	—	–97	—	dB
			–60 dB	—	–67	–61	dB
		16-bit	0 dB	—	–94	–88	dB
			–20 dB	—	–74	—	dB
			–60 dB	—	–34	–28	dB
	Idle channel noise (A-weighted) (defined in Table 3-1)	24-bit, 32-bit, DSD		—	0.55	—	µV
	Full-scale output voltage			4.66	4.90	5.14	Vpp
	Output power			—	5	—	mW
	Interchannel isolation [6](defined in Table 3-1)		217 Hz	—	110	—	dB
			1 kHz	—	95	—	dB
			20 kHz	—	68	—	dB

Table 3-4. Analog Output Characteristics (HV_EN = 1) [1] *(Cont.)*

Test conditions (unless otherwise specified): Fig. 2-1 shows CS4399 connections; input test signal is a 32-bit, full-scale 997-Hz sine wave (unless specified otherwise); GNDA = GNDCP = GNDD = 0 V; voltages are with respect to ground; ASP_M/Sb = 1; typical, min/max performance data taken with VA = VCP = 1.8 V; VL = VD = 1.8 V; VP = 3.6 V; T_A = +25°C; measurement bandwidth is 20 Hz–20 kHz; ASP_SPRATE = 0001 (LRCK = 44.1-kHz mode); PDN_XTAL = 0, MCLK_INT = 1, and MCLK_SRC_SEL = 00 (crystal frequency f_{XTAL} = 22.5792 MHz); Volume = 0 dB; when testing in DSD processor mode, DSD_ZERODB = 1; when testing noise related specifications (dynamic range, THD+N, idle channel noise), no external impedance on REFx.

PCM and DSD Processor Mode Parameter [2,3,4]		Minimum	Typical	Maximum	Units
Other characteristics for AOUTx	Interchannel gain mismatch (defined in Table 3-1)	—	±0.1	—	dB
	Interchannel phase mismatch (defined in Table 3-1)	—	±0.05	—	°
	Output offset voltage: Mute (defined in Table 3-1)	—	±0.5	±1	mV
	Gain drift (defined in Table 3-1)	—	±100	—	ppm/°C
	Load resistance (R_L)	600	—	—	Ω
	Load capacitance (C_L)	—	—	1	nF
	Turn-on time (defined in Table 3-1)	—	—	10	ms
	Click/pop during PDN_HP enable or disable A-weighted	—	—	–60	dBV

1. This table also applies to external VCP_FILT supply mode: CS4399 power up procedure is per description in Section 5.10.1; EXT_VCPFILT = 1; VCP_FILT+ and VCP_FILT– comply to Table 3-2 when EXT_VCPFILT = 1; in this mode, HV_EN setting becomes don't care.
2. One LSB of triangular PDF dither is added to PCM data.
3. Referred to the typical full-scale voltage. Applies to all THD+N and dynamic range values in the table.
4. DSD performance may be limited by the source recording. 0 dB-SACD = 50% modulation index.
5. The volume must be configured as indicated to achieve specified output characteristics.
6. Output test configuration. Symbolized component values are specified in the test conditions.

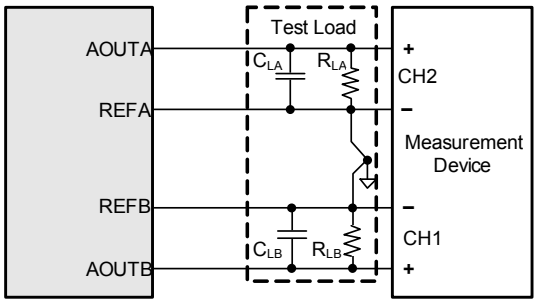


Table 3-5. Combined DAC Digital, On-Chip Analog and AOUTx Filter Characteristics

Test conditions (unless specified otherwise): The filter characteristics have been normalized to the sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs. Single-Speed Mode refers to 32-, 44.1-, and 48-kHz sample rates. Double-Speed Mode refers to 88.2- and 96-kHz sample rates. Quad-Speed Mode refers to 176.4- and 192-kHz sample rates. Octuple-Speed Mode refers to 352.8- and 384-kHz sample rates. MCLK_INT is an integer multiple of Fs; HPF disabled; no DC offset applied; group delay does not include serial port delay.

Parameter			Minimum	Typical	Maximum	Units
Fast Roll-Off (FILTER_SLOW_FASTB = 0) Single-Speed Mode [1]	Passband [2]	to –0.01-dB corner to –3-dB corner attenuation @ Fs/2	0 0 8.44 [3]	— — —	0.4535 [4] 0.49 —	Fs Fs dB
	Passband ripple 10 Hz to –0.01-dB corner [5]		–0.01	—	+0.01	dB
	Stopband		0.547	—	—	Fs
	Stopband attenuation [6]	PHCOMP_LOWLATB = 0 PHCOMB_LOWLATB = 1	110 [7] 105	— —	— —	dB dB
	Group delay (linear phase)	PHCOMB_LOWLATB = 1	—	39.5/Fs [8]	—	s
	Group delay (minimum phase)	PHCOMB_LOWLATB = 0	—	6.3/Fs [9]	—	s
	Deemphasis error [10] (Relative to 1 kHz)	Fs = 44.1 kHz	—	—	±0.14	dB
Fast Roll-Off (FILTER_SLOW_FASTB = 0) Double-Speed Mode [1]	Passband [2]	to –0.01-dB corner to –3-dB corner attenuation @ Fs/2	0 0 7.77	— — —	0.227 0.48 —	Fs Fs dB
	Passband ripple 10 Hz to –0.01-dB corner		–0.01	—	0.01	dB
	Stopband		0.583	—	—	Fs
	Stopband attenuation [6]		80	—	—	dB
	Group delay (linear phase)	PHCOMB_LOWLATB = 1	—	22.3/Fs	—	s
	Group delay (minimum phase)	PHCOMB_LOWLATB = 0	—	7.5/Fs	—	s

Table 3-5. Combined DAC Digital, On-Chip Analog and AOUTx Filter Characteristics *(Cont.)*

Test conditions (unless specified otherwise): The filter characteristics have been normalized to the sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs. Single-Speed Mode refers to 32-, 44.1-, and 48-kHz sample rates. Double-Speed Mode refers to 88.2- and 96-kHz sample rates. Quad-Speed Mode refers to 176.4- and 192-kHz sample rates. Octuple-Speed Mode refers to 352.8- and 384-kHz sample rates. MCLK_INT is an integer multiple of Fs; HPF disabled; no DC offset applied; group delay does not include serial port delay.

Parameter			Minimum	Typical	Maximum	Units
Fast Roll-Off (FILTER_SLOW_FASTB = 0) Quad-Speed Mode [1]	Passband [2]	to –0.01-dB corner	0	—	0.114	Fs
		to –3-dB corner	0	—	0.46	Fs
		attenuation @ Fs/2	9.44	—	—	dB
	Passband ripple 10 Hz to –0.01-dB corner		–0.01	—	0.01	dB
	Stopband		0.583	—	—	Fs
	Stopband attenuation [6]		80	—	—	dB
	Group delay (linear phase)	PHCOMB_LOWLATB = 1	—	20.7/Fs	—	s
	Group delay (minimum phase)	PHCOMB_LOWLATB = 0	—	11.3/Fs	—	s
Slow Roll-Off (FILTER_SLOW_FASTB = 1) Single-Speed Mode [1]	Passband [2]	to –0.01-dB corner	0	—	0.417	Fs
		to –3-dB corner	0	—	0.49	Fs
		attenuation @ Fs/2	6.45 [11]	—	—	dB
	Passband ripple 10 Hz to –0.01-dB corner [5]		–0.01	—	+0.01	dB
	Stopband		0.583	—	—	Fs
	Stopband attenuation [6]		64	—	—	dB
	Group delay (linear phase)	PHCOMB_LOWLATB = 1	—	34.5/Fs [12]	—	s
	Group delay (minimum phase)	PHCOMB_LOWLATB = 0	—	5.6/Fs [13]	—	s
	Deemphasis error [10] (Relative to 1 kHz)	Fs = 44.1 kHz	—	—	±0.14	dB
Slow Roll-Off (FILTER_SLOW_FASTB = 1) Double-Speed Mode [1]	Passband [2]	to –0.01-dB corner	0	—	0.208	Fs
		to –3-dB corner	0	—	0.458	Fs
		attenuation @ Fs/2	7	—	—	dB
	Passband ripple 10 Hz to –0.01-dB corner		–0.01	—	0.01	dB
	Stopband		0.792	—	—	Fs
	Stopband attenuation [6]		70	—	—	dB
	Group delay (linear phase)	PHCOMB_LOWLATB = 1	—	22.3/Fs	—	s
	Group delay (minimum phase)	PHCOMB_LOWLATB = 0	—	6.7/Fs	—	s
Slow Roll-Off (FILTER_SLOW_FASTB = 1) Quad-Speed Mode [1]	Passband [2]	to –0.01-dB corner	0	—	0.104	Fs
		to –3-dB corner	0	—	0.43	Fs
		attenuation @ Fs/2	7.00	—	—	dB
	Passband ripple 10 Hz to –0.01-dB corner		–0.01	—	0.01	dB
	Stopband		0.792	—	—	Fs
	Stopband attenuation [6]		75	—	—	dB
	Group delay (linear phase)	PHCOMB_LOWLATB = 1	—	20.7/Fs	—	s
	Group delay (minimum phase)	PHCOMB_LOWLATB = 0	—	10.6/Fs	—	s
Nonoversampling (NOS) (NOS = 1) Single-Speed Mode [1]	Passband [2]	to –0.01-dB corner	0	—	0.026	Fs
		to –3-dB corner	0	—	0.444	Fs
	Passband droop 10 Hz to 20 kHz		—	—	3.2 [14]	dB
	Group delay		—	2.7/Fs	—	s
Nonoversampling (NOS) (NOS = 1) Double-Speed Mode [1]	Passband [2]	to –0.01-dB corner	0	—	0.0246	Fs
		to –3-dB corner	0	—	0.446	Fs
	Passband droop 10 Hz to 20 kHz		—	—	0.73	dB
	Group delay		—	4.5/Fs	—	s
Nonoversampling (NOS) (NOS = 1) Quad-Speed Mode [1]	Passband [2]	to –0.01-dB corner	0	—	0.026	Fs
		to –3-dB corner	0	—	0.405	Fs
	Passband droop 10 Hz to 20 kHz		—	—	0.167	dB
	Group delay		—	8.4/Fs	—	s
Octuple-Speed Mode [1]	Passband [2]	to –0.01-dB corner	0	—	0.0299	Fs
		to –3-dB corner	0	—	0.302	Fs
	Passband droop 10 Hz to 20 kHz		—	—	0.037	dB
	Group delay		—	17/Fs	—	s

1. Filter response is by design.
2. Response is clock-dependent and scales with Fs.
3. 8.5 dB for 32-kHz sample rate.
4. 0.454 Fs for 32-kHz sample rate.
5. Filter ripple specification is invalid with deemphasis enabled.

6. For Single-Speed Mode, the measurement bandwidth is from stopband to 3 Fs.
   For Double-Speed Mode, the measurement bandwidth is from stopband to 3 Fs.
   For Quad-Speed Mode, the measurement bandwidth is from stopband to 1.34 Fs.
7. 105 dB for 32-kHz sample rate.
8. 39/Fs for 32-kHz sample rate.
9. 5.9/Fs for 32-kHz sample rate.
10. Deemphasis is available only in 44.1 kHz.
11. 6.5 dB for 32-kHz sample rate.
12. 34/Fs for 32-kHz sample rate.
13. 5.2/Fs for 32-kHz sample rate.
14. 3.9 dB for 32-kHz sample rate (passband droop 10 Hz to 15 kHz).

Table 3-6. DAC High-Pass Filter (HPF) Characteristics

Test conditions (unless specified otherwise): Gains are all set to 0 dB; T_A = +25°C.

Parameter [1]		Minimum	Typical	Maximum	Units
Passband [2]	–0.05-dB corner	—	0.18×10^{-3}/N	—	Fs
	–3.0-dB corner	—	19.5×10^{-6}/N	—	Fs
Passband ripple (0.417×10^{-3}/N Fs to 0.417/N Fs; normalized to 0.417/N Fs) [2]		—	—	0.01	dB
Phase deviation @ 0.453×10^{-3}/N Fs [2]		—	2.45	—	°
Filter settling time [3]		—	0.56 [4]	—	s

1. Response scales with Fs in PCM Mode. Specifications are normalized to Fs and are denormalized by multiplying by Fs. For DSD Mode, Fs is 44.1 kHz.
2. For PCM Single-Speed Mode, N = 1.
   For PCM Double-Speed Mode, N = 2.
   For PCM Quad-Speed Mode, N = 4.
   For PCM Octuple-Speed Mode, N = 8.
   For DSD 64 x Fs Mode, N = 1.
   For DSD 128 x Fs Mode, N = 1.
3. Required time for the magnitude of the DC component present at the output of the HPF to reach 5% of the applied DC signal.
4. Filter settling time is 0.775 seconds at Fs = 32 kHz.

Table 3-7. DSD Combined Digital and On-Chip Analog Filter Response [1]

Test conditions (unless specified otherwise): Digital gains are all set to 0 dB; T_A = +25°C; PDN_XTAL = 0, MCLK_INT = 1, and MCLK_SRC_SEL = 00 (crystal frequency f_{XTAL} = 22.5792 MHz).

	Parameter		Minimum	Typical	Maximum	Units
DSD Processor Mode	Passband	to –3-dB corner	—	50	—	kHz
	Frequency response 20 Hz to 20 kHz		–0.05	—	0.05	dB
	Roll-off		27	—	—	dB/Oct

1. Filter response is by design.

Table 3-8. Digital Interface Specifications and Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 shows CS4399 connections; GNDD = GNDCP = GNDA = 0 V; voltages are with respect to ground; parameters can vary with VL and VP; typical performance data taken with VP = 3.6 V, VCP = VA = 1.8 V, VD = 1.8V and VL = 1.8 V; min/max performance data taken with VP = 3.6 V, VCP = VA = 1.8 V, VD = 1.8V and VL = 1.8 V; T_A = +25°C; C_L = 60 pF.

Parameters [1]		Symbol	Minimum	Maximum	Units
Input leakage current [2,3]	LRCK1, DSDB/LRCK2	I_{in}	—	±4	µA
	SDIN1, SCLK1, DSDA/SDIN2, DSDCLK/SCLK2		—	±3	µA
	HP_DETECT		—	±100	nA
	$\overline{SDA}$, SCL		—	±100	nA
	$\overline{INT}$, RESET		—	±100	nA
Internal weak pull-down		—	550	2450	kΩ
Input capacitance		—	—	10	pF
$\overline{INT}$ current sink (V_{OL} = 0.3 V maximum)		—	825	—	µA
VL Logic (non-I²C)	High-level output voltage (I_{OH} = –100 µA)	V_{OH}	0.9•VL	—	V
	Low-level output voltage	V_{OL}	—	0.1•VL	V
	High-level input voltage	V_{IH}	0.7•VL	—	V
	Low-level input voltage	V_{IL}	—	0.3•VL	V
VL Logic (I²C only)	Hysteresis voltage (Fast Mode and Fast Mode Plus)	V_{HYS}	0.05•VL	—	V
	Low-level output voltage	V_{OL}	—	0.2•VL	V
	High-level input voltage	V_{IH}	0.7•VL	—	V
	Low-level input voltage	V_{IL}	—	0.3•VL	V
HP_DETECT [4]	High-level input voltage	V_{IH}	0.93•VP	—	V
	Low-level input voltage	V_{IL}	—	2.0	V
HP_DETECT current to VCP_FILT– [4]		I_{HP_DETECT}	1.00	2.91	µA

1. See Table 1-1 for serial and control-port power rails.
2. Specification is per pin.
3. Includes current through internal pull-up or pull-down resistors on pin.
4. The HP_DETECT input circuit allows the HP_DETECT signal to be as low of a voltage as VCP_FILT– and as high as VP. Section 4.4.1 provides configuration details.

Table 3-9. CLKOUT Characteristics

Test conditions (unless specified otherwise): GNDD = GNDCP = GNDA = 0 V; voltages are with respect to ground; VP = 3.6 V, VCP = VA = 1.8 V, VL = VD = 1.8 V; C_L = 60 pF; PLL reference input must meet the phase-noise mask specified in Fig. 4-12; TA = +25°C; Output jitter is measured from 100 Hz to half of the output frequency.

Parameters		Symbol	Minimum	Typical	Maximum	Units
CLKOUT output frequency		f_{CLKOUT}	2.8224	3	3.072	MHz
			5.6448	6	6.144	MHz
			7.5264	8	8.192	MHz
			11.2896	12	12.288	MHz
CLKOUT output duty cycle		—	40	50	60	%
CLKOUT output TIE jitter (RMS)	CLKOUT_SRC_SEL = 01	t_{JIT}	—	500	—	ps

Table 3-10. PLL Characteristics

Test conditions (unless specified otherwise): GNDD = GNDCP = GNDA = 0 V; voltages are with respect to ground; VP = 3.6 V, VCP = VA = 1.8 V, VL = VD = 1.8 V; PLL reference input must meet the phase-noise mask specified in Fig. 4-12; TA = +25°C.

Parameters	Symbol	Minimum	Typical	Maximum	Units
PLL output frequency	f_{out}	22.5792	24	24.576	MHz
PLL lock time	t_{Lock}	—	620	1000	µs
PLL reference clock input	—	—	11.2896	—	MHz
		—	22.5792	—	MHz
		—	12.2880	—	MHz
		—	24.5760	—	MHz
		—	9.6000	—	MHz
		—	19.2000	—	MHz
		—	12.0000	—	MHz
		—	24.0000	—	MHz
		—	13.0000	—	MHz
		—	26.000	—	MHz
PLL reference clock input jitter	—	—	—	50	ps

Table 3-11. Crystal Characteristics

Test conditions (unless specified otherwise): GNDD = GNDCP = GNDA = 0 V; voltages are with respect to ground; VP = 3.6 V, VCP = VA = 1.8 V, VL = VD = 1.8 V; T_A = +25°C

Parameters [1]	Symbol	Minimum	Typical	Maximum	Units
Crystal oscillator frequency	f_{XTAL}	22.57	22.5792/ 24.576	24.58	MHz
Crystal load capacitance	C_{L_XTAL}	5	—	8	pF
Equivalent series resistance	esr_{XTAL}	—	—	100	Ω
Startup time	t_{XTAL_pup}	—	—	8	ms
Shunt capacitance	C_O	—	—	0.8	pF
Maximum drive level	—	200	—	—	µW

1. Refer to Section 5.3 for supported crystal options.

Table 3-12. Power-Supply Rejection Ratio (PSRR) Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 shows CS4399 connections; input test signal held low (all zero data); GNDA = GNDL = GNDCP = 0 V; voltages are with respect to ground; VL = VA = VD = 1.8 V, VP = 3.6 V; When testing PSRR, PCM input test signal held low (all zero data); T_A = +25°C; PCM_AMUTE = 0.

Parameter [1]		Minimum	Typical	Maximum	Units
AOUTx PSRR with 100-mVpp signal AC coupled to VA supply	217 Hz 1 kHz 20 kHz	— — —	75 75 70	— — —	dB dB dB
AOUTx PSRR with 100-mVpp signal AC coupled to VCP supply	217 Hz 1 kHz 20 kHz	— — —	80 80 60	— — —	dB dB dB
AOUTx PSRR with 100-mVpp signal AC coupled to VP supply	217 Hz 1 kHz 20 kHz	— — —	100 100 80	— — —	dB dB dB

1. PSRR test configuration: Typical PSRR can vary by approximately 6 dB below the indicated values.

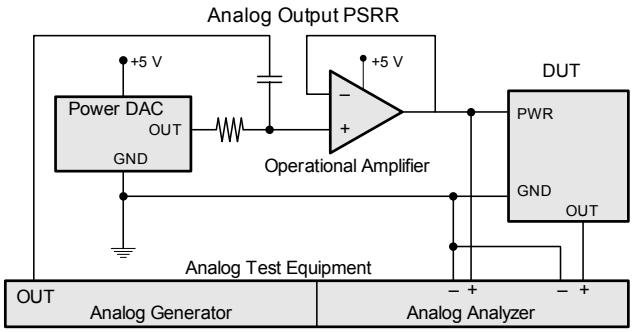


Table 3-13. DC Characteristics

Test conditions (unless otherwise specified): Fig. 2-1 shows CS4399 connections; GNDD = GNDA = 0 V; all voltages with respect to ground.

Parameters			Minimum	Typical	Maximum	Units
VCP_FILT (No load connected to AOUTx) EXT_VCPFILT = 0	VP_LDO Mode	VCP_FILT+ pin (HV_EN = 1) VCP_FILT+ pin (HV_EN = 0) VCP_FILT– pin (HV_EN = 1) VCP_FILT– pin (HV_EN = 0)	— — — —	3.0 2.6 –3.0 –2.6	— — — —	V V V V
	VCP Mode	VCP_FILT+ pin VCP_FILT– pin	— —	VCP –VCP	— —	V V
–VA		–VA pin	—	– VA	—	V
Other DC filter characteristics	FILT+ voltage		—	–0.35	—	V
	FILT– voltage		—	0.35	—	V
	Analog output current limiter on threshold.		—	120	160	mA
	VD power-on reset threshold (V_{POR})	Up Down	— —	1.15 0.950	— —	V V

Table 3-14. Power Consumption

Test conditions (unless specified otherwise): Fig. 2-1 shows CS4399 connections; GNDA = GNDCP = GNDD = 0 V; voltages are with respect to ground; performance data taken with VA = VCP = VD = VL = 1.8 V; VP = 3.6 V; T_A = +25°C; ASP_SPRATE = 0001(44.1-kHz mode); MCLK_INT= 1 (22.5792 MHz); MCLK_SRC_SEL = 00; all other fields are set to defaults; no signal on any input; control port inactive; all serial ports are set to Slave or Master Mode as indicated, input clock/data are held low unless active; test load is R_L = 600 Ω and C_L = 1 nF for AOUTx; measured values include currents consumed by the DAC and do not include current delivered to external loads unless specified otherwise (e.g., from AOUTx outputs); see Fig. 2-1.

Use Cases			Typical Current (µA)						Total Power (µW)
			P_{OUT}	i_{VCP}	i_{VA}	i_{VD}	i_{VL}	i_{VP}	
1		Off [1]	—	0	0	0	0	6	22
2		Standby [2] HPDETECT enabled	—	0	0	256	0	32	576
3	A	Playback External MCLK = 22.5792 MHz, I²S/DoP Stereo AOUT	Quiescent [3]	4021	7302	1444	40	32	23167

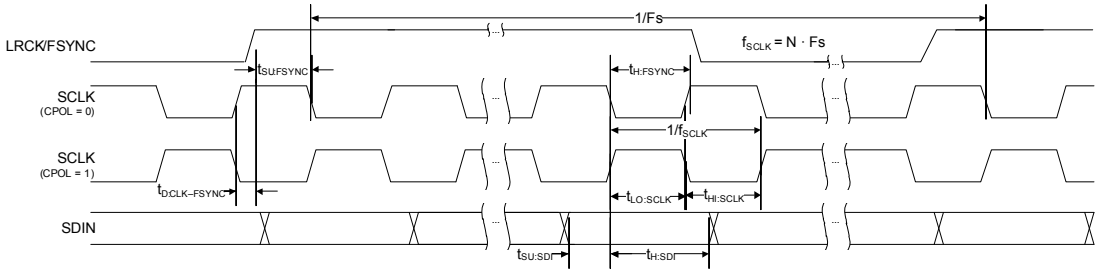
1. Off configuration: Clock/data lines held low; $\overline{\text{RESET}}$ = LOW; VA = VD = VL = 0 V, VCP = 0 V, VP = 3.6 V.
2. Standby configuration: Clock/data lines held low; $\overline{\text{RESET}}$ = HIGH; VA = VD = VL = 1.8 V, VCP = 1.8 V, VP = 3.6 V; HP_DETECT_CTRL = 11 (enabled); HPDETECT_PLUG_INT_MASK=0 (unmasked); PDN_XTAL = 1, MCLK_SRC_SEL = 10 (RCO selected as MCLK source).
3. Quiescent configuration: data lines held low; $\overline{\text{RESET}}$ = HIGH; VA = 1.8 V, VD = VL = VCP = 1.8 V, VP = 3.6 V. Serial port, I²S/DoP Mode (ASP and SDIN, ASP_M/Sb = 0); PDN_XTAL = 1.

Table 3-15. Serial-Port Interface Characteristics

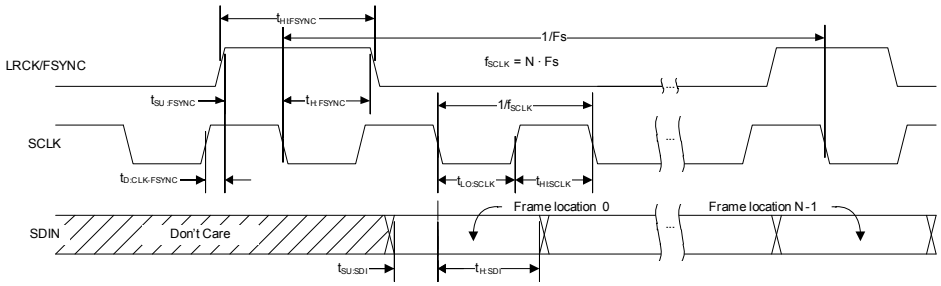
Test conditions (unless specified otherwise): Fig. 2-1 shows CS4399 connections; GNDA = GNDCP = GNDD = 0 V; voltages are with respect to ground; parameters can vary with VL; typical performance data taken with VL = VD = VA = VCP = 1.8 V, VP = 3.6 V; min/max performance data taken with VL = 1.8 V; VD = VA = VCP = 1.8 V, VP = 3.6 V; T_A = +25°C; C_L = 60 pF; Logic 0 = ground, Logic 1 = VL; output timings are measured at V_{OL} and V_{OH} thresholds (see Table 3-8).

Parameters [1,2,3,4,5]		Symbol	Minimum	Typical	Maximum	Units
FSYNC frame rate		Fs	(See Section 4.8.5)			kHz
FSYNC high period [6]		$t_{HI:FSYNC}$	$1/f_{SCLK}$	—	$(n–1)/f_{SCLK}$	s
Master Mode	FSYNC duty cycle xSP_5050 = 1	—	45	—	55	%
	FSYNC delay time after SCLK launching edge [7]	$t_{D:CLK–FSYNC}$	—	—	20	ns
	SCLK frequency	f_{SCLK}	—	—	f_{MCLK_INT}	MHz
	SCLK high period [8]	$t_{HI:SCLK}$	$1/(2•f_{SCLK}) – 1/f_{MCLK\_INT}$	—	$1/(2•f_{SCLK}) + 1/f_{MCLK\_INT}$	ns
	SDIN setup time before SCLK latching edge [7]	$t_{SU:SDI}$	10	—	—	ns
	SDIN hold time after SCLK latching edge [7]	$t_{H:SDI}$	5	—	—	ns
Slave Mode	FSYNC setup time before SCLK latching edge [7]	$t_{SU:FSYNC}$	10	—	—	ns
	FSYNC hold time after SCLK latching edge [7]	$t_{H:FSYNC}$	5	—	—	ns
	SCLK frequency	f_{SCLK}	—	—	24.58	MHz
	SCLK high period	$t_{HI:SCLK}$	16	—	—	ns
	SCLK low period	$t_{LO:SCLK}$	16	—	—	ns
	SDIN setup time before SCLK latching edge [9]	$t_{SU:SDI}$	10	—	—	ns
	SDIN hold time after SCLK latching edge [7]	$t_{H:SDI}$	5	—	—	ns

1. MCLK in this table refers to the external clock supplied to the MCLK pin ($MCLK_{EXT}$).
2. Output clock frequencies follow the master clock ($MCLK_{EXT}$) frequency proportionally. Any deviation of the clock source from the nominal supported rates are directly imparted to the output clock rate by the same factor (e.g., +100-ppm offset in the frequency of $MCLK_{EXT}$ becomes a +100-ppm offset in LRCK/FSYNC and SCLK).
3. I²S interface timing



4. TDM interface timing
   (shown with xSP_FSD = 010, xSP_LCHI = 1)



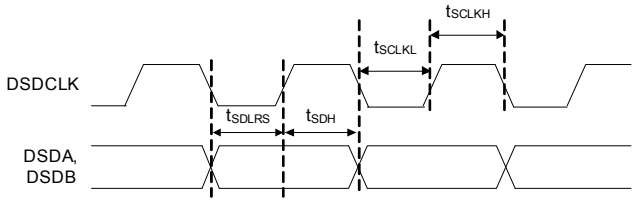
5. Applies to Master and Slave Modes, unless specified otherwise.
6. Maximum LRCK duty cycle is equal to frame length, in SCLK periods, minus 1. Maximum duty cycle occurs when LRCK high (xSP_LCHI) is set to 768 SCLK periods and LRCK period (xSP_LCPR) is set to 769 SCLK periods.
7. Data may be latched/launched on either the rising or falling edge of SCLK.
8. SCLK duty cycle in Master Mode depends on Master Mode clock configuration, and can vary by up to 1 $MCLK_{EXT}$ period.
9. Data is latched/launched on the rising or falling edge of SCLK as determined by xSP_SCPOL_OUT, xSP_SCPOL_IN, and xSP_FSD bits. See the SCLK launching specs in Table 3-15.

Table 3-16. DSD Switching Characteristic

Test conditions (unless specified otherwise): Fig. 2-1 shows CS4399 connections; GNDA = GNDCP = GNDD = 0 V; voltages are with respect to ground; parameters can vary with VL; typical performance data taken with VL = VD = VA = VCP = 1.8 V, VP = 3.6 V; min/max performance data taken with VL = 1.8 V; VD = VA = VCP = 1.8 V, VP = 3.6 V; T_A = +25°C; C_L = 60 pF; Logic 0 = ground, Logic 1 = VL; output timings are measured at V_{OL} and V_{OH} thresholds (see Table 3-8).

Parameter [1,2]	Symbol	Minimum	Typical	Maximum	Units
DSDCLK duty cycle	—	40	—	60	%
DSDCLK pulse width low	t_{SCLKL}	80	—	—	ns
DSDCLK pulse width high	t_{SCLKH}	80	—	—	ns
DSDCLK frequency (64× oversampled) (128× oversampled)	—	1.024 2.048	2.8224 5.6448	$f_{MCLK\_INT}/8$ $f_{MCLK\_INT}/4$	MHz MHz
DSDA/DSDB valid to DSDCLK rising setup time	t_{SDLRS}	20	—	—	ns
DSDCLK rising to DSDA or DSDB hold time	t_{SDH}	20	—	—	ns
DSD clock to data transition (Phase Modulation Mode)	t_{DPM}	–20	—	20	ns

1. Serial audio input interface timing



2. Phase modulation mode serial audio input interface timing

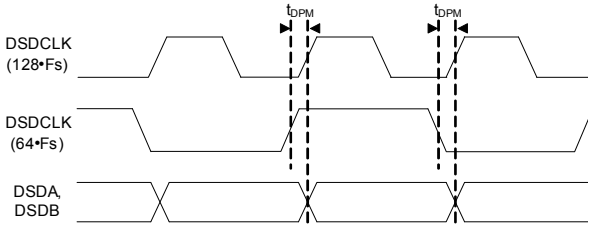


Table 3-17. I²C Slave Port Characteristics

Test conditions (unless specified otherwise): Fig. 2-1 shows typical connections; Inputs: GNDA = GNDL = GNDCP = 0 V; all voltages with respect to ground; VL = 1.8 V; inputs: Logic 0 = GNDA = 0 V, Logic 1 = VL; T_A = +25°C; SDA load capacitance equal to maximum value of C_B = 400 pF; minimum SDA pull-up resistance, $R_{P(min)}$.[1] Table 3-1 describes some parameters in detail. All specifications are valid for the signals at the pins of the CS4399 with the specified load capacitance.

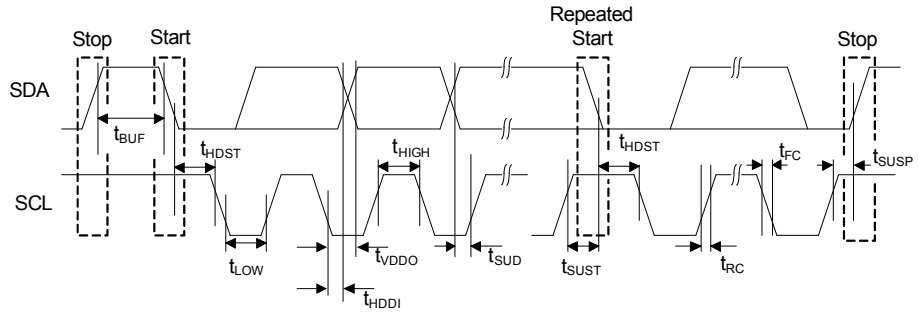
Parameter [2]	Symbol [3]	Minimum	Maximum	Units
SCL clock frequency	f_{SCL}	—	1000	kHz
Clock low time	t_{LOW}	500	—	ns
Clock high time	t_{HIGH}	260	—	ns
Start condition hold time (before first clock pulse)	t_{HDST}	260	—	ns
Setup time for repeated start	t_{SUST}	260	—	ns

Table 3-17. I²C Slave Port Characteristics *(Cont.)*

Test conditions (unless specified otherwise): Fig. 2-1 shows typical connections; Inputs: GNDA = GNDL = GNDCP = 0 V; all voltages with respect to ground; VL = 1.8 V; inputs: Logic 0 = GNDA = 0 V, Logic 1 = VL; T_A = +25°C; SDA load capacitance equal to maximum value of C_B = 400 pF; minimum SDA pull-up resistance, $R_{P(min)}$.[1] Table 3-1 describes some parameters in detail. All specifications are valid for the signals at the pins of the CS4399 with the specified load capacitance.

Parameter [2]		Symbol [3]	Minimum	Maximum	Units
Rise time of SCL and SDA	Standard Mode Fast Mode Fast Mode Plus	t_{RC}	— — —	1000 300 120	ns ns ns
Fall time of SCL and SDA	Standard Mode Fast Mode Fast Mode Plus	t_{FC}	— — —	300 300 120	ns ns ns
Setup time for stop condition		t_{SUSP}	260	—	ns
SDA setup time to SCL rising		t_{SUD}	50	—	ns
SDA input hold time from SCL falling [4]		t_{HDDI}	0	—	ns
Output data valid (Data/Ack) [5]	Standard Mode Fast Mode Fast Mode Plus	t_{VDDO}	— — —	3450 900 450	ns ns ns
Bus free time between transmissions		t_{BUF}	500	—	ns
SDA bus capacitance	SCL frequency = 1 MHz, V_L = 1.8 V SCL frequency ≤ 400 kHz	C_B	— —	400 400	pF pF
SCL/SDA pull-up resistance [1]	V_L = 1.8 V	R_P	350	—	Ω
Pulse width of spikes to be suppressed		t_{PS}	—	50	ns
Switching time between RCO and MCLK_INT [6]		—	150	—	µs
Power-up delay (delay before I²C can communicate after $\overline{\text{RESET}}$ released)		t_{PUD}	1500	—	µs

1. The minimum R_P value (resistor shown in Fig. 2-1) is determined by using the maximum level of VL, the minimum sink current strength of its respective output, and the maximum low-level output voltage V_{OL}. The maximum R_P value may be determined by how fast its associated signal must transition (e.g., the lower the value of R_P, the faster the I²C bus is able to operate for a given bus load capacitance). See I²C bus specification referenced in Section 13.
2. All timing is relative to thresholds specified in Table 3-8, V_{IL} and V_{IH} for input signals, and V_{OL} and V_{OH} for output signals.
3. I²C control-port timing



4. Data must be held long enough to bridge the transition time, t_F, of SCL.
5. Time from falling edge of SCL until data output is valid.
6. Upon setting MCLK_SRC_SEL and sending the I²C stop condition, the switching of RCO and other MCLK_INT sources occurs. A least wait time as specified is required after changing MCLK_SRC_SEL and sending the I²C stop condition before the next I²C transaction is initiated.

4 Functional Description

This section describes the general theory of operation of the CS4399, tracing the signal and control flow through the various blocks within the device. It comprises the following sections:

- Section 4.1, “Overview”
- Section 4.2, “Analog Outputs”
- Section 4.3, “Class H Output”
- Section 4.4, “ Headphone Presence Detect”
- Section 4.5, “Clocking Architecture”
- Section 4.6, “Clock Output and Fractional-N PLL”
- Section 4.7, “Filtering Options”
- Section 4.8, “Audio Serial Port (ASP)”
- Section 4.9, “DSD Interface”
- Section 4.10, “DSD and PCM Mixing”
- Section 4.11, “Standard Interrupts”
- Section 4.12, “Control Port Operation”

4.1 Overview

4.1.1 Analog Outputs

The analog output block includes separate pseudodifferential output. An on-chip inverting charge pump creates a positive and negative voltage equal to the input, allowing an adaptable, full-scale output swing centered around ground. The resulting internal supply can be ±VCP, or ±VP_LDO (either ±3.0 V with HV_EN = 1 or ±2.6 V with HV_EN = 0).

4.1.2 Headphone Detection

The CS4399 detects the presence of a headphone and notifies the application processor to wake up through an interrupt event.

4.1.3 Audio Interfaces and Supported Formats

There are two serial input ports on the CS4399, the audio serial port (ASP) and the auxiliary serial port (XSP). The ASP on the CS4399 supports I²S, TDM, and DoP (DSD over PCM) formats up to a 384-kHz sample rate. The XSP on the CS4399 supports the DoP format up to a 352.8-kHz sample rate.

The CS4399 also has a dedicated DSD interface to support up to 128•Fs. The DSD interface shares pins with the XSP.

4.1.4 System Clocking

The CS4399 internal MCLK can be sourced from three options:

- Direct MCLK/crystal mode. The internal MCLK is provided through XTI/MCLK pin directly or generated by crystal oscillator.
- PLL mode. A PLL reference CLK is provided externally through XTI/MCLK. The PLL is configured, and output is used as the internal MCLK.
- RCO mode. An internal RCO is used as the internal MCLK. This mode can support HP detection and I²C communication. DAC playback function is not supported.

The clock output is provided for audio applications that require high quality audio rate system clock. This clock output can be sourced from the following two options:

- The clock generated by the CS4399 crystal oscillator.
- Output of the internal Fractional-N PLL that refers to MCLK input. See Section 4.6.1 for supported frequencies.

The internal MCLK is used to generate serial port clocks. See Table 4-6 for supported LRCK combinations.

4.1.5 System Interrupts

The CS4399 includes an open-drain interrupt output ($\overline{\text{INT}}$ pin). Interrupt mask registers control whether an event associated with an interrupt status/mask bit pair triggers the assertion of $\overline{\text{INT}}$. All types of interrupts are described in Section 4.10.

4.1.6 System Reset

The CS4399 offers two types of reset options:

- Asserting $\overline{\text{RESET}}$. If $\overline{\text{RESET}}$ is asserted, all registers and all state machines are immediately set to their default values/states. No operation can begin until $\overline{\text{RESET}}$ is deasserted. Before normal operation can begin, $\overline{\text{RESET}}$ must be asserted at least once after the VP supply is first brought up.
- Power-on reset (POR). If the VD supply is lower than the POR threshold specified in Table 3-13, the VD register fields and the state machines are held in reset, setting them to their default values/states. The POR releases the reset when the VD supply goes above the POR threshold. When the VD supply is turned on, the VL and VA supplies must also be turned on at the same time.

4.1.7 Power Down

The CS4399 has a register byte to power down individual components on the chip. Before any change can be applied to an individual component (except PLL), the block must be powered down first. For the PLL, changes can be applied after PLL_START is cleared.

The PDN_HP bit is responsible for enabling or disabling the playback signal chain operation. All the necessary components for playback operation need to be powered up and configured properly before PDN_HP is cleared. To disable the playback signal chain, PDN_HP is set. PDN_HP needs to be set before making any changes to the playback signal chain setup, except the following functions:

- Volume and mute related functions
- PCM filter settings (see Section 7.5.2)

Before ASP, XSP, or DSDIF can safely power down, PDN_HP must be asserted, and PDN_DONE_INT must be present. For XTAL or PLL used as the source of internal MCLK, PDN_HP needs to be set first and MCLK source needs to be properly switched away before PDN_XTAL or PDN_PLL is set. If PLL output is only used as the source of CLKOUT, PDN_PLL can be set without PDN_HP being asserted. If the steps described above are not followed, the CS4399 enters an unresponsive state.

PDN_CLKOUT does not require PDN_HP to be set before it is asserted.

Recommended power-up and power-down sequences can be found in the Section 5.2.

4.2 Analog Outputs

The CS4399 provides an analog output that is derived from the digital audio input ports. This section describes the general flow of the analog outputs.

4.2.1 Analog Output Signal Flow

The CS4399 signal flow is shown in Fig. 4-1.

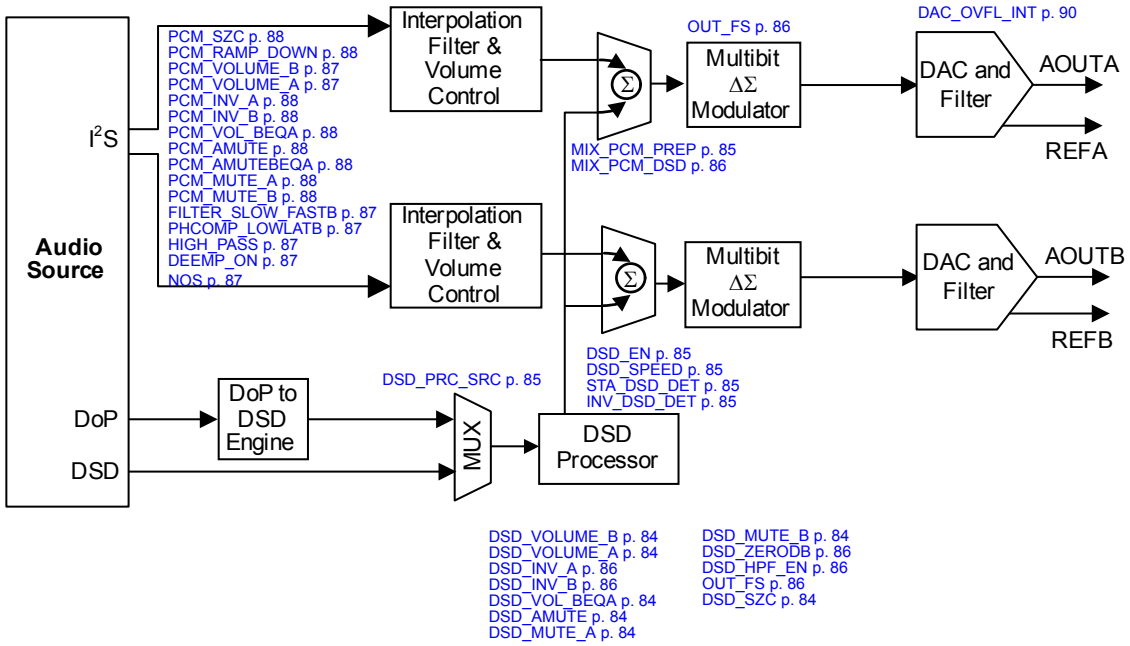


Figure 4-1. Analog Output Signal Flow

The CS4399 has 2 settings of full scale voltage, which are determined by OUT_FS[1:0]. The proper full scale voltage must be set first, and the digital volume settings is used to control signal levels.

The CS4399 digital volume control allows independent control of the signal level in 1/2 dB increments from 0 dB (0b0000 0000) to –127 dB (0b1111 1110) by using x_VOLUME_y (where "x" is either PCM or DSD; "y" is either A or B) register. When the x_VOL_BEQA bit is set, both volumes can be changed simultaneously using x_VOLUME_A). The volume changes are implemented as dictated by PCM_SZC[1:0] and DSD_SZC in the signal control register (see Section 7.4.3 and Section 7.5.5). If soft ramping is enabled, gain and attenuation changes are carried out by incrementally changing the volume level in 1/8-dB steps, from the previous level to the new level. For PCM, when PCM_SZC[1:0] = 2, the volume level changes at an approximate rate of 1 dB/ms. For DSD, when DSD_SZC = 1, the volume level also changes at an approximate rate of 1 dB/ms during power up or when coming out of a mute state (DSD_MUTE_x = 1). Note that when recovering from an error state caused by static DSD data (DSD_STUCK_INT = 1), the volume output will resume at the level specified in DSD_VOLUME_x registers. Both channels can be inverted by setting the INV_A and INV_B bits.

The CS4399 provides individual ramp-up control option (from the global soft ramp settings) for a specific scenario. The PCM_RAMP_DOWN bit is for the scenario when the interpolation filter switches during PCM playback. Refer to the register description for setting details.

The CS4399 can mute both channels simultaneously or independently. Also, it can auto-mute on both PCM stream and DSD stream when mute pattern is identified (defined in PCM_AMUTE and DSD_AMUTE). Additional signal and mute control options can be found in Section 7.4.3 and Section 7.5.5.

The CS4399 has an independent set of controls for the DSD processor path as shown in Fig. 4-1. The DSD processor also offers the control bit SIGCTL_DSDEQPCM, which maps the PCM_x setting to DSD_x setting, once enabled. As a result, some of the DSD_x register settings are ignored. The registers affected are DSD_VOL_BEQA, DSD_SZC, DSD_AMUTE, DSD_AMUTE_BEQA, DSD_MUTE_A, DSD_MUTE_B, DSD_INV_A, DSD_INV_B, DSD_SWAP_CHAN, and

DSD_COPY_CHAN. Refer to Section 7.4.1–Section 7.4.7 for control register details.

4.3 Class H Output

Fig. 4-2 shows the Class H operation.

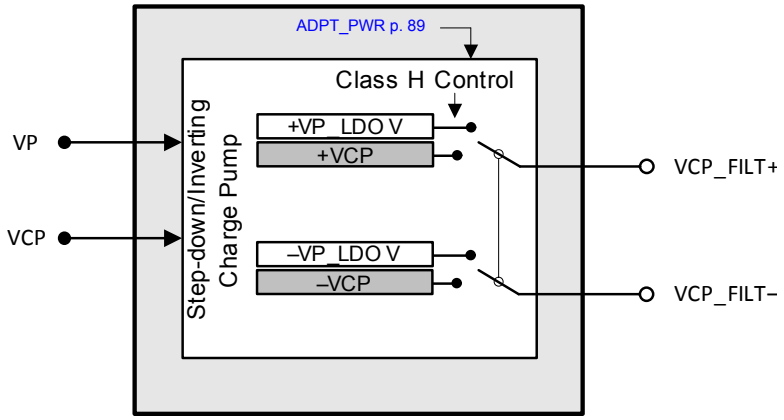


Figure 4-2. Class H Operation

The CS4399 outputs use Cirrus Logic two-mode Class H technology. This prevents unnecessarily wasting energy during low power passages of program material or when the program material is played back at a low volume level.

The internal charge pump is the central component of the two-mode Class H technology implemented in the CS4399. The charge pump receives its input voltage from the voltage present on the VCP or VP pin. From this input voltage, the charge pump creates the differential rail voltages supplied to the output stages.The charge pump can supply two sets of differential rail voltages: ±VCP and ±VP_LDO.

HV_EN setting, as shown in Fig. 4-3, determines the VP_LDO voltage as shown in Table 4-1. HV_EN = 1 setting is required to support the 1.7-V full-scale voltage. In this setting, minimum VP is required to be higher than 3.3 V. When HV_EN = 0, the max output voltage is 1.4-V RMS full-scale voltage. In this setting, minimum VP is required to be higher than 3 V.

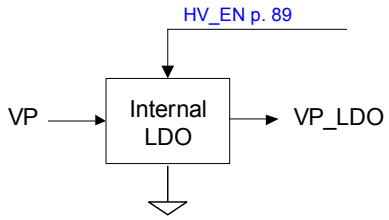


Figure 4-3. Internal LDO Configuration

Table 4-1. VP_LDO Voltage Per HV_EN Setting

HV_EN	VP_LDO Voltage
0	2.6 V
1	3.0 V

Table 4-2 shows the nominal signal and volume level ranges when the output is set to the adapt modes explained in Section 4.3.1. If the signal level is greater than the maximum value of this range, then clipping can occur.

Table 4-2. Class H Supply Modes

Mode	Class H Supply Level	Signal [1] or Volume Level Range [2,3,]
0	±VP_LDO V, internally regulated from VP	≥ –11 dB
1	±VCP	< –11 dB

1. In adapt-to-signal, the volume level ranges are approximations but are within –0.5 dB from the values shown.

2. Relative to digital full scale with output gain set to 0 dB.
3. In fixed modes, clipping can occur if the signal level exceeds the maximum of this range due to setting the supply too low.

4.3.1 Power Supply Control Options

This section describes the two types of operation: standard Class AB and adapt-to-output signal. The set of rail voltages supplied to the amplifier output stages depends on the ADPT_PWR (see p. 89) setting.

4.3.1.1 Standard Class AB Operation (ADPT_PWR = 001 or 010)

If ADPT_PWR is set to 001 or 010, the rail voltages supplied to the amplifiers are held to ±VP_LDO or ±VCP, respectively. The rail voltages supplied to the output stages are held constant, regardless of the output signal level. The CS4399 outputs simply operate in a traditional Class AB configuration.

4.3.1.2 Adapt-to-Output Signal (ADPT_PWR = 111)

If ADPT_PWR is set to 111, the rail voltage sent to the output stages is based solely on whether the signal sent to the amplifiers would cause the amplifiers to clip when operating on the lower set of rail voltages at certain threshold values.

- If it would cause clipping, the control logic instructs the charge pump to provide the next higher set of rail voltages to the amplifiers.
- If it would not cause clipping, the control logic instructs the charge pump to provide the lower set of rail voltages to the amplifiers, eliminating the need to advise the CS4399 of volume settings external to the device.

4.3.2 Power-Supply Transitions

Charge-pump transitions from the lower to the higher set of rail voltages occur on the next FLYN/FLYP clock cycle. Despite the system's fast response time, the VCP_FILT pin's capacitive elements prevent rail voltages from changing instantly. Instead, the rail voltages ramp up from the lower to the higher supply, based on the time constant created by the output impedance of the charge pump and the capacitor on the VCP_FILT pin (the transition time is approximately 20 µs).

Fig. 4-4 shows Class H supply switching. During this charging transition, a high dv/dt transient on the inputs may briefly clip the outputs before the rail voltages charge to the full higher supply level. This transitory clipping has been found to be inaudible in listening tests.

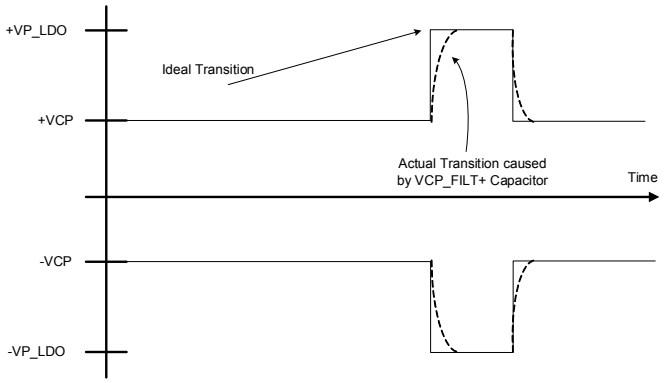


Figure 4-4. VCP_FILT Transitions

When the charge pump transitions from the lower to higher set of rail voltage, there is no delay associated with the transition.

When the charge pump transitions from the higher to the lower set of rail voltages, there is an approximate 5.5-s delay before the charge pump supplies the lower rail voltages to the amplifiers. This hysteresis ensures that the charge pump does not toggle between the two rail voltages as signals approach the clip threshold. It also prevents clipping in the

instance of repetitive high-level transients in the input signal. Fig. 4-5 shows examples of this transitional behavior.

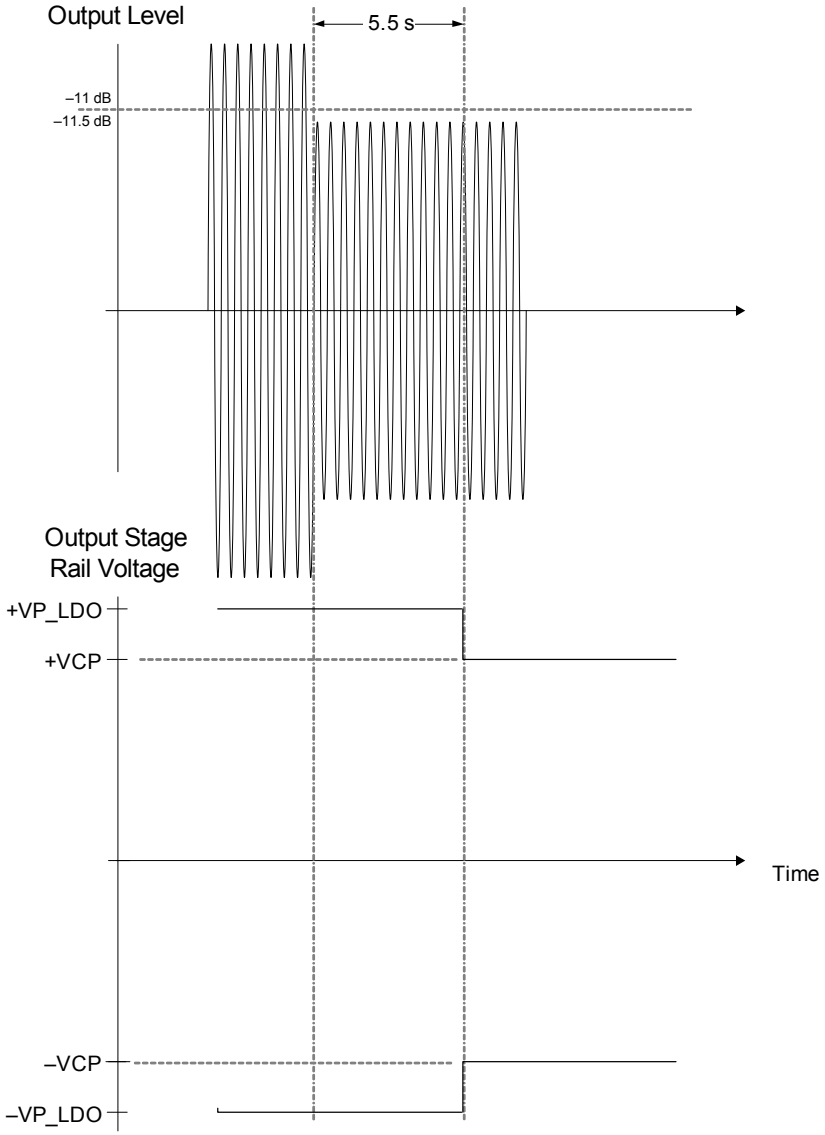


Figure 4-5. VCP_FILT Hysteresis

4.3.3 External VCP_FILT Supply Mode

To bypass the CS4399 Class-H charge-pump circuit, provide external VCP_FILT± supply with the following conditions:

- When CS4399 is operating, apply +3.0 V with ±5% accuracy to VCP_FILT+ and apply –3.0 V with ±5% accuracy to VCP_FILT–.
- When CS4399 is powered down, external circuits present Hi-Z state to the VCP_FILT+ pin (>1k impedance) and VCP_FILT– pin (>10k impedance).

- To avoid possible damage, VCP_FILT± pins must remain within the absolute maximum rating specified.

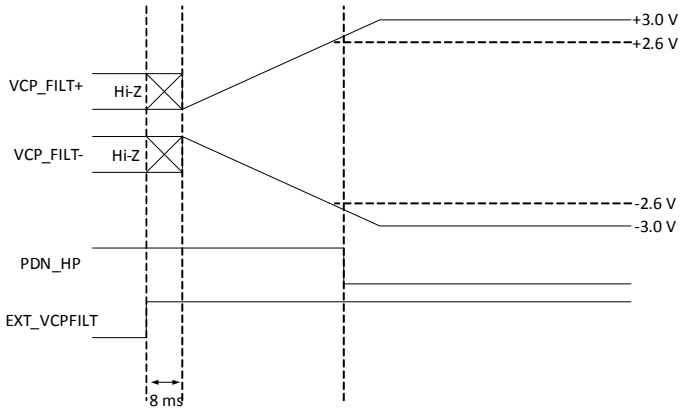


Figure 4-6. External VCP_FILT Power-Up Sequence

For powering up CS4399 in this mode, the recommended sequence must be followed. This assumes that the CS4399 starts from the status where VCP_FILT± pin are presented with Hi-Z.

1. Set EXT_VCPFILT.
2. Wait 8 ms after I²C ACK.
3. Release and start to ramp external voltage on VCP_FILT± pin.
4. Wait until VCP_FILT+ pin voltage to be greater than +2.6V and VCP_FILT– to be less than –2.6 V.
5. Clear the PDN_HP bit.

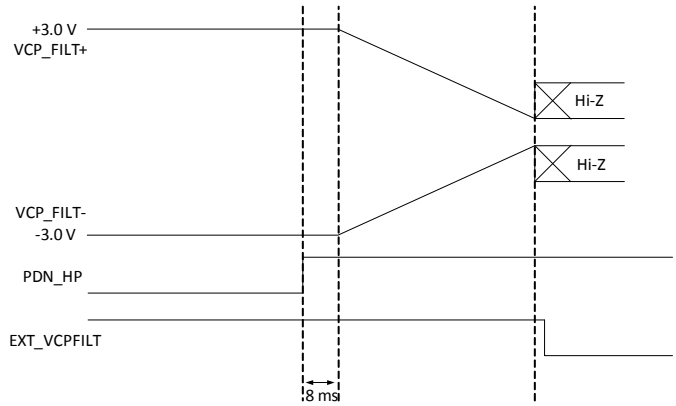


Figure 4-7. External VCP_FILT Power-Down Sequence

For powering down in this mode, use the following recommended sequence. This assumes that the CS4399 starts from the status where VCP_FILT± pin are presented with ±3.0 V, respectively.

1. Execute the power down sequence per Section 5.7.
2. Wait 8 ms after I²C ACK.
3. Start to shut-off external supply to VCP_FILT± pins.
4. Wait until Hi-Z mode is presented on VCP_FILT± pins.
5. Clear EXT_VCPFILT.

4.4 Headphone Presence Detect

The CS4399 provides headphone presence-detect functionality.

4.4.1 Headphone Presence Detect

The CS4399 supports headphone presence-detect capability via the HP_DETECT sense pin. HP_DETECT is debounced to filter out brief events before being reported to the corresponding presence-detect status bit and generating an interrupt if appropriate.

4.4.1.1 Headphone Detect Methods

CS4399 can detect the presence or absence of a plug. For a headphone-presence detect, a sense pin is connected to a terminal on the receptacle such that, if no plug is inserted, the pin is floating. If a plug is inserted, the pin is shorted to the tip (T) terminal. The presence detect function is accomplished by having a small current source inside the CS4399 to pull up the pin if it is left floating (no plug). If a plug is inserted and the sense pin is shorted to headphone output, the sense pin is shorted to the output signal and, therefore, is pulled below a certain threshold via the output stage of the HP amp. Thus, a low level at the sense pin indicates plug inserted, and a high level at the sense pin indicates plug removed.

4.4.1.2 Headphone Detect Registers

This section describes the behavior and interaction of the headphone-detect debounce register fields. See Fig. 4-8 for reference.

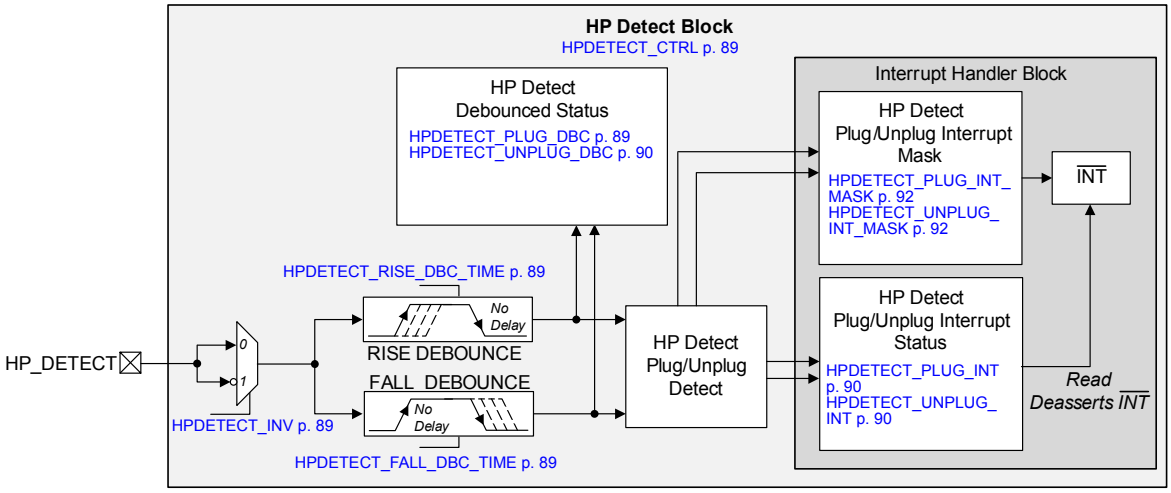


Figure 4-8. Headphone Detect Block Diagram

- HPDETECT_CTRL configures the operation of the HP detect circuit.
- HPDETECT_INV inverts the signal from the HP detect circuit.
- HPDETECT_FALL_DBC_TIME configures the HP_DETECT falling debounce time.
- HPDETECT_RISE_DBC_TIME configures the HP_DETECT rising debounce time.
- HPDETECT_PLUG_DBC shows the falling-edge-debounced version of HP_DETECT signal.
- HPDETECT_UNPLUG_DBC shows the rising-edge-debounced version of HP_DETECT signal.
- HPDETECT_PLUG_INT shows the headphone plug-in event status.
- HPDETECT_UNPLUG_INT shows the headphone unplug event status.
- HPDETECT_PLUG_INT_MASK is the interrupt mask of headphone plug-in event status.
- HPDETECT_UNPLUG_INT_MASK is the interrupt mask of headphone unplug event status.

4.4.1.3 Headphone Detect and Interrupts Setup Instructions

The following steps are required for activation of headphone-detect debounce interrupt status:

1. Ensure the I²C is ready to respond to control port command.
2. Clear the interrupt masks.

3. Write to HPDETECT_RISE_DBC_TIME and HPDETECT_FALL_DBC_TIME (see p. 89) to enable debounce for presence detect plug/unplug.
4. Set HPDETECT_CTRL to 11 to enable the HPDETECT functions.

The interrupt status bits can be found in Section 7.6.1. The status does not contain an event-capture latch (a read always yields the current condition).

4.5 Clocking Architecture

4.5.1 Master Clock (MCLK) Sources

The MCLK is required by the CS4399 to operate any functionality associated with control, serial-port operation, or data conversion. Depending on the setting of MCLK_SRC_SEL (see p. 74), the MCLK can be provided by one of following methods:

- Sourced from a crystal oscillator between XTI/MCLK and XTO pins (see Fig. 4-9), then used directly as MCLK_INT
- Externally sourced through the XTI/MCLK input pin (see Fig. 4-10)
- PLL reference clock is provided through the XTI/MCLK input pin (see Fig. 4-10), then use internal PLL to convert into MCLK_INT
- Use internal RCO as MCLK. This mode can support HP detection and I²C communication. DAC playback is not supported.

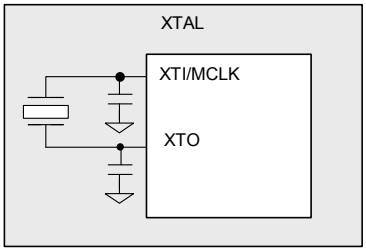


Figure 4-9. System Clocking—Crystal Mode

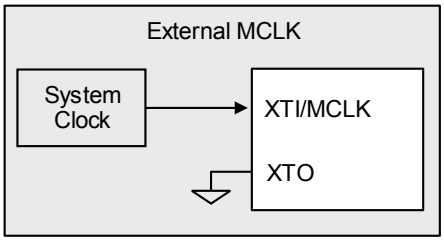


Figure 4-10. System Clocking—External MCLK Mode

If XTAL is used, the supported crystal characteristics and frequencies are listed in Table 3-11. Based on the crystal selection, XTAL_IBIAS must be set properly before powering up. The XTAL_IBIAS information can be found in Section 5.3. PDN_XTAL is cleared to start the crystal oscillator. PDN_XTAL is set to power down the crystal oscillator. The XTAL_READY_INT and XTAL_ERROR_INT status bits indicate the status of crystal operation after power-up. At t_{XTAL_pup} after the crystal oscillator is powered up, if the crystal is started successfully and ready to be used, XTAL_READY_INT is set; if the crystal is started unsuccessfully, XTAL_ERROR_INT is set. The two bits are mutually exclusive when set. Both status bits have corresponding interrupt status bits and interrupt mask bits. To be informed on the crystal status at t_{XTAL_pup} after power-up, unmask both interrupts before powering up the crystal.

When the MCLK is supplied to the device through the XTI/MCLK pin, it must comply with the phase-noise mask shown in Fig. 4-11. Its frequency must be one of the nominal MCLK_INT frequencies (22.5792 or 24.576 MHz), and its duty cycle must be between 45% to 55%.

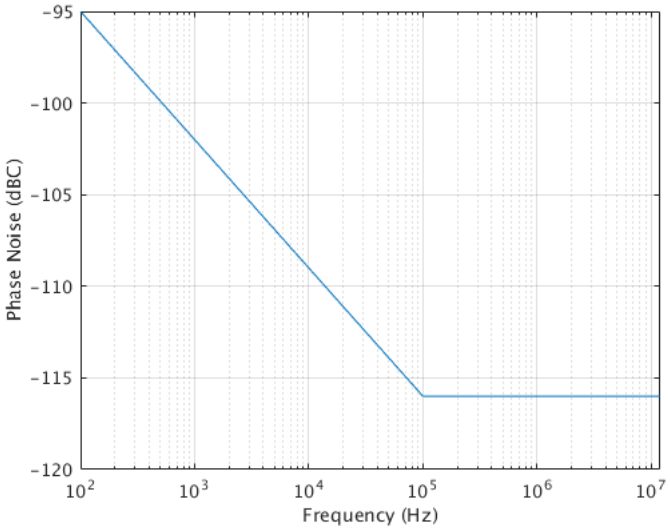


Figure 4-11. MCLK Phase Noise Mask Without PLL

When the PLL reference clock is supplied to the device through the XTI/MCLK pin, it must comply with the phase-noise mask shown in Fig. 4-12.

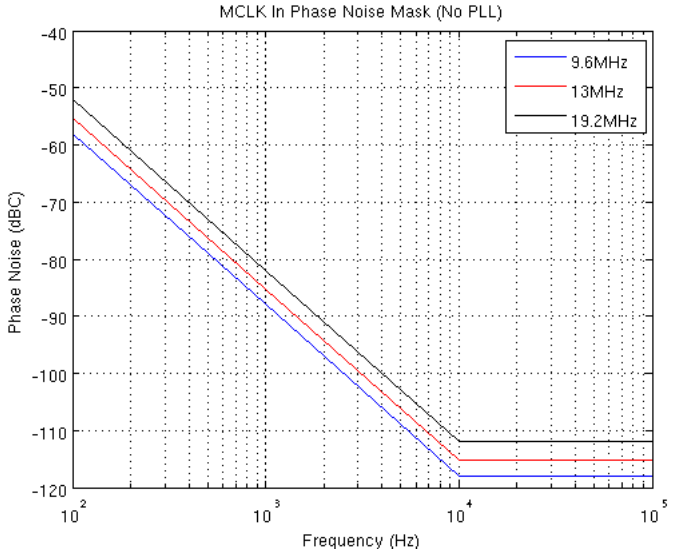


Figure 4-12. MCLK Phase Noise Mask With PLL

Further restrictions are listed in Table 4-3.

Table 4-3. MCLK Source Restrictions

Internal MCLK Source	MCLK_SRC_SEL	MCLK_INT	Restrictions
Direct MCLK or XTAL	00	0	• Nominal MCLK_INT frequency = 24.576 MHz • All specified CLKOUT frequencies (generated by PLL or XTAL) are supported • CLKOUT outputs (/2, /3, /4, /8 divide) optionally
		1	• Nominal MCLK_INT frequency = 22.5792 MHz • All specified CLKOUT frequencies (generated by PLL or XTAL) are supported • CLKOUT outputs (/2, /3, /4, /8 divide) optionally
PLL	01	0	• Nominal MCLK_INT frequency = 24.576 MHz • PDN_PLL = 0 and PLL properly configured to generate 24.576 MHz given reference input frequency on XTI/MCLK pin • Only MCLK_INT on CLKOUT is supported on CLKOUT pin • CLKOUT outputs (/2, /3, /4, /8 divide) optionally
		1	• Nominal MCLK_INT frequency = 22.5792MHz • PDN_PLL = 0 and PLL properly configured to generate 22.5792 MHz given reference input frequency on XTI/MCLK pin • Only MCLK_INT on CLKOUT is supported on CLKOUT pin • CLKOUT outputs (/2, /3, /4, /8 divide) optionally

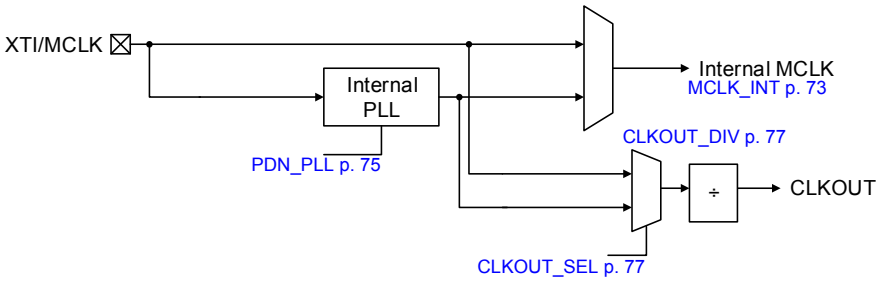


Figure 4-13. MCLK Source Switching

A source to MCLK_INT, either the XTAL (or external MCLK), the PLL, or the RCO, must be provided as long as the CS4399 is operating; otherwise, the CS4399 enters a nonresponsive state, and I²C SDA signal can be held low. The only way to recover from this nonresponsive state is either through a reset or a POR event. Switching MCLK sources during DAC operation causes audible artifacts, but does not put the device in an unrecoverable state. In an MCLK source-switching event, the intended clock source must be present and ready before switching occurs.

After POR or reset event, RCO is selected as default source of MCLK_INT.

4.5.1.1 Internal RC Oscillator

As described in Section 4.5.1, the CS4399 includes an internal RC oscillator that can be used as a clock source for peripheral circuit such as control port or charge pump.

4.6 Clock Output and Fractional-N PLL

The CS4399 clock output can be used as a master clock for other data-conversion or signal-processing components, which requires synchronous timing to the CS4399.

The CLKOUT output is enabled by clearing PDN_CLKOUT.

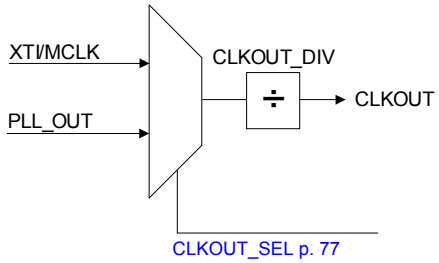


Figure 4-14. CLKOUT Source Selection

Once enabled, CLKOUT is generated either from the internal crystal oscillator output (when used) or from the integrated fractional-N PLL; it can be selected by CLKOUT_SEL. CLKOUT_DIV can be used to set /2, /3, /4, or /8 to divide the selected clock source to targeted frequency.

4.6.1 Fractional-N PLL

The CS4399 has an integrated fractional-N PLL to support the clocking requirements of various applications. This PLL can be enabled or disabled by clearing or setting PDN_PLL bit. The input reference clock for the PLL is signal on XTI/MCLK pin (crystal-generated or external-feed).

4.6.2 Fractional-N PLL Internal Interface

Fig. 4-15 shows how PLL operation can be configured.

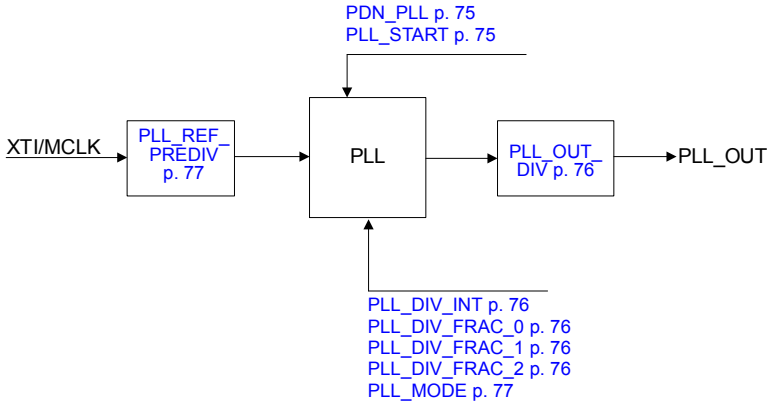


Figure 4-15. Fractional-N PLL

Use Eq. 4-1 to calculate the PLL output frequency.

$$PLL\_OUT = \frac{PLL\_REF}{PLL\_REF\_PREDIV} \times \frac{PLL\_DIV\_INT + PLL\_DIV\_FRAC}{\frac{500}{512} \text{ or } 1, \text{ selected by PLL\_Mode}} \times \frac{1}{PLL\_OUT\_DIV}$$

Equation 4-1. PLL Output Frequency Equation

PLL_REF source must be in range below:

PLL_REF Source	PLL_REF_PREDIV Input	
	Minimum	Maximum
MCLK/XIN pin	9.6 MHz	26 MHz

Table 4-4 lists common settings with XTAL input as PLL reference.

Table 4-4. PLL Configuration for Typical Use Case (XTAL as the PLL Reference)

XTAL (MHz)	PLL_REF_PREDIV (Divide-by Value)	PLL_REF_PREDIV (Setting)	PLL_ DIV_INT	PLL_DIV_FRAC	PLL_OUT_DIV	PLL_ MODE	PLL OUT (MHz)	PLL_CAL_ RATIO
22.5792	8	0x3	0x44	0x06 F700	0x08	0	24.576	139
24.576	8	0x3	0x49	0x80 0000	0x0A	1	22.5792	118

Table 4-5 lists common settings with MCLK input as PLL reference.

Table 4-5. PLL Configuration for Typical Use Case (XIN/MCLK as the PLL Reference)

XIN/MCLK (MHz)	PLL_REF_PREDIV (Divide-by Value)	PLL_REF_PREDIV (Setting)	PLL_DIV_INT	PLL_DIV_FRAC	PLL_OUT_DIV	PLL_ MODE	PLL_OUT (MHz)	PLL_CAL_ RATIO
11.2896	4	0x2	0x40	0x00 0000	0x08	1	22.5792	128
	4	0x2	0x44	0x06 F700	0x08	0	24.576	139
22.5792	8	0x3	0x44	0x06 F700	0x08	0	24.576	139
12.000	4	0x2	0x49	0x80 0000	0x0A	0	22.5792	120
	4	0x2	0x40	0x00 0000	0x08	0	24.576	131
24.000	8	0x3	0x49	0x80 0000	0x0A	0	22.5792	120
	8	0x3	0x40	0x00 0000	0x08	0	24.576	131
12.288	4	0x2	0x49	0x80 0000	0x0A	1	22.5792	118
	4	0x2	0x40	0x00 0000	0x08	1	24.576	128
24.576	8	0x3	0x49	0x80 0000	0x0A	1	22.5792	118
9.600	4	0x2	0x49	0x80 0000	0x08	0	22.5792	151
	4	0x2	0x50	0x00 0000	0x08	0	24.576	164
19.200	8	0x3	0x49	0x80 0000	0x08	0	22.5792	151
	8	0x3	0x50	0x00 0000	0x08	0	24.576	164
13.000	4	0x2	0x45	0x79 7680	0x0A	1	22.5792	111
	4	0x2	0x3C	0x7E A940	0x08	1	24.576	121
26.000	8	0x3	0x45	0x79 7680	0x0A	1	22.5792	111
	8	0x3	0x3C	0x7E A940	0x08	1	24.576	121

Note that in Table 4-4 and Table 4-5:

- The PLL_OUT_DIV value must be even.
- PLL_OUT frequencies are at 22.5792 or 24.576 MHz. CLKOUT frequencies can be obtained by configuring the CLKOUT_DIV value:

PLL_OUT	CLKOUT_DIV (2)	CLKOUT_DIV (3)	CLKOUT_DIV (4)	CLKOUT_DIV (8)
22.5792 MHz	11.2896 MHz	7.5264 MHz	5.6448 MHz	2.8224 MHz
24.576 MHz	12.288 MHz	8.192 MHz	6.144 MHz	4.096 MHz

- PLL_ERROR_INT constantly monitors the PLL error status after PLL_START is set, assuming the PLL reference input is stable and accurate.

4.6.2.1 Powering Up the PLLs

To power up the PLL, follow the following default sequence:

1. Enable the PLL by clearing PDN_PLL.
2. Configure PLL_REF_PREDIV.
3. Configure PLL_OUT_DIV.
4. Configure the three fractional factor registers, PLL_DIV_FRAC.
5. Set the integer factor, PLL_DIV_INT, to the desired value.
6. Configure PLL_MODE and PLL_CAL_RATIO.

7. After properly unmasked (clearing PLL_READY_INT_MASK and PLL_ERROR_INT_MASK), PLL_READY_INT, and PLL_ERROR_INT are used to monitor if PLL has been successfully started.
8. Turn on the PLL by setting PLL_START.

4.6.2.2 Powering Down the PLL

1. Clear PLL_START to stop the PLL operation.
2. For further power saving, set PDN_PLL to disable the PLL block.

4.7 Filtering Options

To accommodate the increasingly complex requirements of digital audio systems, the CS4399 incorporates selectable filters in different playback modes. Note that when switching between filter options, the CS4399 output needs to be powered down in accordance with the sequence specified in Section 5.7.1 first before applying any filter changes. After the filter is changed, for audio playback, the CS4399 output must be powered up.

For PCM/TDM mode, the following interpolation filtering options can be selected:

- Fast roll-off and slow roll-off interpolation filter options.
- In each option above, both low-latency and normal phase-compensation filtering options can be used.
- Nonoversampling (NOS) mode is provided, which minimizes the internal digital processing. Once NOS mode is set, the settings on the above two options are ignored.

The combination of the options results in five different filter combinations. The specifications for each filter can be found in Table 3-5, and response plots can be found in Section 9. These filters have been designed to accommodate a variety of musical tastes and styles. The PCM filter option register (see Section 7.5.2) is used to select filter options.

When in octuple-speed mode, the filter options above are not available and the internal digital processing is minimized. See the specification in Table 3-5 for filter characteristics.

The DSD processor mode uses a decimation-free DSD processing technique that allows for features such as matched PCM level output, DSD volume control, and 50-kHz on-chip filter.

4.8 Audio Serial Port (ASP)

The independent, highly configurable ASPs and auxiliary serial ports (XSPs) communicate audio data from other system devices, such as applications processors. Both ports can be configured to support common audio interfaces, TDM/I^2S and left-justified (LJ).

ASP supports both PCM and DoP stream playback. XSP can only support DoP stream playback. For DAC playback, only one port needs to be enabled. Both ports are enabled only in specific application, such as PCM notification mixing with DSD/DoP content. Details regarding this application setup can be found in Section 4.11.

In this section, the reference to both ports is generalized as “xSP” to explain the common settings between the two ports.

4.8.1 Master and Slave Timing

Each serial port can operate as either the master of timing or as a slave to another device’s timing. If xSP_M/$\overline{S}$ is set, the serial port acts as a clock master. If xSP_M/$\overline{S}$ is cleared, the serial port acts as a clock slave.

- In Master Mode, xSP_SCLK and xSP_LRCK are outputs derived from the internal MCLK.
- In Slave Mode, xSP_SCLK and xSP_LRCK are inputs. Although the CS4399 does not generate the interface timings in Slave Mode, the expected LRCK and SCLK format must be programmed in the same way as in Master Mode (see Table 3-15).
- In both modes, the serial port sample rate register (xSP_SPRATE) must be set per audio content before enabling the serial port.
- When using ASP for PCM playback, the audio serial port sample bit size register (ASP_SPSIZE) must be set per audio content before enabling the ASP.

- When using XSP or ASP for DoP playback, the serial port sample bit size register (XSP_SPSIZE or ASP_SPSIZE) must be set per audio content before enabling the XSP or ASP. Note that the XSP_SPSIZE or ASP_SPSIZE must reflect the length of both DSD marker bits together with audio bits.

4.8.2 Power-Up, Power-Down, and Tristate

The xSP has separate power-down and tristate controls (PDN_xSP and xSP_3ST) for input data paths, which minimizes power consumption if the input port is not used. xSP master/slave operation is controlled only by the xSP_M/$\overline{S}$ setting, irrespective of the PDN_xSP and xSP_3ST settings.

- PDN_xSP. If a serial port's SDIN functionality is not required, xSP can be powered down by setting PDN_xSP, which powers down the input data path and clocks of the serial port.
- xSP_3ST. In Master Mode, setting xSP_3ST tri-states the SCLK and LRCK clocks. Before setting an xSP_3ST bit, the associated serial port must be powered down and must not be powered up until the xSP_3ST bit is cleared. In Slave Mode, xSP_3ST does not affect the functionality of SCLK and LRCK clocks, given both pins are input pins.

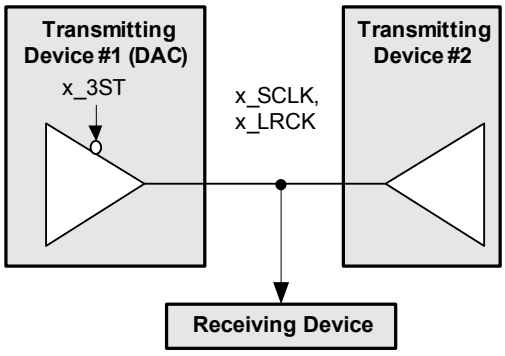
4.8.3 I/O

The ASP port is associated with SDIN1, SCLK1, and LRCK1. The XSP port is associated with SDIN2, SCLK2, and LRCK2, which are shared with DSD interface:

- SCLKx—Serial data shift clock
- LRCKx—Toggles at external sample rate (Fs_{ext}). LRCK (left/right, I²S) identifies each channel's (left or right) location in the data word when I²S format is used. LRCK identifies the start of each serialized data word. FSYNC (frame sync clock, TDM) identifies the start of each TDM frame.
- SDINx—Serial data input

4.8.4 High-Impedance Mode

Serial ports can be placed on a clock bus that allows multiple masters without the need for external buffers. xSP_3ST bits place the internal buffers for the respective serial-port interface signals in a high-impedance state, allowing another device to transmit clocks without bus contention. When the CS4399 serial port is a timing slave, its SCLK and LRCK I/Os are always inputs and are thus unaffected by the xSP_3ST control. Fig. 4-16 shows the busing for CS4399 master timing serial-port use case.



Note: x = XSP or ASP

Figure 4-16. Serial Port Busing when Master Timed

4.8.5 Clock Generation and Control

The CS4399 has a flexible serial port clock generation subsystem that allows independent clocking of the two serial ports. When operating as a master port, the serial port provides a bit clock (xSP_SCLK) and a left-right/frame sync signal (xSP_LRCK/FSYNC).

Fig. 4-17 and Fig. 4-18 show the serial port clocking architecture.

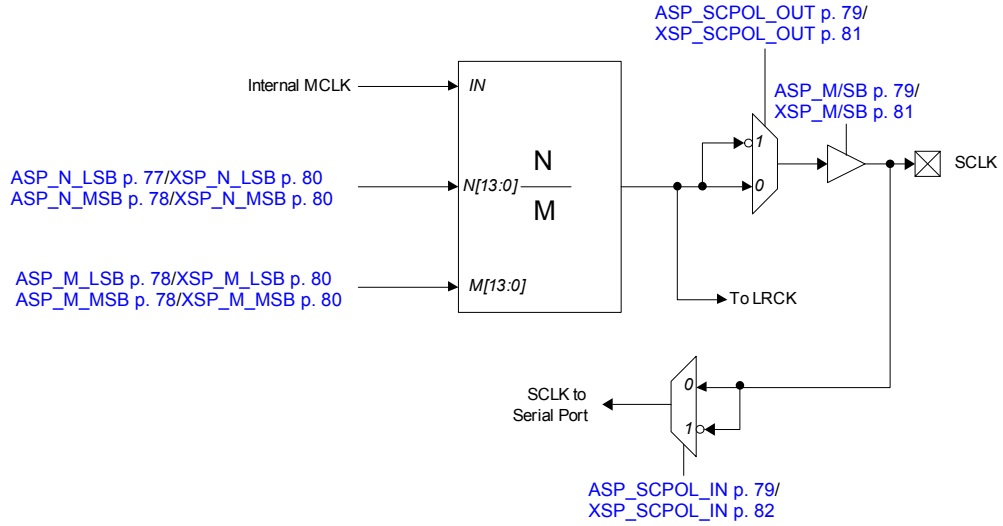


Figure 4-17. xSP SCLK and MCLK Architecture

As shown in Fig. 4-17, the master-mode SCLK output for each serial port is derived from the internal MCLK. The SCLK output can be configured to various frequencies to accommodate many sample rates, sample sizes, and channel counts. The SCLK is output of a fractional divide from the internal MCLK input, where N is the numerator and M is the denominator.

Note: Depending on the chosen fractional divide configuration, the SCLK duty cycle can vary by one MCLK period.

Input and output SCLK polarity controls (xSP_SCPOL_IN and xSP_SCPOL_OUT) are also available. As shown in Fig. 4-17, if Master Mode is used, both polarity controls affect the SCLK used by the serial port module. For example, both polarity controls must be set to invert (xSP_SCPOL_IN = xSP_SCPOL_OUT = 1) to invert the SCLK output and output data on the falling edge. In typical use cases, the values of xSP_SCPOL_IN equals xSP_SCPOL_OUT in each serial port. See Fig. 4-20 for example waveforms showing the various settings of the SCLK polarity controls.

Likewise, input and output LRCK polarity controls (xSP_LCPOL_IN and xSP_LCPOL_OUT) are available. In Master Mode, both LRCK polarity controls affect the LRCK used by the serial-port module as shown in Fig. 4-18. In typical-use cases, the value of xSP_LCPOL_IN equals xSP_LCPOL_OUT in each serial port.

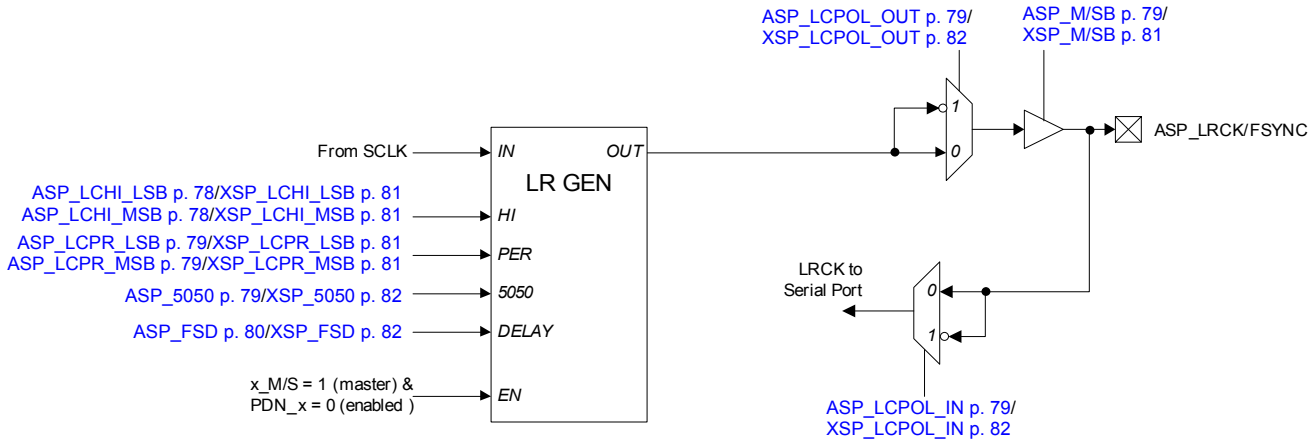


Figure 4-18. xSP LRCK Architecture

As shown in Fig. 4-19, xSP_LCPR determines the LRCK/FSYNC period, in units of SCLK periods. The LRCK period effectively sets the length of the frame and the number of SCLK periods per Fs. Frame length may be programmed in single SCLK period multiples from a minimum of 16 SCLK:Fs up to 1536 SCLK:Fs.

The LRCK-high width (xSP_LCHI) controls the number of SCLK periods for which the LRCK signal is held high during each frame. Like the LRCK period, the LRCK-high width is programmable in single SCLK periods, from a minimum of one period to a maximum of the LRCK period minus one (and an absolute maximum of 768 SCLK periods). That is, LRCK-high width must be less than the LRCK period.

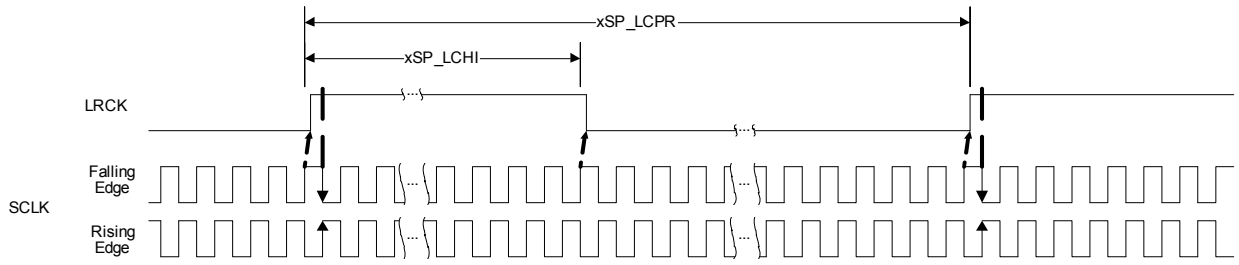


Figure 4-19. xSP LRCK Period, High Width

As shown in Fig. 4-20, if Serial Port 50/50 Mode is enabled (xSP_5050 = 1), the LRCK high duration must be programmed to the LRCK period divided by two (rounded down to the nearest integer when the LRCK period is odd). When the serial port is in 50/50 Mode, setting the LRCK high duration to a value other than half of the period results in erroneous operation.

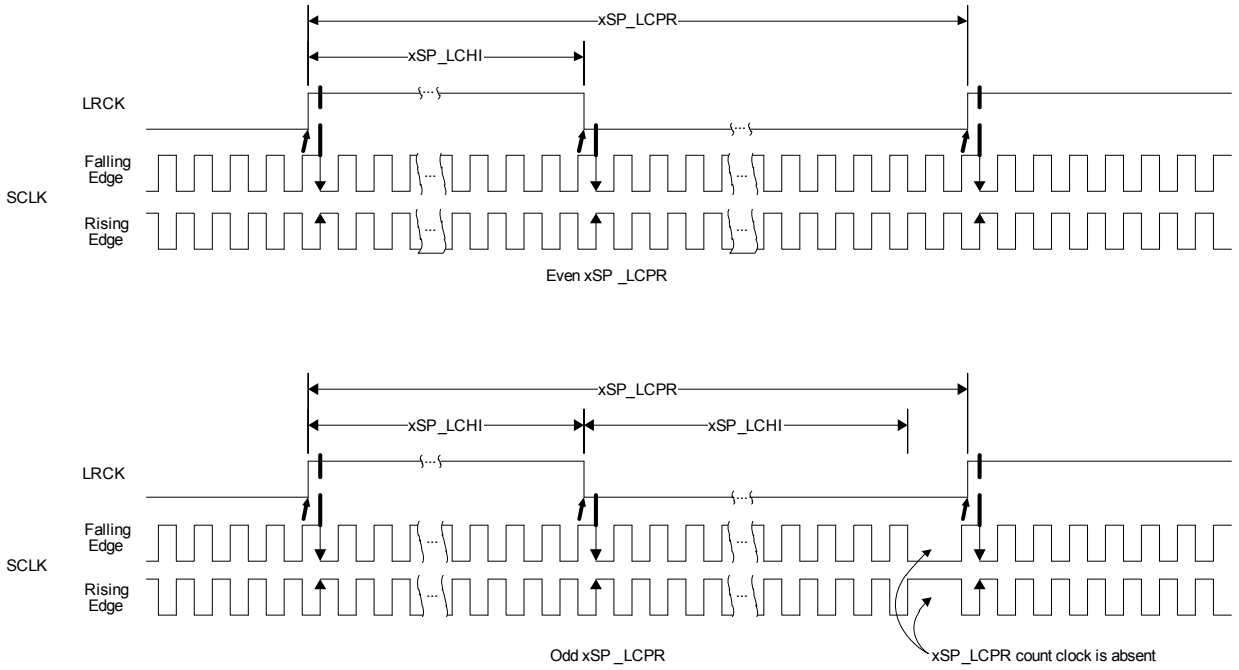


Figure 4-20. xSP_LRCK Period, High Width, 50/50 Mode

Fig. 4-21 shows how LRCK frame start delay (xSP_FSD) controls the number of SCLK periods delay from the LRCK synchronization edge to the start of frame data.

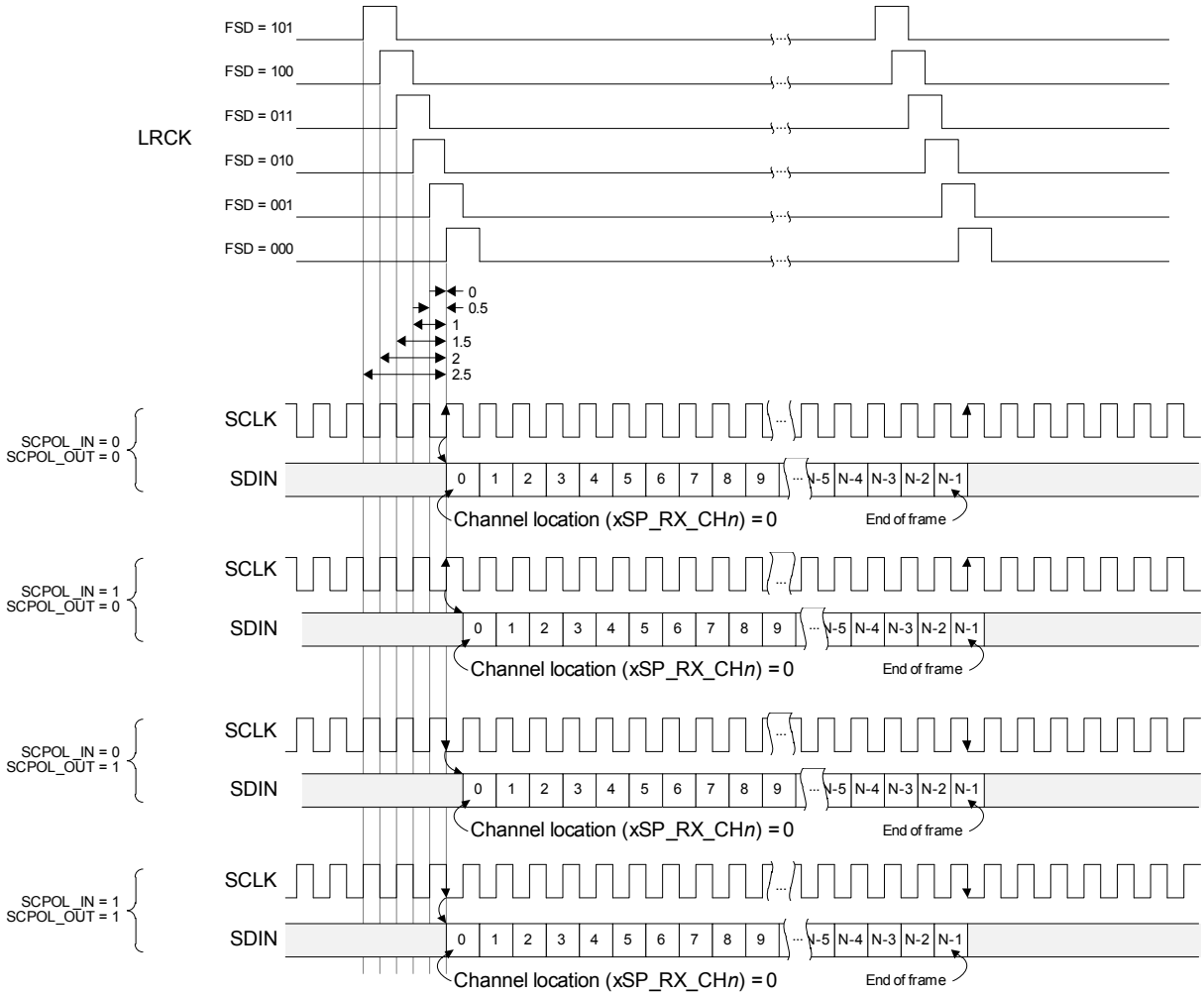


Figure 4-21. LRCK FSD and SCLK Polarity Example Diagram

Table 4-6. Serial Port Clock Generation—Supported Configurations for 32 bits and 2 Channels

Frequency (MHz)	LRCK/FSYNC Rate (kHz)	SCLKs per LRCK Frame		xSP_N[15:0]	xSP_M[15:0]
		xSP_LCPR + 1	xSP_LCPR[10:0]		
22.5792	32.000	64	63	40	441
	44.100	64	63	1	8
	48.000	64	63	20	147
	88.200	64	63	1	4
	96.000	64	63	40	147
	176.400	64	63	1	2
	192.000	64	63	80	147
	352.800	64	63	1	1
24.576	32.000	64	63	1	12
	44.100	64	63	147	1280
	48.000	64	63	1	8
	88.200	64	63	147	640
	96.000	64	63	1	4
	176.400	64	63	147	320
	192.000	64	63	1	2
	352.800	64	63	147	160
	384.000	64	63	1	1

Table 4-7. Serial Port Clock Generation—Supported Configurations for 32-bits and 4 Channels

Frequency (MHz)	LRCK/FSYNC Rate (kHz)	SCLKs per LRCK Frame		xSP_N[15:0]	xSP_M[15:0]
		xSP_LCPR + 1	xSP_LCPR[10:0]		
22.5792	32.000	128	127	80	441
	44.100	128	127	1	4
	48.000	128	127	40	147
	88.200	128	127	1	2
	96.000	128	127	80	147
	176.400	128	127	1	1
24.576	32.000	128	127	1	6
	44.100	128	127	147	640
	48.000	128	127	1	4
	88.200	128	127	147	320
	96.000	128	127	1	2
	176.400	128	127	147	160
	192.000	128	127	1	1

4.8.6 Channel Location and Size

Each serial-port channel has a programmable location offset (xSP_RX_CHn). Channel location is programmable in single SCLK period resolution. When set to the minimum location offset, the channel transmits or receives on the first SCLK period of a new frame.

Channel size is programmable in byte resolution from 8 to 32 bits using xSP_RX_CHn_RES. Channel size and location must not be programmed such that channel data extends beyond the frame boundary. Size and location must not be programmed such that data from a given SCLK period is assigned to more than one channel. The example in Fig. 4-22 shows channel location and size.

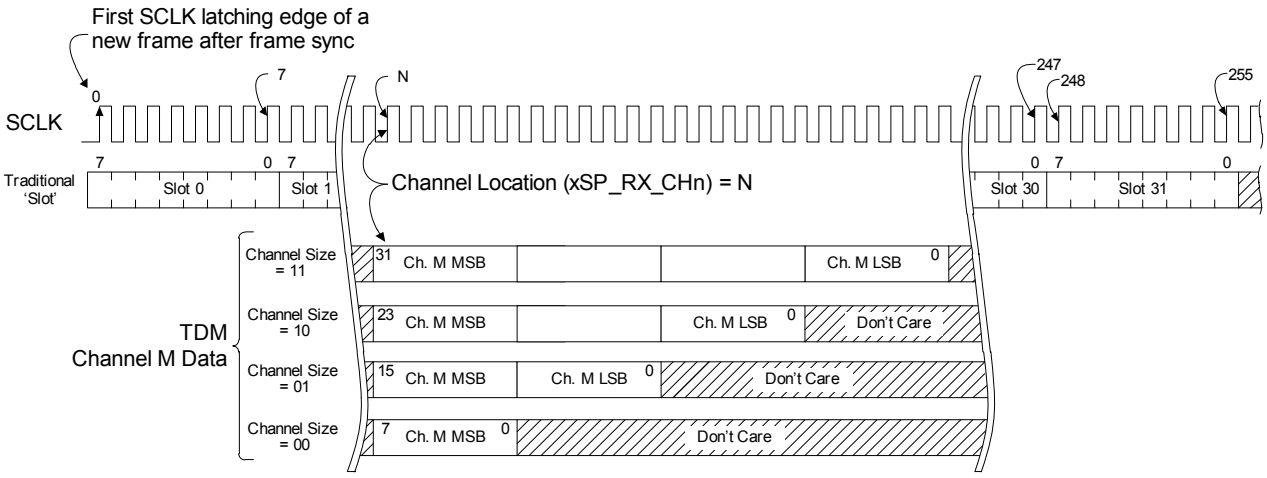
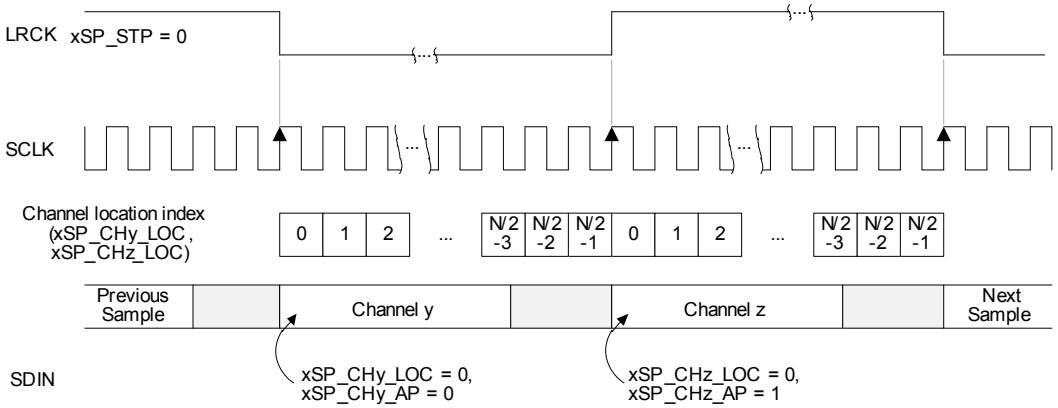


Figure 4-22. Example Channel Location and Size

4.8.7 Frame Start Phase

The serial port can start a frame when xSP_LRCK/FSYNC is high or low, depending on xSP_STP. In typical TDM use cases, a frame starts when FSYNC is high (xSP_STP = 1).

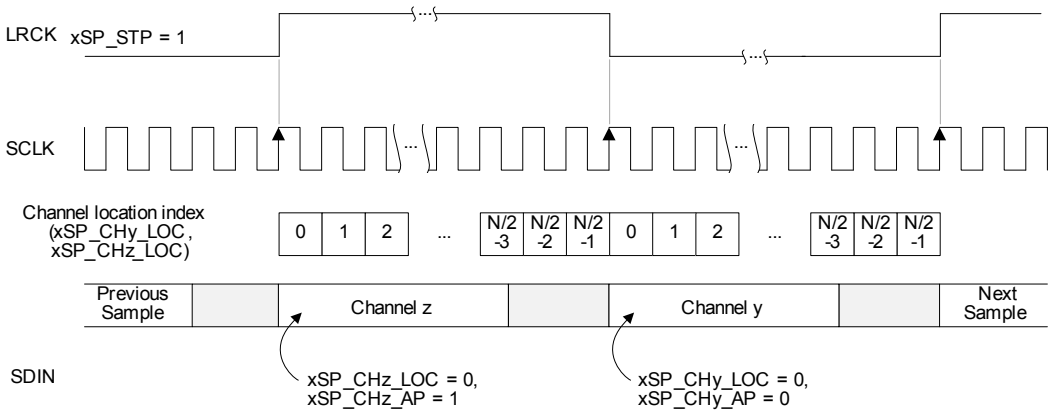
- If xSP_STP = 0, the frame begins when LRCK/FSYNC transitions from high to low. See Fig. 4-23 for an example in 50/50 mode. The TDM Mode behaves similarly.



Note: This diagram assumes xSP _FSD = 0.

Figure 4-23. Example 50/50 Mode (ASP_STP = 0)

- If xSP_STP = 1, the frame begins when LRCK/FSYNC transitions from low to high. See Fig. 4-24 for an example in 50/50 mode. TDM mode is similar.



Note: This diagram assumes xSP_FSD = 0.

Figure 4-24. Example 50/50 Mode (ASP_STP = 1)

4.8.8 50/50 Mode

In typical two-channel I²S operation (50/50 Mode, xSP_5050 = 1), the LRCK duty cycle is 50%, and each channel is transferred during one of the two LRCK phases. In this mode, each serial port channel can be independently programmed to output when LRCK/FSYNC is high or low; this is called the *channel-active phase*.

If the active-phase control bit (xSP_RX_CHn_AP) is set, the respective channel is output when LRCK/FSYNC is high. If xSP_RX_CHn_AP is cleared, the respective channel is output if LRCK/FSYNC is low. Examples of each setting of xSP_RX_CHn_AP are shown in Fig. 4-23 and Fig. 4-24.

In 50/50 Mode, the channel location (see Section 4.8.6) is calculated within the channel-active phase. If there are N bits in a frame, the location of the last bit of each active phase is equal to (N/2) – 1.

Note: If xSP_5050 is set, xSP_LCHI must be programmed to half of xSP_LCPR for a 50% duty cycle. Also, only two channels can be enabled for the corresponding serial port.

4.8.9 Serial Port Status

Each serial port has five status bits. Each bit is sticky and must be read to be cleared. The status bits have associated mask bits to mask setting the INT pin when the status bit sets. A brief description of each status bit is shown in Table 4-8.

Table 4-8. Serial Port Status

Name	Description	Register Reference
Request Overload	Set when too many input buffers request processing at the same time. If all channel size and location registers are properly configured to non-overlapping values, this error status must never set.	ASP_OVFL_INT p. 90 XSP_OVFL_INT p. 91
LRCK Early	Set when the number of SCLK periods per LRCK phase (high or low) is less than the expected count as determined by xSP_LCPR and xSP_LCHI. **Note:** The Rx LRCK early interrupt status is set during the first receive LRCK early event. Subsequent receive LRCK early events are not indicated until after valid LRCK transitions are detected.	ASP_EARLY_INT p. 90 XSP_EARLY_INT p. 91
LRCK Late	Set when the number of SCLK periods per LRCK phase (high or low) is greater than the expected count as determined by xSP_LCPR and xSP_LCHI.	ASP_LATE_INT p. 90 XSP_LATE_INT p. 91
LRCK Error	Logical OR of LRCK early and LRCK late.	ASP_ERROR_INT p. 90 XSP_ERROR_INT p. 91
No LRCK	Set when the number of SCLK periods counted exceeds twice the value of LRCK period (xSP_LCPR) without an LRCK edge. The Tx No LRCK interrupt status is set during the first instance of a no transmit LRCK condition. Subsequent no transmit LRCK conditions are not indicated until after valid LRCK transitions are detected.	ASP_NOLRCK_INT p. 91 XSP_NOLRCK_INT p. 91

4.8.10 Serial Port Clock Pin Status

There are various control bits available that affect the output state of the serial port clock and data pins. Table 4-9 summarizes the possible states depending on these bit settings.

Table 4-9. xSP_SCLK and xSP_LRCK/FSYNC Pin States

xSP_3ST	xSP_M/$\overline{S}$	PDN_xSP	xSP_SCLK Pin State	xSP_LRCK/FSYNC Pin State
1	x	x	Hi-Z with weak pull-down	Hi-Z with weak pull-down
0	0	x	Hi-Z with weak pull-down	Hi-Z with weak pull-down
0	1	0	Active	Active
0	1	1	Inactive	Inactive [1]

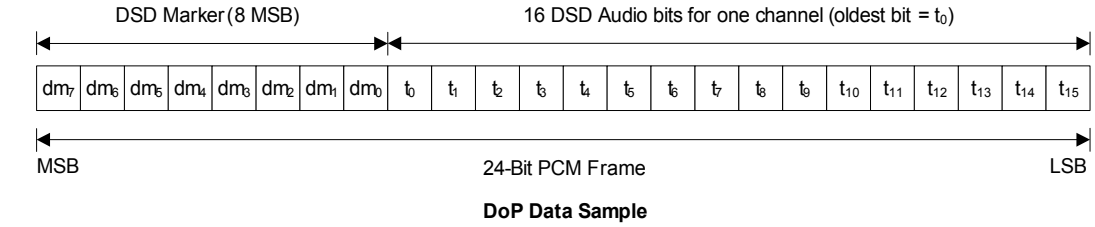
1. If xSP_LCPOL_OUT is set, xSP_LRCK/FSYNC inactive output is high. If xSP_LCPOL_OUT is cleared, xSP_LRCK/FSYNC inactive output is low.

4.8.11 DoP (DSD over PCM) Mode

DoP is a protocol for packetizing DSD data into a PCM frame for transmission over an existing I²S interface. The ASP or XSP can accept DSD data in DoP format.

To use the DoP interface in Slave Mode, if MCLK_INT = 22.5792 MHz, the DoP interface clocks are required to be synchronous to MCLK_INT.

Each sample is 24 bits, as shown in Fig. 4-25, where the 8 most significant bits are used for the DSD marker and alternate with each sample between 0x05/0xFA. Each channel within a sample contains the same marker. The remaining 16 least significant bits are then used for the DSD data, with the first or oldest bit in Slot t0. It is required that markers are provided continuously when the DoP interface is enabled, or a random sustained DC voltage asserts on loads from CS4399 outputs.



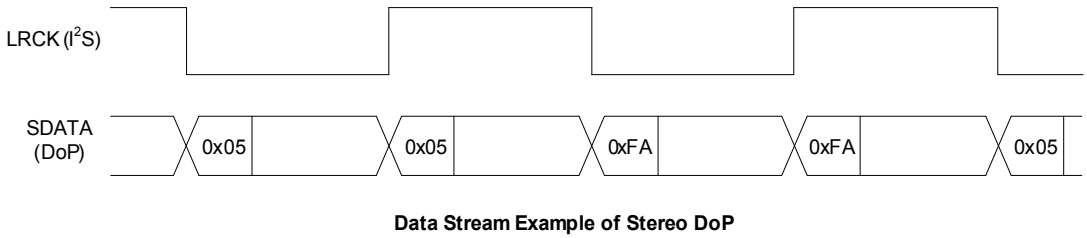


Figure 4-25. DoP Data Sample and Stereo Stream Example

Each PCM frame is assigned to a specific channel (left or right), and when used for DSD streaming, each PCM frame contains only DSD data corresponding to its assigned channel. The CS4399 unpacks the received DoP data and reforms it into a DSD stream to feed the internal DSD data paths.

It includes the following features:

- 24 bits per PCM data sample
- I²S format is supported
- DoP data is unpacked internally for DSD playback
- Clock Master and Slave Mode
- Up to 128 • Fs DSD stream
  - — Accepts a 64•Fs DSD stream with LRCK@176.4 kHz
  - — Accepts a 128•Fs DSD stream with LRCK@352.8 kHz

To enable DoP interface on the ASP to take in DSD source:

1. Configure the ASP per clocking/format required by DoP content.
2. Configure DSD_SPEED per DoP content.
3. Set DSD_PRC_SRC = 01 and DSD_EN = 1.

4.9 DSD Interface

The DSD interface is enabled or disabled by PDN_DSDIF bit. When cleared, the DSD data interface is enabled. When using this interface, the DSD interface clock can be mastered by the CS4399 (DSD_M/SB=1). If set to Master Mode, DSDCLK toggles if both PDN_DSDIF and XSP_3ST bits are cleared, and DSD_EN is set.

If the DSD interface clock is slaved (DSD_M/SB=0), when MCLK_INT is set as 22.5792 MHz, DSDCLK is required to be synchronous to MCLK_INT. The DSDCLK can be derived by either:

- Exporting 1/4 or 1/8 the frequency of the CS4399 crystal to CLKOUT, or
- Sourcing MCLK_INT and DSDCLK from the same external clock source

The DSD_EN bit, when set, is used to configure the device for processing DSD sources. DSD_PRC_SRC configures the DSD interface used for feeding into the DSD processor. DSD_SPEED specifies if a 64•Fs or 128•Fs DSD stream is provided. If PDN_DSDIF = 0 and DSD_M/SB = 1, DSD_SPEED determines the DSDCLK clock frequency generated. When configuring the DSD interface, follow these steps:

1. Configure the DSD_M/SB, DSD_SPEED, DSD_PRC_SRC, and XSP_3ST.
2. Release PDN_DSDIF.
3. Enable DSD_EN.

The DSD_PM_EN bit selects phase modulation (data plus data inverted) as the style of data input. In this mode, the DSD_PM_SEL bit selects whether a 128•Fs or 64•Fs clock is used for phase-modulated 64•Fs data (see Fig. 4-26). Use of phase modulation mode may not directly affect the performance of the CS4399, but may lower the sensitivity of other board-level components to the DSD data signals. Note that phase modulation mode is supported only for DSD 64•Fs data rate.

The CS4399 can detect overmodulation errors in the DSD data that do not comply to the SACD specification. Setting INV_DSD_DET enables detection of overmodulation errors. This condition is reported through the DSD_INVAL_A_INT and DSD_INVAL_B_INT status bits. Overmodulated DSD data is converted as received without intervention, but performance at these levels cannot be guaranteed. Setting STA_DSD_DET allows the CS4399 to mute a DSD stream that is stuck at 1 or 0. This condition is reported through the DSD_STUCK_INT status bit. See Section 7.6.4 for descriptions of the DSD error reporting bits.

More information for these register bits can be found in Section 7.

The DSD input structure and analog outputs are designed to handle a nominal 0 dB-SACD (50% modulation index) at full-rated performance. When 0 dB-SACD and 0 dBFS PCM need to be level matched, DSD_ZERODB must be set. In this mode, signals of +3-dB SACD may be applied for brief periods of time; however, performance at these levels is not guaranteed. If sustained levels approaching +3-dB SACD levels are required, DSD_ZERODB must be cleared, which matches a +3-dB SACD output level.

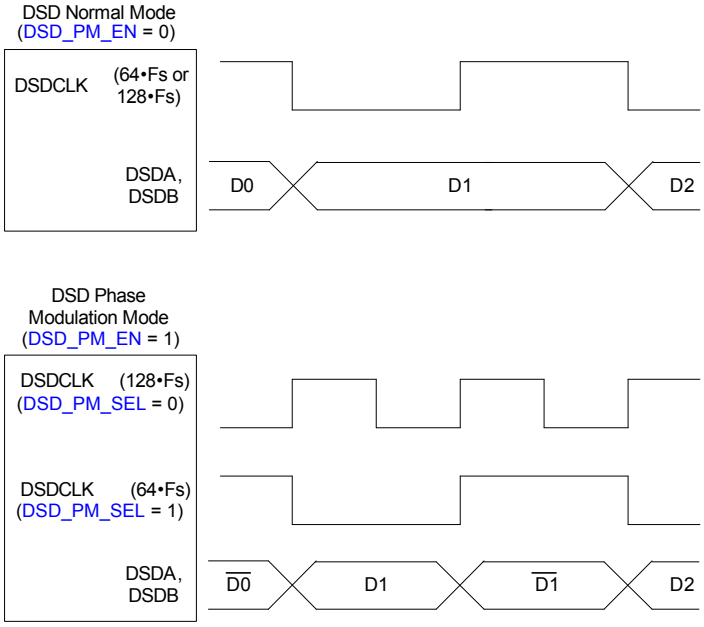


Figure 4-26. DSD Phase Modulation Mode Diagram

4.10 DSD and PCM Mixing

For mobile application, the CS4399 provides a feature for mixing in PCM notification during DSD playback, with the setup in Table 4-10.

Table 4-10. Mixing Configurations Supported by the CS4399

PCM Input Configuration			DSD Input Configuration		
I²S or TDM on ASP	44.1 kHz	Master	DSD on DSD IF	2.8224 or 5.6448 MHz on DSDCLK	Master
		Slave [1]			Slave [1]
		Master	DoP on XSP	176.4 or 352.8 kHz	Master
		Slave [1]			Slave [1]

1. The ASP/XSP subclocks and DSDCLK are required to be synchronous.

It is assumed that the DSD path has been properly configured for DSD playback, and DSD_AMUTE function is disabled.

During normal DSD playback, the ASP can be shut down. At the PCM notification event, the ASP must be properly configured to receive PCM samples at 44.1 kHz. After the ASP subclocks are running, set MIX_PCM_PREP to indicate to the CS4399 that the PCM mixing event is imminent. After 1.6 ms, MIX_PCM_DSD can be safely set to initiate the mixing process. After the PCM notification mixing is complete, clear both MIX_PCM_DSD and MIX_PCM_PREP at the same time. If desired, the ASP can be shut down to save power.

When mixing, use both PCM and DSD volume controls to attenuate the signal content on both paths (e.g., at least –6-dB attenuation on each) to avoid clipping on the mixing product. Use PCM_VOLUMEx to adjust the PCM path and DSD_ VOLUMEx to adjust the DSD path. All the signal path settings apply to both path's individual settings.

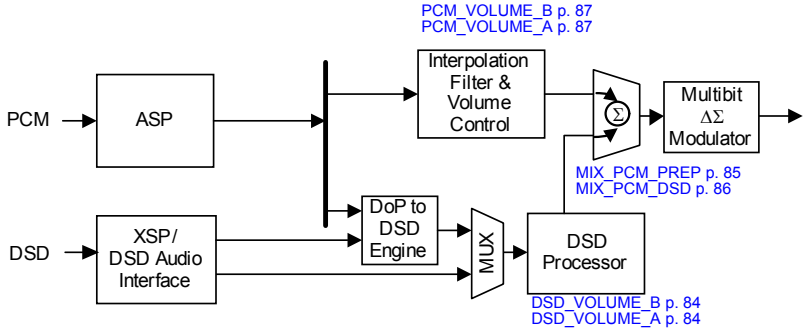


Figure 4-27. PCM and DSD Mixing Signal Flow

4.11 Standard Interrupts

The interrupt output pin, $\overline{\text{INT}}$, is used to signal the occurrence of events within the device's interrupt status registers. Events can be masked individually by setting corresponding bits in the interrupt mask registers. Table 4-11 lists interrupt status and mask registers. The configuration of mask bits determines which events cause the immediate assertion of $\overline{\text{INT}}$:

- When an unmasked interrupt status event is detected, the status bit is set, and $\overline{\text{INT}}$ is asserted.
- When a masked interrupt status event is detected, the interrupt status bit is set, but $\overline{\text{INT}}$ is not affected.

Once $\overline{\text{INT}}$ is asserted, it remains asserted until all status bits that are unmasked and set have been read. Interrupt status bits are sticky and read-to-clear. Once set, they remain set until the register is read and the associated interrupt condition is not present. If a condition is still present and the status bit is read, although $\overline{\text{INT}}$ is deasserted, the status bit remains set.

To clear status bits set due to the initiation of a block, all interrupt status bits must be read after the corresponding module is enabled and before normal operation begins. Otherwise, unmasking these previously set status bits causes assertion of $\overline{\text{INT}}$.

Interrupt source bits are set when edge-detect interrupts is detected, and they remain set until the register is read and the condition that caused the bit to assert is no longer present.

Fig. 4-28 shows sticky-bit behavior.

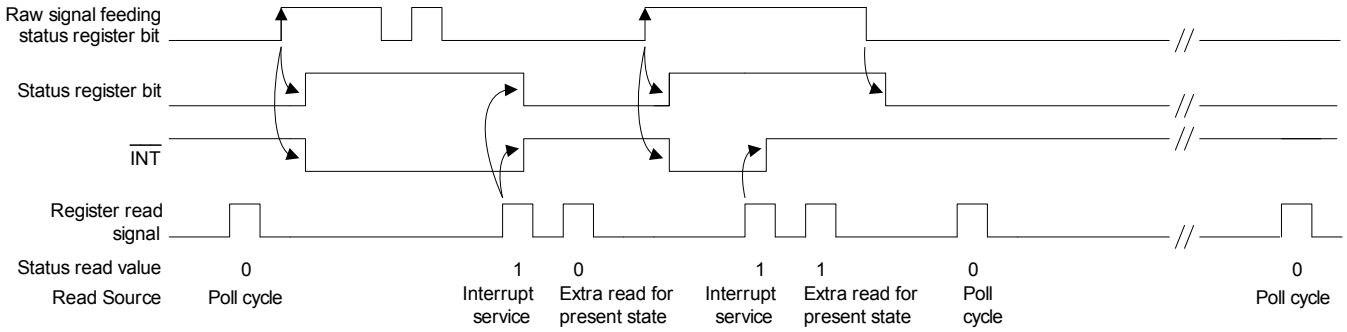


Figure 4-28. Example of Rising-Edge-Sensitive, Sticky, Interrupt-Status-Bit Behavior

Table 4-11. Interrupts Events and Register Bit Fields

Interrupt	Register Bit Field	Interrupt Mask Field
DAC overflow	DAC_OVFL_INT	DAC_OVFL_INT_MASK
HP unplug detect	HPDETECT_UNPLUG_INT	HPDETECT_UNPLUG_INT_MASK
HP plug detect	HPDETECT_PLUG_INT	HPDETECT_PLUG_INT_MASK
XTAL is ready	XTAL_READY_INT	XTAL_READY_INT_MASK
XTAL error detected	XTAL_ERROR_INT	XTAL_ERROR_INT_MASK
ASP overload	ASP_OVLD_INT	ASP_OVLD_INT_MASK
ASP error	ASP_ERR_INT	ASP_ERR_INT_MASK
ASP late	ASP_LATE_INT	ASP_LATE_INT_MASK
ASP early	ASP_EARLY_INT	ASP_EARLY_INT_MASK
ASP no LRCK	ASP_NOLRCK_INT	ASP_NOLRCK_INT_MASK
XSP overload	XSP_OVLD_INT	XSP_OVLD_INT_MASK
XSP error	XSP_ERR_INT	XSP_ERR_INT_MASK
XSP late	XSP_LATE_INT	XSP_LATE_INT_MASK
XSP early	XSP_EARLY_INT	XSP_EARLY_INT_MASK
XSP no LRCK	XSP_NOLRCK_INT	XSP_NOLRCK_INT_MASK
PLL is ready	PLL_READY_INT	PLL_READY_INT_MASK
PLL error detected	PLL_ERROR_INT	PLL_ERROR_INT_MASK
Power down done	PDN_DONE_INT	PDN_DONE_INT_MASK
DSD stuck Error	DSD_STUCK_INT	DSD_STUCK_INT_MASK
DSD channel A invalid error	DSD_INVAL_A_INT	DSD_INVAL_A_INT_MASK
DSD channel B invalid error	DSD_INVAL_B_INT	DSD_INVAL_B_INT_MASK
DSD channel A silence pattern detected	DSD_SILENCE_A_INT	DSD_SILENCE_A_INT_MASK
DSD channel B silence pattern detected	DSD_SILENCE_B_INT	DSD_SILENCE_B_INT_MASK
DSD rate error detected	DSD_RATE_INT	DSD_RATE_INT_MASK
DoP marker detected	DOP_MRK_DET_INT	DOP_MRK_DET_INT_MASK
DoP engine on	DOP_ON_INT	DOP_ON_INT_MASK

4.12 Control Port Operation

The control port is used to access control registers and on-chip memory locations, allowing the device to be configured for desired operational modes and formats. Control port operation may be completely asynchronous with respect to the audio sample rates. However, to avoid potential interference problems, control port pins must remain static if no operation is required.

The control port operates using a I²C interface with the CS4399 acting as a slave device. Device communication must not begin until t_{PUD} (refer to Table 3-17) after power conditions are ready and $\overline{\text{RESET}}$ is released.

4.12.1 I²C Control Port Operation

The I²C control port operates completely asynchronously with the audio sample rates. However, to avoid interference problems, the I²C control-port pins must remain static if no operation is required.

The control-port uses the I²C interface, with the chip acting as a slave device. The I²C control port can operate in the following modes:

- Standard Mode (SM), with a bit rate of up to 100 kbit/s
- Fast Mode (FM), with a bit rate of up to 400 kbit/s
- Fast Mode Plus (FM+), with a bit rate of up to 1 Mbit/s

SDA is a bidirectional data line. Data is clocked into and out of the CS4399 by the SCL clock. Fig. 4-29, Fig. 4-30, and Fig. 4-31 show signal timings for read and write cycles. A Start condition is defined as a falling transition of SDA while SCL is high. A stop condition is defined as a rising transition of SDA while SCL is high. All other transitions of SDA must occur while SCL is low.

To configure the last two bits of I²C address, CS4399 detects the ADR resistor connection type and measures the resistance upon a device power up (POR event) or after a hardware reset event ($\overline{\text{RESET}}$ deasserted). Based on the detected resistance, the I²C address is latched and cannot be changed until the next hardware reset event. The I²C address configuration is not ready until t_{PUD} after the hardware reset event. During this period, the CS4399 does not respond to any user-issued I²C command. After configuration, the IC tristates the ADR pin and becomes high impedance internally to avoid a constant bias current.

When the ADR pin is directly connected to ground, the last two bits of the I²C address are configured as 00 (default). For the other options, use a resistor (with 5% accuracy) as suggested in the Table 4-12.

Table 4-12. I²C Address Configurations

Connection Type	Resistor Value (Ω)	Last Two Bits of I²C Address
Pull-up to VL	0	11
Pull-up to VL	4990	10
Pull-down to GND	4990	01
Pull-down to GND	0	00 (Default)

If the operation is a write, the 3 bytes after the chip address are the memory address pointer (MAP) that select the address of the register to be read or written to next. The byte following the MAP is the control byte. Bit[0] of the control byte, INCR, selects whether autoincrementing is to be used (INCR = 1), allowing successive reads or writes of consecutive registers. Bits[2:1] of the control byte indicate the size of the data for the autoincrement to be acted on. Table 4-13 explains the format for the I²C control byte.

Table 4-13. I²C Control-Byte Format

Bit	Name	Description
7:3	—	Reserved Default: 0
2:1	SIZE	Register access width. Specifies the width of the register access. 00 8-bit (1 byte) 01–11 Reserved
0	INCR	Setting this bit allows the MAP address to autoincrement. The MAP address automatically increments every SIZE + 1 bytes accessed consecutively. 0 Disabled 1 Enabled

Each byte transferred on the I²C bus is separated by an acknowledge (ACK) bit. The CS4399 acknowledges each input byte read from the host, and the host must acknowledge each byte transmitted from the CS4399.

For write operations, the data bytes following the MAP byte are written to the CS4399 register addresses pointed to by the last received MAP address, plus however many autoincrements have occurred. Fig. 4-29 shows a write pattern with autoincrementing.

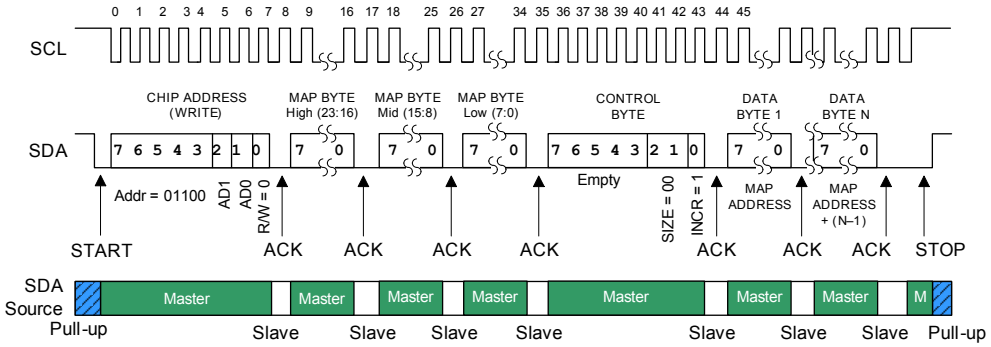


Figure 4-29. Control Port Timing, I²C Writes with Autoincrement (8-bit Data Access)

For read operations, the contents of the register pointed to by the last received MAP address (plus however many autoincrements have occurred if INCR was previously set) are output in the next byte. Fig. 4-30 shows a read pattern following the write pattern in Fig. 4-29. Notice how read addresses are based on the MAP bytes from Fig. 4-29.

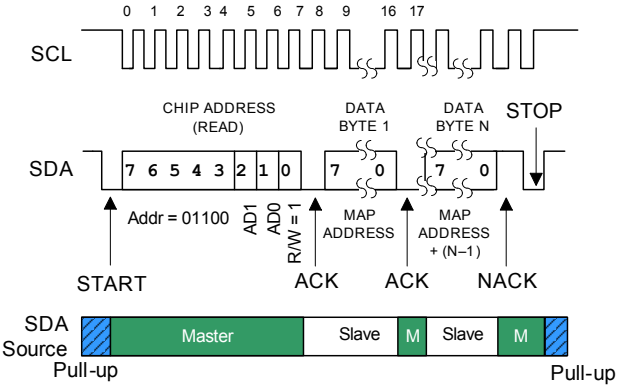


Figure 4-30. Control Port Timing, I²C Reads with Autoincrement (8-Bit Data Access)

To generate a read address not based on the last received MAP address, an aborted write operation can be used as a preamble (see Fig. 4-31). Here, a write operation is aborted (after the ACK for the control byte) by sending a Stop condition.

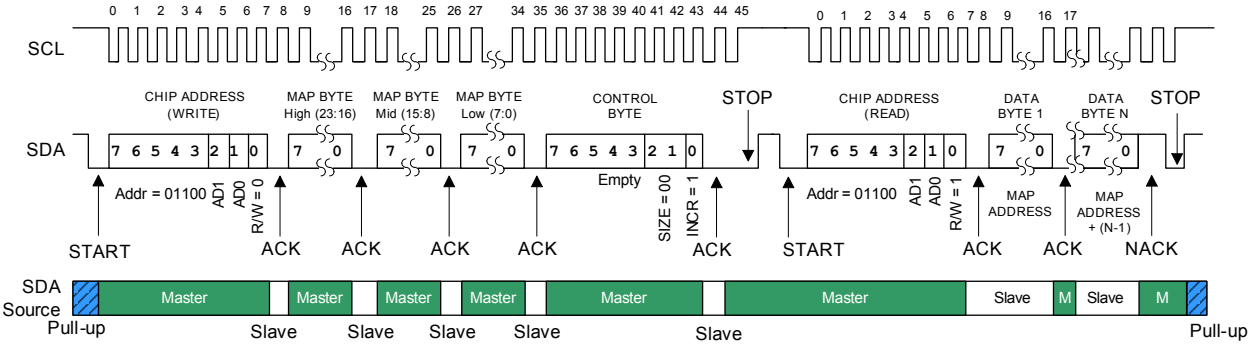


Figure 4-31. Control Port Timing, I²C Reads with Preamble and Autoincrement (8-Bit Data Access)

5 Applications

This section provides recommended application procedures and instruction sequences for standard CS4399 operations.

5.1 PLL Clocking

Data-path logic is in the MCLK_INT domain, where MCLK_INT is expected to be 22.5792 or 24.576 MHz. For clocking scenarios in which the external system MCLK provided to CS4399 is neither 22.5792 nor 24.576 MHz, the PLL must be turned on to provide the desired internal MCLK. At start up, the system uses RCO as the internal MCLK for PLL programming over I²C and switches to the PLL output after it settles. PLL start-up time is a maximum of 1 ms.

5.2 Power Sequencing

Note the following for power-up sequencing on the CS4399:

- VP must be powered up first.
- All other supplies can come up in any order before $\overline{\text{RESET}}$ is released.

Note the following for power-down sequencing on the CS4399:

- After $\overline{\text{RESET}}$ is asserted, VA/VCP/VL/VD can be removed in any order.
- VP must be powered down last.

5.3 Crystal Tuning

The CS4399 uses an external crystal as the source for internal MCLK. Refer to Table 3-11 for the load capacitance that is supported by CS4399. Table 5-1 lists supported crystals that meet the requirements for CS4399 and also shows also shows the XTAL_IBIAS settings for different crystals.

Table 5-1. Example List of Supported Crystals

Manufacturer [1]	Part Number [1]	Frequency (MHz)	Bias Current Strength (µA)	Crystal Setting Register (0x20052)
River Electronics	FCX-06-22.5792J51933	22.5792	12.5	0x04
	FCX-06-24.5760J51930	24.576	7.5	0x06
NDK	NX2016SA 22.5792M EXS00A-CS09116	22.5792	15	0x02
	NX2016SA 24.576M EXS00A-CS09117	24.576		
TXC	8Y22570001	22.5792	12.5	0x04
	8Y24570001	24.576		

1.Contact your local Cirrus Logic representative for a list of supported manufacturers and part numbers.

The crystal setting register (0x20052) must be set appropriately based on the crystal used.

The frequency at which the crystal eventually oscillates can be calculated using the formula below:

$$F_{osc} = 1/(2*\pi*\text{sqrt}[Lm*(C_m\ (C_0+C_L))/(C_m+C_0+C_L)]) ,$$

where

L_m = motional inductance of crystal
C_m = motional capacitance of crystal
C_0 = shunt capacitance
C_L = load capacitance

Trace capacitance and pad capacitance (approximately 0.5 pF) must also be taken into account while calculating the value of the load capacitors. Below are the steps to tune the crystal to the correct frequency:

1. Select load capacitor values that match the load capacitance spec in crystal manufacturer's data sheet.

2. Power up and verify communication with CS4399. If there is no communication, it is possible that the crystal did not start. Check power rails and load capacitance and try again.
3. Clear PDN_CLKOUT in the Power Down Control (0x20000) register. This sets the clock output at MCLK_INT/2 frequency from CLKOUT pin.
4. Measure the frequency and verify that it is within acceptable range of the desired frequency. If yes, continue normal operation. If not, power down the chip, change the load capacitor values and go back to step 2.

Note: These steps need to be performed only once per PCB.

5.4 Alert Mixing Shutdown

To prevent a DSD mute pattern from turning off the DAC while mixing DSD data with PCM data, turn off the auto mute by clearing the DSD_AMUTE bit.

5.5 Enable/Disable Nonoversampling Filter

If the user decides to use the nonoversampling filter, the following sequences must be followed to enable/disable the nonoversampling filter.

5.5.1 Nonoversampling Filter Enable Sequence

Task	Register/Bit Fields	Value	Description
Configure PCM filter	0x10010	0x99	
	0xC0001	0x0C	
	PCM Filter Option 0x90000	0x22	
	FILTER_SLOW_FASTB	0	
	PHCOMP_LOWLATB	0	
	NOS	1	Nonoversampling filter is selected
	Reserved	0 00	
	HIGH_PASS	1	High-pass filter is selected
	DEEMP_ON	0	
	0x10010	0x0	

5.5.2 Nonoversampling Filter Disable Sequence

Task	Register/Bit Fields	Value	Description
Configure PCM filter	0x10010	0x99	
	0xC0001	0x0D	
	PCM Filter Option 0x90000	0x02	
	FILTER_SLOW_FASTB	0	
	PHCOMP_LOWLATB	0	
	NOS	0	
	Reserved	0 00	
	HIGH_PASS	1	High-pass filter is selected
	DEEMP_ON	0	
	0x10010	0x0	

5.6 CS4399 Analog Output and Filtering

The CS4399 requires an external opamp filter stage for driving headphone loads. One of the typical filter topologies used for this purpose is the multiple-feedback filter configuration. The CS4399 does not include phase or amplitude compensation for an external filter. Therefore, the DAC system and phase response is dependent on the external circuitry.

5.7 Audio Output Power Down Sequences

Examples of power down sequences for PCM and DSD are shown in Ex. 5-1 and Ex. 5-2, respectively. Follow the stated sequence every time to shut down the audio output. The sequence assumes that the PDN_DONE_INT interrupt bit is unmasked.

5.7.1 PCM Power Down Sequence

Example 5-1. PCM Power Down Sequence

Step	Task	Register/Bit Fields	Value	Description
1	Pop-free power down	0x10010	0x99	
		0xC0002	0x12	
		0xC000E	0x02	
		0xC0009	0x12	
2	Mute	PCM Path Signal Control 1. 0x90003	data(0x90003) OR (0x03)	
		PCM_RAMP_DOWN	x	
		PCM_VOL_BEQA	x	
		PCM_SZC	x	
		Reserved	x	
		PCM_AMUTE	x	
		PCM_AMUTEBEQA	x	
		PCM_MUTE_A	1	Mute channel A
		PCM_MUTE_B	1	Mute channel B
3	Wait time delay. If PCM_SZC = 2, then delay = (255 - max(PCM_VOLUME_A, PCM_VOLUME_B)) / 2 ms. Else, delay = 130 ms.			
4	Power down amplifier	Power Down Control. 0x20000	data(0x20000) OR (0x10)	
		PDN_XSP	x	
		PDN_ASP	x	
		PDN_DSDIF	x	
		PDN_HP	1	Turn off DAC output
		PDN_XTAL	x	
		PDN_PLL	x	
		PDN_CLKOUT	x	
		Reserved	x	
5	Wait for interrupt. Check for PDN_DONE_INT = 1 in Interrupt Status 1 register (0xF0000).			
6	Reset data buffer	0x90097	0x01	
7	Power down ASP	Power Down Control. 0x20000	data(0x20000) OR (0x40)	
		PDN_XSP	x	
		PDN_ASP	1	Turn off ASP
		PDN_DSDIF	x	
		PDN_HP	x	
		PDN_XTAL	x	
		PDN_PLL	x	
		PDN_CLKOUT	x	
		Reserved	x	
8	Unmute	PCM Path Signal Control 1. 0x90003	data(0x90003) AND (0xFC)	
		PCM_RAMP_DOWN	x	
		PCM_VOL_BEQA	x	
		PCM_SZC	x	
		Reserved	x	
		PCM_AMUTE	x	
		PCM_AMUTEBEQA	x	
		PCM_MUTE_A	0	Unmute channel A
		PCM_MUTE_B	0	Unmute channel B
9	Restore defaults	0xC0002	0x10	
		0xC000E	0x00	
		0xC0009	0x16	
		0x10010	0x00	

5.7.2 DSD Power Down Sequence

Example 5-2. DSD Power Down Sequence

Step	Task	Register/Bit Fields	Value	Description
10	Pop-free power down	0x10010	0x99	
		0xC0002	0x12	
		0xC000E	0x02	
		0xC0009	0x12	

Example 5-2. DSD Power Down Sequence *(Cont.)*

Step	Task	Register/Bit Fields	Value	Description
11	Mute	DSD Processor Path Signal Control 1. 0x70002	data(0x70002) OR (0x03)	
		Reserved	x	
		DSD_VOL_BEQA	x	
		DSD_SZC	x	
		Reserved	x	
		DSD_AMUTE	x	
		DSD_AMUTEBEQA	x	
		DSD_MUTE_A	1	Mute channel A
		DSD_MUTE_B	1	Mute channel B
12	Wait time delay. If DSD_SZC = 1, then delay = (255 - max(DSD_VOLUME_A, DSD_VOLUME_B)) / 2 ms. Else, delay = 130 ms.			
13	Power down amplifier	Power Down Control. 0x20000	data(0x20000) OR (0x10)	
		PDN_XSP	x	
		PDN_ASP	x	
		PDN_DSDIF	x	
		PDN_HP	1	Turn off DAC output
		PDN_XTAL	x	
		PDN_PLL	x	
		PDN_CLKOUT	x	
		Reserved	x	
14	Wait for interrupt. Check for PDN_DONE_INT = 1 in Interrupt Status 1 register (0xF0000).			
15	Reset data buffer	0x90097	0x01	
16	Power down DSD/XSP/ ASP interfaces	Power Down Control. 0x20000	data(0x20000) OR (0xE0)	
		PDN_XSP	1	
		PDN_ASP	1	
		PDN_DSDIF	1	
		PDN_HP	x	
		PDN_XTAL	x	
		PDN_PLL	x	
		PDN_CLKOUT	x	
		Reserved	x	
17	Unmute	DSD Processor Path Signal Control 1. 0x70002	data(0x70002) AND (0xFC)	
		Reserved	1	
		DSD_VOL_BEQA	x	
		DSD_SZC	x	
		Reserved	0	
		DSD_AMUTE	x	
		DSD_AMUTEBEQA	x	
		DSD_MUTE_A	0	Unmute channel A
		DSD_MUTE_B	0	Unmute channel B
18	Restore defaults	0xC0002	0x10	
		0xC000E	0x00	
		0xC0009	0x16	
		0x10010	0x00	

5.8 Audio Output Power-Up Initialization

An example of the power-up initialization for PCM and DSD are shown in Ex. 5-3 and Ex. 5-4, respectively. Follow the stated sequence every time to initialize the audio output.

5.8.1 PCM Power-Up Initialization

Example 5-3. PCM Power-Up Initialization

Step	Task	Register/Bit Fields	Value	Description
1	PCM Power-Up Initialization	0x10010	0x99	
		0x10025	0x01	
		0x1002E	0x00	
		0xC0006	0x01	
		0xC0002	0x12	
		0xC0009	0x00	
		0xC0003	0x28	
		0xC0005	0x28	

5.8.2 DSD Power-Up Initialization

Example 5-4. DSD Power-Up Initialization

Step	Task	Register/Bit Fields	Value	Description
1	DSD Power-Up Initialization	0x10010	0x99	
		0x10025	0x01	
		0x1002E	0x00	
		0xC0006	0x01	
		0xC0002	0x12	
		0xC0009	0x00	
		0xC0003	0x1E	
		0xC0005	0x20	

5.9 Audio Output Power-Up Sequence

An example of the power-up sequence for PCM and DSD are shown in Ex. 5-5 and Ex. 5-6, respectively. Follow the stated sequence every time to power up the audio output.

5.9.1 PCM Power-Up Sequence

Example 5-5. PCM Power-Up Sequence

Step	Task	Register/Bit Fields	Value	Description
1	Run PCM power-up initialization sequence in Ex. 5-3.			
2	Power up ASP	Power Down Control. 0x20000	data (0x20000) AND (0xBF)	
		PDN_XSP	x	
		PDN_ASP	0	Power up ASP
		PDN_DSDIF	x	
		PDN_HP	x	
		PDN_XTAL	x	
		PDN_PLL	x	
		PDN_CLKOUT	x	
		Reserved	x	
3	Pop-free startup	0x1002C	0x0A	
4	Power on amplifier	Power Down Control. 0x20000	data (0x20000) AND (0xEF)	
		PDN_XSP	x	
		PDN_ASP	x	
		PDN_DSDIF	x	
		PDN_HP	0	Power up DAC output
		PDN_XTAL	x	
		PDN_PLL	x	
		PDN_CLKOUT	x	
		Reserved	x	
5	Wait for 10 ms			
6	Restore defaults	0xC0006	0x0C	
		0xC0002	0x10	
		0xC0009	0x20	
7	Audio output will be active. Wait for 1000 ms.			
8	Restore defaults	0x1002C	0x00	
		0x10010	0x00	

5.9.2 DSD Power-Up Sequence

Example 5-6. DSD Power-Up Sequence

Step	Task	Register/Bit Fields	Value	Description
1	Run DSD power-up initialization sequence in Ex. 5-4.			
2	Power on appropriate interface.	Power Down Control. 0x20000	data (0x20000) AND (0xHH)	For DoP on XSP, HH = 7F. For DoP on ASP, HH = BF. For DSD interface, HH = DF.
		PDN_XSP	B	XSP interface enable
		PDN_ASP	B	ASP interface enable
		PDN_DSDIF	B	DSD interface enable
		PDN_HP	x	
		PDN_XTAL	x	
		PDN_PLL	x	
		PDN_CLKOUT	x	
		Reserved	x	
3	Pop-free startup	0x1002C	0x0A	
4	Power on amplifier	Power Down Control. 0x20000	data (0x20000) AND (0xEF)	
		PDN_XSP	x	
		PDN_ASP	x	
		PDN_DSDIF	x	
		PDN_HP	0	Power up DAC output
		PDN_XTAL	x	
		PDN_PLL	x	
		PDN_CLKOUT	x	
		Reserved	0	
5	Wait for 10 ms			
6	Restore defaults	0xC0006	0x0C	
		0xC0002	0x10	
		0xC0009	0x20	
7	Audio output will be active. Wait for 1000 ms.			
8	Restore defaults	0x1002C	0x00	
		0x10010	0x00	

5.10 Example Sequences

This section provides recommended instruction sequences for standard CS4399 operations.

5.10.1 Power-up Sequence to I²S Playback

In Ex. 5-7, a 22.5792-MHz crystal is used, ASP is set to I²S master at 44.1 kHz, and full-scale output is 1.732 Vrms.

Example 5-7. Startup to I²S Playback

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Apply all relevant power supplies, then assert $\overline{\text{RESET}}$.			
2	Wait for 1.5 ms			
3	Configure XTAL driver			
4	Configure XTAL bias current strength (assuming River Crystal at 22.5792 MHz)	Crystal Setting. 0x20052	0x04	
		Reserved	0000 0	
		XTAL_IBIAS	100	Bias current set to 12.5 µA
5	Read Interrupt Status 1 register (0xF0000) to clear any pending interrupts.			
6	Enable XTAL interrupts	Interrupt Mask 1. 0xF0010	0xE7	
		DAC_OVFL_INT_MASK	1	
		HPDETECT_PLUG_INT_MASK	1	Enable XTAL_READY interrupt
		HPDETECT_UNPLUG_INT_MASK	1	Enable XTAL_ERROR interrupt
		XTAL_READY_INT_MASK	0	
		XTAL_ERROR_INT_MASK	0	
		PLL_READY_INT_MASK	1	
		PLL_ERROR_INT_MASK	1	
		PDN_DONE_INT_MASK	1	
7	Start XTAL	Power Down Control. 0x20000	0xF6	
		PDN_XSP	1	
		PDN_ASP	1	
		PDN_DSDIF	1	
		PDN_HP	1	
		PDN_XTAL	0	Power up XTAL driver
		PDN_PLL	1	
		PDN_CLKOUT	1	
		Reserved	0	
8	Apply PCM power-up initialization in Ex. 5-3			
9	Configure ASP interface. Sample rate set to 44.1 kHz. ASP is clock master.			
10	Set ASP sample rate	Serial Port Sample Rate. 0x1000B	0x01	
		Reserved	0000	
		ASP_SPRATE	0001	Set sample rate to 44.1 kHz
11	Set ASP sample bit size. XSP is don't care	Serial Port Sample Bit Size. 0x1000C	0x04	
		Reserved	0000	
		XSP_SPSIZE	01	XSP sample bit size set to 24 bits
		ASP_SPSIZE	00	ASP sample bit size set to 32 bits
12	Set ASP numerator	ASP Numerator 1. 0x40010	0x01	
		ASP_N_LSB	0x01	LSB of ASP sample rate fractional divide numerator
		ASP Numerator 2. 0x40011	0x00	
		ASP_N_MSB	0x00	MSB of ASP sample rate fractional divide numerator
13	Set ASP denominator	ASP Denominator 1. 0x40012	0x08	
		ASP_M_LSB	0x08	LSB of ASP sample rate fractional divide denominator
		ASP Denominator 2. 0x40013	0x00	
		ASP_M_MSB	0x00	MSB of ASP sample rate fractional divide denominator
14	Set ASP LRCK high time	ASP LRCK High Time 1. 0x40014	0x1F	
		ASP_LCHI_LSB	0x1F	LSB of ASP LRCK high time duration
		ASP LRCK High Time 2. 0x40015	0x00	
		ASP_LCHI_MSB	0x00	MSB of ASP LRCK high time duration
15	Set ASP LRCK period	ASP LRCK Period 1. 0x40016	0x3F	
		ASP_LCPR_LSB	0x3F	LSB of ASP LRCK period
		ASP LRCK Period 2. 0x40017	0x00	
		ASP_LCPR_MSB	0x00	MSB of ASP LRCK period

Example 5-7. Startup to I²S Playback *(Cont.)*

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
16	Configure ASP clock	ASP Clock Configuration. 0x40018	0x1C	
		Reserved	000	
		ASP_M/SB	1	Set ASP port to be master
		ASP_SCPOL_OUT	1	Configure clock polarity for I²S input
		ASP_SCPOL_IN	1	
		ASP_LCPOL_OUT	0	
		ASP_LCPOL_IN	0	
17	Configure ASP frame	ASP Frame Configuration. 0x40019	0x0A	
		Reserved	000	Configure ASP port to accept I²S input
		ASP_STP	0	
		ASP_5050	1	
		ASP_FSD	010	
18	Set ASP channel location	ASP Channel 1 Location. 0x50000	0x00	
		ASP_RX_CH1	0x00	ASP Channel 1 starts on SCLK0
		ASP Channel 2 Location. 0x50001	0x00	
		ASP_RX_CH2	0x00	ASP Channel 2 starts on SCLK0
19	Set ASP channel size and enable	ASP Channel 1 Size and Enable. 0x5000A	0x07	
		Reserved	0000	
		ASP_RX_CH1_AP	0	ASP Channel 1 Active Phase
		ASP_RX_CH1_EN	1	ASP Channel 1 Enable
		ASP_RX_CH1_RES	11	ASP Channel 1 Size is 32 bits
		ASP Channel 2 Size and Enable. 0x5000B	0x0F	
		Reserved	0000	
		ASP_RX_CH2_AP	1	ASP Channel 2 Active Phase
		ASP_RX_CH2_EN	1	ASP Channel 2 Enable
		ASP_RX_CH2_RES	11	ASP Channel 2 Size is 32 bits
20	Configure PCM interface. HPF filter is used. Deemphasis off.			
21	Configure PCM filter	PCM Filter Option. 0x90000	0x02	
		FILTER_SLOW_FASTB	0	
		PHCOMP_LOWLATB	0	
		NOS	0	
		Reserved	0 00	
		HIGH_PASS	1	High pass filter is selected
		DEEMP_ON	0	
22	Set volume for channel B	PCM Volume B. 0x90001	0x00	
		PCM_VOLUME_B	0x00	Set volume to 0 dB
23	Set volume for channel A	PCM Volume A. 0x90002	0x00	
		PCM_VOLUME_A	0x00	Set volume to 0 dB
24	Configure PCM path signal control	PCM Path Signal Control 1. 0x90003	0xEC	
		PCM_RAMP_DOWN	1	Soft ramp down of volume on filter change
		PCM_VOL_BEQA	1	Volume setting on both channels controlled by PCM_VOLUME_A
		PCM_SZC	10	Enable soft ramp
		PCM_AMUTE	1	Mute after reception of 8192 samples of 0 or –1.
		PCM_AMUTEBEQA	1	Mute only when AMUTE condition is detected on both channels
		PCM_MUTE_A	0	Function is disabled
		PCM_MUTE_B	0	Function is disabled
		PCM Path Signal Control 2. 0x90004	0x00	
		Reserved	0000	
		PCM_INV_A	0	Disable all functions in this register
		PCM_INV_B	0	
		PCM_SWAP_CHAN	0	
		PCM_COPY_CHAN	0	
25	Configure DAC output			
26	Configure Class H amplifier	Class H Control. 0xB0000	0x1E	
		Reserved	000	
		ADPT_PWR	1 11	Output signal determines voltage level
		HV_EN	1	High voltage mode enabled
		EXT_VCPFILT	0	Using internal VCPFILT source.
27	Set DAC output to full scale	Analog Output Control 1. 0x80000	0x30	
		Reserved	0	
		Reserved	0	
		OUT_FS	11	Set DAC output to full scale (1.732 V rms)
		Reserved	0	
		Reserved	000	

Example 5-7. Startup to I²S Playback *(Cont.)*

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
28	Configure Headphone detect	HP Detect. 0xD0000	0x04	
		HPDETECT_CTRL	00	HP detect disabled
		HPDETECT_INV	0	HP detect input is not inverted
		HPDETECT_RISE_DBC_TIME	0 0	Tip sense rising debounce time set to 0 ms
		HPDETECT_FALL_DBC_TIME	10	Tip sense falling debounce time set to 500 ms
		Reserved	0	
29	Headphone detect	HP Detect. 0xD0000	0xC4	
		HPDETECT_CTRL	11	HP detect enabled
		HPDETECT_INV	0	HP detect input is not inverted
		HPDETECT_RISE_DBC_TIME	0 0	Tip sense rising debounce time set to 0 ms
		HPDETECT_FALL_DBC_TIME	10	Tip sense falling debounce time set to 500 ms
		Reserved	0	
30	Enable interrupts			
31	Read Interrupt Status 1 register (0xF0000) and Interrupt Status 2 register (0xF0001) to clear sticky bits.			
32	Enable headphone detect interrupts	Interrupt Mask 1. 0xF0010	0x87	
		DAC_OVFL_INT_MASK	1	
		HPDETECT_PLUG_INT_MASK	0	Enable HPDETECT_PLUG interrupt
		HPDETECT_UNPLUG_INT_MASK	0	Enable HPDETECT_UNPLUG interrupt
		XTAL_READY_INT_MASK	0	
		XTAL_ERROR_INT_MASK	0	
		PLL_READY_INT_MASK	1	
		PLL_ERROR_INT_MASK	1	
		PDN_DONE_INT_MASK	1	
33	Enable ASP interrupts	Interrupt Mask 2. 0xF0011	0x07	
		ASP_OVFL_INT_MASK	0	Enable ASP_OVFL interrupt
		ASP_ERROR_INT_MASK	0	Enable ASP_ERROR interrupt
		ASP_LATE_INT_MASK	0	Enable ASP_LATE interrupt
		ASP_EARLY_INT_MASK	0	Enable ASP_EARLY interrupt
		ASP_NOLRCK_INT_MASK	0	Enable ASP_NOLRCK interrupt
		Reserved	111	
34	Wait for interrupt. Check if XTAL_READY_INT = 1 in Interrupt Status 1 register (0xF0000).			
35	Switch MCLK source to XTAL	System Clocking Control 1. 0x10006	0x04	
		Reserved	0000 0	MCLK Source set to XTAL. MCLK_INT frequency set to 22.5792 MHz
		MCLK_INT	1	
		MCLK_SRC_SEL	00	
36	Wait at least 150 µs.			
37	Enable ASP clocks	Pad Interface Configuration. 0x1000D	0x02	
		Reserved	0000 00	
		XSP_3ST	1	XSP Interface status is don't care (set to default)
		ASP_3ST	0	Enable serial clocks in Master Mode
38	Power up DAC	Refer to Ex. 5-5 for PCM power-up sequence. Skip Step 1 of Ex. 5-5 (completed in Step 8 above).		

5.10.2 Power-Up Sequence to DSD Playback

In Ex. 5-8, a 22.5792-MHz crystal is used, the PLL is used to create a 24.576-MHz MCLK, XSP is set as DSD slave at 2.8224 MHz, and full-scale output is 1.732 Vrms.

Example 5-8. Startup to DSD Playback

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Apply all relevant power supplies, then assert $\overline{\text{RESET}}$.			
2	Wait for 1.5 ms			
3	Configure XTAL driver			
4	Configure XTAL bias current strength (assuming River Crystal at 22.5792 MHz)	Crystal Setting. 0x20052	0x04	
		Reserved	0000 0	
		XTAL_IBIAS	100	Bias current set to 12.5 µA
5	Read Interrupt Status 1 register (0xF0000) to clear any pending interrupts.			
6	Enable XTAL interrupts	Interrupt Mask 1. 0xF0010	0xE7	
		DAC_OVFL_INT_MASK	1	
		HPDETECT_PLUG_INT_MASK	1	
		HPDETECT_UNPLUG_INT_MASK	1	
		XTAL_READY_INT_MASK	0	Enable XTAL_READY interrupt
		XTAL_ERROR_INT_MASK	0	Enable XTAL_ERROR interrupt
		PLL_READY_INT_MASK	1	
		PLL_ERROR_INT_MASK	1	
		PDN_DONE_INT_MASK	1	

Example 5-8. Startup to DSD Playback *(Cont.)*

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
7	Start XTAL	Power Down Control. 0x20000	0xF6	
		PDN_XSP	1	
		PDN_ASP	1	
		PDN_DSDIF	1	
		PDN_HP	1	
		PDN_XTAL	0	Power up XTAL driver
		PDN_PLL	1	
		PDN_CLKOUT	1	
		Reserved	0	
8	Apply DSD power-up initialization in Ex. 5-4			
9	Configure PLL. Input is 22.5792 MHz. Output is 24.576 MHz.			
10	Power up PLL	Power Down Control. 0x20000	0xF2	
		PDN_XSP	1	
		PDN_ASP	1	
		PDN_DSDIF	1	
		PDN_HP	1	
		PDN_XTAL	0	
		PDN_PLL	0	Power up PLL
		PDN_CLKOUT	1	
		Reserved	0	
11	Set PLL Pre-Divide	PLL Setting 9. 0x40002	0x03	
		PLL_REF_PREDIV	11	Divide PLL Reference by 8
		Reserved	00 0000	
12	Set PLL Output Divide	PLL Setting 6. 0x30008	0x08	
		PLL_OUT_DIV	0x08	Divide PLL output by 8
13	Set Fractional portion of PLL divide ratio	PLL Setting 2. 0x30002	0x00	
		PLL_DIV_FRAC_0	0x00	
		PLL Setting 3. 0x30003	0xF7	
		PLL_DIV_FRAC_1	0xF7	
		PLL Setting 4. 0x30004	0x06	
		PLL_DIV_FRAC_2	0x06	
14	Set integer portion of PLL divide ratio	PLL Setting 5. 0x30005	0x44	
		PLL_DIV_INT	0x44	
15	Set PLL Mode	PLL Setting 8. 0x3001B	0x01	
		Reserved	0000 00	
		PLL_MODE	0	Use 500/512 factor
		Reserved	1	
16	Set PLL Calibration Ratio	PLL Setting 7. 0x3000A	0x8B	
		PLL_CAL_RATIO	0x8B	Set PLL Cal Ratio to 139
17	Read Interrupt Status 1 register (0xF0000) to clear any pending interrupts.			
18	Enable PLL Interrupts	Interrupt Mask 1. 0xF0010	0xE1	
		DAC_OVFL_INT_MASK	1	
		HPDETECT_PLUG_INT_MASK	1	
		HPDETECT_UNPLUG_INT_MASK	1	Enable PLL Ready and Error Interrupts
		XTAL_READY_INT_MASK	0	
		XTAL_ERROR_INT_MASK	0	
		PLL_READY_INT_MASK	0	
		PLL_ERROR_INT_MASK	0	
		PDN_DONE_INT_MASK	1	
19	Start PLL	PLL Setting 1. 0x30001	0x01	
		Reserved	000 0001	
		PLL_START	0	Start PLL
20	Configure DSDIF to playback 64•Fs DSD stream. DSDIF is configured as a slave.			
21	Configure DSD Volume	DSD Volume A. 0x70001	0x00	
		DSD_VOLUME_A	0x00	Channel A volume set to 0dB
22	Configure DSD path Signal Control1	DSD Processor Path Signal Control 1. 0x70002	0xEC	
		Reserved	1	
		DSD_VOL_BEQA	1	DSD Volume B equals DSD volume A
		DSD_SZC	1	Soft ramp control enabled
		Reserved	0	
		DSD_AMUTE	1	Mute occurs after 256 repeated 8-bit DSD mute patterns
		DSD_AMUTE_BEQA	1	Mute happens only when mute pattern is detected in both channels
		DSD_MUTE_A	0	Function is disabled
		DSD_MUTE_B	0	Function is disabled

Example 5-8. Startup to DSD Playback *(Cont.)*

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
23	Configure DSD Interface	DSD Interface Configuration. 0x70003	0x00	
		Reserved	0000 0	
		DSD_M/SB	0	DSD is clock slave
		DSD_PM_EN	0	Function is disabled
		DSD_PM_SEL	0	Function is disabled
24	Configure DSD path Signal Control 2	DSD Processor Path Signal Control 2. 0x70004	0x13	
		Reserved	0	
		DSD_PRC_SRC	00	Set source of DSD processor to DSDIF
		DSD_EN	1	Enable DSD playback
		Reserved	0	
		DSD_SPEED	0	Set DSD clock speed to 64•FS
		STA_DSD_DET	1	Static DSD detection enabled
		INV_DSD_DET	1	Invalid DSD detection enabled
25	Configure DAC output			
26	Configure Class H Amplifier	Class H Control. 0xB0000	0x1E	
		Reserved	000	
		ADPT_PWR	111	Output Signal determines voltage level
		HV_EN	1	High Voltage Mode Enabled
		EXT_VCPFILT	0	Using Internal VCPFILT source.
27	Set DAC output to full scale	Analog Output Control 1. 0x80000	0x30	
		Reserved	0	
		Reserved	0	
		OUT_FS	11	Set DAC output to Full Scale (1.732 V rms)
		Reserved	0	
		Reserved	000	
28	Configure Headphone Detect	HP Detect. 0xD0000	0x04	
		HPDETECT_CTRL	00	HP Detect disabled
		HPDETECT_INV	0	HP detect input is not inverted
		HPDETECT_RISE_DBC_TIME	0 0	Tip Sense rising debounce time set to 0ms
		HPDETECT_FALL_DBC_TIME	10	Tip sense falling debounce time set to 500ms
		Reserved	0	
29	Headphone Detect	HP Detect. 0xD0000	0xC4	
		HPDETECT_CTRL	11	HP Detect enabled
		HPDETECT_INV	0	HP detect input is not inverted
		HPDETECT_RISE_DBC_TIME	0 0	Tip Sense rising debounce time set to 0ms
		HPDETECT_FALL_DBC_TIME	10	Tip sense falling debounce time set to 500ms
		Reserved	0	
30	Enable Interrupts			
31	Read Interrupt Status 1 register (0xF0000) and Interrupt Status 5 register (0xF0004) to clear sticky bits			
32	Enable Headphone Detect Interrupts	Interrupt Mask 1. 0xF0010	0x81	
		DAC_OVFL_INT_MASK	1	
		HPDETECT_PLUG_INT_MASK	0	Unmask HPDETECT_PLUG interrupt and
		HPDETECT_UNPLUG_INT_MASK	0	HPDETECT_UNPLUG interrupt
		XTAL_READY_INT_MASK	0	
		XTAL_ERROR_INT_MASK	0	
		PLL_READY_INT_MASK	0	
		PLL_ERROR_INT_MASK	0	
		PDN_DONE_INT_MASK	1	
33	Enable DSD Interrupts	Interrupt Mask 5. 0xF0014	0x03	
		DSD_STUCK_INT_MASK	0	Enable DSD_STUCK interrupt
		DSD_INVAL_A_INT_MASK	0	Enable DSD_INVAL_A interrupt
		DSD_INVAL_B_INT_MASK	0	Enable DSD_INVAL_B interrupt
		DSD_SILENCE_A_INT_MASK	0	Enable DSD_SILENCE_A interrupt
		DSD_SILENCE_B_INT_MASK	0	Enable DSD_SILENCE_B interrupt
		DSD_RATE_ERROR_INT_MASK	0	Enable DSD_RATE_ERROR interrupt
		DOP_MRK_DET_INT_MASK	1	Disable DOP_MRK_DET interrupt
		DOP_ON_INT_MASK	1	Disable DOP_ON interrupt
34	Wait for interrupt. Check if PLL_READY_INT = 1 in Interrupt Status 1 register(0xF0000)			
35	Switch MCLK source to PLL	System Clocking Control 1. 0x10006	0x01	
		Reserved	0000 0	MCLK Source set to PLL. MCLK_INT frequency set
		MCLK_INT	0	to 24.576 MHz
		MCLK_SRC_SEL	01	
36	Wait at least 150 µs			
37	Power up DAC	Refer to Ex. 5-6 for DSD power-up sequence. Skip Step 1 of Ex. 5-6 (completed in Step 8 above).		

5.10.3 Power-Up Sequence to DoP Playback with PLL

In Ex. 5-9, an external 19.2-MHz MCLK is used with a PLL to generate an internal MCLK or 22.5792 MHz, and the ASP is in clock master receiving DoP data with LRCLK at 176.4 kHz and SCLK at 8.4672 MHz.

Example 5-9. DoP Playback with PLL

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Apply all relevant power supplies, then assert $\overline{\text{RESET}}$.			
2	Wait for 1.5 ms			
3	Apply DSD power-up initialization in Ex. 5-4			
4	Configure PLL. XTI/MCLK input coming from an external 19.2 MHz source with PLL output set to 22.5792 MHz. Refer to Section 4.6.2 for register settings for other frequency combinations			
5	Power up PLL	Power Down Control. 0x20000	0xFA	
		PDN_XSP	x	
		PDN_ASP	x	
		PDN_DSDIF	x	
		PDN_HP	x	
		PDN_XTAL	x	
		PDN_PLL	0	Power up PLL block
		PDN_CLKOUT	x	
		Reserved	0	
6	Set PLL Predivide value	PLL Setting 9. 0x40002	0x03	
		Reserved	0000 00	
		PLL_REF_PREDIV	11	Set PLL predivide value to 8
7	Set PLL output divide	PLL Setting 6. 0x30008	0x08	
		PLL_OUT_DIV	0x08	Set PLL output divide value to 8
8	Set Fractional portion of PLL Divide Ratio	PLL Setting 2. 0x30002	0x00	
		PLL_DIV_FRAC_0	0x00	Set LSB of PLL fractional divider value to 0
		PLL Setting 3. 0x30003	0x00	
		PLL_DIV_FRAC_1	0x00	Set Middle Byte of PLL fractional divider value to 0
		PLL Setting 4. 0x30004	0x80	
		PLL_DIV_FRAC_2	0x80	Set MSB of PLL fractional divider value to 0x80
9	Set Integer portion of PLL Divide Ratio	PLL Setting 5. 0x30005	0x49	
		PLL_DIV_INT	0x49	Set PLL integer Divide value to 0x49
10	Set PLL mode	PLL Setting 8. 0x3001B	0x01	
		Reserved	0000 00	
		PLL_MODE	0	500/512 factor is used in PLL frequency calculation
		Reserved	1	
11	Read Interrupt Status 1 register (0xF0000) to clear sticky bits.			
12	Set PLL calibration ratio	PLL Setting 7. 0x3000A	0x97	
		PLL_CAL_RATIO	0x97	PLL Calibration Ratio is set to 0x97 (151)
13	Enable PLL interrupts	Interrupt Mask 1. 0xF0010	0xF9	
		DAC_OVFL_INT_MASK	1	DAC_OVFL_INT is don't care
		HPDETECT_PLUG_INT_MASK	1	Unmask HPDETECT_PLUG interrupt
		HPDETECT_UNPLUG_INT_MASK	1	Unmask HPDETECT_UNPLUG interrupt
		XTAL_READY_INT_MASK	1	XTAL_READY_INT is Don't Care
		XTAL_ERROR_INT_MASK	1	XTAL_ERROR_INT is Don't Care
		PLL_READY_INT_MASK	0	PLL_READY Interrupt is already unmasked
		PLL_ERROR_INT_MASK	0	PLL_ERROR Interrupt is already unmasked
		PDN_DONE_INT_MASK	1	PDN_DONE_INT is Don't Care
14	Start PLL	PLL Setting 1. 0x30001	0x01	
		Reserved	0000 000	
		PLL_START	1	Enable PLL Output
15	Playback DoP audio. Assuming 64•Fs DSD stream			
16	Configure ASP interface for DoP input			
17	Set ASP sample rate	Serial Port Sample Rate. 0x1000B	0x05	
		Reserved	0000	
		ASP_SPRATE	0101	Set sample rate to 176.4 kHz
18	Set ASP sample bit size. XSP is don't care	Serial Port Sample Bit Size. 0x1000C	0x05	
		Reserved	0000	
		XSP_SPSIZE	01	XSP sample bit size set to 24 bits
		ASP_SPSIZE	01	ASP sample bit size set to 24 bits

Example 5-9. DoP Playback with PLL *(Cont.)*

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
19	Set ASP numerator	ASP Numerator 1. 0x40010	0x03	
		ASP_N_LSB	0x03	LSB of ASP sample rate fractional divide numerator
		ASP Numerator 2. 0x40011	0x00	
		ASP_N_MSB	0x00	MSB of ASP sample rate fractional divide numerator
20	Set ASP denominator	ASP Denominator 1. 0x40012	0x08	
		ASP_M_LSB	0x08	LSB of ASP sample rate fractional divide denominator
		ASP Denominator 2. 0x40013	0x00	
		ASP_M_MSB	0x00	MSB of ASP sample rate fractional divide denominator
21	Set ASP LRCK high time	ASP LRCK High Time 1. 0x40014	0x17	
		ASP_LCHI_LSB	0x17	LSB of ASP LRCK high time duration
		ASP LRCK High Time 2. 0x40015	0x00	
		ASP_LCHI_MSB	0x00	MSB of ASP LRCK high time duration
22	Set ASP LRCK period	ASP LRCK Period 1. 0x40016	0x2F	
		ASP_LCPR_LSB	0x2F	LSB of ASP LRCK period
		ASP LRCK Period 2. 0x40017	0x00	
		ASP_LCPR_MSB	0x00	MSB of ASP LRCK period
23	Configure ASP clock	ASP Clock Configuration. 0x40018	0x1C	
		Reserved	000	
		ASP_M/SB	1	Set ASP port to be Master
		ASP_SCPOL_OUT	1	Set output SCLK polarity
		ASP_SCPOL_IN	1	Input SCLK polarity is don't care
		ASP_LCPOL_OUT	0	Set Output LRCK polarity
		ASP_LCPOL_IN	0	Input LRCK polarity is don't care
24	Configure ASP frame	ASP Frame Configuration. 0x40019	0x0A	
		Reserved	000	
		ASP_STP	0	
		ASP_5050	1	Configure ASP port to accept I²S input
		ASP_FSD	010	
25	Set ASP channel location	ASP Channel 1 Location. 0x50000	0x00	
		ASP_RX_CH1	0x00	ASP Channel 1 starts on SCLK0
		ASP Channel 2 Location. 0x50001	0x00	
		ASP_RX_CH2	0x00	ASP Channel 2 starts on SCLK0
26	Set ASP channel size and enable	ASP Channel 1 Size and Enable. 0x5000A	0x06	
		Reserved	0000	
		ASP_RX_CH1_AP	0	ASP Channel 1 active phase
		ASP_RX_CH1_EN	1	ASP Channel 1 enable
		ASP_RX_CH1_RES	10	ASP Channel 1 size is 24 bits
		ASP Channel 2 Size and Enable. 0x5000B	0x0E	
		Reserved	0000	
		ASP_RX_CH2_AP	1	ASP Channel 2 active phase
		ASP_RX_CH2_EN	1	ASP Channel 2 enable
		ASP_RX_CH2_RES	10	ASP Channel 2 size is 24 bits
27	Wait for interrupt. Check if PLL_READY_INT = 1 in Interrupt Status 1 register(0xF0000).			
28	Configure DSD processor			
29	Configure DSD volume	DSD Volume A. 0x70001	0x00	
		DSD_VOLUME_A	0x00	Channel A volume set to 0 dB
30	Configure DSD Path Signal Control 1	DSD Processor Path Signal Control 1. 0x70002	0xEC	
		Reserved	1	
		DSD_VOL_BEQA	1	DSD Volume B equals DSD volume A
		DSD_SZC	1	Soft ramp control enabled
		Reserved	0	
		DSD_AMUTE	1	Mute occurs after 256 repeated 8-bit DSD mute patterns
		DSD_AMUTE_BEQA	1	Mute happens only when mute pattern is detected in both channels
		DSD_MUTE_A	0	Function is disabled
		DSD_MUTE_B	0	Function is disabled

Example 5-9. DoP Playback with PLL *(Cont.)*

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
31	Configure DSD interface	DSD Interface Configuration. 0x70003	0x04	
		Reserved	0000 0	
		DSD_M/SB	1	DSD is clock master
		DSD_PM_EN	0	Function is disabled
		DSD_PM_SEL	0	Function is disabled
32	Configure DSD Path Signal Control 2	DSD Processor Path Signal Control 2. 0x70004	0x50	
		Reserved	0	
		DSD_PRC_SRC	10	Set source of DSD processor to ASP
		DSD_EN	1	Enable DSD playback
		Reserved	0	
		DSD_SPEED	0	Set DSD clock speed to 64•Fs
		STA_DSD_DET	0	Static DSD detection disabled
		INV_DSD_DET	0	Invalid DSD detection disabled
33	Configure DSD path Signal Control 3	DSD Processor Path Signal Control 3. 0x70006	0xC0	
		DSD_ZERODB	1	The SACD 0–dB reference level (50%modulation index) matches PCM 0-dB full scale.
		DSD_HPF_EN	1	Enable HPF in DSD processor
		Reserved	0	
		SIGCTL_DSDEQPCM	0	Function is disabled
		DSD_INV_A	0	Function is disabled
		DSD_INV_B	0	Function is disabled
		DSD_SWAP_CHAN	0	Function is disabled
		DSD_COPY_CHAN	0	Function is disabled
34	Configure DAC output for 1.732 V rms			
35	Configure Class H amplifier	Class H Control. 0xB0000	0x1E	
		Reserved	000	
		ADPT_PWR	1 11	Output signal determines voltage level
		HV_EN	1	High voltage mode enabled
		EXT_VCPFILT	0	Using internal VCPFILT source.
36	Set DAC output to full scale	Analog Output Control 1. 0x80000	0x30	
		Reserved	0	
		Reserved	0	
		OUT_FS	11	Set DAC output to full scale (1.732 V rms)
		Reserved	0	
		Reserved	000	
37	Headphone detect	HP Detect. 0xD0000	0xC4	
		HPDETECT_CTRL	11	HP detect enabled
		HPDETECT_INV	0	HP detect input is not inverted
		HPDETECT_RISE_DBC_TIME	0 0	Tip Sense rising debounce time set to 0 ms
		HPDETECT_FALL_DBC_TIME	10	Tip sense falling debounce time set to 500 ms
		Reserved	0	
38	Enable interrupts			
39	Read Interrupt Status 1 register (0xF0000), Interrupt Status 2 register (0xF0001) and Interrupt Status 5 register (0xF0004) to clear sticky bits.			
40	Enable headphone detect interrupts	Interrupt Mask 1. 0xF0010	0x99	
		DAC_OVFL_INT_MASK	1	DAC_OVFL_INT is don't care
		HPDETECT_PLUG_INT_MASK	0	Enable HPDETECT_PLUG interrupt
		HPDETECT_UNPLUG_INT_MASK	0	Enable HPDETECT_UNPLUG interrupt
		XTAL_READY_INT_MASK	1	XTAL_READY_INT is don't care
		XTAL_ERROR_INT_MASK	1	XTAL_ERROR_INT is don't care
		PLL_READY_INT_MASK	0	PLL_READY interrupt already enabled
		PLL_ERROR_INT_MASK	0	PLL_ERROR interrupt already enabled
		PDN_DONE_INT_MASK	1	PDN_DONE_INT is don't care
41	Enable ASP interrupts	Interrupt Mask 2. 0xF0011	0x07	
		ASP_OVFL_INT_MASK	0	Enable ASP_OVFL interrupt
		ASP_ERROR_INT_MASK	0	Enable ASP_ERROR interrupt
		ASP_LATE_INT_MASK	0	Enable ASP_LATE interrupt
		ASP_EARLY_INT_MASK	0	Enable ASP_EARLY interrupt
		ASP_NOLRCK_INT_MASK	0	Enable ASP_NOLRCK interrupt
		Reserved	111	
42	Enable DSD and DoP interrupts	Interrupt Mask 5. 0xF0014	0x01	
		DSD_STUCK_INT_MASK	0	Enable DSD_STUCK interrupt
		DSD_INVAL_A_INT_MASK	0	Enable DSD_INVAL_A interrupt
		DSD_INVAL_B_INT_MASK	0	Enable DSD_INVAL_B interrupt
		DSD_SILENCE_A_INT_MASK	0	Enable DSD_SILENCE_A interrupt
		DSD_SILENCE_B_INT_MASK	0	Enable DSD_SILENCE_B interrupt
		DSD_RATE_ERROR_INT_MASK	0	Enable DSD_RATE_ERROR interrupt
		DOP_MRK_DET_INT_MASK	0	Enable DOP_MRK_DET interrupt
		DOP_ON_INT_MASK	1	Disable DOP_ON interrupt
43	Wait for interrupt. Check if PLL_READY_INT = 1 in Interrupt Status 1 register(0xF0000).			

Example 5-9. DoP Playback with PLL *(Cont.)*

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
44	Set MCLK source and frequency	System Clocking Control. 0x10006	0x05	
		Reserved	0000 0	
		MCLK_INT	1	MCLK Frequency is set to 22.5792 MHz
		MCLK_SRC_SEL	01	MCLK Source is set to PLL
45	Wait for at least 150 µs.			
46	Enable ASP clocks	Pad Interface Configuration. 0x1000D	0x02	
		Reserved	0000 00	
		XSP_3ST	1	XSP Interface status is don't care (set to default)
		ASP_3ST	0	Enable serial clocks in Master Mode
47	Power up DAC	Refer to Ex. 5-6 for DSD power-up sequence. Note that in Step 2 of Ex. 5-6, HH = BF for DoP on ASP interface. Skip Step 1 of Ex. 5-6 (completed in Step 3 above).		

5.10.4 Switching MCLK Frequency

Ex. 5-10 shows steps necessary to switch the MCLK frequency in order to play audio at a different sample rate that is no longer an integer divide of current MCLK. It makes the following assumptions:

- The CS4399 is already powered up and out of reset.
- MCLK is sourced directly from external clock input (Direct MCLK). MCLK_INT is 22.5792 MHz, and the sample rate is an integer divide of MCLK.
- ASP is used for audio delivery and PDN_HP = 0.

Example 5-10. Sequence for Switching MCLK Frequency

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Power down PCM	Refer to Ex. 5-1 for PCM power-down sequence		
2	Switch MCLK Source to RCO			
3	Set MCLK Source to RCO	System Clocking Control 1. 0x10006	0x06	
		Reserved	0000 0	
		MCLK_INT	1	Frequency of MCLK_INT is don't care
		MCLK_SRC_SEL	10	MCLK source set to RCO
4	Wait for 150 µs			
5	Switch to a different MCLK Frequency. Assuming new MCLK frequency is 24.576MHz.			
6	Change MCLK_INT frequency to 24.576 MHz	System Clocking Control 1. 0x10006	0x02	
		Reserved	0000 0	
		MCLK_INT	0	MCLK_INT frequency set to 24.576 MHz
		MCLK_SRC_SEL	10	
7	Apply PCM power-up initialization in Ex. 5-3			
8	Configure ASP for appropriate sample rate, bit size and clock mode. Unmute PCM CHA and CHB outputs. Enable appropriate interrupts			
9	Switch MCLK source to direct MCLK mode	System Clocking Control 1. 0x10006	0x0	
		Reserved	0000 0	
		MCLK_INT	0	MCLK_INT frequency set to 24.576 MHz
		MCLK_SRC_SEL	00	MCLK source set to direct MCLK mode
10	Wait at least 150 µs.			
11	Power up DAC	Refer to Ex. 5-5 for PCM power-up sequence. Skip Step 1 of Ex. 5-5 (completed in Step 7 above).		

5.10.5 Headphone Detection

Ex. 5-11 shows steps necessary to detect the presence of a headphone. It makes the following assumptions:

- The CS4399 is already powered up and out of reset.
- The HP Detect register is not configured.

Example 5-11. Sequence for Headphone Detection

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Read Interrupt Status 1 register (0xF0000) to clear any sticky bits.			
2	Read HP Status register (0xD0001) to clear any sticky bits.			
3	Enable HPDETECT interrupts	Interrupt Mask 1. 0xF0010	data (0xF0010) AND 0x9F	
		DAC_OVFL_INT_MASK	x	
		HPDETECT_PLUG_INT_MASK	0	Enable HPDETECT interrupts
		HPDETECT_UNPLUG_INT_MASK	0	
		XTAL_READY_INT_MASK	x	
		XTAL_ERROR_INT_MASK	x	
		PLL_READY_INT_MASK	x	
		PLL_ERROR_INT_MASK	x	
		PDN_DONE_INT_MASK	x	
4	Configure HP Detect parameters	HP Detect. 0xD0000	0x04	
		HPDETECT_CTRL	00	
		HPDETECT_INV	0	
		HPDETECT_RISE_DBC_TIME	0 0	Rising edge debounce time set to 0 ms
		HPDETECT_FALL_DBC_TIME	10	Falling edge debounce time set to 500 ms
		Reserved	0	
5	Enable HP Detect	HP Detect. 0xD0000	data (0xD0000) OR (0xC0)	
		HPDETECT_CTRL	11	Enable headphone detection
		HPDETECT_INV	x	
		HPDETECT_RISE_DBC_TIME	x x	
		HPDETECT_FALL_DBC_TIME	xx	
		Reserved	0	

Example 5-11. Sequence for Headphone Detection *(Cont.)*

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
6	Wait for interrupt. Check if HPDETECT_PLUG_INT or HPDETECT_UNPLUG_INT is set in the Interrupt Status 1 register (0xF0000).			

5.10.6 DoP and PCM Mixing

Ex. 5-12 shows steps necessary to mix DoP and PCM. The XSP is in clock master receiving DoP data with LRCLK at 176.4 kHz and SCLK at 8.4672 MHz. The ASP is clock master receiving PCM data with LRCLK at 44.1 kHz and SCLK at 2.8224 MHz.

Example 5-12. DoP and PCM Mixing

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
1	Apply all relevant power supplies, then assert $\overline{\text{RESET}}$.			
2	Wait for 1.5 ms			
3	Configure XTAL Driver			
4	Configure XTAL bias current strength (assuming River Crystal at 22.5792 MHz)	Crystal Setting. 0x20052	0x04	
		Reserved	0000 0	
		XTAL_IBIAS	100	Bias current set to 12.5 µA
5	Enable XTAL interrupts	Interrupt Mask 1. 0xF0010	0xE7	
		DAC_OVFL_INT_MASK	1	
		HPDETECT_PLUG_INT_MASK	1	
		HPDETECT_UNPLUG_INT_MASK	1	
		XTAL_READY_INT_MASK	0	Enable XTAL_READY interrupt
		XTAL_ERROR_INT_MASK	0	Enable XTAL_ERROR interrupt
		PLL_READY_INT_MASK	1	
		PLL_ERROR_INT_MASK	1	
		PDN_DONE_INT_MASK	1	
6	Start XTAL	Power Down Control. 0x20000	0xF6	
		PDN_XSP	1	
		PDN_XSP	1	
		PDN_DSDIF	1	
		PDN_HP	1	
		PDN_XTAL	0	Power up XTAL driver
		PDN_PLL	1	
		PDN_CLKOUT	1	
		Reserved	0	
7	Apply DSD power-up initialization in Ex. 5-4			
8	Playback DoP audio. Assuming 64•Fs DSD stream			
9	Configure XSP interface for DoP input.			
10	Set sample bit size.	Serial Port Sample Bit Size. 0x1000C	0x05	
		Reserved	0000	
		XSP_SPSIZE	01	XSP sample bit size is set to 24 bits
		ASP_SPSIZE	01	ASP sample bit size is set to 24 bits
11	Set XSP Numerator	XSP Numerator 1. 0x40020	0x03	
		XSP_N_LSB	0x03	LSB of XSP sample rate fractional divide numerator
		XSP Numerator 2. 0x40021	0x00	
		XSP_N_MSB	0x00	MSB of XSP sample rate fractional divide numerator
12	Set XSP Denominator	XSP Denominator 1. 0x40022	0x08	
		XSP_M_LSB	0x08	LSB of XSP sample rate fractional divide denominator
		XSP Denominator 2. 0x40023	0x00	
		XSP_M_MSB	0x00	MSB of XSP sample rate fractional divide denominator
13	Set XSP LRCK high Time	XSP LRCK High Time 1. 0x40024	0x17	
		XSP_LCHI_LSB	0x17	LSB of XSP LRCK high time duration
		XSP LRCK High Time 2. 0x40025	0x00	
		XSP_LCHI_MSB	0x00	MSB of XSP LRCK high time duration
14	Set XSP LRCK period	XSP LRCK Period 1. 0x40026	0x2F	
		XSP_LCPR_LSB	0x2F	LSB of XSP LRCK period
		XSP LRCK Period 2. 0x40027	0x00	
		XSP_LCPR_MSB	0x00	MSB of XSP LRCK period
15	Configure XSP Clock	XSP Clock Configuration. 0x40028	0x1C	
		Reserved	000	
		XSP_M/SB	1	Set XSP port to be Master
		XSP_SCPOL_OUT	1	Set output SCLK polarity
		XSP_SCPOL_IN	1	Input SCLK polarity is don't care
		XSP_LCPOL_OUT	0	Set Output LRCLK polarity
		XSP_LCPOL_IN	0	Input LRCLK polarity is don't care

Example 5-12. DoP and PCM Mixing *(Cont.)*

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
16	Configure XSP Frame	XSP Frame Configuration. 0x40029	0x0A	
		Reserved	000	
		XSP_STP	0	Configure XSP port to accept I²S input
		XSP_5050	1	
		XSP_FSD	010	
17	Set XSP Channel Location	XSP Channel 1 Location. 0x60000	0x00	
		XSP_RX_CH1	0x00	XSP Channel 1 starts on SCLK0
		XSP Channel 2 Location. 0x60001	0x00	
		XSP_RX_CH2	0x00	XSP Channel 2 starts on SCLK0
18	Set XSP Channel Size and Enable	XSP Channel 1 Size and Enable. 0x6000A	0x06	
		Reserved	0000	
		XSP_RX_CH1_AP	0	XSP Channel 1 Active Phase
		XSP_RX_CH1_EN	1	XSP Channel 1 Enable
		XSP_RX_CH1_RES	10	XSP Channel 1 Size is 24 bits
		XSP Channel 2 Size and Enable. 0x6000B	0x0E	
		Reserved	0000	
		XSP_RX_CH2_AP	1	XSP Channel 2 Active Phase
		XSP_RX_CH2_EN	1	XSP Channel 2 Enable
		XSP_RX_CH2_RES	10	XSP Channel 2 Size is 24 bits
19	Configure DSD Processor			
20	Configure DSD Volume	DSD Volume A. 0x70001	0x00	
		DSD_VOLUME_A	0x00	Channel A volume set to 0 dB
21	Configure DSD path Signal Control 1	DSD Processor Path Signal Control 1. 0x70002	0xEC	
		Reserved	1	
		DSD_VOL_BEQA	1	DSD Volume B equals DSD volume A
		DSD_SZC	1	Soft ramp control enabled
		Reserved	0	
		DSD_AMUTE	1	Mute occurs after 256 repeated 8-bit DSD mute patterns
		DSD_AMUTE_BEQA	1	Mute happens only when mute pattern is detected in both
		DSD_MUTE_A	0	channels
		DSD_MUTE_B	0	Function is disabled Function is disabled
22	Configure DSD Interface	DSD Interface Configuration. 0x70003	0x00	
		Reserved	0000 0	
		DSD_M/SB	0	DSD_M/SB is don't care
		DSD_PM_EN	0	Function is disabled
		DSD_PM_SEL	0	Function is disabled
23	Configure DSD path Signal Control 2	DSD Processor Path Signal Control 2. 0x70004	0x70	
		Reserved	0	
		DSD_PRC_SRC	11	Set source of DSD processor to XSP
		DSD_EN	1	Enable DSD playback
		Reserved	0	
		DSD_SPEED	0	Set DSD clock speed to 64•FS
		STA_DSD_DET	0	Static DSD detection disabled
		INV_DSD_DET	0	Invalid DSD detection disabled
24	Configure DSD path Signal Control 3	DSD Processor Path Signal Control 3. 0x70006	0xC0	
		DSD_ZERODB	1	DSD stream volume setting
		DSD_HPF_EN	1	Enable DSD HPF
		Reserved	0	
		SIGCTL_DSDEQPCM	0	Function is disabled
		DSD_INV_A	0	Function is disabled
		DSD_INV_B	0	Function is disabled
		DSD_SWAP_CHAN	0	Function is disabled
		DSD_COPY_CHAN	0	Function is disabled
25	Configure DAC Output for 1.732 Vrms			
26	Configure Class H Amplifier	Class H Control. 0xB0000	0x1E	
		Reserved	000	
		ADPT_PWR	111	Output Signal determines voltage level
		HV_EN	1	High Voltage Mode enabled
		EXT_VCPFILT	0	Using Internal VCPFILT source.
27	Set DAC output to full scale	Analog Output Control 1. 0x80000	0x30	
		Reserved	00	Set DAC output to Full Scale (1.732 Vrms)
		OUT_FS	11	
		Reserved	0000	

Example 5-12. DoP and PCM Mixing *(Cont.)*

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
28	Headphone Detect	HP Detect. 0xD0000	0xC4	
		HPDETECT_CTRL	11	HP Detect enabled
		HPDETECT_INV	0	HP detect input is not inverted
		HPDETECT_RISE_DBC_TIME	00	Tip Sense rising debounce time set to 0 ms
		HPDETECT_FALL_DBC_TIME	10	Tip sense falling debounce time set to 500 ms
		Reserved	0	
29	Enable Interrupts			
30	Read Interrupt Status 1 register (0xF0000), Interrupt Status 2 register (0xF0001) and Interrupt Status 5 register (0xF0004) to clear sticky bits			
31	Enable Headphone Detect Interrupts	Interrupt Mask 1. 0xF0010	0x99	
		DAC_OVFL_INT_MASK	1	DAC_OVFL_INT is don't care
		HPDETECT_PLUG_INT_MASK	0	Unmask HPDETECT_PLUG interrupt
		HPDETECT_UNPLUG_INT_MASK	0	Unmask HPDETECT_UNPLUG interrupt
		XTAL_READY_INT_MASK	1	XTAL_READY_INT is don't care
		XTAL_ERROR_INT_MASK	1	XTAL_ERROR_INT is don't care
		PLL_READY_INT_MASK	0	PLL_READY Interrupt is already unmasked
		PLL_ERROR_INT_MASK	0	PLL_ERROR Interrupt is already unmasked
		PDN_DONE_INT_MASK	1	PDN_DONE_INT is don't care
32	Enable XSP Interrupts	Interrupt Mask 2. 0xF0011	0x07	
		XSP_OVFL_INT_MASK	0	Enable XSP_OVFL interrupt
		XSP_ERROR_INT_MASK	0	Enable XSP_ERROR interrupt
		XSP_LATE_INT_MASK	0	Enable XSP_LATE interrupt
		XSP_EARLY_INT_MASK	0	Enable XSP_EARLY interrupt
		XSP_NOLRCK_INT_MASK	0	Enable XSP_NOLRCK interrupt
		Reserved	111	
33	Enable DSD and DoP Interrupts	Interrupt Mask 5. 0xF0014	0x01	
		DSD_STUCK_INT_MASK	0	Enable DSD_STUCK interrupt
		DSD_INVAL_A_INT_MASK	0	Enable DSD_INVAL_A interrupt
		DSD_INVAL_B_INT_MASK	0	Enable DSD_INVAL_B interrupt
		DSD_SILENCE_A_INT_MASK	0	Enable DSD_SILENCE_A interrupt
		DSD_SILENCE_B_INT_MASK	0	Enable DSD_SILENCE_B interrupt
		DSD_RATE_ERROR_INT_MASK	0	Enable DSD_RATE_ERROR interrupt
		DOP_MRK_DET_INT_MASK	0	Enable DOP_MRK_DET interrupt
		DOP_ON_INT_MASK	1	Disable DOP_ON interrupt
34	Set MCLK Source and Frequency	System Clocking Control. 0x10006	0x04	
		Reserved	0000 0	
		MCLK_INT	1	MCLK Frequency is set to 22.5792 MHz
		MCLK_SRC_SEL	00	MCLK Source is set to XTAL
35	Wait for at least 150 µs			
36	Enable XSP Clocks	Pad Interface Configuration. 0x1000D	0x01	
		Reserved	0000 00	
		XSP_3ST	0	ASP Interface status is don't care (set to default)
		ASP_3ST	1	Enable XSP serial clocks in master mode
37	Apply DSD Power-up Sequence in Ex. 5-6. Note that in Step 2 of Ex. 5-6, HH = 7F for DoP on XSP interface. Skip Step 1 of Ex. 5-6 (completed in Step 7 above).			
38	Enable ASP			
39	Set ASP sample rate	Serial Port Sample Rate. 0x1000B	0x01	
		Reserved	0000	
		ASP_SPRATE	0001	Set sample rate to 44.1 kHz
40	Set ASP sample bit size	Serial Port Sample Bit Size. 0x1000C	0x04	
		Reserved	0000	
		XSP_SPSIZE	01	
		ASP_SPSIZE	00	ASP sample bit size set to 32 bits
41	Set ASP Numerator	ASP Numerator 1. 0x40010	0x01	
		ASP_N_LSB	0x01	LSB of ASP sample rate fractional divide numerator
		ASP Numerator 2. 0x40011	0x00	
		ASP_N_MSB	0x00	MSB of ASP sample rate fractional divide numerator
42	Set ASP Denominator	ASP Denominator 1. 0x40012	0x08	
		ASP_M_LSB	0x08	LSB of ASP sample rate fractional divide denominator
		ASP Denominator 2. 0x40013	0x00	
		ASP_M_MSB	0x00	MSB of ASP sample rate fractional divide denominator
43	Set ASP LRCK high Time	ASP LRCK High Time 1. 0x40014	0x1F	
		ASP_LCHI_LSB	0x1F	LSB of ASP LRCK high time duration
		ASP LRCK High Time 2. 0x40015	0x00	
		ASP_LCHI_MSB	0x00	MSB of ASP LRCK high time duration
44	Set ASP LRCK period	ASP LRCK Period 1. 0x40016	0x3F	
		ASP_LCPR_LSB	0x3F	LSB of ASP LRCK period
		ASP LRCK Period 2. 0x40017	0x00	
		ASP_LCPR_MSB	0x00	MSB of ASP LRCK period

Example 5-12. DoP and PCM Mixing *(Cont.)*

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
45	Configure ASP Clock	ASP Clock Configuration. 0x40018	0x1C	
		Reserved	000	
		ASP_M/SB	1	Set ASP port to be Master
		ASP_SCPOL_OUT	1	Set output SCLK polarity
		ASP_SCPOL_IN	1	Input SCLK polarity is don't care
		ASP_LCPOL_OUT	0	Set Output LRCLK polarity
		ASP_LCPOL_IN	0	Input LRCLK polarity is don't care
46	Configure ASP Frame	ASP Frame Configuration. 0x40019	0x0A	
		Reserved	000	Configure ASP port to accept I²S input
		ASP_STP	0	
		ASP_5050	1	
		ASP_FSD	010	
47	Set ASP Channel Location	ASP Channel 1 Location. 0x50000	0x00	
		ASP_RX_CH1	0x00	ASP Channel 1 starts on SCLK0
		ASP Channel 2 Location. 0x50001	0x00	
		ASP_RX_CH2	0x00	ASP Channel 2 starts on SCLK0
48	Set ASP Channel Size and Enable	ASP Channel 1 Size and Enable. 0x5000A	0x07	
		Reserved	0000	
		ASP_RX_CH1_AP	0	ASP Channel 1 Active Phase
		ASP_RX_CH1_EN	1	ASP Channel 1 Enable
		ASP_RX_CH1_RES	11	ASP Channel 1 Size is 32 bits
		ASP Channel 2 Size and Enable. 0x5000B	0x0F	
		Reserved	0000	
		ASP_RX_CH2_AP	1	ASP Channel 2 Active Phase
		ASP_RX_CH2_EN	1	ASP Channel 2 Enable
		ASP_RX_CH2_RES	11	ASP Channel 2 Size is 32 bits
49	Setup PCM			
50	Configure PCM Filter	PCM Filter Option. 0x90000	0x02	
		FILTER_SLOW_FASTB	0	High Pass Filter is selected
		PHCOMP_LOWLATB	0	
		NOS	0	
		Reserved	0 00	
		HIGH_PASS	1	
		DEEMP_ON	0	
51	Set Volume for Channel B	PCM Volume B. 0x90001	0x0C	
		PCM_VOLUME_B	0x0C	Set volume to –6 dB
52	Set Volume for Channel A	PCM Volume A. 0x90002	0x0C	
		PCM_VOLUME_A	0x0C	Set volume to –6 dB
53	Configure PCM Path Signal Control	PCM Path Signal Control 1. 0x90003	0xEC	
		PCM_RAMP_DOWN	1	Soft ramp down of volume on filter change
		PCM_VOL_BEQA	1	Volume setting on both channels controlled by PCM_VOLUME_A
		PCM_SZC	10	Enable soft ramp
		PCM_AMUTE	1	Mute after reception of 8192 samples of 0 or -1.
		PCM_AMUTEBEQA	1	Mute only when AMUTE condition is detected on both channels
		PCM_MUTE_A	0	Function is disabled
		PCM_MUTE_B	0	Function is disabled
		PCM Path Signal Control 2. 0x90004	0x00	
		Reserved	0000	Disable all functions in this register
		PCM_INV_A	0	
		PCM_INV_B	0	
		PCM_SWAP_CHAN	0	
		PCM_COPY_CHAN	0	
54	Read interrupt status 2 register	Interrupt Status 2. 0xF0001		Clear sticky bits
55	Enable ASP Interrupts	Interrupt Mask 2. 0xF0011	0x07	
		ASP_OVFL_INT_MASK	0	Enable ASP_OVFL interrupt
		ASP_ERROR_INT_MASK	0	Enable ASP_ERROR interrupt
		ASP_LATE_INT_MASK	0	Enable ASP_LATE interrupt
		ASP_EARLY_INT_MASK	0	Enable ASP_EARLY interrupt
		ASP_NOLRCK_INT_MASK	0	Enable ASP_NOLRCK interrupt
		Reserved	111	
56	Enable ASP Clocks	Pad Interface Configuration. 0x1000D	0x00	
		Reserved	0000 00	
		XSP_3ST	0	Enable ASP serial clocks
		ASP_3ST	0	

Example 5-12. DoP and PCM Mixing *(Cont.)*

STEP	TASK	REGISTER/BIT FIELDS	VALUE	DESCRIPTION
57	Enable ASP	Power Down Control. 0x20000	0x24	
		PDN_XSP	0	
		PDN_ASP	0	Enable ASP
		PDN_DSDIF	1	
		PDN_HP	0	
		PDN_XTAL	0	
		PDN_PLL	1	
		PDN_CLKOUT	0	
		Reserved	0	
58	Enable PCM/DoP mix			
59	Configure DSD Volume	DSD Volume A. 0x70001	0x0C	
		DSD_VOLUME_A	0x0C	Channel A volume set to 0 dB
60	Prepare for PCM/DoP Mix operation	DSD and PCM Mixing Control. 0x70005	0x02	
		Reserved	0000 00	Enable PCM playback path for DoP Mixing
		MIX_PCM_PREP	1	
		MIX_PCM_DSD	0	
61	Wait for 6 ms			
62	Enable PCM/DoP mix	DSD and PCM Mixing Control. 0x70005	0x03	
		Reserved	0000 00	Enable PCM/DoP Mixing
		MIX_PCM_PREP	1	
		MIX_PCM_DSD	1	

6 Register Quick Reference

Notes: Default values are shown below the bit field names. The default values in all reserved bits must be preserved.

Table 6-1. Register Quick Reference

Address	Function	7	6	5	4	3	2	1	0
0x01 0000 p. 73	Device ID A and B (Read Only)	DEVIDA 0	1	0	0	DEVIDB 0	0	1	1
0x01 0001 p. 73	Device ID C and D (Read Only)	DEVIDC 1	0	0	1	DEVIDD 1	0	0	1
0x01 0004 p. 73	Revision ID (Read Only)	AREVID x	x	x	x	MTLREVID x	x	x	x
0x01 0005 p. 73	Subrevision ID (Read Only)	SUBREVID x	x	x	x	x	x	x	x
0x01 0006 p. 73	System Clocking Control	— 0	0	0	0	0	MCLK_INT 1	MCLK_SRC_SEL 1	0
0x01 0007– 0x01 000A	Reserved	— 0	0	0	0	0	0	0	0
0x01 000B p. 74	Serial Port Sample Rate	— 0	0	0	0	ASP_SPRATE 0	0	0	1
0x01 000C p. 74	Serial Port Sample Bit Size	— 0	0	0	0	XSP_SPSIZE 0	1	ASP_SPSIZE 0	1
0x01 000D p. 74	Pad Interface Configuration	— 0	0	0	0	0	0	XSP_3ST 1	ASP_3ST 1
0x01 000E– 0x01 FFFF	Reserved	— 0	0	0	0	0	0	0	0
0x02 0000 p. 75	Power Down Control	PDN_XSP 1	PDN_ASP 1	PDN_DSDIF 1	PDN_HP 1	PDN_XTAL 1	PDN_PLL 1	PDN_CLKOUT 1	— 0
0x02 0001– 0x02 0051	Reserved	— 0	0	0	0	0	0	0	0
0x02 0052 p. 75	Crystal Setting	— 0	0	0	0	0	XTAL_IBIAS 1	0	0
0x02 0053– 0x03 0000	Reserved	— 0	0	0	0	0	0	0	0
0x03 0001 p. 75	PLL Setting 1	— 0	0	0	0	0	0	0	PLL_START 0
0x03 0002 p. 76	PLL Setting 2	PLL_DIV_FRAC_0 0	0	0	0	0	0	0	0
0x03 0003 p. 76	PLL Setting 3	PLL_DIV_FRAC_1 0	0	0	0	0	0	0	0
0x03 0004 p. 76	PLL Setting 4	PLL_DIV_FRAC_2 0	0	0	0	0	0	0	0
0x03 0005 p. 76	PLL Setting 5	PLL_DIV_INT 0	1	0	0	0	0	0	0
0x03 0006– 0x03 0007	Reserved	— 0	0	0	0	0	0	0	0
0x03 0008 p. 76	PLL Setting 6	PLL_OUT_DIV 0	0	0	1	0	0	0	0
0x03 0009	Reserved	— 0	0	0	0	0	0	0	0
0x03 000A p. 76	PLL Setting 7	PLL_CAL_RATIO 1	0	0	0	0	0	0	0
0x03 000B– 0x03 001A	Reserved	— 0	0	0	0	0	0	0	0
0x03 001B p. 77	PLL Setting 8	— 0	0	0	0	— 0	— 0	PLL_MODE 1	— 1
0x03 001C– 0x04 0001	Reserved	— 0	0	0	0	0	0	0	0
0x04 0002 p. 77	PLL Setting 9	— 0	0	0	0	0	0	PLL_REF_PREDIV 1	0
0x04 0003	Reserved	— 0	0	0	0	0	0	0	0
0x04 0004 p. 77	CLKOUT Control	— 0	0	0	CLKOUT_DIV 0	0	0	CLKOUT_SEL 0	0

Table 6-1. Register Quick Reference *(Cont.)*

Address	Function	7	6	5	4	3	2	1	0
0x04 0005– 0x04 000F	Reserved	—							
		0	0	0	0	0	0	0	0
0x04 0010 p. 77	ASP Numerator 1	ASP_N_LSB							
		0	0	0	0	0	0	0	1
0x04 0011 p. 78	ASP Numerator 2	ASP_N_MSB							
		0	0	0	0	0	0	0	0
0x04 0012 p. 78	ASP Denominator 1	ASP_M_LSB							
		0	0	0	0	1	0	0	0
0x04 0013 p. 78	ASP Denominator 2	ASP_M_MSB							
		0	0	0	0	0	0	0	0
0x04 0014 p. 78	ASP LRCK High Time 1	ASP_LCHI_LSB							
		0	0	0	1	1	1	1	1
0x04 0015 p. 78	ASP LRCK High Time 2	ASP_LCHI_MSB							
		0	0	0	0	0	0	0	0
0x04 0016 p. 79	ASP LRCK Period 1	ASP_LCPR_LSB							
		0	0	1	1	1	1	1	1
0x04 0017 p. 79	ASP LRCK Period 2	ASP_LCPR_MSB							
		0	0	0	0	0	0	0	0
0x04 0018 p. 79	ASP Clock Configuration	—			ASP_M/SB	ASP_SCPOL_OUT	ASP_SCPOL_IN	ASP_LCPOL_OUT	ASP_LCPOL_IN
		0	0	0	0	1	1	0	0
0x04 0019 p. 79	ASP Frame Configuration	—			ASP_STP	ASP_5050	ASP_FSD		
		0	0	0	0	1	0	1	0
0x04 001A– 0x04 001F	Reserved	—							
		0	0	0	0	0	0	0	0
0x04 0020 p. 80	XSP Numerator 1	XSP_N_LSB							
		0	0	0	0	0	0	0	1
0x04 0021 p. 80	XSP Numerator 2	XSP_N_MSB							
		0	0	0	0	0	0	0	0
0x04 0022 p. 80	XSP Denominator 1	XSP_M_LSB							
		0	0	0	0	0	0	1	0
0x04 0023 p. 80	XSP Denominator 2	XSP_M_MSB							
		0	0	0	0	0	0	0	0
0x04 0024 p. 81	XSP LRCK High Time 1	XSP_LCHI_LSB							
		0	0	0	1	1	1	1	1
0x04 0025 p. 81	XSP LRCK High Time 2	XSP_LCHI_MSB							
		0	0	0	0	0	0	0	0
0x04 0026 p. 81	XSP LRCK Period 1	XSP_LCPR_LSB							
		0	0	1	1	1	1	1	1
0x04 0027 p. 81	XSP LRCK Period 2	XSP_LCPR_MSB							
		0	0	0	0	0	0	0	0
0x04 0028 p. 81	XSP Clock Configuration	—			XSP_M/SB	XSP_SCPOL_OUT	XSP_SCPOL_IN	XSP_LCPOL_OUT	XSP_LCPOL_IN
		0	0	0	0	1	1	0	0
0x04 0029 p. 82	XSP Frame Configuration	—			XSP_STP	XSP_5050	XSP_FSD		
		0	0	0	0	1	0	1	0
0x04 002A– 0x04 FFFF	Reserved	—							
		0	0	0	0	0	0	0	0
0x05 0000 p. 82	ASP Channel 1 Location	ASP_RX_CH1							
		0	0	0	0	0	0	0	0
0x05 0001 p. 82	ASP Channel 2 Location	ASP_RX_CH2							
		0	0	0	0	0	0	0	0
0x05 0002– 0x05 0009	Reserved	—							
		0	0	0	0	0	0	0	0
0x05 000A p. 82	ASP Channel 1 Size and Enable	—				ASP_RX_CH1_AP	ASP_RX_CH1_EN	ASP_RX_CH1_RES	
		0	0	0	0	0	1	1	0
0x05 000B p. 82	ASP Channel 2 Size and Enable	—				ASP_RX_CH2_AP	ASP_RX_CH2_EN	ASP_RX_CH2_RES	
		0	0	0	0	1	1	1	0
0x05 000C– 0x05 FFFF	Reserved	—							
		0	0	0	0	0	0	0	0
0x06 0000 p. 83	XSP Channel 1 Location	XSP_RX_CH1							
		0	0	0	0	0	0	0	0

Table 6-1. Register Quick Reference *(Cont.)*

Address	Function	7	6	5	4	3	2	1	0
0x06 0001 p. 83	XSP Channel 2 Location	XSP_RX_CH2							
		0	0	0	0	0	0	0	0
0x06 0002–0x06 0009	Reserved	—							
		0	0	0	0	0	0	0	0
0x06 000A p. 83	XSP Channel 1 Size and Enable	—				XSP_RX_CH1_AP	XSP_RX_CH1_EN	XSP_RX_CH1_RES	
		0	0	0	0	0	1	1	0
0x06 000B p. 83	XSP Channel 2 Size and Enable	—				XSP_RX_CH2_AP	XSP_RX_CH2_EN	XSP_RX_CH2_RES	
		0	0	0	0	1	1	1	0
0x06 000C–0x06 FFFF	Reserved	—							
		0	0	0	0	0	0	0	0
0x07 0000 p. 84	DSD Volume B	DSD_VOLUME_B							
		0	1	1	1	1	0	0	0
0x07 0001 p. 84	DSD Volume A	DSD_VOLUME_A							
		0	1	1	1	1	0	0	0
0x07 0002 p. 84	DSD Processor Path Signal Control 1	—	DSD_VOL_BEQA	DSD_SZC	—	DSD_AMUTE	DSD_AMUTE_BEQA	DSD_MUTE_A	DSD_MUTE_B
		1	0	1	0	1	0	0	0
0x07 0003 p. 85	DSD Interface Configuration	—					DSD_M_SB	DSD_PM_EN	DSD_PM_SEL
		0	0	0	0	0	0	0	0
0x07 0004 p. 85	DSD Processor Path Signal Control 2	—	DSD_PRC_SRC		DSD_EN	—	DSD_SPEED	STA_DSD_DET	INV_DSD_DET
		0	0	0	0	0	0	1	0
0x07 0005 p. 85	DSD and PCM Mixing Control	—						MIX_PCM_PREP	MIX_PCM_DSD
		0	0	0	0	0	0	0	0
0x07 0006 p. 86	DSD Processor Path Signal Control 3	DSD_ZERODB	DSD_HPF_EN	—	SIGCTL_DSDEQPCM	DSD_INV_A	DSD_INV_B	DSD_SWAP_CHAN	DSD_COPY_CHAN
		0	1	0	0	0	0	0	0
0x07 0008–0x07 FFFF	Reserved	—							
		0	0	0	0	0	0	0	0
0x08 0000 p. 86	Analog Output Control 1	—	—	OUT_FS		—	—		
		0	0	1	1	0	0	0	0
0x08 0001–0x08 FFFF	Reserved	—							
		0	0	0	0	0	0	0	0
0x09 0000 p. 87	PCM Filter Option	FILTER_SLOW_FASTB	PHCOMP_LOWLATB	NOS	—			HIGH_PASS	DEEMP_ON
		0	0	0	0	0	0	1	0
0x09 0001 p. 87	PCM Volume B	PCM_VOLUME_B							
		0	1	1	1	1	0	0	0
0x09 0002 p. 87	PCM Volume A	PCM_VOLUME_A							
		0	1	1	1	1	0	0	0
0x09 0003 p. 88	PCM Path Signal Control 1	PCM_RAMP_DOWN	PCM_VOL_BEQA	PCM_SZC		PCM_AMUTE	PCM_AMUTEBEQA	PCM_MUTE_A	PCM_MUTE_B
		1	0	1	0	1	0	0	0
0x09 0004 p. 88	PCM Path Signal Control 2	—				PCM_INV_A	PCM_INV_B	PCM_SWAP_CHAN	PCM_COPY_CHAN
		0	0	0	0	0	0	0	0
0x09 0005–0x0A FFFF	Reserved	—							
		0	0	0	0	0	0	0	0
0x0B 0000 p. 89	Class H Control	—			ADPT_PWR			HV_EN	EXT_VCPFILT
		0	0	0	1	1	1	1	0
0x0B 0001–0x0C FFFF	Reserved	—							
		0	0	0	0	0	0	0	0
0x0D 0000 p. 89	HP Detect	HPDETECT_CTRL		HPDETECT_INV	HPDETECT_RISE_DBC_TIME		HPDETECT_FALL_DBC_TIME		—
		0	0	0	0	0	1	0	0
0x0D 0001 p. 89	HP Status (Read Only)	—	HPDETECT_PLUG_DBC	HPDETECT_UNPLUG_DBC			—		
		0	0	0	0	0	0	0	0
0x0D 0002–0x0E 001A	Reserved	—							
		0	0	0	0	0	0	0	0
0x0E 001B–0x0E FFFF	Reserved	—							
		0	0	0	0	0	0	0	0

Table 6-1. Register Quick Reference *(Cont.)*

Address	Function	7	6	5	4	3	2	1	0
0x0F 0000	Interrupt Status 1 (Read Only)	DAC_OVFL_INT	HP_DETECT_PLUG_INT	HP_DETECT_UNPLUG_INT	XTAL_READY_INT	XTAL_ERROR_INT	PLL_READY_INT	PLL_ERROR_INT	PDN_DONE_INT
p. 90		0	0	0	0	0	0	0	0
0x0F 0001	Interrupt Status 2 (Read Only)	ASP_OVFL_INT	ASP_ERROR_INT	ASP_LATE_INT	ASP_EARLY_INT	ASP_NOLRCK_INT	—		
p. 90		0	0	0	0	0	0	0	0
0x0F 0002	Interrupt Status 3 (Read Only)	XSP_OVFL_INT	XSP_ERROR_INT	XSP_LATE_INT	XSP_EARLY_INT	XSP_NOLRCK_INT	—		
p. 91		0	0	0	0	0	0	0	0
0x0F 0003	Reserved	—							
		0	0	0	0	0	0	0	0
0x0F 0004	Interrupt Status 5 (Read Only)	DSD_STUCK_INT	DSD_INVAL_A_INT	DSD_INVAL_B_INT	DSD_SILENCE_A_INT	DSD_SILENCE_B_INT	DSD_RATE_ERROR_INT	DOP_MRK_DET_INT	DOP_ON_INT
p. 91		0	0	0	0	0	0	0	0
0x0F 0005–0x0F 000F	Reserved	—							
		0	0	0	0	0	0	0	0
0x0F 0010	Interrupt Mask 1	DAC_OVFL_INT_MASK	HP_DETECT_PLUG_INT_MASK	HP_DETECT_UNPLUG_INT_MASK	XTAL_READY_INT_MASK	XTAL_ERROR_INT_MASK	PLL_READY_INT_MASK	PLL_ERROR_INT_MASK	PDN_DONE_INT_MASK
p. 92		1	1	1	1	1	1	1	1
0x0F 0011	Interrupt Mask 2	ASP_OVFL_INT_MASK	ASP_ERROR_INT_MASK	ASP_LATE_INT_MASK	ASP_EARLY_INT_MASK	ASP_NOLRCK_INT_MASK	—		
p. 92		1	1	1	1	1	1	1	1
0x0F 0012	Interrupt Mask 3	XSP_OVFL_INT_MASK	XSP_ERROR_INT_MASK	XSP_LATE_INT_MASK	XSP_EARLY_INT_MASK	XSP_NOLRCK_INT_MASK	—		
p. 93		1	1	1	1	1	1	1	1
0x0F 0003	Reserved	—							
		0	0	0	0	0	0	0	0
0x0F 0014	Interrupt Mask 5	DSD_STUCK_INT_MASK	DSD_INVAL_A_INT_MASK	DSD_INVAL_B_INT_MASK	DSD_SILENCE_A_INT_MASK	DSD_SILENCE_B_INT_MASK	DSD_RATE_ERROR_INT_MASK	DOP_MRK_DET_INT_MASK	DOP_ON_INT_MASK
p. 94		1	1	1	1	1	1	1	1
0x0F 0015–0x0F FFFF	Reserved	—							
		0	0	0	0	0	0	0	0

7 Register Descriptions

All registers are read/write, except for the device's ID, revision, and status registers, which are read only. The following tables describe bit assignments. The default state of each bit after a power-up sequence or reset is listed in each bit description. All reserved bits must maintain their default state.

7.1 Global Registers

7.1.1 Device ID A and B

Address 0x10000

	7	6	5	4	3	2	1	0
R/O	DEVIDA				DEVIDB			
Default	0	1	0	0	0	0	1	1

Bits	Name	Description
7:4	DEVIDA	Part number first digit: 4
3:0	DEVIDB	Part number second digit: 3

7.1.2 Device ID C and D

Address 0x10001

	7	6	5	4	3	2	1	0
R/O	DEVIDC				DEVIDD			
Default	1	0	0	1	1	0	0	1

Bits	Name	Description
7:4	DEVIDC	Part number third digit: 9
3:0	DEVIDD	Part number fourth digit: 9

7.1.3 Revision ID

Address 0x10004

	7	6	5	4	3	2	1	0
R/O	AREVID				MTLREVID			
Default	x	x	x	x	x	x	x	x

Bits	Name	Description
7:4	AREVID	Alpha revision. AREVID and MTLREVID form the complete device revision ID (e.g., A0, B2).
3:0	MTLREVID	Metal revision. AREVID and MTLREVID form the complete device revision ID (e.g., A0, B2).

7.1.4 Subrevision ID

Address 0x10005

	7	6	5	4	3	2	1	0
R/O	SUBREVID							
Default	x	x	x	x	x	x	x	x

Bits	Name	Description
7:0	SUBREVID	Subrevision level.

7.1.5 System Clocking Control

Address 0x10006

	7	6	5	4	3	2	1	0
R/W	—					MCLK_INT	MCLK_SRC_SEL	
Default	0	0	0	0	0	1	1	0

Bits	Name	Description
7:3	—	Reserved
2	MCLK_INT	The frequency of internal MCLK. 0 Internal MCLK is expected to be 24.576 MHz 1 (Default) Internal MCLK is expected to be 22.5792 MHz

Bits	Name	Description
1:0	MCLK_SRC_SEL	Select the source of internal MCLK. 00 Direct MCLK/XTAL Mode 01 PLL Mode 10 (Default) RCO Mode 11 Reserved

7.1.6 Serial Port Sample Rate

Address 0x1000B

R/W	7	6	5	4	3	2	1	0
	—				ASP_SPRATE			
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:4	—	Reserved
3:0	ASP_SPRATE	ASP sample rate. This register must be programmed for both Master Mode and Slave Mode operation. 0000 32 kHz 0001 (Default) 44.1 kHz 0010 48 kHz 0011 88.2 kHz 0100 96 kHz 0101 176.4 kHz 0110 192 kHz 0111 352.8 kHz 1000 384 kHz 1001–1111 Reserved

7.1.7 Serial Port Sample Bit Size

Address 0x1000C

R/W	7	6	5	4	3	2	1	0
	—				XSP_SPSIZE		ASP_SPSIZE	
Default	0	0	0	0	0	1	0	1

Bits	Name	Description
7:4	—	Reserved
3:2	XSP_SPSIZE	XSP sample bit size. 00 32 bits 01 (Default) 24 bits 10–11 Reserved
1:0	ASP_SPSIZE	ASP sample bit size. 00 32 bits 01 (Default) 24 bits 10 16 bits 11 8 bits

7.1.8 Pad Interface Configuration

Address 0x1000D

R/W	7	6	5	4	3	2	1	0
	—						XSP_3ST	ASP_3ST
Default	0	0	0	0	0	0	1	1

Bits	Name	Description
7:2	—	Reserved
1	XSP_3ST	Determines the state of the XSP clock drivers when in Master Mode. When in Slave Mode, the serial port clocks are inputs, whose function is not affected by this bit. Before setting an xSP_3ST bit, the associated serial port must be powered down and not powered up until the xSP_3ST bit is cleared. 0 When in Master Mode, serial port clocks are active. 1 (Default) When in Master Mode, serial port clocks are Hi-Z.
0	ASP_3ST	Determines the state of the ASP clock drivers when in Master Mode. When in Slave Mode, the serial port clock pins are inputs, whose function is not affected by this bit. Before setting an xSP_3ST bit, the associated serial port must be powered down and not powered up until the xSP_3ST bit is cleared. 0 When in Master Mode, serial port clocks are active. 1 (Default) When in Master Mode, serial port clocks are Hi-Z.

7.1.9 Power Down Control

Address 0x20000

R/W	7	6	5	4	3	2	1	0
	PDN_XSP	PDN_ASP	PDN_DSDIF	PDN_HP	PDN_XTAL	PDN_PLL	PDN_CLKOUT	—
Default	1	1	1	1	1	1	1	0

Bits	Name	Description
7	PDN_XSP	XSP input path power control. Configures XSP SDIN path power state. 0 Powered up. 1 (Default) Powered down.
6	PDN_ASP	ASP input path power control. Configures ASP SDIN path power state. 0 Powered up. 1 (Default) Powered down.
5	PDN_DSDIF	DSD interface power control. Sets the power state of the DSD interface block. 0 Powered up. 1 (Default) Powered down.
4	PDN_HP	Power down AOUTx. 0 Powered up. The DACx are powered up. 1 (Default) Powered down. The DACx are powered down. When this bit is set, the audio outputs are soft ramped to mute.
3	PDN_XTAL	Power down crystal oscillator. 0 Powered up. The XTAL driver is powered up to start generating MCLK. 1 (Default) Powered down. The XTAL driver is powered down.
2	PDN_PLL	PLL output power control. Sets the power state of the PLL block. 0 Powered up. 1 (Default) Powered down. PLL block is powered down.
1	PDN_CLKOUT	CLKOUT output power control. Sets the power state of the CLOCKOUT output. 0 Powered up 1 (Default) Powered down. CLKOUT are driven low.
0	—	Reserved

7.1.10 Crystal Setting

Address 0x20052

R/W	7	6	5	4	3	2	1	0
	—					XTAL_IBIAS		
Default	0	0	0	0	0	1	0	0

Bits	Name	Description
7:3	—	Reserved
2:0	XTAL_IBIAS	Crystal bias current strength. 010 15.0 µA 100 (Default) 12.5 µA 110 7.5 µA Others Reserved

7.2 PLL Registers

7.2.1 PLL Setting 1

Address 0x30001

R/W	7	6	5	4	3	2	1	0
	—							PLL_START
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:1	—	Reserved
0	PLL_START	PLL start bit. Enable PLL output after it has been properly configured. 0 (Default) PLL is not started 1 PLL is started

7.2.2 PLL Setting 2

Address 0x30002

	7	6	5	4	3	2	1	0
R/W	PLL_DIV_FRAC_0							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PLL_DIV_FRAC_0	PLL fractional portion of divide ratio LSB. There are 3 bytes of PLL feedback divider fraction portion and this is LSB byte; e.g., 0xFF means ($2^{-17} + 2^{-18} + \ldots + 2^{-24}$). 0000 0000 (Default)

7.2.3 PLL Setting 3

Address 0x30003

	7	6	5	4	3	2	1	0
R/W	PLL_DIV_FRAC_1							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PLL_DIV_FRAC_1	PLL fractional portion of divide ratio middle byte; e.g., 0xFF means ($2^{-9} + 2^{-10} + \ldots + 2^{-16}$). 0000 0000 (Default)

7.2.4 PLL Setting 4

Address 0x30004

	7	6	5	4	3	2	1	0
R/W	PLL_DIV_FRAC_2							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PLL_DIV_FRAC_2	PLL fractional portion of divide ratio MSB; e.g., 0xFF means ($2^{-1} + 2^{-2} + \ldots + 2^{-8}$). 0000 0000 (Default)

7.2.5 PLL Setting 5

Address 0x30005

	7	6	5	4	3	2	1	0
R/W	PLL_DIV_INT							
Default	0	1	0	0	0	0	0	0

Bits	Name	Description
7:0	PLL_DIV_INT	PLL integer portion of divide ratio. Integer portion of PLL feedback divider. 0100 0000 (Default)

7.2.6 PLL Setting 6

Address 0x30008

	7	6	5	4	3	2	1	0
R/W	PLL_OUT_DIV							
Default	0	0	0	1	0	0	0	0

Bits	Name	Description
7:0	PLL_OUT_DIV	Final PLL clock output divide value. 0001 0000 (Default)

7.2.7 PLL Setting 7

Address 0x3000A

	7	6	5	4	3	2	1	0
R/W	PLL_CAL_RATIO							
Default	1	0	0	0	0	0	0	0

Bits	Name	Description
7:0	PLL_CAL_RATIO	PLL calibration ratio. See Section 4.6.2 for configuration details. Target value for PLL VCO calibration. 1000 0000 (Default)

7.2.8 PLL Setting 8

Address 0x3001B

R/W	7	6	5	4	3	2	1	0
	—						PLL_MODE	—
Default	0	0	0	1	0	0	1	1

Bits	Name	Description
7:2	—	Reserved
1	PLL_MODE	500/512 factor used in PLL frequency calculation equation, Eq. 4-1. 0 No bypass 1 (Default) Bypass
0	—	Reserved

7.2.9 PLL Setting 9

Address 0x40002

R/W	7	6	5	4	3	2	1	0
	—						PLL_REF_PREDIV	
Default	0	0	0	0	0	0	1	0

Bits	Name	Description
7:2	—	Reserved
1:0	PLL_REF_PREDIV	PLL reference divide select. 00 Divide by 1 01 Divide by 2 10 (Default) Divide by 4 11 Divide by 8

7.3 ASP and XSP Registers

7.3.1 CLKOUT Control

Address 0x40004

R/W	7	6	5	4	3	2	1	0
	—			CLKOUT_DIV			CLKOUT_SEL	
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:5	—	Reserved
4:2	CLKOUT_DIV	Divider setting on internal MCLK path to CLKOUT. 000 (Default) Divide by 2 001 Divide by 3 010 Divide by 4 011 Divide by 8 100–111 Reserved
1:0	CLKOUT_SEL	Select the source of CLKOUT. 00 (Default) XTAL/MCLK path 01 PLL output path 10–11 Reserved

7.3.2 ASP Numerator 1

Address 0x40010

R/W	7	6	5	4	3	2	1	0
	ASP_N_LSB							
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:0	ASP_N_LSB	The value in this register cannot be changed while the serial port is powered up. ASP sample rate fractional divide numerator LSB. Along with ASP_M_MSB/LSB, selects the fractional divide value for setting the SCLK frequency. (Default) ASP_N = 1

7.3.3 ASP Numerator 2

Address 0x40011

	7	6	5	4	3	2	1	0
R/W	ASP_N_MSB							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	ASP_N_MSB	The value in this register cannot be changed while the serial port is powered up. ASP sample rate fractional divide numerator MSB. Along with ASP_M_MSB/LSB, selects the fractional divide value for setting the SCLK frequency. (Default) ASP_N = 1

7.3.4 ASP Denominator 1

Address 0x40012

	7	6	5	4	3	2	1	0
R/W	ASP_M_LSB							
Default	0	0	0	0	1	0	0	0

Bits	Name	Description
7:0	ASP_M_LSB	The value in this register cannot be changed while the serial port is powered up. ASP sample rate fractional divide denominator LSB. Along with ASP_N_MSB/LSB, selects the fractional divide value for setting the SCLK frequency. (Default) ASP_M = 8

7.3.5 ASP Denominator 2

Address 0x40013

	7	6	5	4	3	2	1	0
R/W	ASP_M_MSB							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	ASP_M_MSB	The value in this register cannot be changed while the serial port is powered up. ASP sample rate fractional divide denominator LSB. Along with ASP_N_MSB/LSB, selects the fractional divide value for setting the SCLK frequency. (Default) ASP_M = 8

7.3.6 ASP LRCK High Time 1

Address 0x40014

	7	6	5	4	3	2	1	0
R/W	ASP_LCHI_LSB							
Default	0	0	0	1	1	1	1	1

Bits	Name	Description
7:0	ASP_LCHI_LSB	The value in this register cannot be changed while the serial port is powered up. ASP LRCK high duration, in units of ASP_SCLK periods stored in ASP_LCHI_MSB/LSB. This value must be less than ASP_LCPR. (Default) ASP_LCHI = 31

7.3.7 ASP LRCK High Time 2

Address 0x40015

	7	6	5	4	3	2	1	0
R/W	ASP_LCHI_MSB							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	ASP_LCHI_MSB	The value in this register cannot be changed while the serial port is powered up. ASP LRCK high duration, in units of ASP_SCLK periods stored in ASP_LCHI_MSB/LSB. This value must be less than ASP_LCPR. (Default) ASP_LCHI = 31

7.3.8 ASP LRCK Period 1

Address 0x40016

	7	6	5	4	3	2	1	0
R/W	ASP_LCPR_LSB							
Default	0	0	1	1	1	1	1	1

Bits	Name	Description
7:0	ASP_LCPR_LSB	The value in this register cannot be changed while the serial port is powered up. ASP LRCK period, in units of ASP_SCLK periods stored in ASP_LCPR_MSB/LSB. (Default) ASP_LCPR = 63

7.3.9 ASP LRCK Period 2

Address 0x40017

	7	6	5	4	3	2	1	0
R/W	ASP_LCPR_MSB							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	ASP_LCPR_MSB	The value in this register cannot be changed while the serial port is powered up. ASP LRCK period, in units of ASP_SCLK periods stored in ASP_LCPR_MSB/LSB. (Default) ASP_LCPR = 63

7.3.10 ASP Clock Configuration

Address 0x40018

	7	6	5	4	3	2	1	0
R/W	—			ASP_M/SB	ASP_SCPOL_OUT	ASP_SCPOL_IN	ASP_LCPOL_OUT	ASP_LCPOL_IN
Default	0	0	0	0	1	1	0	0

Bits	Name	Description
7:5	—	Reserved
4	ASP_M/SB	ASP port master or slave configuration. 0 (Default) Slave Mode (input) 1 Master Mode (output)
3	ASP_SCPOL_OUT	ASP SCLK output drive polarity. 0 Normal 1 (Default) Inverted
2	ASP_SCPOL_IN	ASP SCLK input polarity (pad to logic). 0 Normal 1 (Default) Inverted
1	ASP_LCPOL_OUT	ASP LRCK output drive polarity. 0 (Default) Normal 1 Inverted
0	ASP_LCPOL_IN	ASP LRCK input polarity (pad to logic). 0 (Default) Normal 1 Inverted

7.3.11 ASP Frame Configuration

Address 0x40019

	7	6	5	4	3	2	1	0
R/W	—			ASP_STP	ASP_5050	ASP_FSD		
Default	0	0	0	0	1	0	1	0

Bits	Name	Description
7:5	—	Reserved
4	ASP_STP	ASP start phase. Controls which LRCK/FSYNC phase starts a frame. 0 (Default) The frame begins when LRCK/FSYNC transitions from high to low 1 The frame begins when LRCK/FSYNC transitions from low to high
3	ASP_5050	ASP LRCK fixed 50/50 duty cycle. 0 Programmable duty cycle per ASP_LCHI and ASP_LCPR. 1 (Default) Fixed 50% duty cycle

Bits	Name	Description
2:0	ASP_FSD	ASP frame start delay (units of ASP_SCLK periods). 000 0 delay 001 0.5 delay 010 (Default) 1.0 delay ... 101 2.5 delay 110–111 Reserved

7.3.12 XSP Numerator 1

Address 0x40020

R/W	7	6	5	4	3	2	1	0
	XSP_N_LSB							
Default	0	0	0	0	0	0	0	1

Bits	Name	Description
7:0	XSP_N_LSB	The value in this register cannot be changed while the serial port is powered up. XSP sample rate fractional divide numerator LSB. Along with XSP_M_MSB/LSB, selects the fractional divide value for setting the SCLK frequency. (Default) XSP_N = 1

7.3.13 XSP Numerator 2

Address 0x40021

R/W	7	6	5	4	3	2	1	0
	XSP_N_MSB							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	XSP_N_MSB	The value in this register cannot be changed while the serial port is powered up. XSP sample rate fractional divide numerator MSB. Along with XSP_M_MSB/LSB, selects the fractional divide value for setting the SCLK frequency. (Default) XSP_N = 1

7.3.14 XSP Denominator 1

Address 0x40022

R/W	7	6	5	4	3	2	1	0
	XSP_M_LSB							
Default	0	0	0	0	0	0	1	0

Bits	Name	Description
7:0	XSP_M_LSB	The value in this register cannot be changed while the serial port is powered up. XSP sample rate fractional divide denominator LSB. Along with XSP_N_MSB/LSB, selects the fractional divide value for setting the SCLK frequency. (Default) XSP_M = 2

7.3.15 XSP Denominator 2

Address 0x40023

R/W	7	6	5	4	3	2	1	0
	XSP_M_MSB							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	XSP_M_MSB	The value in this register cannot be changed while the serial port is powered up. XSP sample rate fractional divide denominator MSB. Along with XSP_N_MSB/LSB, selects the fractional divide value for setting the SCLK frequency. (Default) XSP_M = 2

7.3.16 XSP LRCK High Time 1

Address 0x40024

	7	6	5	4	3	2	1	0
R/W	XSP_LCHI_LSB							
Default	0	0	0	1	1	1	1	1

Bits	Name	Description
7:0	XSP_LCHI_LSB	The value in this register cannot be changed while the serial port is powered up. XSP LRCK high duration, in units of XSP_SCLK periods stored in XSP_LCHI_LSB/MSB. This value must be less than XSP_LCPR. (Default) XSP_LCHI = 31

7.3.17 XSP LRCK High Time 2

Address 0x40025

	7	6	5	4	3	2	1	0
R/W	XSP_LCHI_MSB							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	XSP_LCHI_MSB	The value in this register cannot be changed while the serial port is powered up. XSP LRCK high duration, in units of XSP_SCLK periods stored in XSP_LCHI_LSB/MSB. This value must be less than XSP_LCPR. (Default) XSP_LCHI = 31

7.3.18 XSP LRCK Period 1

Address 0x40026

	7	6	5	4	3	2	1	0
R/W	XSP_LCPR_LSB							
Default	0	0	1	1	1	1	1	1

Bits	Name	Description
7:0	XSP_LCPR_LSB	The value in this register cannot be changed while the serial port is powered up. XSP LRCK period, in units of XSP_SCLK periods stored in XSP_LCPR_LSB/MSB. (Default) XSP_LCPR = 63

7.3.19 XSP LRCK Period 2

Address 0x40027

	7	6	5	4	3	2	1	0
R/W	XSP_LCPR_MSB							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	XSP_LCPR_MSB	The value in this register cannot be changed while the serial port is powered up. XSP LRCK period, in units of XSP_SCLK periods stored in XSP_LCPR_LSB/MSB. (Default) XSP_LCPR = 63

7.3.20 XSP Clock Configuration

Address 0x40028

	7	6	5	4	3	2	1	0
R/W	—			XSP_M/SB	XSP_SCPOL_OUT	XSP_SCPOL_IN	XSP_LCPOL_OUT	XSP_LCPOL_IN
Default	0	0	0	0	1	1	0	0

Bits	Name	Description
7:5	—	Reserved
4	XSP_M/SB	XSP port master or slave configuration. 0 (Default) Slave Mode (input) 1 Master Mode (output)
3	XSP_SCPOL_OUT	XSP SCLK output drive polarity. 0 Normal 1 (Default) Inverted

Bits	Name	Description
2	XSP_SCPOL_IN	XSP SCLK input polarity (pad to logic). 0 Normal 1 (Default) Inverted
1	XSP_LCPOL_OUT	XSP LRCK output drive polarity. 0 (Default) Normal 1 Inverted
0	XSP_LCPOL_IN	XSP LRCK input polarity (pad to logic). 0 (Default) Normal 1 Inverted

7.3.21 XSP Frame Configuration

Address 0x40029

	7	6	5	4	3	2	1	0
R/W	—			XSP_STP	XSP_5050	XSP_FSD		
Default	0	0	0	0	1	0	1	0

Bits	Name	Description
7:5	—	Reserved
4	XSP_STP	XSP start phase. Controls which LRCK/FSYNC phase starts a frame. 0 (Default) The frame begins when LRCK/FSYNC transitions from high to low 1 The frame begins when LRCK/FSYNC transitions from low to high
3	XSP_5050	XSP LRCK fixed 50/50 duty cycle. 0 Programmable duty cycle per XSP_LCHI and XSP_LCPR 1 (Default) Fixed 50% duty cycle
2:0	XSP_FSD	XSP frame start delay (units of XSP_SCLK periods). 000 0 delay 001 0.5 delay 010 (Default) 1.0 delay ... 101 2.5 delay 110–111 Reserved

7.3.22 ASP Channel 1 and 2 Location

Address 0x50000, 0x50001

	7	6	5	4	3	2	1	0
R/W	ASP_RX_CH1							
	ASP_RX_CH2							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	ASP_RX_CHn	ASP Rx channel *n* location. Sets the location in ASP_SCLK periods of the ASP Rx channel *n* from the start of the TDM frame. 0x00 Start on SCLK 0 ... 0xFF Start on SCLK 255 Defaults are 0x00.

7.3.23 ASP Channel 1 Size and Enable

Address 0x5000A

	7	6	5	4	3	2	1	0
R/W	—				ASP_RX_CH1_AP	ASP_RX_CH1_EN	ASP_RX_CH1_RES	
Default	0	0	0	0	0	1	1	0

7.3.24 ASP Channel 2 Size and Enable

Address 0x5000B

	7	6	5	4	3	2	1	0
R/W	—				ASP_RX_CH2_AP	ASP_RX_CH2_EN	ASP_RX_CH2_RES	
Default	0	0	0	0	1	1	1	0

Bits	Name	Description
7:4	—	Reserved

Bits	Name	Description
3	ASP_RX_CH*n*_AP	ASP RX channel *n* active phase. Valid only in 50/50 mode (ASP_5050 = 1). 0 (Default when *n* = 1) In 50/50 mode, channel data is input when LRCK/FSYNC is low 1 (Default when *n* = 2) In 50/50 mode, channel data is input when LRCK/FSYNC is high
2	ASP_RX_CH*n*_EN	ASP RX channel *n* enable. Configures the state of the data for the ASP on channel *n*. The same rule applies to CHx_EN. 0 (Default) Input channel data is not propagated to the internal data path 1 Input channel data is propagated to the internal data path
1:0	ASP_RX_CH*n*_RES	ASP RX channel *n* size (in bits). Sets the output resolution of the ASP RX channel *n* samples. 00 8 bits per sample 01 16 bits per sample 10 (Default) 24 bits per sample 11 32 bits per sample

7.3.25 XSP Channel 1 and 2 Location

Address 0x60000, 0x60001

R/W	7	6	5	4	3	2	1	0
	XSP_RX_CH1							
	XSP_RX_CH2							
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:0	XSP_RX_CH*n*	XSP Rx channel *n* location. Sets the location in XSP_SCLK periods of the XSP Rx channel *n* from the start of the TDM frame. 0x00 Start on SCLK 0 ... 0xFF Start on SCLK 255 Defaults are 0x00.

7.3.26 XSP Channel 1 Size and Enable

Address 0x6000A

R/W	7	6	5	4	3	2	1	0
	—				XSP_RX_CH1_AP	XSP_RX_CH1_EN	XSP_RX_CH1_RES	
Default	0	0	0	0	0	1	1	0

7.3.27 XSP Channel 2 Size and Enable

Address 0x6000B

R/W	7	6	5	4	3	2	1	1
	—				XSP_RX_CH2_AP	XSP_RX_CH2_EN	XSP_RX_CH2_RES	
Default	0	0	0	0	1	1	1	0

Bits	Name	Description
7:4	—	Reserved
3	XSP_RX_CH*n*_AP	XSP Rx channel *n* active phase. Valid only in 50/50 mode (XSP_5050 = 1). 0 (Default when *n* = 1) In 50/50 mode, channel data is input when LRCK/FSYNC is low 1 (Default when *n* = 2) In 50/50 mode, channel data is input when LRCK/FSYNC is high
2	XSP_RX_CH*n*_EN	XSP Rx channel *n* enable. Configures the state of the data for the XSP on channel *n*. The same rule applies to CHx_EN. 0 Input channel data is not propagated to the internal data path 1 (Default) Input channel data is propagated to the internal data path
1:0	XSP_RX_CH*n*_RES	XSP Rx channel *n* size (in bits). Sets the output resolution of the XSP Rx channel *n* samples. 00 8 bits per sample 01 16 bits per sample 10 (Default) 24 bits per sample 11 32 bits per sample

7.4 DSD Registers

7.4.1 DSD Volume B

Address 0x70000

R/W	7	6	5	4	3	2	1	0
	DSD_VOLUME_B							
Default	0	1	1	1	1	0	0	0

Bits	Name	Description
7:0	DSD_ VOLUME_B	Digital volume control registers for DSD processor channel B. It allows independent control of the signal level in 1/2 dB increments from 0 dB. Volume settings are decoded as shown below. The volume changes are dictated by the DSD_ SZC bit. The same condition applies to DSD_VOLUME_A setting. 0000 0000 0 dB 0000 0001 –0.5 dB ... 01111000 –60 dB (Default) ... 1111 1110 –127 dB 1111 1111 Digital mute

7.4.2 DSD Volume A

Address 0x70001

R/W	7	6	5	4	3	2	1	0
	DSD_VOLUME_A							
Default	0	1	1	1	1	0	0	0

Bits	Name	Description
7:0	DSD_ VOLUME_A	Digital volume control registers for channel A. See DSD_VOLUME_B for description.

7.4.3 DSD Processor Path Signal Control 1

Address 0x70002

R/W	7	6	5	4	3	2	1	0
	—	DSD_VOL_ BEQA	DSD_SZC	—	DSD_AMUTE	DSD_AMUTE_ BEQA	DSD_MUTE_A	DSD_MUTE_B
Default	1	0	1	0	1	0	0	0

Bits	Name	Description
7	—	Reserved
6	DSD_VOL_ BEQA	DSD_VOLUME_B equals DSD_VOLUME_A. 0 (Default) Volume setting of both channels in DSD processor are controlled independently 1 Volume setting of both channels are controlled by DSD_VOLUME_A. DSD_VOLUME_B is ignored
5	DSD_SZC	Soft ramp control. 0 Immediate change 1 (Default) Soft ramp
4	—	Reserved
3	DSD_AMUTE	DSD auto mute. 0 Function disabled 1 (Default) Mute occurs after reception of 256 repeated 8-bit DSD mute patterns. A single bit not fitting the repeated pattern releases the mute. Detection and muting is done independently for each channel.
2	DSD_ AMUTE_ BEQA	DSD Processor Auto mute channel B equals channel A. 0 (Default) Function disabled 1 Only mute when both channels AMUTE conditions are detected
1	DSD_MUTE_ A	DSD Processor Channel A mute. 0 (Default) Function is disabled 1 Channel output is muted. Muting function is affected by the DSD_SZC bit
0	DSD_MUTE_ B	DSD Processor Channel B mute. 0 (Default) Function is disabled. 1 Channel output is muted. Muting function is affected by the DSD_SZC bit.

7.4.4 DSD Interface Configuration

Address 0x70003

R/W	7	6	5	4	3	2	1	0
	—					DSD_M/SB	DSD_PM_EN	DSD_PM_SEL
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:3	—	Reserved
2	DSD_M/SB	DSD clock master or Slave Mode. 0 (Default) Slave Mode 1 Master Mode
1	DSD_PM_EN	DSD phase modulation mode. Can only be used when DSD_SPEED = 0 (64•Fs). 0 (Default) this function is disabled (DSD normal mode) 1 DSD phase modulation input mode is enabled, and the DSD_PM_SEL bit must be set accordingly.
0	DSD_PM_SEL	DSD phase modulation mode select. 0 (Default) The 128•Fs (BCKA) clock must be input to DSD_SCLK for phase modulation mode. 1 The 64•Fs (BCKD) clock must be input to DSD_SCLK for phase modulation mode.

7.4.5 DSD Processor Path Signal Control 2

Address 0x70004

R/W	7	6	5	4	3	2	1	0
	—	DSD_PRC_SRC		DSD_EN	—	DSD_SPEED	STA_DSD_DET	INV_DSD_DET
Default	0	0	0	0	0	0	1	0

Bits	Name	Description
7	—	Reserved
6:5	DSD_PRC_SRC	Select the source for DSD processor. 00 (Default) DSD interface 01 Reserved 10 ASP 11 XSP
4	DSD_EN	Enable DSD playback. 0 (Default) Function disabled 1 DSD playback is enabled
3	—	Reserved
2	DSD_SPEED	Setup DSD clock speed. 0 (Default) 64•Fs 1 128•Fs
1	STA_DSD_DET	Static DSD detection. 0 Function disabled 1 (Default) Static DSD detection is enabled. The DSD processor checks for 28 consecutive zeros or ones and, if detected, sets the DSD_STUCK_INT interrupt status bit and mutes the output until the static condition is cleared.
0	INV_DSD_DET	Invalid DSD detection. 0 (Default) Function disabled 1 Invalid DSD detection is enabled. The DSD processor checks for 25 out of 28 bits of the same value and, if detected, sets the DSD_INVAL_A_INT and/or DSD_INVAL_B_INT interrupt status bits.

7.4.6 DSD and PCM Mixing Control

Address 0x70005

R/W	7	6	5	4	3	2	1	0
	—						MIX_PCM_PREP	MIX_PCM_DSD
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:2	—	Reserved
1	MIX_PCM_PREP	Enable PCM playback path for PCM and DSD mixing. This bit must be set prior to setting MIX_PCM_DSD. Disable this bit after disabling MIX_PCM_DSD. This mode requires DSD_EN to be enabled and DSD_PRC_SRC set to receive DSD through either the DSD interface or XSP. 0 (Default) Function disabled 1 Enable PCM playback path for PCM and DSD mixing

Bits	Name	Description
0	MIX_PCM_ DSD	Enable PCM stream mixing into DSD stream. This bit must be set only after MIX_PCM_PREP is enabled. Disable this bit prior to disabling MIX_PCM_PREP bit. This mode requires DSD_EN to be enabled and DSD_PRC_SRC set to receive DSD through either the DSD interface or XSP. 0 (Default) Function disabled 1 Enable PCM stream mixing into the DSD stream

7.4.7 DSD Processor Path Signal Control 3

Address 0x70006

R/W	7	6	5	4	3	2	1	0
	DSD_ZERODB	DSD_HPF_EN	—	SIGCTL_ DSDEQPCM	DSD_INV_A	DSD_INV_B	DSD_SWAP_ CHAN	DSD_COPY_ CHAN
Default	0	1	0	0	0	0	0	0

Bits	Name	Description
7	DSD_ ZERODB	Setting on DSD stream volume to match PCM stream volume. 0 (Default) The SACD +3.1-dB level (71% modulation index) matches PCM 0 dB full scale. 1 The SACD 0-dB reference level (50% modulation index) matches PCM 0 dB full scale.
6	DSD_HPF_EN	Enable the high pass filter in the DSD processor. 0 HPF disabled 1 (Default) Enable HPF in the DSD processor
5	—	Reserved
4	SIGCTL_ DSDEQPCM	Enable DSD signal path control register bits to be controlled by PCM setting. DSD setting is ignored. Register bits affected are the following: DSD_VOL_BEQA, DSD_SZC, DSD_AMUTE, DSD_AMUTE_BEQA, DSD_MUTE_A, DSD_MUTE_B, DSD_INV_A, DSD_INV_B, DSD_SWAP_CHAN, DSD_COPY_CHAN After set, each DSD_x register bit is equal to setting of PCM_x register bit. 0 (Default) Function is disabled 1 Function is enabled
3	DSD_INV_A	DSD Processor Channel A signal invert. 0 (Default) Function is disabled 1 Signal polarity of channel A is inverted
2	DSD_INV_B	DSD Processor Channel B signal invert 0 (Default) the function is disabled 1 Signal polarity of channel B is inverted
1	DSD_SWAP_ CHAN	Swap channels A and B at the input. This bit takes effect before DSD_COPY_CHAN and DSD_INV_x. 0 (Default) Function disabled 1 Enable channel A and B swapping
0	DSD_COPY_ CHAN	Copy channel A to channel B. This bit takes effect after DSD_SWAP_CHAN, but before DSD_INV_x. 0 (Default) Function disabled 1 Enable copy A to B function

7.5 Analog Output and PCM Registers

7.5.1 Analog Output Control 1

Address 0x80000

R/W	7	6	5	4	3	2	1	0
	—	—	OUT_FS		—	—		
Default	0	0	1	1	0	0	0	0

Bits	Name	Description
7:6	—	Reserved
5:4	OUT_FS	Output full scale setting. This setting must only be updated when PDN_HP is set. 00 Reserved 01 Reserved 10 1.41 V 11 (Default) 1.73 V
3	—	Reserved
2:0	—	Reserved

7.5.2 PCM Filter Option

Address 0x90000

R/W	7	6	5	4	3	2	1	0
	FILTER_SLOW_FASTB	PHCOMP_LOWLATB	NOS	—			HIGH_PASS	DEEMP_ON
Default	0	0	0	0	0	0	1	0

Bits	Name	Description
7	FILTER_SLOW_FASTB	Fast and slow filter selection. 0 (Default) Fast filter is selected. 1 Slow filter is selected.
6	PHCOMP_LOWLATB	Low-latency and phase-compensated filter selection 0 (Default) Low-latency is selected. 1 Phase-compensated filter is selected.
5	NOS	Nonoversampling emulation mode on. When enabled, FILTER_SLOW_FASTB and PHCOMP_LOWLATB are ignored. 0 (Default) NOS emulation mode is off. 1 NOS emulation mode is on.
4:2	—	Reserved
1	HIGH_PASS	High-pass filter enable. 0 High-pass filter is disabled. 1 (Default) High-pass filter is selected.
0	DEEMP_ON	Deemphasis filter on. 0 (Default) Deemphasis for 44.1 kHz is disabled. 1 Deemphasis for 44.1 kHz is enabled.

7.5.3 PCM Volume B

Address 0x90001

R/W	7	6	5	4	3	2	1	0
	PCM_VOLUME_B							
Default	0	1	1	1	1	0	0	0

Bits	Name	Description
7:0	PCM_VOLUME_B	Digital volume control registers for PCM channel B. It allows independent control of the signal level in 1/2 dB increments from 0 to –127 dB. Volume settings are decoded as shown below. The volume changes are dictated by the PCM_SZC bits. The same rule applies to PCM_VOLUME_A setting. 0000 0000 0 dB 0000 0001 –0.5 dB ... 01111000 –60 dB (Default) ... 1111 1110 –127 dB 1111 1111 Digital mute

7.5.4 PCM Volume A

Address 0x90002

R/W	7	6	5	4	3	2	1	0
	PCM_VOLUME_A							
Default	0	1	1	1	1	0	0	0

Bits	Name	Description
7:0	PCM_VOLUME_A	Digital volume control registers for channel A. See PCM_VOLUME_B for description.

7.5.5 PCM Path Signal Control 1

Address 0x90003

R/W	7	6	5	4	3	2	1	0
	PCM_RAMP_DOWN	PCM_VOL_BEQA	PCM_SZC		PCM_AMUTE	PCM_AMUTEBEQA	PCM_MUTE_A	PCM_MUTE_B
Default	1	0	1	0	1	0	0	0

Bits	Name	Description
7	PCM_RAMP_DOWN	Soft volume ramp-down before filter mode change. A mute is performed before filter mode change and an unmute is performed after executing the filter mode change. 0 Immediate mute is performed prior to executing a filter mode change 1 (Default) This mute and unmute is controlled by PCM_SZC.
6	PCM_VOL_BEQA	PCM_VOLUME_B equals PCM_VOLUME_A. 0 (Default) Volume setting of both channels are controlled independently. 1 Volume setting of both channels are controlled by PCM_VOLUME_A. PCM_VOLUME_B is ignored.
5:4	PCM_SZC	Soft ramp and zero cross control. 00 Immediate change 01 In PCM mode, zero cross change 10 (Default) Soft ramp 11 In PCM mode, soft ramp and zero crossings
3	PCM_AMUTE	PCM auto mute. 0 Function disabled 1 (Default) Mute occurs after reception of 8,192 consecutive audio samples of static 0 or –1. A single sample of non-static data releases the mute. Detection and muting is done independently for each channel.
2	PCM_AMUTEBEQA	Auto mute channel B equals channel A. 0 (Default) Function disabled. 1 Only mute when both channels AMUTE conditions are detected.
1	PCM_MUTE_A	Channel A mute. 0 (Default) Function is disabled. 1 Channel output is muted. Muting function is affected by the PCM_SZC bits.
0	PCM_MUTE_B	Channel A mute. 0 (Default) Function is disabled. 1 Channel output is muted. Muting function is affected by the PCM_SZC bits.

7.5.6 PCM Path Signal Control 2

Address 0x90004

R/W	7	6	5	4	3	2	1	0
	—				PCM_INV_A	PCM_INV_B	PCM_SWAP_CHAN	PCM_COPY_CHAN
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7:4	—	Reserved
3	PCM_INV_A	Channel A signal invert. 0 (Default) Function is disabled 1 Signal polarity of channel A is inverted
2	PCM_INV_B	Channel B signal invert. 0 (Default) the function is disabled 1 Signal polarity of channel B is inverted
1	PCM_SWAP_CHAN	Swap channels A and B at the input. This bit takes effect before PCM_COPY_CHAN. 0 (Default) Function disabled 1 Enable channel A and B swapping
0	PCM_COPY_CHAN	Copy channel A to channel B. This bit takes effect after PCM_SWAP_CHAN. 0 (Default) Function disabled 1 Enable copy A to B function

7.5.7 Class H Control

Address 0xB0000

R/W	7	6	5	4	3	2	1	0
	—			ADPT_PWR			HV_EN	EXT_VCPFILT
Default	0	0	0	1	1	1	1	0

Bits	Name	Description
7:5	—	Reserved
4:2	ADPT_PWR	Adaptive power adjustment. Configures how power to line output amplifiers adapts to the output signal level. 000 Reserved 001 Fixed, Mode 0 (±VP_LDO) 010 Fixed, Mode 1 (±VCP) 011–110 Reserved 111 (Default) Adapt to signal. The output signal dynamically determines the voltage level.
1	HV_EN	High voltage mode enable. 0 Function disabled (VP_LDO = 2.6V) 1 (Default) Function enabled (VP_LDO = 3.0 V). This requires VP min to be 3.3 V. Also, this mode only applies to load 600 Ω and above.
0	EXT_VCPFILT	External VCP_FILT± voltage mode. 0 (Default) Function disabled 1 When enabled, VCP_FILT± voltages can be provided externally at ±3.0 V. See power sequencing/timing requirement in related functional description.

7.5.8 HP Detect

Address 0xD0000

R/W	7	6	5	4	3	2	1	0
	HPDETECT_CTRL		HPDETECT_INV	HPDETECT_RISE_DBC_TIME		HPDETECT_FALL_DBC_TIME		—
Default	0	0	0	0	0	1	0	0

Bits	Name	Description
7:6	HPDETECT_CTRL	HP detect control. Configures operation of the HP detect circuit. The internal weak current source pull-up is enabled in all modes. 00 (Default) Disabled. The HP detect digital circuit is powered down and does not report to the status registers (HPDETECT_PLUG_INT and HPDETECT_UNPLUG_INT are also cleared). 01–10 Reserved 11 Enabled
5	HPDETECT_INV	HP detect invert. Can be used to invert the signal from the HP detect circuit. 0 (Default) Not inverted 1 Inverted
4:3	HPDETECT_RISE_DBC_TIME	Tip sense rising debounce time. 00 (Default) 0 ms 01 250 ms 10 500 ms 11 1.0 s
2:1	HPDETECT_FALL_DBC_TIME	Tip sense falling debounce time. 00 0 ms 01 250 ms 10 (Default) 500 ms 11 1.0 s
0	—	Reserved

7.5.9 HP Status

Address 0xD0001

R/O	7	6	5	4	3	2	1	0
	—	HPDETECT_PLUG_DBC	HPDETECT_UNPLUG_DNC			—		
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	—	Reserved
6	HPDETECT_PLUG_DBC	HPDETECT plug debounce status. Setting HPDETECT_INV reverses the meaning of this bit. 0 (Default) Condition is not present 1 Condition is present

Bits	Name	Description
5	HPDETECT_ UNPLUG_ DBC	HPDETECT unplug debounce status. Setting HPDETECT_INV reverses the meaning of this bit. 0 (Default) Condition is not present 1 Condition is present
4:0	—	Reserved

7.6 Interrupt Status and Mask Registers

7.6.1 Interrupt Status 1

Address 0xF0000

R/O	7	6	5	4	3	2	1	0
	DAC_OVFL_ INT	HPDETECT_ PLUG_INT	HPDETECT_ UNPLUG_INT	XTAL_READY_ INT	XTAL_ ERROR_INT	PLL_READY_ INT	PLL_ERROR_ INT	PDN_DONE_ INT
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	DAC_OVFL_ INT	Status indicating DAC modulator overflow condition is detected. 0 Condition is not present 1 Condition is present
6	HPDETECT_ PLUG_INT	Status indicating HP plug event is detected. 0 Condition is not present 1 Condition is present
5	HPDETECT_ UNPLUG_INT	Status indicating HP unplug event is detected. 0 Condition is not present 1 Condition is present
4	XTAL_ READY_INT	Status indicating XTAL is ready after PDN_XTAL is cleared. 0 Condition is not present 1 Condition is present
3	XTAL_ ERROR_INT	Status indicating XTAL error condition is detected after PDN_XTAL is cleared. 0 Condition is not present 1 Condition is present
2	PLL_READY_ INT	Status indicating PLL ready condition is detected after PLL_START is set. 0 Condition is not present 1 Condition is present
1	PLL_ERROR_ INT	Status indicating PLL error condition is detected after PLL_START is set. 0 Condition is not present 1 Condition is present
0	PDN_DONE_ INT	Status indicating PDN_HP process is completed after a request. 0 Condition is not present 1 Condition is present

7.6.2 Interrupt Status 2

Address 0xF0001

R/O	7	6	5	4	3	2	1	0
	ASP_OVFL_ INT	ASP_ERROR_ INT	ASP_LATE_ INT	ASP_EARLY_ INT	ASP_ NOLRCK_INT	—		
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	ASP_OVFL_ INT	ASP RX request overload. 0 Condition is not present 1 Condition is present
6	ASP_ ERROR_INT	ASP RX LRCK error. Logical OR of LRCK early and LRCK late errors. 0 Condition is not present 1 Condition is present
5	ASP_LATE_ INT	ASP RX LRCK late. 0 Condition is not present 1 Condition is present
4	ASP_EARLY_ INT	ASP RX LRCK early. 0 Condition is not present 1 Condition is present

Bits	Name	Description
3	ASP_ NOLRCK_INT	ASP RX no LRCK. 0 Condition is not present 1 Condition is present
2:0	—	Reserved

7.6.3 Interrupt Status 3

Address 0xF0002

R/O	7	6	5	4	3	2	1	0
	XSP_OVFL_ INT	XSP_ERROR_ INT	XSP_LATE_ INT	XSP_EARLY_ INT	XSP_ NOLRCK_INT	—		
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	XSP_OVFL_ INT	XSP RX request overload. 0 Condition is not present 1 Condition is present
6	XSP_ ERROR_INT	XSP RX LRCK error. Logical OR of LRCK early and LRCK late errors. 0 Condition is not present 1 Condition is present
5	XSP_LATE_ INT	XSP RX LRCK late. 0 Condition is not present 1 Condition is present
4	XSP_EARLY_ INT	XSP RX LRCK early. 0 Condition is not present 1 Condition is present
3	XSP_ NOLRCK_INT	XSP RX no LRCK. 0 Condition is not present 1 Condition is present
2:0	—	Reserved

7.6.4 Interrupt Status 5

Address 0xF0004

R/O	7	6	5	4	3	2	1	0
	DSD_STUCK_ INT	DSD_INVAL_ A_INT	DSD_INVAL_ B_INT	DSD_ SILENCE_A_ INT	DSD_ SILENCE_B_ INT	DSD_RATE_ ERROR_INT	DOP_MRK_ DET_INT	DOP_ON_INT
Default	0	0	0	0	0	0	0	0

Bits	Name	Description
7	DSD_STUCK_ INT	At least one DSD input channel is stuck at 0 or 1. 0 Condition is not present 1 Condition is present
6	DSD_INVAL_ A_INT	Channel A input exceeds the max peak level of +3.1-dB SACD. 0 Condition is not present 1 Condition is present
5	DSD_INVAL_ B_INT	Channel B input exceeds the max peak level of +3.1-dB SACD. 0 Condition is not present 1 Condition is present
4	DSD_ SILENCE_A_ INT	Channel A contains DSD silence pattern. 0 Condition is not present 1 Condition is present
3	DSD_ SILENCE_B_ INT	Channel B contains DSD silence pattern. 0 Condition is not present 1 Condition is present
2	DSD_RATE_ ERROR_INT	DSD data rate-related error is detected. The rate of the input DSD stream is not as described in DSD_SPEED setting. 0 Condition is not present 1 Condition is present
1	DOP_MRK_ DET_INT	A valid sequence of DoP markers has been detected. 0 Condition is not present 1 Condition is present

Bits	Name	Description
0	DOP_ON_INT	The DoP decoder is powered up. 0 Condition is not present 1 Condition is present

7.6.5 Interrupt Mask 1

Address 0xF0010

R/W	7	6	5	4	3	2	1	0
	DAC_OVFL_INT_MASK	HPDETECT_PLUG_INT_MASK	HPDETECT_UNPLUG_INT_MASK	XTAL_READY_INT_MASK	XTAL_ERROR_INT_MASK	PLL_READY_INT_MASK	PLL_ERROR_INT_MASK	PDN_DONE_INT_MASK
Default	1	1	1	1	1	1	1	1

Bits	Name	Description
7	DAC_OVFL_INT_MASK	DAC_OVFL_INT mask. 0 Unmasked 1 (Default) Masked
6	HPDETECT_PLUG_INT_MASK	HP_DETECT_PLUG_INT mask. 0 Unmasked 1 (Default) Masked
5	HPDETECT_UNPLUG_INT_MASK	HP_DETECT_UNPLUG_INT mask. 0 Unmasked 1 (Default) Masked
4	XTAL_READY_INT_MASK	XTAL_READY_INT mask. 0 Unmasked 1 (Default) Masked
3	XTAL_ERROR_INT_MASK	XTAL_ERROR_INT mask. 0 Unmasked 1 (Default) Masked
2	PLL_READY_INT_MASK	PLL_READY_INT mask. 0 Unmasked 1 (Default) Masked
1	PLL_ERROR_INT_MASK	PLL_ERROR_INT mask. 0 Unmasked 1 (Default) Masked
0	PDN_DONE_INT_MASK	PDN_DONE_INT mask. 0 Unmasked 1 (Default) Masked

7.6.6 Interrupt Mask 2

Address 0xF0011

R/W	7	6	5	4	3	2	1	0
	ASP_OVFL_INT_MASK	ASP_ERROR_INT_MASK	ASP_LATE_INT_MASK	ASP_EARLY_INT_MASK	ASP_NOLRCK_INT_MASK	—		
Default	1	1	1	1	1	1	1	1

Bits	Name	Description
7	ASP_OVFL_INT_MASK	ASP_OVFL_INT mask. 0 Unmasked 1 (Default) Masked
6	ASP_ERROR_INT_MASK	ASP_ERROR_INT mask. 0 Unmasked 1 (Default) Masked
5	ASP_LATE_INT_MASK	ASP_LATE_INT mask. 0 Unmasked 1 (Default) Masked
4	ASP_EARLY_INT_MASK	ASP_EARLY_INT mask. 0 Unmasked 1 (Default) Masked

Bits	Name	Description
3	ASP_ NOLRCK_ INT_MASK	ASP_NOLRCK_INT mask. 0 Unmasked 1 (Default) Masked
2:0	—	Reserved

7.6.7 Interrupt Mask 3

Address 0xF0012

R/W	7	6	5	4	3	2	1	0
	XSP_OVFL_ INT_MASK	XSP_ERROR_ INT_MASK	XSP_LATE_ INT_MASK	XSP_EARLY_ INT_MASK	XSP_ NOLRCK_INT_ MASK	—		
Default	1	1	1	1	1	0	0	0

Bits	Name	Description
7	XSP_OVFL_ INT_MASK	XSP_OVFL_INT mask. 0 Unmasked 1 (Default) Masked
6	XSP_ ERROR_INT_ MASK	XSP_ERROR_INT mask. 0 Unmasked 1 (Default) Masked
5	XSP_LATE_ INT_MASK	XSP_LATE_INT mask. 0 Unmasked 1 (Default) Masked
4	XSP_EARLY_ INT_MASK	XSP_EARLY_INT mask. 0 Unmasked 1 (Default) Masked
3	XSP_ NOLRCK_ INT_MASK	XSP_NOLRCK_INT mask. 0 Unmasked 1 (Default) Masked
2:0	—	Reserved

7.6.8 Interrupt Mask 5

Address 0xF0014

R/W	7	6	5	4	3	2	1	0
	DSD_STUCK_INT_MASK	DSD_INVAL_A_INT_MASK	DSD_INVAL_B_INT_MASK	DSD_SILENCE_A_INT_MASK	DSD_SILENCE_B_INT_MASK	DSD_RATE_ERROR_INT_MASK	DOP_MRK_DET_INT_MASK	DOP_ON_INT_MASK
Default	1	1	1	1	1	1	1	1

Bits	Name	Description
7	DSD_STUCK_INT_MASK	DSD_STUCK_INT mask. 0 Unmasked 1 (Default) Masked
6	DSD_INVAL_A_INT_MASK	DSD_INVAL_A_INT mask. 0 Unmasked 1 (Default) Masked
5	DSD_INVAL_B_INT_MASK	DSD_INVAL_B_INT mask. 0 Unmasked 1 (Default) Masked
4	DSD_SILENCE_A_INT_MASK	DSD_SILENCE_A_INT mask. 0 Unmasked 1 (Default) Masked
3	DSD_SILENCE_B_INT_MASK	DSD_SILENCE_B_INT mask. 0 Unmasked 1 (Default) Masked
2	DSD_RATE_ERROR_INT_MASK	DSD_RATE_ERROR_INT mask. 0 Unmasked 1 (Default) Masked
1	DOP_MRK_DET_INT_MASK	DOP_MRK_DET_INT mask. 0 Unmasked 1 (Default) Masked
0	DOP_ON_INT_MASK	DOP_ON_INT mask. 0 Unmasked 1 (Default) Masked

8 PCB Layout Considerations

The following sections provide general guidelines for PCB layout to ensure the best performance of the CS4399.

8.1 Power Supply

As with any high-resolution converter, the CS4399 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Fig. 2-1 shows the recommended power arrangements with VA and VCP connected to independent clean supplies. VL and VD, which power the digital circuitry, may be run from the shared system logic supply.

8.2 Grounding

Note the following:

- Extensive use of power and ground planes, ground-plane fill in unused areas, and surface-mount decoupling capacitors are recommended.
- Decoupling capacitors must be as close as possible to the CS4399 pins.
- To minimize inductance effects, the low-value ceramic capacitor must be closest to the pin and mounted on the same side of the board as the CS4399.
- To avoid unwanted coupling into the modulators, all signals, especially clocks, must be isolated from the FILT+ and FILT- pins.
- The FILT+ capacitors must be positioned to minimize the electrical path from the pin to VA.
- The FILT– capacitors must be positioned to minimize the electrical path from the pin to –VA.
- The VCP_FILT+ and VCP_FILT– capacitors must be positioned to minimize the electrical path from each respective pin to GNDCP.

8.3 REFA and REFB Routing

For best interchannel isolation performance, REFA and REFB must be routed independently to the headphone connector reference pin. The REFA and REFB are electrically connected to system's ground plane through via at the headphone connector ground pin. Fig. 2-1 illustrates the recommended arrangements.

For interfacing the REFA and REFB pins with an IC that performs alternate pinout headset detect functions, both signals must be routed independently to the CS4399's ground pin connecting the detected headset ground pole. Follow the recommended grounding scheme of the CS4399.

8.4 QFN Thermal Pad

The CS4399 comes in a compact QFN package, the underside of which reveals a large metal pad that serves as a thermal relief to provide maximum heat dissipation. This pad must mate with an matching copper pad on the PCB and must be electrically connected to ground. A series of vias must be used to connect this copper pad to one or more larger ground planes on other PCB layers. For best performance in split-ground systems, connect this thermal pad to GNDA.

9 Performance Plots

9.1 Digital Filter Response

9.1.1 Combined Filter Response—Single Speed (Fs = 32 kHz, Slow Roll-Off)

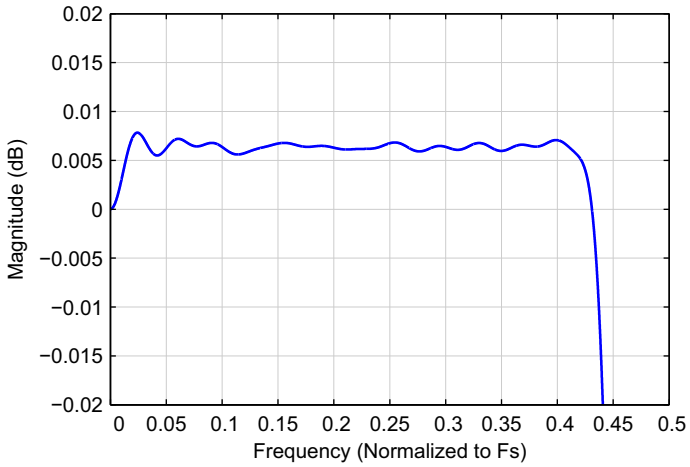


Figure 9-1. Passband Ripple

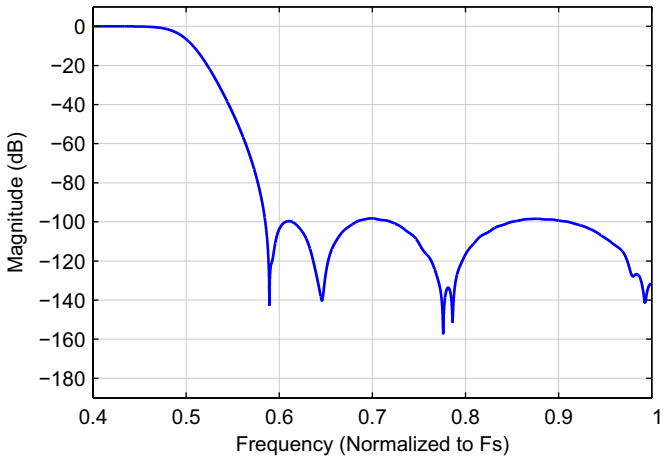


Figure 9-2. Stopband Attenuation

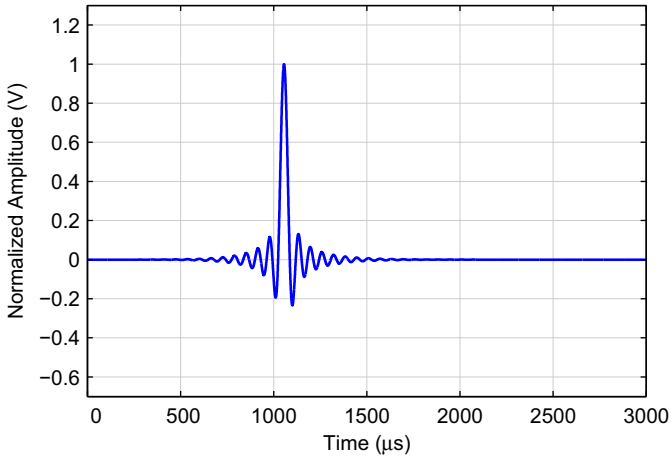


Figure 9-3. Impulse Response—Linear Phase

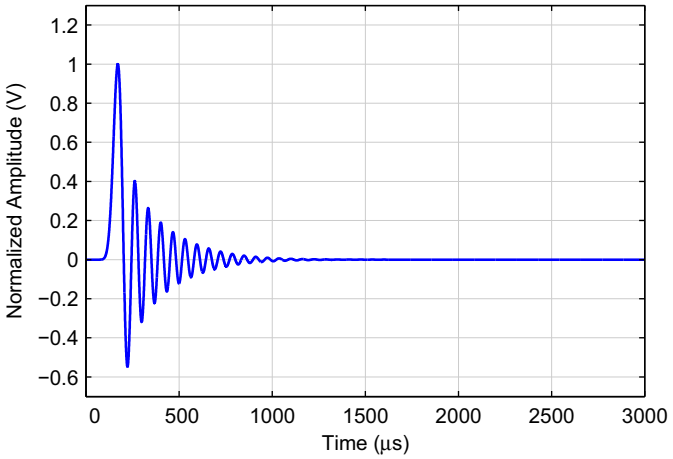


Figure 9-4. Impulse Response—Minimum Phase

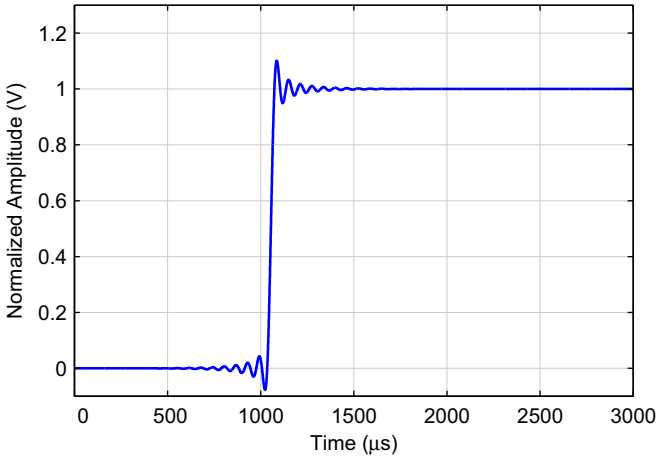


Figure 9-5. Step Response—Linear Phase

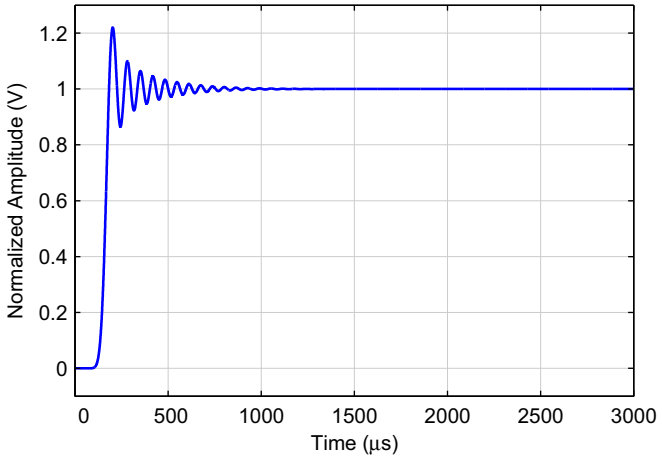


Figure 9-6. Step Response—Minimum Phase

9.1.2 Combined Filter Response—Single Speed (Fs = 32 kHz, Fast Roll-Off)

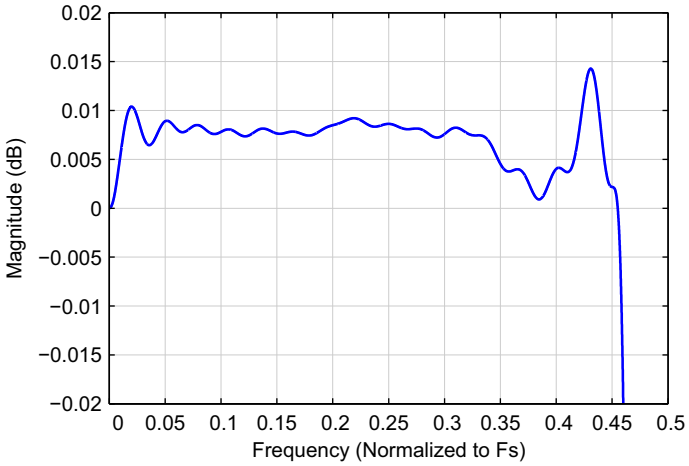


Figure 9-7. Passband Ripple

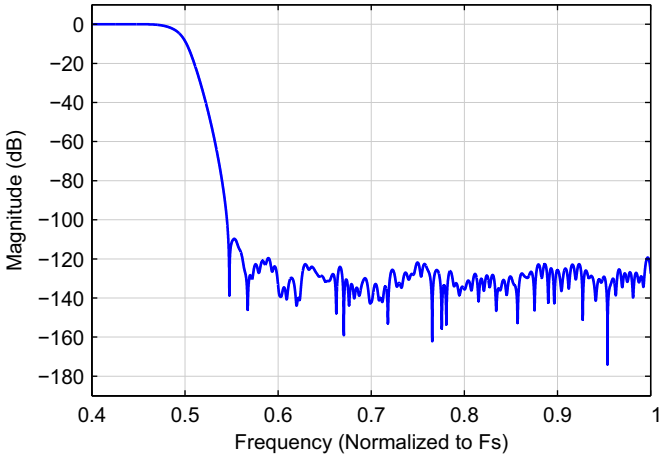


Figure 9-8. Stopband Attenuation

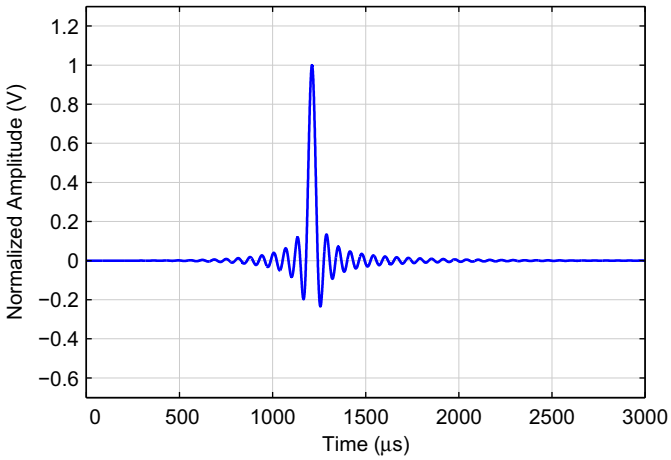


Figure 9-9. Impulse Response—Linear Phase

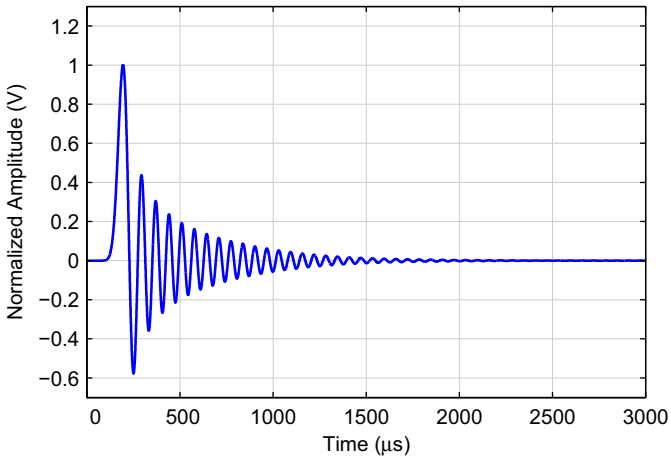


Figure 9-10. Impulse Response—Minimum Phase

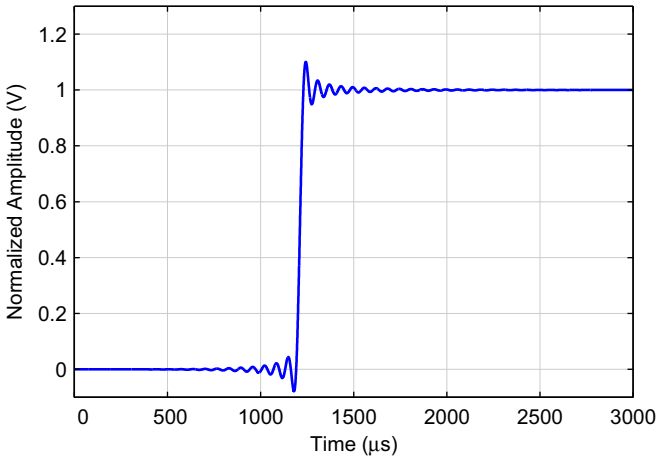


Figure 9-11. Step Response—Linear Phase

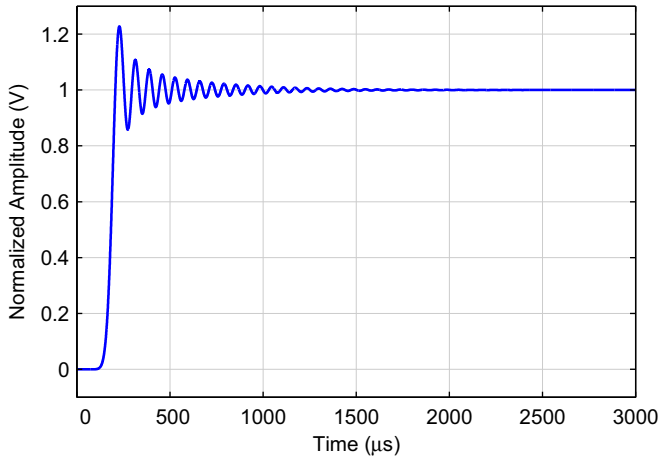


Figure 9-12. Step Response—Minimum Phase

9.1.3 Combined Filter Response—Single Speed (Fs = 44.1 and 48 kHz, Slow Roll-Off)

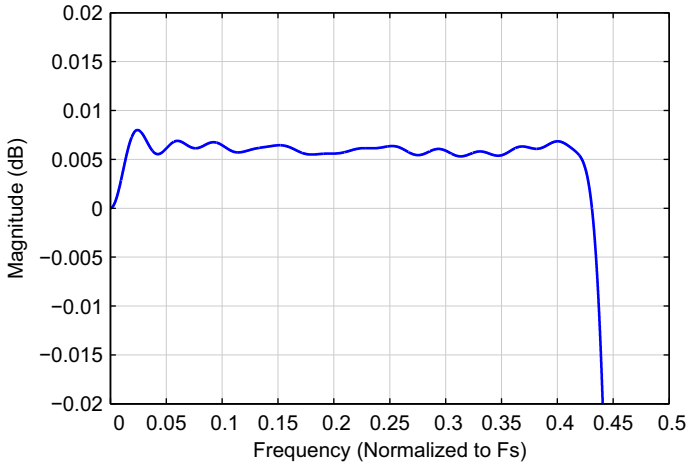


Figure 9-13. Passband Ripple

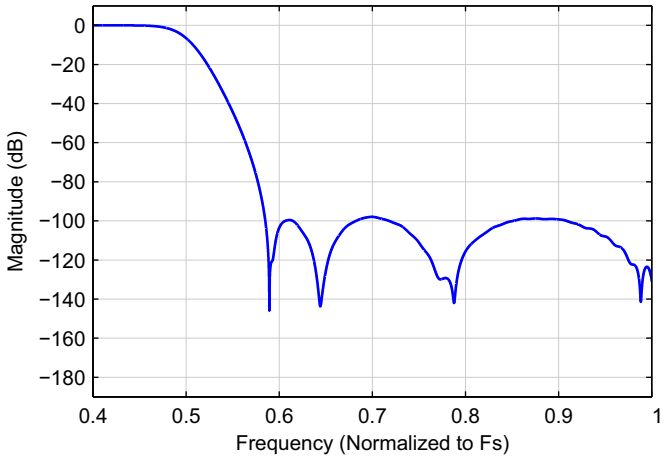


Figure 9-14. Stopband Attenuation

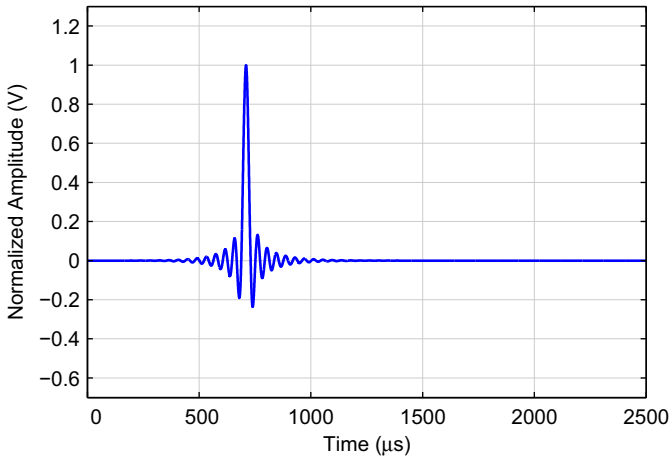


Figure 9-15. Impulse Response—Linear Phase

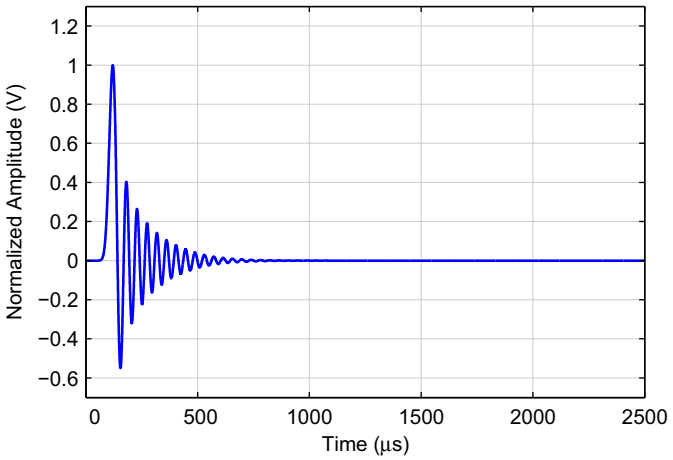


Figure 9-16. Impulse Response—Minimum Phase

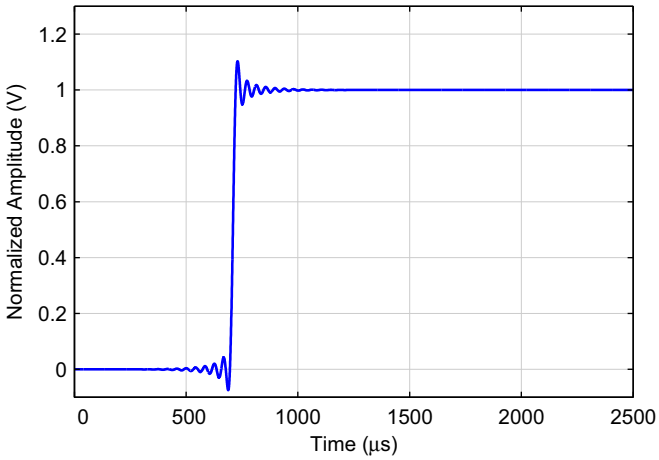


Figure 9-17. Step Response—Linear Phase

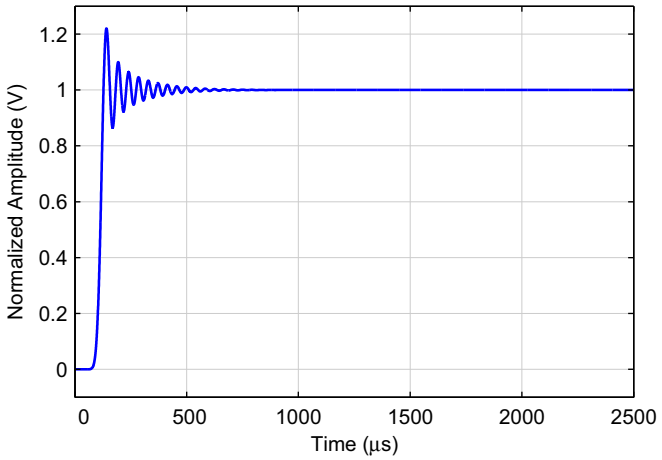


Figure 9-18. Step Response—Minimum Phase

9.1.4 Combined Filter Response—Single Speed (Fs = 44.1 and 48 kHz, Fast Roll-Off)

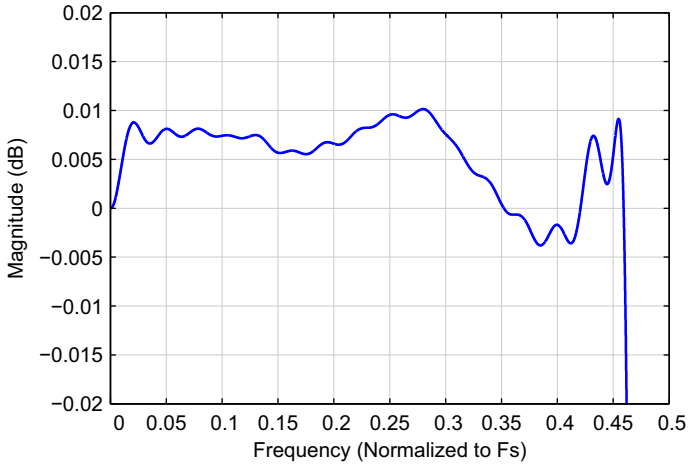


Figure 9-19. Passband Ripple

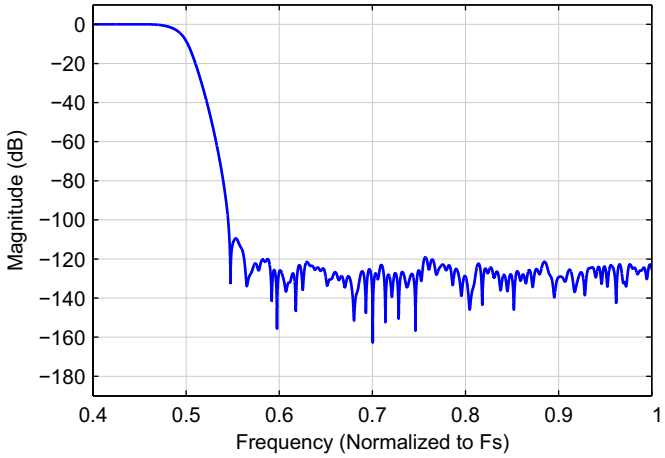


Figure 9-20. Stopband Attenuation

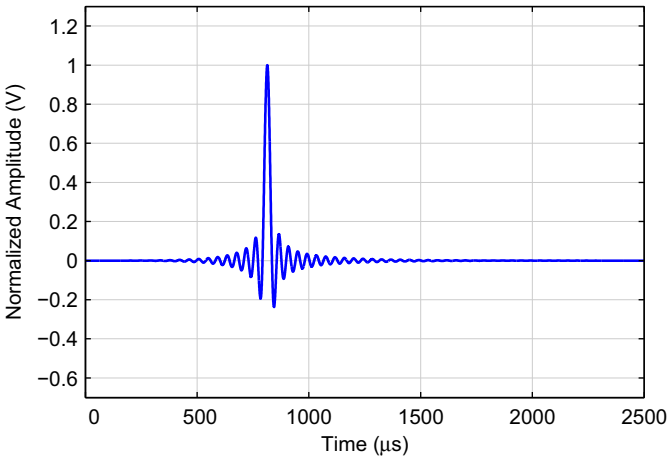


Figure 9-21. Impulse Response—Linear Phase

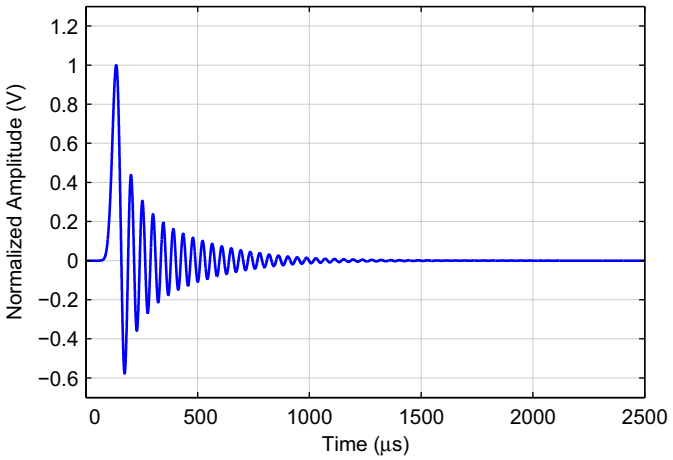


Figure 9-22. Impulse Response—Minimum Phase

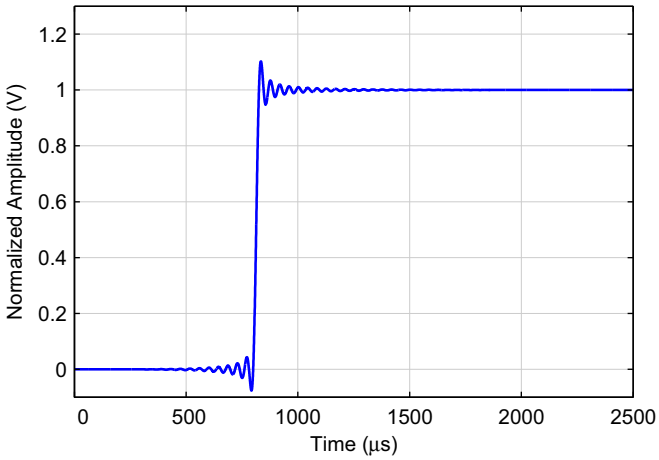


Figure 9-23. Step Response—Linear Phase

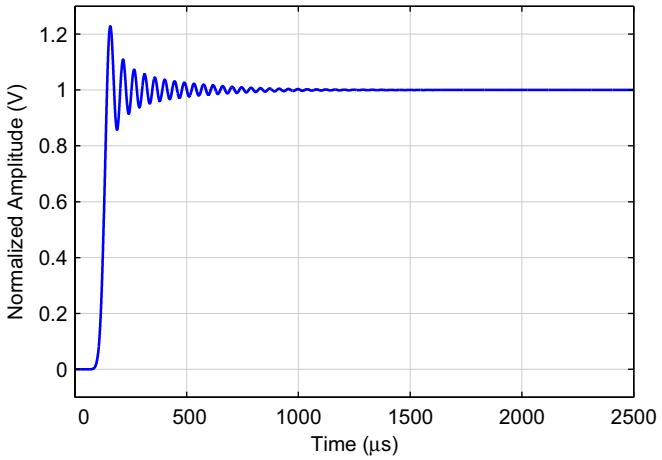


Figure 9-24. Step Response—Minimum Phase

9.1.5 Combined Filter Response—Double Speed (Slow Roll-Off)

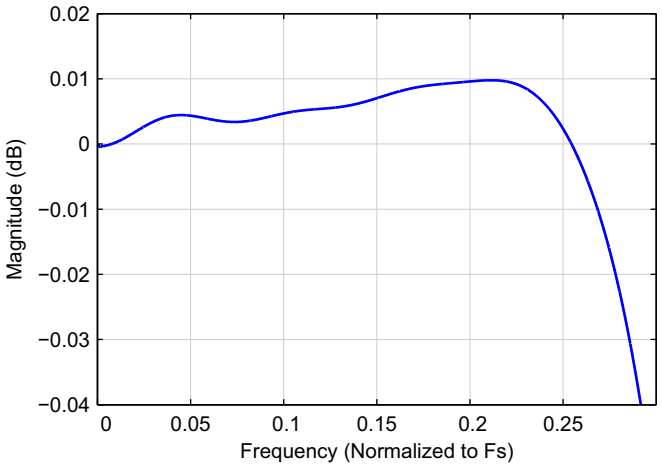


Figure 9-25. Passband Ripple

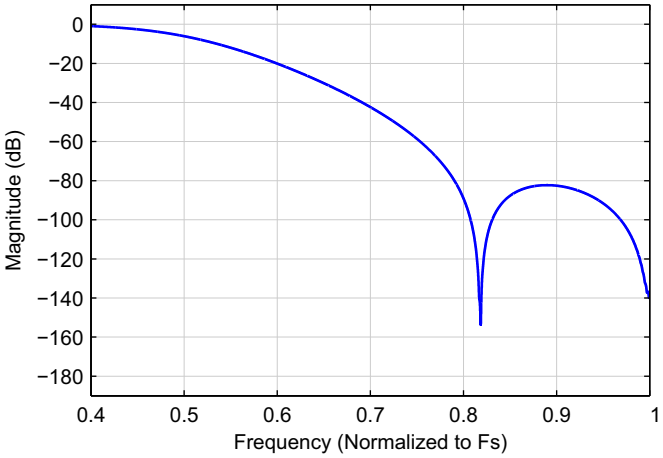


Figure 9-26. Stopband Attenuation

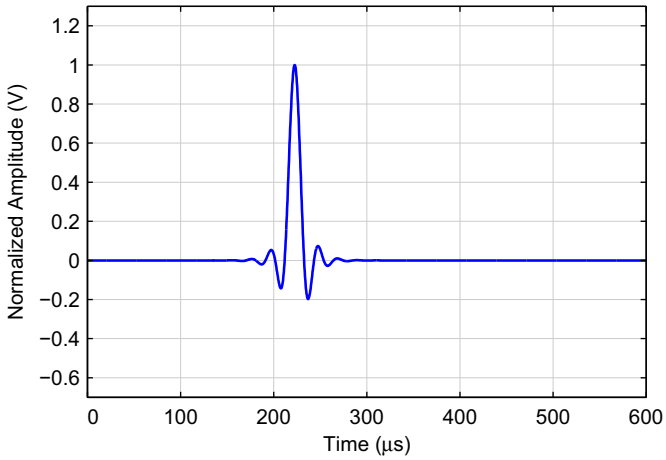


Figure 9-27. Impulse Response—Linear Phase

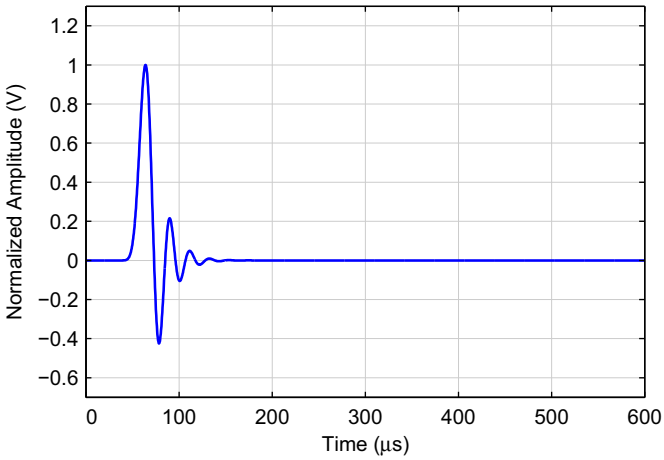


Figure 9-28. Impulse Response—Minimum Phase

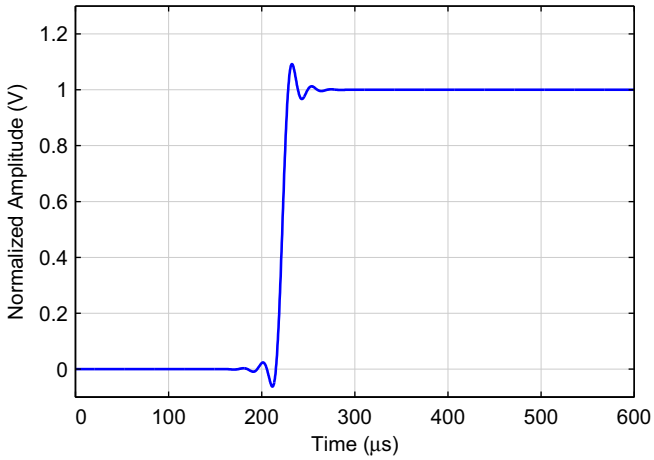


Figure 9-29. Step Response—Linear Phase

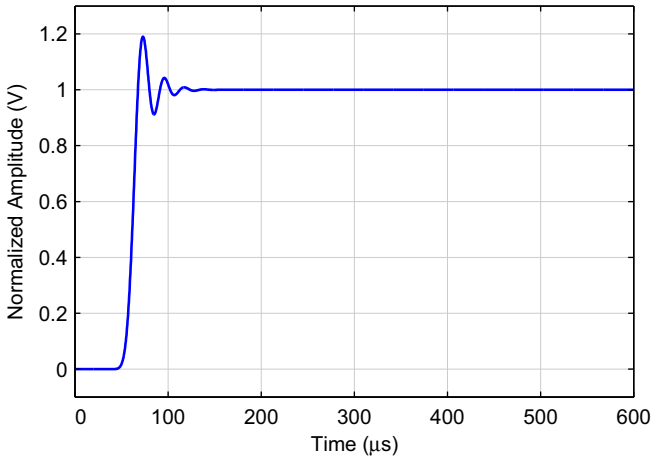


Figure 9-30. Step Response—Minimum Phase

9.1.6 Combined Filter Response—Double Speed (Fast Roll-Off)

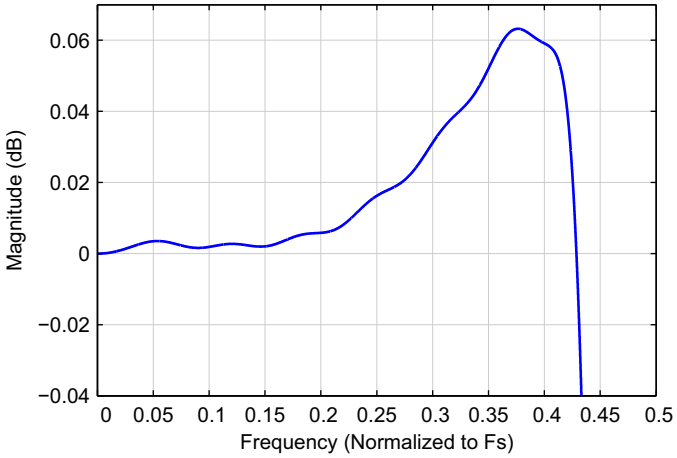


Figure 9-31. Passband Ripple

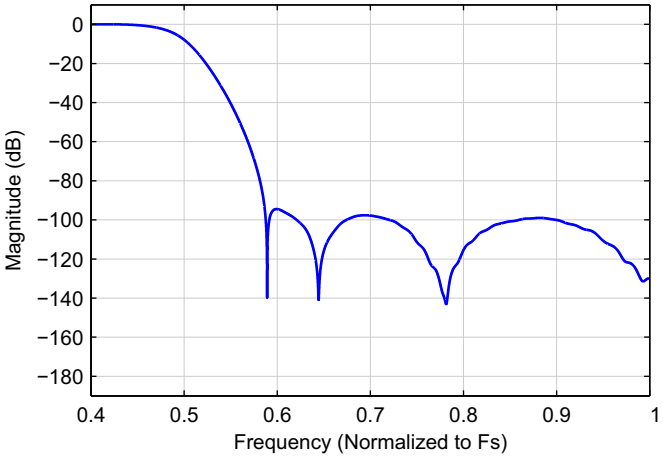


Figure 9-32. Stopband Attenuation

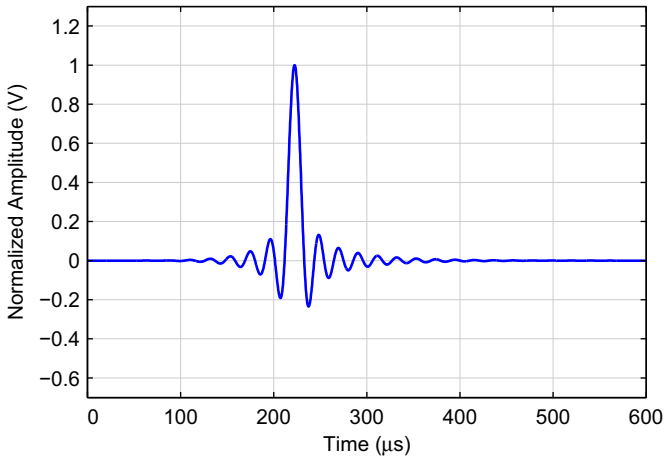


Figure 9-33. Impulse Response—Linear Phase

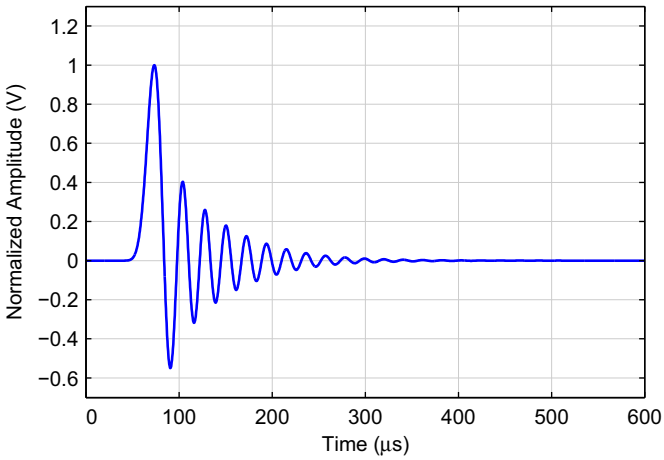


Figure 9-34. Impulse Response—Minimum Phase

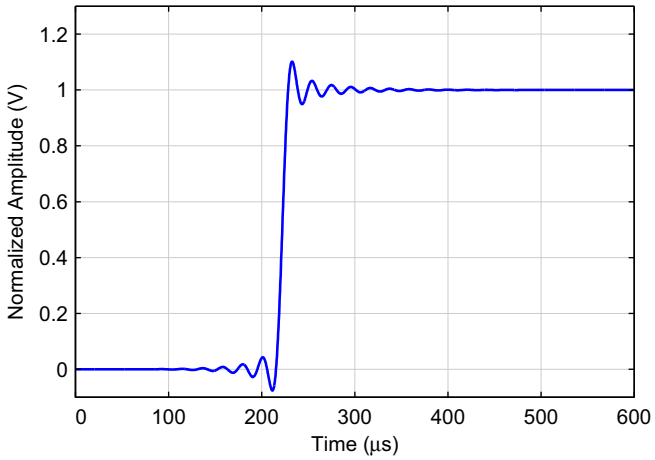


Figure 9-35. Step Response—Linear Phase

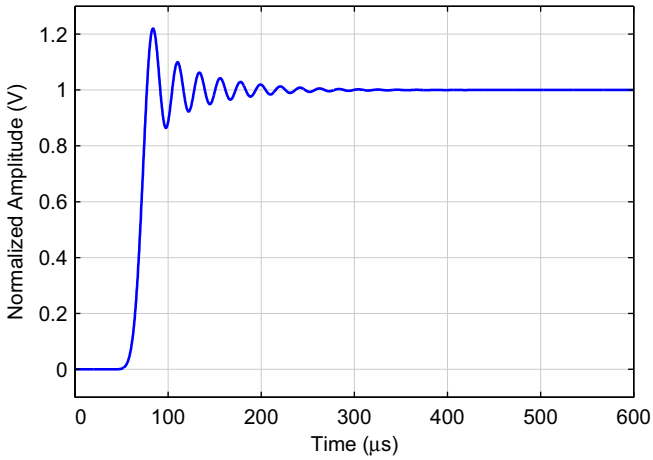


Figure 9-36. Step Response—Minimum Phase

9.1.7 Combined Filter Response—Quad Speed (Slow Roll-Off)

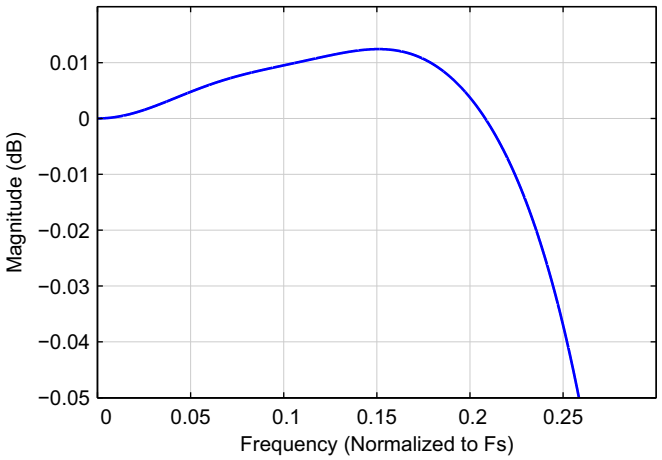


Figure 9-37. Passband Ripple

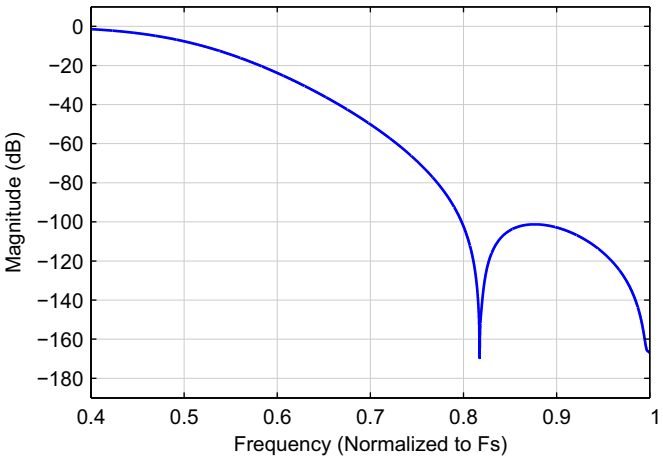


Figure 9-38. Stopband Attenuation

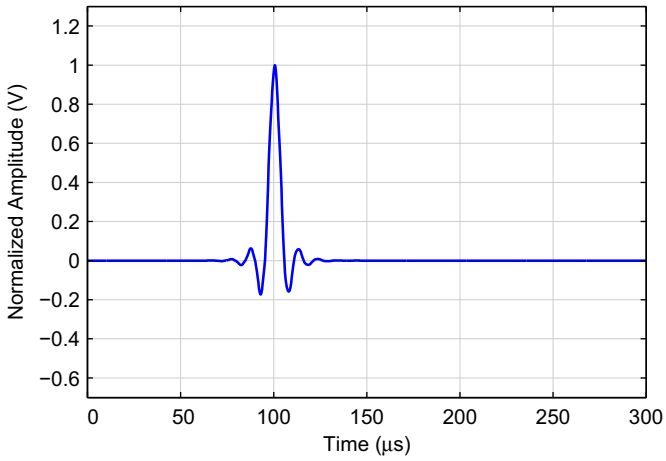


Figure 9-39. Impulse Response—Linear Phase

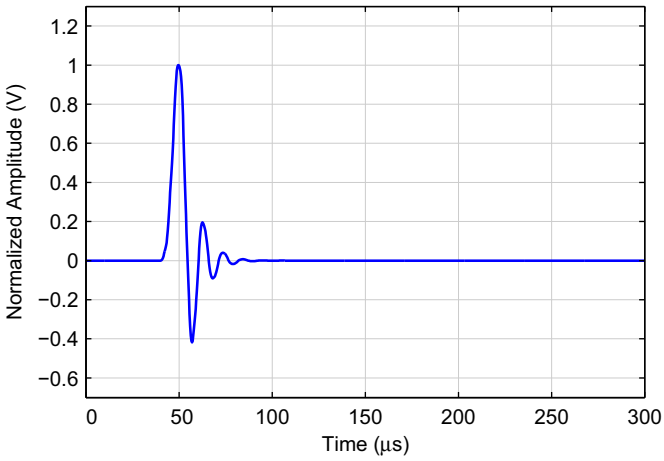


Figure 9-40. Impulse Response—Minimum Phase

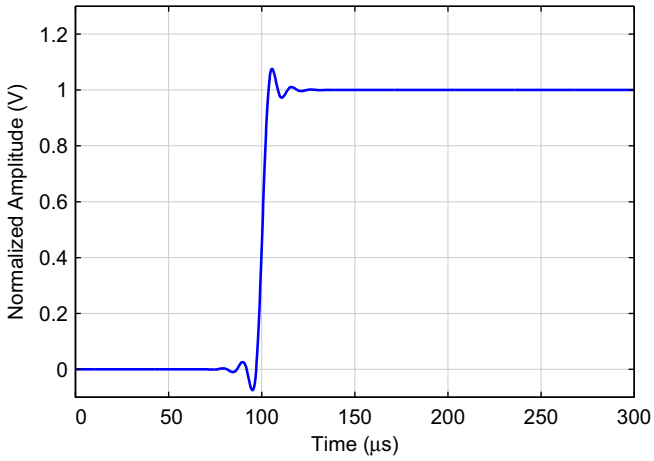


Figure 9-41. Step Response—Linear Phase

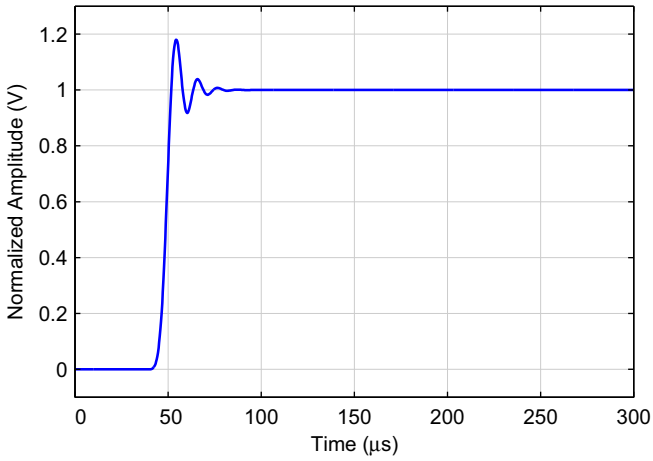


Figure 9-42. Step Response—Minimum Phase

9.1.8 Combined Filter Response—Quad Speed (Fast Roll-Off)

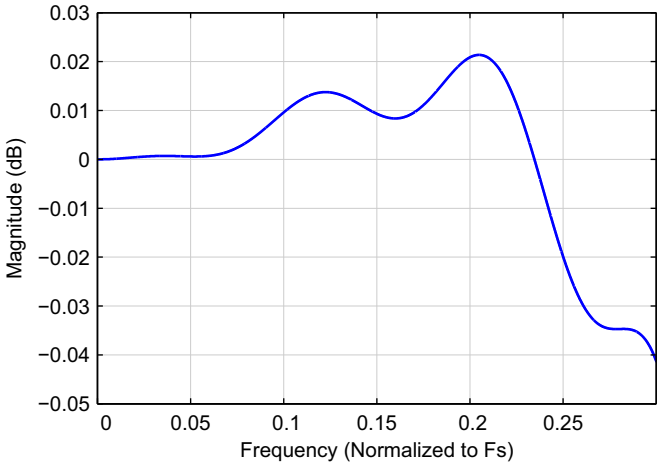


Figure 9-43. Passband Ripple

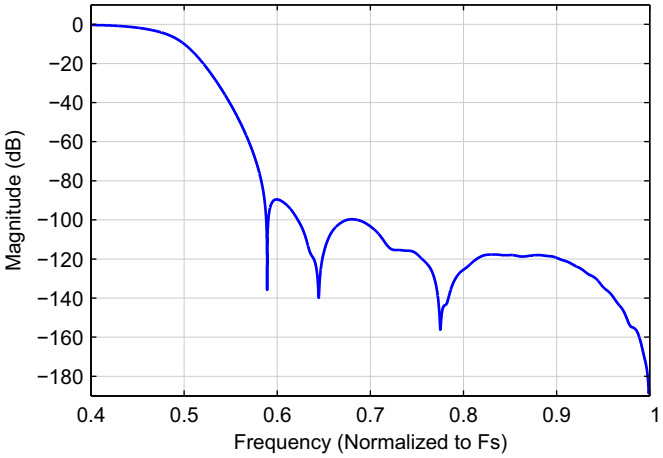


Figure 9-44. Stopband Attenuation

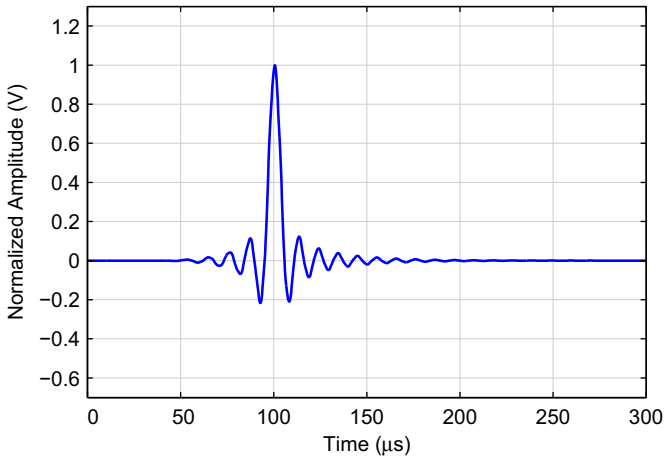


Figure 9-45. Impulse Response—Linear Phase

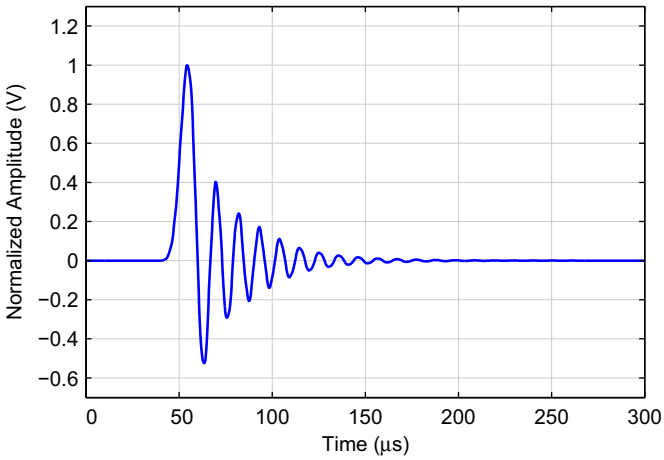


Figure 9-46. Impulse Response—Minimum Phase

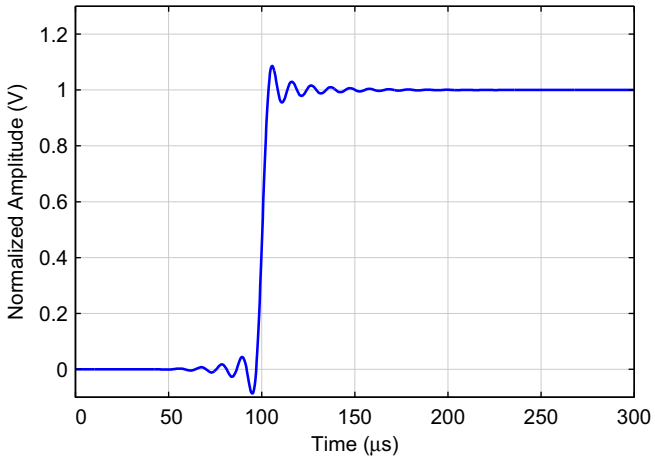


Figure 9-47. Step Response—Linear Phase

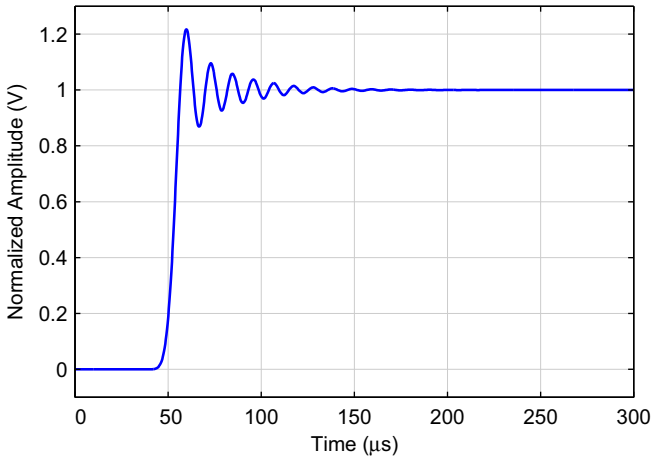


Figure 9-48. Step Response—Minimum Phase

9.1.9 Combined Filter Response—Octuple Speed

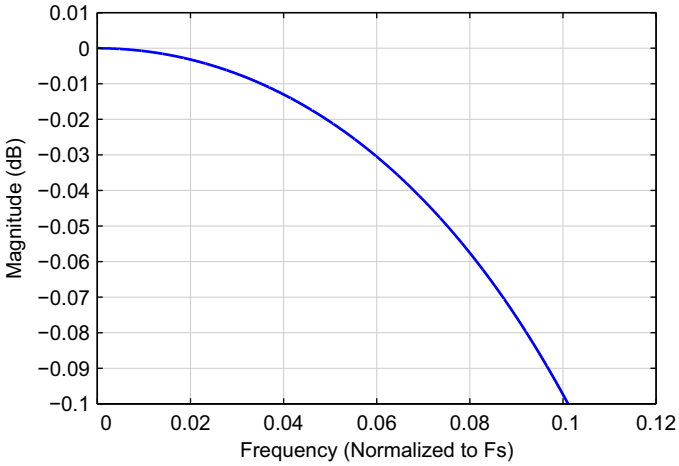


Figure 9-49. Passband Ripple

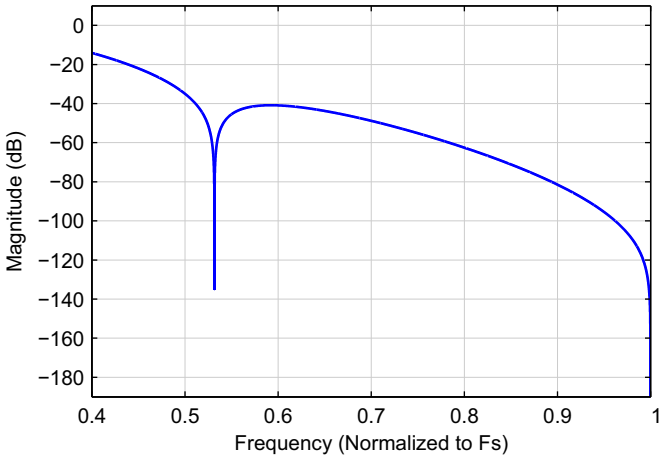


Figure 9-50. Stopband Attenuation

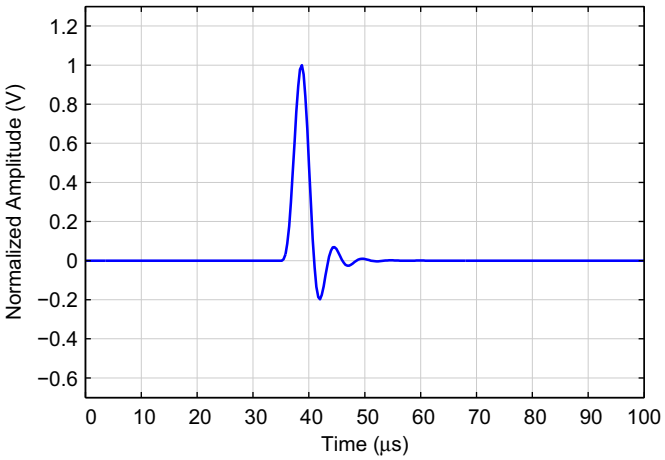


Figure 9-51. Impulse Response

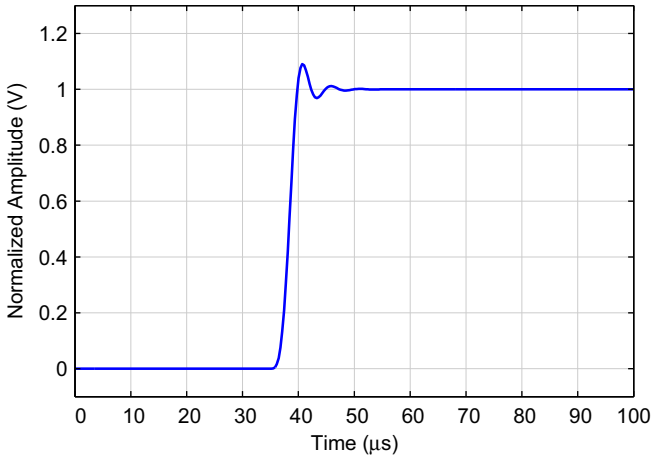


Figure 9-52. Step Response

9.1.10 Combined Filter Response—Single Speed (NOS = 1)

Note: 44.1 kHz and 48 kHz only.

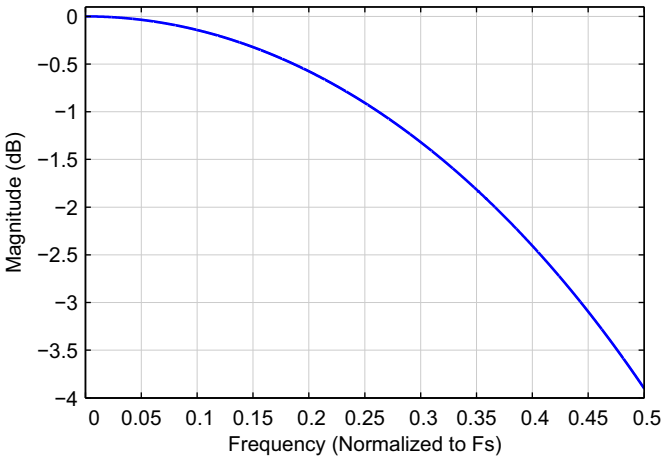


Figure 9-53. Passband Ripple

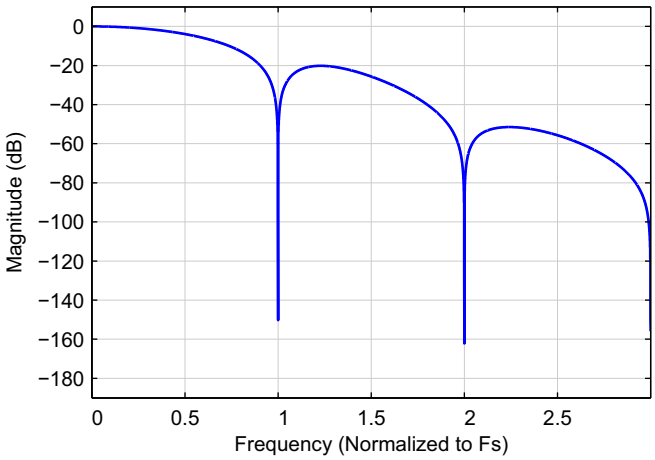


Figure 9-54. Stopband Attenuation

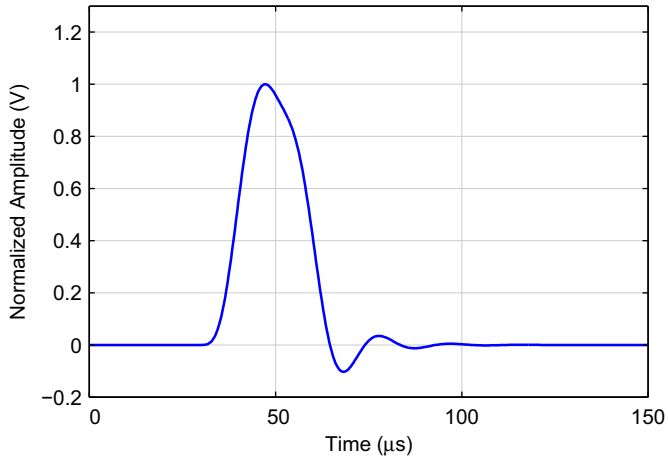


Figure 9-55. Impulse Response

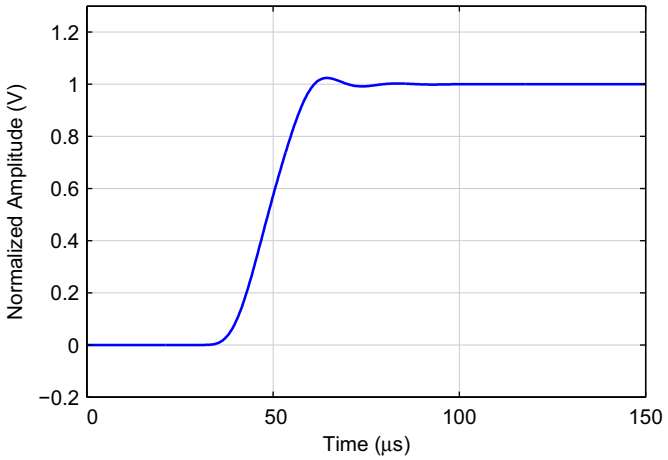


Figure 9-56. Step Response

9.1.11 Combined Filter Response—Double Speed (NOS = 1)

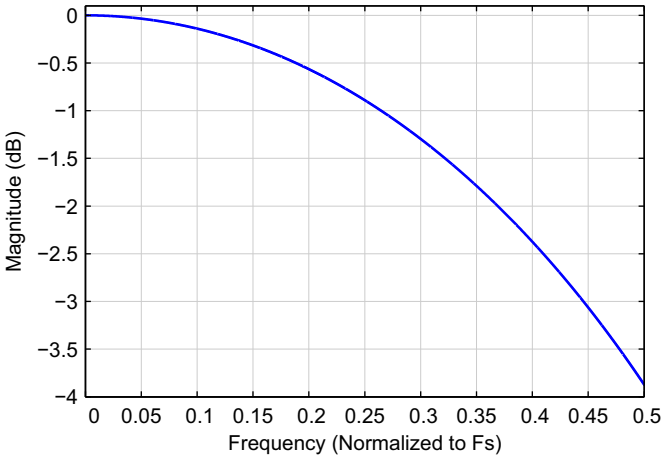


Figure 9-57. Passband Ripple

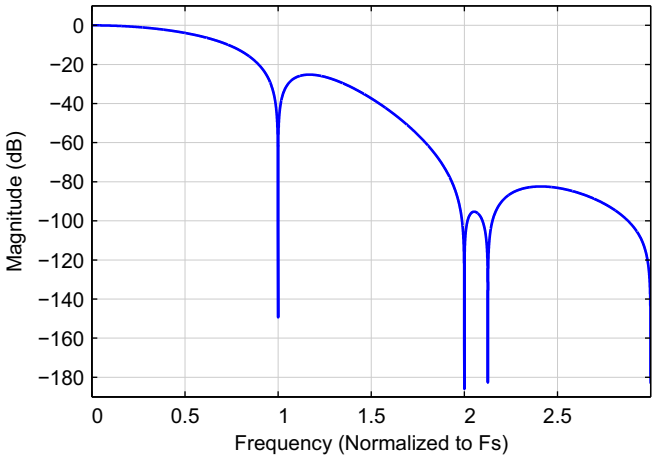


Figure 9-58. Stopband Attenuation

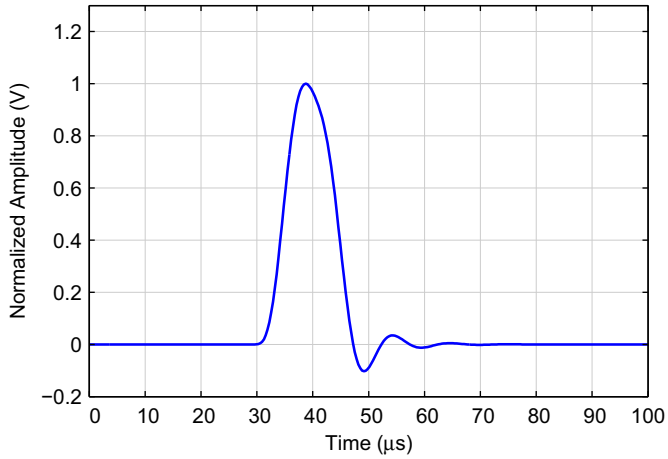


Figure 9-59. Impulse Response

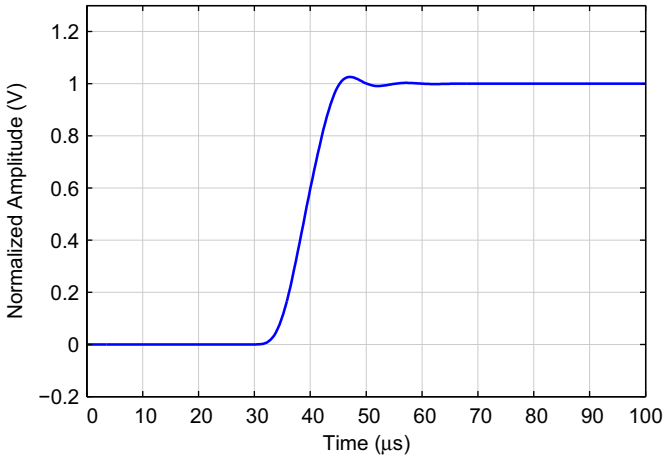


Figure 9-60. Step Response

9.1.12 Combined Filter Response—Quad Speed (NOS = 1)

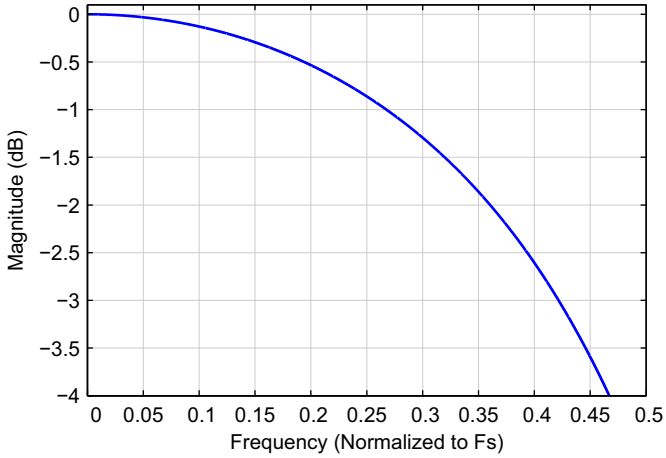


Figure 9-61. Passband Ripple

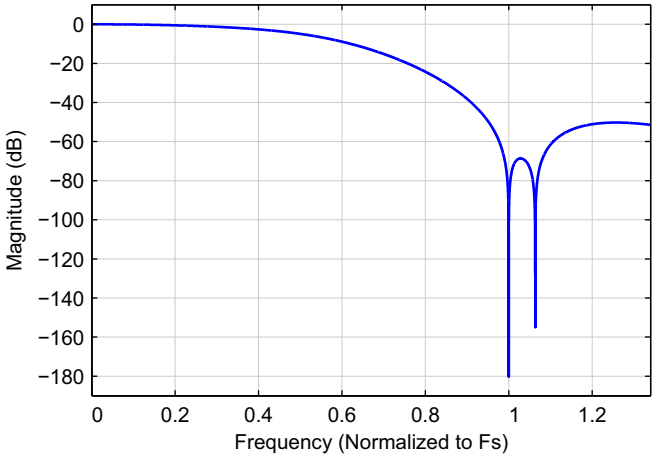


Figure 9-62. Stopband Attenuation

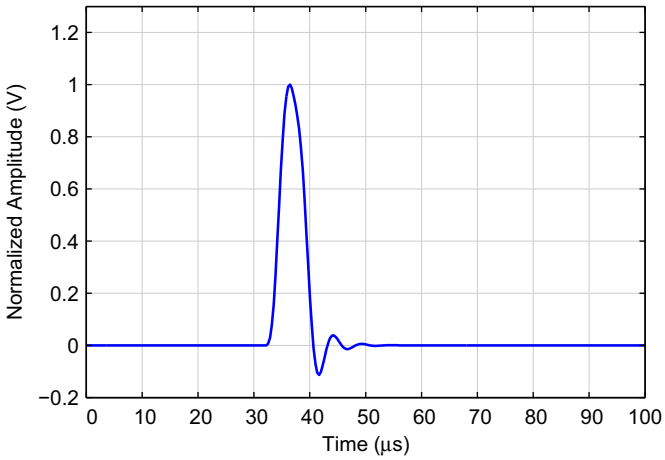


Figure 9-63. Impulse Response

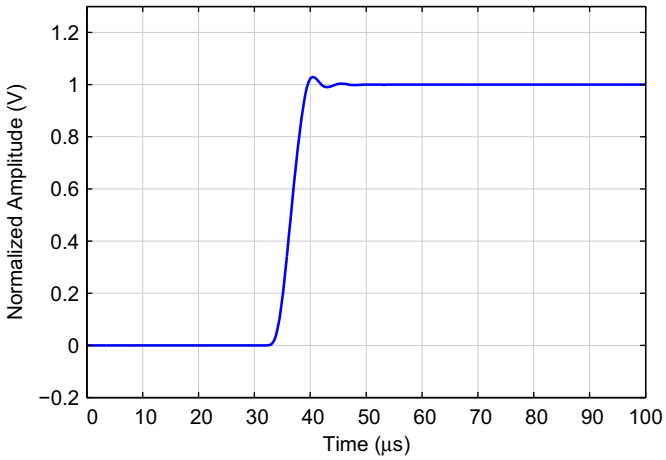


Figure 9-64. Step Response

9.1.13 Combined Filter Response—DSD

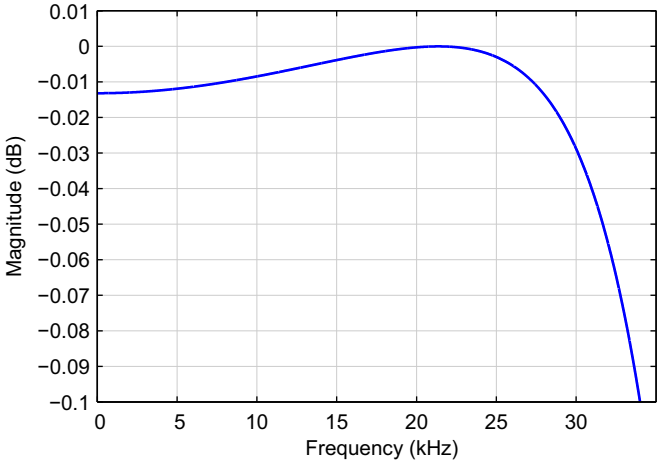


Figure 9-65. Passband Ripple

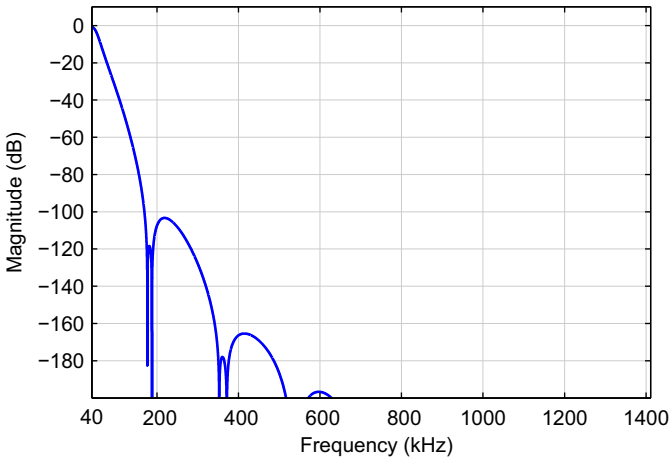


Figure 9-66. Stopband Attenuation

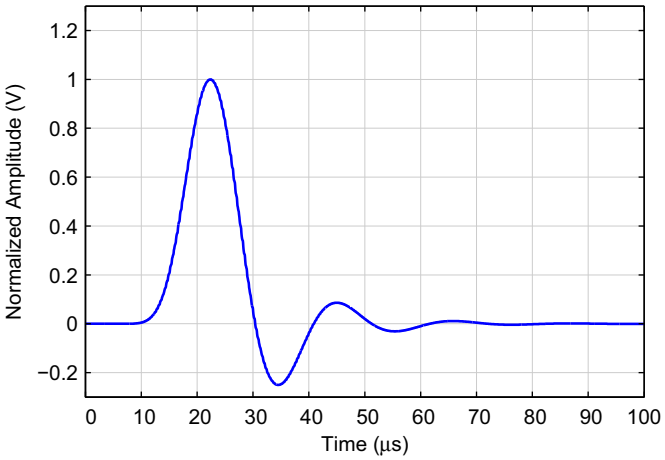


Figure 9-67. Impulse Response

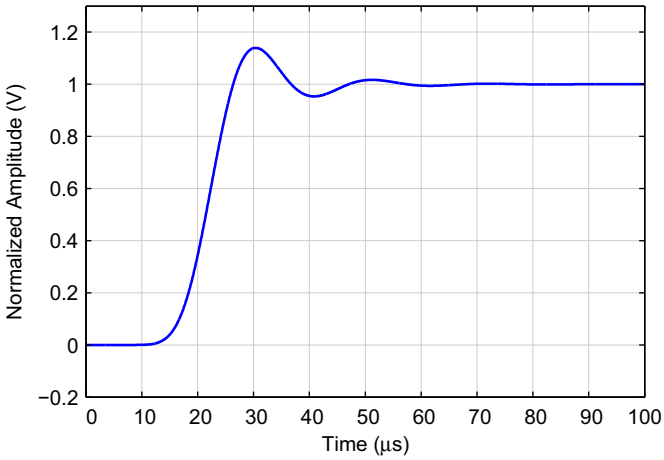


Figure 9-68. Step Response

9.1.14 High-pass Filter and Deemphasis

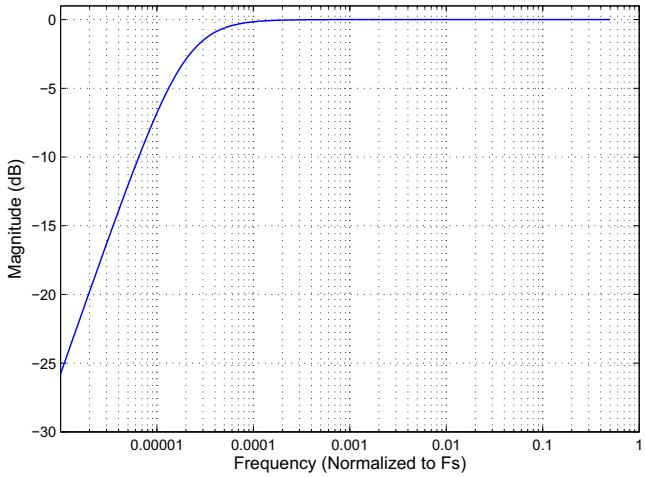


Figure 9-69. High-pass Filter for PCM and DSD Paths

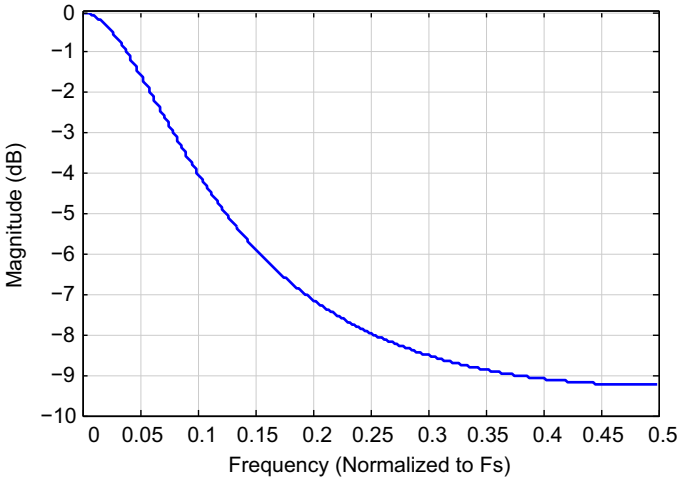


Figure 9-70. Deemphasis

10 Package Dimensions

10.1 40-Pin QFN Package Dimensions

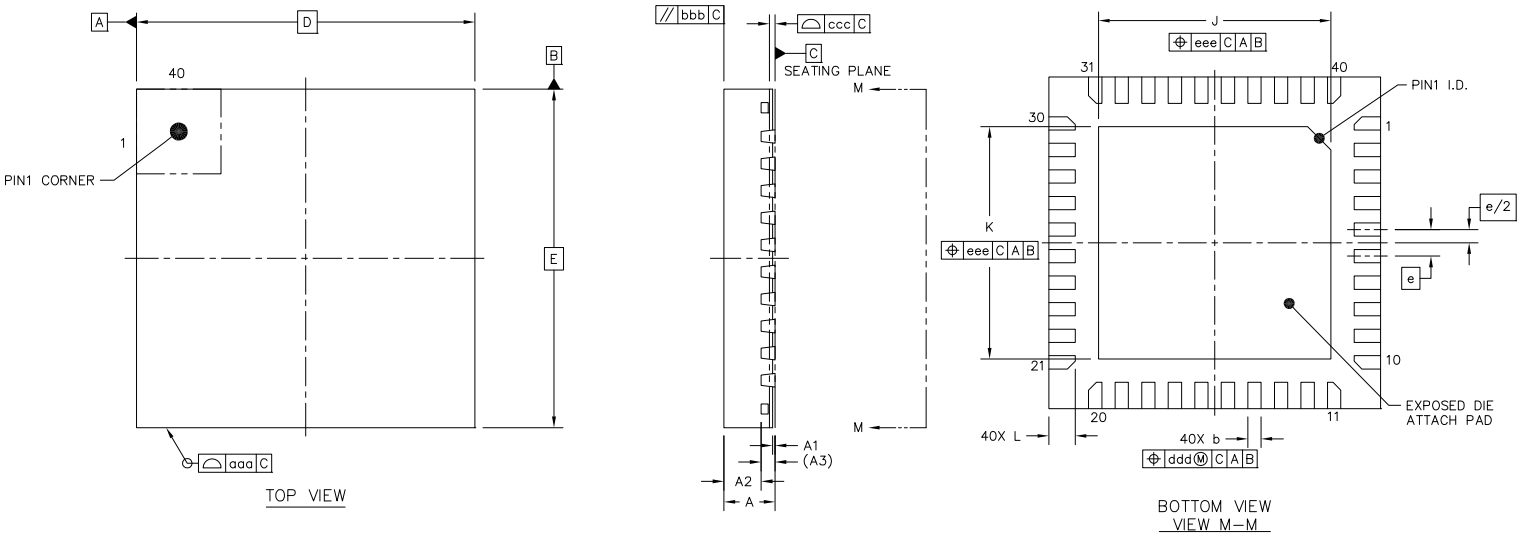


Figure 10-1. 40-Pin QFN Package Drawing

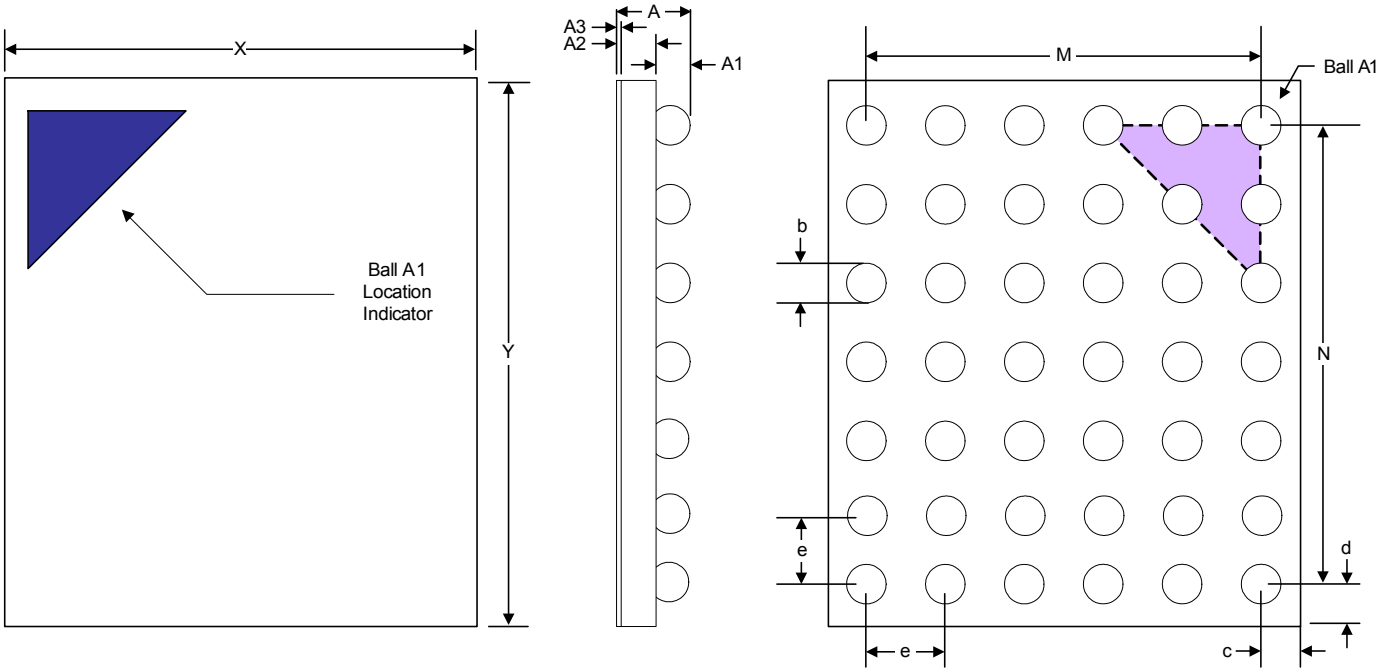
Table 10-1. 40-Pin QFN Package Dimensions

Description		Dim	Millimeters		
			Minimum	Nominal	Maximum
Total thickness		A	0.7	0.75	0.8
Stand off		A1	0	0.035	0.05
Mold thickness		A2	—	0.55	—
L/F thickness		A3		0.203 REF	
Lead width		b	0.15	0.2	0.25
Body size	X	D		5 BSC	
	Y	E		5 BSC	
Lead pitch		e		0.4 BSC	
EP size	X	J	3.4	3.5	3.6
	Y	K	3.4	3.5	3.6
Lead length		L	0.35	0.4	0.45
Package edge tolerance		aaa		0.1	
Mold flatness		bbb		0.1	
Coplanarity		ccc		0.08	
Lead offset		ddd		0.1	
Exposed pad offset		eee		0.1	

Notes:

- Dimensioning and tolerances per ASME Y 14.5M–1995.
- X/Y Dimensions are estimates.
- The Ball 1 location indicator shown above is for illustration purposes only and may not be to scale.
- Dimensioning and tolerances per ASME Y 14.5M–1994.
- Dimension “b” applies to the solder sphere diameter and is measured at the midpoint between the package body and the seating plane.

10.2 42-Ball WLCSP Package Dimensions



Wafer Back Side Side View Bump Side

Notes:
- Controlling dimensions are in millimeters.
- Dimensioning and tolerances per ASME Y 14.5M-1994.
- The Ball A1 position indicator is for illustration purposes only and may not be to scale.
- Dimension “b” applies to the solder sphere diameter and is measured at the midpoint between the package body and the seating plane datum Z.
- Dimension A3 describes the thickness of the backside film.

Figure 10-2. 42-Ball WLCSP Package Drawing

Table 10-2. 42-Ball WLCSP Package Dimensions

Dimension	Millimeters		
	Minimum	Nominal	Maximum
A	0.461	0.491	0.521
A1	0.175	0.190	0.205
A2	0.286	0.301	0.316
A3	—	0.022	—
M	—	2.000	—
N	—	2.400	—
b	0.220	0.270	0.320
c	—	0.354	—
d	—	0.391	—
e	—	0.400	—
X	—	2.707	—
Y	—	3.181	—

Notes: X/Y dimensions are estimates.
- Unless otherwise specified, tolerances are: Linear ±0.05 mm, Angular ±1 deg

11 Thermal Characteristics

Table 11-1. Typical JEDEC Four-Layer, 2s2p Board Thermal Characteristics

Parameter	Symbol	WLCSP	QFN	Units
Junction-to-ambient thermal resistance	θ_{JA}	42.3	32.7	°C/W
Junction-to-board thermal resistance	θ_{JB}	11.1	8.8	°C/W
Junction-to-case thermal resistance	θ_{JC}	0.22	0.92	°C/W
Junction-to-board thermal-characterization parameter	Ψ_{JB}	11.0	8.8	°C/W
Junction-to-package-top thermal-characterization parameter	Ψ_{JT}	0.09	0.23	°C/W

Notes:
- Natural convection at the maximum recommended operating temperature T_A (see Table 3-2)
- Four-layer, 2s2p PCB as specified by JESD51-9 and JESD51-11; dimensions: 101.5 x 114.5 x 1.6 mm
- Thermal parameters as defined by JESD51-12

12 Ordering Information

Table 12-1. Ordering Information

Product	Description	Package	Halogen Free	Pb Free	Grade	Temperature Range	Container	Order Number
CS4399	130-dB, 32-Bit High-Performance DAC	42-ball WLCSP	Yes	Yes	Commercial	–10°C to +70°C	Tape and Reel	CS4399-CWZR
		40-pin QFN	Yes	Yes	Commercial	–10°C to +70°C	Tray	CS4399-CNZ
							Tape and Reel	CS4399-CNZR

13 References

- NXP Semiconductors, *The I²C-Bus Specification and User Manual (UM10204)*. http://www.nxp.com/

14 Revision History

Table 14-1. Revision History

Revision	Changes
F1 DEC ‘16	Initial release

Important: Please check with your Cirrus Logic sales representative to confirm that you are using the latest revision of this document and to determine whether there are errata associated with this device.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com.