100 kSps, 16-bit, High-throughput ΔΣ ADC
Evaluation Board

Features

- Analog Input Channels to the CS5571 ADC
- Pre-configured to require a minimum number of external connections to your data acquisition system.
- All functionality accessible through the connector interface and board-level options.
- On-board 4.096 V Reference
- Pre-configured for Master mode SPI™ communication to a data capture system.

General Description

The CDB5571 is a versatile tool designed for evaluating the functionality and performance of the CS5571 ADC (Analog-to-Digital Converter). The SPI serial port on the CDB5571 evaluation board is configured in Master mode and will start transmitting data after power-up upon reset. This evaluation board is designed to connect to your data capture system or will interface to the CapturePlus II data acquisition system available from Cirrus Logic.

The CS5571 delta-sigma ADC produces fully settled conversions to full specified accuracy at 100 kSps. This ability to produce fully settled conversions for every sample makes it suitable for converting multiplexed input signals. To help evaluate this feature, the CDB5571 includes two single-ended analog inputs multiplexed into the CS5571. The multiplexer can be switched at the CS5571 ADC sample speed and the ADC will produce fully settled conversion data for each input channel.

All evaluation board functionality for evaluating the CS5571 ADC is accessed through the connector interface and board-level options.


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CDB5571 Evaluation Board
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1. INTRODUCTION

The CDB5571 evaluation board is a platform for evaluating the CS5571 ADC performance. The evaluation board is designed to connect to the SPI serial port of a processor or data capture system or will interface directly to the CapturePlus II data acquisition system available from Cirrus Logic. The CapturePlus II data acquisition system is a powerful integrated hardware/software tool designed to fully exercise the CDB5571 and other Cirrus Logic evaluation boards.

The CDB5571 evaluation board is designed to simplify the hardware setup required to evaluate the CS5571. Interfacing the CDB5571 evaluation board to a user-supplied data capture system can be as simple as connecting the SPI port and using the CDB5571 default hardware configuration. In this configuration, simply press the Reset switch on the CDB5571 and it will automatically begin transmitting data to the data capture system.

All evaluation board functionality for evaluating the CS5571 ADC is accessed through the connector interface and board-level options.

The CS5571 delta-sigma ADC produces fully settled conversions to full specified accuracy at 100 kSps. The ability to produce fully settled conversions for every sample makes it suitable for converting multiplexed input signals. To help evaluate this feature, the CDB5571 includes two single-ended analog inputs multiplexed into the CS5571. The multiplexer can be switched at the CS5571 ADC sample speed and the ADC will produce fully settled conversion data for each input channel.

For detailed information on the CS5571 ADC, please reference data sheet DS768 at www.cirrus.com.
1.1 Overview

The CDB5571 evaluation board has both analog and digital circuit sections. The analog section consists of the CS5571 ADC, two analog input signal buffers, controlled through a multiplexer, that condition the signals into the ADC, and a precision 4.096 V reference. The digital section consists of board operation configuration control signals, reset circuitry, an SPI™ serial port, a jumper connection for initiating ADC calibration, and an EEPROM for evaluation board identification.

The evaluation board operates from +2.5V, -2.5V, +3.3V and communicates through an SPI™ serial port.

Figure 1 illustrates the CDB5571 block diagram.

![CDB5571 Block Diagram](image)

Figure 1. CDB5571 Block Diagram
2. QUICK START

The CDB5571 evaluation board is designed to interface with a data acquisition system. To connect and configure the CDB5571 perform the following initialization procedure:

1. Verify that the power supplies are off.
2. Connect the power supplies to the CDB5571 as shown in Table 1 on page 6.
3. Verify that the power is off to the analog input signal & control signal sources.
4. Connect the analog input signal source to the evaluation board per Table 2 on page 6. Verify from Table 4 on page 8 that the analog input channel selected is IN_A.
5. Configure the CDB5571 by connecting the control signal sources to the evaluation board as shown in Table 3 on page 7. Apply logic-level inputs as required to override the resistor pull-ups/pull-downs.
6. Make connections to the SPI™ serial port connector as shown in Table 5 on page 8. The CS5571 ADC serial port is configured by default to operate in the SSC (Synchronous Self Clocking) mode. Refer to the CS5571 data sheet for more information on serial communication modes and signal timing.
7. Turn on the power supplies to the evaluation board.
8. Apply power to the signal source.
9. Press the Reset switch on the evaluation board.
10. The CS5571 ADC's SPI™ serial port should now be communicating data.

Figure 2. CDB5571 Board Layout

NOTES:
1. Shaded boxes marked with "OPT. CONFIG." are not necessary for operation in an end user product.
2. Calibration function has been removed from the device but still appears on the PCB. J2 must be shorted (grounded) for proper operation. See Appendix E for details.
3. HARDWARE DESCRIPTION

3.1 Absolute Maximum Ratings

Observe the following limits to ensure the CDB5571 component ratings are not exceeded.

- **CS5571**
  - The absolute maximum supply voltage that can be applied to the +3.3V power supply connection is +3.6V.
  - The absolute maximum power supply voltage that can be applied between pins VL and V1- is 6.1 V.

- **CS3004**
  - The absolute maximum power supply voltage that can be applied between the +2.5V and -2.5V power supply connections is +5.5V.

3.2 Power Supply

Power supply connections and requirements are specified in Table 1. below.

**Table 1. Power Supply Connections**

<table>
<thead>
<tr>
<th>Power Supply Requirement</th>
<th>Power Supply Connection</th>
<th>Associated Ground Return</th>
<th>Associated Test Points</th>
</tr>
</thead>
<tbody>
<tr>
<td>+2.5 V DC, ±5%, &lt;50 mA</td>
<td>E5</td>
<td>E3</td>
<td>TP2, TP1 (GND)</td>
</tr>
<tr>
<td>-2.5 V DC, ±5%, &lt;50 mA</td>
<td>E9</td>
<td>E7</td>
<td>TP4, TP3 (GND)</td>
</tr>
<tr>
<td>+3.3 V DC, ±5%, &lt;50 mA</td>
<td>E16</td>
<td>E13</td>
<td>TP6, TP5 (GND)</td>
</tr>
</tbody>
</table>

Important: It is recommended that all power supplies be isolated from utility ground to prevent the introduction of a ground loop. One ground connection may already exist through the serial port connection to utility ground. Using the Cirrus Logic CapturePlus II system simplifies making connections to the CDB5571 by providing electrical isolation between the two.

Using twisted/shielded wire will reduce electrical noise induced onto the power supply cables.

Power supplies are to be adequately regulated and sufficiently low noise to meet the application requirements.

3.3 Analog Section

3.3.1 Analog Input Buffers

The analog input signal connections to the input buffers are made at the IN_A and IN_B connectors, as specified in Table 2.

**Table 2. Analog Input Connections**

<table>
<thead>
<tr>
<th>Channel</th>
<th>Analog Input Connection</th>
<th>Input Signal Voltage Range</th>
<th>Impedance</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN_A</td>
<td>J10</td>
<td>-2.048 V to +2.048 V</td>
<td>50 Ohms</td>
</tr>
<tr>
<td>IN_B</td>
<td>J11</td>
<td>-2.048 V to +2.048 V</td>
<td>50 Ohms</td>
</tr>
</tbody>
</table>

There are two analog input channels on the evaluation board. Each analog input channel consists of a low-noise amplifier configured as a unity gain non-inverting buffer. The buffers utilize a Cirrus Logic CS3004 precision, low-noise, low-voltage, dual opamp. These op-amps enable both the inputs and outputs of the analog input buffer to operate virtually rail to rail. The channel input impedance is 50 Ohms.
The analog inputs are designed for connections to single-ended input signals referenced to ground. The usable input voltage range is -2.048 V to +2.048 V. The theoretical input frequency range of the CS5571 is from DC to the Nyquist frequency of 50 kHz. The analog input buffer amplifiers are configured for a cut-off frequency of 16.8 kHz to band-limit noise into the ADC. Changing the cutoff frequency will change the noise bandwidth accordingly.

### 3.3.2 Multiplexer

Analog input channel selection is controlled through the multiplexer. The multiplexer is configured with a pull-down resistor on the MUX control line to enable input channel labeled "INPUT A" by default. To select channel B, apply 3.3 V to the multiplexer input control line (MUX). Signal levels for controlling the multiplexer that selects between analog input channels A and B is shown in Table 3.

#### Table 3. Analog Input Channel Selection

<table>
<thead>
<tr>
<th>Multiplexer Control Input (MUX)</th>
<th>Input Channel Enabled</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 V</td>
<td>A</td>
</tr>
<tr>
<td>3.3 V</td>
<td>B</td>
</tr>
</tbody>
</table>

During multiplexing, the maximum sample rate for each channel is half that of the ADC’s maximum sample rate. Additionally, the Nyquist frequency for each channel is half of the ADC’s Nyquist frequency.

### 3.3.3 ADC Reset

The CS5571 ADC makes use of an externally generated power-on reset. Therefore, after power is applied to the ADC, the reset pin must be driven low then released. Pressing the Reset button generates a reset cycle. A reset cycle can be generated at any time during ADC operation. The ADC RST pin (active low) is held inactive through a pull-up resistor.

### 3.3.4 Voltage Reference

The voltage reference IC provided generates a 4.096 V precision reference.

### 3.3.5 ADC Reference Frequency

The reference frequency for the CS5571 ADC is provided by a 16.000 MHz oscillator.
3.4 Digital Section

3.4.1 Hardware Configuration

The CDB5571 evaluation board hardware comes pre-configured so the only connection required between it and a data acquisition system is the serial port connection.

The hardware setup is reconfigurable through the hardware control interface connectors. Configure the evaluation board by setting the appropriate control line to the appropriate logic level.

<table>
<thead>
<tr>
<th>Function</th>
<th>Default Level</th>
<th>Label</th>
<th>Connector</th>
<th>Test Point</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Channel Select</td>
<td>IN_A = Selected (Low)</td>
<td>MUX</td>
<td>J6, Pin 16</td>
<td>J3, Pin 2</td>
</tr>
<tr>
<td>Analog Input Buffers</td>
<td>Buffers = Enabled (High)</td>
<td>BUFEN</td>
<td>J1</td>
<td>J3, Pin 1</td>
</tr>
<tr>
<td>Serial Port Mode</td>
<td>Sync. Self Clock = Enabled (High)</td>
<td>SMODE</td>
<td>J6, Pin 12</td>
<td>J3, Pin 3</td>
</tr>
<tr>
<td>Data Ready Flag</td>
<td>Data Ready When Set (Low)</td>
<td>RDY</td>
<td>J8, Pin 10</td>
<td>J3, Pin 4</td>
</tr>
<tr>
<td>Reset</td>
<td>Reset = Inactive (High)</td>
<td>RST</td>
<td>J6, Pin 6; S1</td>
<td>J3, Pin 6</td>
</tr>
<tr>
<td>Bipolar / Unipolar Mode</td>
<td>Bipolar = Enabled (High)</td>
<td>BP / UP</td>
<td>J6, Pin 2</td>
<td>J3, Pin 8</td>
</tr>
<tr>
<td>Digital Filter Dither</td>
<td>Dither = Enabled (High)</td>
<td>DITHER</td>
<td>J6, Pin 4</td>
<td>J3, Pin 9</td>
</tr>
<tr>
<td>Serial Port Communication</td>
<td>Chip Select = Enabled (Low)</td>
<td>CS</td>
<td>J8, Pin 2</td>
<td>E23</td>
</tr>
<tr>
<td>Data Conversion Mode</td>
<td>Continuous Conversion = Active (Low)</td>
<td>CONV</td>
<td>J8, Pin 12</td>
<td>E23</td>
</tr>
</tbody>
</table>

3.4.2 SPI™ Serial Port Communications

The CS5571 ADC communications port features an SPI™ serial port. It can be configured for SSC mode (Master) or SEC mode (Slave) mode as shown in Table 4. Test points are provided to monitor serial communications.

Connections to the serial interface are made according to the following table.

<table>
<thead>
<tr>
<th>Function</th>
<th>Label</th>
<th>Connector</th>
<th>Test Point</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip Select</td>
<td>CS</td>
<td>J8, Pin 2</td>
<td>E23</td>
</tr>
<tr>
<td>Serial Data Input</td>
<td>SDI</td>
<td>J8, Pin 4</td>
<td>E24</td>
</tr>
<tr>
<td>Serial Data Output</td>
<td>SDO</td>
<td>J8, Pin 6</td>
<td>E25</td>
</tr>
<tr>
<td>Serial Clock</td>
<td>SCLK</td>
<td>J8, Pin 8</td>
<td>E26</td>
</tr>
</tbody>
</table>
APPENDIX A. MAXIMIZING THE PERFORMANCE OF THE CS5571

A.1 PCB Layout Considerations

- Keep the signal path short between the CS5571 ADC input capacitors C37, C44 and the ADC input pin to minimize trace inductance.

- The analog input buffer amplifiers and ADC input buffer capacitors are placed before the multiplexer. Placing the buffer amplifiers before the multiplexer allows the amplifiers driving the ADC buffer capacitors to be fully settled when sampled by the ADC. Therefore, the multiplexer must be of a low on-resistance type to prevent distortion or latency issues.

- Power supply noise is a major design consideration and the power supplies need adequate bypassing and bulk capacitance.

- When operating the ADC from +2.5 V and -2.5 V split supplies, place the power supply & buffer amplifier bypass capacitor ground connections close together.

- Keep all ground connections on each differential buffer amplifier as close to the device as possible to avoid introducing differential noise through high-impedance connections.

- Keep trace lengths short between the ADC and the voltage reference IC negative supply pins.

- Route the oscillator output away from analog circuitry.

- Use a solid ground plane in the PCB layout.

- Provide adequate separation between analog and digital signals.

- To minimize distortion within the analog signal path, consider using components with smaller voltage dependencies.

- Minimize ADC digital output edge transition current loading.

A.2 Hardware Considerations

At a system level, use shielded cable for interconnects. Keep interconnect cable lengths as short as possible. Route analog and digital signals connecting to the PCB away from each other.
CIRRUS LOGIC  
CDB5571_REV_A4.PL  

**APPENDIX B. BILL OF MATERIALS**

<table>
<thead>
<tr>
<th>Item</th>
<th>Cirrus P/N</th>
<th>Rev</th>
<th>Description</th>
<th>Qty</th>
<th>Reference Designator</th>
<th>MFG</th>
<th>MFG P/N</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>001-03713-Z1</td>
<td>A</td>
<td>CAP 100pF ±10% 50V X7R NPb 0805</td>
<td>2</td>
<td>C1 C2</td>
<td>KEMET</td>
<td>C0805C102X5RAC</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>001-04345-Z1</td>
<td>A</td>
<td>CAP 10µF ±5% 16V NPb CASE A</td>
<td>3</td>
<td>C6 C7 C13</td>
<td>PANASONIC</td>
<td>EEC1C5100RA</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>001-03867-Z1</td>
<td>A</td>
<td>CAP 100µF ±5% 16V X7R NPb 1206</td>
<td>2</td>
<td>C24 C45</td>
<td>KEMET</td>
<td>C1206C104X5RAC</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>001-05897-Z1</td>
<td>A</td>
<td>DIODE ESR 6.8V 0603 NPb DO-214AA</td>
<td>3</td>
<td>D1 D2 D3</td>
<td>LITTLEFUSE</td>
<td>PSMB063.8A</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>001-00011-Z1</td>
<td>A</td>
<td>DIODE SCHOTTKY BAR 30V 2A NPb SOT23</td>
<td>1</td>
<td>D4</td>
<td>PHILIPS</td>
<td>BAT54</td>
<td></td>
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<tr>
<td>6</td>
<td>000-00025-Z1</td>
<td>A</td>
<td>NO POP 040 PAD 040 NPb TH</td>
<td>0</td>
<td>E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 E11 E12 E13 E14 E15 E16 E17 E18 E19 E20 E21 E22 E23 E24 E25 E26 E27 E28</td>
<td>NO POP</td>
<td>NP-PAD-040</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>115-00052-Z1</td>
<td>A</td>
<td>HDR 2x1 ML 1&quot;CTR 093 GLD NPb</td>
<td>0</td>
<td>J1 J2</td>
<td>SAMTEC</td>
<td>TSW-102-2-6-G-S</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>115-00051-Z1</td>
<td>A</td>
<td>HDR 10x1 FLM 1&quot; 093 GLD NPb TH</td>
<td>0</td>
<td>J3</td>
<td>SAMTEC</td>
<td>SSW-110-01-G-S</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>115-00050-Z1</td>
<td>A</td>
<td>HDR 8x2 093BD RML 1&quot; .331&quot; NPb NPb</td>
<td>1</td>
<td>J4</td>
<td>SAMTEC</td>
<td>SSW-105-01-G-D</td>
<td></td>
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<tr>
<td>10</td>
<td>115-00049-Z1</td>
<td>A</td>
<td>HDR 5x2 093BD RML 1&quot; .331&quot; NPb NPb</td>
<td>1</td>
<td>J5</td>
<td>SAMTEC</td>
<td>SSW-105-01-G-D</td>
<td></td>
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<tr>
<td>11</td>
<td>115-00048-Z1</td>
<td>A</td>
<td>HDR 6x2 093BD RML 1&quot; .331&quot; NPb NPb</td>
<td>1</td>
<td>J6</td>
<td>SAMTEC</td>
<td>SSW-105-01-G-D</td>
<td></td>
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<td>12</td>
<td>130-00026-Z1</td>
<td>A</td>
<td>HDR 30x1 093BD RML 1&quot; .331&quot; NPb NPb</td>
<td>2</td>
<td>J10 J11</td>
<td>SAMTEC</td>
<td>SSW-105-01-G-D</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>120-00057-Z1</td>
<td>A</td>
<td>SWT SPST 130G 01 7mm TACT ESD NPb</td>
<td>1</td>
<td>S1</td>
<td>ITT INDUSTRIES</td>
<td>PTS645TL70</td>
<td>INSTALL AFTER WASH PROCESS</td>
</tr>
<tr>
<td>14</td>
<td>110-00045-Z1</td>
<td>A</td>
<td>CON TEST PT 1&quot;CTR TIN PLAT NPb BLK</td>
<td>3</td>
<td>TP1 TP3 TP5</td>
<td>KEYSTONE</td>
<td>5001</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>110-00024-Z1</td>
<td>A</td>
<td>CON TEST PT 1&quot; TIN PLT RED NPb TH</td>
<td>2</td>
<td>TP2 TP6</td>
<td>KEYSTONE</td>
<td>5002</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>110-00025-Z1</td>
<td>A</td>
<td>CON TEST PT 1&quot; TIN PLATE WHT NPb</td>
<td>1</td>
<td>TP4</td>
<td>KEYSTONE</td>
<td>5002</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>060-00387-Z1</td>
<td>A</td>
<td>IC LNR PREC VREF 4.096Vout NPb SO8</td>
<td>1</td>
<td>U1</td>
<td>MAXIM</td>
<td>MAXIMAX1284A1</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>065-00239-Z1</td>
<td>A</td>
<td>IC CRUS ADC 10k5ps 16p NPb SSM24</td>
<td>1</td>
<td>U2</td>
<td>CIRRUS LOGIC</td>
<td>CS55571TS280</td>
<td>ECO521, ECO542</td>
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<tr>
<td>19</td>
<td>060-00352-Z1</td>
<td>A</td>
<td>IC LNR ANA SW 40MH SPDT NPb MCP101</td>
<td>1</td>
<td>U4</td>
<td>MAXIM</td>
<td>MAXIMAX4605UB+</td>
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<tr>
<td>20</td>
<td>060-00219-Z1</td>
<td>A</td>
<td>IC CRUS PREC DL VO AMP NPb SOP10</td>
<td>1</td>
<td>U5</td>
<td>CIRRUS LOGIC</td>
<td>CS5004-F527/A0</td>
<td></td>
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<tr>
<td>21</td>
<td>060-00398-Z1</td>
<td>A</td>
<td>IC LNR DIFF COMPPS 5.25V NPb SOIC8</td>
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<td>U6</td>
<td>TEXAS INSTRUMENTS</td>
<td>TL122D</td>
<td></td>
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<tr>
<td>22</td>
<td>062-00064-Z1</td>
<td>A</td>
<td>IC PGMM SPLEEPROM 8X8 2MH NPb SO8</td>
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<td>U7</td>
<td>MICROCHIP</td>
<td>25LC640-USN</td>
<td></td>
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<td>23</td>
<td>102-00097-Z1</td>
<td>A</td>
<td>OSC 16MHz 50ppm 3.3V NPb SMD 3x5</td>
<td>1</td>
<td>Y1</td>
<td>ASBRACON</td>
<td>ASY14L-16.000MHZ-EC-T</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>603-00284-Z1</td>
<td>A</td>
<td>ASSY DYG CDB5571-1 Npb</td>
<td>REF</td>
<td>CIRRUS LOGIC</td>
<td>603-00284-Z1</td>
<td></td>
<td></td>
</tr>
<tr>
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APPENDIX C. SCHEMATICS

Figure 3. Schematic - Block Diagram

- DUT
- MUX
- SINGLE-ENDED_BUFF_A
- SINGLE-ENDED_BUFF_B
- RESET SWITCH
- CALIBRATE SWITCH
- 18MHz
- 4.096V
- 1 Top signal
- 2 AGND
- 3 +2.5V, +1.3V
- 4 Bottom signal
- Power Supplies: +2.5V, -2.5V, +3.3V
- PCB Layers
- DUT and communications port
- Logic inputs and outputs
- MUX, A, B, etc.
Figure 4. Schematic - Power Supplies
Figure 5. Schematic - Input Buffers and Multiplexer
Figure 7. Schematic - Configuration & Misc.
APPENDIX D. LAYER PLOTS

Figure 8. Top Silkscreen

Calibration function has been removed from the device but still appears on the PCB. J2 must be shorted (grounded) for proper operation. See Appendix E for details.
Figure 10. Top Routing
Figure 11. Ground Plane
Figure 13. Bottom Solder Mask
Figure 14. Bottom Silkscreen
APPENDIX E. CALIBRATION FUNCTION
The calibration function has been removed from the CS5571. All references to calibration have been re-
moved from this document. However, calibration still appears on the PCB. A jumper must be added to J2 for proper operation.
REVISION HISTORY

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<th>Revision</th>
<th>Date</th>
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<td>DB1</td>
<td>APR 2007</td>
<td>Initial Release.</td>
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<td>DB2</td>
<td>AUG 2007</td>
<td>Added 3.3.2 Multiplexer section.</td>
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<td>DB3</td>
<td>DEC 2007</td>
<td>Updated schematic to reflect new silicon revision.</td>
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<tr>
<td>DB4</td>
<td>OCT 2009</td>
<td>Removed calibration function / added Appendix E.</td>
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Contacting Cirrus Logic Support
For all product questions and inquiries contact a Cirrus Logic Sales Representative. To find the one nearest to you go to www.cirrus.com

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