1. Features and Benefits

- 3-phase BLDC gate driver
  - ❑ Level shifting between MCU PWM outputs and 3 external half-bridges
  - ❑ Compatible with 3.3V-5V microcontrollers
- Supporting different driver strength
  - ❑ MLX83203: 1.00A gate drivers
  - ❑ MLX83202: 0.33A gate drivers
- Supported supply voltage range
  - ❑ Absolute maximum rating: 45V
  - ❑ Operating range: 4.5V-28V
  - ❑ 12V-28V Battery systems
  - ❑ Automotive qualified for 12V
  - ❑ Sleep mode with current <30µA
- Two charge pump configuration modes for
  - ❑ Low voltage operation
  - ❑ Reverse polarity N-FET protection
- High-side gate drivers with bootstrap circuits
  - ❑ Integrated 12V voltage regulator
  - ❑ Supports 6x 350nC N-FETs at 20kHz PWM
  - ❑ Supports 100% PWM operation
- Integrated current sense amplifier
  - ❑ Low offset and low offset drift
  - ❑ Fast settling time < 1µs
  - ❑ Programmable gain: 8x-48x
- Extensive diagnostics
  - ❑ Under/over voltage detection
  - ❑ Over temperature warning
  - ❑ Programmable V_{DS} monitoring
  - ❑ V_{GS} monitoring
- Serial, PWM diagnostics interface
  - ❑ Configurable diagnostics
  - ❑ Full diagnostic feedback
- Customer configurable EEPROM
  - ❑ Driver configuration
  - ❑ Diagnostics configuration
- Small package
  - ❑ 32-pin QFN-EP
  - ❑ Wettable flanks
- AEC-Q100 qualified

2. Application Examples

- Automotive 12V BLDC applications
  - ❑ Water pump / Oil pump / Fuel pump
  - ❑ Engine Cooling fan
  - ❑ HVAC blower / compressor
- Industrial BLDC motor drivers up to 28V
  - ❑ Pumps
  - ❑ Fans
  - ❑ Blowers / compressors

3. Ordering Information

Product	Temperature	Package	Option Code	Packing Form
MLX83203	K (-40°C to 125°C)	LW (QFN32-EP 5x5mm wettable flanks)	DDA-000	RE (Reel)
MLX83202	K (-40°C to 125°C)	LW (QFN32-EP 5x5mm wettable flanks)	DDA-000	RE (Reel)

Ordering Example: *"MLX83203KLW-DDA-000-RE".*

4. Functional Diagram

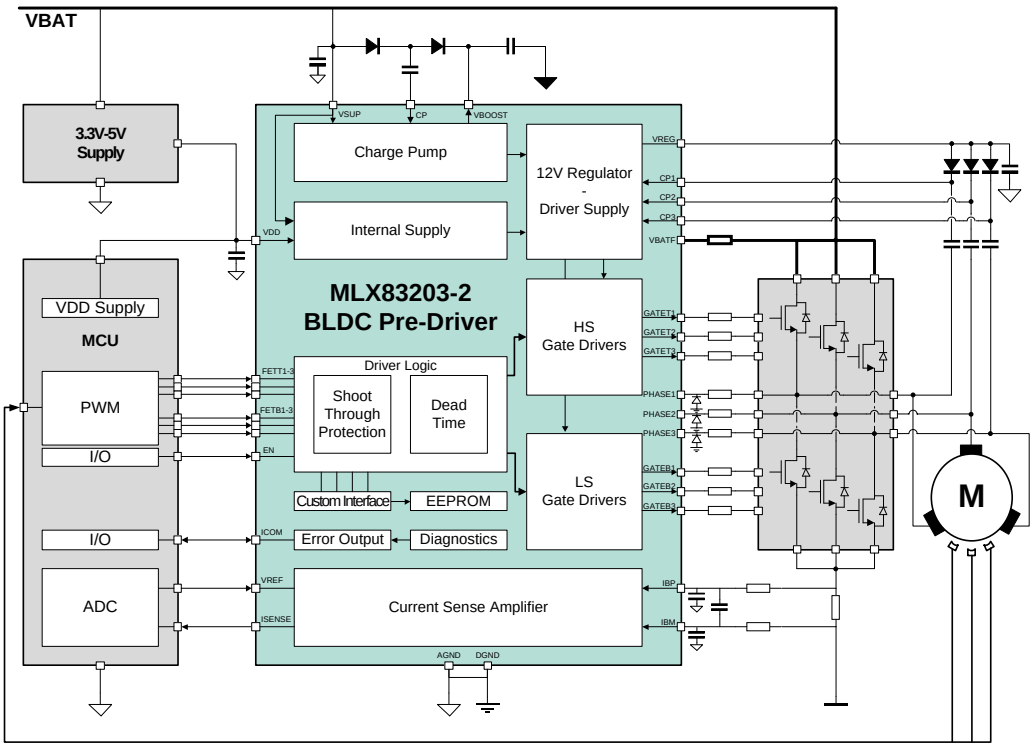

Figure 4-1 Typical application diagram

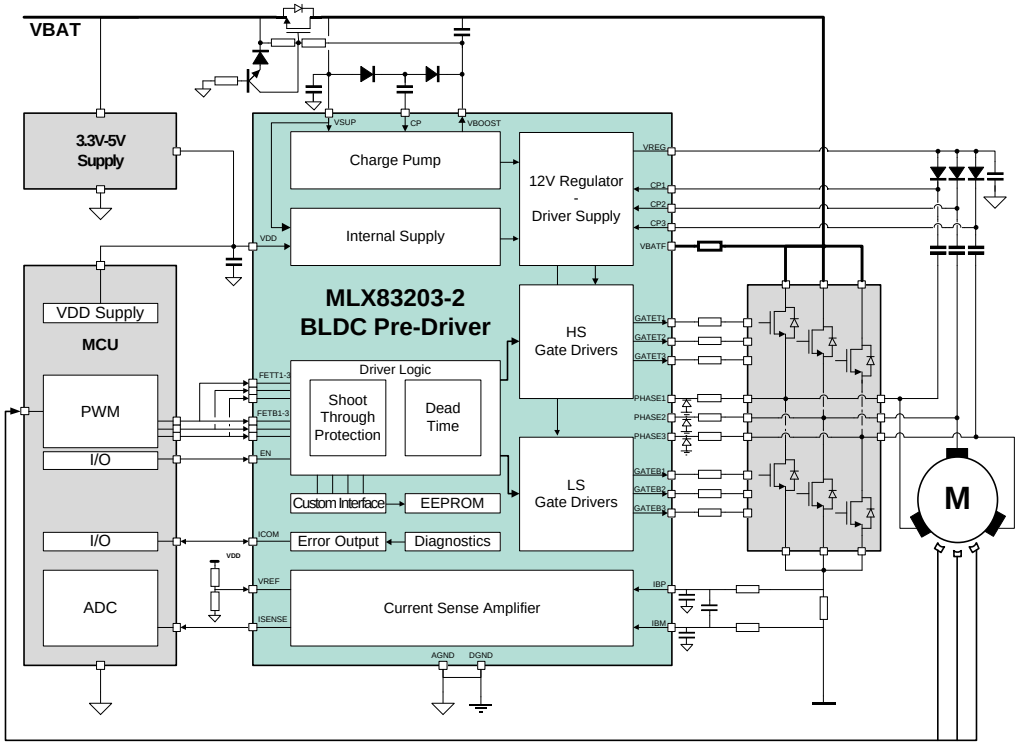

Figure 4-2 Alternative application diagram with reverse polarity N-FET

5. General Description

The MLX83203-2 is a three phase pre-driver (also called ‘bridge’ or ‘gate’ driver) IC with integrated current sense amplifier. This device is used to drive brushless DC motors in combination with a microcontroller and six discrete power N-FETs.

For the high power applications, the MLX83203 provides powerful gate drivers of 1A typical. The MLX83202 has reduced gate drive strength of 300mA and targets mid power applications.

Both devices are able to control six external N-FETs in the supply range from 4.5V to 28V, by means of the integrated charge pump. The high side gate drivers are supplied via bootstrap circuits. The trickle charge pump allows 100% PWM operation despite the use of bootstrap capacitors. The bootstrap voltage regulator is optimized for gate charges up to 350nC per FET at 20 kHz PWM.

The device comprises various monitoring and protection functions, including under voltage and over voltage detection at multiple internal voltage nodes, over temperature detection, drain-source and gate-source voltage monitoring of the external N-FETs. In case of fault detection, the ICOM diagnostics interface will inform the microcontroller with a PWM signal, whose duty cycle indicates the nature of the error.

An integrated fast, high-bandwidth, low offset current sense amplifier allows for precise torque control, with programmable gain selection.

The MLX83203-2 provides an EEPROM for configurability, avoiding the need for a high pin-count package. The configuration allows the customer to optimize the pre-driver’s operation for different applications.

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7. Pin Configuration & Definition

7.1. Pin Configuration

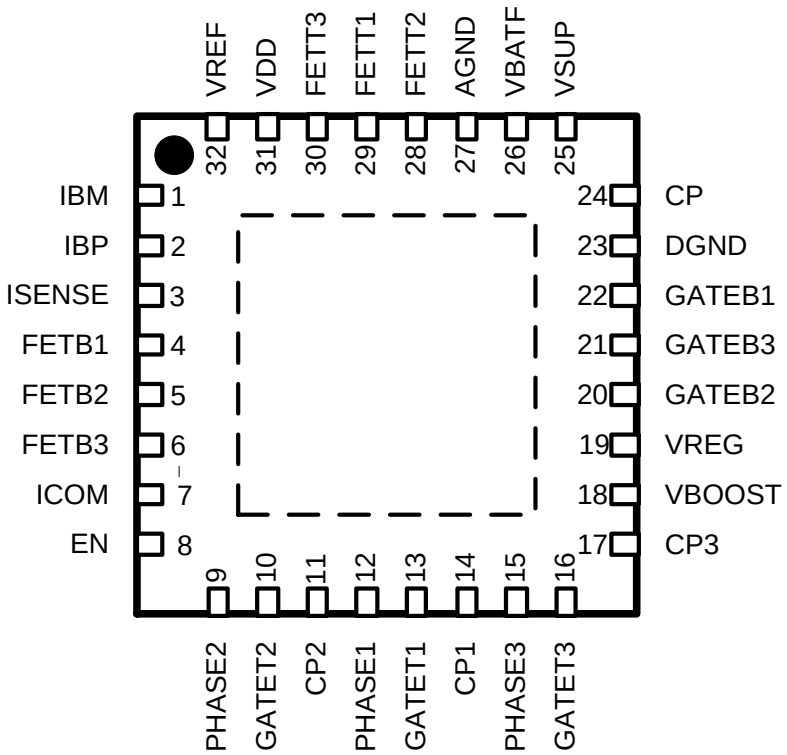

Figure 7-1 Pin configuration

7.2. Pin Definition

Pin #	Name	Description
1	IBM	Current sense amplifier negative input
2	IBP	Current sense amplifier positive input
3	ISENSE	Current sense amplifier output
4	FETB1	Low-side FET1 PWM control input (active low) MISO output for SPI
5	FETB2	Low-side FET2 PWM control input (active low) CLK input for SPI
6	FETB3	Low-side FET3 PWM control input (active low) MOSI input for SPI
7	ICOM	Bidirectional, serial diagnostics interface CSB input for SPI
8	EN	Enable input for gate driver outputs (active high)
9	PHASE2	Motor phase 2
10	GATET2	High-side FET2 gate driver output

11	CP2	High-side FET2 bootstrap capacitor
12	PHASE1	Motor phase 1
13	GATET1	High-side FET1 gate driver output
14	CP1	High-side FET1 bootstrap capacitor
15	PHASE3	Motor phase 3
16	GATET3	High-side FET3 gate driver output
17	CP3	High-side FET3 bootstrap capacitor
18	VBOOST	Charge pump boosted supply output
19	VREG	Driver supply output for bootstrap capacitors
20	GATEB2	Low-side FET2 gate driver output
21	GATEB3	Low-side FET3 gate driver output
22	GATEB1	Low-side FET1 gate driver output
23	DGND	Driver ground
24	CP	Charge pump floating capacitor
25	VSUP	Power supply input (Battery input)
26	VBATF	Battery voltage connection for VDS-monitoring
27	AGND	Analog ground
28	FETT2	High-side FET2 PWM control input (active high)
29	FETT1	High-side FET1 PWM control input (active high)
30	FETT3	High-side FET3 PWM control input (active high)
31	VDD	Digital supply for IO’s and current sense amplifier
32	VREF	Current sense amplifier reference input
33	PAD	Exposed pad

Table 7-1 Pin definition

8. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Power supply voltage	V_{VSUP}, V_{BATF}	-0.3	-	45	V	t < 500ms (during load dump)
Power supply voltage	V_{VSUP}, V_{BATF}	-0.3	-	28	V	Permanent (functional)
VBATF voltage	V_{BATF}	-0.3		V_{SUP}+1.4	V	For any IC-version before DDA
Negative input current	I_{VSUP}	-15	-	-	mA	
Negative input current	I_{VBATF}	-10	-	-	mA	Defines with max. reverse polarity voltage the R_{VBATF}
Digital supply voltage	V_{VDD}	-0.3	-	5.5	V	
Analog input voltage	V_{VREF}, V_{IBM}, V_{IBF}	-0.3	-	V_{DD}+0.3	V	
Analog output voltage	V_{ISENSE}	-0.3	-	V_{DD}+0.3	V	
Digital input voltage	V_{FETBx}, V_{FETTx}, V_{EN}	-0.3	-	V_{DD}+0.3	V	
Digital input current		-10	-	10	mA	
Digital output voltage	V_{ICOM}	-0.3	-	V_{DD}+0.3	V	
Output voltage	V_{GATEBx}, V_{REG}	-0.3	-	17	V	
Output voltage	V_{GATETx}	-0.3	-	V_{REG}+35	V	
Input voltage on CPx pins	V_{CPx}	-0.3	-	V_{REG}+35	V	
Input voltage on PHASEx pins	V_{PHASEx}	-0.7	-	45	V	
Maximum latch-up free current at any pin	I_{LATCH}	-100	-	100	mA	According to JEDEC JESD78, AEC-Q100-004
ESD capability	ESD	-2	-	+2	kV	Human Body Model
Storage temperature	T_{stg}	-55	-	150	˚C	
Junction temperature	T_J	-40	-	150	˚C	
Thermal resistance SOIC-16	R_{th-JA}	-	37	-	K/W	In free air on multilayer PCB (JEDEC 1s2p)
Thermal resistance SOIC-16	R_{th-JC}	-	10	-	K/W	Referring center of exposed pac

Table 8-1 Absolute maximum ratings

Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

9. Operating Range

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Power supply voltage range	V_{VSUP}	4.5	-	28	V	Full functionality
Digital supply voltage range	V_{VDD}	3	-	5.5	V	CP discharged, power FETs off
Ambient temperature	T_A	-40	-	125	˚C	
Junction temperature	T_J	-40	-	150	˚C	

Table 9-1 Operating range

10. General Electrical Specifications

	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
	Power Supply VSUP						
No.1	Supply voltage range	V_{SUP}	Functional	7	-	18	V
No.2	Supply voltage extended range low	V_{SUP_ERL}	Functional w. decreased gate drive voltage	4.5	-	7	V
No.3	Supply voltage extended range high	V_{SUP_ERH}		18	-	28	V
No.4	Quiescent current from V_{SUP}	I_{SUP_SLEEP}	V_{DD} = Low	-	-	30	µA
No.5	Operating current from V_{SUP}	I_{SUP_INT}	Pre-driver operation 25kHz PWM, no load	-	-	5	mA
No.6	Supply over voltage high	V_{SUP_OVH}	Warning on ICOM	-	-	35	V
No.7	Supply over voltage low	V_{SUP_OVL}	ICOM released	30	-	-	V
No.8	Supply over voltage hysteresis	V_{SUP_OVHY}		0.4	-	1	V
No.9	Supply over voltage debounce time	$V_{SUP\_OV\_DEB}$		-	-	2	µs
No.10	Supply under voltage high	V_{SUP_UVH}	ICOM released	-	-	6	V
No.11	Supply under voltage low	V_{SUP_UVL}	Warning on ICOM	5	-	-	V
No.12	Supply under voltage hysteresis	V_{SUP_UVHY}		0.2	-	0.5	V
No.13	Supply under voltage debounce time	$V_{SUP\_UV\_DEB}$		-	-	10	µs
No.14	Power on reset level	V_{POR}	Reset released on rising edge V_{SUP} when V_{DD}=high	2.6	-	4.5	V
	VVBATF						
No.15	Leakage from V_{BATF} to GND	R_{VBATF_LEAK}	Pre-driver not in sleep	-	-	30	µA
	Temperature Warning						
No.16	Over temperature high	OVT_H	Warning on ICOM	-	185	-	°C
No.17	Over temperature low	OVT_L	ICOM released	-	168	-	°C
	On-Chip Oscillator						
No.18	Oscillator frequency	f_{OSC}	Internal Oscillator	6.8	8	9.2	MHz

	Charge Pump CP, VBOOST						
No.19	Output slew rate	V_{CP}		-	100	-	V/µs
No.20	Charge pump frequency	f_{CP}		170	200	230	kHz
No.21	Reverse polarity N-FET gate-source voltage (V_{BOOST}-V_{SUP})	V_{GS_RPFET}	CP Mode 1 V_{SUP} > 7V I_{REG} < 20mA	5	12	13	V
No.22	Resistive load from V_{BOOST} to GND	R_{BOOST_LEAK}	R_{Typ} at room temperature R_{Min} at 150°C T_J (excl. R_{VREG_LEAK})	6	8	-	MOhm
No.23	V_{BOOST} under voltage high	V_{BOOST_UVH}	COM released CP Mode 0 (V_{BOOST}) CP Mode 1 (V_{BOOST}-V_{SUP})	6.1	-	7.2	V
No.24	V_{BOOST} under voltage low	V_{BOOST_UVL}	Warning on ICOM CP Mode 0 (V_{BOOST}) CP Mode 1 (V_{BOOST}-V_{SUP})	5.6	-	6.7	V
No.25	V_{BOOST} discharge stop	$V_{BOOST\_DISSTOP}$	CP Mode 1 (V_{BOOST}-V_{SUP}) Discharge activated by V_{SUP_OV} and topped by $V_{BOOST\_DIS\_STOP}$	V_{SUP}-0.2	-	V_{SUP}+0.8	V
No.26	V_{BOOST} discharge current	I_{BOOST_DIS}	CP Mode 1 (V_{BOOST}-V_{SUP}) From V_{BOOST} to DGND	25	-	90	mA
	Driver Supply VREG						
No.27	Load current on V_{REG}	$I_{REG\_CPMODE0}$	V_{REG} > 11V CP Mode 0, EN_CP = 1	-	-	40	mA
		$I_{REG\_CPMODE1}$	V_{REG} > 11V CP Mode 1, EN_CP = 1	-	-	20	mA
No.28	Output voltage V_{REG}	V_{REG}	CP Mode 0, EN_CP = 1 V_{SUP} > 8V I_{REG} < 40mA	11	12	13	V
			CP Mode 0, EN_CP = 1 7V< V_{SUP} < 8V I_{REG} < 40mA	10	-	13	V
			CP Mode 1, EN_CP = 1 I_{REG} < 20mA	11	12	13	V
No.29	Internal resistive load from V_{REG} to GND	R_{VREG_LEAK}	R_{Typ} at room temperature R_{Min} at 150°C T_J	0.3	0.4	-	MOhm
No.30	V_{REG} over voltage high	V_{REG_OVH}	Warning on ICOM	14.2	-	16.5	V

No.31	V_{REG} over voltage low	V_{REG_OVL}	ICOM released	13.5	-	15.8	V
No.32	V_{REG} over voltage hysteresis	V_{REG_OVHY}		0.65	-	1.5	V
No.33	V_{REG} under voltage high	V_{REG_UVH}	ICOM released	7.2	-	8.1	V
No.34	V_{REG} under voltage low	V_{REG_UVL}	Warning on ICOM	6.9	-	7.8	V
No.35	V_{REG} under voltage hysteresis	V_{REG_UVHY}		0.3	-	0.7	V
	Digital Supply VDD						
No.36	V_{DD} operating current	I_{DD}	Incl. ICOM current sourcing	4	-	7	mA
No.37	V_{DD} pull down resistance	V_{DD_RPD}		200	300	370	kOhm
No.38	V_{DD} input voltage	V_{DD}	V_{DD} = 3.3V or 5V	3	-	5.5	V
No.39	V_{DD} under voltage high	V_{DD_UVH}	ICOM released	2.55	-	2.95	V
No.40	V_{DD} under voltage low	V_{DD_UVL}	Warning on ICOM	2.45	-	2.85	V
No.41	V_{DD} under voltage hysteresis	V_{DD_UVHY}		0.08	0.10	0.14	V
No.42	V_{DD} sleep voltage high	V_{DD_SLEEPH}	Out of sleep	2.1	-	2.7	V
No.43	V_{DD} sleep voltage low	V_{DD_SLEEPL}	Go to sleep	1.6	-	2.1	V
No.44	V_{DD} sleep voltage hysteresis	$V_{DD\_SLEEPHY}$		0.45	0.58	0.80	V

	Gate Drivers						
No.45	Rise time	t_r	C_{LOAD} = 1nF, 20% to 80%	6	7	15	ns
No.46	Fall time	t_f	C_{LOAD} = 1nF, 80% to 20%	4	7	15	ns
No.47	Pull-up ON resistance low-side pre-driver	R_{ON_UP}	V_{SUP} > 7V -10mA, T_J = -40°C	2.4 (10)	-	7.0 (30)	Ohm
	Pull-up ON resistance high-side pre-driver		-10mA, T_J = 150°C (for MLX83202)	2.0 (15)	-	9.2 (30)	Ohm
No.48	Pull-down ON resistance low-side pre-driver	R_{ON_DN}	V_{SUP} > 7V 10mA, T_J = -40°C	1.5 (10)	-	5.7 (30)	Ohm
	Pull-down ON resistance high-side pre-driver		10mA, T_J = 150°C (for MLX83202)	2.0 (15)	-	9.2 (30)	Ohm
No.49	Turn-on gate drive peak current (sourcing)	I_{GON}	V_{GS} = 0V, V_{SUP} > 7V (for MLX83202)		-	-1.4 (-0.45)	A
No.50	Turn-off gate drive peak current (sinking)	I_{GOFF}	V_{GS} = 12V, V_{SUP} > 7V (for MLX83202)		-	1.6 (0.45)	A
No.51	Propagation delay	t_{PDDRV}	From logic input threshold to 2V V_{GS} drive output at no load	20	-	120[1]	ns
No.52	Propagation delay matching	t_{PDDRVM}	Transitions at the different phases at no load condition	-20	-	20	ns
No.53	Programmable dead time : asynchronous internal delay between high-side and low-side pre-driver of one half bridge	t_{DEAD}	DEAD_TIME [2:0] = 000 001 010 011 100 101 110 111	-25%	0.00 0.51 0.80 1.10 1.67 2.30 3.40 6.90	+25%	µs
No.54	Dead time matching between different channels	t_{DEAD_TOL}		-15	-	15	%
No.55	Programmable drain-source voltage for monitoring of external N-FETs	V_{VDS_MON}	VDSMON[2:0] = 000 001 010 011 100 101 110	 0.40 0.60 0.85 1.05 1.25 1.50	Disabled 0.50 0.75 1.00 1.25 1.50 1.75	 0.60 0.90 1.15 1.45 1.75 2.00	V

[1] *For bare it is specified to 200ns max due measurement accuracy at wafer level*

			111	1.70	2.00	2.30	
No.56	Programmable drain-source monitor blanking time: Delay between gate high and enabling corresponding V_{DS} monitor	t_{VDS_BL}	VDS_BLANK_TIME[1:0] = 00 01 10 11	5.10 2.55 1.28 0.60	6.80 3.40 1.70 0.80	8.50 4.25 2.13 1.00	µs
No.57	Sleep gate discharge resistor	Rsgd	Internal resistance between FET gate-source pins to switch-off FET. V_{DD} = 0V (sleep mode) V_{GS} = 0.5V	-	-	1	kOhm
No.58	Trickle charge pump current capability	I_{TCP}	V_{SUP} > 12V PHASEx = V_{SUP} V_{GSx} = V_{PHASEx} + 6.5V $I_{TCP,max}$ @ T_J = 150C See performance graphs	-	-	-25 -20 (T_J>150C)	µA
No.59	V_{GS} under voltage threshold high	V_{GS_UVH}	ICOM released	42	-	70	$\%V_{RG}$
No.60	V_{GS} under voltage threshold low	V_{GS_UVL}	Warning on ICOM	36	-	63	$\%V_{RG}$
No.61	PWM frequency	f_{DR_PWM}		-	20	100	kHz
No.62	Leakage from CPx - PHASEx	R_{CP_LEAK}	R_{Typ} at room temperature R_{Min} at 150°C T_J	0.5	1	-	MOhm
No.63	V_{CPx} discharge current	I_{BOOST_DIS}	Activated by V_{SUP_OVH} event From V_{CPx} to V_{PHASEx}	8	-	40	mA
	Logic IO's - FET inputs						
No.64	Digital input high voltage	$V_{IN\_DIG\_H}$	Min. voltage logical high	80	-	-	$\%V_{DD}$
No.65	Digital input low voltage	$V_{IN\_DIG\_L}$	Max. voltage logical low	-	-	20	$\%V_{DD}$
No.66	Input pull-up resistance	$R_{IN\_DIG\_PU}$	FETB2, FETB3-pins FETB1 in normal mode	90	-	410	kOhm
No.67	Input pull-down resistance	$R_{IN\_DIG\_PD}$	FETTx-pins	90	-	410	kOhm
No.104	MISO RDSon pull-down	$R_{ON\_PD\_MISO}$	FETB1 (MISO) in SPI mode	0.5	1.1	3.4	kOhm
No.105	MISO RDSon pull-up	$R_{ON\_PU\_MISO}$	FETB1 (MISO) in SPI mode	1.3	2.0	3.2	kOhm
No.106	MISO source current	I_{MISO_SOURCE}	FETB1 (MISO) in SPI mode	-	3	6	mA
No.107	MISO sink current	I_{MISO_SINK}	FETB1 (MISO) in SPI mode	-	3	6	mA

	Logic IO's - EN input						
No.68	Input pull-down resistance	R_{EN_PD}	EN	90	-	410	kOhm
No.69	Bridge disable propagation delay	EN_{PR_DEL}	From bridge disable EN<0.2V_{DD} to V_{GS} < 0.5V, C_{LOAD} = 1nF	-	-	1	µs
	Logic IO's - ICOM						
No.70	Pull-up current	$ICOM_{PU}$	V_{ICOM} = 0V	-2.2	-	-5.0	mA
No.71	Pull-down current	$ICOM_{PD}$	V_{ICOM} = V_{DD}	5.0	-	2.6	mA
No.72	ICOM PWM frequency fast	f_{ICOMF}		85	100	115	kHz
No.73	ICOM PWM frequency slow	f_{ICOMS}		10.6	12.5	14.4	kHz
No.74	SPI start-up pulse duration on ICOM to enter SPI mode	t_{SPI_SU}	EN = Low FETTx = Low, FETBx = High	2048/ f_{osc}	-	4096/ f_{osc}	s
	SPI Timing						
No.75	SPI initial setup time	t_{SPI_ISU}		2	-	-	µs
No.76	SPI clock frequency	f_{SPI}		-	-	500	kHz
No.77	Rise/fall times	t_{SPI_RF}	CLK, CSB, MISO, MOSI	-	-	200	ns
No.78	CSB setup time	t_{CSB_SU}		1	-	-	µs
No.79	CSB high time	t_{CSB_H}		2	-	-	µs
No.80	Clock high time	t_{CLK_H}		1	-	-	µs
No.81	Clock low time	t_{CLK_L}		1	-	-	µs
No.82	Data in setup time	t_{DI_SU}		1	-	-	µs
No.83	Data in hold time	t_{DI_H}		500	-		ns
No.84	Data out ready delay	t_{DO_R}	C_{LOAD} at FETB1 < 50pF	-	500	-	ns
No.85	EEPROM read delay	t_{EE_RD}	EE_RD = 1	6	-		µs
No.86	EEPROM write delay	t_{EE_WR}	EE_WR = 1	12	-	-	ms
No.87	Temperature for EEPROM read	$T_{J\_EE\_RD}$	Junction temperature	-40	-	150	°C
No.88	Temperature for EEPROM write	$T_{J\_EE\_WR}$	Junction temperature	-40	-	150	°C

	Current Sense Amplifier						
No.89	Input offset voltage	V_{IS_IO}		-7.6	-	7.6	mV
No.90	Input offset voltage thermal drift	$V_{IS\_IO\_TDRIFT}$		-10	-	10	µV/°C
No.91	Input common mode rejection ratio DC	IS_{CMRR_DC}	Input differential voltage within ±100mV Common mode [-0.5, 1.0] V	60	-	-	dB
No.92	Input common mode rejection ratio 1MHz	IS_{CMRR_AC}		40	-	-	dB
No.93	Input power supply rejection ratio DC for V_{DD} supply	IS_{PSRR_DC}		60	-	-	dB
No.94	Input power supply rejection ratio 1MHz for V_{DD} supply	IS_{PSRR_AC}		40	-	-	dB
No.95	Closed loop gain	IS_{GAIN}	Current sense gain = 000 001 010 011 100 101 110 111	-3%	8.0 10.3 13.3 17.2 22.2 28.7 37.0 47.8	+3%	
No.96	Output settling time	IS_{SET}	Amplified output to 99% of final value after input change	-	-	1.0	µs
No.97	Output voltage range high	V_{ISENSE_MAX}	ISENSE output max level	V_{DD}-0.02	-	V_{DD}	V
No.98	Output voltage range low	V_{ISENSE_MIN}	ISENSE output min level	GND	-	GND+0.02	V
No.99	Output short circuit current to ground	I_{ISENSE_SC}	Output current saturation level	-	1.4	-	mA
No.100	Gain bandwidth (GBW)	IS_{GBW}		6	-	-	MHz
No.101	Output slew rate	IS_{SR}		–	8	-	V/µs
No.102	CM spike recovery	IS_{CM_REC}	CM spike = ±1.5V, t=250ns	-	-	730	ns
No.103	VREF voltage input	V_{REF}		0	-	50	%V_{DD}

Table 10-1 General Electrical Specifications

10.1. MLX83203 Typical Performance Graphs

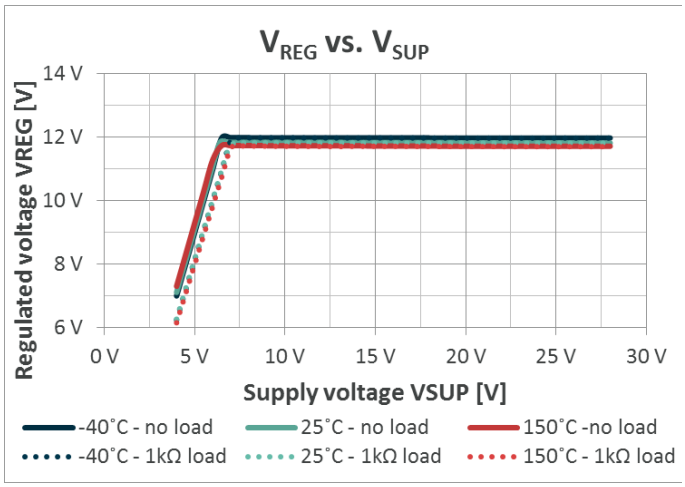

Figure 10-1 MLX83203 Regulated output voltage vs. supply voltage

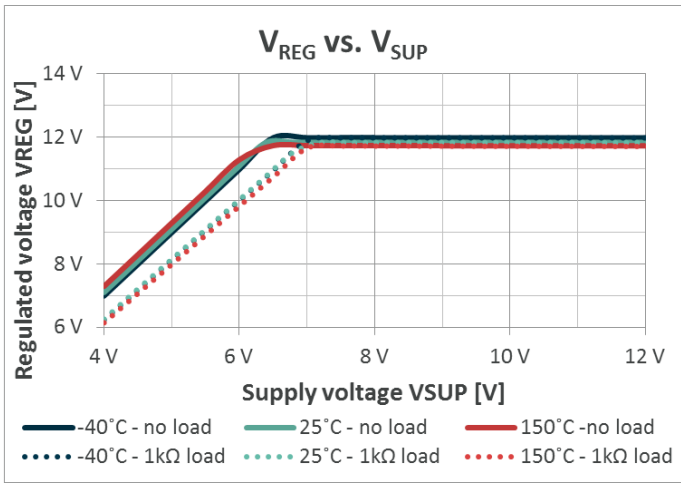

Figure 10-2 MLX83203 Regulated output voltage vs. supply voltage

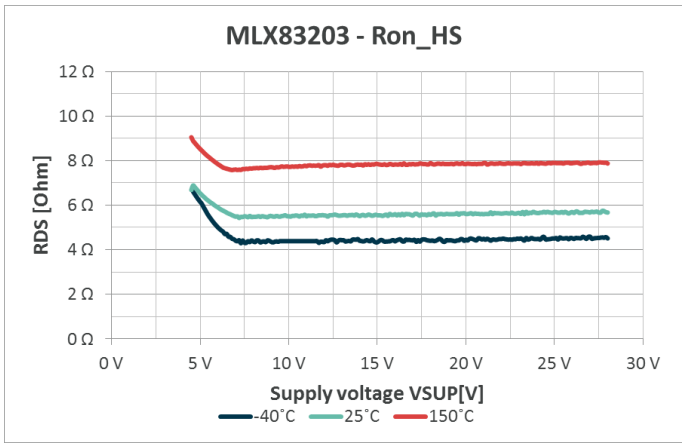

Figure 10-3 MLX83203 High-side driver FET R_{ON} resistance vs. supply voltage

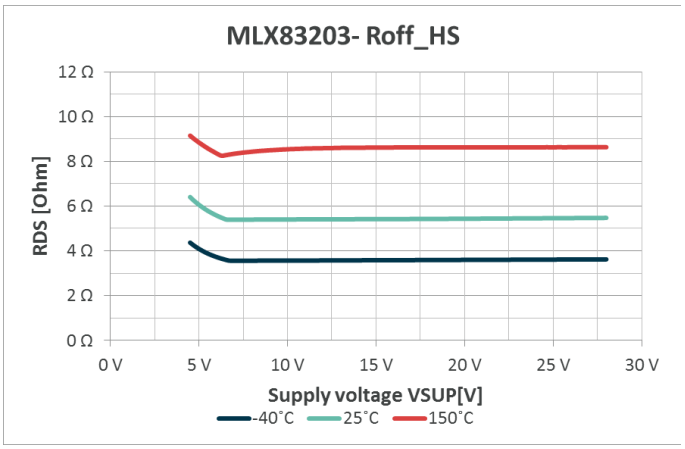

Figure 10-4 MLX83203 High-side driver FET R_{OFF} resistance vs. supply voltage

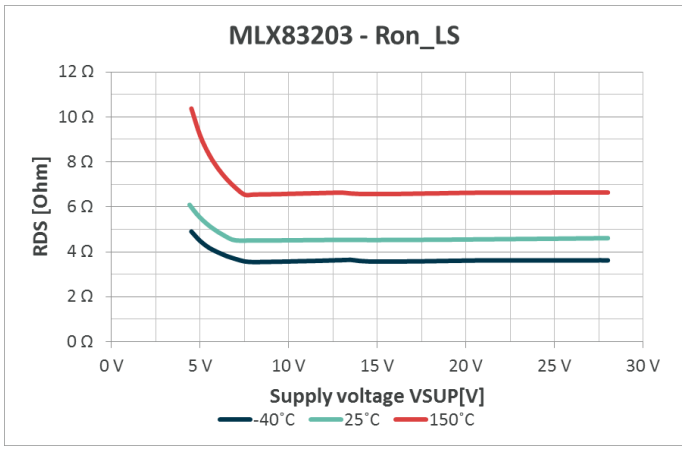

Figure 10-5 MLX83203 Low-side driver FET R_{ON} resistance vs. supply voltage

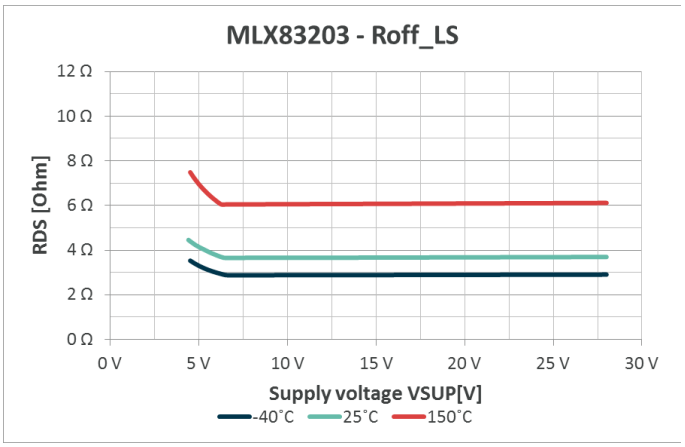

Figure 10-6 MLX83203 Low-side driver FET R_{OFF} resistance vs. supply voltage

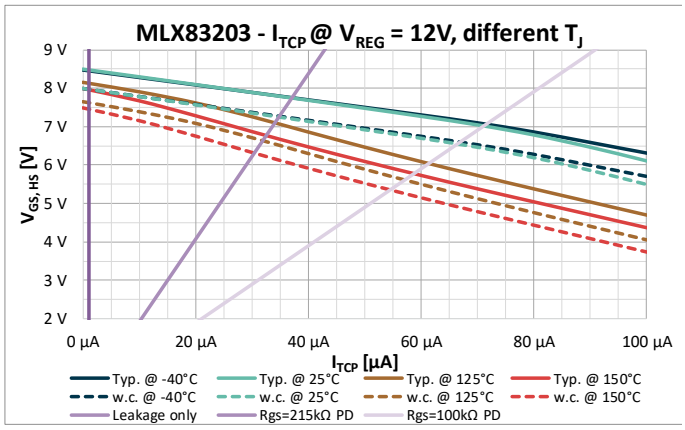

Figure 10-7 MLX83203 Trickle charge pump current capability vs gate drive voltage at different temperatures

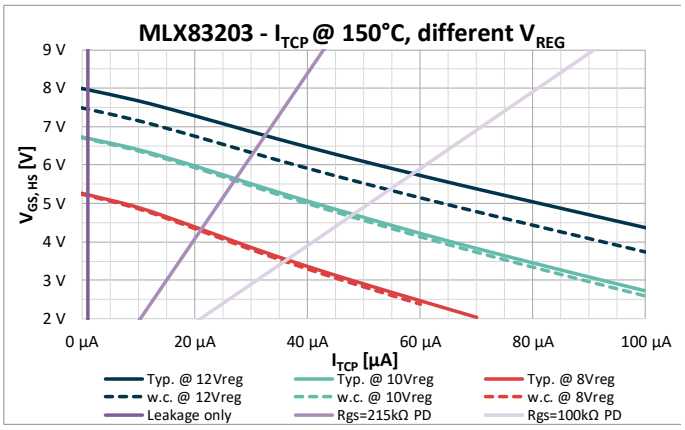

Figure 10-8 MLX83203 Trickle charge pump current capability vs gate drive voltage at different VREG, at 150°C

10.2. MLX83202 Typical Performance Graphs

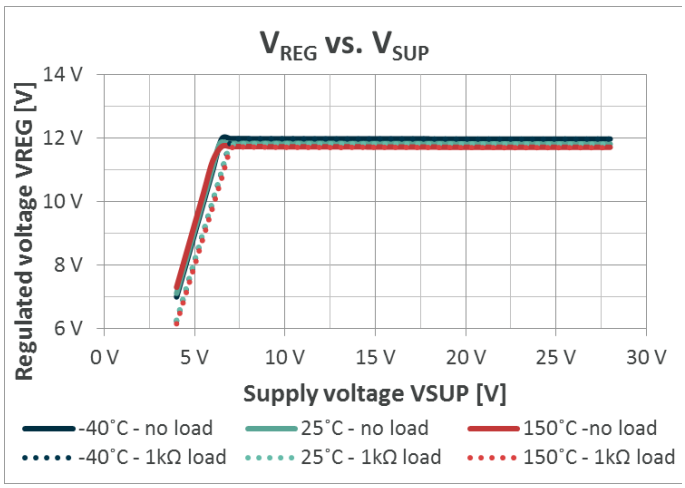

Figure 10-9 MLX83202 Regulated output voltage vs. supply voltage

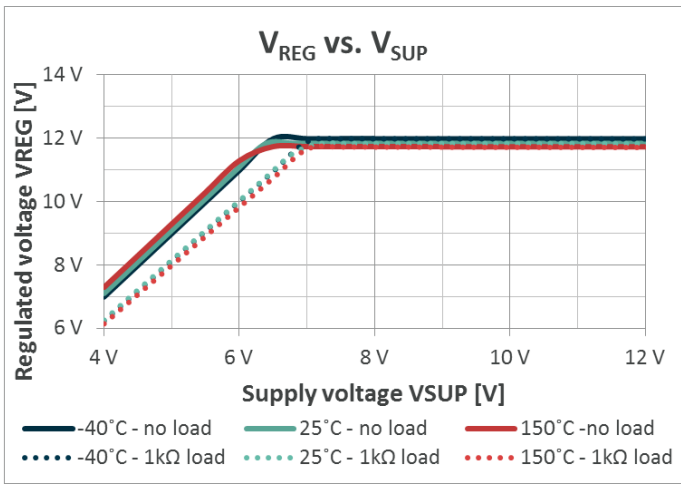

Figure 10-10 MLX83202 Regulated output voltage vs. supply voltage

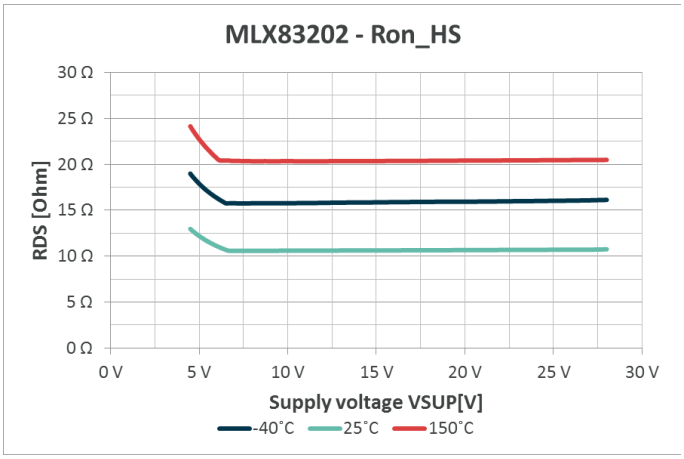

Figure 10-11 MLX83202 High-side driver FET R_{ON} resistance vs. supply voltage

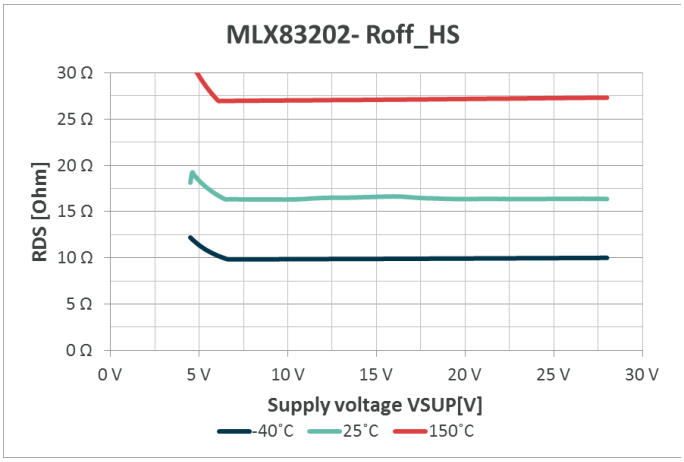

Figure 10-12 MLX83202 High-side driver FET R_{OFF} resistance vs. supply voltage

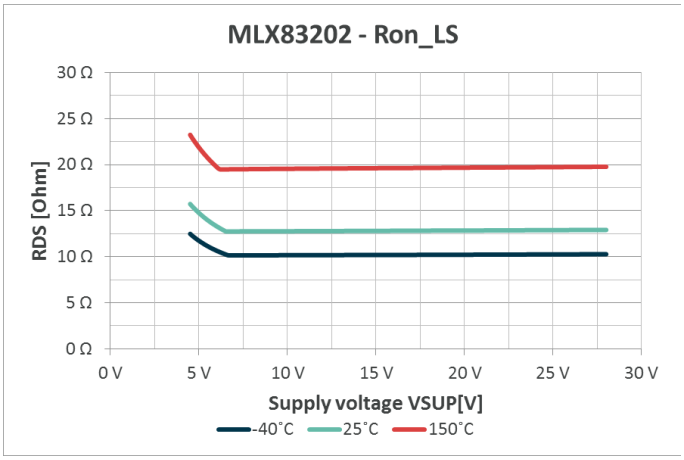

Figure 10-13 MLX83202 Low-side driver FET R_{ON} resistance vs. supply voltage

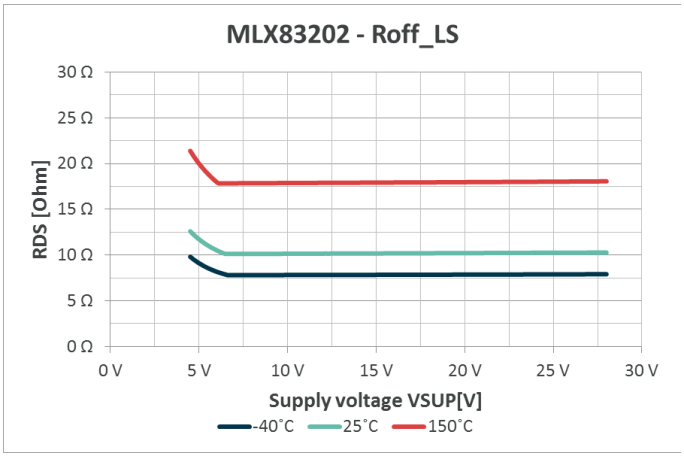

Figure 10-14 MLX83202 Low-side driver FET R_{OFF} resistance vs. supply voltage

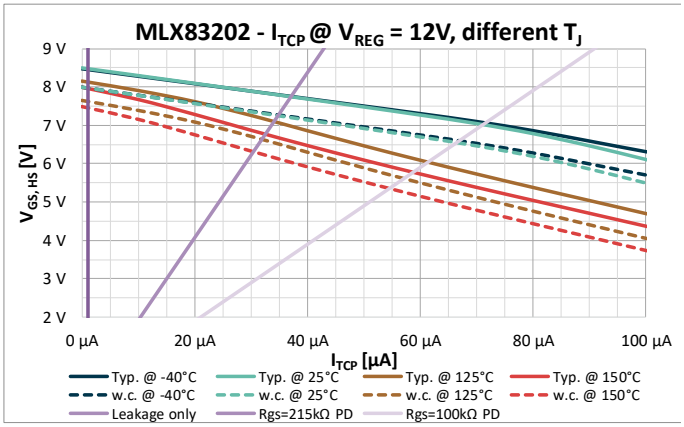

Figure 10-15 MLX83202 Trickle charge pump current capability vs gate drive voltage at different temperatures

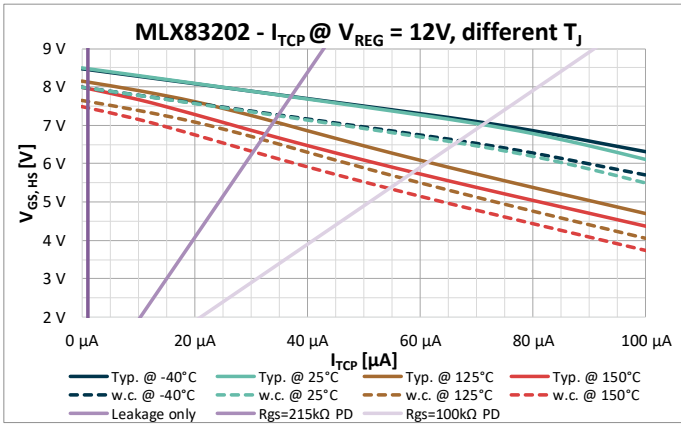

Figure 10-16 MLX83202 Trickle charge pump current capability vs gate drive voltage at different VREG, at 150°C

11. Block Diagram

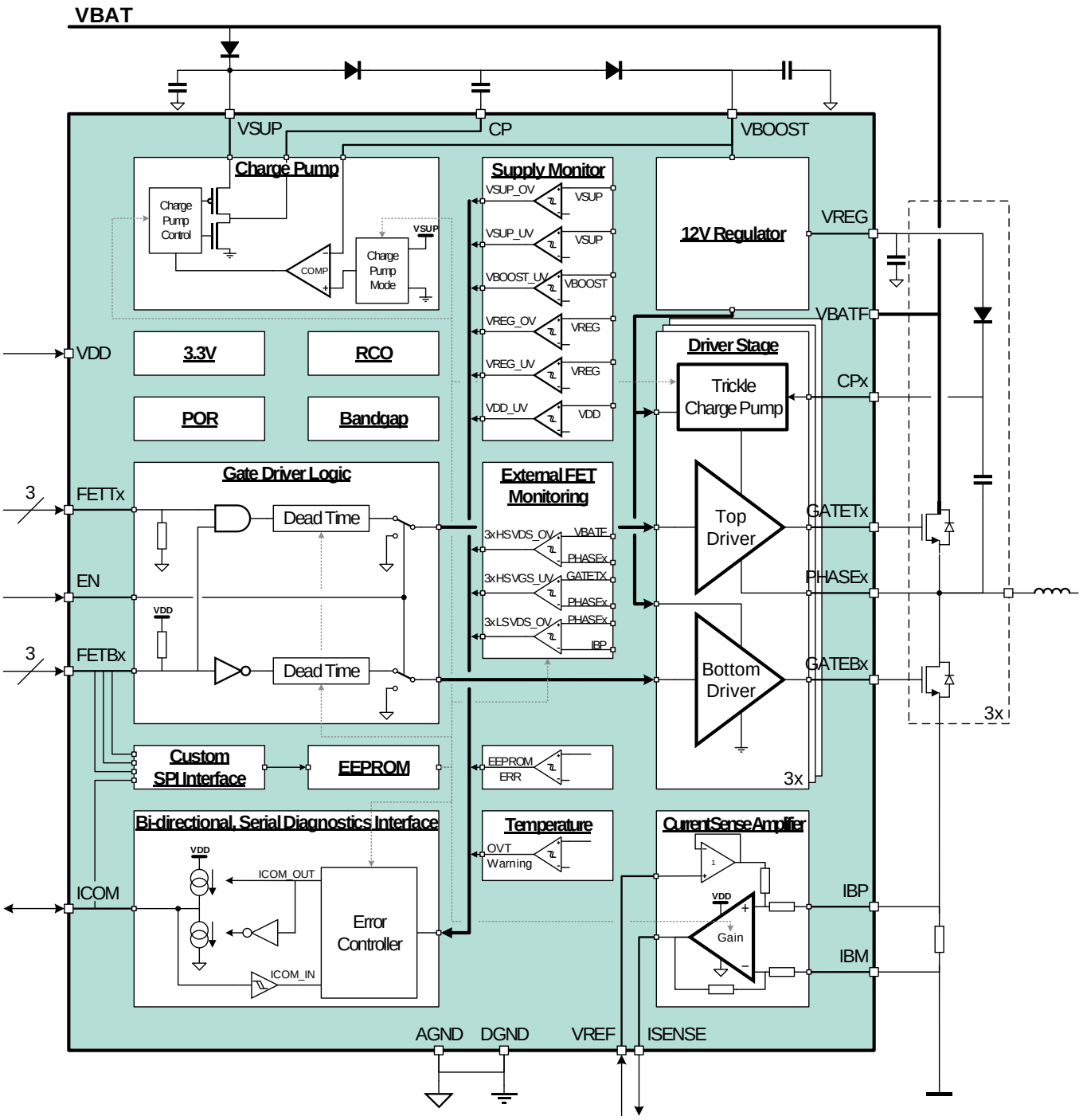

Figure 11-1 Block diagram

12. Functional Description

12.1. Supply System

The MLX83203-2 is supplied via pins VSUP and VDD. The power supply VSUP supplies the internal operation of the pre-driver, the charge pump and the voltage regulator used for the bootstrap based architecture. The digital supply VDD supplies the IO's and the current sense amplifier.

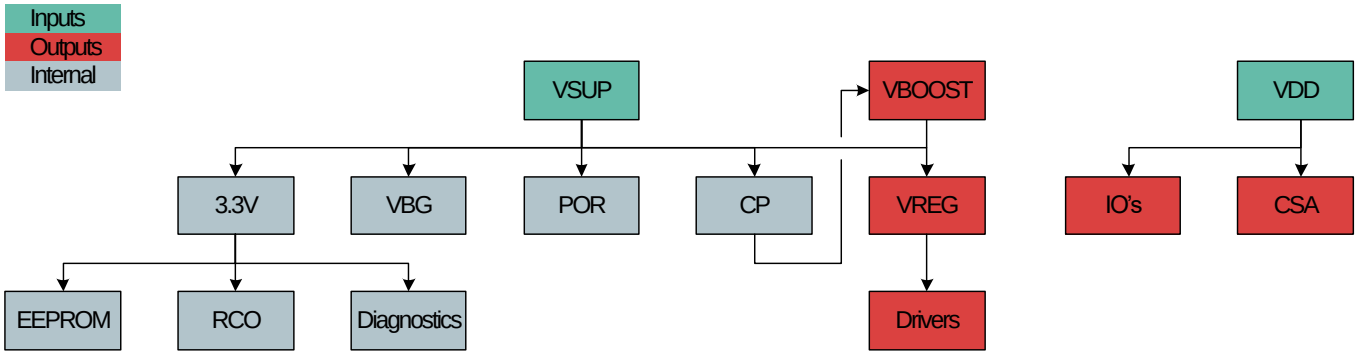

Figure 12-1 Principle organization of the supply system

12.1.1. Power Supply - VSUP

The internal operation of the pre-driver is supplied from the power supply input pin VSUP. It supplies the bandgap reference, power-on-reset system and internal 3.3V regulator. This 3.3V regulator in turn supplies the EEPROM, RC-oscillator and diagnostics. For safety reasons the pre-driver provides integrated under voltage and over voltage detection on VSUP.

12.1.2. Charge Pump - VBOOST

The IC comprises a charge pump, supplied from VSUP, which allows full device operation down to 4.5V. The charge pump boosted output voltage is available on VBOOST. This boosted voltage powers the voltage regulator VREG used to supply the low-side drivers directly, and high-side drivers via the bootstrap architecture. See Figure 4-1 for the standard charge pump configuration where VBOOST is regulated relative to ground. The charge pump will not be switching when $V_{SUP} > V_{REG} + 2xV_{f,\ diode}$.

An alternative mode of operation for the charge pump supports the use of an external low drop N-FET for reverse polarity protection. In this mode the charge pump boosts the output voltage relative to the supply voltage instead of relative to ground, see application diagram in Figure 4-2. The disadvantage is an additional amount of dissipation inside the driver to regulate VREG.

The charge pump architecture is a supply voltage doubler with feedback loop for stable output voltage generation, as shown in Figure 12-2. It can be configured in EEPROM to either regulate the boosted output voltage VBOOST relative to ground or relative to the supply voltage, see Figure 12-3 for the typical output voltage. Furthermore the EEPROM configuration allows disabling the charge pump for applications not requiring the low voltage operation, in order to reduce the overall power consumption.

For safety reasons the pre-driver provides integrated under voltage detection on VBOOST. In addition the charge pump comprises a discharge switch in order to keep VBOOST output voltage in a safe operating area in case of over voltage on the supply input pin. The discharge switch is activated as soon as the supply voltage VSUP exceeds the V_{SUP_OVH} threshold level and is deactivated when it drops below the V_{SUP_OVL} threshold. At the same time the charge pump is deactivated.

EN_CP	CPMODE	Charge pump configuration
0	x	Charge pump disabled
1	0	Charge pump configured to regulate VBOOST relative to ground, to support low voltage operation
1	1	Charge pump configured to regulate VBOOST relative to the supply, to support the use of a reverse polarity N-FET

Table 12-1 Charge pump configuration options

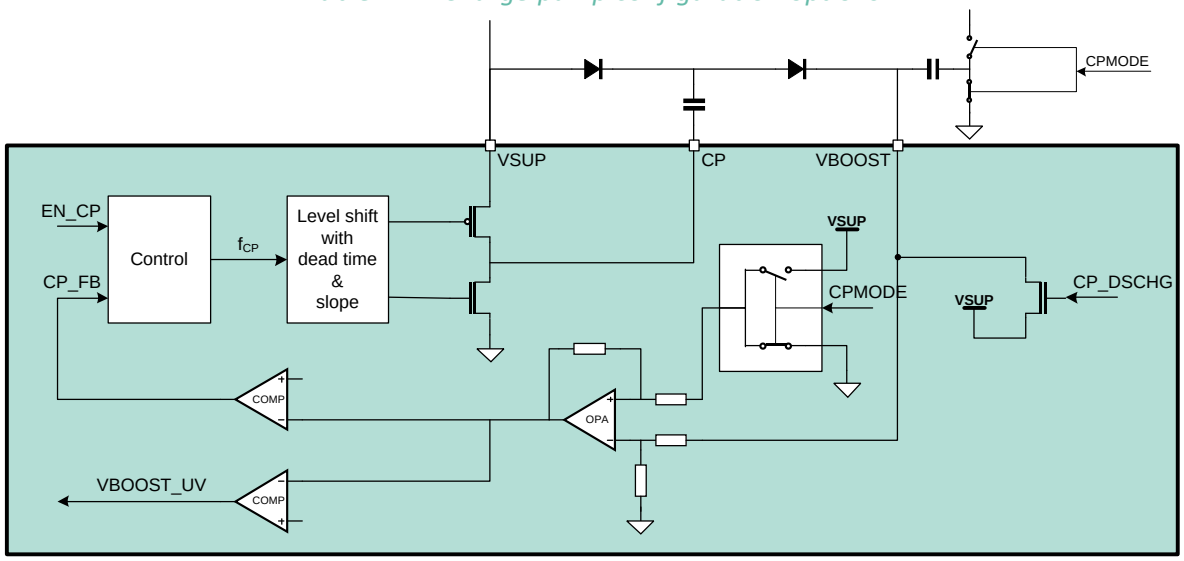

Figure 12-2 Charge pump principle schematic

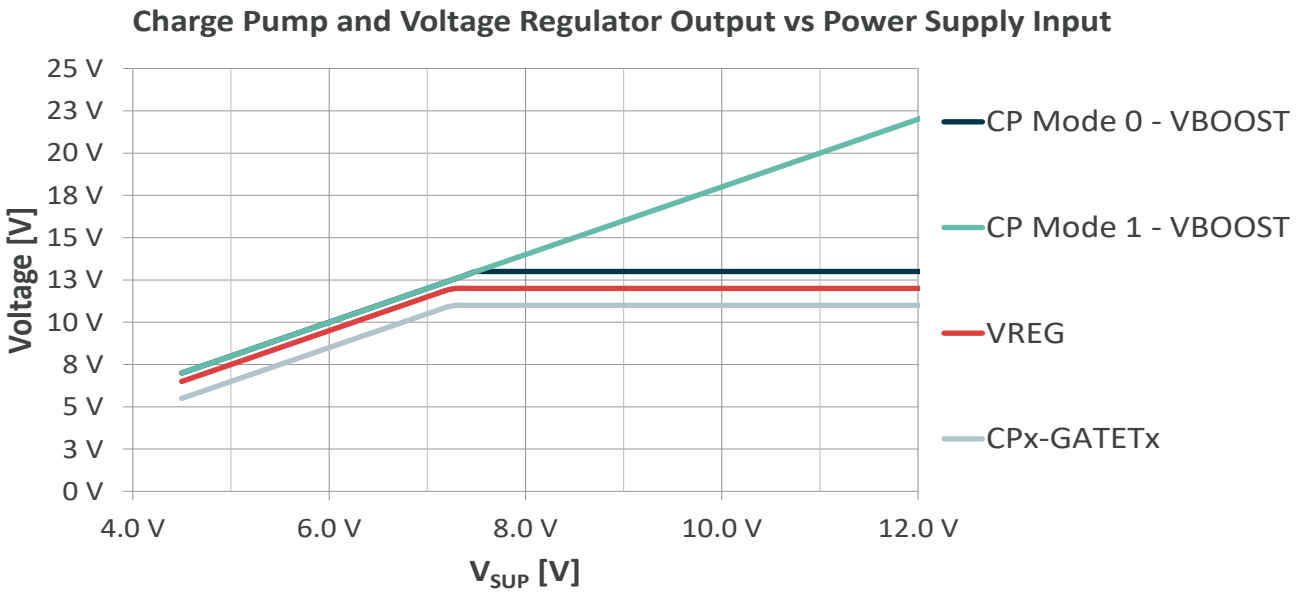

Figure 12-3 Charge pump output and driver supply

12.1.3. Voltage Regulator - VREG

The voltage regulator regulates the power supply down to 12V, in order to supply the low-side gate drivers and switch the external low-side N-FETs without gate-source over voltage at high battery voltages. The regulated output voltage VREG further provides the bootstrap voltage for driving the high-side N-FETs.

For safety reasons the pre-driver provides integrated under voltage and over voltage detection on VREG.

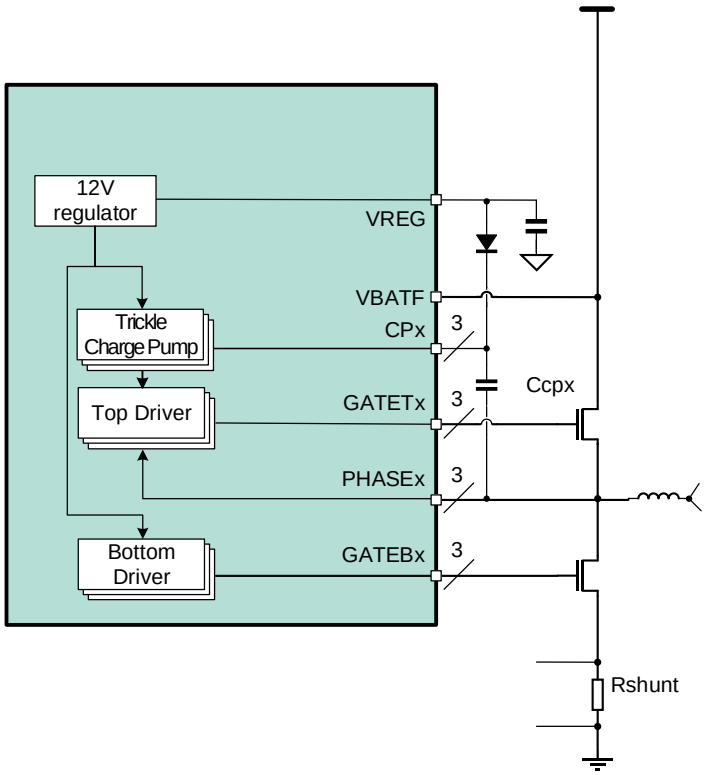

Figure 12-4 Voltage regulator for driver supply – VREG

12.1.4. Digital Supply - VDD

The MLX83203-2 comprises a current sense amplifier. The current sense amplifier and IO's are supplied from the digital supply VDD.

For safety reasons the pre-driver provides integrated under voltage detection on VDD.

Note:
When supplying VDD with a limited output impedance (e.g. from a microcontroller IO) the performance of the amplifier may be affected.

12.1.5. Sleep Mode

Sleep mode is activated when the digital supply input VDD is pulled below "VVDD sleep voltage threshold low". In sleep mode the charge pump is disabled and the current consumption on VSUP is reduced. All gate drivers are switched off via sleep gate discharge resistors R_{SGD}. The pre-driver will wake-up as soon as the voltage level on VDD rises above "VVDD sleep voltage threshold high".

Pin Name	State in sleep mode
CP	The charge pump is disabled.
VBOOST	Since the charge pump is disabled VBOOST is pulled to the supply voltage via the external charge pump diodes.
GATEBx	In sleep mode, gate-discharge resistors (R_{SGD}) between GATEBx and DGND are activated, ensuring all low-side gate drivers are switched off
GATETx	In sleep mode, gate-discharge resistors (R_{SGD}) between GATETx and PHASEx are activated, ensuring all high-side gate drivers are switched off
PHASEx	Phases are kept low with GATETx through the internal body diode of the pre-driver
VREG	Voltage regulator is disabled
CPx	Any charge that remains after VREG is disabled will leak to ground
ISENSE	Current sense amplifier is supplied from VDD, and thus not active
FETBx, FETTx EN, ICOM	All IO's are supplied from VDD, and thus not active

Table 12-2 Drivers in Sleep Mode

Notes:

1. In case any of the digital input pins are externally pulled high while VDD is low, current will flow into VDD via internal ESD protection diodes. This condition is not allowed.

2. When VDD is pulled low, also ICOM will go low. This should not be interpreted as a diagnostic interrupt.

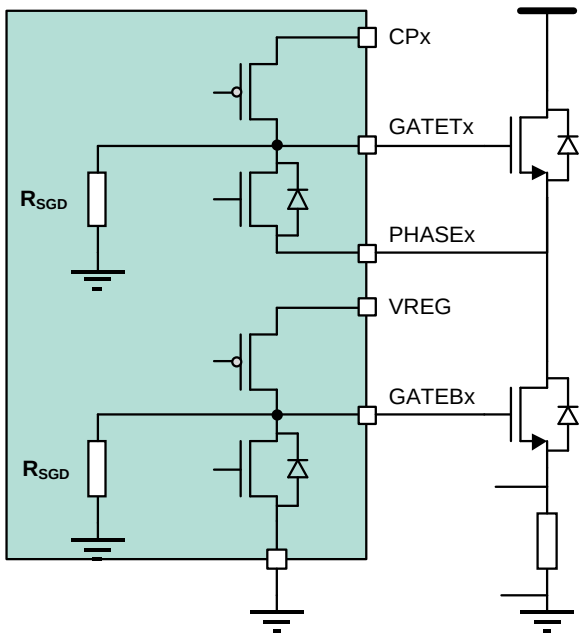

Figure 13-1-5 Drivers in Sleep Mode

12.2. Gate Drivers

12.2.1. PWM Input Control Logic – FETBx & FETTx

Each of the 6 external N-FETs can be controlled independently via the 6 digital PWM input pins: FETBx and FETTx. However, the digital logic provides the option to control the 3 external half bridges with only 3 control signals, by shorting high-side and low-side PWM input pins for each half bridge.

The IC provides internal shoot through protection since the digital logic prevents simultaneous activation of both high-side and low-side driver of one half bridge. A configurable dead time ensures the high-side (low-side) N-FET is fully switched off, before switching on the complementary low-side (high-side) N-FET.

For safety reasons the pre-driver provides integrated drain-source and gate-source monitoring for each of the 6 external N-FETs.

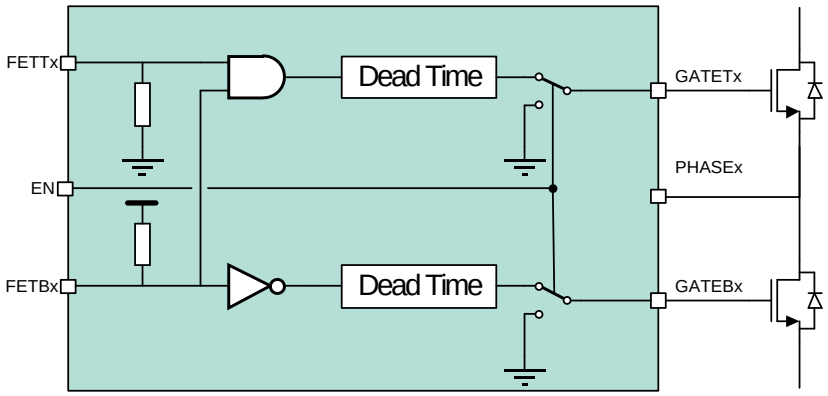

Figure 12-5 Input control logic of the driver stage

12.2.2. Enable Input EN

The enable input pin EN enables the gate driver outputs when set high. When reset, all gate driver outputs are switched to the low state, switching off all external N-FETs. This is performed by pulling all gate drivers to ground via the pull-down on-resistances. The enable pin can be used by the microcontroller to disable all drivers in case of any fault detection.

While EN is low, the programming of the EEPROM via SPI can be initiated by pulling ICOM low for the SPI start-up time specified by t_{SPI_SU}.

12.2.3. Gate Driver Supply and Bootstrap Architecture – VREG & CPx

The voltage regulator regulates the power supply voltage down to 12V. The regulated voltage is used to directly supply the low-side drivers. To provide sufficient supply voltage for the high-side drivers a bootstrap architecture is used. When the low-side N-FET is switched on, the phase voltage will be pulled low and the bootstrap capacitor is charged from the VREG buffer capacitor through the bootstrap diode. Afterwards, if the low-side N-FET is switched off and the high-side N-FET is switched on, the charge of the bootstrap capacitor is used to supply sufficient gate drive voltage to the high-side N-FET. The integrated trickle charge pump assures the bootstrap capacitor will not be discharged, and allows 100% PWM operation.

12.3. Integrated Current Sense Amplifier

The IC comprises an integrated fast, high-bandwidth, low offset current sense amplifier.

The current sense amplifier is supplied from the digital supply. It senses the voltage over the low-side shunt, amplifies it with the gain programmed in EEPROM and adds the offset provided on VREF. The output of the amplifier is available on ISENSE.

$$ISENSE = Current \times Shunt \times Gain_{EEPROM} + V_{VREF}$$

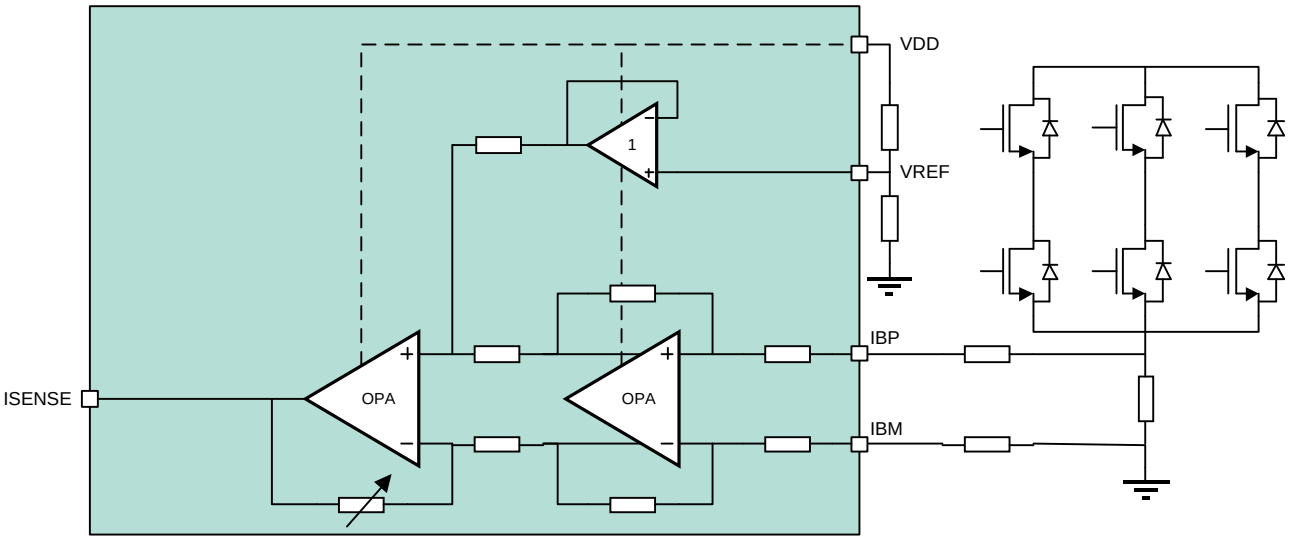

Figure 12-6 Current Sense Amplifier

12.4. Protection and Diagnostic Functions

12.4.1. Power Supply Over Voltage Shutdown (VSUP_OV)

The pre-driver has an integrated VSUP over voltage shut down to prevent destruction of the IC at high supply voltages.

12.4.2. Power Supply Under Voltage Warning (VSUP_UV)

The pre-driver has an integrated VSUP under voltage detection. The diagnostics interface will give a warning to the microcontroller. It is the responsibility of the microcontroller to take action in order to ensure reliable operation.

12.4.3. Digital Supply Under Voltage Warning (VDD_UV)

The pre-driver has an integrated VDD under voltage detection. The diagnostics interface will give a warning to the microcontroller. It is the responsibility of the microcontroller to take action in order to ensure reliable communication between microcontroller and pre-driver.

12.4.4. VBOOST Under Voltage Warning (VBOOST_UV)

The integrated charge pump boosts the supply voltage in low voltage operation on the VBOOST output. There is an under voltage detection on VBOOST to warn the microcontroller the charge pump is not ready. It is the responsibility of the microcontroller to take action in order to ensure reliable motor operation.

12.4.5. Gate Driver Supply Over Voltage Warning/Shutdown (VREG_OV)

The MLX83203-2 comprises an integrated VREG over voltage detection. The reaction of the pre-driver on this VREG_OV event depends on the status of the Bridge Feedback bit in EEPROM. If this VREG_OV_BF_EN bit is set the pre-driver will disable all gate drivers, switching off all external N-FETs. If the bit is reset it will just give a warning to the microcontroller.

VREG_OV_BF_EN	Pre-driver reaction VREG_OV event
0	VREG_OV is reported on ICOM, but the drivers remain active
1	VREG_OV is reported on ICOM and the drivers are disabled

Table 12-3 EEPROM Configuration for VREG over voltage detection

12.4.6. Gate Driver Supply Under Voltage Warning (VREG_UV)

The pre-driver detects when the regulated voltage drops below the under voltage threshold. The diagnostics interface will give a warning to the microcontroller. It is the responsibility of the microcontroller to take action in order to ensure reliable switching of the external N-FETs, since the VREG voltage directly supplies the low-side gate drivers.

12.4.7. Gate Source Voltage Monitoring Warning (VGS_UV)

In order to ensure reliable switching of the high-side N-FETs, the MLX83203-2 comprises gate-source monitors for each of the high-side N-FETs. In case of an under voltage, the diagnostics interface will give a warning to the microcontroller, if the gate-source comparators are enabled in EEPROM. It is the responsibility of the microcontroller to take action in order to ensure reliable switching of the high-side gate drivers.

12.4.8. Over Temperature Warning (OVT)

If the junction temperature exceeds the specified threshold, a warning will be communicated to the microcontroller. The pre-driver will continue in normal operation. It is the responsibility of the microcontroller to protect the IC against over temperature destruction.

12.4.9. Shoot Through Protection and Dead Time

The pre-drivers' internal implementation guarantees that low-side and high-side N-FET of the same external half bridge cannot be conducting at the same time, preventing a short between the supply and ground. In addition the pre-driver provides a programmable dead time in EEPROM. The dead time sets the delay between the moment when the high-side (low-side) N-FET is switched off, and the moment when the complementary low-side (high-side) N-FET can be switched on.

12.4.10. Drain-Source Voltage Monitoring Warning/Shutdown (VDS_ERR)

The MLX83203-2 provides a drain-source voltage monitoring feature for each external N-FET to protect against short circuits to ground or supply. For the high-sides the drain-source voltage are sensed via the VBATF –and PHASEx-pins. For the low-sides the PHASEx –and IBP-pins are used. The drain-source voltage comparator can be enabled or disabled in EEPROM.

The drain-source voltage monitor for a certain external N-FET is activated when the corresponding input is switched on and the dead time has passed. An additional blanking time can be programmed in EEPROM. If the drain-source voltage remains higher than the VDS monitor threshold voltage, the VDS error is raised. The threshold voltage is configurable in EEPROM.

The reaction of the pre-driver on a VDS error can be configured in EEPROM with the Bridge Feedback bit. If this bit is set the pre-driver automatically disables the drivers when a VDS error is detected. If the bit is reset, the drivers remain active. In both cases the VDS error will be reported to the microcontroller.

VDS_COMP_EN	VDS_BF_EN	Pre-driver reaction on VDS-error event
0	x	Any VDS error is ignored and no error is reported on ICOM
1	0	VDS_ERR is reported on ICOM, but the drivers remain active
1	1	VDS_ERR is reported on ICOM and the drivers are disabled

Table 12-4 EEPROM Configuration for drain-source error detection

12.4.11. EEPROM Error Warning (EEP_ERR)

To ensure reliable communication with EEPROM the pre-driver provides an automatic single bit error correction and double error detection. If two bits in the addressed word are bad the EEPROM gives the EEP_ERR warning, indicating a double error was detected.

12.4.12. Diagnostics Interface – ICOM

All diagnostic events described above are reported to the microcontroller via a single pin, ICOM. In normal operation, when no error is detected, ICOM is default high.

The ICOM interface acts as a serial interface that feeds back detailed diagnostics information. If an error is detected, ICOM goes from default high to communicating a PWM-signal. The speed of this PWM signal depends on the EEPROM configuration of bit PWM_SPEED. Each error corresponds to a duty cycle with a 5-bit resolution. Thus the microcontroller can distinguish different errors by reading the duty cycle, see Table 12-7.

PWM_SPEED	Description
0	Slow mode: for slow microcontrollers
1	Fast mode : for fastest response of microcontroller

Table 12-5 EEPROM Configuration for diagnostics communication speed

The duty cycle is transmitted until the microcontroller sends the acknowledgement. This is done by pulling ICOM low for more than a PWM-period, $t_{Ack} > t_{ICOM}$. At each ICOM falling edge the pre-driver checks the actual voltage on ICOM in order to detect an acknowledgement. After acknowledgement the duty cycle of the next error is transmitted, if multiple errors were detected. All errors have been reported when the end-of-frame duty cycle is send. When all errors are physically removed, and the end-of-frame message is acknowledged by the microcontroller, ICOM returns to its default high state.

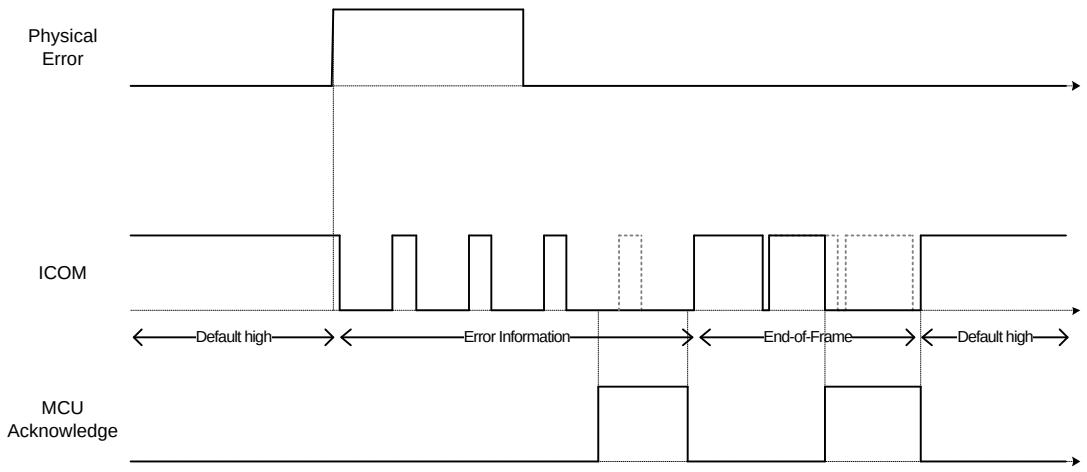

Figure 12-7 ICOM Diagnostics Communication

Notes:

1. When VDD is pulled low to put the pre-driver in sleep mode, ICOM will go low as well. This should not be interpreted as a diagnostic interrupt. As soon as VDD goes high, the pre-driver wakes-up and ICOM will return to its default high state.

2. At POR it is possible that the voltages on VSUP and VREG were not above the under voltage thresholds (e.g. due to charging of external capacitors). It is possible that ICOM reports these under voltage errors after POR. This implies that the microcontroller has to acknowledge these errors before ICOM will be in its default high state and the pre-driver is ready for normal operation.

The drivers are disabled when	The drivers are enabled again as soon as
An error condition is detected for which the hardware protection is activated VSUP_OV VREG_OV VDS_ERR	The microcontroller acknowledges the error
VDD = Low (sleep mode)	VDD = High (wake-up)
EN = Low	EN = High

Table 12-6 Pre-Driver Output State Summary

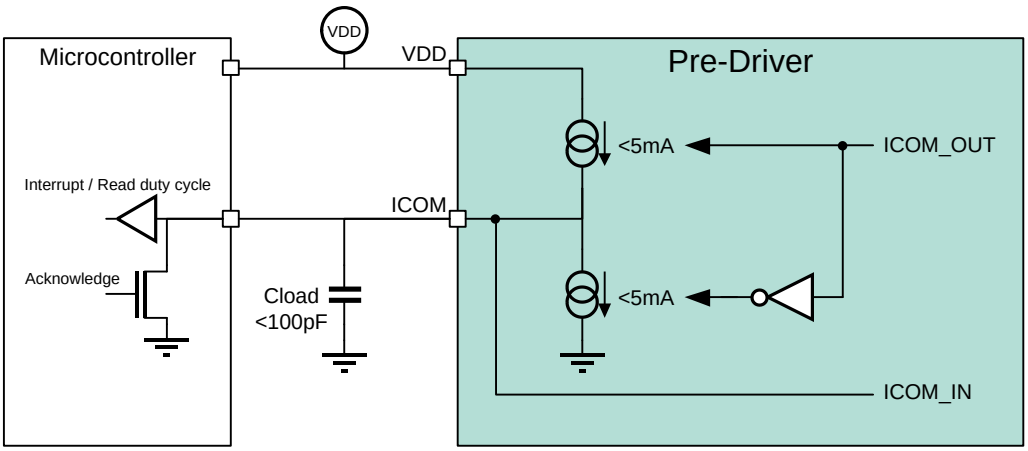

Figure 12-8 ICOM Diagnostics Interface

In case multiple errors occur at the same time, the priority is as defined in Table 12-7. The highest priority is 0 and 16 is the lowest priority.

Priority	Error Event	% Duty Cycle	Debounce Time	Description
11	ICOM_EOF	94.44 % (±1%)	n/a	End of frame
10	VDS_ERR	83.33 % (±1%)	2 µs	VDS Error = VDS_T1 | VDS_T2 | VDS_T3 | VDS_B1 | VDS_B2 | VDS_B3 This event can be masked by setting VDS_COMP_EN = 0 To avoid erroneous triggering due to switching there is a programmable blanking time on top of the debounce time: VDS_BLANK_TIME[1:0].
9	EEP_ERR	55.56 % (±1%)	n/a	EEPROM dual error detected
8	VDD_UV	50.00 % (±1%)	8 µs	VDD under voltage
7	VSUP_OV	44.44 % (±1%)	2 µs	VSUP over voltage
6	VSUP_UV	38.89 % (±1%)	8 µs	VSUP under voltage
5	OVT	33.33 % (±1%)	2 µs	OVT over temperature
4	VREG_UV	27.78 % (±1%)	16 µs	VREG under voltage
3	VGS_UV	22.22 % (±1%)	2 µs	VGS under voltage This event can be masked by setting VGS_UV_COMP_EN = 0
2	VBOOST_UV	16.67 % (±1%)	16 µs	VBOOST under voltage
1	VREG_OV	11.11 % (±1%)	2 µs	VREG over voltage This event can be masked by setting VGS_UV_COMP_EN = 0

Table 12-7 Overview Diagnostics over ICOM with Priority Definitions

12.5. EEPROM Configuration

The MLX83203-2 provides an EEPROM for configuration of the IC, the current sense amplifier and over current comparator, protection and diagnostic functions. This allows to optimize the pre-drivers' operation for the application requirements. The configuration can be done at customer production testing by using the PTC-04, or by the microcontroller via a custom program interface.

The EEPROM features single error correction and double error detection.

12.5.1. Memory Map

The MLX83203-2 comprises 6 bytes of EEPROM for user configurability. The first two bytes are not used for the internal configuration of the pre-driver, and can thus be used by the customer for traceability purposes. The other 4 bytes are used for configuration of the current sense amplifier and configuration of the diagnostics.

The pre-driver is programmed with default settings per table below.

Address	ED7	ED6	ED5	ED4	ED3	ED2	ED1	ED0
0	-	-	-	-	-	-	-	MLX
0x00	0	0	0	0	0	0	0	0
1	-	-	-	-	-	-	-	MLX
0x00	0	0	0	0	0	0	0	0
2	DEAD_TIME[2:0]			VDSMON[2:0]			CPMODE	MLX
0x7C	011			111			0	0
3	VDS_BLANK_TIME[1:0]		PWM_SPEED	-	CUR_GAIN[2:0]			MLX
0x86	10		0	0	011			0
4	VREG_OV _BF_EN	VDS _BF_EN	VDS _COMP_EN	VGS_UV _COMP_EN	EN_TCP	EN_CP	-	MLX
0xF4	1	1	1	1	0	1	0	0
5(-6-7)	SPI_EN	MLX	-	-	-	-	-	MLX
0xC0	1	1	0	0	0	0	0	0

Table 12-8 EEPROM Memory Map and Default Configuration

Bit Name	Description	Default
Configuration of the IC		
CPMODE	Defines the mode of operation of the internal charge pump 1: VBOOST voltage is regulated relative to VSUP for reverse polarity N-FET protection 0: VBOOST voltage is regulated relative to GND for low voltage operation with minimal power consumption	0
EN_CP	Defines the status of the pre-drivers' internal charge pump 1: Charge pump active 0: Charge pump not active	1
EN_TCP	Defines the status of the pre-drivers' trickle charge pump 1: Trickle charge pump active 0: Trickle charge pump not active	0
SPI_EN	Defines the accessibility of EEPROM through the custom SPI interface 1: EEPROM accessible via the custom SPI interface 0: EEPROM not accessible via the custom SPI interface	1
Configuration of the Current Sense Amplifier and Over Current Comparator		
CUR_GAIN[2:0]	Defines the gain of the current sense amplifier	011
Configuration of the Protection and Diagnostic Functions		
PWM_SPEED	Defines the diagnostics communication speed on ICOM 1: Fast mode for fastest response of microcontroller 0: Slow mode for low-end microcontrollers	0
VREG_OV_BF_EN	Defines the pre-drivers' reaction on a regulated supply over voltage: 1: Report VREG_OV on ICOM and disable gate drivers 0: Report VREG_OV on ICOM without effect on gate drivers	1
DEAD_TIME[2:0]	Defines the dead time between switching off high-side (low-side) N-FET and switching on complementary low-side (high-side) N-FET	011
VDSMON[2:0]	Defines the threshold level for the VDS monitoring of the external N-FETs	111
VDS_BLANK_TIME[1:0]	Defines the duration of the VDS blanking time after switching on the N-FET	10
VDS_COMP_EN	Defines the status of the pre-drivers' drain-source monitoring 1: Drain-source comparators active 0: Drain-source comparators not active	1
VDS_BF_EN	Defines the pre-drivers' reaction on a drain-source fault: 1: Report VDS_ERR on ICOM and disable gate drivers 0: Report VDS_ERR on ICOM without effect on gate drivers	1
VGS_UV_COMP_EN	Defines the status of the pre-drivers' gate-source monitoring 1: Drain-source comparators active 0: Drain-source comparators not active	1

Table 12-9 EEPROM Bit Description

12.5.2. “SPI Program Mode”

The EEPROM memory can be accessed through a custom SPI interface. It allows the user to read/program the EEPROM by the microcontroller in the application. This custom interface re-uses the low-side driver pins for SPI communication.

Since the same pins are used for both reading/writing the EEPROM and for controlling the motor, the EEPROM is only accessible when the motor is not running. Furthermore it is necessary to apply a certain sequence of conditions before the pre-driver will enter the “SPI Program Mode”. Once in this mode, the EEPROM can be accessed for reading and writing, until the IC enters “Normal Mode” again and motor operation is possible.

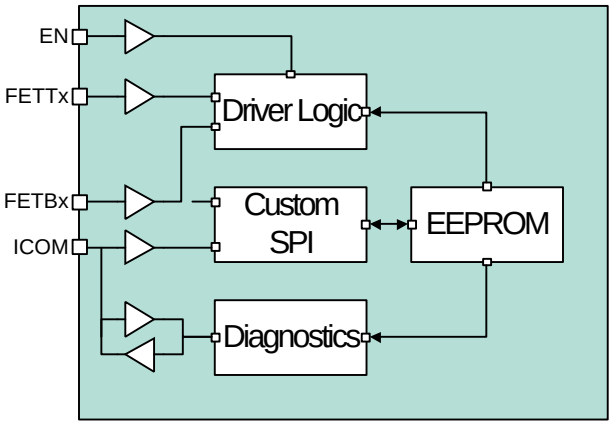

Figure 12-9 Custom SPI interface

Pin Name	SPI Signal	Description
ICOM	CSB	SPI-frames are defined by CSB low
FETB3	MOSI	The MOSI (Master Out – Slave In) shift register is reading in data on the rising edge of CLK
FETB2	CLK	Clock input, each SPI-frame has to consist of 16 clock periods
FETB1	MISO	The MISO (Master In – Slave Out) output is guaranteed to be stable while the CLK is low

Table 12-10 SPI Signals

The EEPROM controller refreshes the registers with the EEPROM conf. every 2ms (with same accuracy as the RCO). The loading of the EEPROM configuration in the configuration registers takes <100µs. During this loading, entry in SPI is forbidden, to guarantee valid data in the registers and to prevent the digital getting in a locked stage. If the pre-driver is in a locked stage, a POR is necessary. Therefore entry in SPI is advised after POR in a fixed window, as defined in Figure 12-10.

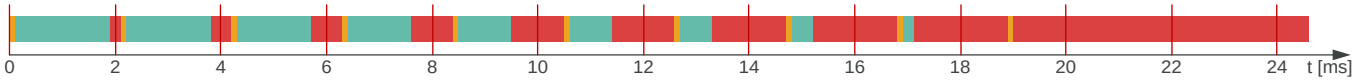

Figure 12-10 Entry in SPI mode after POR
(green = safe zone to enter SPI mode, red = accuracy of the 2ms timer, orange = loading time of 100us)

12.5.2.1. Entering "SPI Program Mode"

The MLX83203-2 enters "SPI Program Mode" when all below conditions are satisfied.

- ICOM
  - Any pending errors have been removed and acknowledged, so ICOM is in default high state
  - A low level pulse is applied on ICOM for a time t_{SPI_SU}
    At the end of this pulse, the rising edge, below conditions are checked as well
- EN = 0
- FETTx = Low (High-side FET inputs off) & FETBx = High (Low-side FET inputs off)

Note: To enter "SPI Program Mode" the MCU has to pull the FETB1-pin high. When the pre-driver enters this mode, the FETB1-pin becomes the MISO push-pull output pin with default low state. The MCU should release the FETB1/MISO-pin as soon as possible, as a current may be flowing from the MCU pin to the pre-driver pin. Make sure the current does not exceed the pre-drivers' max. specified MISO sink current and check potential effects on microcontroller side.

12.5.2.2. Exiting "SPI Program Mode"

The MLX83203-2 will exit the "SPI Program Mode" when the enable input EN is pulled high. Similar to when the MLX83203-2 comes out of POR, after leaving the "SPI Program Mode" the pre-driver is blocked until the data have been copied to the registers. Meaning that before entering "Normal Mode" the EEPROM write will be completed and the EEPROM state machine will copy all EEPROM contents into registers. During this time ICOM is kept low. When it returns to its default high state the pre-driver is ready for normal operation.

12.5.2.3. Protocol

Once the IC is in "SPI Program Mode" the microcontroller can read/write the EEPROM, following the protocol depicted below.

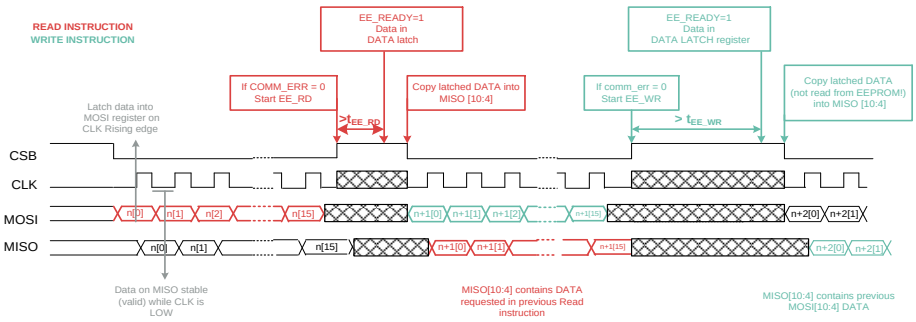

Figure 12-11 SPI Protocol (LSB first)

12.5.2.4. Registers Description

MOSI [15:0]							
Bit [15]	Bit [14]	Bit [13]	Bit [12]	Bit [11]	Bit [10]	Bit [9]	Bit [8]
MOSI_PAR	x	x	CMD [1:0]		MOSI_DATA [7:5]		
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
MOSI_DATA [4:1]				x	ADDRESS [2:0]		

Table 12-11 MOSI frame description

MISO[15:0]							
Bit [15]	Bit [14]	Bit [13]	Bit [12]	Bit [11]	Bit [10]	Bit [9]	Bit [8]
MISO_PAR	COMM_ERR	EE_READY	CMD [1:0]		MISO_DATA [7:5]		
Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
MISO_DATA [4:1]				x	ADDRESS [2:0]		

Table 12-12 MISO frame description

Bit	Description
ADDRESS	Address of the byte in EEPROM that needs to be read/written to.
MOSI_DATA[7:1]	In case of write command, the data that needs to be written. Don't care for any read command.
MISO_DATA[7:1]	In case previous command was write instruction, it returns the data that was written. In case of a read instruction, it returns the data read from EEPROM.
CMD [1:0]	Read/Write command 00: EE_RD: Read command 01: EE_WR: Write command 10: EE_RDAW1 11: EE_RDAW2
EE_READY	Reading/writing the EEPROM takes a certain time, specified by t_{EE_RD} and t_{EE_WR} respectively. These times define the minimum time CSB (ICOM) has to remain high between two SPI-frames in order to finish the read/ write action. As soon as the read/write action starts, the EE_READY bit is reset. After completion of the read/write action the bit is set. If the read/write delay between SPI-frames was long enough to execute the read/write action, the EE_READY bit will thus be set, signaling the read/write action was finished. If the time was too short, the bit will still be 0.
COMM_ERR	This bit indicates if the previous MOSI-frame was received correctly. If no communication error occurred the bit will be reset, and the read/write action was started as soon as CSB was pulled high. If a communication error occurred in the previous MOSI-frame the read/write command was not executed. Possible communication errors are: Odd parity bit was set incorrect Number of clock periods was not equal to 16
MOSI_PAR, MISO_PAR	Odd parity bit of the current MOSI/MISO frame.

Table 12-13 MOSI/MISO frames bit description

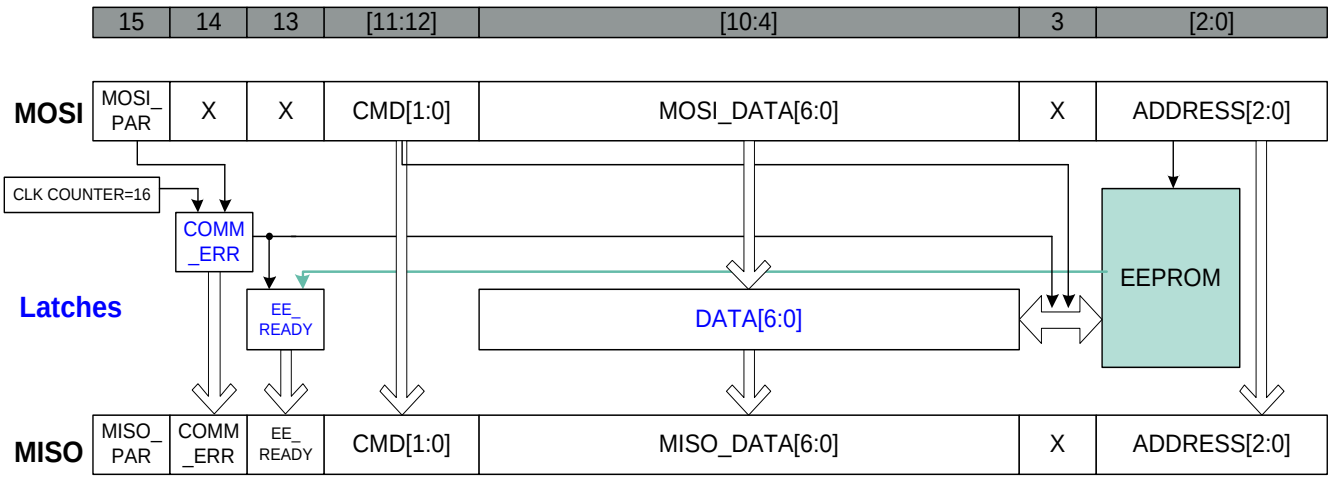

Figure 12-12 MOSI/MISO registers and relation to internal data latches

12.5.2.5. Read Instruction

In order to read one of the EEPROM bytes, the microcontroller should compose the MOSI(N) frame according to Table 12-11 with the address it wants to read, the read command and set the odd parity bit in a correct way.

After transmission of this MOSI(N)-frame and when the CSB signal is pulled high, the pre-driver will start to read the data at the specific address. If CSB is kept high long enough for the pre-driver to execute the read action, it will transmit the read data on the next MISO(N+1)-frame.

The data in this MISO(N+1)-frame is valid only if

- COMM_ERR = 0 : no communication error was detected on the previous MOSI(N)-frame
- EE_READY = 1 : the read delay was long enough to finish the read
- MISO_PAR = correct : the MISO(N+1)-frame has a correct odd parity bit

12.5.2.6. Write Instruction

The MLX83203-2 provides different configuration options through the EEPROM programming. In order to program one of the EEPROM bytes, the microcontroller should compose the MOSI(N) frame according to Table 12-11 with the address and data it wants to write, the write command and set the odd parity bit in a correct way.

After transmission of this MOSI(N)-frame and when the CSB signal is pulled high, the pre-driver will start to write the data at the specific address. If CSB is kept high long enough the pre-driver will be able to complete the write instruction.

In total three verification steps are possible in order to ensure successful writing of the EEPROM. On the first MISO-frame after the write command, it can be checked if the write command is received correctly and the correct address and data are used. In the next two MISO-frames the data written in EEPROM can be read in order to guarantee the desired data has been written in EEPROM

- Verification Step 1: Correct receive of the write instruction using the MISO(N+1)-frame
  - COMM_ERR = 0 : no communication error detected on MOSI(N)-write command
  - EE_READY = 1 : the write delay was long enough to finish the write instruction
  - MISO_PAR = correct : the MISO(N+1)-frame has a correct odd parity bit
  - MISO_DATA(N+1) = MOSI_DATA(N) : the correct data was used for the write instruction

- Verification Step2: EE_RDAW1 using the MISO(N+2)-frame
  - COMM_ERR = 0 : no communication error detected on MOSI(N+2)-RDAW1 command
  - EE_READY = 1 : the read delay was long enough to finish the read instruction
  - MISO_PAR = correct : the MISO(N+2)-frame has a correct odd parity bit
  - MISO_DATA(N+2) = MOSI_DATA(N) : the correct data is written

- Verification Step3: EE_RDAW2 using the MISO(N+3)-frame
  - COMM_ERR = 0 : no communication error detected on MOSI(N+3)-RDAW2 command
  - EE_READY = 1 : the read delay was long enough to finish the read instruction
  - MISO_PAR = correct : the MISO(N+3)-frame has a correct odd parity bit
  - MISO_DATA(N+3) = MOSI_DATA(N) : the correct data is written

13. ESD Protection

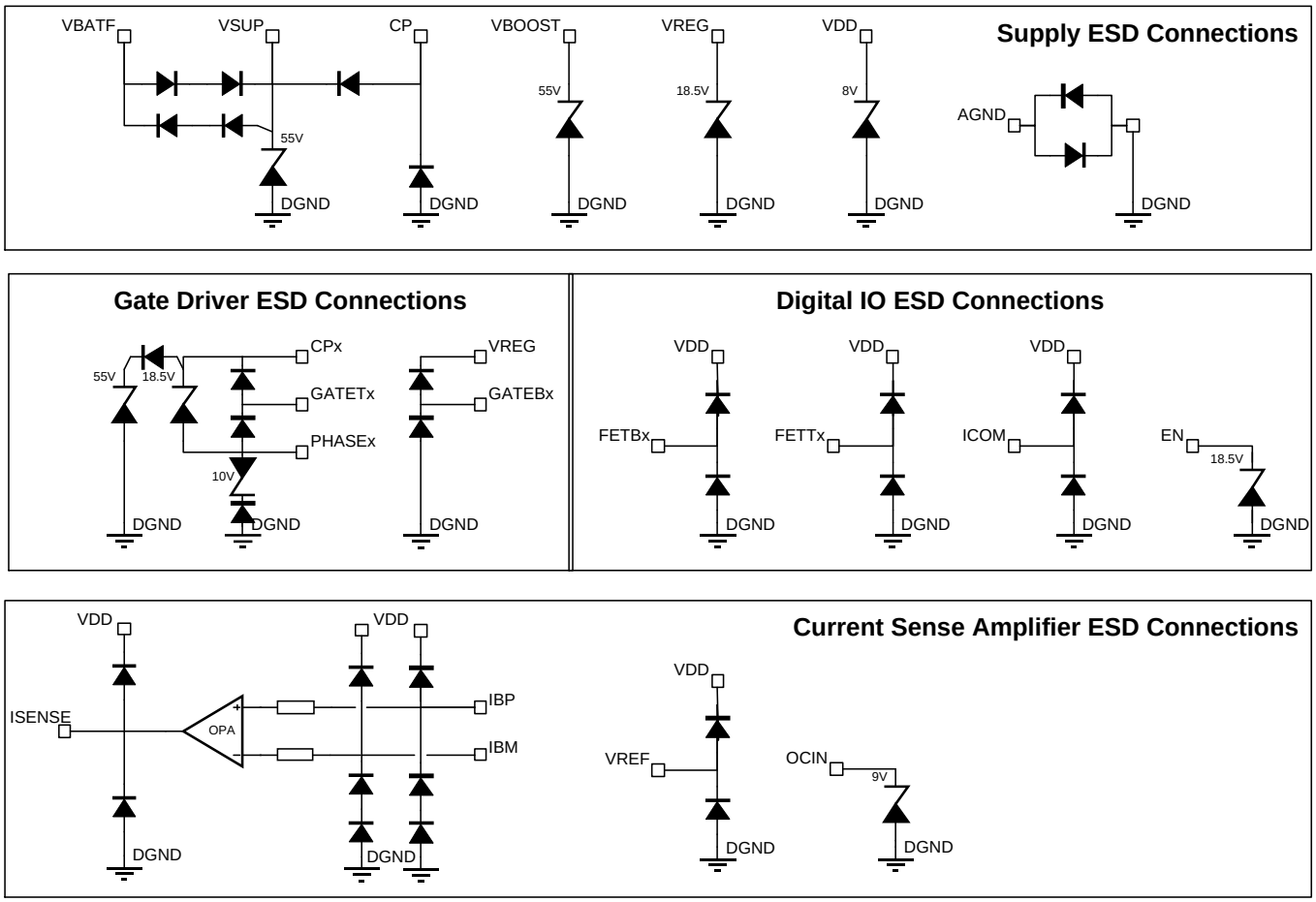

Figure 13-1 Principle Schematic highlighting ESD Connections

Note:

All pins are referenced to the driver ground DGND as depicted in the picture above, but only for the ESD protection.

14. Package Information

14.1. Package Marking

Product name: MLX83203DD or MLX83202DD

Lot number:	xxxxxx	format free
Date code:	yyww	year and week

Figure 14-1 Package marking

14.2. Package Data

	A	A1	A3	D	E	D2	E2	L	K	b	e
Min	0.80	0	0.2 REF	4.90	4.90	3.50	3.50	0.30	0.20	0.18	0.50 BSC
Nom.	0.90	0.025		5.00	5.00	3.60	3.60	0.40	-	0.25	
Max.	1.00	0.050		5.10	5.10	3.70	3.70	0.50	-	0.30	

Table 14-1 Mechanical dimensions

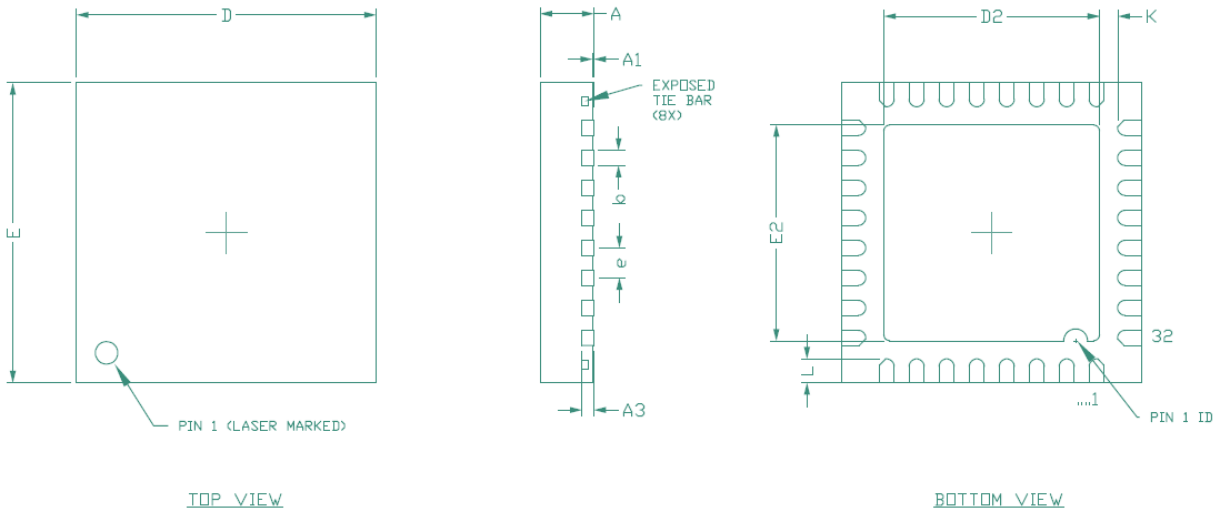

Figure 14-2 Package drawing and mechanical dimensions

15. Revision History

Revision	Date	Description
1.0	01-02-12	▪ Initial Draft version
1.1	01-03-12	▪ EE_RD meaning in SPI description corrected ▪ RDSon specification split up in ON/OFF ▪ Added RDSon for 83202 variant ▪ Added package marking
1.2	28-03-12	▪ TQFP48 pin out included
1.3	15-05-12	▪ Added appl. Schematics, Pin internal structures, updated block diagram ▪ Updated SPI enabling. ▪ Updated ICOM duty cycles ▪ Updated sleep mode ▪ Updated leakage spec on VBATF
		▪ Max voltage on all pins
1.4	03-07-12	▪ Final package dimensions
1.5	28-11-12	▪ Parameters updated per test data ▪ Device description updated
1.6	21-12-12	▪ Information about DC variant of pre-driver moved to separate datasheet
1.7	15-01-13	▪ Protection and diagnostic functions updated
2.0	26-02-13	▪ Customer release
2.1	06-05-13	▪ Max voltage on phase pins updated
2.2	04-12-13	▪ Entering SPI mode by disabling all 6x FET input signals
2.3	01-03-14	▪ Temperature codes for ordering information updated ▪ Abs. max. rating updated ▪ Driver stage specification for 83202 variant added ▪ Block diagram and application diagrams updated ▪ Changed ICOM duty cycle for VDS_ERR from 5.5% to 82.5%
3.0	09-05-14	▪ General update according to new template
3.1	24-07-14	▪ Drain-source monitor blanking ▪ Largest dead time value ▪ ICOM pull-up current
4.0	31-07-14	▪ Performance graphs added
4.1	02-11-15	▪ TQFP version cancelled

4.2	18-12-15	▪ Electrical specifications updated
		  ▪ Operating current from V_{SUP} (with PWM operation)
		  ▪ VSUP under and over voltage hysteresis
		  ▪ Internal leakage from V_{BATF} to GND
		  ▪ V_{DD} operating current
		  ▪ Drivers resistance for MLX83202
		  ▪ Discharge currents for V_{BOOST} and V_{CPx} specified in case of V_{SUP_OVH}
		▪ Ordering information is updated
		▪ Package information updated

4.3	17-03-16	▪ “Data in hold time” and “Data out ready delay” units corrected to ns
4.4	31-08-16	▪ Default EEPROM configuration corrected for PWM_SPEED ▪ Minimum specification on input PWM frequency removed ▪ Drain-source voltage monitoring description updated with pin-description
5.0	01-09-16	▪ New Melexis template
5.1	13-12-16	▪ No reduced gate drive voltage for higher extended supply range
5.2	28-06-17	▪ Package marking updated
5.4	13-03-19	▪ Order code and package marking updated for DCA-version ▪ ICOM Duty cycles corrected, added duty cycle accuracy ▪ Entry in SPI mode after POR specified ▪ TCP Removed ▪ Package dimensions updated
5.6	26-06-19	▪ “General Electrical Specifications”: VDS_BLANK_TIME options reversed
5.7	11-06-20	▪ “Entering SPI Program Mode” updated including MISO-pin note ▪ “General Electrical Specifications”: MISO push-pull stage specification
5.8	15-12-20	▪ Order code and package marking updated for DDA-version ▪ TCP Description updated
5.9	13-04-21	▪ TCP performance graph included ▪ Max. VBATF-VSUP voltage specified for IC versions before DDA

Table 15-1 Revision history

16. Standard Information

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to standards in place in Semiconductor industry.

For further details about test method references and for compliance verification of selected soldering method for product integration, Melexis recommends reviewing on our web site the General Guidelines soldering recommendation. For all soldering technologies deviating from the one mentioned in above document (regarding peak temperature, temperature gradient, temperature profile etc), additional classification and qualification tests have to be agreed upon with Melexis.

For package technology embedding trim and form post-delivery capability, Melexis recommends to consult the dedicated trim&form recommendation application note: lead trimming and forming recommendations

Melexis is contributing to global environmental conservation by promoting lead free solutions. For more information on qualifications of RoHS compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website: http://www.melexis.com/en/quality-environment

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