EVB71120

300 to 930MHz Receiver Evaluation Board Description



Features and Benefits

- Dual RF input for antenna space and frequency diversity, LNA cascading or differential feeding
- Fully integrated PLL-based synthesizer
- 2nd mixer with image rejection
- Reception of ASK or FSK modulated signals
- Wide operating voltage and temperature ranges
- Very low standby current consumption
- Low operating current consumption
- External IF filters 455kHz or 10.7MHz
- Internal FSK demodulator
- Average or peak detection data slicer mode
- RSSI output with high dynamic range for RF level indication
- Output noise cancellation filter
- MCU clock output
- High over-all frequency accuracy

Application Examples

- General digital and analog RF receivers at 300 to 930MHz
- Tire pressure monitoring systems (TPMS)
- Remote keyless entry (RKE)
- Low power telemetry systems
- Alarm and security systems
- Active RFID tags
- Remote controls
- Garage door openers
- Home and building automation

Ordering information

Part No. (see paragraph 4)

EVB71120-315-C EVB71120-433-C EVB71120-868-C EVB71120-915-C

Note 1: Peak detection mode, IF2 selection = 10.7MHz is default population.

General Description

The MLX71120 is a multi-band, single-channel RF receiver based on a double-conversion superheterodyne architecture. It can receive FSK and ASK modulated signals. The IC is designed for general purpose applications for example in the European bands at 433MHz and 868MHz or for similar applications in North America or Asia, e.g. at 315MHz or 915MHz. It is also well-suited for narrow-band applications according to the ARIB STD-T67 standard in the frequency range 426MHz to 470MHz.

The receiver's extended temperature and supply voltage ranges make the device a perfect fit for automotive or similar applications where harsh environmental conditions are expected.

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1. Theory of Operation

1.1. General

The MLX71120 receiver architecture is based on a double-conversion super-heterodyne approach. The two LO signals are derived from an on-chip integer-N PLL frequency synthesizer. The PLL reference frequency is derived from a crystal (XTAL). As the first intermediate frequency (IF1) is very high, a reasonably high degree of image rejection is provided even without using an RF front-end filter. At applications asking for very high image rejections, cost-efficient RF front-end filtering can be realized by using a SAW filter in front of the LNA. The second mixer MIX2 is an image-reject mixer.

The receiver signal chain is setup by one (or two) low noise amplifier(s) (LNA1, LNA2), two down-conversion mixers (MIX1, MIX2) and an external IF filter with an on-chip amplifier (IFA). By choosing the required modulation via an FSK/ASK switch (at pin MODSEL), either the on-chip FSK demodulator (FSK DEMOD) or the RSSI-based ASK detector is selected. A second order data filter (OA1) and a data slicer (OA2) follow the demodulator. The data slicer threshold can be generated from the mean-value of the data stream or by means of the positive and negative peak detectors (PKDET+/-). A digital post-processing of the sliced data signal can be performed by a noise filter (NF) building block.

The dual LNA configuration can be used for antenna space diversity or antenna frequency diversity or to setup an LNA cascade (to further improve the input sensitivity). The two LNAs can also be setup to feed the RF signal differentially.

A sequencer circuit (SEQ) controls the timing during start-up. This is to reduce start-up time and to minimize power dissipation.

A clock output, which is a divide-by-8 version of the crystal oscillator signal, can be used to drive a microcontroller. The clock output is open drain and gets activated through a load connected to positive supply.

1.2. Technical Data Overview

Input frequency ranges:

- 300 to 470MHz
- G10 to 930MHz
- Power supply range: 2.1 to 5.5V
- Temperature range: -40 to +125°C
- Shutdown current: 50 nA
- Operating current: 6.5 to 8.1mA
- Selectable IF2 frequency: 10.7MHz or 455kHz
- FSK deviation range:
 - □ ±10kHz to ±100kHz (WB)
 - □ ±2kHz to ±10kHz (NB)

- Image rejection:
 - □ 65dB 1st IF (with external RF frontend filter)
 - 25dB 2nd IF (internal image rejection)
- Maximum data rate:
 - 50kps RZ (bi-phase) code,
 - 100kps NRZ
- Spurious emission: < -54dBm
- Linear RSSI range: > 70dB
- Crystal reference frequency: 16 to 27MHz
- MCU clock frequency: 2.0 to 3.4

| D Input Sensitivity: at 4kbps NRZ, BER = $3 \cdot 10^{-3}$ | | | | | |
|---|--|---------|------------|-----------|---------|
| | Frequency | 315 MHz | 433.92 MHz | 868.3 MHz | 915 MHz |
| FSK | wide band 180kHz BW, IF2=10.7MHz Δf = ±20kHz | -109dBm | -108dBm | -106dBm | -104dBm |
| FSK | narrow band 20kHz BW, IF2=455kHz $\Delta { m f}$ = ± 5 kHz | -114dBm | -112dBm | -111dBm | -109dBm |
| ASK | wide band 180kHz BW, IF2=10.7MHz | -113dBm | -113dBm | -111dBm | -109dBm |

Note: - Sensitivities given for RF input 1 (without SAW filter)

- Sensitivity for RF input 2 is about 2 to 3dB worse (because of SAW filter loss)



1.3. Block Diagram

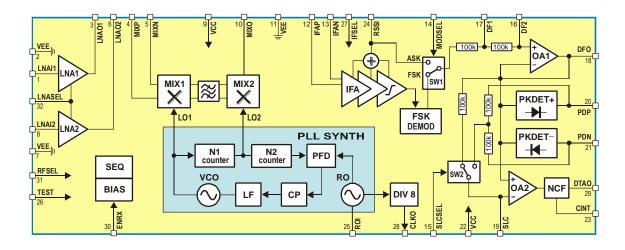


Fig. 1: MLX71120 block diagram

The MLX71120 receiver IC consists of the following building blocks:

- PLL synthesizer (PLL SYNTH) to generate the first and second local oscillator signals LO1 and LO2. The PLL SYNTH consists of a fully integrated voltage-controlled oscillator (VCO), a distributed feedback divider chain (N1, N2), a phase-frequency detector (PFD) a charge pump (CP), a loop filter (LF) and a crystal-based reference oscillator (RO).
- Two low-noise amplifiers (LNA) for high-sensitivity RF signal reception
- First mixer (MIX1) for down-conversion of the RF signal to the first IF (intermediate frequency)
- Second mixer (MIX2) with image rejection for down-conversion from the first to the second IF
- IF amplifier (IFA) to provide a high voltage gain and an RSSI signal output
- FSK demodulator (FSK DEMOD)
- Operational amplifiers OA1 and OA2 for low-pass filtering and data slicing, respectively
- Positive (PKDET+) and negative (PKDET-) peak detectors
- Switches SW1 to select between FSK and ASK as well as SW2 to chose between averaging or peak detection mode.
- Noise cancellation filter (NF)
- Sequencer circuit (SEQ) and biasing (BIAS) circuit
- Clock output (DIV8)

1.4. Operating Modes

| ENRX | Description | | |
|------|---------------|--|--|
| 0 | Shutdown mode | | |
| 1 | Receive mode | | |

Note: ENRX is pulled down internally.



1.5. Frequency Range

Two different receive frequency ranges can be selected by the control signal RFSEL.

| RFSEL | Description |
|-------|-------------------------------------|
| 0 | Input frequency range 300 to 470MHz |
| 1 | Input frequency range 610 to 930MHz |

1.6. LNA Selection

| LNASEL | Description | | |
|--------|----------------------------|--|--|
| 0 | LNA1 active, LNA2 shutdown | | |
| Hi-Z | LNA1 and LNA2 active | | |
| 1 | LNA1 shutdown, LNA2 active | | |

Note: Hi-Z state means pin LNASEL is left floating (pin is internally pulled to $V_{CC}/2$ in this case).

1.7. External IF2 Selection

| IFSEL | Description |
|-------|----------------|
| 0 | IF2 = 455 kHz |
| 1 | IF2 = 10.7 MHz |

1.8. Demodulation Selection

| MODSEL | Description | | |
|--------|------------------|--|--|
| 0 | ASK demodulation | | |
| 1 | FSK demodulation | | |

1.9. Data Slicer

| SLCSEL | Description |
|--------|--------------------------|
| 0 | Averaging detection mode |
| 1 | Peak detection mode |



2. Frequency Planning

Because of the double conversion architecture that employs two mixers and two IF signals, there are four different combinations for injecting the LO1 and LO2 signals:

- LO1 high side and LO2 high side: receiving at f_{RF}(high-high)
- LO1 high side and LO2 low side: receiving at $f_{\rm RF}({\rm high}{-}{\rm low})$
- LO1 low side and LO2 high side: receiving at $f_{\mbox{\tiny RF}}(\mbox{low-high})$
- LO1 low side and LO2 low side: receiving at $\rm f_{\rm RF}(low-low)$

As a result, four different radio frequencies (RFs) could yield one and the same second IF (IF2). Fig. 2 shows this for the case of receiving at f_{RF} (high-high). In the example of Fig. 2, the image signals at f_{RF} (low-high) and f_{RF} (low-low) are suppressed by the bandpass characteristic provided by the RF front-end. The bandpass shape can be achieved either with a SAW filter (featuring just a couple of MHz bandwidth), or by the tank circuits at the LNA input and output (this typically yields 30 to 60MHz bandwidth). In any case, the high value of the first IF (IF1) helps to suppress the image signals at f_{RF} (low-high) and f_{RF} (low-low).

The two remaining signals at IF1 resulting from f_{RF} (high-high) and f_{RF} (high-low) are entering the second mixer MIX2. This mixer features image rejection with so-called single-sideband (SSB) selection. This means either the upper or lower sideband of IF1 can be selected. In the example of Fig. 2, LO2 high-side injection has been chosen to select the IF2 signal resulting from f_{RF} (high-high).

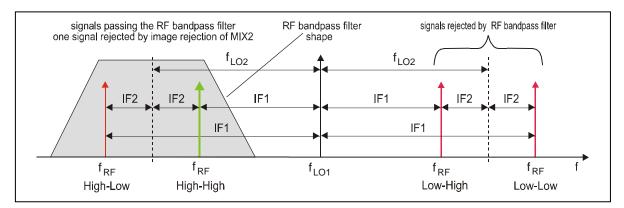


Fig. 2: The four receiving frequencies in a double conversion superhet receiver

It can be seen from the block diagram of Fig. 1 that there is a fixed relationship between the LO signal frequencies (f_{LO1} , f_{LO2}) and the reference oscillator frequency f_{RO} .

$$\mathbf{f}_{\text{LO1}} = \mathbf{N}_1 \cdot \mathbf{f}_{\text{LO2}} \qquad \qquad \mathbf{f}_{\text{LO2}} = \mathbf{N}_2 \cdot \mathbf{f}_{\text{RO}}$$

The IF2 frequency can be selected to 455kHz or 10.7MHz via the logic level at the IFSEL control pin. At the same time the output impedance of the 2nd mixer at pin MIXO is set according to the IF2 (please refer to pin description for details). Of course, also the operating frequency of the FSK demodulator (FSK DEMOD) is set accordingly.



2.1. Calculation of Frequency Settings

The receiver has two predefined receive frequency plans which can be selected by the RFSEL control pin. Depending on the logic level of RFSEL pin the sideband selection of the second mixer and the counter settings for N1 and N2 are changed accordingly. (see in 1.5)

| RFSEL | Injection | f _{RFmin} [MHz] | f _{RFmax} [MHz] | N1 | N ₂ |
|-------|-----------|--------------------------|--------------------------|----|----------------|
| 0 | high-low | 300 | 470 | 4 | 6 |
| 1 | low-high | 610 | 930 | 2 | 12 |

The following table shows the relationships of several internal receiver frequencies for the two input frequency ranges.

| f _{RF} [MHz] | f _{IF1} | f _{L01} | f _{LO2} | f _{RO} |
|-----------------------|---|---|--|---|
| 300 to 470 | $\frac{\mathbf{f}_{\mathrm{RF}} + \mathbf{N}_{1}\mathbf{f}_{\mathrm{IF2}}}{\mathbf{N}_{1} - 1}$ | $\frac{N_{1}(f_{RF} + f_{IF2})}{N_{1} - 1}$ | $\frac{f_{\text{RF}}+f_{\text{IF2}}}{N_1-1}$ | $\frac{f_{\rm RF} + f_{\rm IF2}}{N_2(N_1 - 1)}$ |
| 610 to 930 | $\frac{\mathbf{f}_{\text{RF}} - \mathbf{N}_{1}\mathbf{f}_{\text{IF2}}}{\mathbf{N}_{1} + 1}$ | $\frac{N_{1}(f_{RF} + f_{IF2})}{N_{1} + 1}$ | $\frac{f_{\rm RF}+f_{\rm IF2}}{N_1+1}$ | $\frac{f_{\rm RF} + f_{\rm IF2}}{N_2(N_1 + 1)}$ |

Given IF2 is selectable at either 455kHz or 10.7MHz and the corresponding N_1 , N_2 counter settings, above equations can be transferred into the following table.

IF2=455kHz

| f _{RF} [MHz] | f _{IF1} | f _{LO1} | f _{LO2} | f _{RO} |
|-----------------------|-------------------------------|----------------------------------|-----------------------------------|--------------------------------|
| 300 to 470 | $f_{\rm RF}$ + 1.82MHz | $\frac{4(f_{RF} + 0.455MHz)}{2}$ | | $\frac{f_{RF} + 0.455MHz}{10}$ |
| | 3 | 3 | $\underline{f_{RF}} + 0.455 M Hz$ | 18 |
| 610 to 930 | $\frac{f_{RF} - 0.91 MHz}{3}$ | $\frac{2(f_{RF} + 0.455MHz)}{3}$ | 3 | $\frac{f_{RF} + 0.455MHz}{36}$ |

IF2=10.7MHz

| f _{RF} [MHz] | f _{IF1} | f _{LO1} | f _{LO2} | f _{RO} |
|-----------------------|------------------------------|---------------------------------|----------------------|---------------------------------|
| 300 to 470 | $\frac{f_{RF} + 42.8MHz}{3}$ | $\frac{4(f_{RF}+10.7MHz)}{3}$ | $f_{RF} + 10.7 M Hz$ | $\frac{f_{RF} + 10.7 M Hz}{18}$ |
| 610 to 930 | $\frac{f_{RF} - 21.4MHz}{3}$ | $\frac{2(f_{RF} + 10.7MHz)}{3}$ | 3 | $\frac{f_{RF} + 10.7 M Hz}{36}$ |



2.2. Standard Frequency Plans

IF2 = 455kHz

| f _{RF} [MHz] | f _{iF1} [MHz] | f _{L01} [MHz] | f _{LO2} [MHz] | f _{RO} [MHz] |
|-----------------------|------------------------|------------------------|------------------------|-----------------------|
| 315 | 105.6067 | 420.6067 | 105.1517 | 17.525277 |
| 433.92 | 145.2467 | 579.1667 | 144.7917 | 24.131944 |
| 868.3 | 289.1300 | 579.1700 | 289.5850 | 24.132083 |
| 915 | 304.6967 | 610.3033 | 305.1517 | 25.429305 |

IF2 = 10.7MHz

| f _{RF} [MHz] | f _{iF1} [MHz] | f _{L01} [MHz] | f _{LO2} [MHz] | f _{ro} [MHz] |
|-----------------------|------------------------|------------------------|------------------------|-----------------------|
| 315 | 119.2667 | 434.2667 | 108.5667 | 18.094444 |
| 433.92 | 158.0667 | 592.8267 | 148.2067 | 24.701111 |
| 868.3 | 282.3000 | 586.0000 | 293.0000 | 24.416666 |
| 915 | 297.8667 | 617.1333 | 308.5667 | 25.713888 |

2.3. 433/868MHz Frequency Diversity

The receiver's multi-band functionality can be used to operate at two different frequency bands just by changing the logic level at pin RFSEL and without changing the crystal. This feature is applicable for common use of the 433 and 868MHz bands. Below table shows the corresponding frequency plans.

IF2 = 455kHz

| RFSEL | f _{RF} [MHz] | f _{IF1} [MHz] | f _{LO1} [MHz] | f _{LO2} [MHz] | f _{RO} [MHz] | |
|-------|-----------------------|------------------------|------------------------|------------------------|-----------------------|--|
| 0 | 433.9225 | 145.2483 | 579.17 | 144.7925 | 24 4 2 2 0 0 2 | |
| 1 | 868.3 | 289.1300 | 579.17 | 289.5850 | 24.132083 | |



3. Dual-Channel Application Circuits for FSK & ASK Reception

3.1. Peak Detector Data Slicer

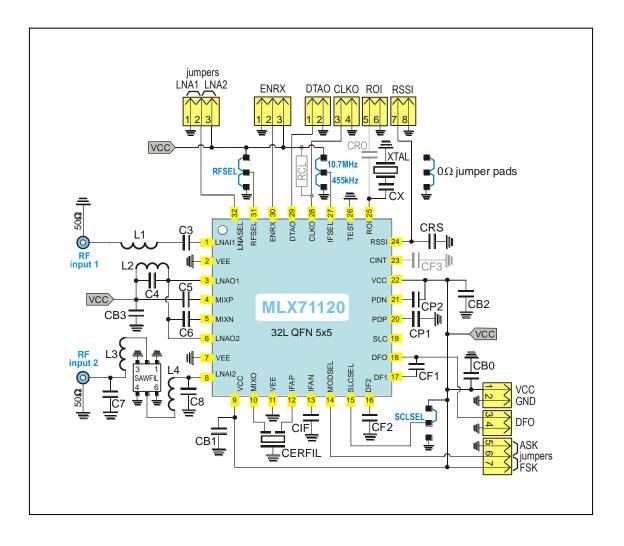


Fig. 3: Circuit schematic



3.1.1. Component Arrangement Top Side (Peak Detection Data Slicer, IF2 = 10.7MHz)

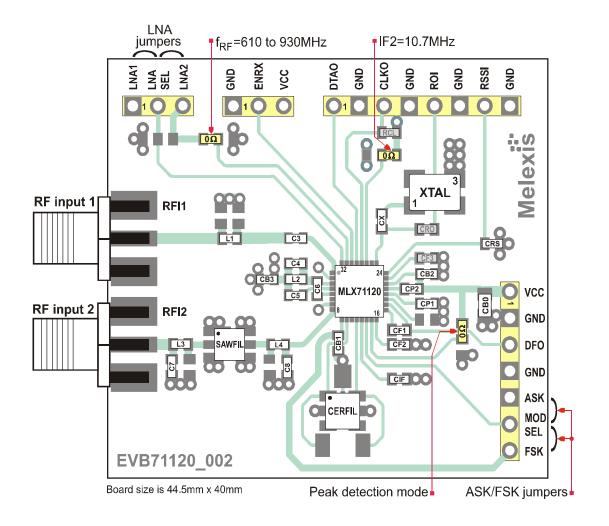


Fig. 4: PCB top-side view



3.1.2. Component Arrangement Top Side (Peak Detection Data Slicer, IF2 = 455kHz)

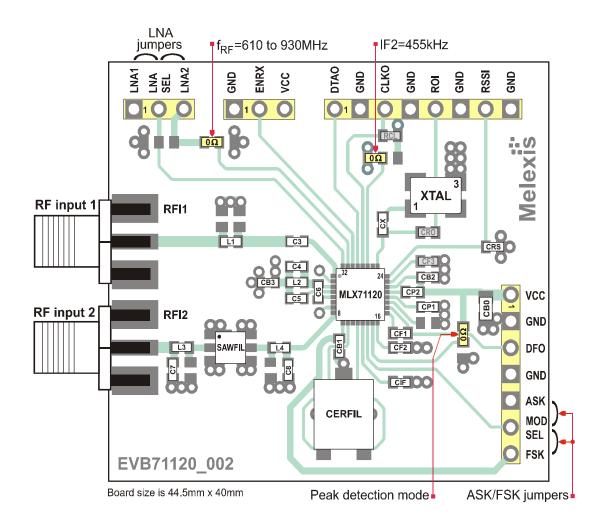


Fig. 5: PCB top-side view



3.2. Averaging Data Slicer Configured for Bi-Phase Codes

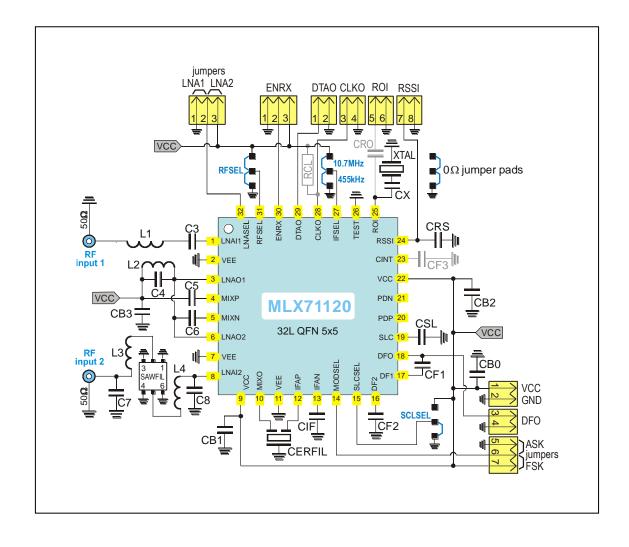


Fig. 6: Circuit schematic



300 to 930MHz Receiver Evaluation Board Description

3.2.1. Component Arrangement Top Side (Averaging Data Slicer, IF2 = 10.7MHz)

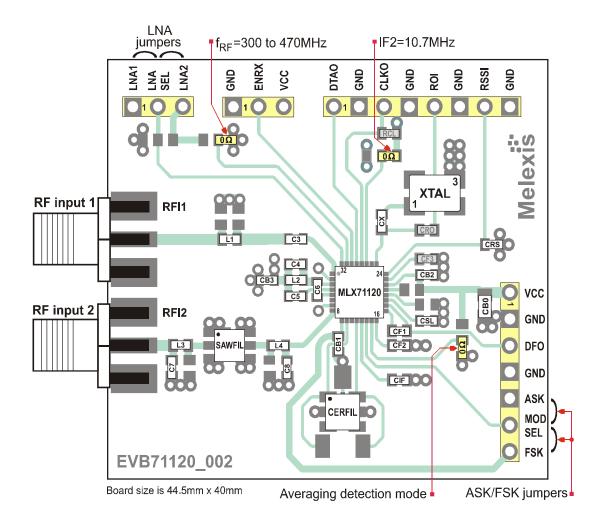


Fig. 7: PCB top-side view

300 to 930MHz Receiver Evaluation Board Description

3.3. Component List for Dual-Channel Application

Below table is valid for test circuits shown in Figures 3.1 to 3.2.

| DEIUW | | | cuits snown in F | igui es 5.1 (0 5 | | | | | |
|-------|-----------------|---------------------------|----------------------------------|--------------------------------------|---------------------------|------|--|------------------------------------|--|
| Part | Size | Value @ 315 MHz | Value @ 433.92 MHz | Value @ Value @ 868.3 MHz 915 MHz | | Tol. | | Description | |
| C3 | 0603 | 100 pF | 100 pF | 100 pF | 100 pF | ±5% | LNA input filteri | ng capacitor | |
| C4 | 0603 | 4.7 pF | 3.9 pF | 2.2 pF | 1.5 pF | ±5% | LNA output tank capacitor | | |
| C5 | 0603 | 100 pF | 100 pF | 100 pF | 100 pF | ±5% | MIX1 positive input matching capacitor | | |
| C6 | 0603 | 100 pF | 100 pF | 100 pF | 100 pF | ±5% | MIX1 negative input matching capacitor | | |
| C7 | 0603 | NIP | 4.7 pF | 3.9 pF | NIP | ±5% | matching capacitor | | |
| C8 | 0603 | NIP | NIP | 1.0 pF | NIP | ±5% | matching capacitor | | |
| CB0 | 0805 | 330 nF | 330 nF | 330 nF | 330 nF | ±10% | decoupling capa | acitor | |
| CB1 | 0603 | 330 pF | 330 pF | 330 pF | 330 pF | ±10% | decoupling capa | acitor | |
| CB2 | 0603 | 330 pF | 330 pF | 330 pF | 330 pF | ±10% | decoupling capa | acitor | |
| CB3 | 0603 | 330 pF | 330 pF | 330 pF | 330 pF | ±10% | decoupling capa | acitor | |
| CF1 | 0603 | 680 pF | 680 pF | 680 pF | 680 pF | ±10% | data low-pass fi for data rate of | | |
| CF2 | 0603 | 330 pF | 330 pF | 330 pF | 330 pF | ±10% | data low-pass fi for data rate of | | |
| CE2 | 0602 | | value according t | to the data rate | • | ±10% | ontional canacit | or for poice cancellation filter | |
| CF3 | 0603 | cor | nnected to ground if | f noise filter not u | sed | ±10% | optional capacit | or for noise cancellation filter | |
| CIF | 0603 | 1 nF | 1 nF | 1 nF | 1 nF | ±10% | IFA feedback ca | pacitor | |
| CP1 | 0603 | 33 nF | 33 nF | 33 nF | 33 nF | ±10% | positive PKDET capacitor, for data rate of 4 kbps NRZ | | |
| CP2 | 0603 | 33 nF | 33 nF | 33 nF | 33 nF | ±10% | negative PKDET capacitor, for data rate of 4 kbps NRZ | | |
| CRS | 0603 | 1 nF | 1 nF | 1 nF | 1 nF | ±10% | RSSI output low pass capacitor | | |
| CRO | 0603 | 1 nF | 1 nF | 1 nF | 1 nF | ±5% | optional capacitor, to couple external RO signal | | |
| CSL | 0603 | 100 nF | 100 nF | 100 nF | 100 nF | ±10% | data slicer capacitor, | | |
| CJL | 0005 | | for averaging dete | ction mode only | | 10/0 | for data rate of | 4 kbps NRZ | |
| СХ | 0603 | 27 pF | 27 pF | 27 pF | 27 pF | ±5% | crystal series capacitor | | |
| L1 | 0603 | 56 nH | 27 nH | 0 Ω | 0 Ω | ±5% | matching inductor | | |
| L2 | 0603 | 27 nH | 15 nH | 3.9 nH | 3.9 nH | ±5% | LNA output tank | rinductor | |
| L3 | 0603 | 0 Ω | 47 nH | 22 nH | 0 Ω | ±5% | matching induct | or | |
| L4 | 0603 | 56 nH | 68 nH | 22 nH | 0 Ω | ±5% | matching induct | or | |
| RCL | 0603 | 3.3 kΩ | 3.3 kΩ | 3.3 kΩ | 3.3 kΩ | ±5% | optional CLK ou to clock output | tput resistor, signal generated | |
| SAW | SMD | SAFDC315M | RF3446 | SAFCC868M | SAFCC915M | | low-loss SAW fil | ter from Murata | |
| FIL | 3x3 | SM0T00 (315 MHz) | (433.92 MHz) | SL0X00 (868.3 MHz) | ALON00 (915 MHz) | | or equivalent pa | | |
| CER | SMD 3.45x3.1 | (313 10112) | SFECF10N B _{3dB} = 1 | И7НА00 | (913 10112) | | IF2=10.7MHz | ceramic filter | |
| FIL | SMD | | CFUKG45 | | | | | from Murata, | |
| | 6.5x6.0 | | $B_{6dB} = 2$ | | | | IF2=455kHz or equivalent part | | |
| | | 18.094444 | 24.701111 | 24.416667 | 25.713889 | | | | |
| | | MHz | MHz | MHz | MHz | | | | |
| | | HEX24- | HEX24- | HEX24- | HEX24- | | 152 10 70411- | | |
| | CMD | 18.094444MH Z-12-50-F- | 24.701111MHZ- | 24.416667MHZ | 25.713889MH Z-12-50-F- | | IF2=10.7MHz | crystal from Telcona, | |
| XTAL | SMD 5x3.2 | H20-T2075- | 12-50-F-H20- | -12-50-F-H20- | H20-T2075- | | | or equivalent part | |
| | 373.2 | W2-T | T2075-W2-T | T2075-W2-T | W2-T | | | | |
| | | 17.525278 MHz | 24.132 MH | | 25.429306 MHz | | IF2=455kHz | | |
| | | | \pm 20ppm cal., \pm | 30ppm temp. | | | | · | |
| l | | | | | | | 1 | | |

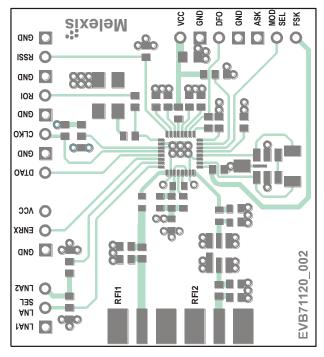
Note: NIP – not in place, may be used optionally

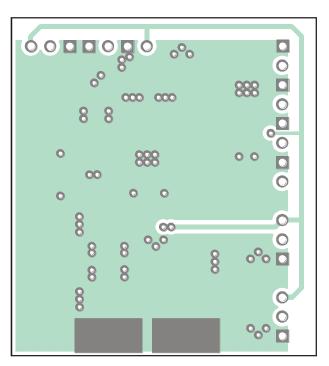




3.4. PCB Layouts for Antenna Space Diversity

Board layout data in Gerber format is available, board size is 40mm x 44.5mm.





PCB top view

PCB bottom view

4. Board Variants

| Туре | Freque | ncy/MHz | Board Execution | | |
|----------|--------|---------|-----------------|-------------------|--|
| EVB71120 | -315 | | -A | antenna version | |
| | -433 | | -C | connector version | |
| | -868 | | | | |
| | -915 | | | | |

Note:

available EVB setups



5. Package Description



The device MLX71120 is RoHS compliant.

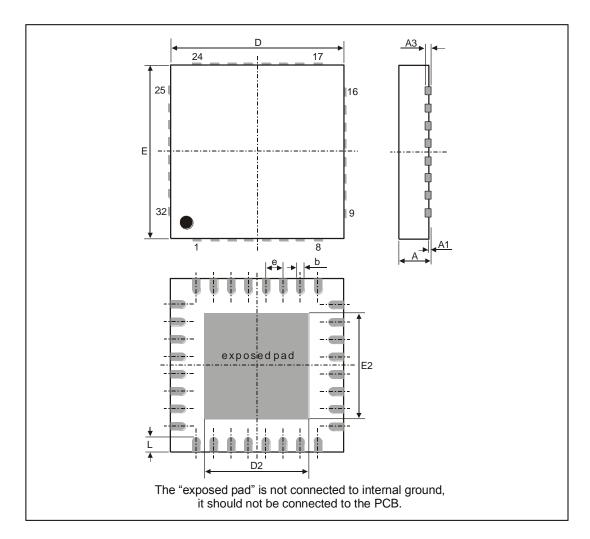


Fig. 8: 32L QFN 5x5 Quad

| all Dime | nsion in r | nm | | | | | | | | |
|----------|-----------------------|-------|-------|-------|--------|-------|--------|--------|--------|--------|
| | D | E | D2 | E2 | Α | A1 | A3 | L | е | b |
| min | 4.75 | 4.75 | 3.00 | 3.00 | 0.80 | 0 | 0.20 | 0.3 | 0.50 | 0.18 |
| max | 5.25 | 5.25 | 3.25 | 3.25 | 1.00 | 0.05 | 0.20 | 0.5 | 0.50 | 0.30 |
| all Dime | all Dimension in inch | | | | | | | | | |
| min | 0.187 | 0.187 | 0.118 | 0.118 | 0.0315 | 0 | 0.0070 | 0.0118 | 0.0197 | 0.0071 |
| max | 0.207 | 0.207 | 0.128 | 0.128 | 0.0393 | 0.002 | 0.0079 | 0.0197 | | 0.0118 |



5.1. Soldering Information

 The device MLX71120 is qualified for MSL3 with soldering peak temperature 260 deg C according to JEDEC J-STD-20

6. Reliability Information

This Melexis device is classified and qualified regarding soldering technology, solderability and moisture sensitivity level, as defined in this specification, according to following test methods:

Reflow Soldering SMD's (<u>Surface Mount Devices</u>)

- IPC/JEDEC J-STD-020
 "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices (classification reflow profiles
 according to table 5-2)"
- EIA/JEDEC JESD22-A113 "Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing (reflow profiles according to table 2)"

Wave Soldering SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EN60749-20 "Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat"
- EIA/JEDEC JESD22-B106 and EN60749-15 "Resistance to soldering temperature for through-hole mounted devices"

Iron Soldering THD's (Through Hole Devices)

EN60749-15
 "Resistance to soldering temperature for through-hole mounted devices"

Solderability SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

• EIA/JEDEC JESD22-B102 and EN60749-21 "Solderability"

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Melexis is contributing to global environmental conservation by promoting **lead free** solutions. For more information on qualification of **RoHS** compliant products (RoHS = European directive on the Restriction Of the Use of Certain Hazardous Substances) please visit the quality page on our website:

http://www.melexis.com/quality_leadfree.aspx_

7. ESD Precautions

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD). Always observe Electro Static Discharge control procedures whenever handling semiconductor products.



8. Contact

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For additional information, please contact our Direct Sales team and get help for your specific needs:

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