An Ultra-low Power, RDS$_{ON}$ 18 mΩ, 1 A, 0.82 mm^2 WLCSP Integrated Power Switch with 550 µs Total Turn-on Time

General Description

The SLG59M1742C is a high-performance 1 A capable, single-channel integrated power switch designed for high-side power control applications up to 1 A. This feature-rich nFET IPS has been optimized for all small form-factor, single-cell Li-ion applications including smartphone, fitness bands, and watches.

Operating from 2.7 V to 3.6 V supplies, the SLG59M1742C's RDS$_{ON}$ is a 18 mΩ and exhibits an input voltage range that extends from 0.25 V to 1.5 V. With a typical 550 µs total turn-on time (adjustable via metal mask from 300 µs to 1 ms), inrush currents at V$_{IN}$ are well behaved.

Using Dialog's proprietary MOSFET IP, the SLG59M1742C achieves a stable RDS$_{ON}$ as a function of both the supply and input voltages. Fully specified over the -40 °C to 85 °C temperature range, this advanced nFET IPS is available in 6-lead WLCSP measuring 0.71 mm x 1.16 mm x 0.5 mm with 0.35 mm pitch.

### Pin Configuration
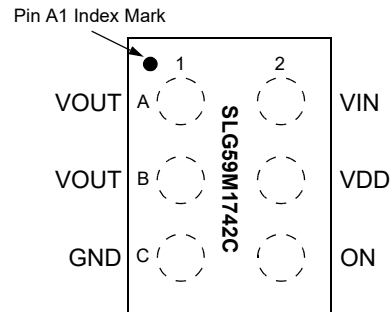
6L WLCSP
(Laser Marking View)

Features

- High-performance nFET Design:
  - Low Typical RDS$_{ON}$: 18 mΩ
- Steady-state Operating Current: 1 A
- Very Low Supply current after startup: < 1 µA
- Operating V$_{DD}$ Range: 2.7 V ≤ V$_{DD}$ ≤ 3.6 V
- Operating V$_{IN}$ Range: 0.25 V ≤ V$_{IN}$ ≤ 1.5 V
- Typical total turn on time: 550 µs
- Fast V$_{OUT}$ Discharge
- ON/OFF Control: Active HIGH
- Operating Temperature: -40 °C to 85 °C
- Pb-Free / Halogen-Free / RoHS compliant WLCSP
  - 6 lead 0.71 mm x 1.16 mm, 0.35 mm pitch

Applications

- Smartphones
- Fitness Bands
- Watches
- Tablet PCs

Block Diagram
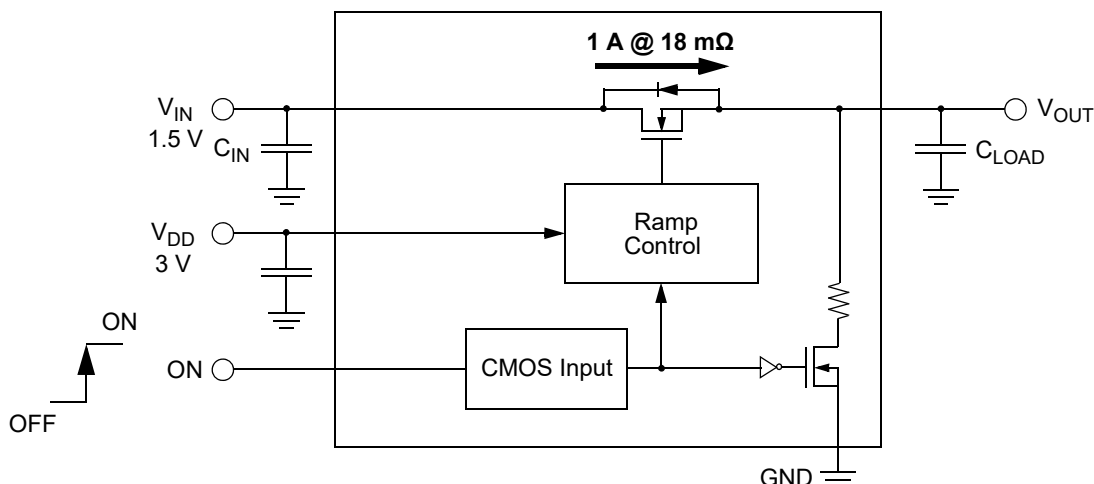
An Ultra-low Power, RDS$_{ON}$ 18 mΩ, 1 A, 0.82 mm^2 WLCSP
Integrated Power Switch with 550 µs Total Turn-on Time

Pin Description

Pin #	Pin Name	Type	Pin Description
B2	VDD	Power	VDD supplies the power for the operation of the power switch and the internal control circuitry. Bypass the VDD pin to GND with a 0.1 µF (or larger) capacitor.
A2	VIN	MOSFET	Drain terminal connection of the n-channel MOSFET. Connect a 1 µF (or larger) low-ESR capacitor from this pin to ground.
A1, B1	VOUT	MOSFET	Source terminal connections of the n-channel MOSFET. Connect a low-ESR capacitor from this pin to ground and consult the Electrical Characteristics table for recommended C$_{LOAD}$ range.
C2	ON	Input	A low-to-high transition on this pin initiates the operation of the SLG59M1742C's state machine. ON is an asserted HIGH, level-sensitive CMOS input with ON_V$_{IL}$ < 0.3 V and ON_V$_{IH}$ > 0.85 V. As the ON pin input circuit has an internal 8 MΩ pull-down, connect this pin to a general-purpose output (GPO) of a microcontroller, an application processor, or a system controller.
C1	GND	VOUT	Ground connection. Connect this pin to system analog or power ground plane.

Ordering Information

Part Number	Type	Production Flow
SLG59M1742C	WLCSP 6L	Industrial, -40 °C to 85 °C
SLG59M1742CTR	WLCSP 6L (Tape and Reel)	Industrial, -40 °C to 85 °C

An Ultra-low Power, RDS_{ON} 18 mΩ, 1 A, 0.82 mm^2 WLCSP
Integrated Power Switch with 550 µs Total Turn-on Time

Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD} to GND	Power Supply Voltage to GND		-0.3	--	5	V
V_{IN} to GND	Power Switch Input Voltage to GND		-0.3	--	5	V
V_{OUT} to GND	Power Switch Output Voltage to GND		-0.3	--	5	V
ON to GND	ON Pin Voltage to GND		-0.3	--	5	V
T_S	Storage Temperature		-65	--	150	°C
ESD_{HBM}	ESD Protection	Human Body Model	3000	--	--	V
ESD_{CDM}	ESD Protection	Charged Device Model	1300	--	--	V
MSL	Moisture Sensitivity Level			1		
θ_{JA}	Package Thermal Resistance, Junction-to-Ambient	0.71 x 1.16 mm 6L WLCSP; Determined using 0.25 in^2, 1 oz .copper pads under each VIN and VOUT terminal and FR4 pcb material.	--	88	--	°C/W
$T_{J,MAX}$	Maximum Junction Temperature		--	150	--	°C
MOSFET IDS_{PK} Peak Current from VIN to VOUT		Maximum pulsed switch current, pulse width < 1 ms, 1% duty cycle	--	--	1.5	A

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

2.7 V ≤ V_{DD} ≤ 3.6 V; 0.25 V ≤ V_{IN} ≤ 1.5 V; T_A = -40 °C to 85 °C, unless otherwise noted. Typical values are at T_A = 25°C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Voltage		2.7	--	3.6	V
V_{IN}	Power Switch Input Voltage		0.25	--	1.5	V
I_{DD_Q1}	V_{DD} Quiescent Supply Current during startup	V_{DD} = 2.7 V; ON = V_{DD}; No Load	--	61.5	82.5	µA
		V_{DD} = 2.7 V; ON = 1.8 V; No Load	--	61.5	82.5	µA
		V_{DD} = 3.0 V; ON = V_{DD}; No Load	--	61.7	83.6	µA
		V_{DD} = 3.0 V; ON = 1.8 V; No Load	--	61.7	83.6	µA
		V_{DD} = 3.3 V; ON = V_{DD}; No Load	--	61.8	84.2	µA
		V_{DD} = 3.3 V; ON = 1.8 V; No Load	--	61.8	84.2	µA
		V_{DD} = 3.6 V; ON = V_{DD}; No Load	--	61.8	84.2	µA
		V_{DD} = 3.6 V; ON = 1.8 V; No Load	--	61.8	84.2	µA
I_{DD_Q2}	V_{DD} Quiescent Supply Current after startup / Power FET fully turned on	2.7 V ≤ V_{DD} ≤ 3.6 V; ON = V_{DD} after startup; No Load	--	--	0.5	µA
I_{SHDN}	OFF Mode Supply Current	2.7 V ≤ V_{DD} ≤ 3.6 V; ON = LOW; No Load	--	--	0.33	µA
MOSFET IDS	Current from VIN to VOUT	Continuous	--	--	1	A

An Ultra-low Power, RDS$_{ON}$ 18 mΩ, 1 A, 0.82 mm^2 WLCSP
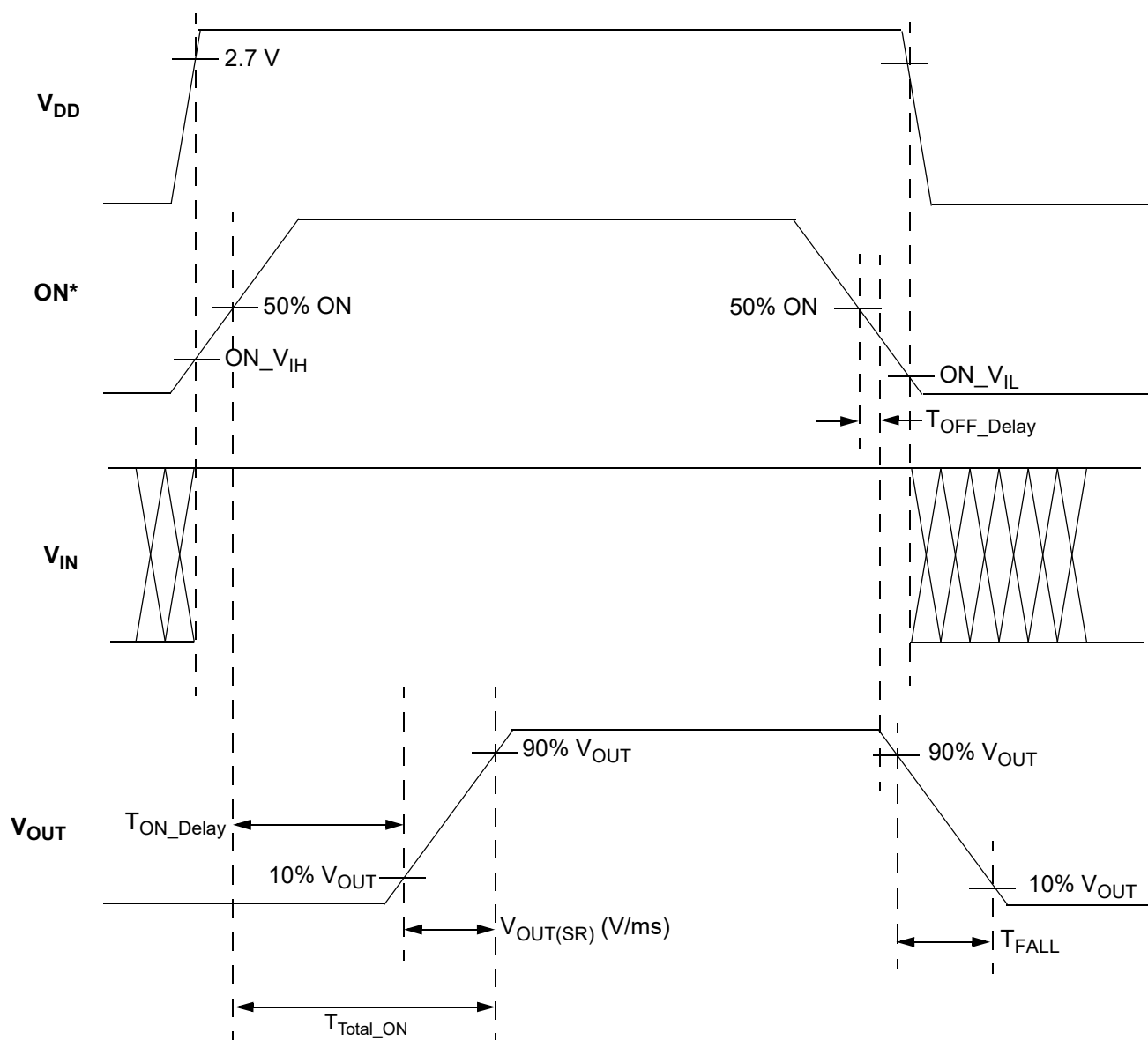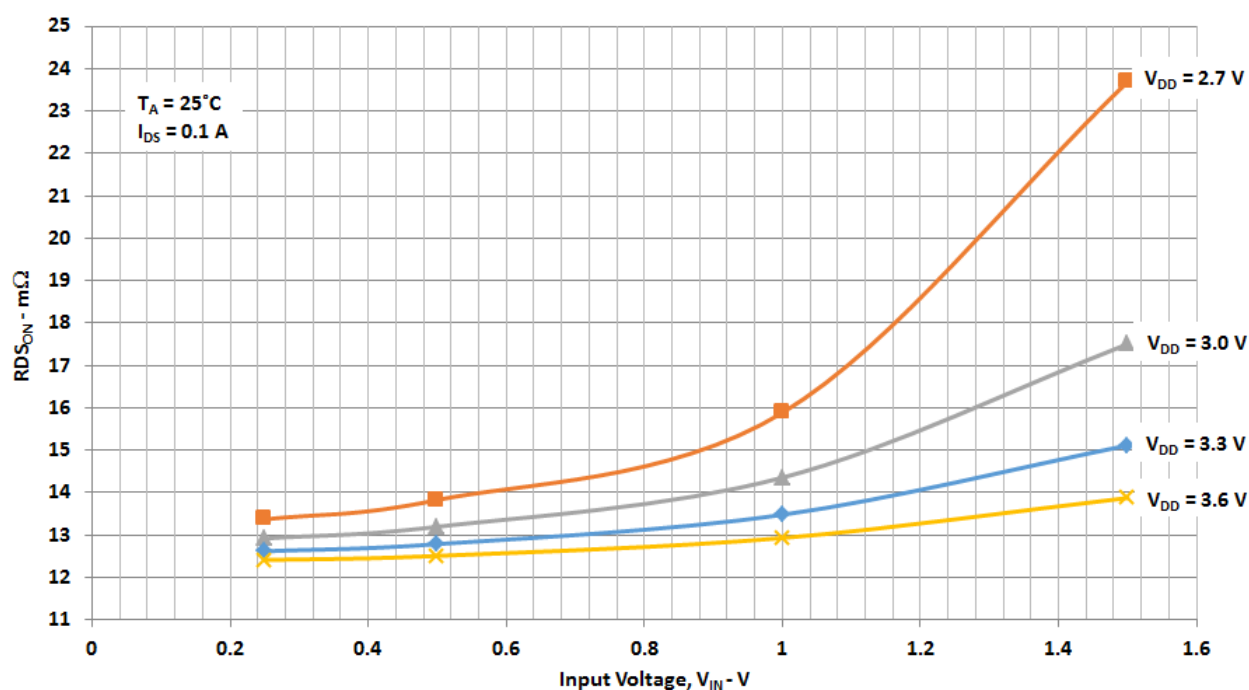Integrated Power Switch with 550 µs Total Turn-on Time

Electrical Characteristics (continued)

2.7 V ≤ V$_{DD}$ ≤ 3.6 V; 0.25 V ≤ V$_{IN}$ ≤ 1.5 V; T$_A$ = -40 °C to 85 °C, unless otherwise noted. Typical values are at T$_A$ = 25°C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
RDS$_{ON}$	ON Resistance	T$_A$ = 25°C; V$_{DD}$ = 3.0 V; V$_{IN}$ = 1.5 V; I$_{DS}$ = 0.1 A	--	18	20	mΩ
		T$_A$ = 85°C; V$_{DD}$ = 3.0 V; V$_{IN}$ = 1.5 V; I$_{DS}$ = 0.1 A	--	21	24	mΩ
I$_{FET\_OFF}$	MOSFET OFF Leakage Current	2.7 V ≤ V$_{DD}$ ≤ 3.6 V; V$_{IN}$ = 1.5 V, V$_{OUT}$ = 0 V; ON = LOW	--	0.01	1	µA
T$_{ON\_Delay}$	ON Delay Time	50% ON to 10% V$_{OUT}$ ↑; V$_{DD}$ = 2.7 V; V$_{IN}$ = 1.5 V; R$_{LOAD}$ = 1 kΩ; C$_{LOAD}$ = 10 µF	--	0.27	0.36	ms
		50% ON to 10% V$_{OUT}$ ↑; V$_{DD}$ = 3.6 V; V$_{IN}$ = 1.5 V; R$_{LOAD}$ = 1 kΩ; C$_{LOAD}$ = 10 µF	--	0.27	0.36	ms
V$_{OUT(SR)}$	Slew Rate	10% V$_{OUT}$ to 90% V$_{OUT}$ ↑; V$_{DD}$ = 2.7 V; V$_{IN}$ = 1.5 V; R$_{LOAD}$ = 1 kΩ; C$_{LOAD}$ = 10 µF	3.2	4.3	5.5	V/ms
		10% V$_{OUT}$ to 90% V$_{OUT}$ ↑; V$_{DD}$ = 3.6 V; V$_{IN}$ = 1.5 V; R$_{LOAD}$ = 1 kΩ; C$_{LOAD}$ = 10 µF	3.2	4.3	5.5	V/ms
T$_{Total\_ON}$	Total Turn On Time	50% ON to 90% V$_{OUT}$ ↑; V$_{DD}$ = 2.7 V; V$_{IN}$ = 1.5 V; R$_{LOAD}$ = 1 kΩ; C$_{LOAD}$ = 10 µF	0.45	0.55	0.65	ms
		50% ON to 90% V$_{OUT}$ ↑; V$_{DD}$ = 3.6 V; V$_{IN}$ = 1.5 V; R$_{LOAD}$ = 1 kΩ; C$_{LOAD}$ = 10 µF	0.45	0.55	0.65	ms
T$_{OFF\_Delay}$	OFF Delay Time	50% ON to V$_{OUT}$ Fall Start; V$_{DD}$ = 2.7 V; V$_{IN}$ = 1.5 V; R$_{LOAD}$ = 1 kΩ; no C$_{LOAD}$	--	2.8	5	µs
		50% ON to V$_{OUT}$ Fall Start; V$_{DD}$ = 3.6 V; V$_{IN}$ = 1.5 V; R$_{LOAD}$ = 1 kΩ; no C$_{LOAD}$	--	6.3	8	µs
C$_{LOAD}$	Output Load Capacitance	C$_{LOAD}$ connected from VOUT to GND	--	10	30	µF
R$_{DISCHRG}$	Output Discharge Resistance	2.7 V ≤ V$_{DD}$ ≤ 3.6 V; V$_{OUT}$ < 0.4 V	--	160	210	Ω
ON_V$_{IH}$	ON Pin Input High Voltage		0.85	--	V$_{DD}$	V
ON_V$_{IL}$	ON Pin Input Low Voltage		-0.3	0	0.3	V

An Ultra-low Power, RDS$_{ON}$ 18 mΩ, 1 A, 0.82 mm^2 WLCSP
Integrated Power Switch with 550 µs Total Turn-on Time

T$_{Total\_ON}$, T$_{ON\_Delay}$ and Slew Rate Measurement

*Rise and Fall Times of the ON Signal are 100 ns

An Ultra-low Power, RDS_{ON} 18 mΩ, 1 A, 0.82 mm^2 WLCSP
Integrated Power Switch with 550 µs Total Turn-on Time

Typical Performance Characteristics
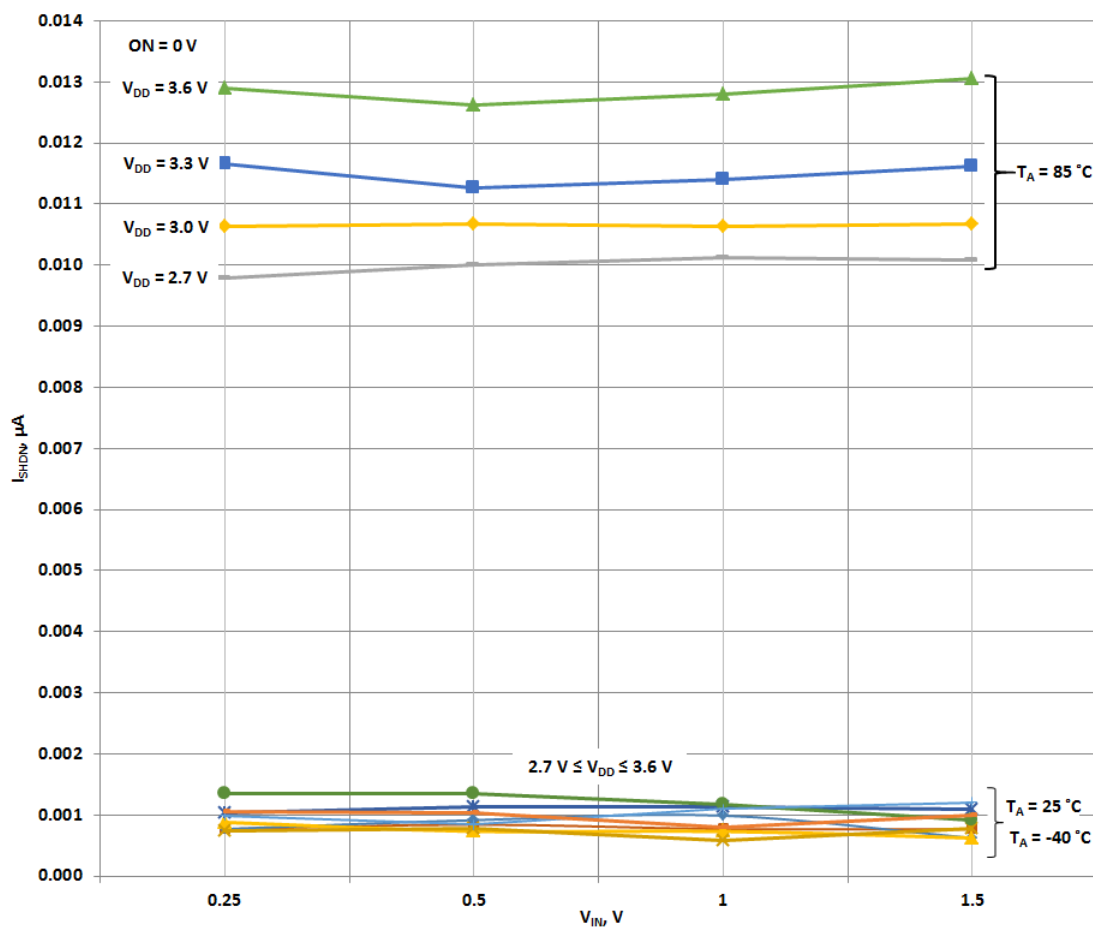
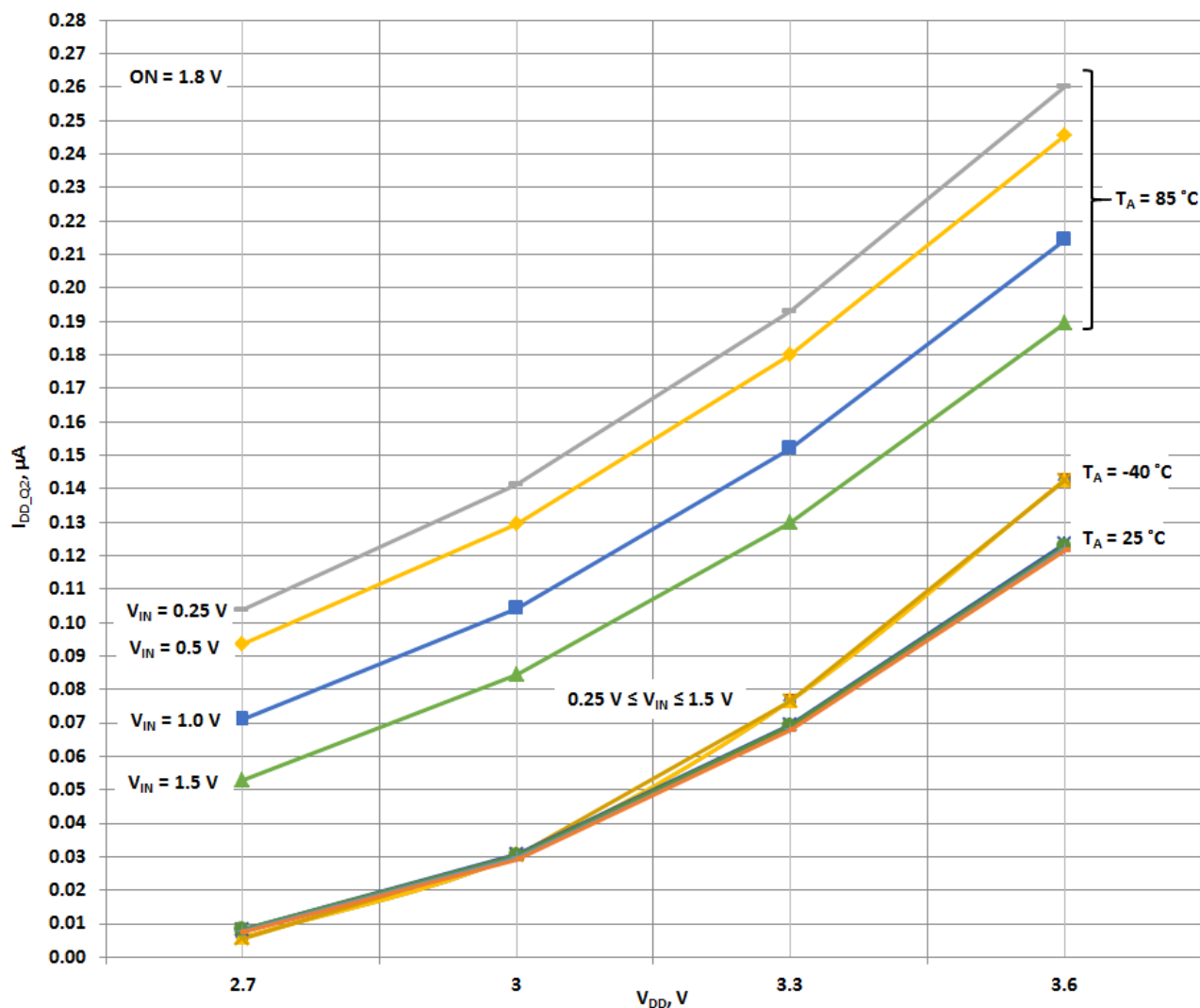### RDS_{ON} vs. Temperature, V_{IN}, and V_{DD}
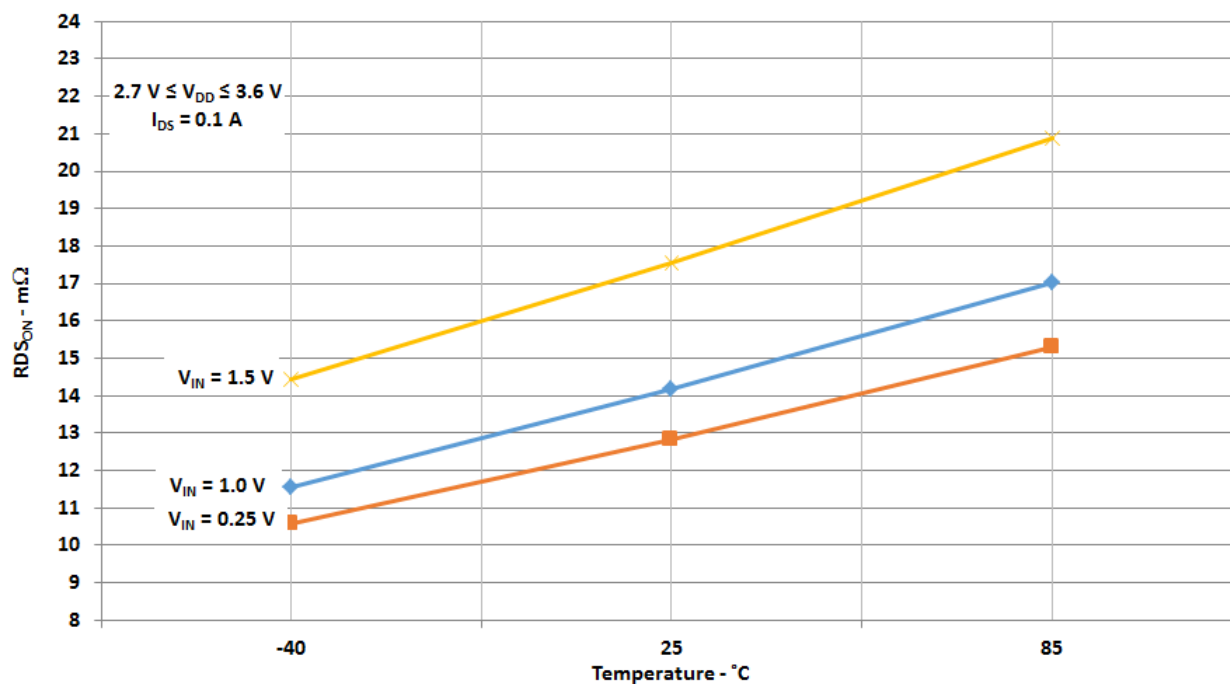
RDS_{ON} vs. V_{IN}, and V_{DD}

An Ultra-low Power, RDS$_{ON}$ 18 mΩ, 1 A, 0.82 mm^2 WLCSP
Integrated Power Switch with 550 µs Total Turn-on Time

I$_{SHDN}$ vs. V$_{IN}$, V$_{DD}$, and Temperature

An Ultra-low Power, RDS$_{ON}$ 18 mΩ, 1 A, 0.82 mm^2 WLCSP
Integrated Power Switch with 550 µs Total Turn-on Time

I_{DD_Q2} when ON = 1.8 V vs. V_{IN}, V_{DD}, and Temperature

An Ultra-low Power, RDS$_{ON}$ 18 mΩ, 1 A, 0.82 mm^2 WLCSP
Integrated Power Switch with 550 µs Total Turn-on Time

I$_{DD\_Q2}$ when ON = V$_{DD}$ vs. V$_{IN}$, V$_{DD}$, and Temperature
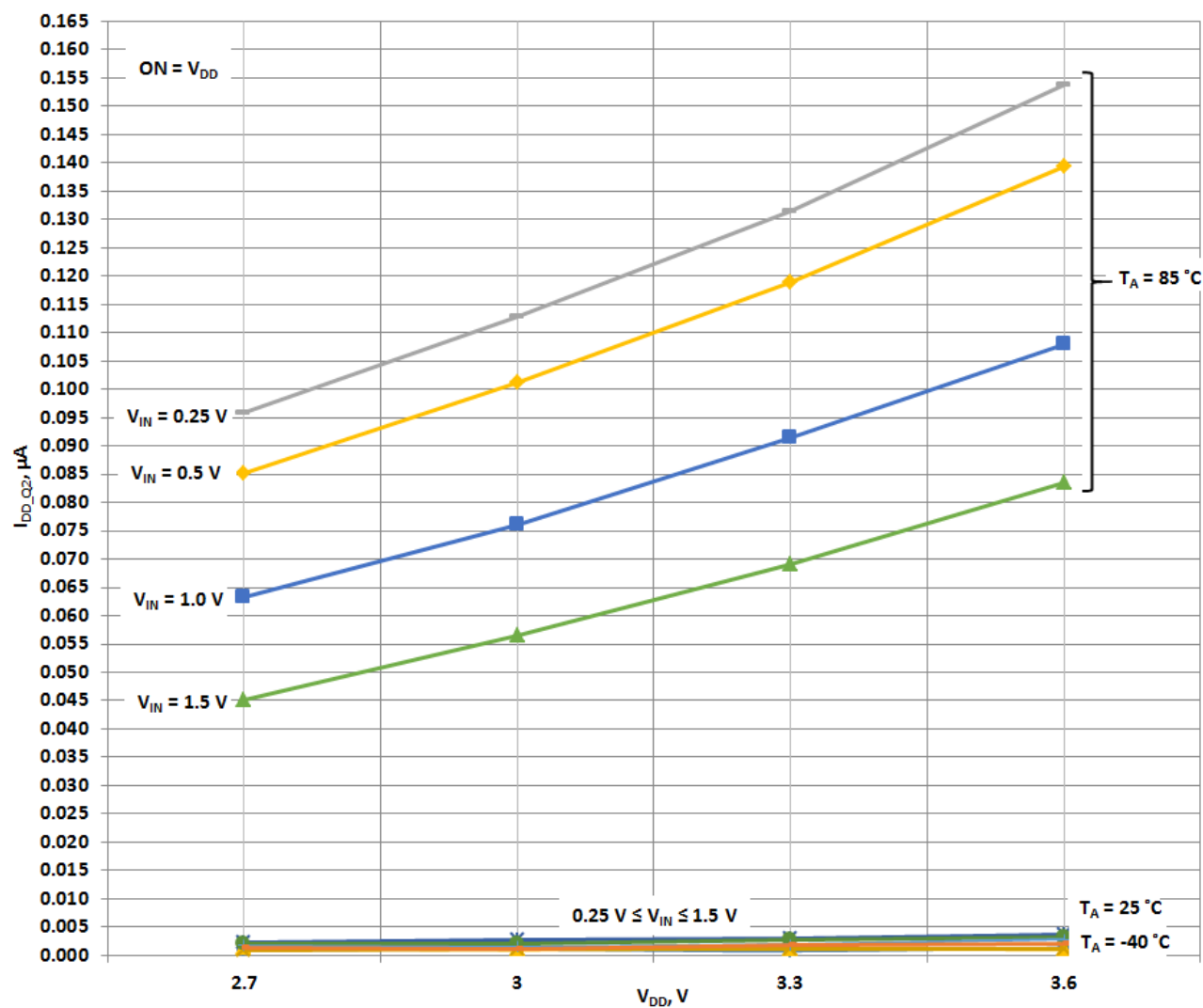
An Ultra-low Power, RDS$_{ON}$ 18 mΩ, 1 A, 0.82 mm^2 WLCSP
Integrated Power Switch with 550 μs Total Turn-on Time

Typical Turn-on Waveforms
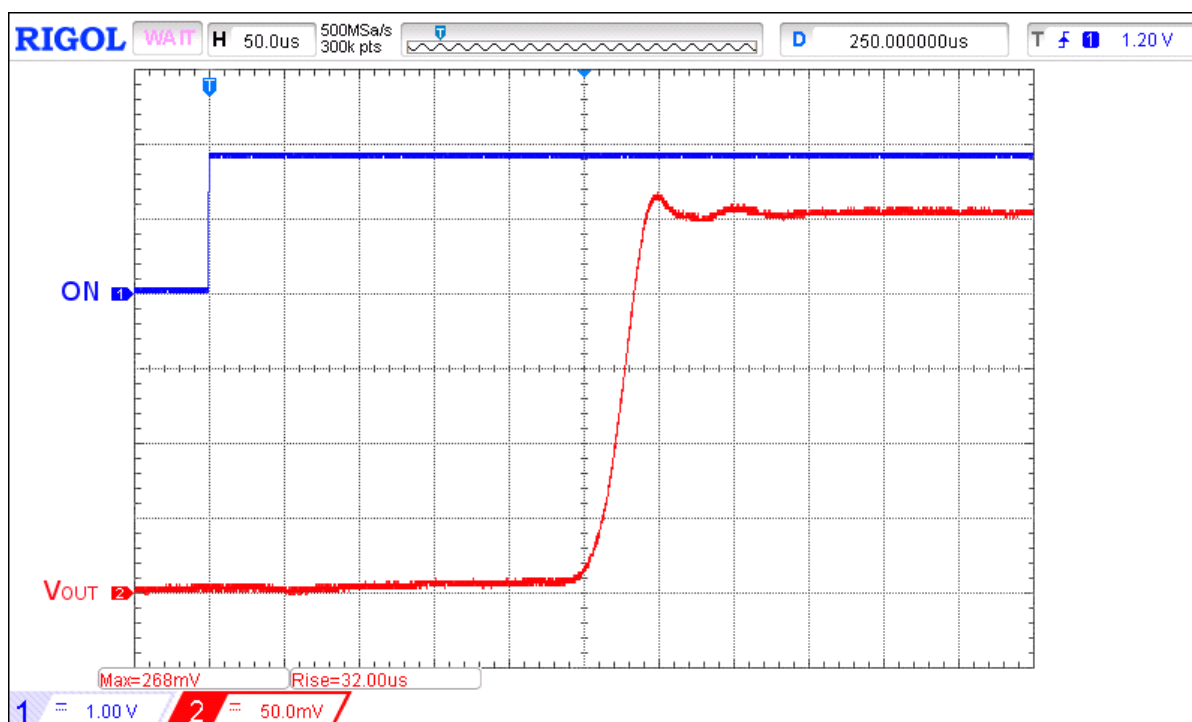
Figure 1. Typical Turn ON operation waveform for V$_{DD}$ = 2.7 V, V$_{IN}$ = 0.25 V, C$_{LOAD}$ = 10 μF, R$_{LOAD}$ = 1 kΩ
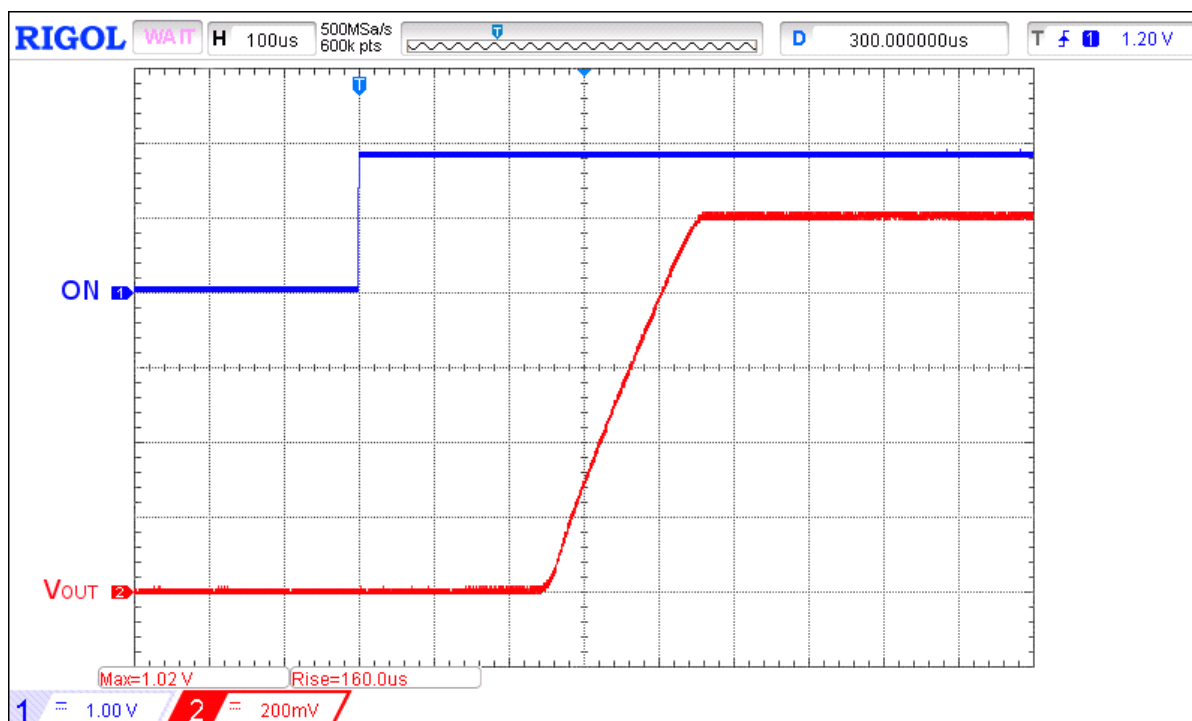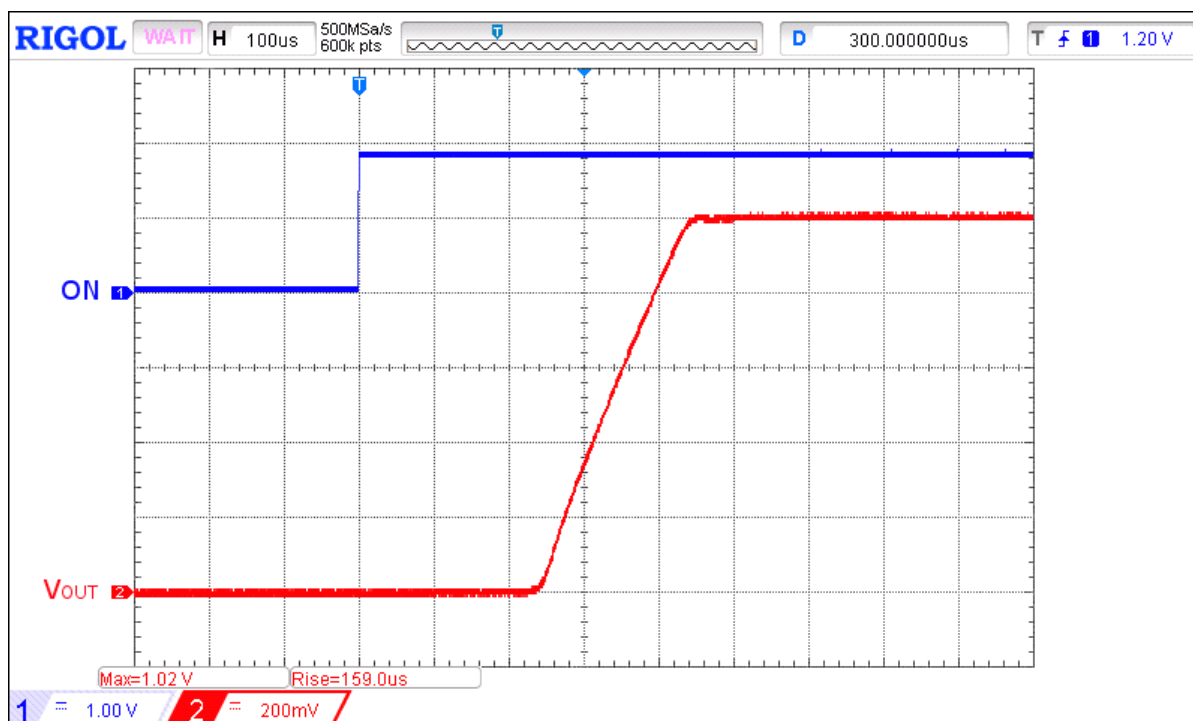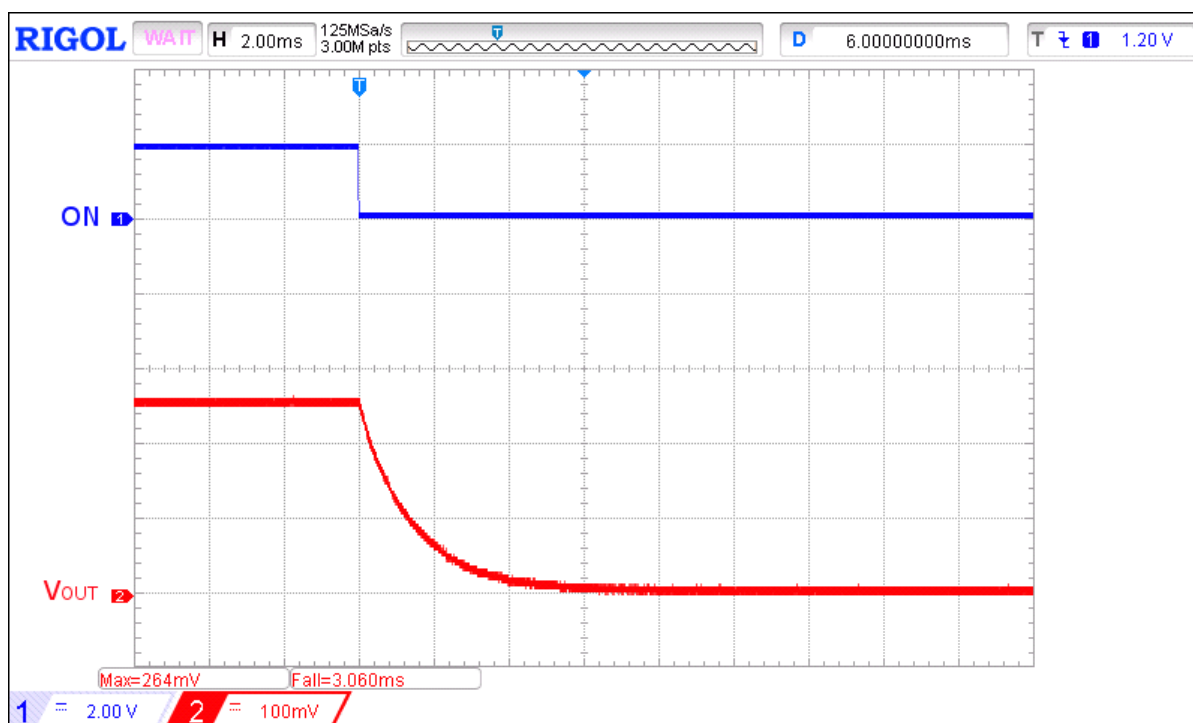

Figure 2. Typical Turn ON operation waveform for V$_{DD}$ = 2.7 V, V$_{IN}$ = 1 V, C$_{LOAD}$ = 10 μF, R$_{LOAD}$ = 1 kΩ

An Ultra-low Power, RDS$_{ON}$ 18 mΩ, 1 A, 0.82 mm^2 WLCSP
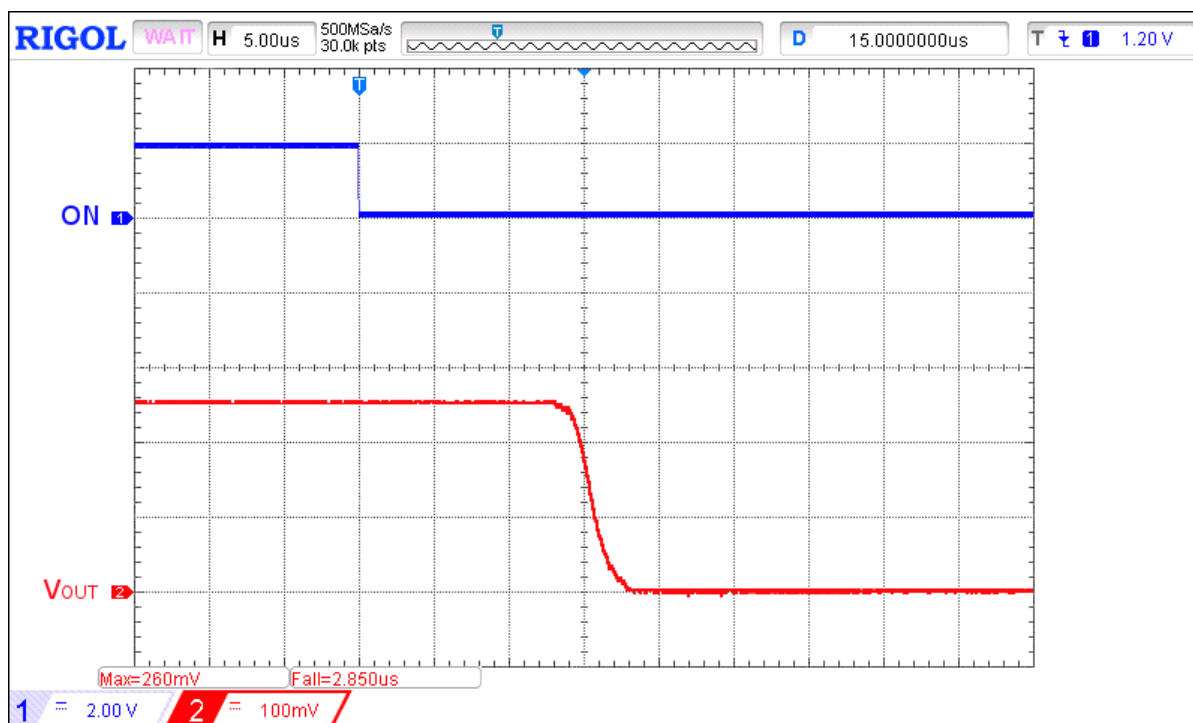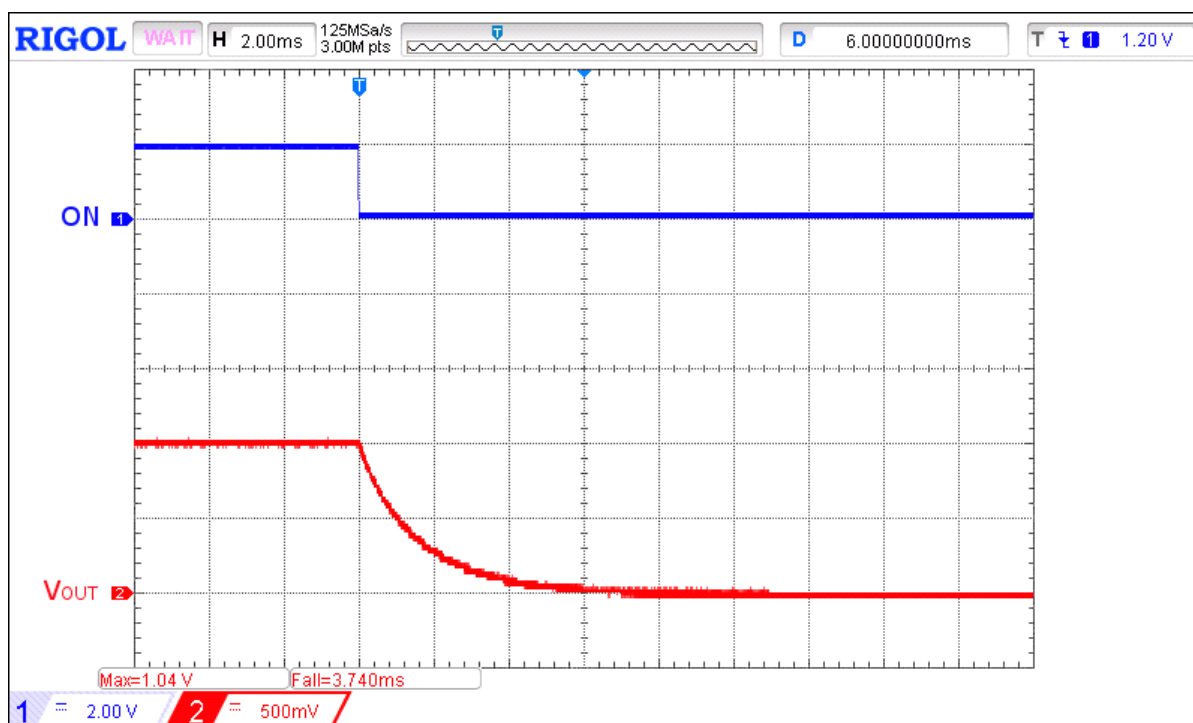Integrated Power Switch with 550 µs Total Turn-on Time
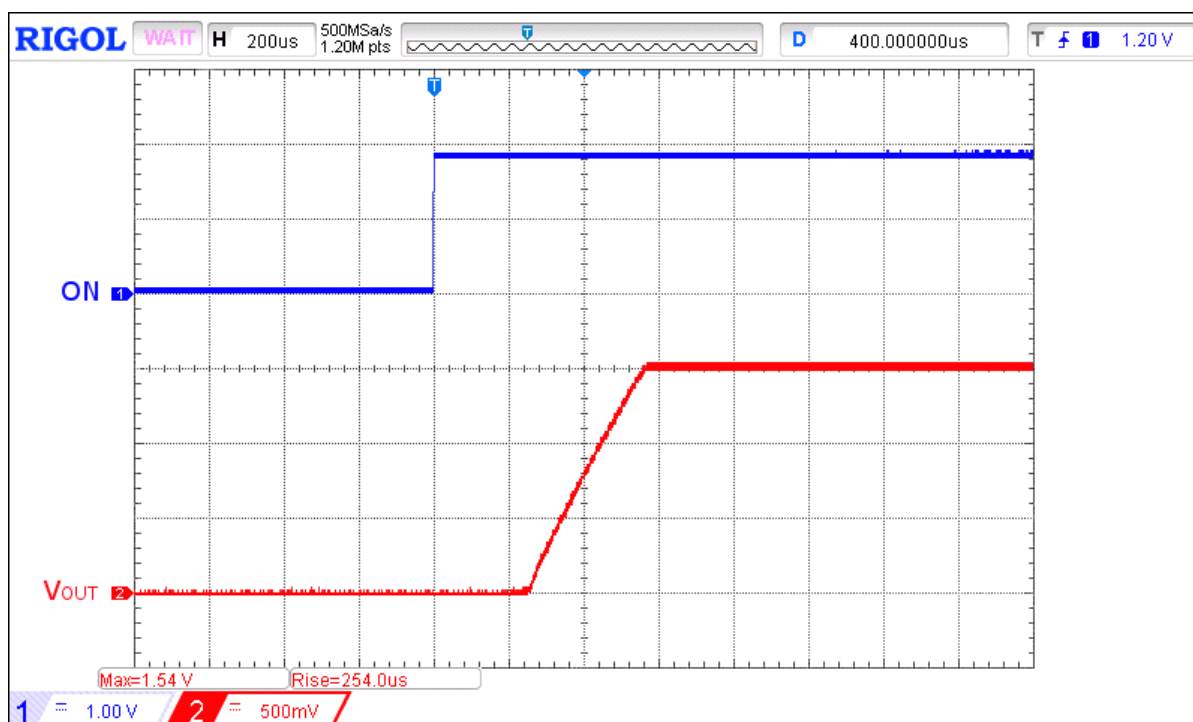
Figure 3. Typical Turn ON operation waveform for V$_{DD}$ = 2.7 V, V$_{IN}$ = 1.5 V, C$_{LOAD}$ = 10 µF, R$_{LOAD}$ = 1 kΩ
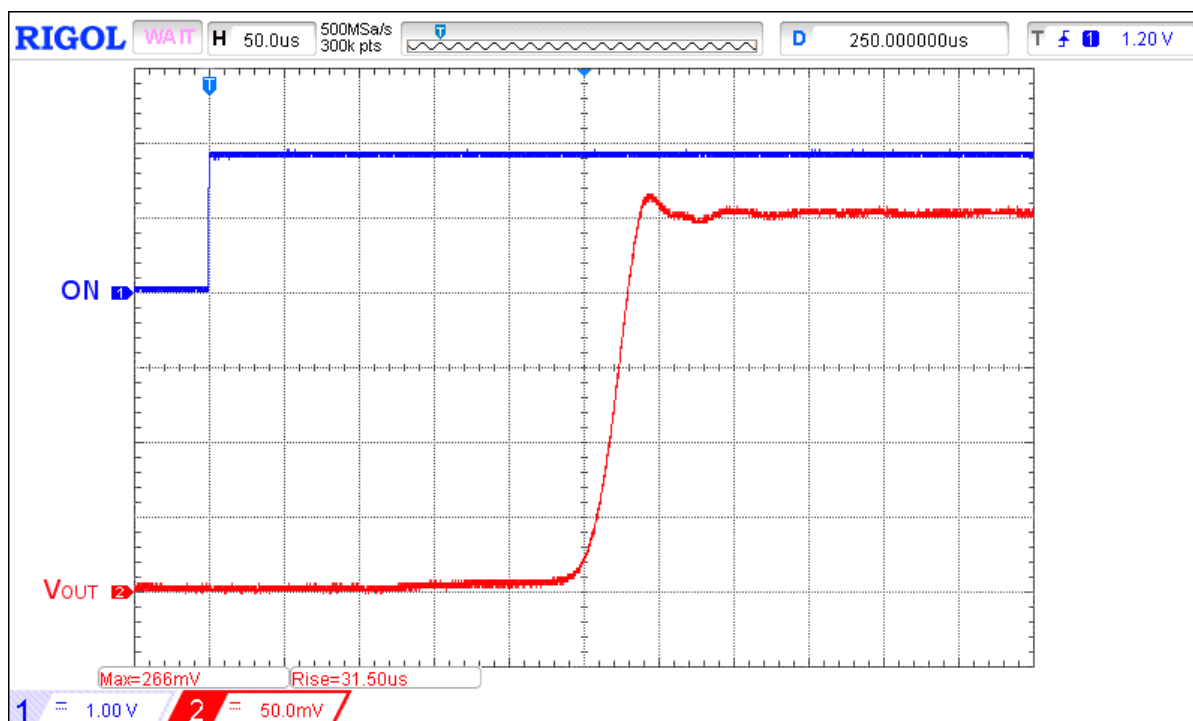
Figure 4. Typical Turn ON operation waveform for V$_{DD}$ = 3 V, V$_{IN}$ = 0.25 V, C$_{LOAD}$ = 10 µF, R$_{LOAD}$ = 1 kΩ
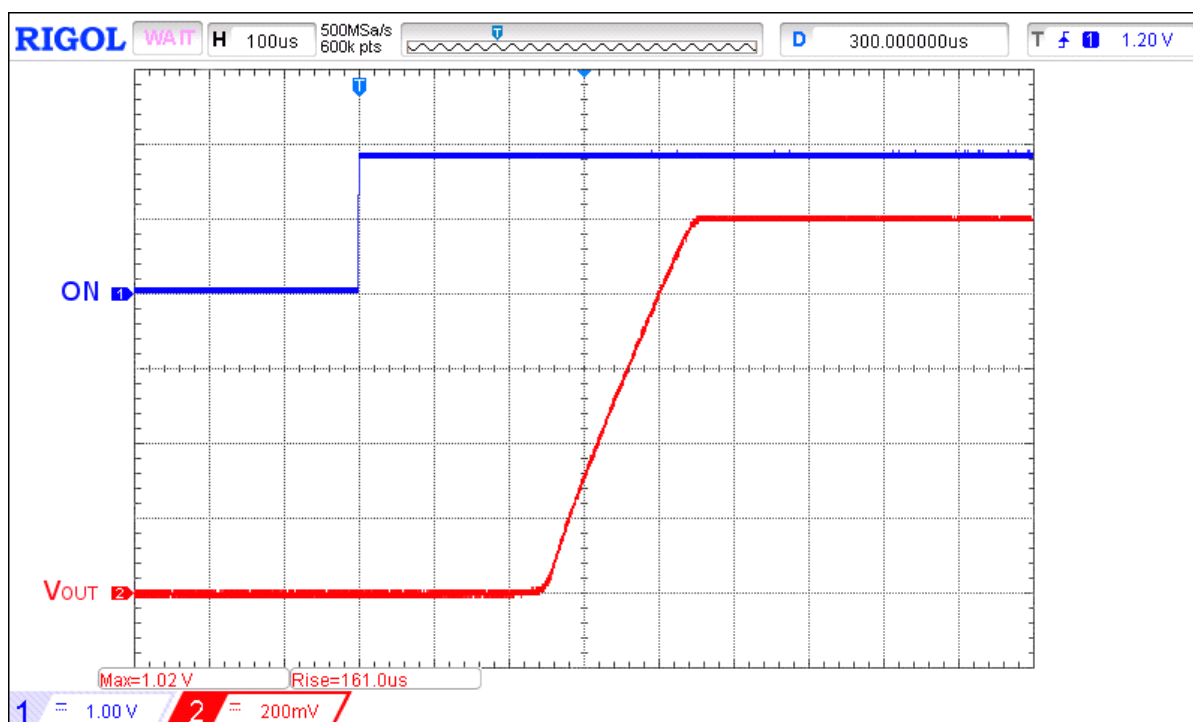
Figure 5. Typical Turn ON operation waveform for V$_{DD}$ = 3 V, V$_{IN}$ = 1 V, C$_{LOAD}$ = 10 µF, R$_{LOAD}$ = 1 kΩ
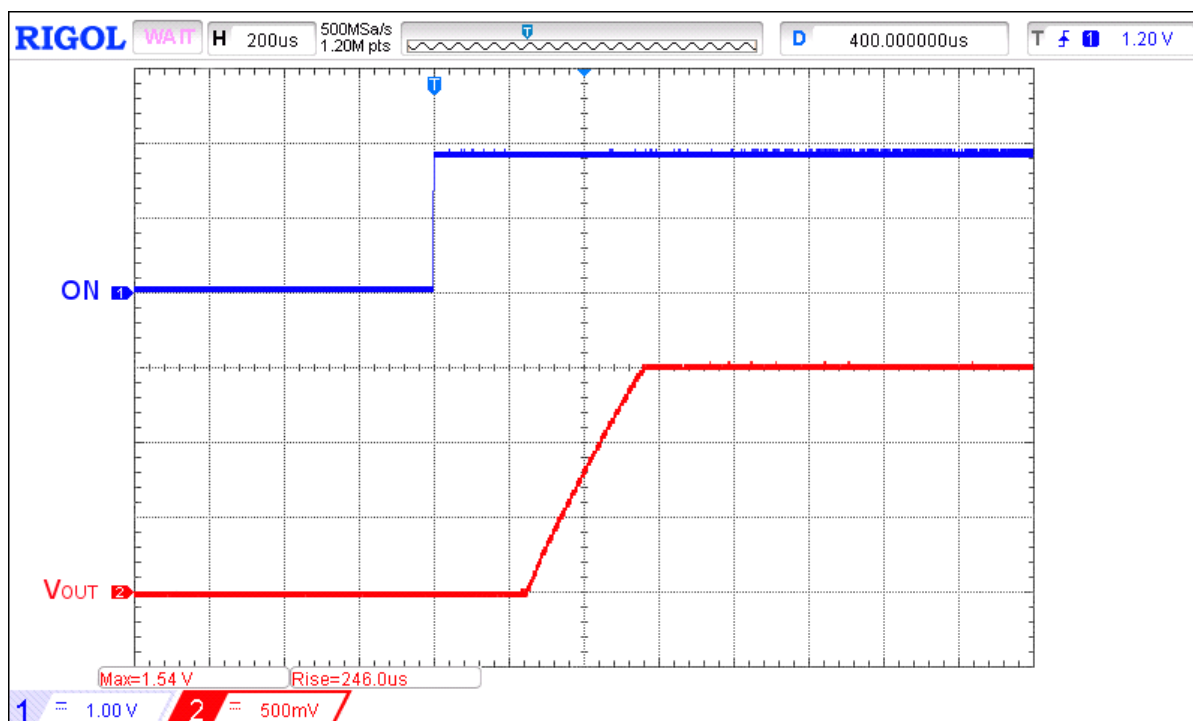
Figure 6. Typical Turn ON operation waveform for V$_{DD}$ = 3 V, V$_{IN}$ = 1.5 V, C$_{LOAD}$ = 10 µF, R$_{LOAD}$ = 1 kΩ
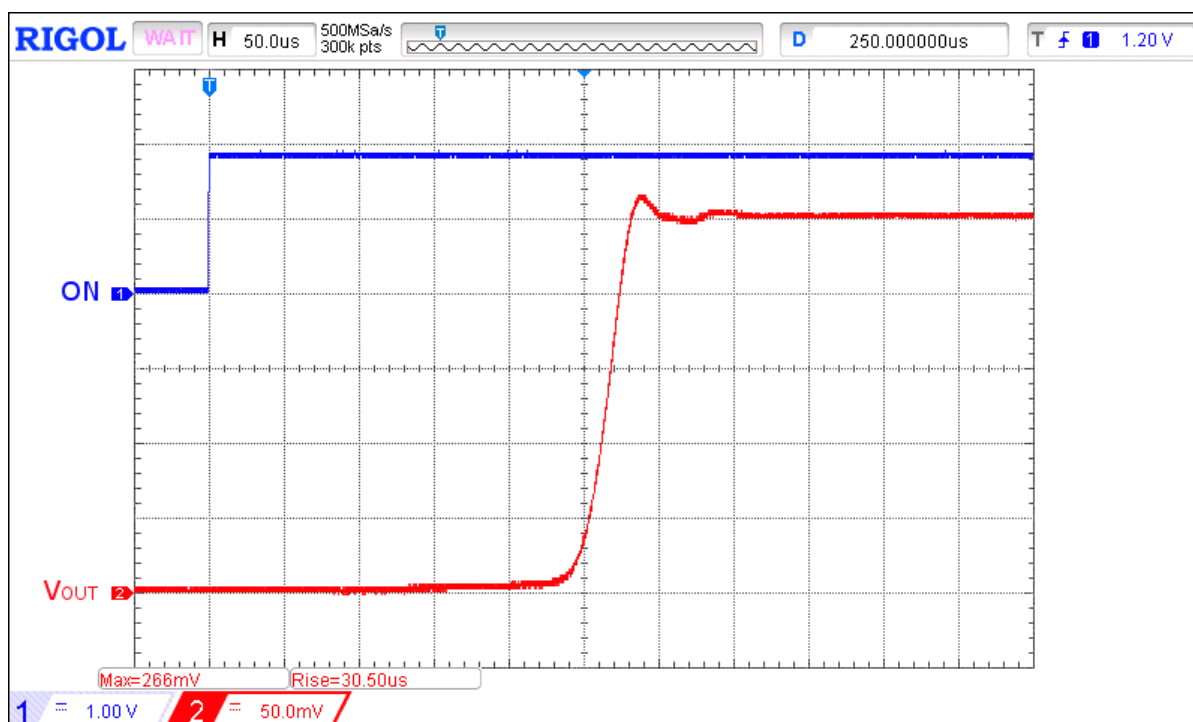
Figure 7. Typical Turn ON operation waveform for V$_{DD}$ = 3.6 V, V$_{IN}$ = 0.25 V, C$_{LOAD}$ = 10 μF, R$_{LOAD}$ = 1 kΩ

Figure 8. Typical Turn ON operation waveform for V$_{DD}$ = 3.6 V, V$_{IN}$ = 1 V, C$_{LOAD}$ = 10 μF, R$_{LOAD}$ = 1 kΩ

An Ultra-low Power, RDS$_{ON}$ 18 mΩ, 1 A, 0.82 mm^2 WLCSP
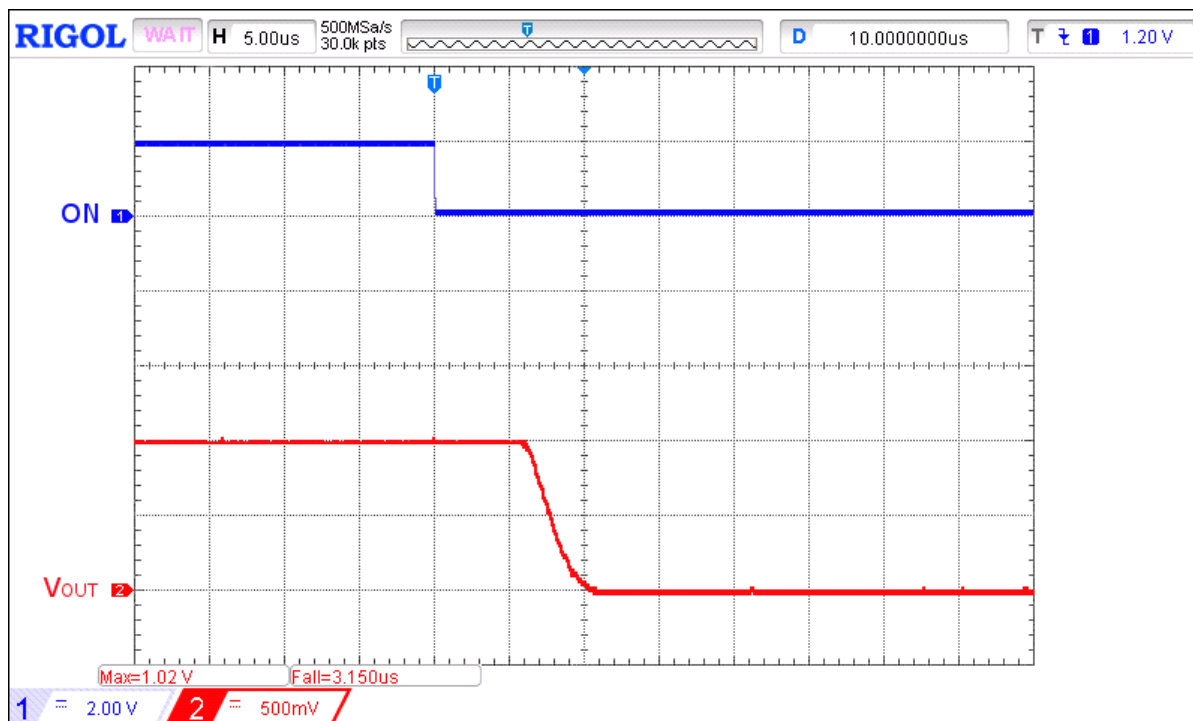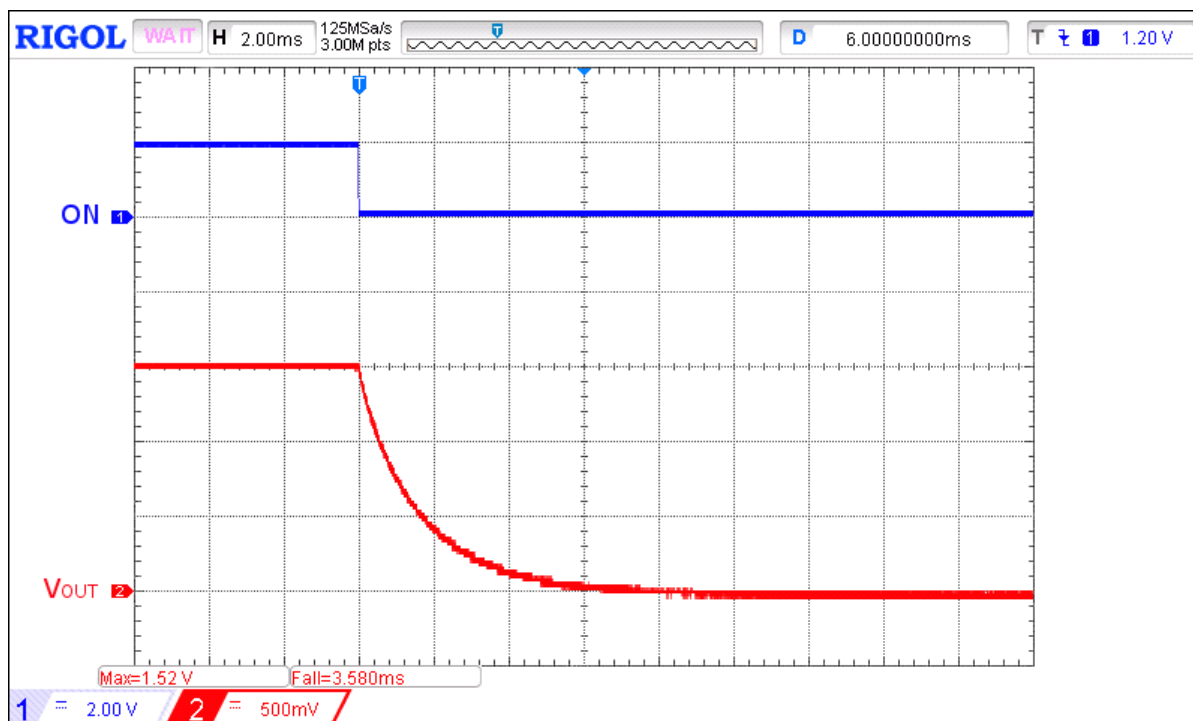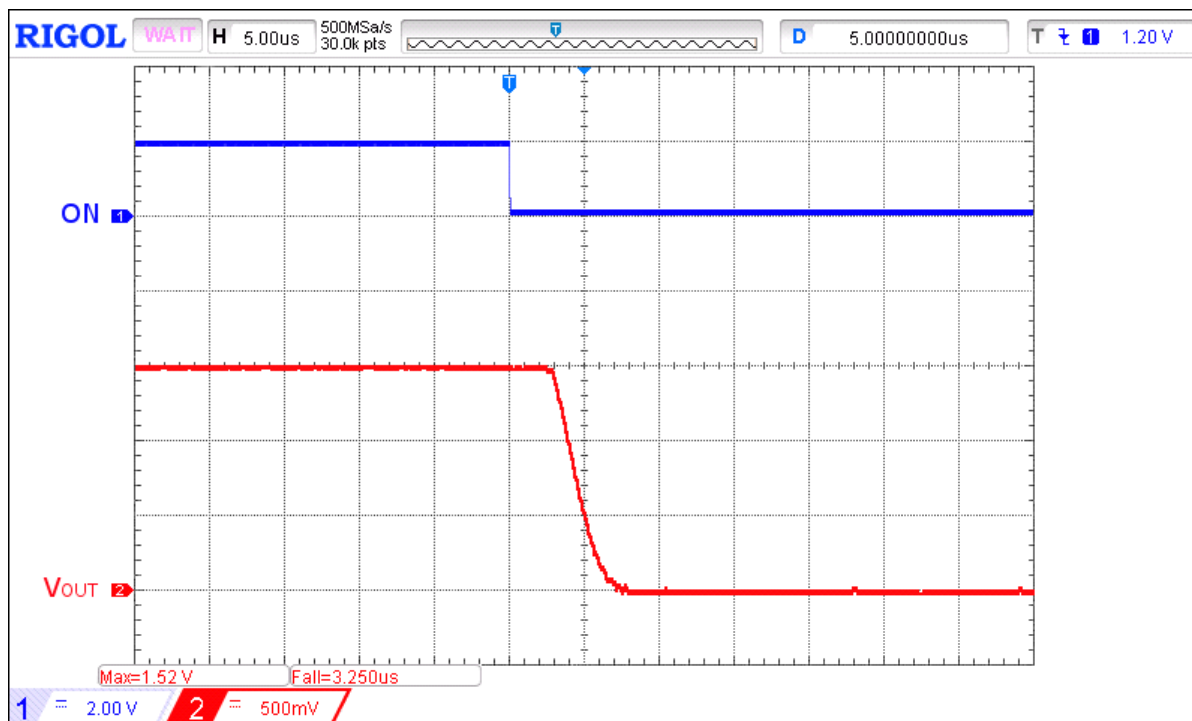Integrated Power Switch with 550 μs Total Turn-on Time
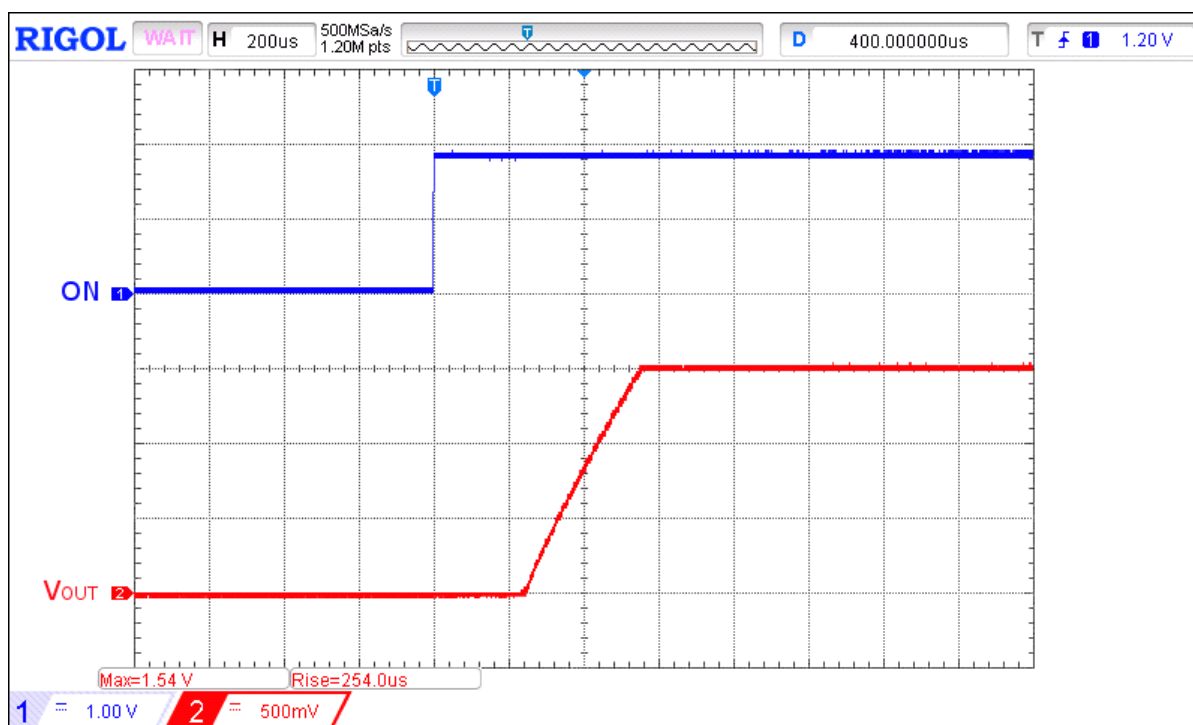
Figure 9. Typical Turn ON operation waveform for V$_{DD}$ = 3.6 V, V$_{IN}$ = 1.5 V, C$_{LOAD}$ = 10 μF, R$_{LOAD}$ = 1 kΩ

Typical Turn-off Waveforms

Figure 10. Typical Turn OFF operation waveform for V$_{DD}$ = 2.7 V, V$_{IN}$ = 0.25 V, C$_{LOAD}$ = 10 μF, R$_{LOAD}$ = 1 kΩ

Figure 11. Typical Turn OFF operation waveform for V$_{DD}$ = 2.7 V, V$_{IN}$ = 0.25 V, no C$_{LOAD}$, R$_{LOAD}$ = 1 kΩ

Figure 12. Typical Turn OFF operation waveform for V$_{DD}$ = 2.7 V, V$_{IN}$ = 1 V, C$_{LOAD}$ = 10 µF, R$_{LOAD}$ = 1 kΩ
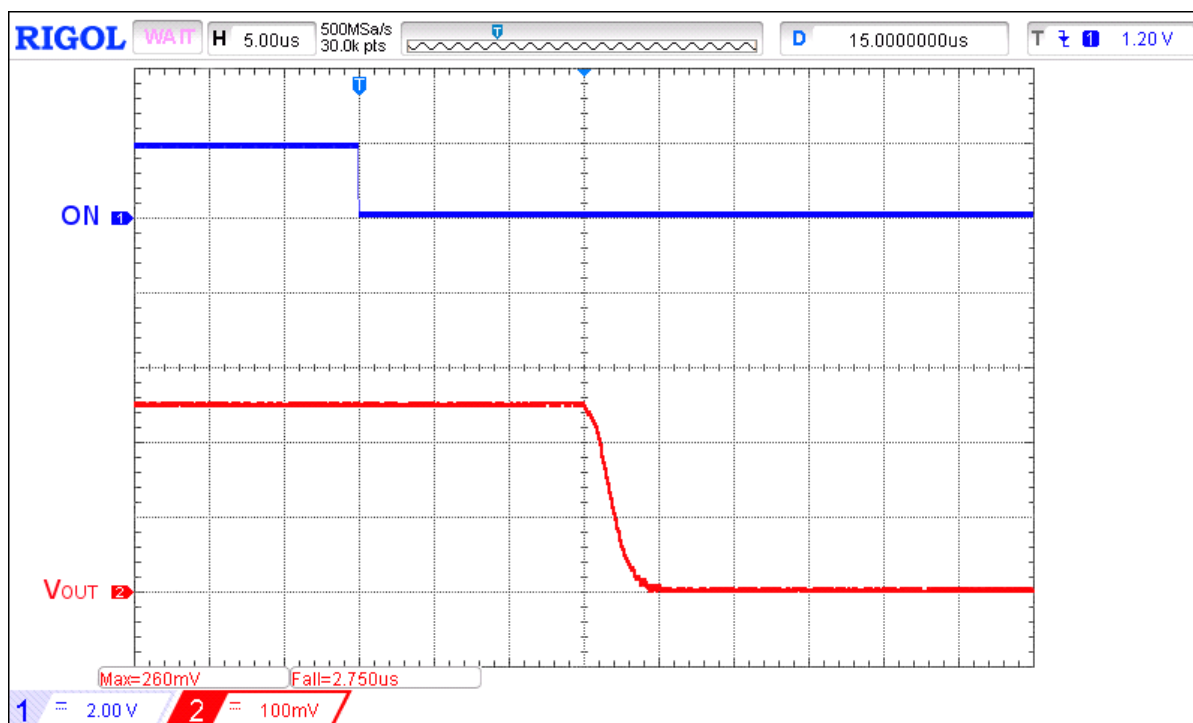
Figure 13. Typical Turn OFF operation waveform for V$_{DD}$ = 2.7 V, V$_{IN}$ = 1 V, no C$_{LOAD}$, R$_{LOAD}$ = 1 kΩ

Figure 14. Typical Turn OFF operation waveform for V$_{DD}$ = 2.7 V, V$_{IN}$ = 1.5 V, C$_{LOAD}$ = 10 µF, R$_{LOAD}$ = 1 kΩ

An Ultra-low Power, RDS$_{ON}$ 18 mΩ, 1 A, 0.82 mm^2 WLCSP
Integrated Power Switch with 550 µs Total Turn-on Time

Figure 15. Typical Turn OFF operation waveform for V$_{DD}$ = 2.7 V, V$_{IN}$ = 1.5 V, no C$_{LOAD}$, R$_{LOAD}$ = 1 kΩ
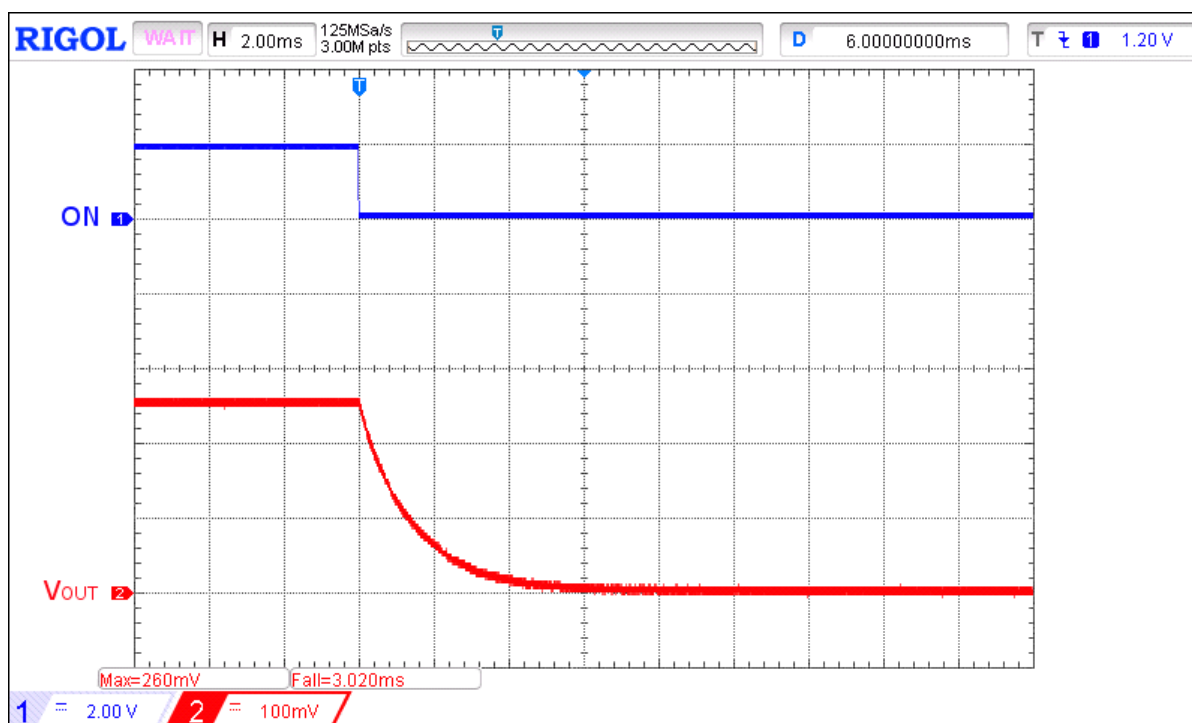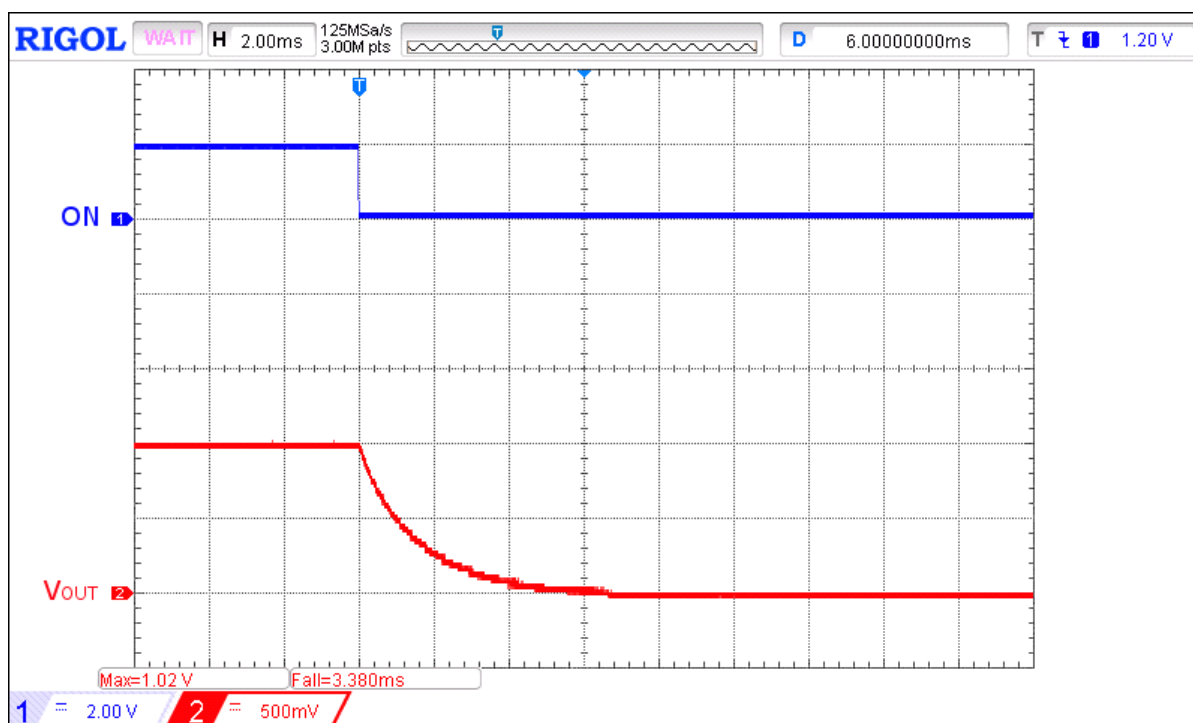

Figure 16. Typical Turn OFF operation waveform for V$_{DD}$ = 3 V, V$_{IN}$ = 0.25V, C$_{LOAD}$ = 10 µF, R$_{LOAD}$ = 1 kΩ

Figure 17. Typical Turn OFF operation waveform for V$_{DD}$ = 3 V, V$_{IN}$ = 0.25 V, no C$_{LOAD}$, R$_{LOAD}$ = 1 kΩ

Figure 18. Typical Turn OFF operation waveform for V$_{DD}$ = 3 V, V$_{IN}$ = 1 V, C$_{LOAD}$ = 10 µF, R$_{LOAD}$ = 1 kΩ
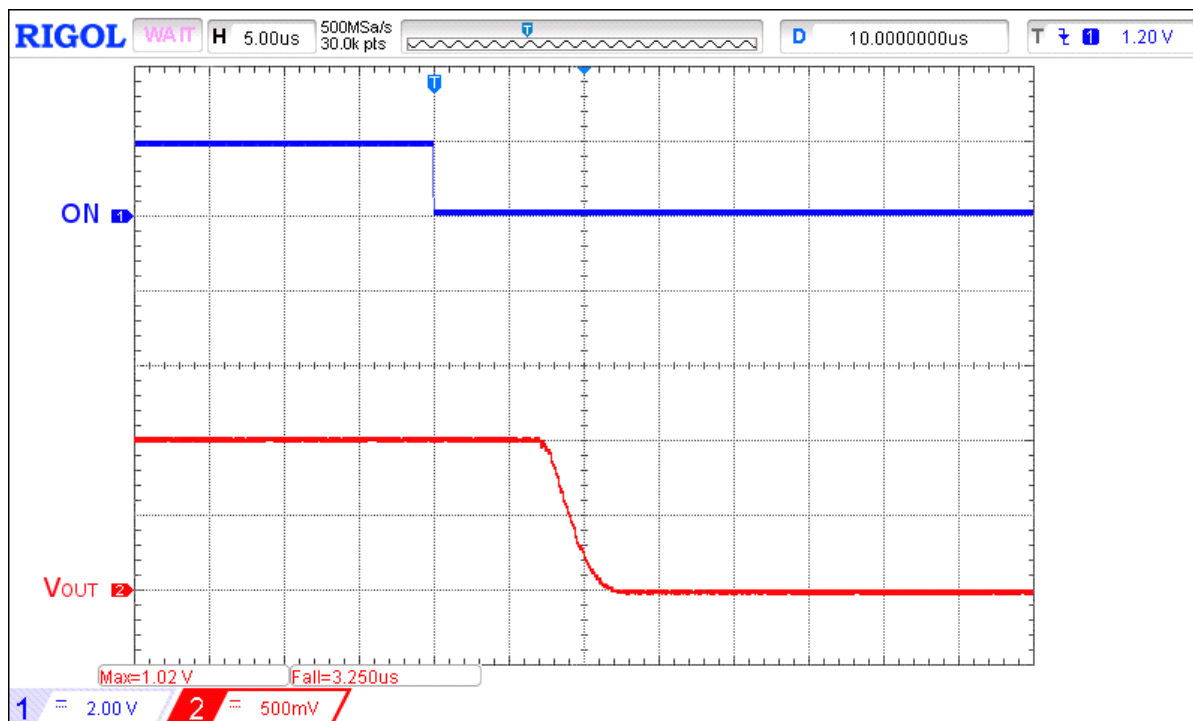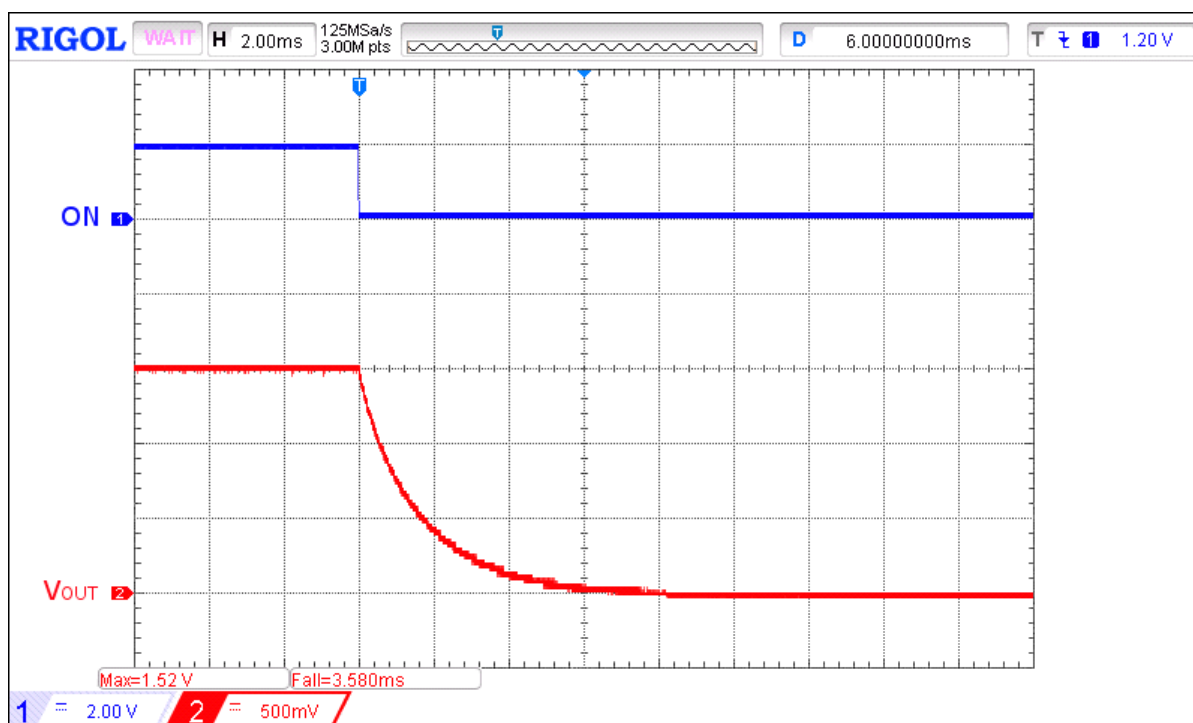
Figure 19. Typical Turn OFF operation waveform for V$_{DD}$ = 3 V, V$_{IN}$ = 1 V, no C$_{LOAD}$, R$_{LOAD}$ = 1 kΩ

Figure 20. Typical Turn OFF operation waveform for V$_{DD}$ = 3 V, V$_{IN}$ = 1.5 V, C$_{LOAD}$ = 10 μF, R$_{LOAD}$ = 1 kΩ
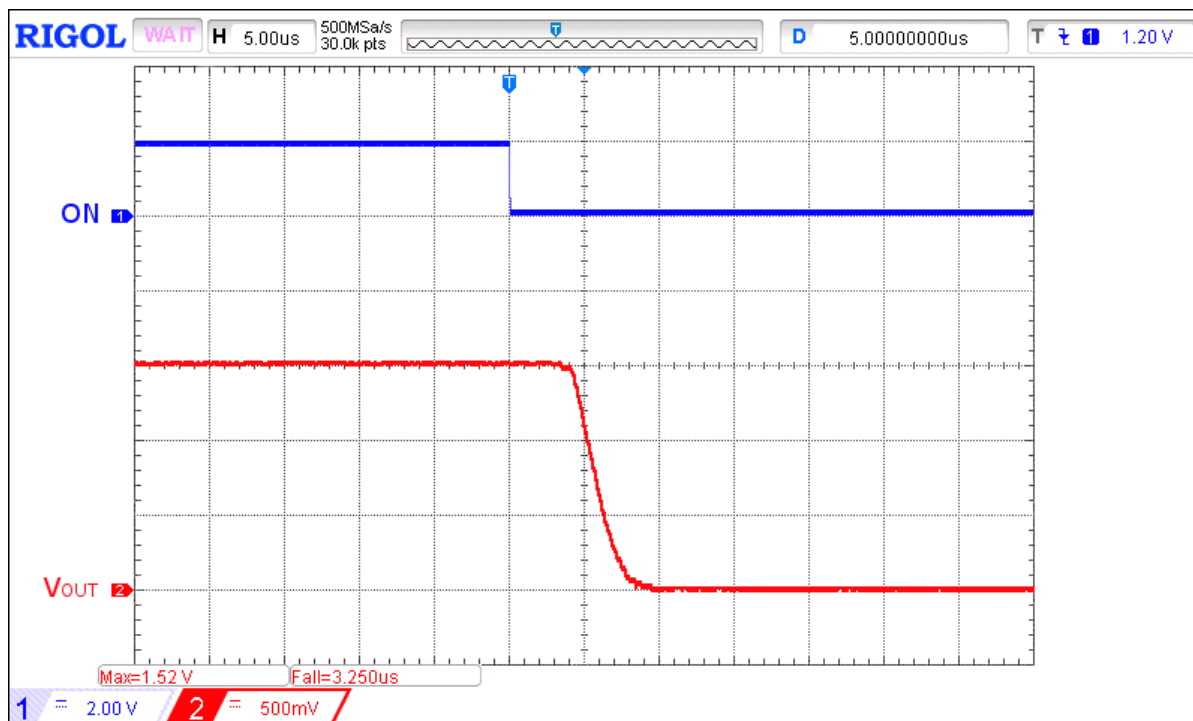
Figure 21. Typical Turn OFF operation waveform for V$_{DD}$ = 3 V, V$_{IN}$ = 1.5 V, no C$_{LOAD}$, R$_{LOAD}$ = 1 kΩ
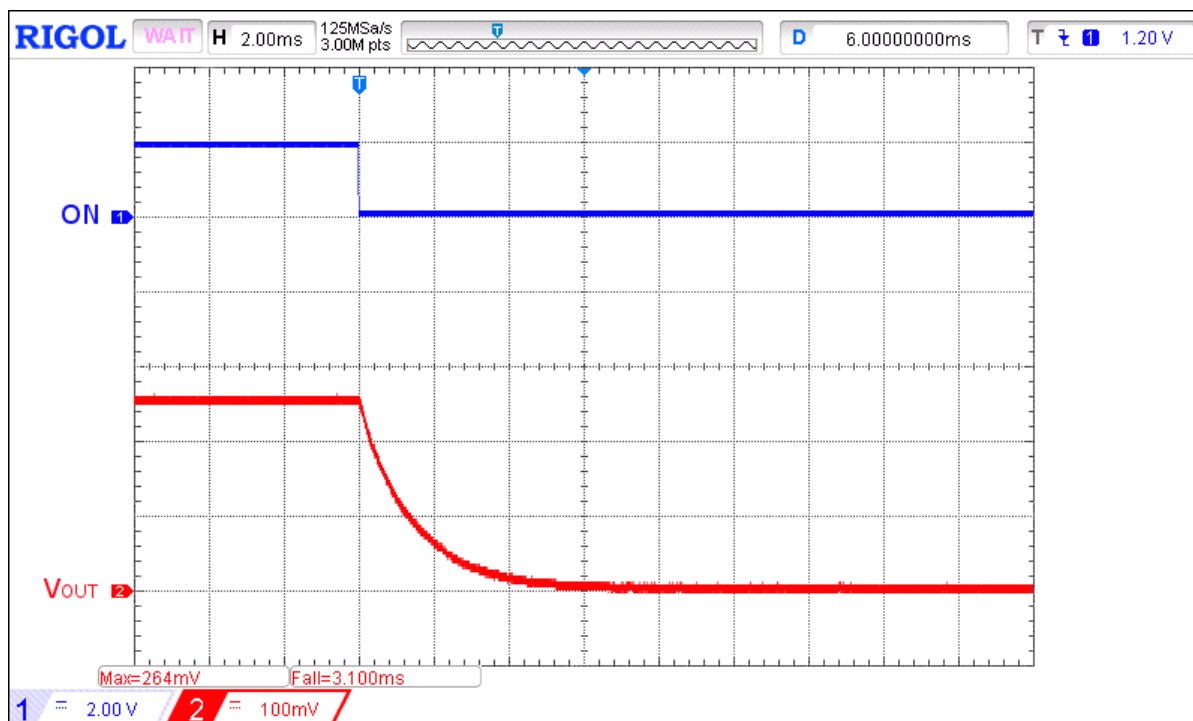
Figure 22. Typical Turn OFF operation waveform for V$_{DD}$ = 3.6 V, V$_{IN}$ = 0.25 V, C$_{LOAD}$ = 10 µF, R$_{LOAD}$ = 1 kΩ

Figure 23. Typical Turn OFF operation waveform for V$_{DD}$ = 3.6 V, V$_{IN}$ = 0.25 V, no C$_{LOAD}$, R$_{LOAD}$ = 1 kΩ
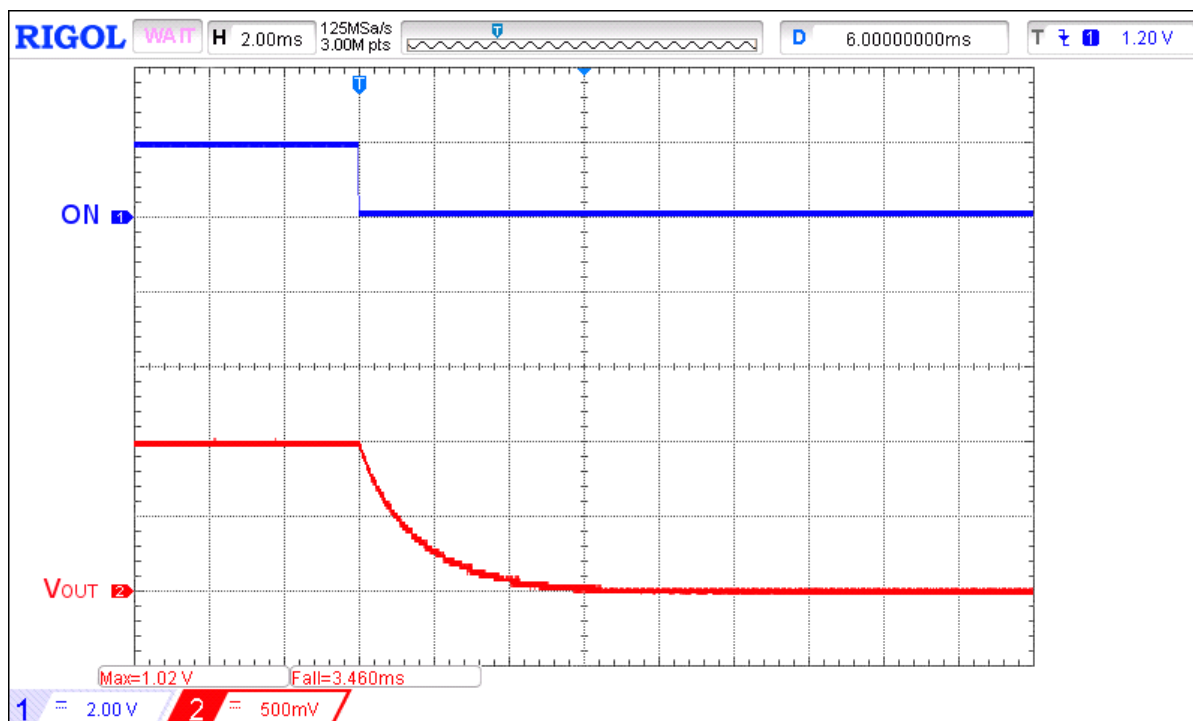
Figure 24. Typical Turn OFF operation waveform for V$_{DD}$ = 3.6 V, V$_{IN}$ = 1 V, C$_{LOAD}$ = 10 μF, R$_{LOAD}$ = 1 kΩ
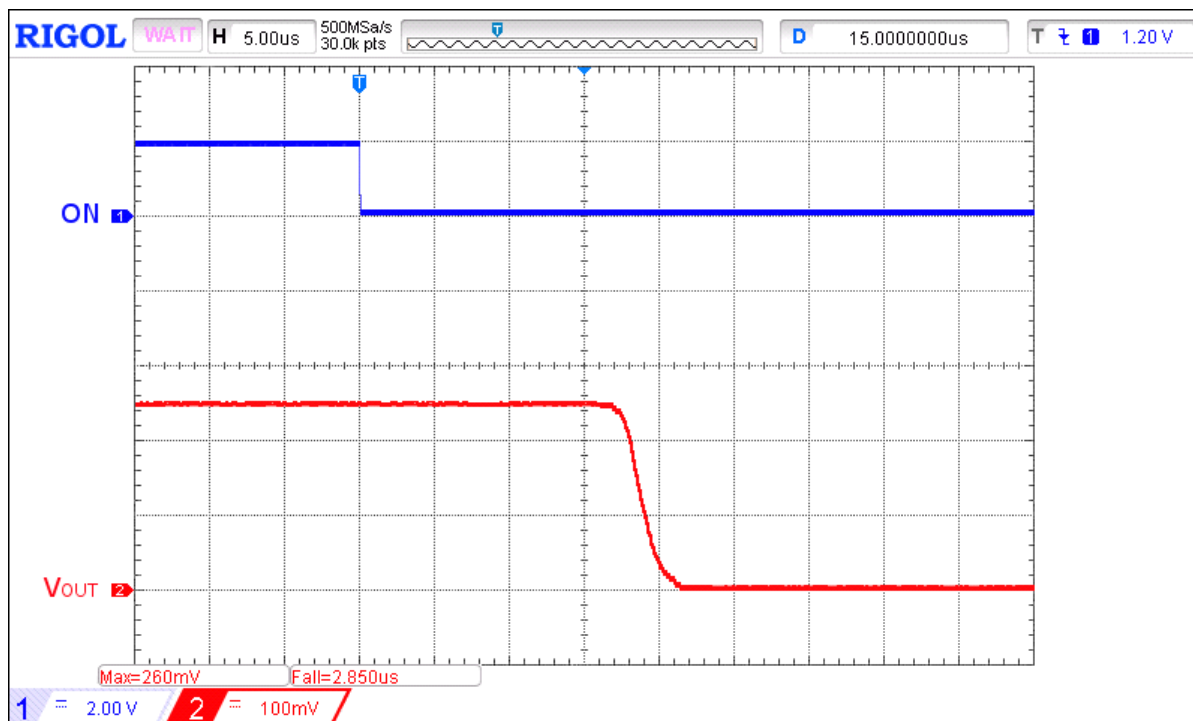
Figure 25. Typical Turn OFF operation waveform for V$_{DD}$ = 3.6 V, V$_{IN}$ = 1 V, no C$_{LOAD}$, R$_{LOAD}$ = 1 kΩ
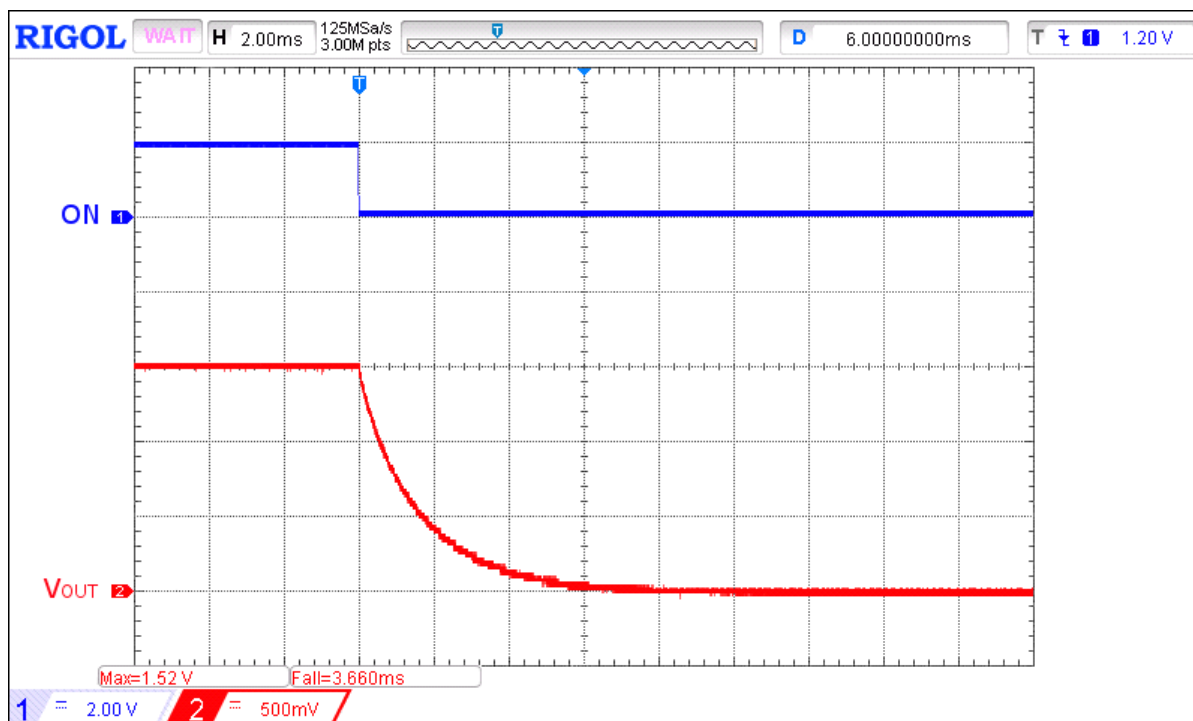
Figure 26. Typical Turn OFF operation waveform for V$_{DD}$ = 3.6 V, V$_{IN}$ = 1.5 V, C$_{LOAD}$ = 10 µF, R$_{LOAD}$ = 1 kΩ

An Ultra-low Power, RDS$_{ON}$ 18 mΩ, 1 A, 0.82 mm^2 WLCSP
Integrated Power Switch with 550 µs Total Turn-on Time

Figure 27. Typical Turn OFF operation waveform for V$_{DD}$ = 3.6 V, V$_{IN}$ = 1.5 V, no C$_{LOAD}$, R$_{LOAD}$ = 1 kΩ
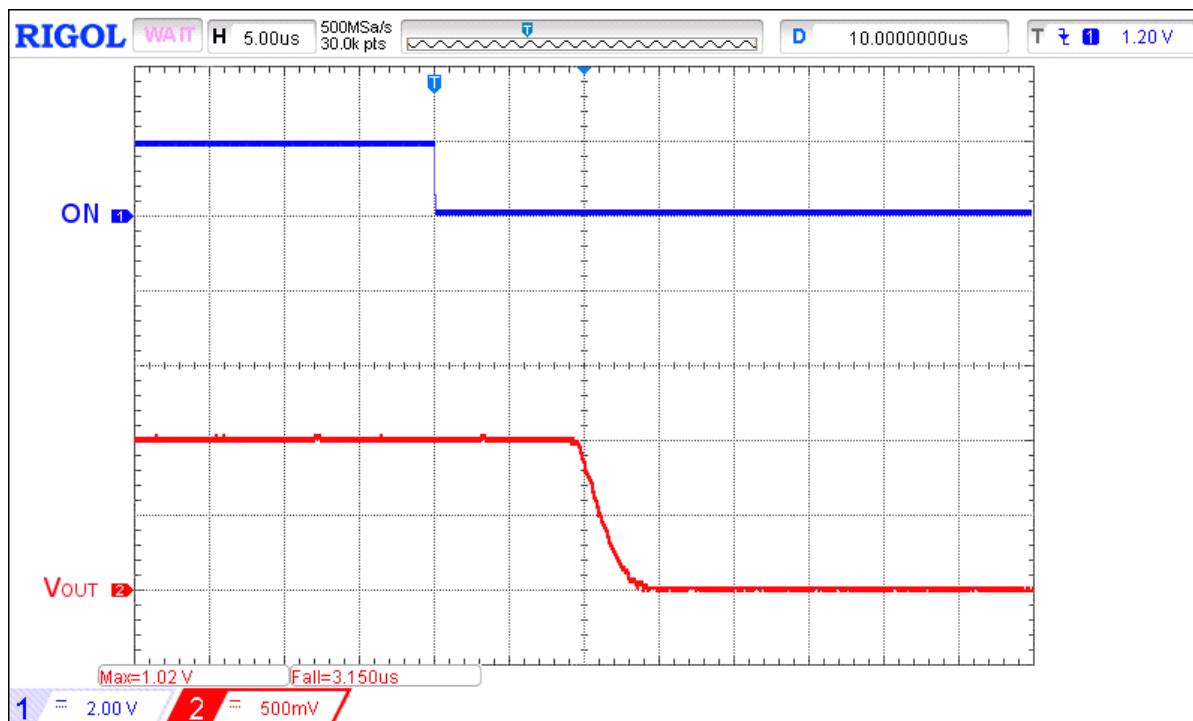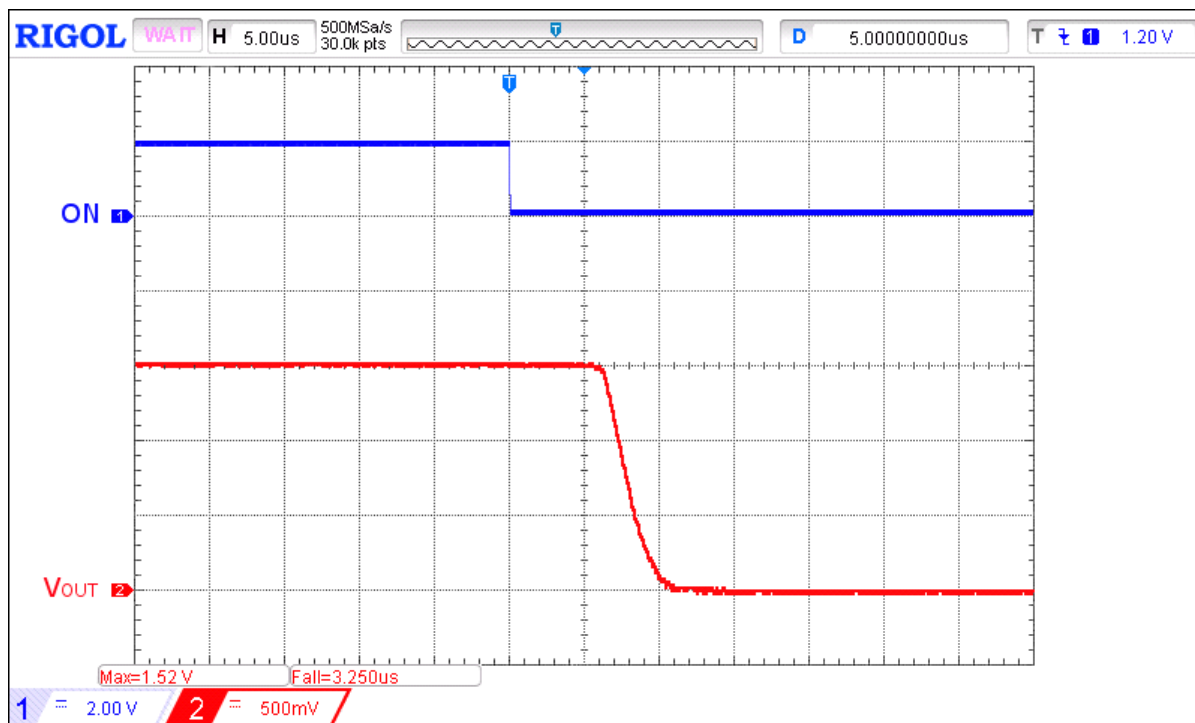
Datasheet

Revision 1.00

30-May-2018

CFR0011-120-01

Page 23 of 30

© 2018 Dialog Semiconductor

An Ultra-low Power, RDS$_{ON}$ 18 mΩ, 1 A, 0.82 mm^2 WLCSP Integrated Power Switch with 550 µs Total Turn-on Time

Applications Information

SLG59M1742C Power-Up/Power-Down Sequence Considerations

During V$_{DD}$ power-up operation, SLG59M1742Cs internal circuitry is activated once V$_{DD}$ crosses 1 V, but the switch will not be turned on if ON = 0. Once V$_{DD}$ has reached 90% of its steady-state value (and within SLG59M1742C's nominal supply voltage range of 2.7 V to 3.6 V), the ON pin can then be toggled LOW-to-HIGH to close the switch.

A nominal power-up sequence is to apply V$_{DD}$ first, followed by V$_{IN}$ only after V$_{DD}$ is > 2.7 V, and finally toggling the ON pin LOW-to-HIGH after V$_{IN}$ is at least 90% of its final value.

A nominal power-down sequence is the power-up sequence in reverse order.

If V$_{DD}$ and V$_{IN}$ are applied at the same time, a voltage glitch may appear on the output pin at V$_{OUT}$. To prevent glitches at the output, it is recommended to connect at least 1 µF capacitor from the V$_{OUT}$ pin to GND and to keep the V$_{DD}$ & V$_{IN}$ ramp times higher than 2 ms.

As illustrated in the typical performance transient scope captures, the V$_{OUT}$ output follows a linear ramp when the power switch is turned on.

If ON and VDD are tied together and powered up, the IPS can be turned on, but the behavior may differ from datasheet specifications.

Power Dissipation

The junction temperature of the SLG59M1742C depends on different factors such as board layout, ambient temperature, and other environmental factors. The primary contributor to the increase in the junction temperature of the SLG59M1742C is the power dissipation of its power MOSFET. Its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$P_D = RDS_{ON} \times I_{DS}^2 + V_{DD} \times I_{DD\_Q2}$$

where:
P$_D$ = Power dissipation, in Watts (W)
RDS$_{ON}$ = Power MOSFET ON resistance, in Ohms (Ω)
I$_{DS}$ = Output current, in Amps (A)
V$_{DD}$ = Applied Supply Voltage, in Volts (V)
I$_{DD\_Q2}$ = IC's Supply Current, in Amps (A)

and

$$T_J = P_D \times \theta_{JA} + T_A$$

where:

T$_J$ = Junction temperature, in Celsius degrees (°C)
θ$_{JA}$ = Package thermal resistance, in Celsius degrees per Watt (°C/W)
T$_A$ = Ambient temperature, in Celsius degrees (°C)

An Ultra-low Power, RDS$_{ON}$ 18 mΩ, 1 A, 0.82 mm^2 WLCSP
Integrated Power Switch with 550 µs Total Turn-on Time

Package Top Marking System Definition

Pin A1 Identifier
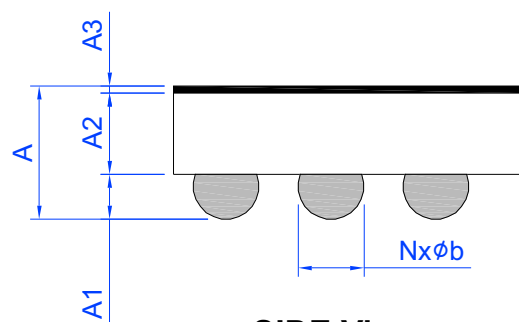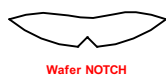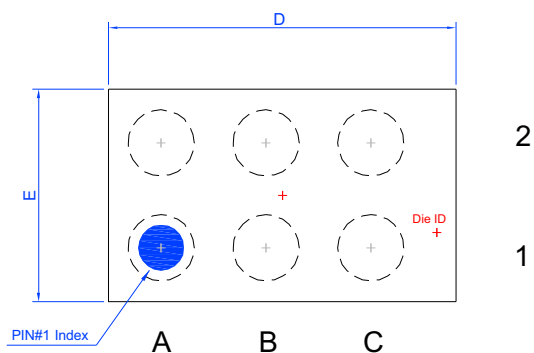
Serial Number Code

NNN - Serial Number Code Field[1]

Note 1: Each character in code field can be alphanumeric A-Z and 0-9

An Ultra-low Power, RDS_{ON} 18 mΩ, 1 A, 0.82 mm^2 WLCSP
Integrated Power Switch with 550 μs Total Turn-on Time
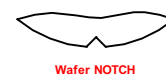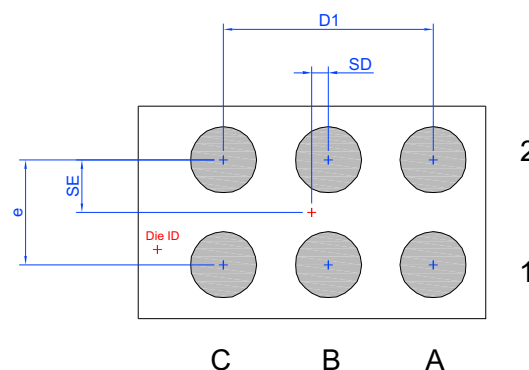
Package Drawing and Dimensions

6 Pin WLCSP Green Package 0.71 x 1.16 mm

## Laser Marking View

Bump View

SIDE View

UNIT: mm							
Symbol	Min.	Nom.	Max.	Symbol	Min.	Nom.	Max.
A	0.390	0.445	0.500	D	1.130	1.160	1.190
A1	0.125	0.150	0.175	E	0.680	0.710	0.740
A2	0.245	0.270	0.295	e	0.35 BSC		
A3	0.020	0.025	0.030	D1	0.70 BSC		
b	0.195	0.220	0.245	SD	0.055 BSC		
N	6 (bump)			SE	0.175 BSC		

An Ultra-low Power, RDS_{ON} 18 mΩ, 1 A, 0.82 mm^2 WLCSP
Integrated Power Switch with 550 µs Total Turn-on Time

SLG59M1742C 6 Pin WLCSP PCB Landing Pattern

Exposed Bump
(Laser marking view)

Recommended
Land Pattern

6X ⌀185 ± 25
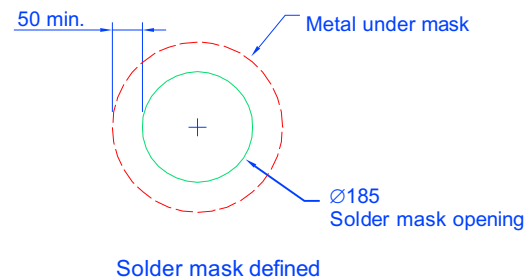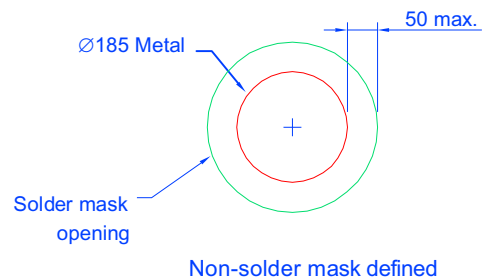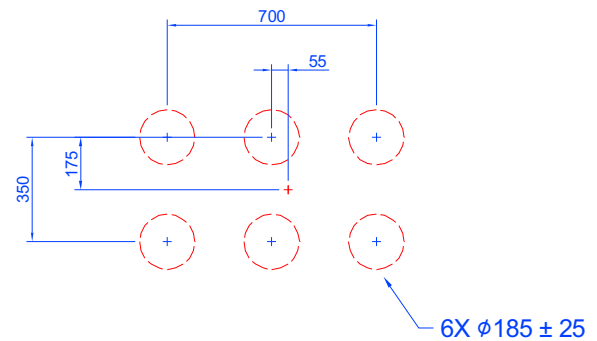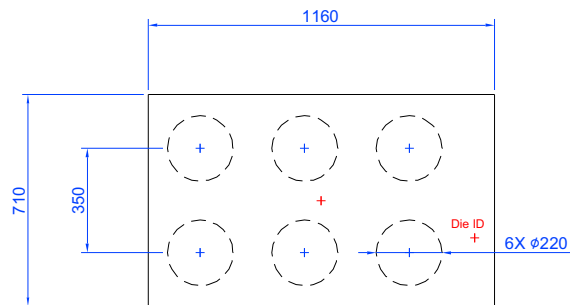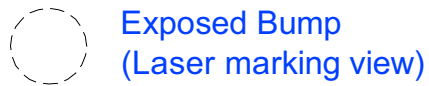
Solder mask detail (not to scale)

Unit: um

An Ultra-low Power, RDS_{ON} 18 mΩ, 1 A, 0.82 mm^2 WLCSP
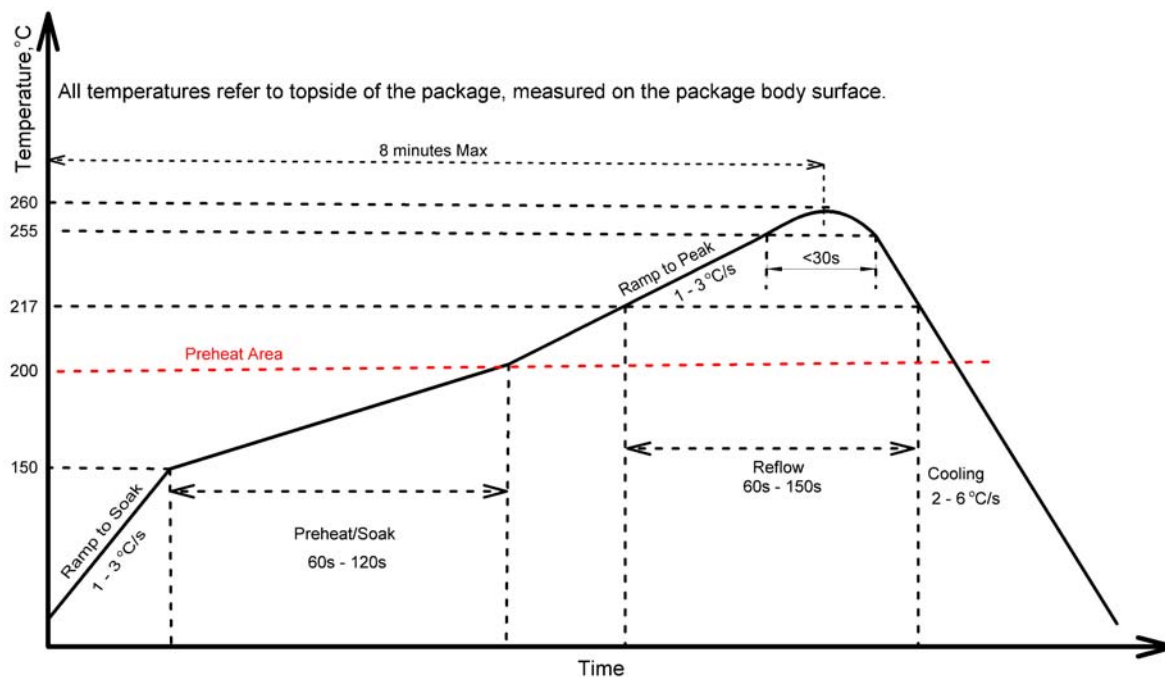Integrated Power Switch with 550 µs Total Turn-on Time

Recommended Reflow Soldering Profile

For successful reflow of the SLG59M1742C a recommended thermal profile is illustrated below:

Note: This reflow profile is for classification/preconditioning and are not meant to specify board assembly profile. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed parameters depicted on figure above.

Please see more information on IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.352 mm^3 (nominal).
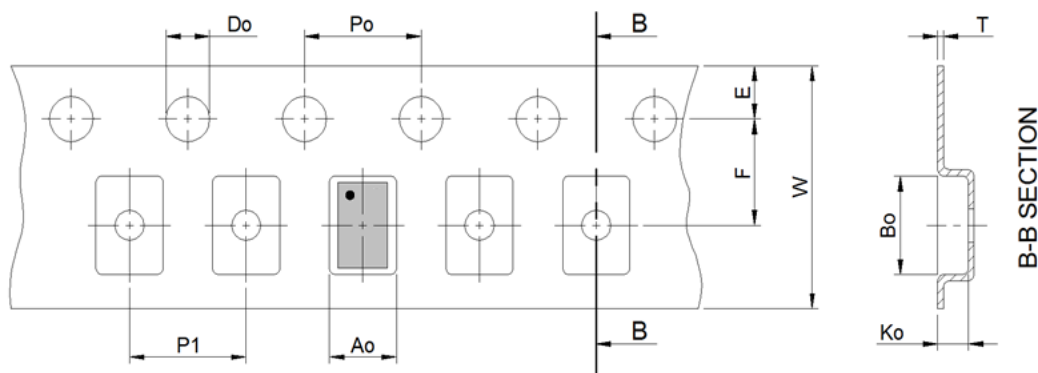
An Ultra-low Power, RDS_{ON} 18 mΩ, 1 A, 0.82 mm^2 WLCSP
Integrated Power Switch with 550 µs Total Turn-on Time

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
WLCSP 6L 0.71 x 1.16 mm 0.35P Green	6	0.71 x 1.16	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
WLCSP 6L 0.71 x 1.16 mm 0.35P Green	0.77	1.22	0.53	4	4	1.5	1.75	3.5	0.2

Refer to EIA-481 specification

An Ultra-low Power, RDS$_{ON}$ 18 mΩ, 1 A, 0.82 mm^2 WLCSP
Integrated Power Switch with 550 µs Total Turn-on Time

Revision History

Date	Version	Change
5/30/2018	1.00	Production Release

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Dialog Semiconductor](#):

  [SLG59M1742C-EVB](#)