A 125 °C Rated, 4 mm^2, 13 mΩ, 3.5 A Integrated Power Switch with Protection Features and an Analog Current Monitor Output

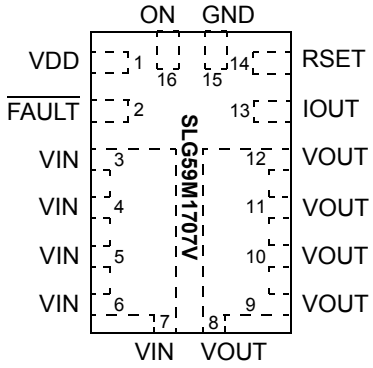
General Description

Operating from a 2.5 V to 5.5 V power supply and fully specified over the -40 °C to 125 °C extended industrial temperature range, the SLG59M1707V is a high-performance 13 mΩ, 3.5 A single-channel nFET integrated power switch designed for all 0.8 V to 5.5 V power rail applications. With a fixed V_{OUT} slew rate of 3 V/ms, inrush current is internally limited. Using a proprietary MOSFET design, the SLG59M1707V achieves a stable 13 mΩ RDS_{ON} across a wide input/supply voltage range. The SLG59M1707V also incorporates resistor-adjustable current limiting as well as thermal protection. Using Silego's proprietary CuFET™ technology for high-current operation, the SLG59M1707V is packaged in a space-efficient, low thermal resistance, RoHS-compliant 1.6mm x 2.5 mm STQFN package.

Features

- Low RDS_{ON} nFET Block: 13 mΩ
- Steady-state Operating Current: Up to 3.5 A
- Supply Voltage: 2.5 V ≤ V_{DD} ≤ 5.5 V
- Wide Input Voltage Range: 0.8 V ≤ V_{IN} ≤ V_{DD}
- Fixed V_{OUT} Slew Rate: 3 V/ms
- Two-stage Overcurrent Protection:
  - Resistor-adjustable Active Current Limit
  - Fixed 0.5 A Short-circuit Current Limit
- Thermal Shutdown Protection
- Analog MOSFET Current Monitor Output: 100 µA/A
- Open-drain $\overline{FAULT}$ Signaling
- Operating Temperature: -40 °C to 125 °C
- Low θ_{JA}, 16-pin 1.6 mm x 2.5 mm STQFN
  - Pb-Free / Halogen-Free / RoHS compliant

Pin Configuration

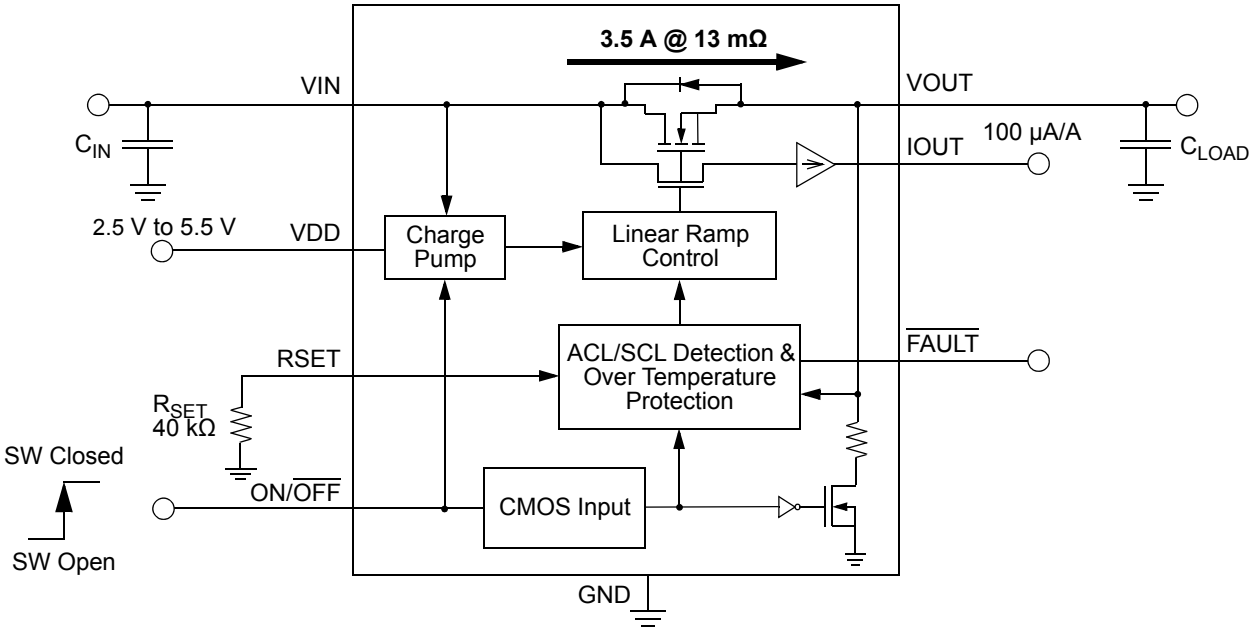


16-pin FC-STQFN
(Top View)

Applications

- Notebook Power Rail Switching
- Tablet Power Rail Switching
- Smartphone Power Rail Switching

Block Diagram



Pin Description

Pin #	Pin Name	Type	Pin Description
1	VDD	PWR	With an internal 1.9V UVLO threshold, VDD supplies the power for the operation of the power switch and internal control circuitry where its range is 2.5 V ≤ V_{DD} ≤ 5.5 V. Bypass the VDD pin to GND with a 0.1 µF (or larger) capacitor
2	$\overline{\text{FAULT}}$	Output	An open drain output, $\overline{\text{FAULT}}$ is asserted within 8ms when a current-limit or an over-temperature condition is detected. $\overline{\text{FAULT}}$ is deasserted within 8 ms when the fault condition is removed. Connect an external 10-kΩ resistor from the $\overline{\text{FAULT}}$ pin to local system logic supply.
3-7	VIN	MOSFET	Drain terminal of Power MOSFET (Pins 3-7 fused together). Connect a 10 µF (or larger) low ESR capacitor from this pin to GND. Capacitors used at VIN should be rated at 10 V or higher.
8-12	VOUT	MOSFET	Source terminal of Power MOSFET (Pins 8-12 fused together). Connect a low ESR capacitor (up to 100 µF) from this pin to GND. Capacitors used at VOUT should be rated at 10 V or higher.
13	IOUT	Output	MOSFET Load Current Monitor Output. As an analog output current, this signal when applied to a ground-reference resistor generates a voltage proportional to the current through the n-channel MOSFET. The I_{OUT} transfer characteristic is typically 100 µA/A with a voltage compliance range of 0.5 V ≤ V_{IOUT} ≤ V_{DD} - 1V. Optimal I_{OUT} linearity is exhibited for 0.5 A ≤ I_{DS} ≤ 3.5 A. Bypass the IOUT pin to GND with a 0.01 µF capacitor.
14	RSET	Input	A 1%-tolerance, metal-film resistor between 20 kΩ and 80 kΩ sets the IPS's active current limit. A 40 kΩ resistor sets the SLG59M1707V's active current limit to 2 A and a 80 kΩ resistor sets the active current limit to 1 A.
15	GND	GND	Ground
16	ON	Input	A low-to-high transition on this pin closes the power switch. ON is an asserted-HIGH, level-sensitive CMOS input with V_{IL} < 0.3 V and V_{IH} > 0.85 V. Connect this pin to the output of a general-purpose output (GPO) from a microcontroller or other application processor. While there is an internal pull down circuit to ground (~4 MΩ), do not allow this pin to be open-circuited.

Ordering Information

Part Number	Type	Production Flow
SLG59M1707V	STQFN 16L	Extended Industrial, -40 °C to 125 °C
SLG59M1707VTR	STQFN 16L (Tape and Reel)	Extended Industrial, -40 °C to 125 °C

Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Pin to GND		--	--	6	V
V_{IN} to GND	Power Switch Input Voltage to GND		-0.3	--	6	V
V_{OUT} to GND	Power Switch Output Voltage to GND		-0.3	--	V_{IN}	V
ON, RSET, IOUT, and $\overline{FAULT}$ to GND	ON, RSET, IOUT, and $\overline{FAULT}$ Pin Voltages to GND		-0.3	--	6	V
T_S	Storage Temperature		-65	--	150	°C
ESD_{HBM}	ESD Protection	Human Body Model	2000	--	--	V
ESD_{CDM}	ESD Protection	Charged Device Model	500	--	--	V
MSL	Moisture Sensitivity Level		1			
θ_{JA}	Package Thermal Resistance, Junction-to-Ambient	1.6mm x 2.5mm STQFN; Determined using 1 in^2, 1.2 oz. copper pads under VIN and VOUT on FR4 pcb material	--	35	--	°C/W
W_{DIS}	Package Power Dissipation		--	--	1.2	W
IDS_{MAX}	Max Continuous Switch Current		--	--	3.5	A
MOSFET IDS_{PK}	Peak Current from Drain to Source	Maximum pulsed switch current, pulse width < 1 ms, 1% duty cycle	--	--	4.5	A

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

T_A = -40 °C to 125 °C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Voltage		2.5	--	5.5	V
$V_{DD(UVLO)}$	V_{DD} Undervoltage Lockout Threshold	V_{DD} ↑	1.6	1.9	2.2	V
		V_{DD} ↓	1.5	1.8	2.2	V
I_{DD}	Power Supply Current when OFF	V_{DD} = V_{IN} = 5.5 V; ON = 0 V	--	--	1	µA
	Power Supply Current, ON (Steady State)	V_{DD} = V_{IN} = ON = 5.5 V; No Load; R_{SET} = 80 kΩ	--	170	210	µA
RDS_{ON}	ON Resistance	T_A 25°C MOSFET @100 mA; V_{DD} = V_{IN} = 5 V	--	13	15.5	mΩ
		T_A 85°C MOSFET @100 mA; V_{DD} = V_{IN} = 5 V		16	19.5	mΩ
		T_A 125°C MOSFET @100 mA; V_{DD} = V_{IN} = 5 V		20	25	mΩ
MOSFET IDS	Current from V_{IN} to V_{OUT}	Continuous	--	--	3.5	A
I_{FET_OFF}	MOSFET OFF Leakage Current	V_{DD} = V_{IN} = 5.5 V; V_{OUT} = 0 V; ON = 0 V	--	0.1	5.5	µA
I_{OUT}	MOSFET Load Current Monitor Output	0.5 V ≤ V_{IOUT} ≤ V_{DD} – 1 V; I_{DS} = 1 A	90	100	120	µA

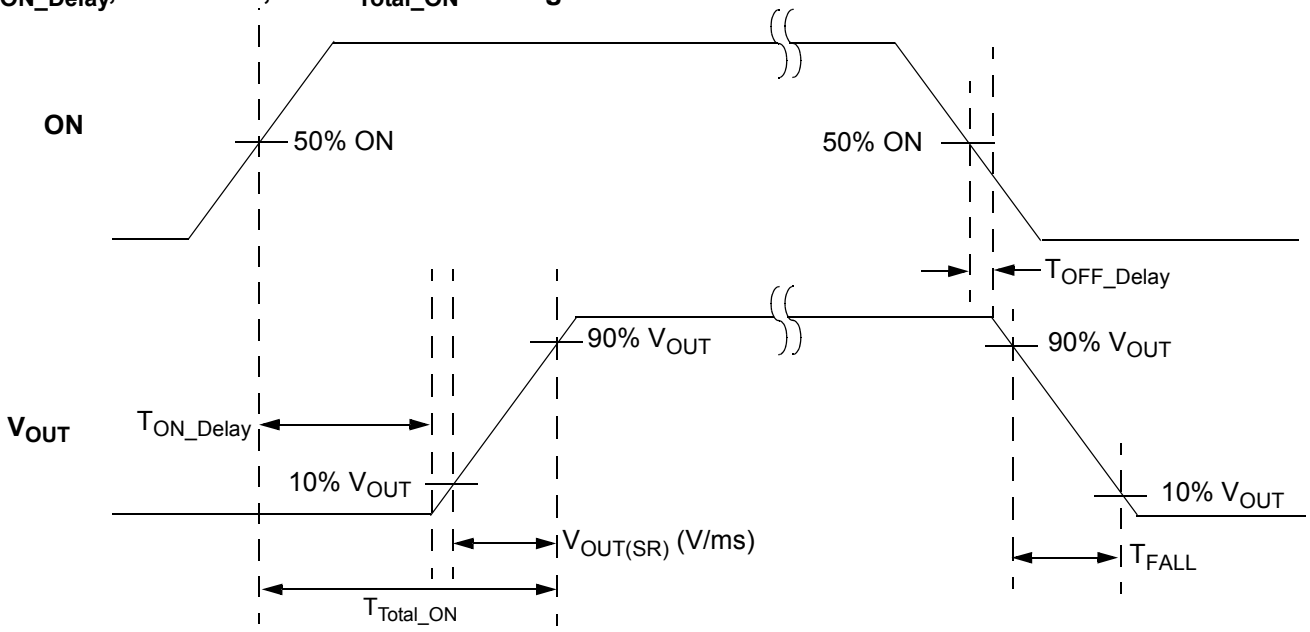
Electrical Characteristics (continued)

T_A = -40 °C to 125 °C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Drain Voltage		0.8	--	V_{DD}	V
T_{ON_Delay}	ON pin Delay Time	50% ON to V_{OUT} Ramp Start, V_{DD} = V_{IN} = 5 V; R_{LOAD} = 20 Ω; C_{LOAD} = 10 µF	--	200	500	µs
$V_{OUT(SR)}$	V_{OUT} Slew Rate	10% V_{OUT} to 90% V_{OUT} ↑; V_{DD} = V_{IN} = 5 V; R_{LOAD} = 20 Ω; C_{LOAD} = 10 µF	2.4	3	3.6	V/ms
T_{Total_ON}	Total Turn-on Time	50% ON to 90% V_{OUT} ↑; V_{DD} = V_{IN} = 5 V; R_{LOAD} = 20 Ω; C_{LOAD} = 10 µF	1.4	1.8	2.2	ms
T_{OFF_Delay}	OFF Delay Time	50% ON to V_{OUT} Fall; V_{DD} = V_{IN} = 5 V; R_{LOAD} = 20 Ω; no C_{LOAD}	--	6	9	µs
C_{LOAD}	Output Load Capacitance	C_{LOAD} connected from VOUT to GND	1	10	100	µF
I_{LIMIT}	Active Current Limit, I_{ACL}	V_{OUT} > 0.25 V; R_{SET} = 40 kΩ[1]	1.5	2	2.5	A
	Short-circuit Current Limit, I_{SCL}	V_{OUT} < 0.25 V	--	0.5	--	A
$T\overline{FAULT}_{LOW}$	FAULT Assertion Time	Abnormal Step Load Current event to Fault↓[1]	5	8	12	ms
$T\overline{FAULT}_{HIGH}$	FAULT De-assertion Time	Delay to $\overline{FAULT}$↑ after fault condition is removed[1]	5	8	12	ms
$\overline{FAULT}_{VOL}$	$\overline{FAULT}$ Output Low Voltage	$I_{\overline{FAULT}}$ = 1 mA	--	0.2	--	V
ON_V_{IH}	High Input Voltage on ON pin		0.85	--	V_{DD}	V
ON_V_{IL}	Low Input Voltage on ON pin		-0.3	0	0.3	V
$R_{DISCHRG}$	Output Discharge Resistance	V_{DD} = V_{IN} = 5 V	--	210	250	Ω
$THERM_{ON}$	Thermal shutoff turn-on temperature	V_{DD} = V_{IN} = 5 V	--	150	--	°C
$THERM_{OFF}$	Thermal shutoff turn-off temperature	V_{DD} = V_{IN} = 5 V	--	130	--	°C

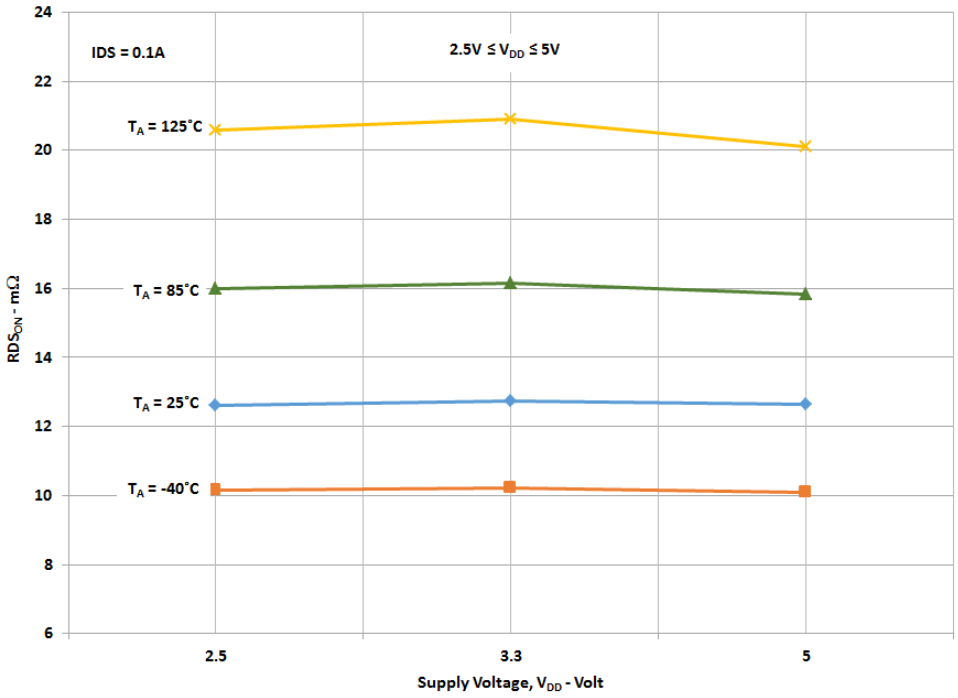
Notes:
1. See Application Diagram on Page 15.

T_{ON_Delay}, Slew Rate, and T_{Total_ON} Timing Details

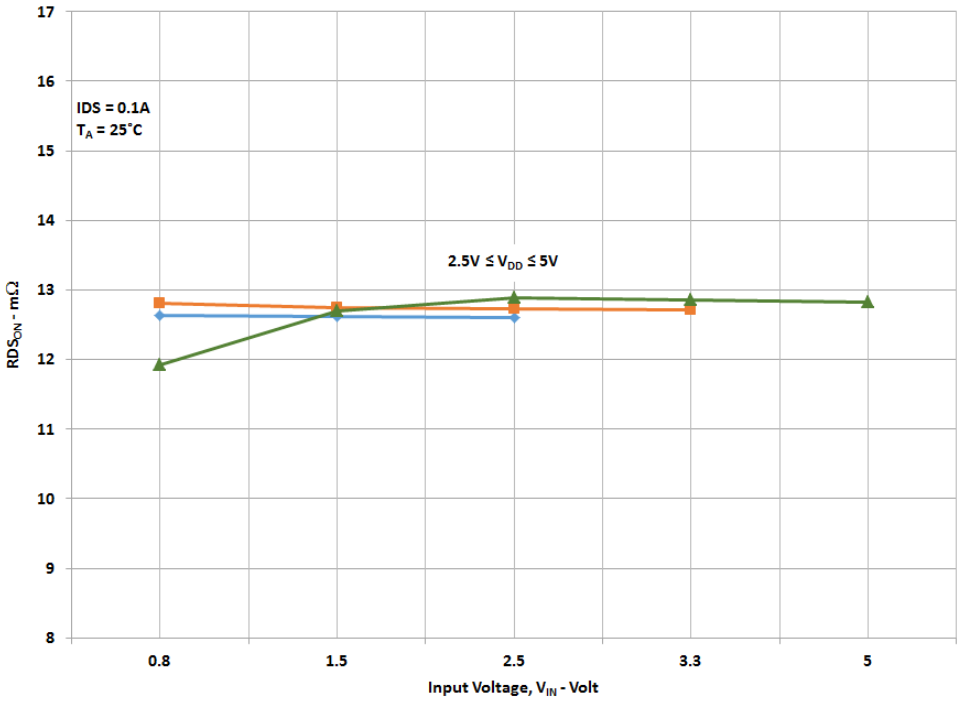


Typical Performance Characteristics

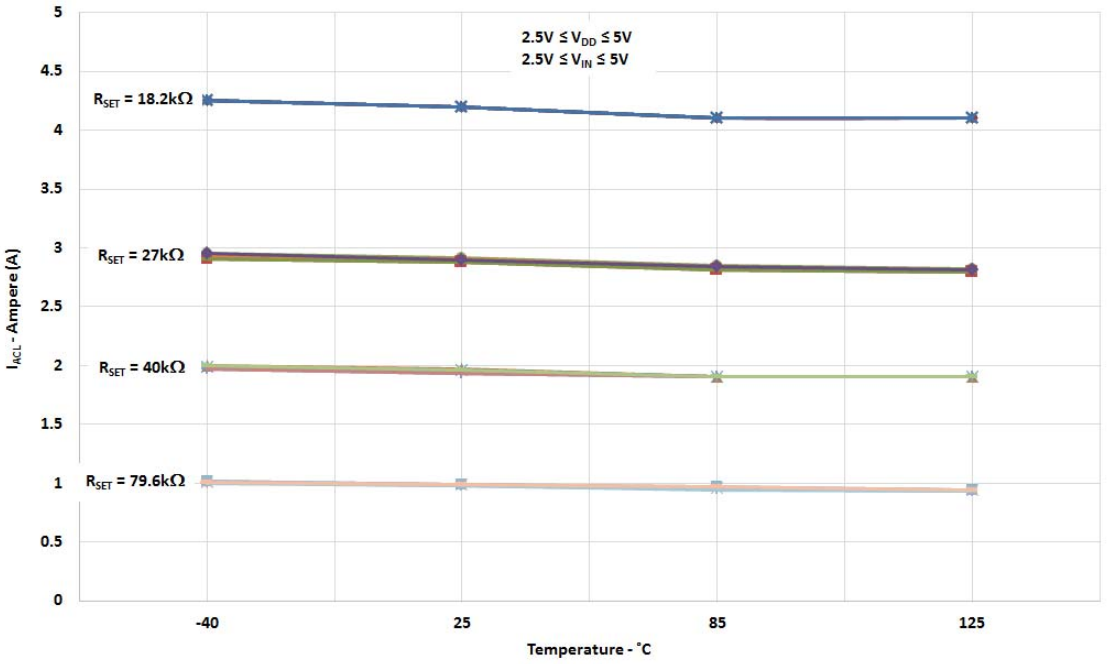
RDS_{ON} vs. Temperature and V_{DD}



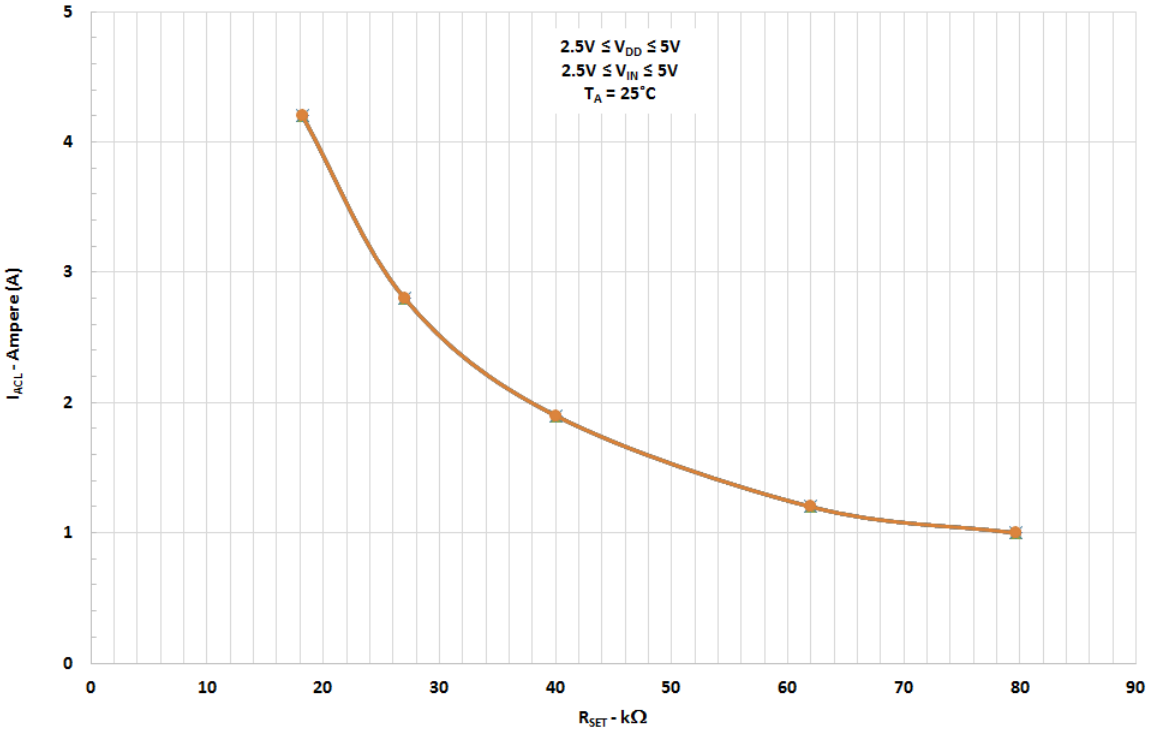
RDS_{ON} vs. V_{IN} and V_{DD}



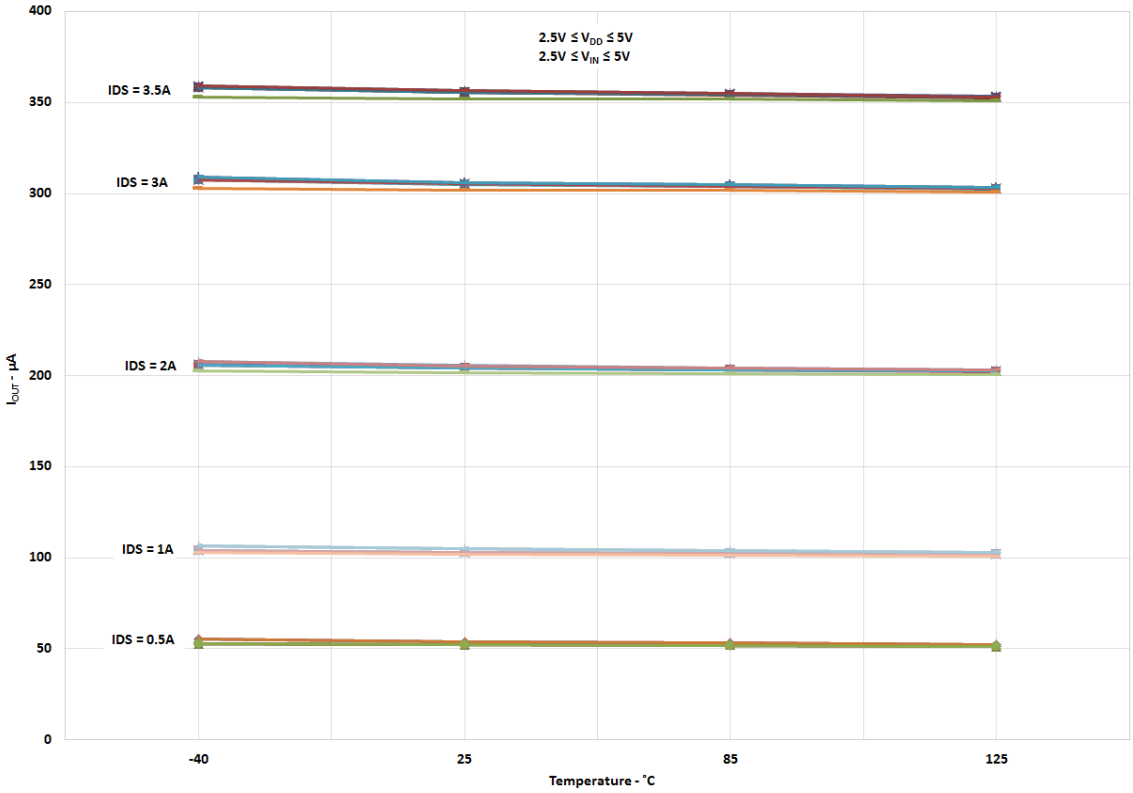
I_{ACL} vs. Temperature, R_{SET}, V_{DD}, and V_{IN}



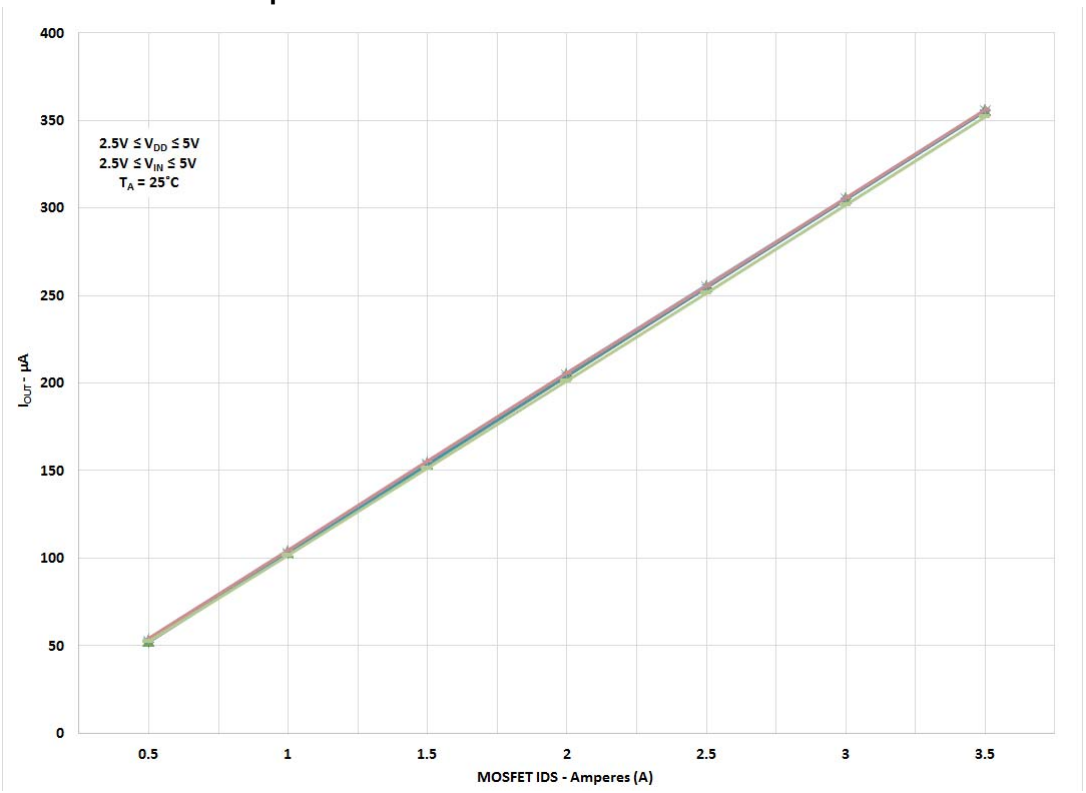
I_{ACL} vs. R_{SET}, V_{DD}, and V_{IN}



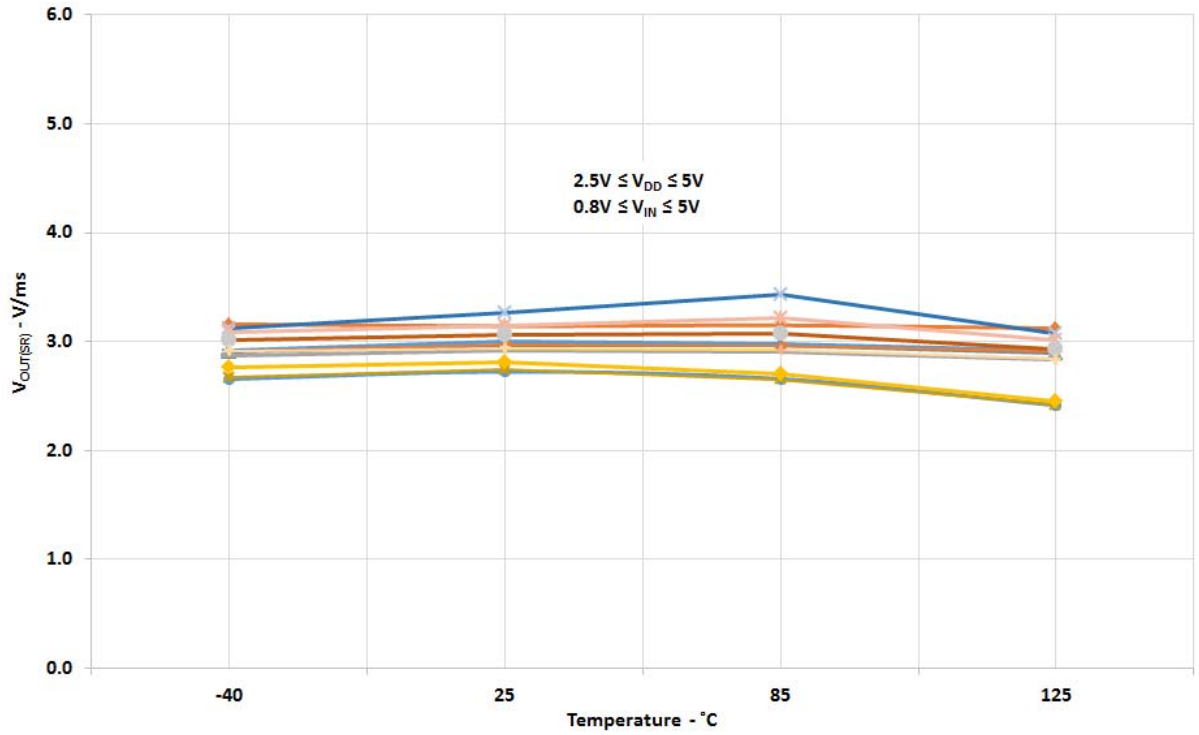
I_{OUT} vs. Temperature and MOSFET IDS



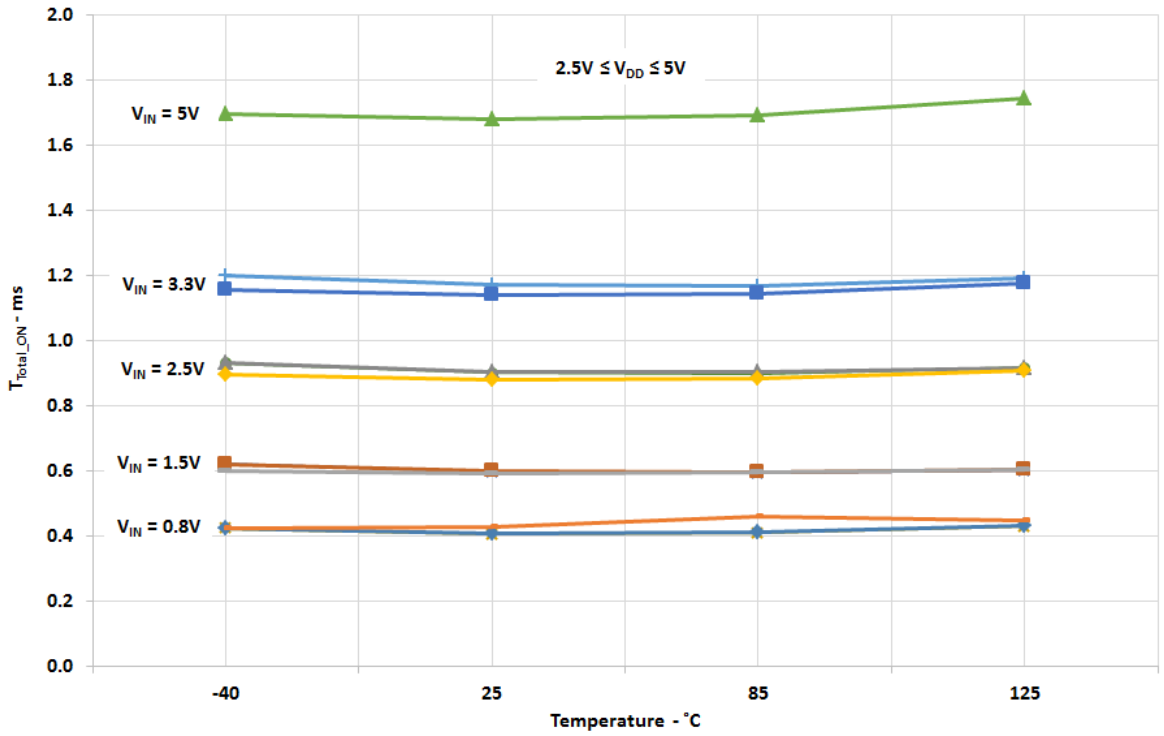
I_{OUT} vs. MOSFET IDS and Temperature



V_{OUT} Slew Rate vs. Temperature, V_{DD}, and V_{IN}



T_{Total_ON} vs. Temperature, V_{DD}, and V_{IN}



Typical Turn-on Waveforms

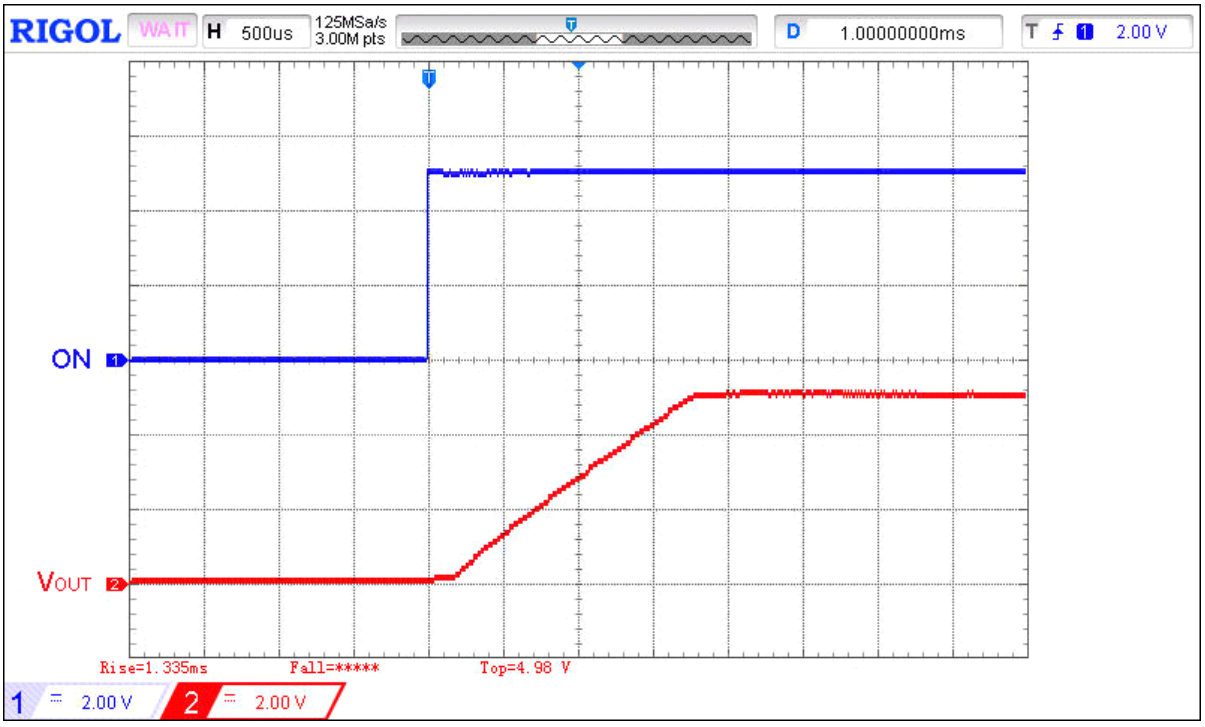


Figure 1. Typical Turn ON operation waveform for V_{DD} = V_{IN} = 5 V, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω

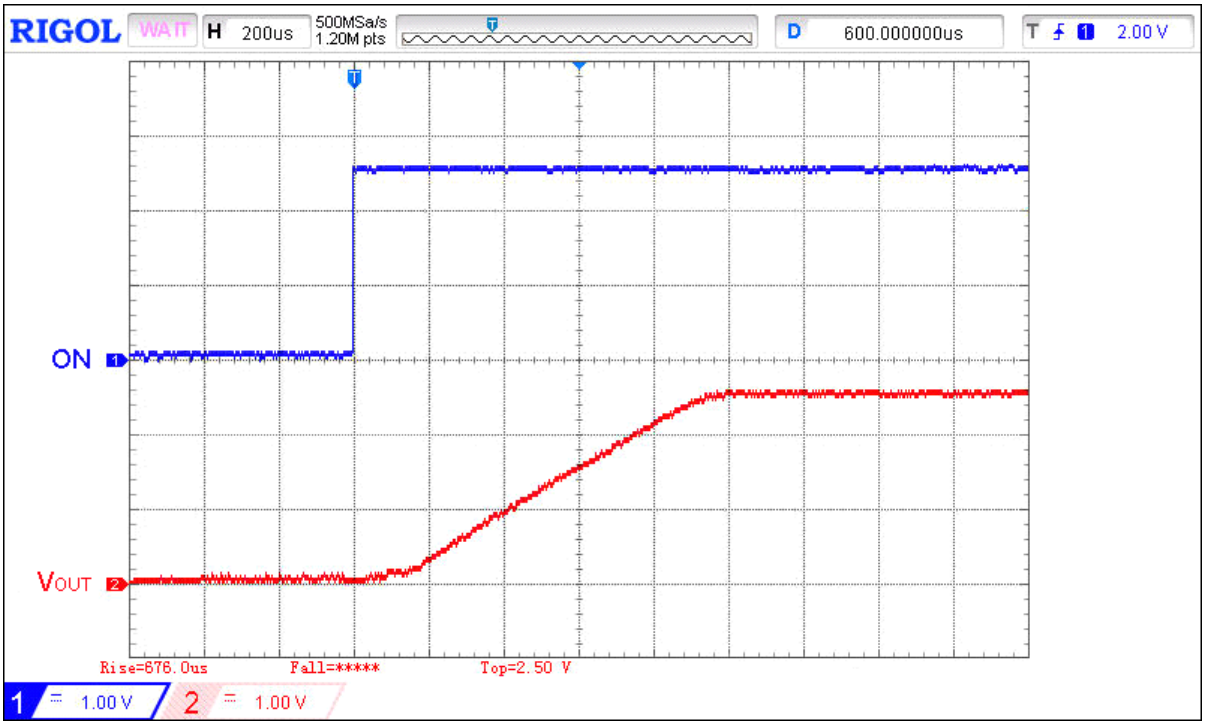


Figure 2. Typical Turn ON operation waveform for V_{DD} = V_{IN} = 2.5 V, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω

Typical Turn-off Waveforms

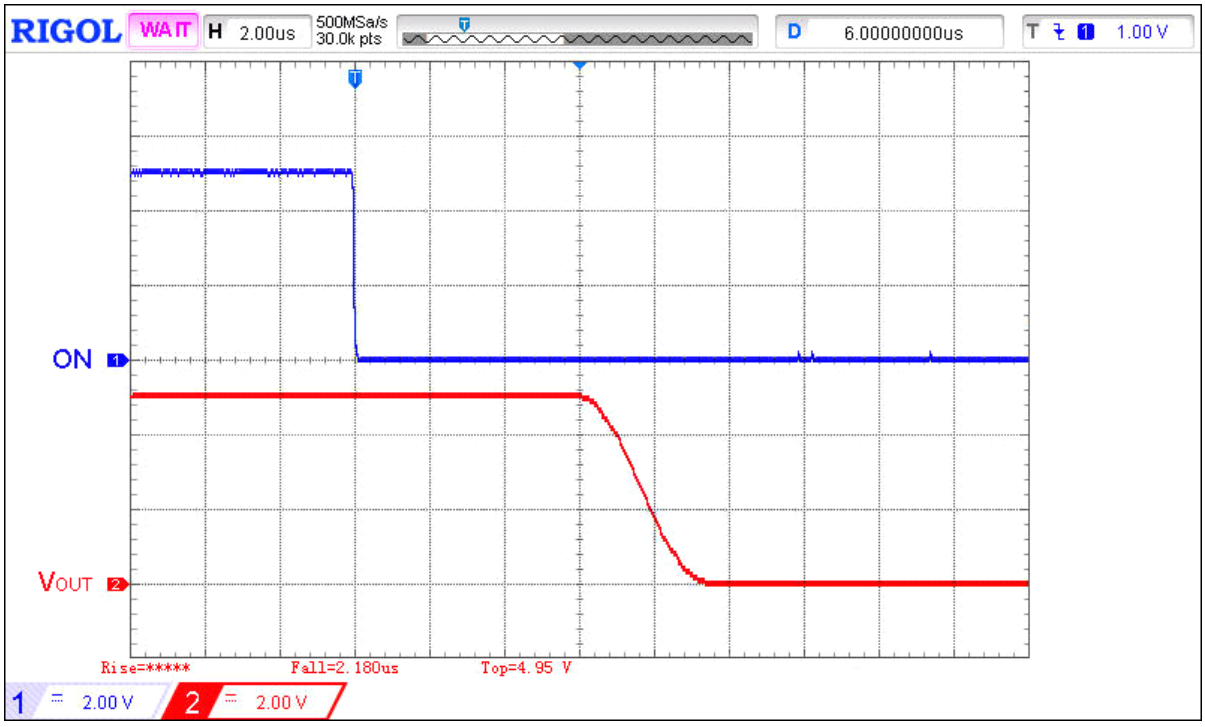


Figure 3. Typical Turn OFF operation waveform for V_{DD} = V_{IN} = 5 V, no C_{LOAD}, R_{LOAD} = 20 Ω

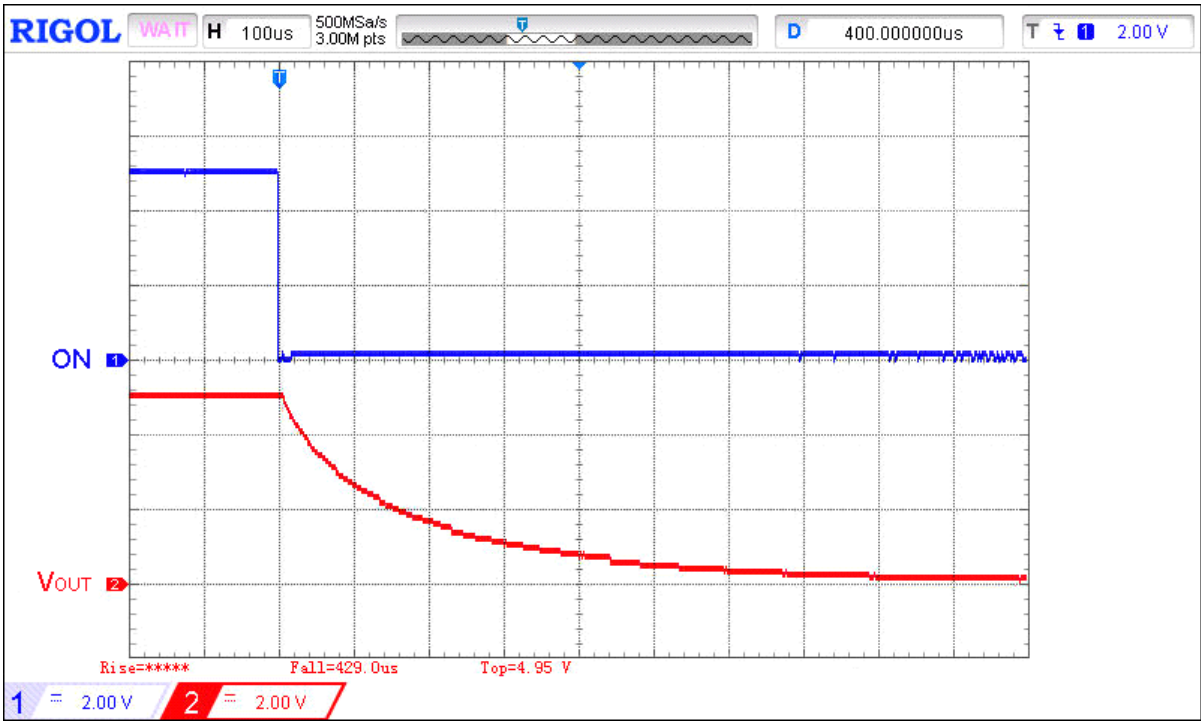


Figure 4. Typical Turn OFF operation waveform for V_{DD} = V_{IN} = 5 V, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω

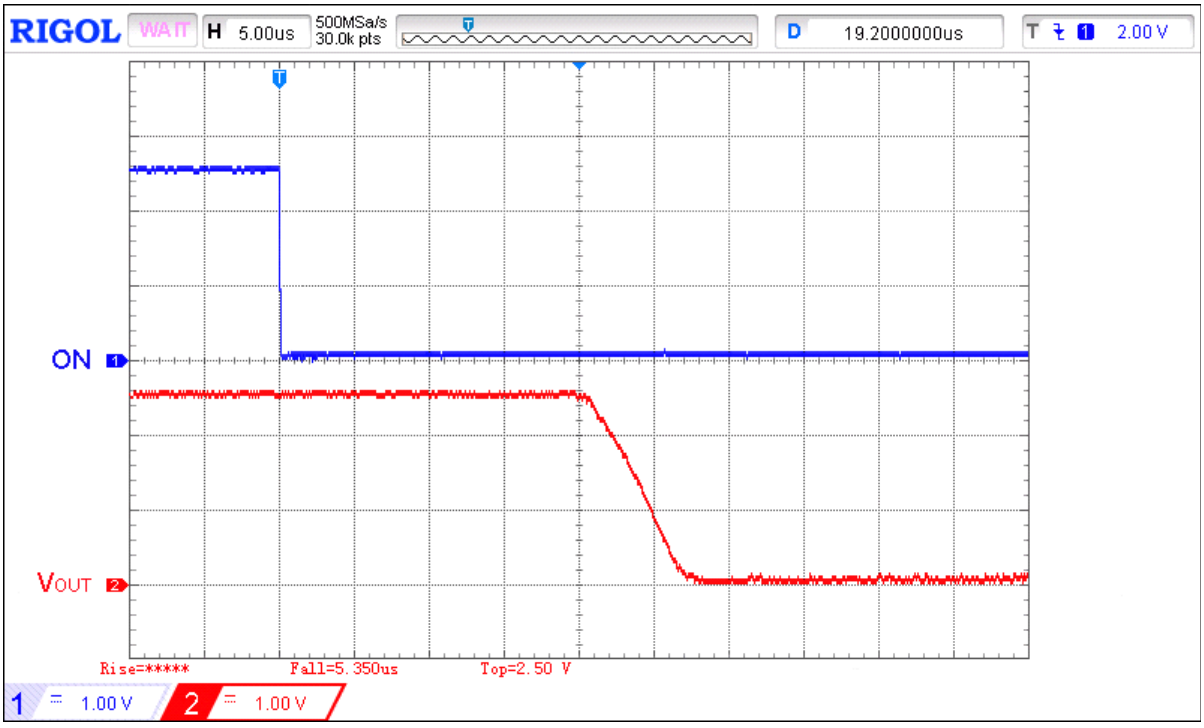


Figure 5. Typical Turn OFF operation waveform for V_{DD} = V_{IN} = 2.5 V, no C_{LOAD}, R_{LOAD} = 20 Ω

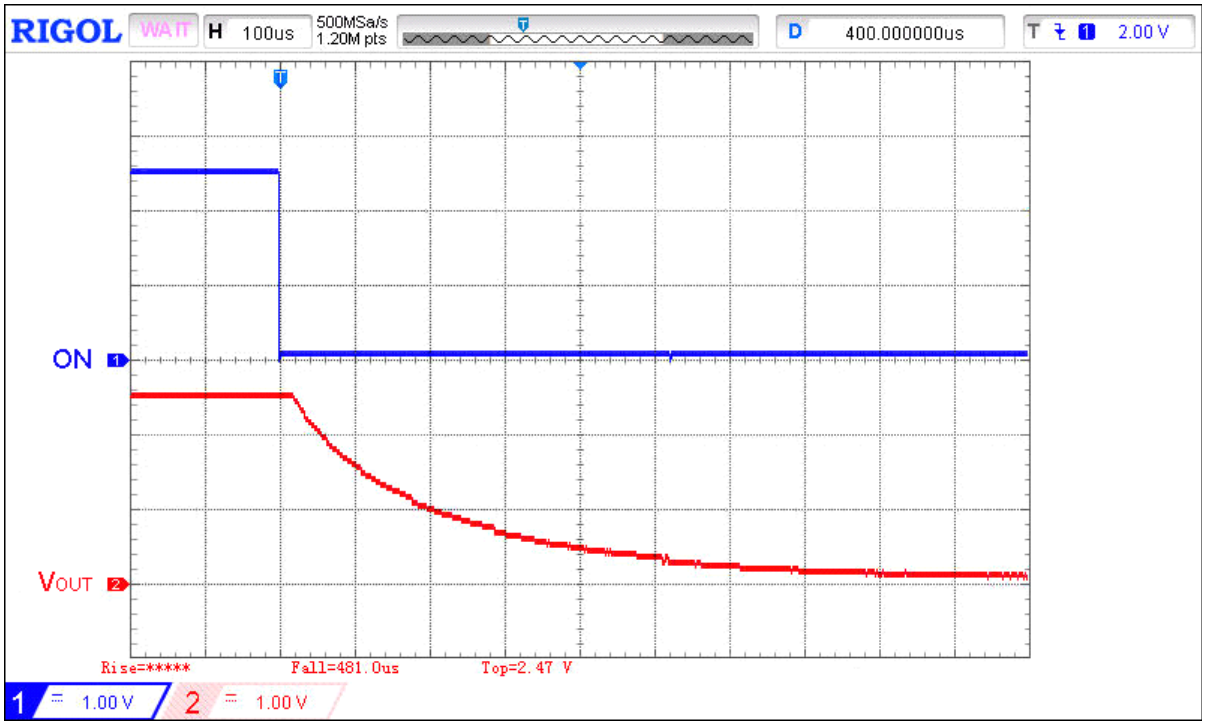
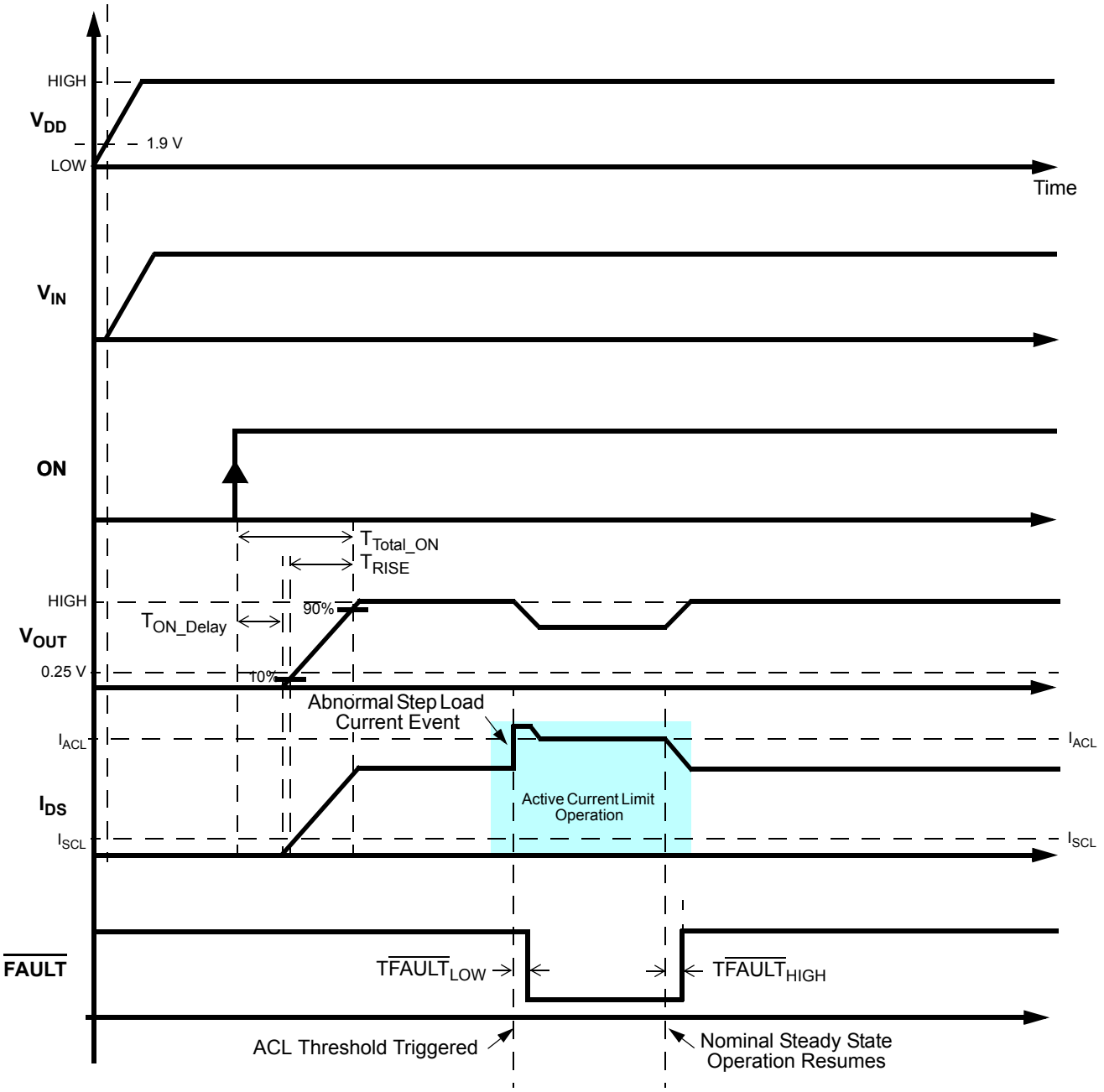
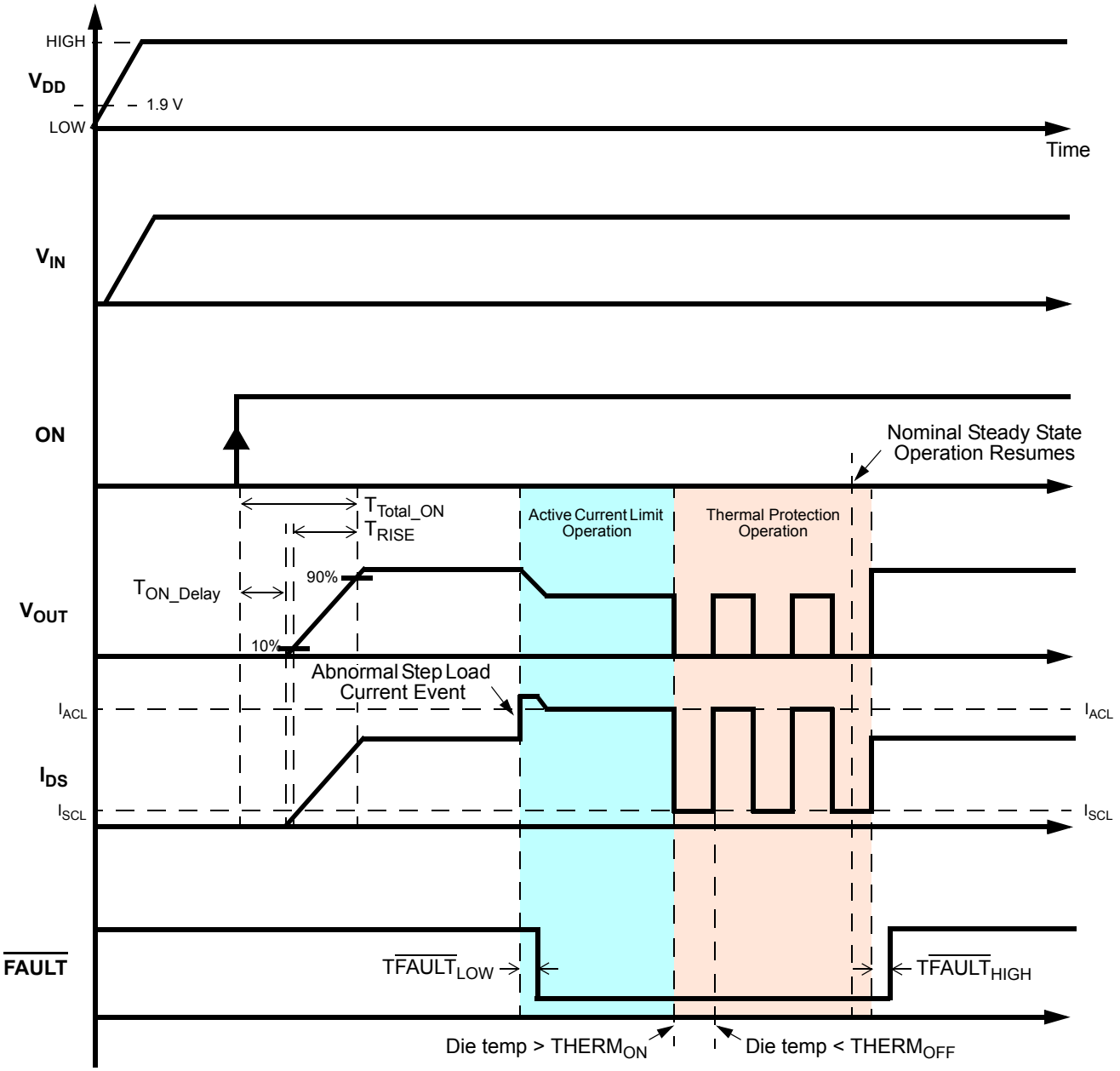


Figure 6. Typical Turn OFF operation waveform for V_{DD} = V_{IN} = 2.5 V, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω

Timing Diagram - Basic Operation including Active Current Limit Protection



Timing Diagram - Active Current Limit & Thermal Protection Operation



SLG59M1707V Application Diagram

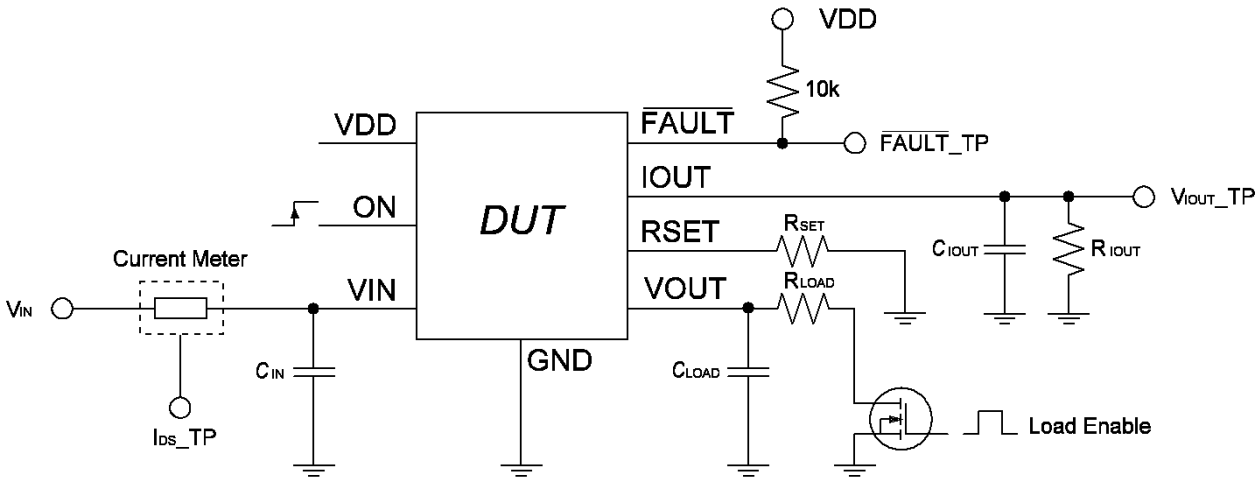


Figure 7. Test setup Application Diagram

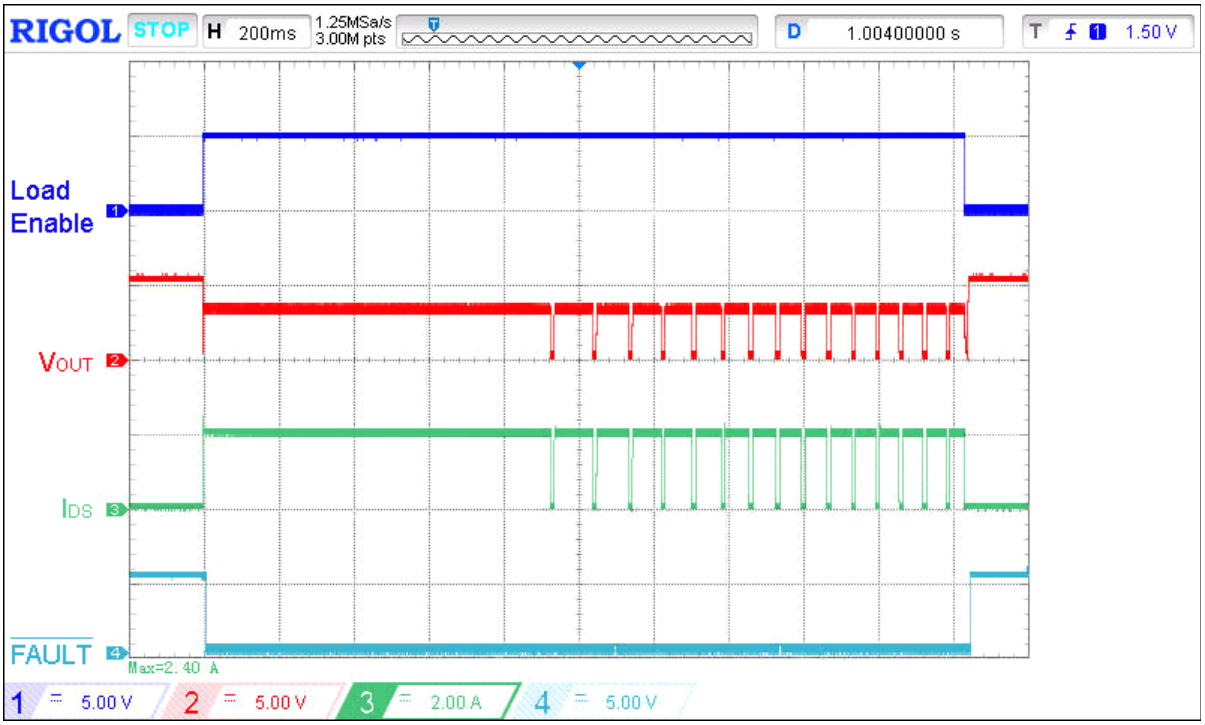


Figure 8. Typical ACL operation waveform for V_{DD} = V_{IN} = 5 V, C_{LOAD} = 10 µF, I_{DS} = 2 A, R_{SET} = 40 kΩ

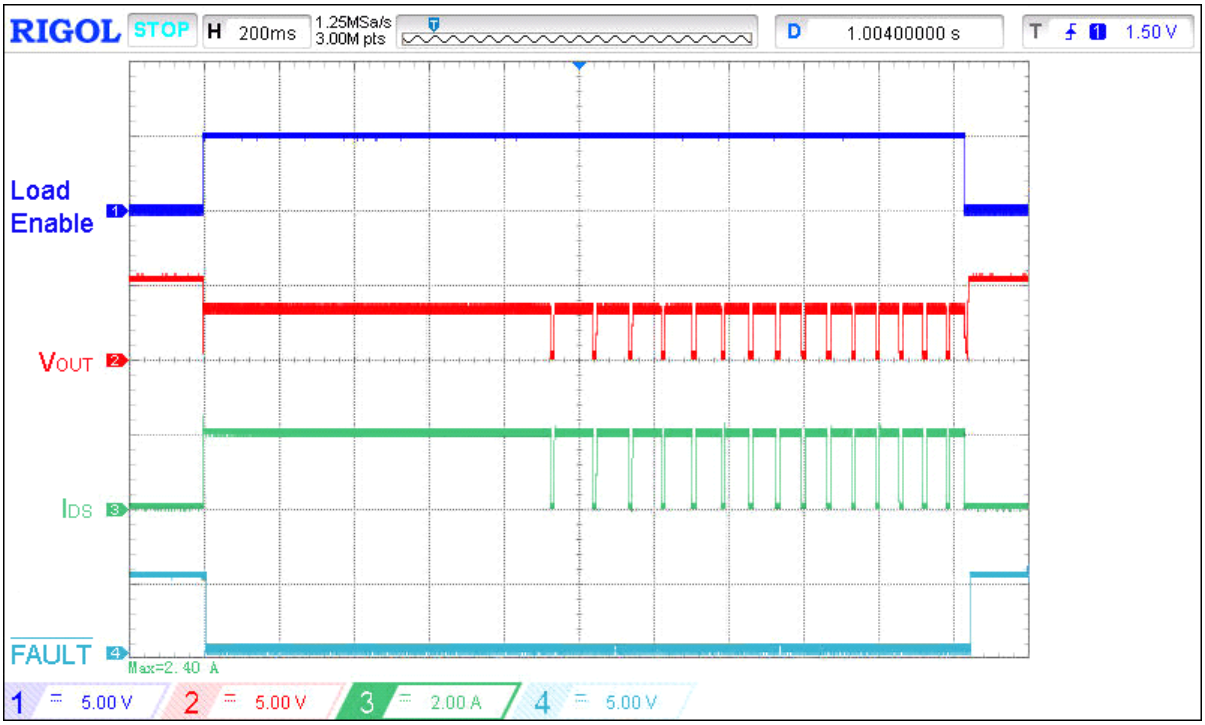


Figure 9. Typical $\overline{\text{FAULT}}$ assertion waveform for V_{DD} = V_{IN} = 5 V, C_{LOAD} = 10 µF, I_{ACL} = 2 A, R_{SET} = 40 kΩ, switch in 2 Ω load

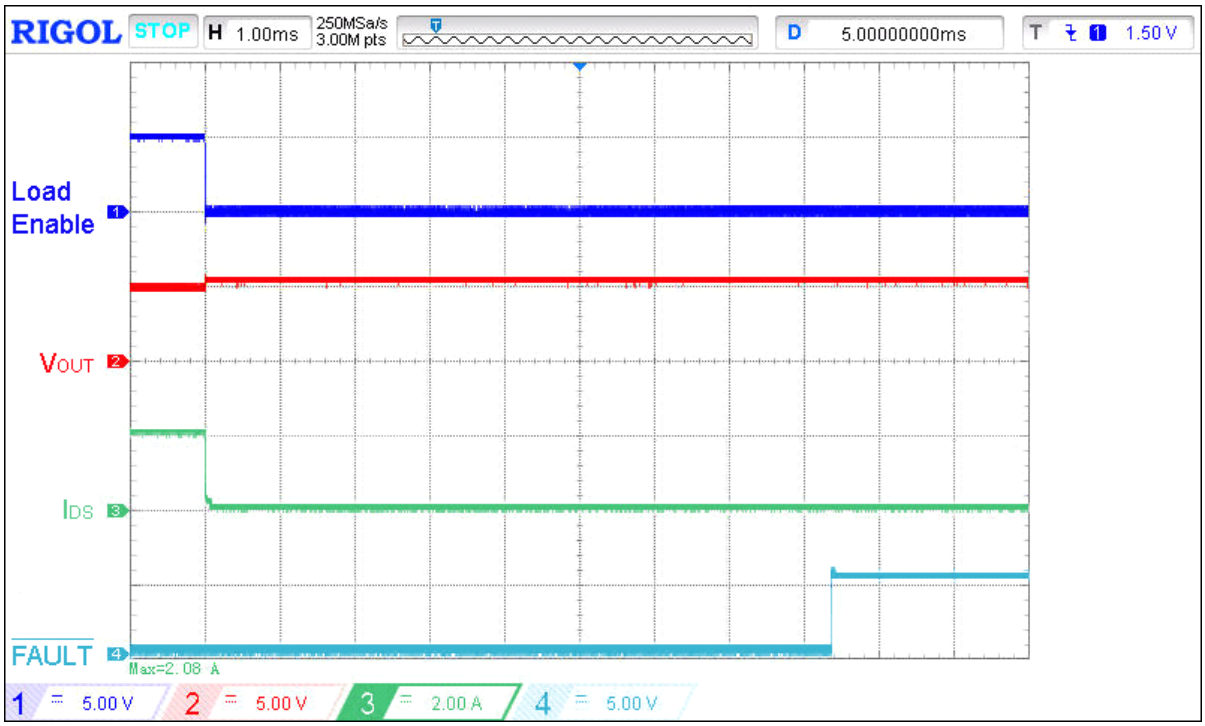


Figure 10. Typical $\overline{\text{FAULT}}$ de-assertion waveform for V_{DD} = V_{IN} = 5 V, C_{LOAD} = 10 µF, I_{ACL} = 2 A, R_{SET} = 40 kΩ, switch out 2 Ω load

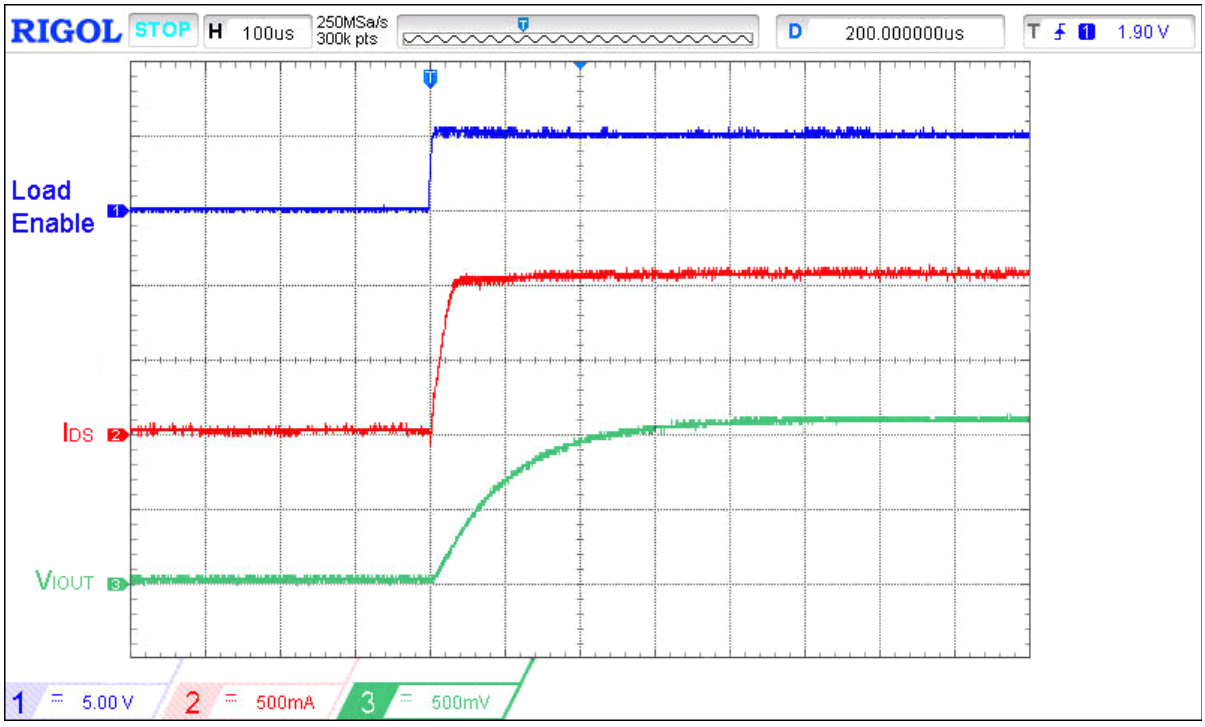


Figure 11. Typical I_{OUT} response time waveform for V_{DD} = V_{IN} = 5 V, C_{LOAD} = 10 µF, R_{LOAD} = 5 Ω, C_{IOUT} = 0.01 µF, R_{IOUT} = 10 kΩ, Load Step 0 A to 1 A

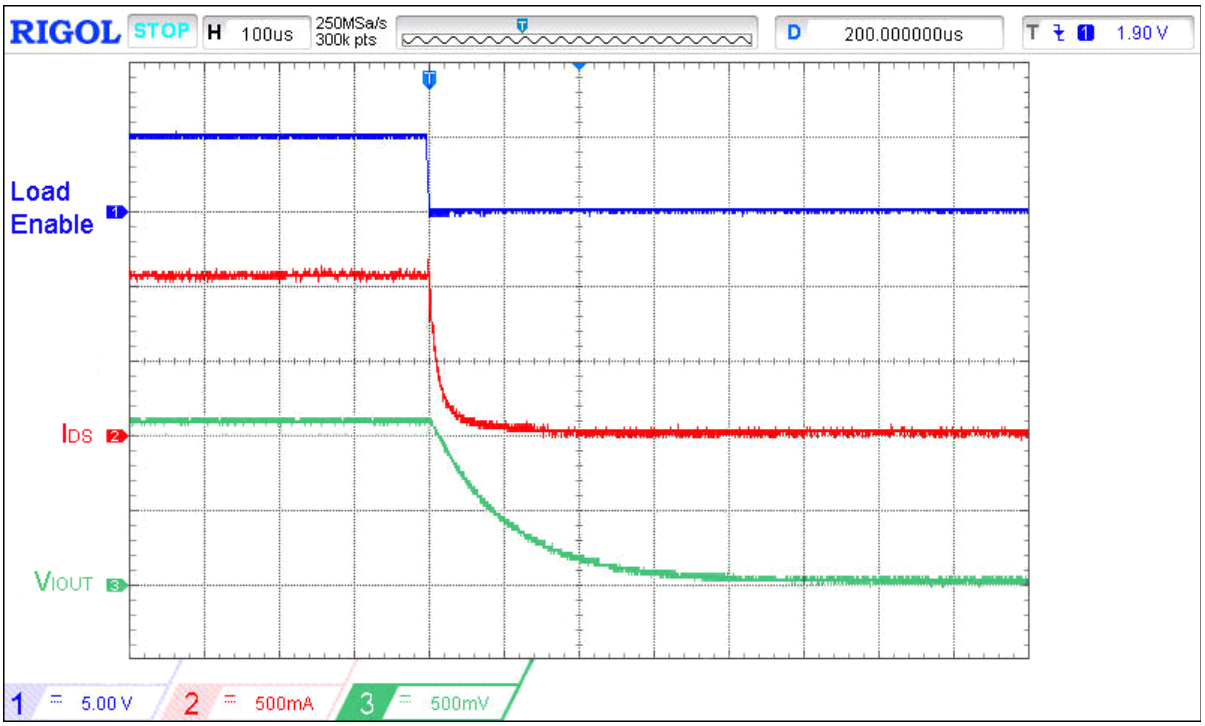


Figure 12. Typical I_{OUT} response time waveform for V_{DD} = V_{IN} = 5 V, C_{LOAD} = 10 µF, R_{LOAD} = 5 Ω, C_{IOUT} = 0.01 µF, R_{IOUT} = 10 kΩ, Load Step 1 A to 0 A

SLG59M1707V Power-Up/Power-Down Sequence Considerations

To ensure glitch-free power-up under all conditions, apply V_{DD} first, followed by V_{IN} after V_{DD} exceeds 1.9 V. Then allow V_{IN} to reach 90% of its max value before toggling the ON pin from Low-to-High. Likewise, power-down in reverse order.

If V_{DD} and V_{IN} need to be powered up simultaneously, glitching can be minimized by having a suitable load capacitor. A 10 µF C_{LOAD} will prevent glitches for rise times of V_{DD} and V_{IN} less than 2 ms.

If the ON pin is toggled HIGH before V_{DD} and V_{IN} have reached their steady-state values, the IPS timing parameters may differ from datasheet specifications.

SLG59M1707V Current Limiting Operation

The SLG59M1707V has two types of current limiting triggered by the output V_{OUT} pin voltage.

1. Standard Current Limiting Mode (with Thermal Shutdown Protection)

When the V_{OUT} pin voltage > 250 mV, the output current is initially limited to the Active Current Limit (I_{ACL}) specification listed in the Electrical Characteristics table. The ACL monitor's response time is very fast and is triggered within a few microseconds to sudden (transient) changes in load current. When a load current overload is detected, the ACL monitor increases the FET resistance to keep the current from exceeding the power switch's I_{ACL} threshold. During active current-limit operation, V_{OUT} is also reduced by I_{ACL} x $RDSON_{ACL}$. This observed behavior is illustrated in the timing diagrams on Pages 13 and 14.

When a current-limit event is detected, the $\overline{FAULT}$ signal becomes asserted in approximately $T\overline{FAULT}_{LOW}$ and the SLG59M1707V operates in constant current mode with the output current set by R_{SET} (see R_{SET}-Current Limit Table). The SLG59M1707V continues to operate in constant current mode indefinitely until a) the current-limit event has elapsed or b) the SLG59M1707V's internal thermal shutdown threshold is reached. When a current-limit event has elapsed or been removed, its $\overline{FAULT}$ signal will be deasserted after approximately $T\overline{FAULT}_{HIGH}$.

Once thermal shutdown has been triggered, the IC's $\overline{FAULT}$ signal will remain asserted. As the die cools, the MOSFET will be turned back on when the die temperature falls to ~130°C; in this case, the $\overline{FAULT}$ signal will be deasserted in approximately $T\overline{FAULT}_{HIGH}$. If the current-limiting condition has not elapsed or been removed, die temperature will increase and the SLG59M1707V's thermal shutdown operation will repeat indefinitely.

2. Short Circuit Current Limiting Mode (with Thermal Shutdown Protection)

The SLG59M1707V's short-circuit current-limit monitor includes two operating modes depending upon the state of the IC's ON pin:

a) Before ON low-to-high transition

When the V_{OUT} voltage < 0.25 V (which is the case with a hard short, such as a solder bridge on the power rail), the power switch's internal Short-circuit Current Limit (SCL) monitor limits the FET current to approximately 500 mA (the I_{SCL} threshold). The SLG59M1707V's short-circuit current limit (SCL) protection scheme is disabled automatically once V_{OUT} rises above 0.25 V. While the internal Thermal Shutdown Protection circuit remains enabled and since the I_{SCL} threshold is much lower than the I_{ACL} threshold, thermal shutdown protection may become activated only at higher ambient temperatures.

b) After ON low-to-high transition

If a short-circuit or a very large load current transient occurs after an ON low-to-high transition, the SLG59M1707V's internal SCL circuit will be triggered if V_{OUT} falls by 0.4 V. The response time of this fast turn-off detection is ~1 µs.

SLG59M1707V $\overline{\text{FAULT}}$ Operation

As previously stated in the Pin Description section, the open-drain $\overline{\text{FAULT}}$ output is asserted when an active-current limit (ACL) or thermal shutdown fault condition is detected. This output becomes asserted in $T\overline{\text{FAULT}}_{LOW}$ upon the detection of a fault condition and becomes deasserted $T\overline{\text{FAULT}}_{HIGH}$ once the fault condition is removed. If the ON pin is toggled HIGH-to-LOW while the $\overline{\text{FAULT}}$ output is low, the $\overline{\text{FAULT}}$ output is deasserted without delay.

Setting the SLG59M1707V Output Current Limit with R_{SET}

The current-limit operation of the SLG59M1707V begins by choosing the appropriate ±1%-tolerance R_{SET} value for the application. The recommended range for R_{SET} is:

$$20\ k\Omega \leq R_{SET} \leq 80\ k\Omega$$

which corresponds to an output constant current limit in the following range:

$$1\ A \leq I_{ACL} \leq 4\ A$$

Table 1: Setting Current Limit Threshold vs. R_{SET}

Constant Current Limit	R_{SET}
1 A	80 kΩ
2 A	40 kΩ
4 A	20 kΩ

Power Dissipation

The junction temperature of the SLG59M1707V depends on different factors such as board layout, ambient temperature, and other environmental factors. The primary contributor to the increase in the junction temperature of the SLG59M1707V is the power dissipation of its power MOSFET. Its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD = RDS_{ON} \times I_{DS}^2$$

where:
PD = Power dissipation, in Watts (W)
RDS_{ON} = Power MOSFET ON resistance, in Ohms (Ω)
I_{DS} = Output current, in Amps (A)

and

$$T_J = PD \times \Theta_{JA} + T_A$$

where:

T_J = Junction temperature, in Celsius degrees (°C)
Θ_{JA} = Package thermal resistance, in Celsius degrees per Watt (°C/W)
T_A = Ambient temperature, in Celsius degrees (°C)

Power Dissipation (continued)

During active current-limit operation, the SLG59M1707V's power dissipation can be calculated by taking into account the voltage drop across the power switch (V_{IN} - V_{OUT}) and the magnitude of the output current in active current-limit operation (I_{ACL}):

$$PD = (V_{IN} - V_{OUT}) \times I_{ACL} \text{ or}$$

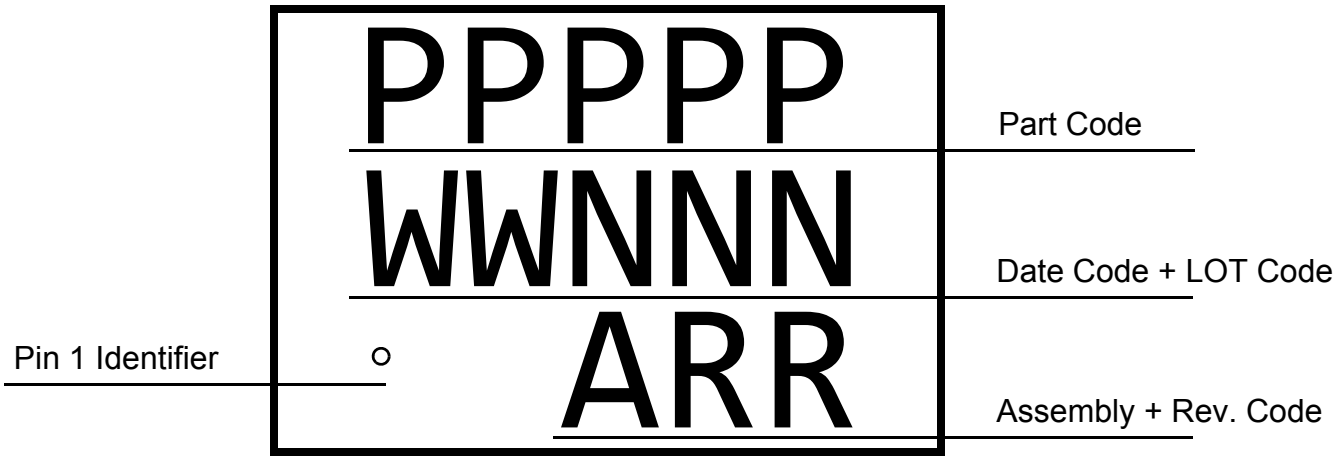
$$PD = (V_{IN} – (R_{LOAD} \times I_{ACL})) \times I_{ACL}$$

where:

PD = Power dissipation, in Watts (W)
V_{IN} = Input Voltage, in Volts (V)
R_{LOAD} = Load Resistance, in Ohms (Ω)
I_{ACL} = Output limited current, in Amps (A)
$V_{OUT} = R_{LOAD} \times I_{ACL}$

For more information on Silego GreenFET3 integrated power switch features, please visit our Application Notes page at our website and see App Note "AN-1068 GreenFET3 Integrated Power Switch Basics".

Package Top Marking System Definition

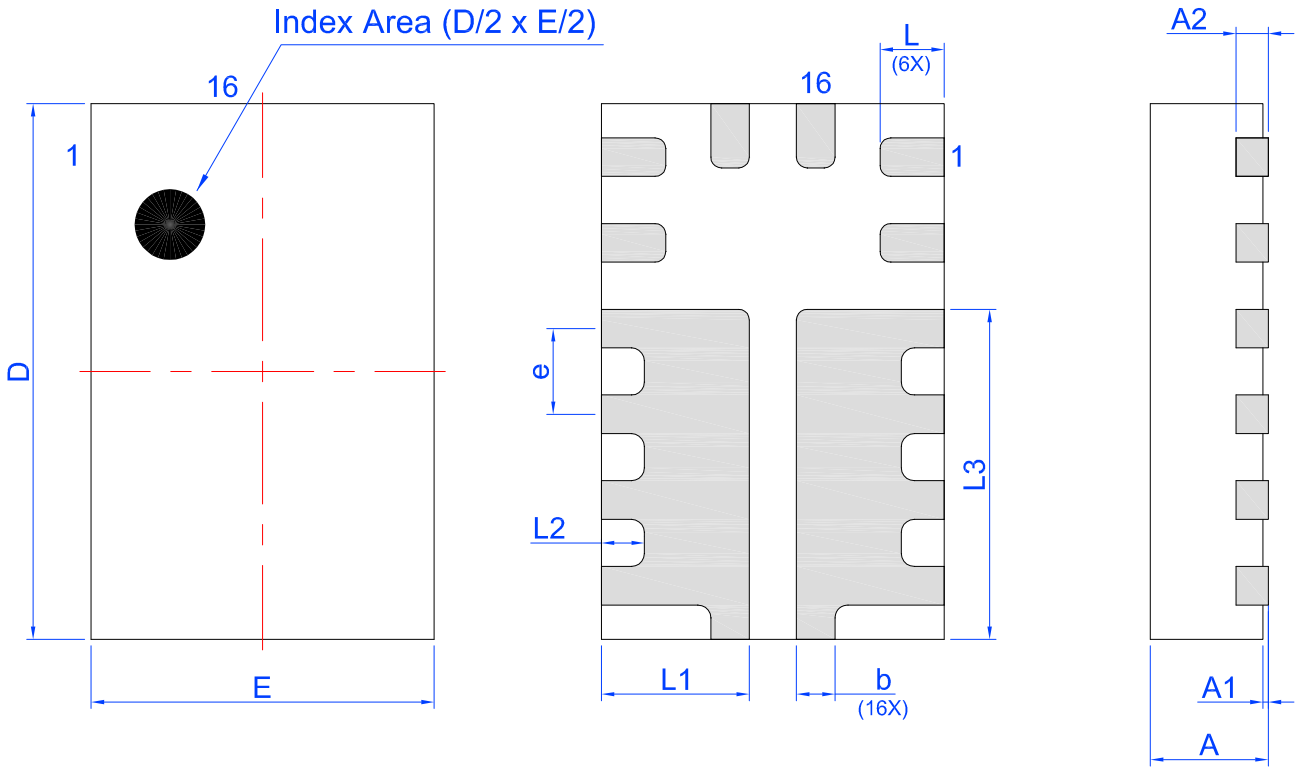


PPPPP - Part ID Field
WW - Date Code Field[1]
NNN - Lot Traceability Code Field[1]
A - Assembly Site Code Field [2]
RR - Part Revision Code Field[2]

Note 1: Each character in code field can be alphanumeric A-Z and 0-9
Note 2: Character in code field can be alphabetic A-Z

Package Drawing and Dimensions

16 Lead STQFN Package 1.6 mm x 2.5 mm (Fused Lead)



Top View BTM View Side View

Unit: mm

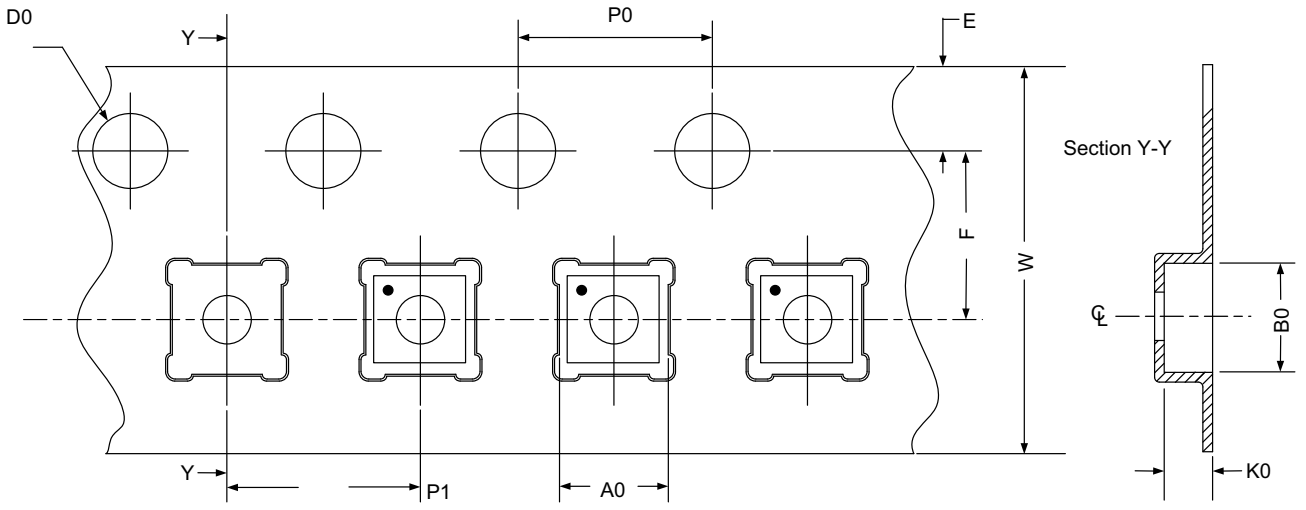
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.45	2.50	2.55
A1	0.005	-	0.05	E	1.55	1.60	1.65
A2	0.10	0.15	0.20	L	0.25	0.30	0.35
b	0.13	0.18	0.23	L1	0.64	0.69	0.74
e	0.40 BSC			L2	0.15	0.20	0.25
				L3	1.49	1.54	1.59

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 16L 1.6x2.5mm 0.4P FCA Green	16	1.6x2.5x 0.55mm	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 16L 1.6x2.5mm 0.4P FCA Green	1.8	2.8	0.7	4	4	1.55	1.75	3.5	8



Refer to EIA-481 specification

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.2 mm^3 (nominal). More information can be found at www.jedec.org.

Revision History

Date	Version	Change
2/23/2017	1.00	Production Release

Mouser Electronics

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Dialog Semiconductor:

SLG59M1707V