

@ 2018 Dialog Semiconductor

## A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch with $V_{IN}$ Lockout Select and MOSFET Current Monitor Output

### Pin Description

Pin #	Pin Name	Type	Pin Description
1	ON	Input	A low-to-high transition on this pin initiates the operation of the SLG59H1020V's state machine. ON is an asserted HIGH, level-sensitive CMOS input with $ON\_V_{IL} < 0.3\text{ V}$ and $ON\_V_{IH} > 0.9\text{ V}$ . As the ON pin input circuit does not have an internal pull-down resistor, connect this pin to a general-purpose output (GPO) of a microcontroller, an application processor, or a system controller – do not allow this pin to be open-circuited.
2	SEL0	Input	As level-sensitive, CMOS inputs with $V_{IL} < 0.3\text{ V}$ and $V_{IH} > 1.65\text{ V}$ , the SEL0 (LSB) and the SEL1 (MSB) pins select one of four $V_{IN}$ overvoltage lockout thresholds. Please see the Applications Section for additional information and the Electrical Characteristics table for the $V_{IN}$ overvoltage thresholds. A logic LOW on either pin is achieved by connecting the pin of interest to GND; a logic HIGH on either pin is achieved by connecting a 10 kΩ external resistor from the pin in question to the system's local logic supply.
3	GND	GND	Pin 3 is the main ground connection for the SLG59H1020V's internal charge pump, its gate driver and current-limit circuits as well as its internal state machine. Therefore, use a short, stout connection from Pin 3 to the system's analog or power plane.
4-8	VIN	MOSFET	VIN supplies the power for the operation of the SLG59H1020V, its internal control circuitry, and the drain terminal of the back-to-back, reverse-blocking nFET power switch. With 5 pins fused together at VIN, connect a 47 μF (or larger) low-ESR capacitor from this pin to ground. Capacitors used at VIN should be rated at 50 V or higher.
9-13	VOUT	MOSFET	Drain terminal of n-channel MOSFET (5 pins fused for VOUT). Connect a 22 μF (or larger) low-ESR capacitor from this pin to ground. Capacitors used at VOUT should be rated at 50 V or higher.
14	SEL1	Input	Please see SEL0 Pin Description above
15	$\overline{\text{FAULT}}$	Output	An open drain output, $\overline{\text{FAULT}}$ is asserted within $T_{\text{FAULT\_LOW}}$ when a $V_{IN}$ overvoltage, a current-limit, or an over-temperature condition is detected. $\overline{\text{FAULT}}$ is deasserted within $T_{\text{FAULT\_HIGH}}$ when the fault condition is removed. Connect an 100 kΩ external resistor from the $\overline{\text{FAULT}}$ pin to local system logic supply.
16	CAP	Output	A low-ESR, stable dielectric, ceramic surface-mount capacitor connected from CAP pin to GND sets the $V_{OUT}$ slew rate and overall turn-on time of the SLG59H1020V. For best performance, the range for $C_{\text{SLEW}}$ values are $10\text{ nF} \leq C_{\text{SLEW}} \leq 20\text{ nF}$ – please see typical characteristics for additional information. Capacitors used at the CAP pin should be rated at 10 V or higher. Please consult Applications Section on how to select $C_{\text{SLEW}}$ based on $V_{OUT}$ slew rate and loading conditions.
17	IOUT	Output	IOUT is the SLG59H1020V's power MOSFET load current monitor output. As an analog current output, this signal when applied to a ground-reference resistor generates a voltage proportional to the current through the n-channel MOSFET. The $I_{OUT}$ transfer characteristic is typically 10 μA/A with a voltage compliance range of $0.5\text{ V} \leq V_{IOUT} \leq 4\text{ V}$ . Optimal $I_{OUT}$ linearity is exhibited for $0.5\text{ A} \leq I_{DS} \leq 3\text{ A}$ . In addition, it is recommended to bypass the IOUT pin to GND with a 0.18 nF capacitor.
18	RSET	Input	A 1%-tolerance, metal-film resistor between 30 kΩ and 91 kΩ sets the SLG59H1020V's active current limit. A 91 kΩ resistor sets the SLG59H1020V's active current limit to 1 A and a 30 kΩ resistor sets the active current limit to 3 A.

### Ordering Information

Part Number	Type	Production Flow
SLG59H1020V	STQFN 18L FC	Industrial, -40 °C to 85 °C

## SLG59H1020V



A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch  
with  $V_{IN}$  Lockout Select and MOSFET Current Monitor Output

Part Number	Type	Production Flow
SLG59H1020VTR	STQFN 18L FC (Tape and Reel)	Industrial, -40 °C to 85 °C

## A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch with $V_{IN}$ Lockout Select and MOSFET Current Monitor Output

### Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
$V_{IN}$ to GND	Power Switch Input Voltage to GND	Continuous	-0.3	--	30	V
		Maximum pulsed $V_{IN}$ , pulse width < 0.1 s	--	--	32	V
$V_{OUT}$ to GND	Power Switch Output Voltage to GND		-0.3	--	$V_{IN}$	V
ON, SEL[1,0], CAP, RSET, IOUT, and FAULT to GND	ON, SEL[1,0], CAP, RSET, IOUT, and FAULT Pin Voltages to GND		-0.3	--	7	V
$T_S$	Storage Temperature		-65	--	150	°C
ESD <sub>HBM</sub>	ESD Protection	Human Body Model	2000	--	--	V
ESD <sub>CDM</sub>	ESD Protection	Charged Device Model	500	--	--	V
MSL	Moisture Sensitivity Level		1			
$\theta_{JA}$	Thermal Resistance	1.6 x 3.0 mm 18L STQFN; Determined with the device mounted onto a 1 in <sup>2</sup> , 1 oz. copper pad of FR-4 material	--	40	--	°C/W
$T_{J,MAX}$	Maximum Junction Temperature		--	150	--	°C
MOSFET $I_{DS,CONT}$	Continuous Current from VIN to VOUT	$T_J < 150$ °C	--	--	3	A
MOSFET $I_{DS,PEAK}$	Peak Current from VIN to VOUT	Maximum pulsed switch current, pulse width < 1 ms	--	--	5	A

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### Electrical Characteristics

4.5 V ≤  $V_{IN}$  ≤ 20 V;  $C_{IN}$  = 47 μF,  $T_A$  = -40 °C to 85 °C, unless otherwise noted. Typical values are at  $T_A$  = 25 °C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
$V_{IN}$	Operating Input Voltage		4.5	--	20	V
$V_{IN(OVLO)}$	$V_{IN}$ Overvoltage Lockout Threshold	$V_{IN} \uparrow$ ; SEL[1,0] = [0,0]	5.5	6.0	6.5	V
		$V_{IN} \uparrow$ ; SEL[1,0] = [0,1]	10.2	10.8	11.4	V
		$V_{IN} \uparrow$ ; SEL[1,0] = [1,0]	16.0	17.0	18.0	V
		$V_{IN} \uparrow$ ; SEL[1,0] = [1,1]	20.5	22.0	23.5	V
$V_{IN(OVLOHYST)}$	$V_{IN}$ Overvoltage Lockout Hysteresis		--	2	--	%
$I_Q$	Quiescent Supply Current	ON = HIGH; $I_{DS}$ = 0 A	--	0.5	0.6	mA
$I_{SHDN}$	OFF Mode Supply Current	ON = LOW; $I_{DS}$ = 0 A	--	1	3	μA
$R_{DS,ON}$	ON Resistance	$T_A$ = 25 °C; $I_{DS}$ = 0.1 A	--	50	52	mΩ
		$T_A$ = 85 °C; $I_{DS}$ = 0.1 A	--	65	70	mΩ
MOSFET $I_{DS}$	Current from VIN to VOUT	Continuous	--	--	3	A
$I_{REVERSE}$	MOSFET Reverse-Leakage Current	$V_{IN}$ = 0 V; $V_{OUT}$ = 20 V; ON = 0 V	--	--	3	μA
$I_{LIMIT}$	Active Current Limit, $I_{ACL}$	$V_{OUT} > 0.5$ V; $R_{SET}$ = 30.1 kΩ	3	3.2	3.4	A
	Short-circuit Current Limit, $I_{SCL}$	$V_{OUT} < 0.5$ V; $V_{IN}$ = 4.5 V; $R_{LOAD}$ = 0.5 Ω	--	0.8	--	A

## A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch with $V_{IN}$ Lockout Select and MOSFET Current Monitor Output

### Electrical Characteristics (continued)

4.5 V  $\leq V_{IN} \leq 20$  V;  $C_{IN} = 47 \mu\text{F}$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ , unless otherwise noted. Typical values are at  $T_A = 25^\circ\text{C}$

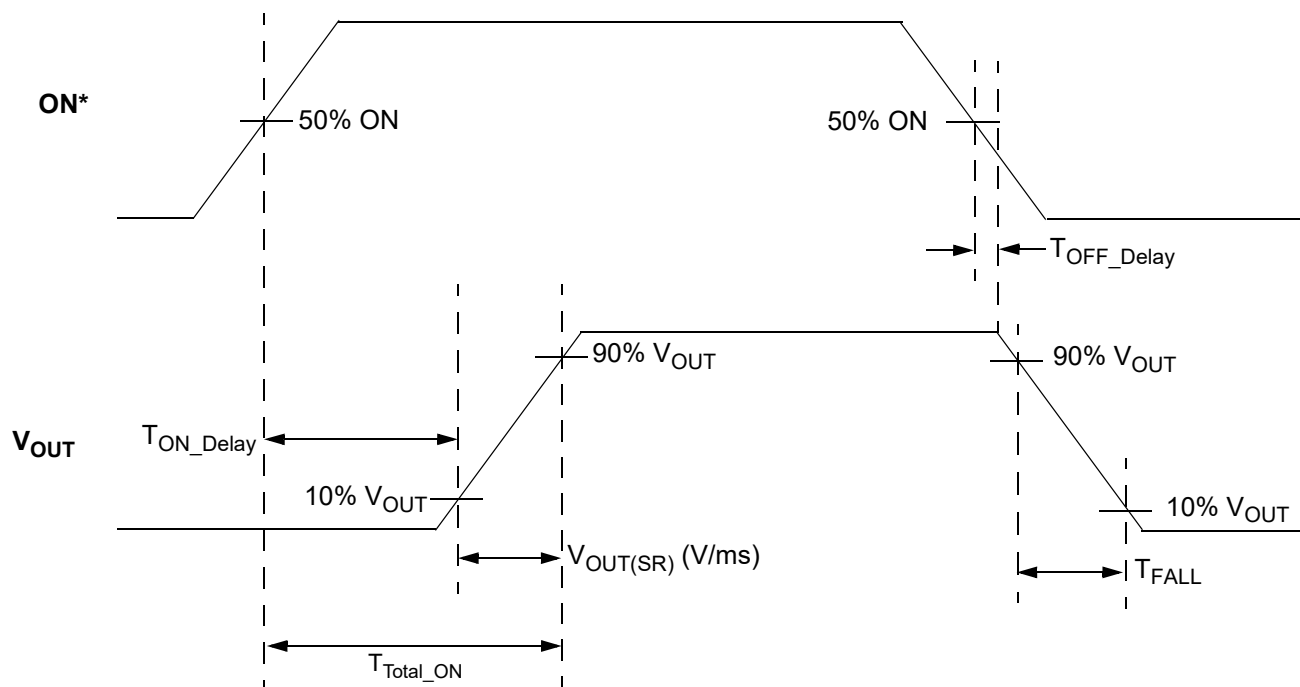
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
$T_{ACL}$	Active Current Limit Response Time	$R_{SET} = 51.6 \text{ k}\Omega$	--	120	--	$\mu\text{s}$
$I_{OUT}$	MOSFET Current Analog Monitor Output	$I_{DS} = 1 \text{ A}$	9.3	10	10.7	$\mu\text{A}$
		$I_{DS} = 3 \text{ A}$	28.5	30	31.5	$\mu\text{A}$
$T_{IOUT}$	$I_{OUT}$ Response Time to Change in Main MOSFET Current	$C_{IOUT} = 180 \text{ pF}$ ; Step load 0 to 2.4 A; 0% to 90% $I_{OUT}$	--	45	--	$\mu\text{s}$
$C_{LOAD}$	Output Load Capacitance	$C_{LOAD}$ connected from $V_{OUT}$ to GND	--	22	--	$\mu\text{F}$
$T_{ON\_Delay}$	ON Delay Time	50% ON to 10% $V_{OUT} \uparrow$ ; $V_{IN} = 4.5 \text{ V}$ ; $C_{SLEW} = 10 \text{ nF}$ ; $R_{LOAD} = 100 \Omega$ , $C_{LOAD} = 10 \mu\text{F}$	--	0.3	0.5	ms
		50% ON to 10% $V_{OUT} \uparrow$ ; $V_{IN} = 20 \text{ V}$ ; $C_{SLEW} = 10 \text{ nF}$ ; $R_{LOAD} = 100 \Omega$ , $C_{LOAD} = 10 \mu\text{F}$	--	0.7	1.2	ms
$T_{Total\_ON}$	Total Turn ON Time	50% ON to 90% $V_{OUT} \uparrow$	Set by External $C_{SLEW}^1$			ms
		50% ON to 90% $V_{OUT} \uparrow$ ; $V_{IN} = 4.5 \text{ V}$ ; $C_{SLEW} = 10 \text{ nF}$ ; $R_{LOAD} = 100 \Omega$ , $C_{LOAD} = 10 \mu\text{F}$	--	1.5	2.1	ms
		50% ON to 90% $V_{OUT} \uparrow$ ; $V_{IN} = 20 \text{ V}$ ; $C_{SLEW} = 10 \text{ nF}$ ; $R_{LOAD} = 100 \Omega$ , $C_{LOAD} = 10 \mu\text{F}$	--	6.5	8	ms
$V_{OUT(SR)}$	$V_{OUT}$ Slew rate	50% ON to 90% $V_{OUT} \uparrow$	Set by External $C_{SLEW}^1$			V/ms
		10% to 90% $V_{OUT} \uparrow$ ; $V_{IN} = 4.5 \text{ V}$ to $20 \text{ V}$ ; $C_{SLEW} = 10 \text{ nF}$ ; $R_{LOAD} = 100 \Omega$ , $C_{LOAD} = 10 \mu\text{F}$	2.7	3.2	3.9	V/ms
$T_{OFF\_Delay}$	OFF Delay Time	50% ON to $V_{OUT}$ Fall Start $\downarrow$ ; $V_{IN} = 4.5 \text{ V}$ to $20 \text{ V}$ ; $R_{LOAD} = 100 \Omega$ , No $C_{LOAD}$	--	15	--	$\mu\text{s}$
$T_{FALL}$	$V_{OUT}$ Fall Time	90% $V_{OUT}$ to 10% $V_{OUT} \downarrow$ ; ON = HIGH-to-LOW; $V_{IN} = 4.5 \text{ V}$ to $20 \text{ V}$ ; $R_{LOAD} = 100 \Omega$ , No $C_{LOAD}$	10.4	12.7	14.3	$\mu\text{s}$
$T_{FAULT\_LOW}$	$\overline{\text{FAULT}}$ Assertion Time	Abnormal Step Load Current event to $\overline{\text{FAULT}} \downarrow$ ; $I_{ACL} = 1 \text{ A}$ ; $V_{IN} = 20 \text{ V}$ ; $R_{SET} = 91 \text{ k}\Omega$ ; switch in $20 \Omega$ load	--	80	--	$\mu\text{s}$
$T_{FAULT\_HIGH}$	$\overline{\text{FAULT}}$ De-assertion Time	Delay to $\overline{\text{FAULT}} \uparrow$ after fault condition is removed; $I_{ACL} = 1 \text{ A}$ ; $V_{IN} = 20 \text{ V}$ ; $R_{SET} = 91 \text{ k}\Omega$ ; switch out $20 \Omega$ load	--	180	--	$\mu\text{s}$
$\overline{\text{FAULT}}_{VOL}$	$\overline{\text{FAULT}}$ Output Low Voltage	$I_{FAULT} = 1 \text{ mA}$	--	0.2	--	V
ON_ $V_{IH}$	ON Pin Input High Voltage		0.9	--	5	V
ON_ $V_{IL}$	ON Pin Input Low Voltage		-0.3	0	0.3	V
SEL[1,0]_ $V_{IH}$	SEL[1,0] pins Input High Voltage		1.65	--	4.5	V
SEL[1,0]_ $V_{IL}$	SEL[1,0] pins Input Low Voltage		-0.3	--	0.3	V
$I_{ON(Leakage)}$	ON Pin Leakage Current	1 V $\leq \text{ON} \leq 5 \text{ V}$ or ON = GND	--	--	1	$\mu\text{A}$
THERM <sub>ON</sub>	Thermal Protection Shutdown Threshold		--	125	--	$^\circ\text{C}$
THERM <sub>OFF</sub>	Thermal Protection Restart Threshold		--	100	--	$^\circ\text{C}$

#### Notes:

1. Refer to typical Timing Parameter vs.  $C_{SLEW}$  performance charts for additional information when available.

A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch  
 with  $V_{IN}$  Lockout Select and MOSFET Current Monitor Output

### $T_{Total\_ON}$ , $T_{ON\_Delay}$ and Slew Rate Measurement

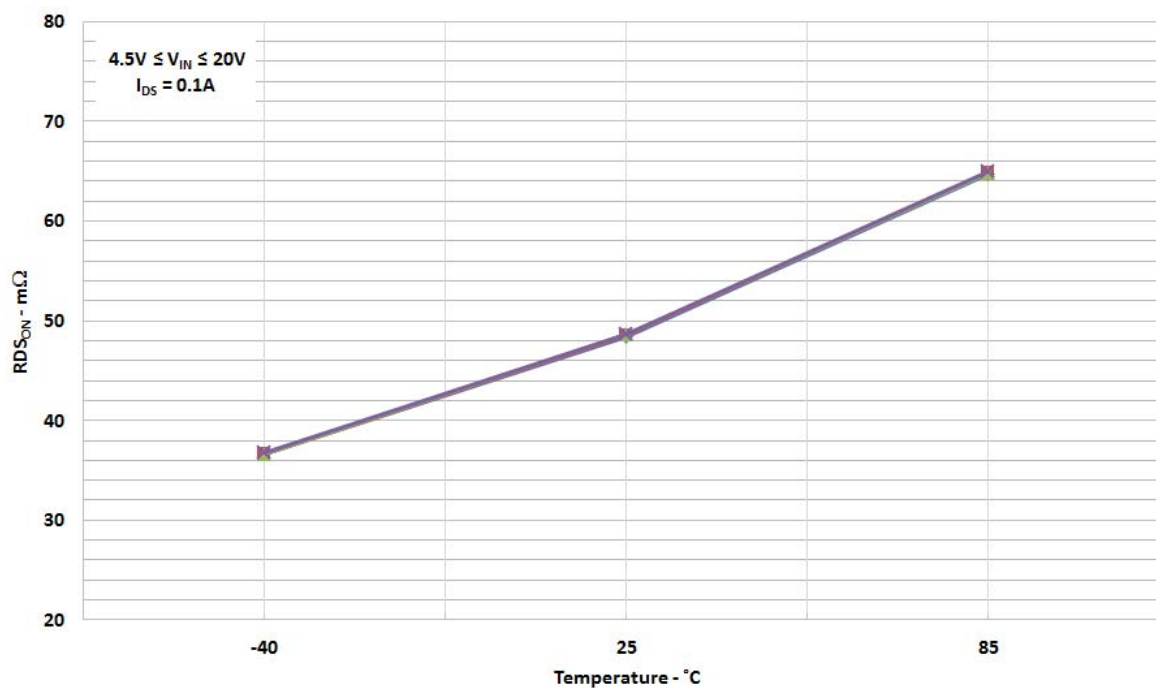


\*Rise and Fall Times of the ON Signal are 100 ns

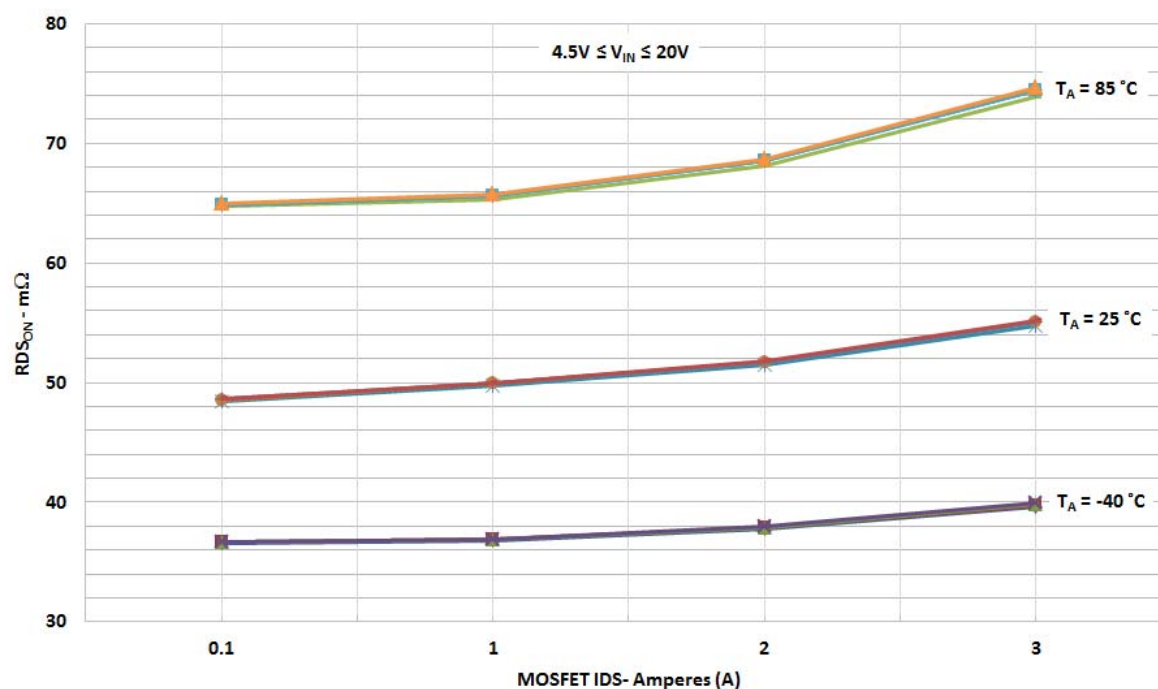
A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch with  $V_{IN}$  Lockout Select and MOSFET Current Monitor Output

## Typical Performance Characteristics

### $R_{DS(ON)}$ vs. Temperature and $V_{IN}$

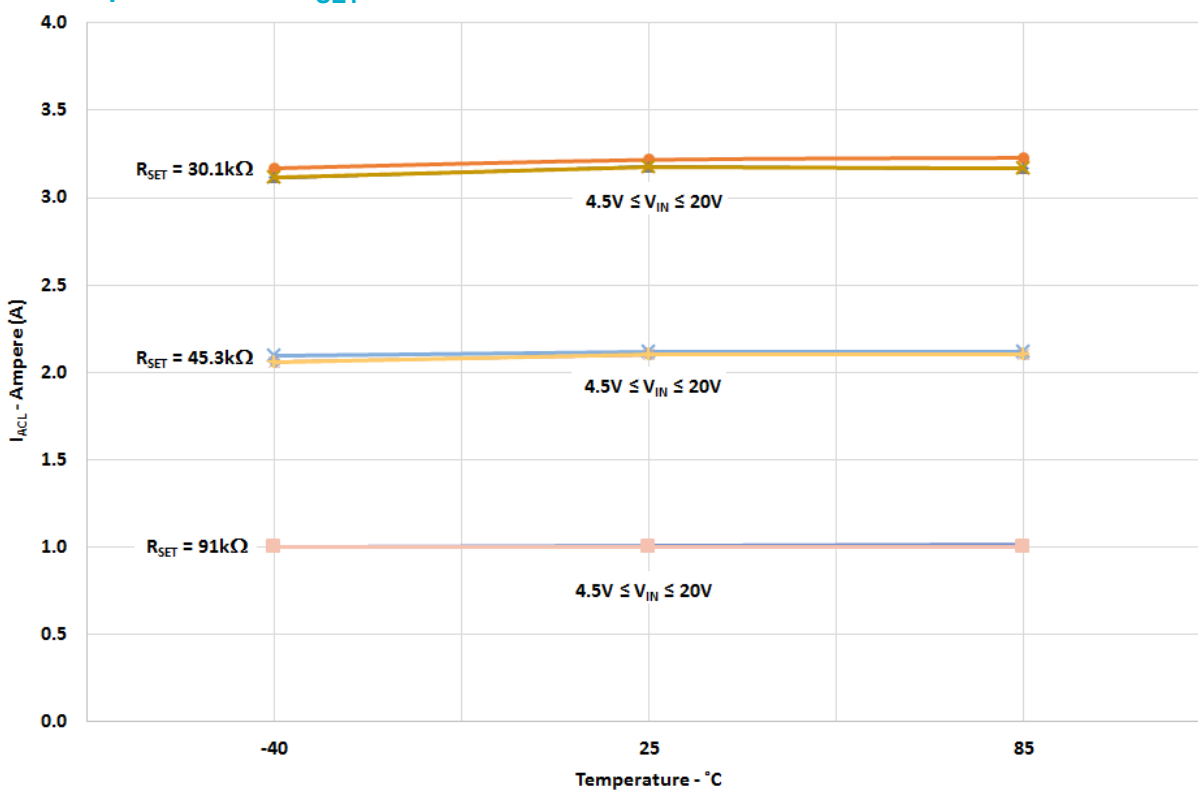


### $R_{DS(ON)}$ vs. MOSFET $I_{DS}$ , $V_{IN}$ , and Temperature

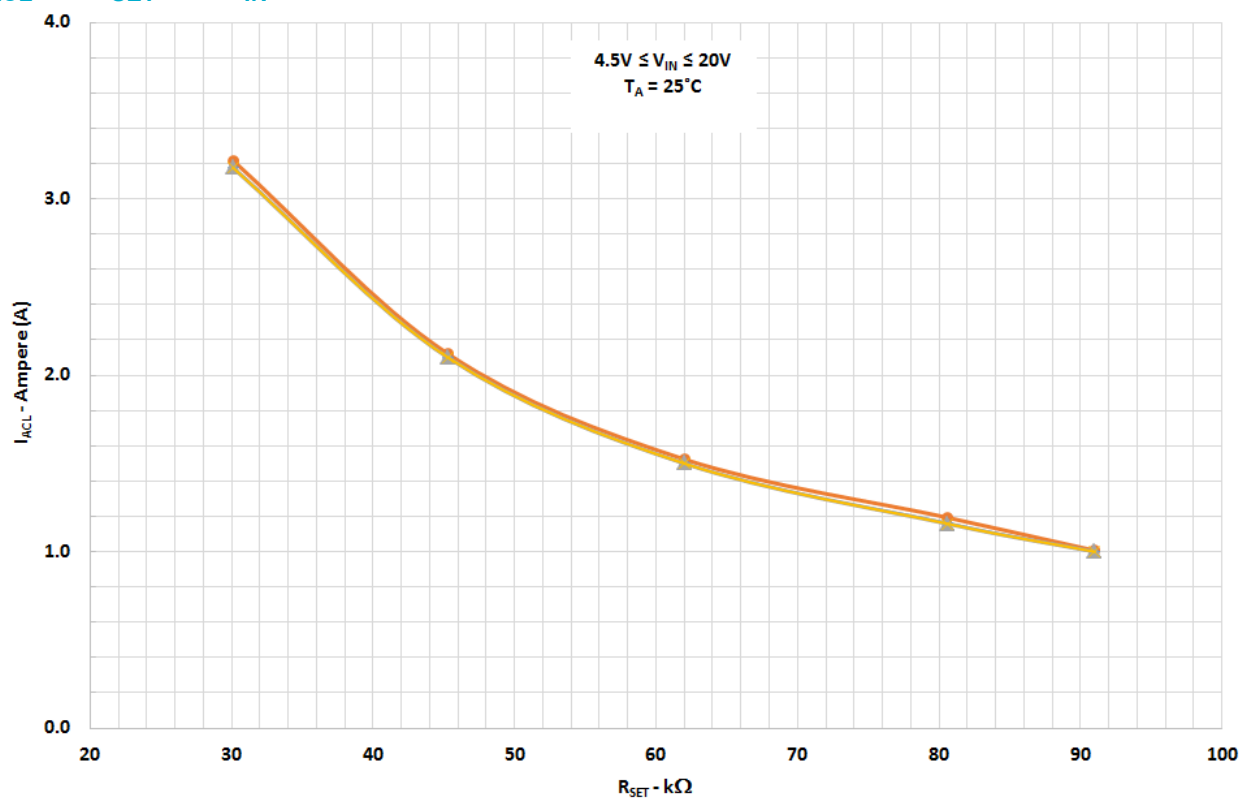


A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch  
with  $V_{IN}$  Lockout Select and MOSFET Current Monitor Output

### $I_{ACL}$ vs. Temperature and $R_{SET}$



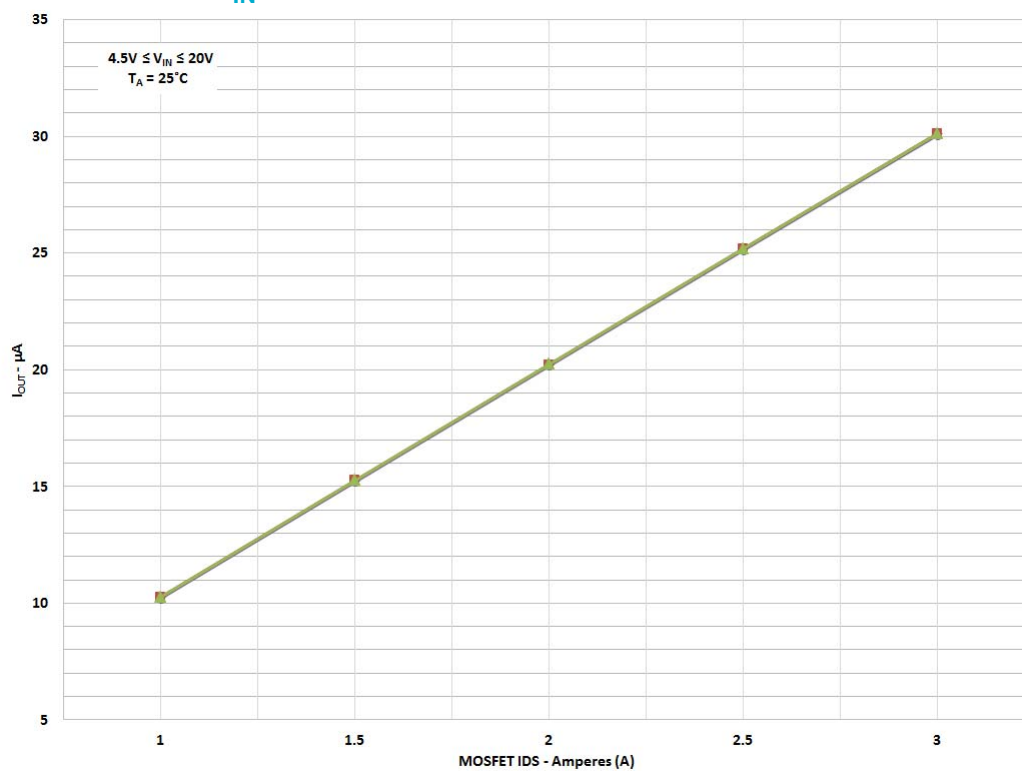
### $I_{ACL}$ vs. $R_{SET}$ and $V_{IN}$



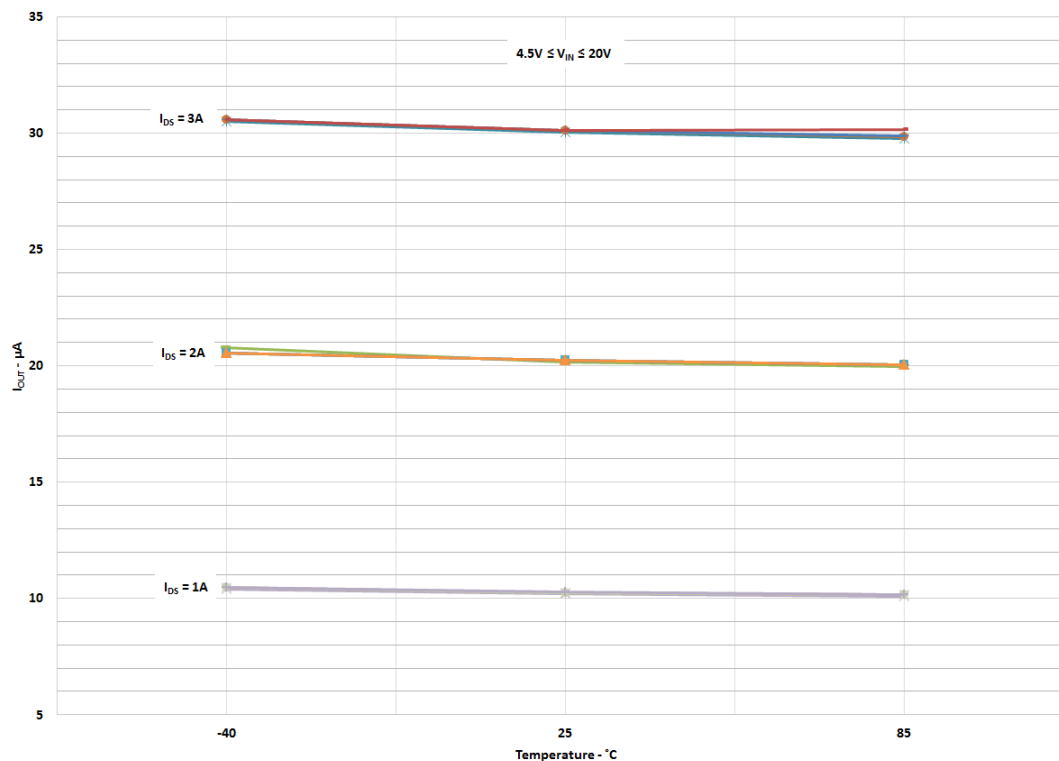


A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch  
 with  $V_{IN}$  Lockout Select and MOSFET Current Monitor Output

### $I_{OUT}$ vs. MOSFET $I_{DS}$ and $V_{IN}$

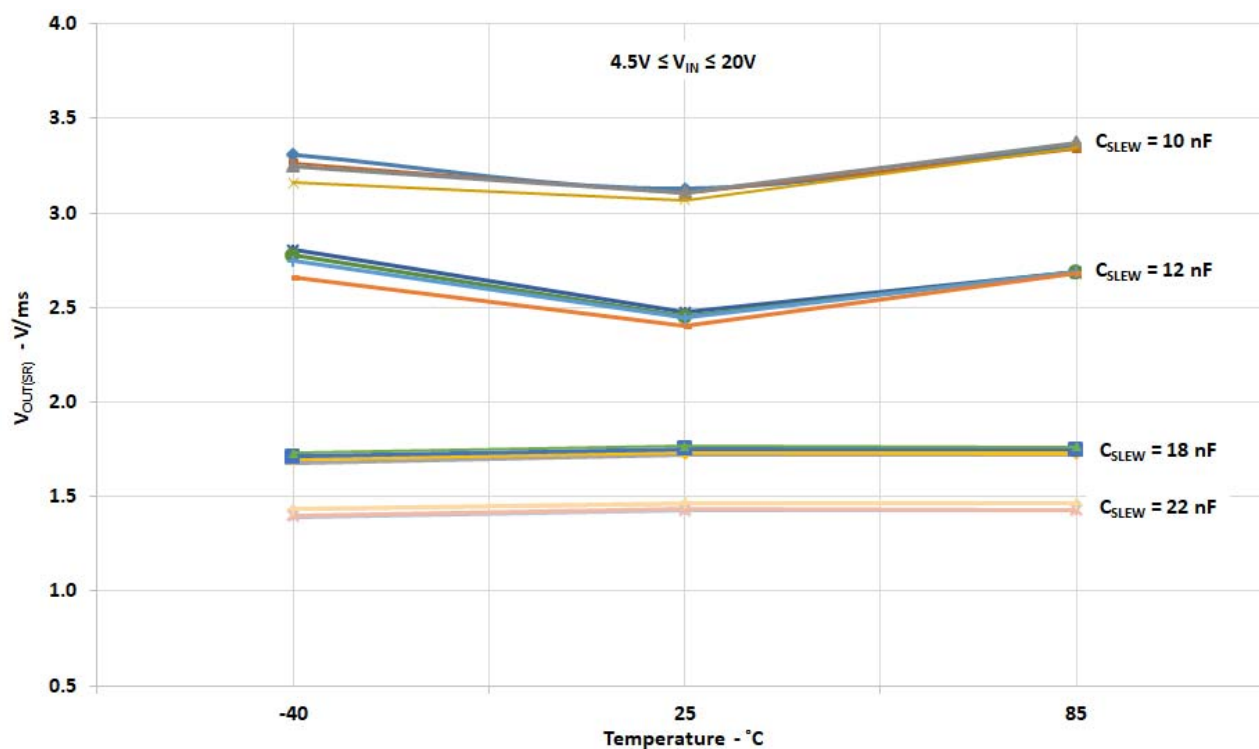


### $I_{OUT}$ vs. Temperature and MOSFET $I_{DS}$

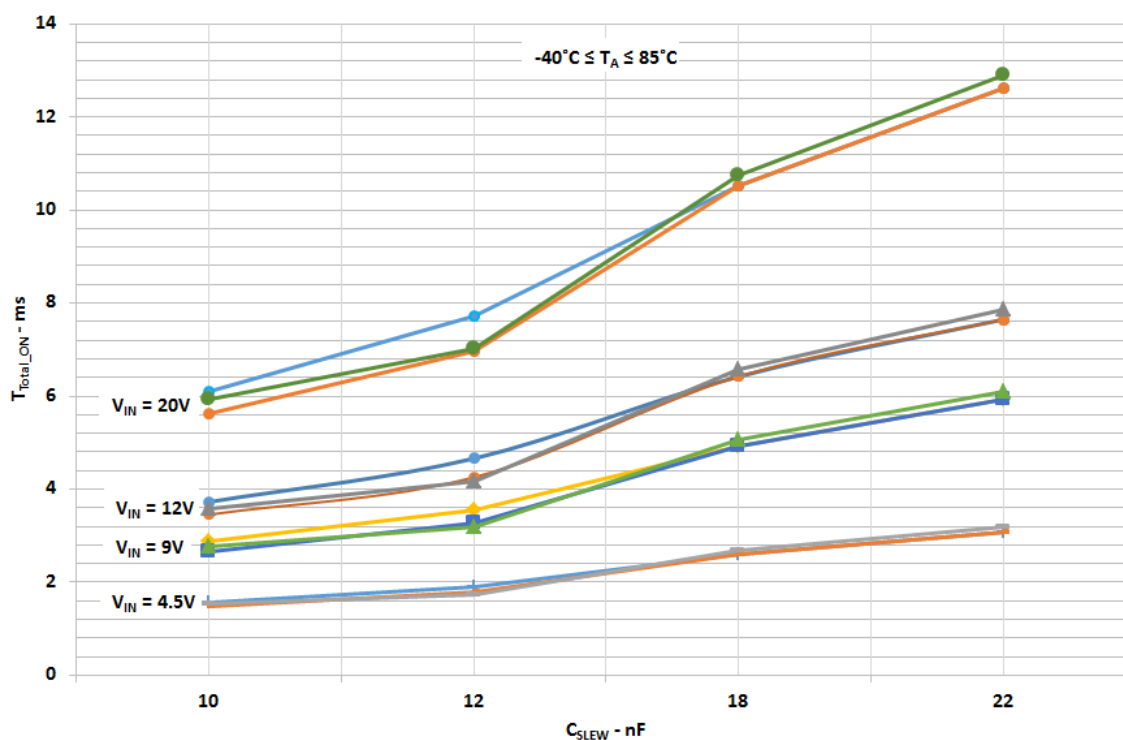


A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch with  $V_{IN}$  Lockout Select and MOSFET Current Monitor Output

### $V_{OUT}$ Slew Rate vs. Temperature, $V_{IN}$ , and $C_{SLEW}$



### $T_{Total\_ON}$ vs. $C_{SLEW}$ , $V_{IN}$ , and Temperature



## SLG59H1020V Application Diagram



ON 1

VOUT 2

Rise=1.085ms Max=4.56V

1 = 2.00 V 2 = 1.00 V

**Figure 2. Typical Turn ON operation waveform for  $V_{IN} = 4.5\text{ V}$ ,  $C_{SLEW} = 10\text{ nF}$ ,  $C_{LOAD} = 10\text{ }\mu\text{F}$ ,  $R_{LOAD} = 100\text{ }\Omega$**

A 20 V, 50 m $\Omega$ , 3 A, Reverse Blocking Integrated Power Switch  
 with  $V_{IN}$  Lockout Select and MOSFET Current Monitor Output

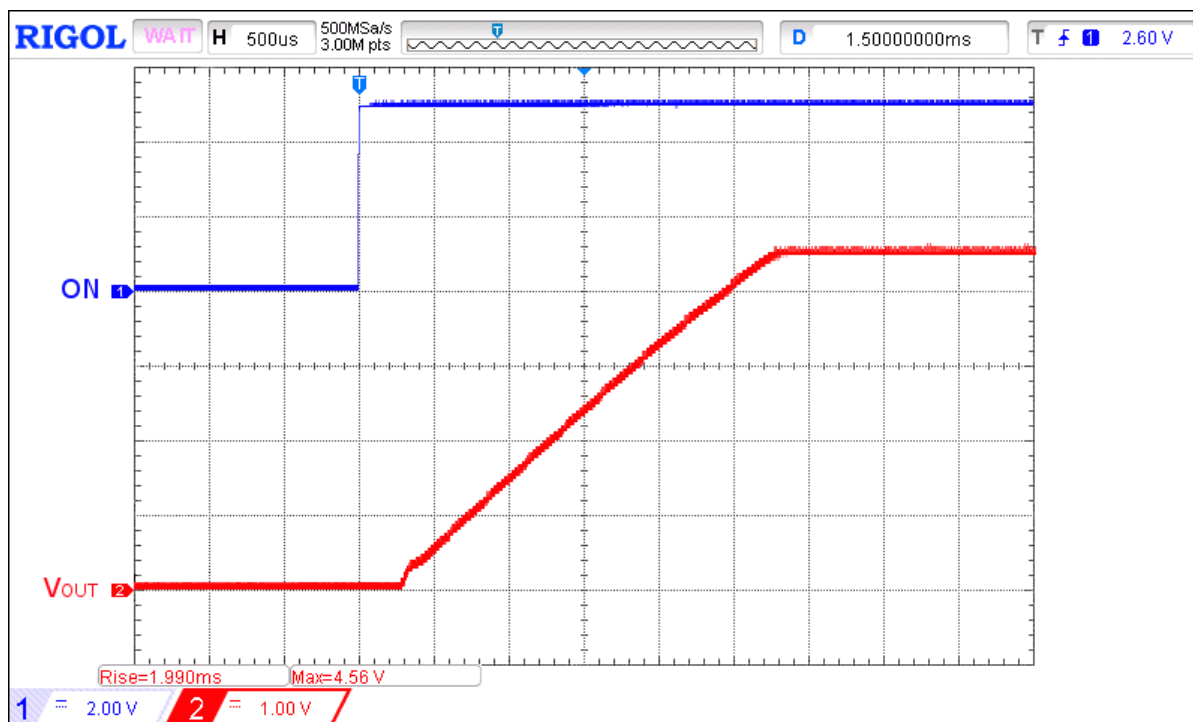


Figure 3. Typical Turn ON operation waveform for  $V_{IN} = 4.5\text{ V}$ ,  $C_{SLEW} = 18\text{ nF}$ ,  $C_{LOAD} = 10\text{ }\mu\text{F}$ ,  $R_{LOAD} = 100\text{ }\Omega$

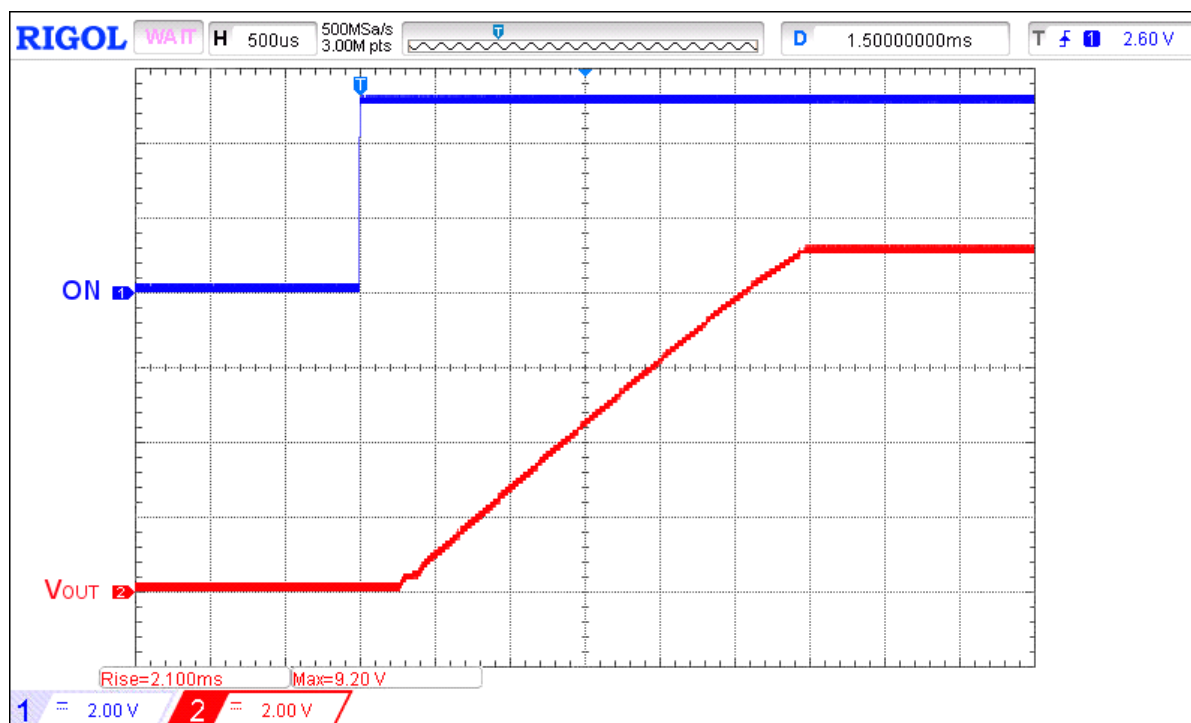


Figure 4. Typical Turn ON operation waveform for  $V_{IN} = 9\text{ V}$ ,  $C_{SLEW} = 10\text{ nF}$ ,  $C_{LOAD} = 10\text{ }\mu\text{F}$ ,  $R_{LOAD} = 100\text{ }\Omega$

A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch  
 with  $V_{IN}$  Lockout Select and MOSFET Current Monitor Output

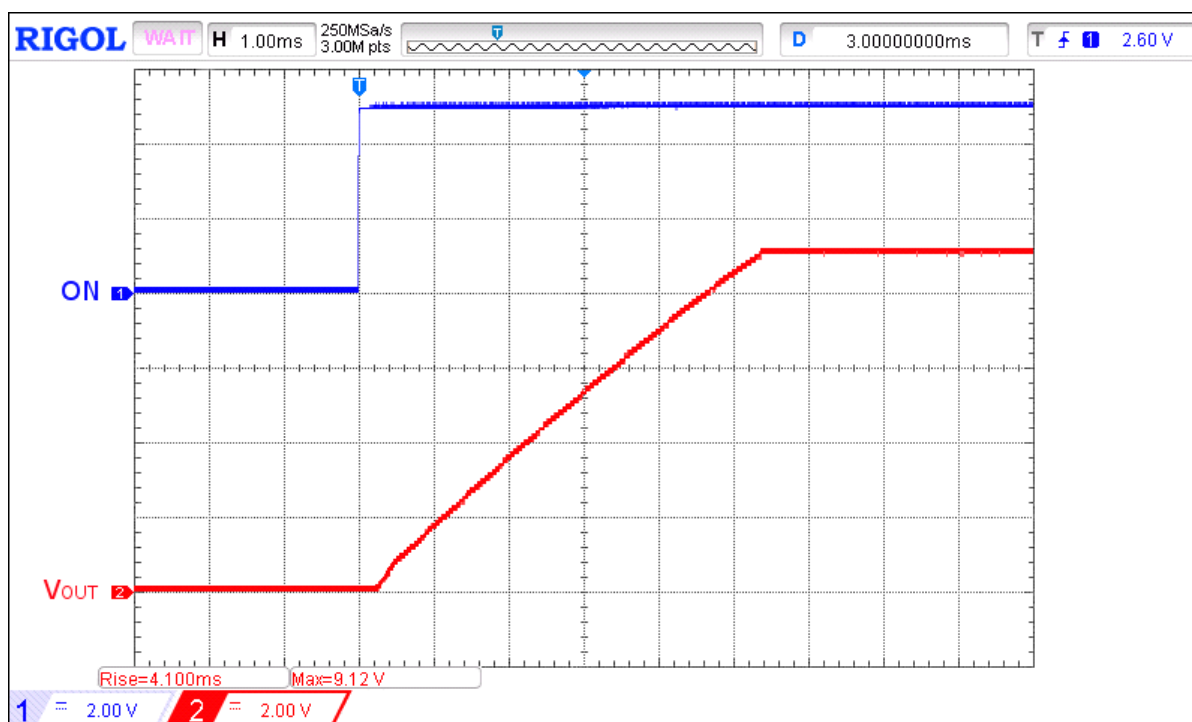


Figure 5. Typical Turn ON operation waveform for  $V_{IN} = 9\text{ V}$ ,  $C_{SLEW} = 18\text{ nF}$ ,  $C_{LOAD} = 10\text{ }\mu\text{F}$ ,  $R_{LOAD} = 100\text{ }\Omega$

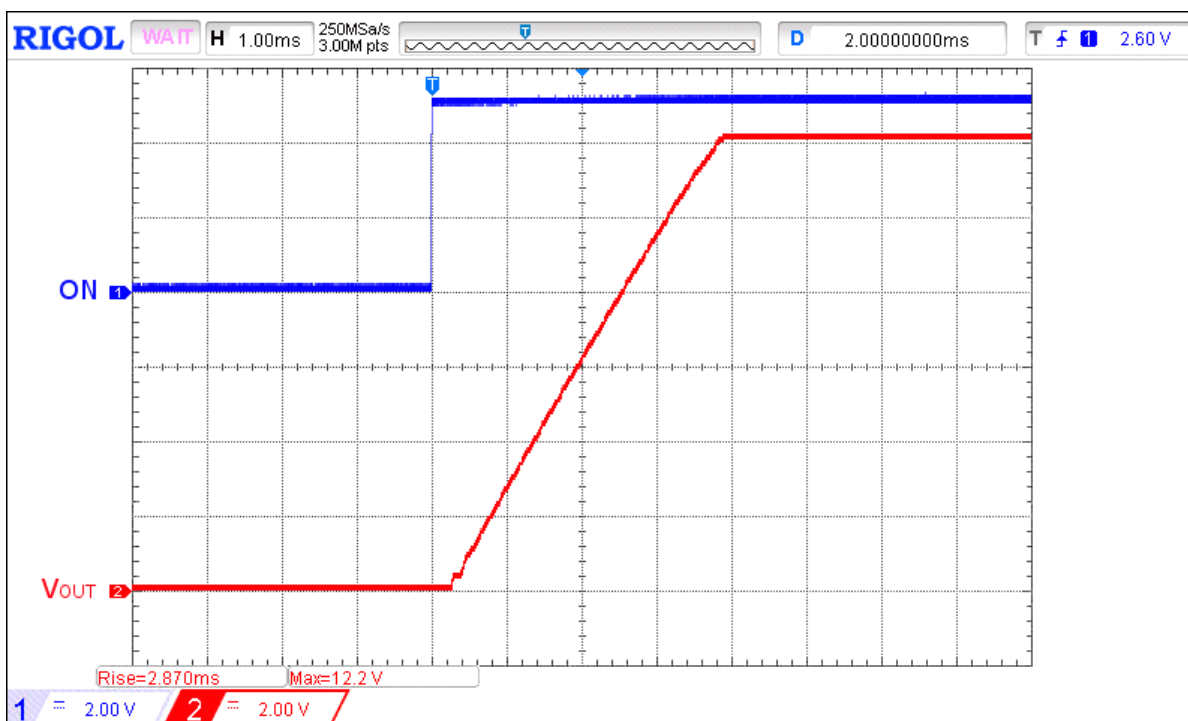


Figure 6. Typical Turn ON operation waveform for  $V_{IN} = 12\text{ V}$ ,  $C_{SLEW} = 10\text{ nF}$ ,  $C_{LOAD} = 10\text{ }\mu\text{F}$ ,  $R_{LOAD} = 100\text{ }\Omega$

A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch  
 with  $V_{IN}$  Lockout Select and MOSFET Current Monitor Output

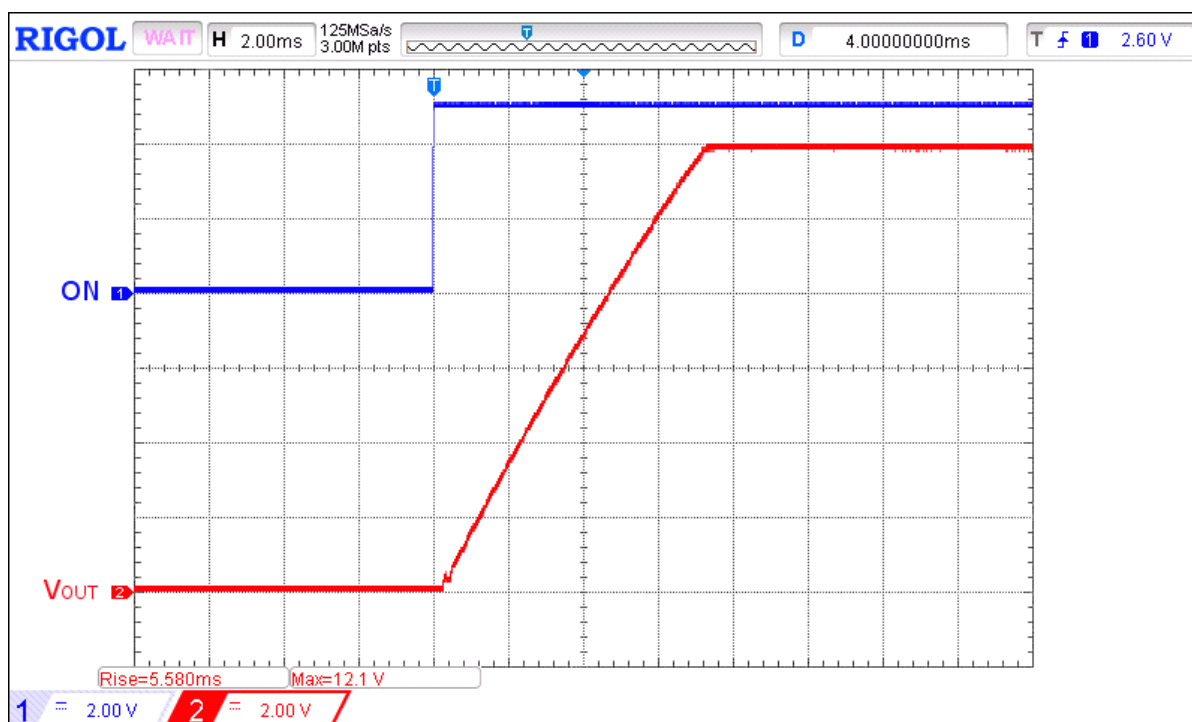


Figure 7. Typical Turn ON operation waveform for  $V_{IN} = 12\text{ V}$ ,  $C_{SLEW} = 18\text{ nF}$ ,  $C_{LOAD} = 10\text{ }\mu\text{F}$ ,  $R_{LOAD} = 100\text{ }\Omega$

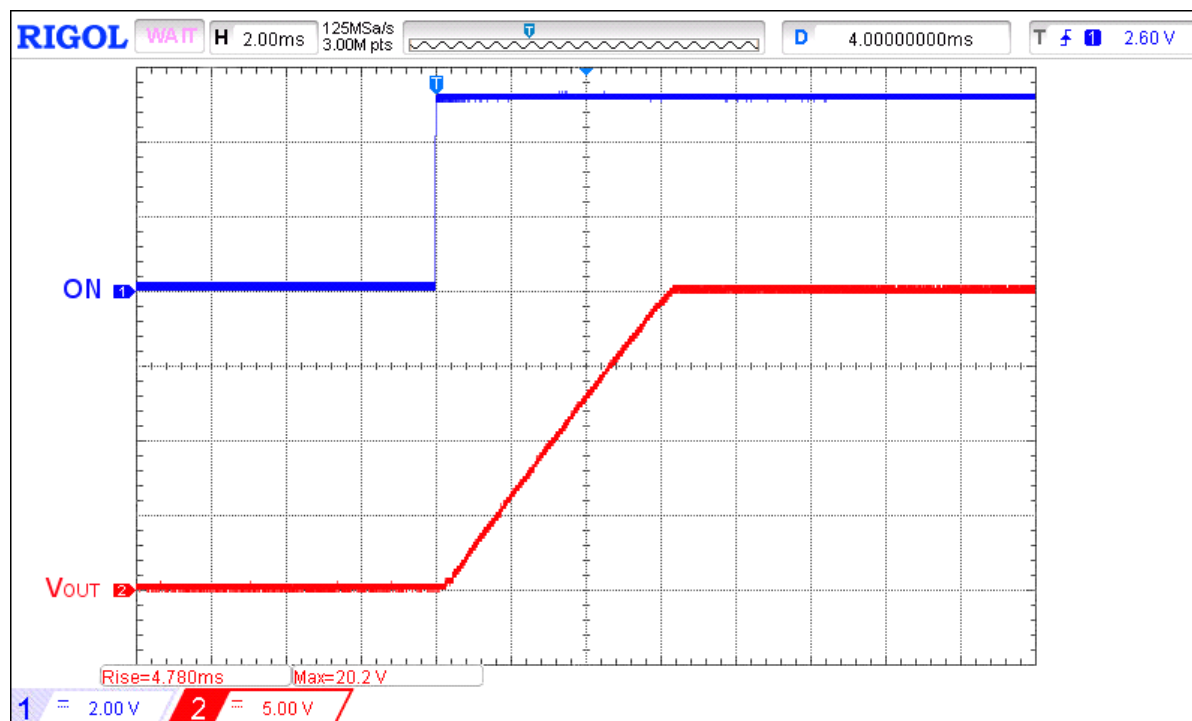


Figure 8. Typical Turn ON operation waveform for  $V_{IN} = 20\text{ V}$ ,  $C_{SLEW} = 10\text{ nF}$ ,  $C_{LOAD} = 10\text{ }\mu\text{F}$ ,  $R_{LOAD} = 100\text{ }\Omega$

A 20 V, 50 m $\Omega$ , 3 A, Reverse Blocking Integrated Power Switch  
 with  $V_{IN}$  Lockout Select and MOSFET Current Monitor Output

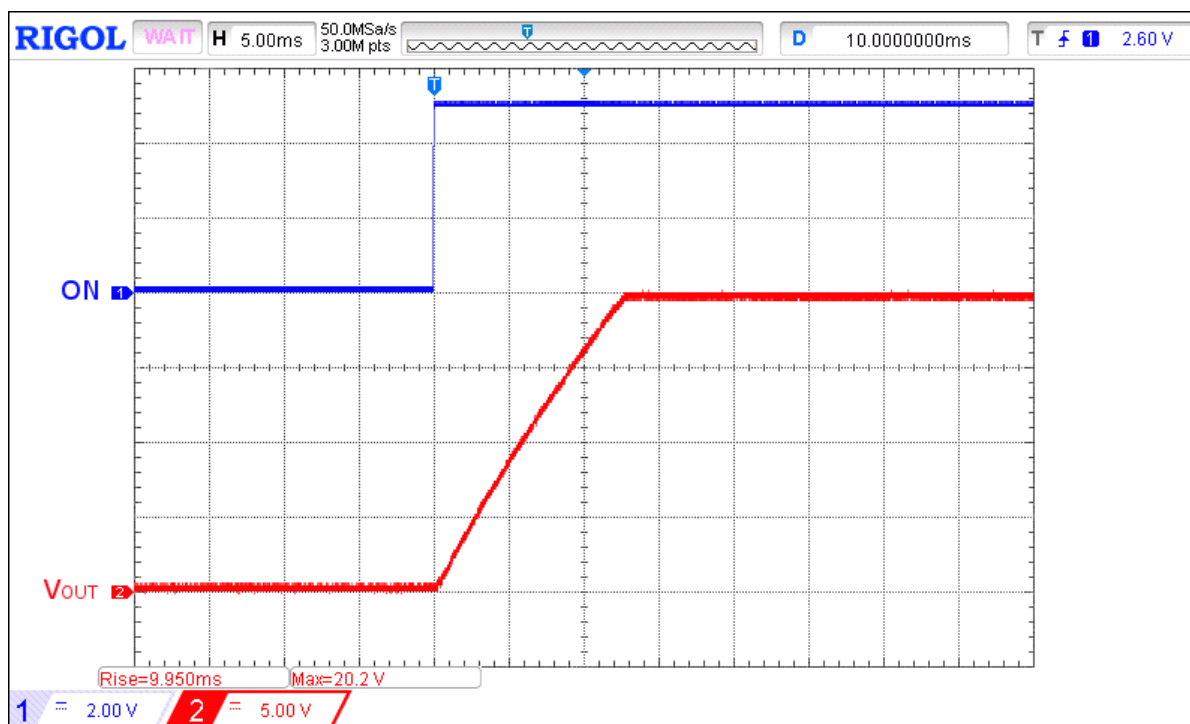


Figure 9. Typical Turn ON operation waveform for  $V_{IN} = 20\text{ V}$ ,  $C_{SLEW} = 18\text{ nF}$ ,  $C_{LOAD} = 10\text{ }\mu\text{F}$ ,  $R_{LOAD} = 100\text{ }\Omega$

A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch  
 with  $V_{IN}$  Lockout Select and MOSFET Current Monitor Output

### Typical Turn-off Waveforms

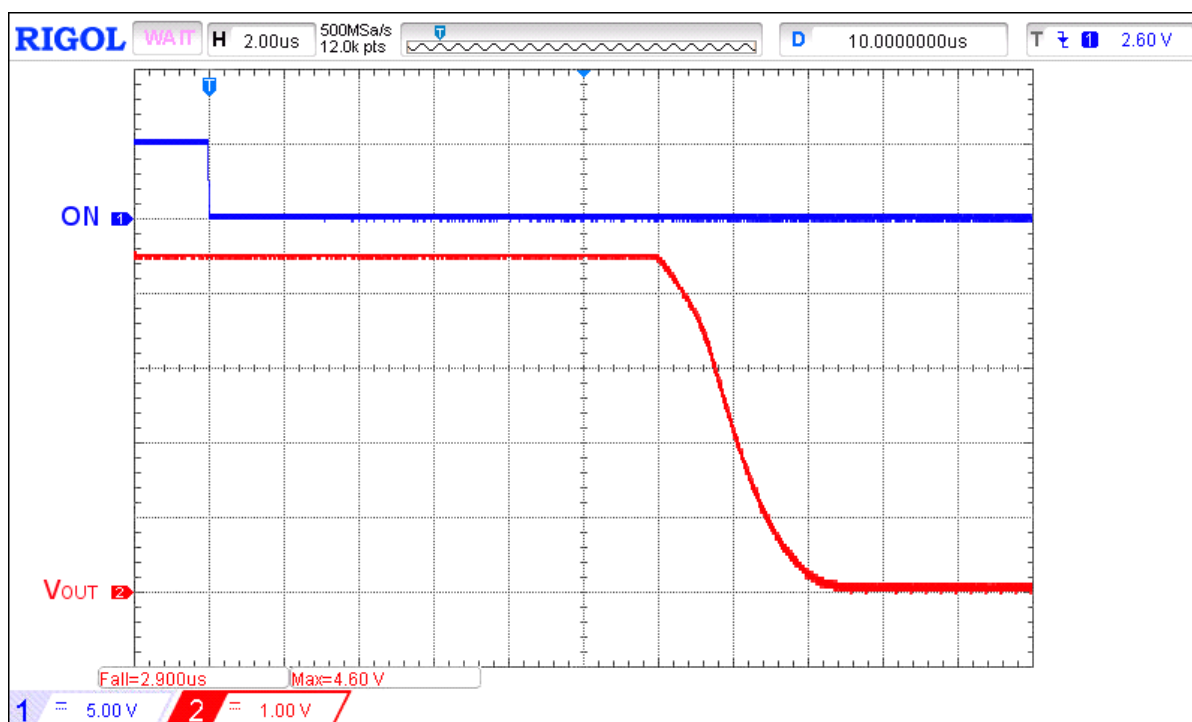


Figure 10. Typical Turn OFF operation waveform for  $V_{IN} = 4.5$  V,  $C_{SLEW} = 10$  nF, no  $C_{LOAD}$ ,  $R_{LOAD} = 100$  Ω

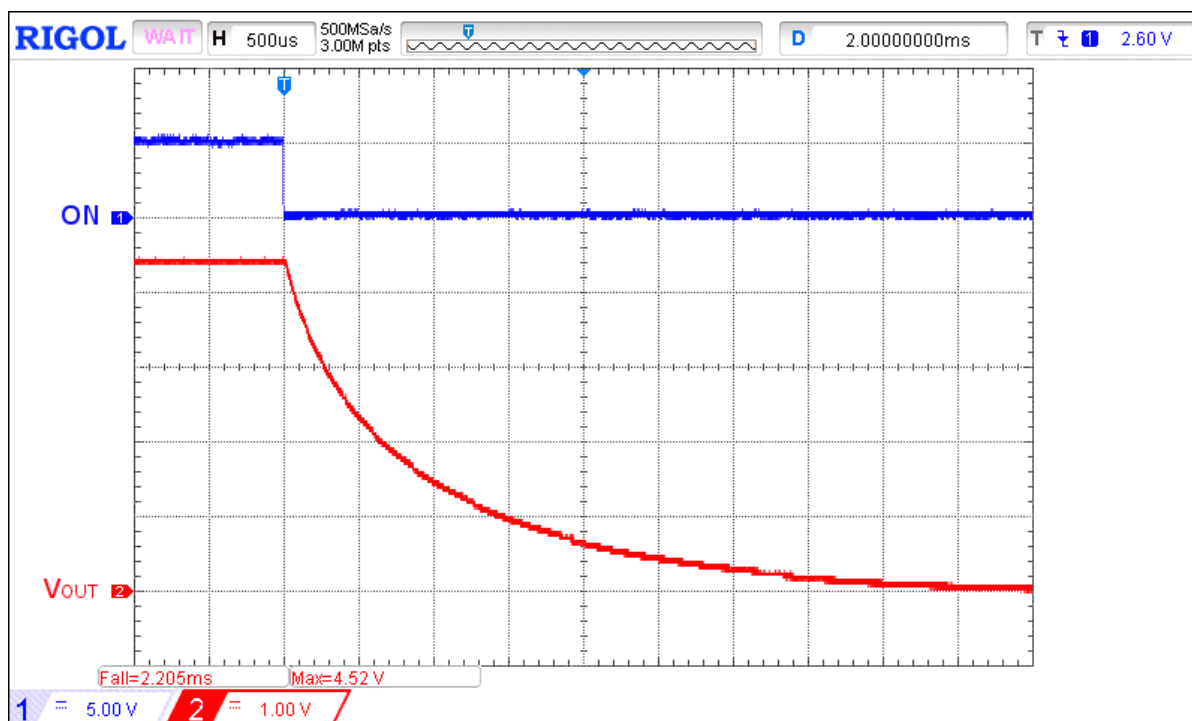


Figure 11. Typical Turn OFF operation waveform for  $V_{IN} = 4.5$  V,  $C_{SLEW} = 10$  nF,  $C_{LOAD} = 10$  μF,  $R_{LOAD} = 100$  Ω



A 20 V, 50 m $\Omega$ , 3 A, Reverse Blocking Integrated Power Switch  
 with  $V_{IN}$  Lockout Select and MOSFET Current Monitor Output

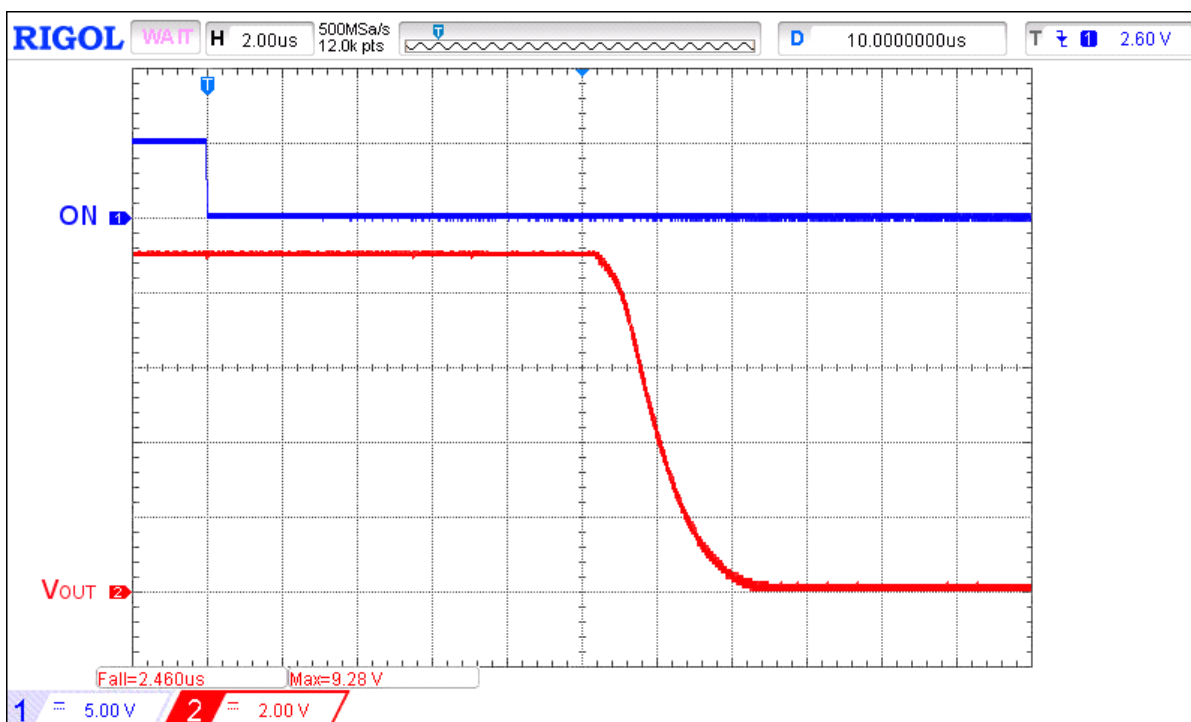


Figure 12. Typical Turn OFF operation waveform for  $V_{IN} = 9\text{ V}$ ,  $C_{SLEW} = 10\text{ nF}$ , no  $C_{LOAD}$ ,  $R_{LOAD} = 100\text{ }\Omega$

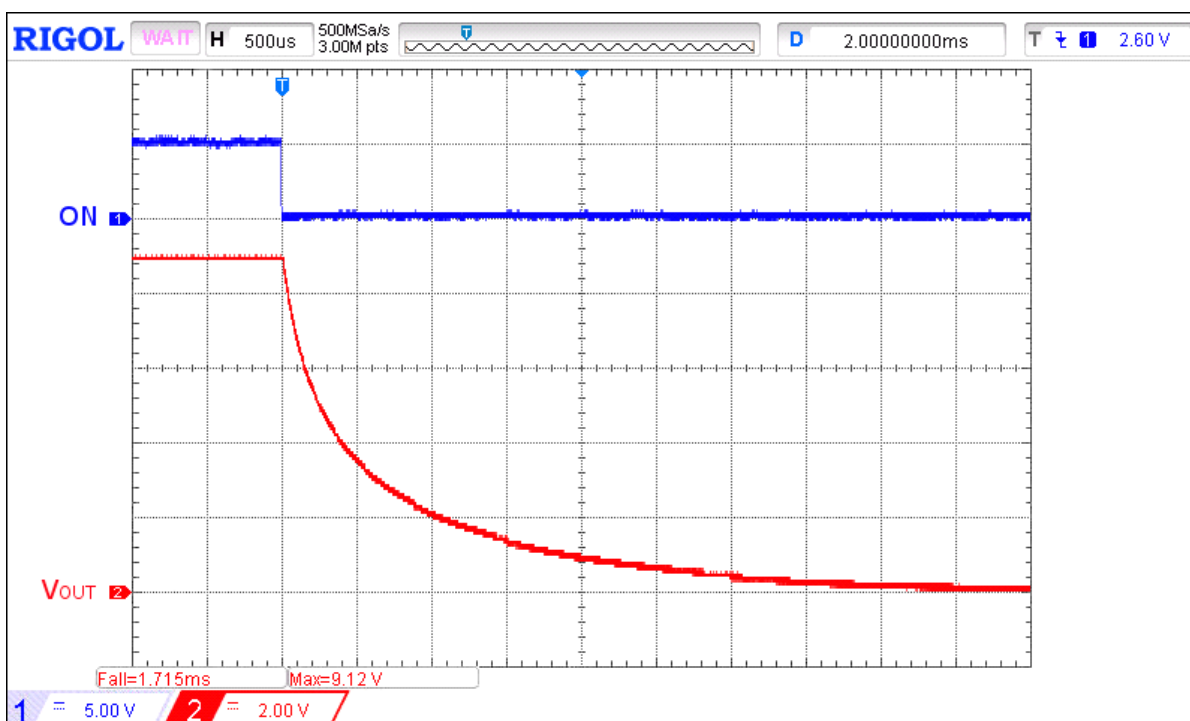


Figure 13. Typical Turn OFF operation waveform for  $V_{IN} = 9\text{ V}$ ,  $C_{SLEW} = 10\text{ nF}$ ,  $C_{LOAD} = 10\text{ }\mu\text{F}$ ,  $R_{LOAD} = 100\text{ }\Omega$

A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch  
 with  $V_{IN}$  Lockout Select and MOSFET Current Monitor Output

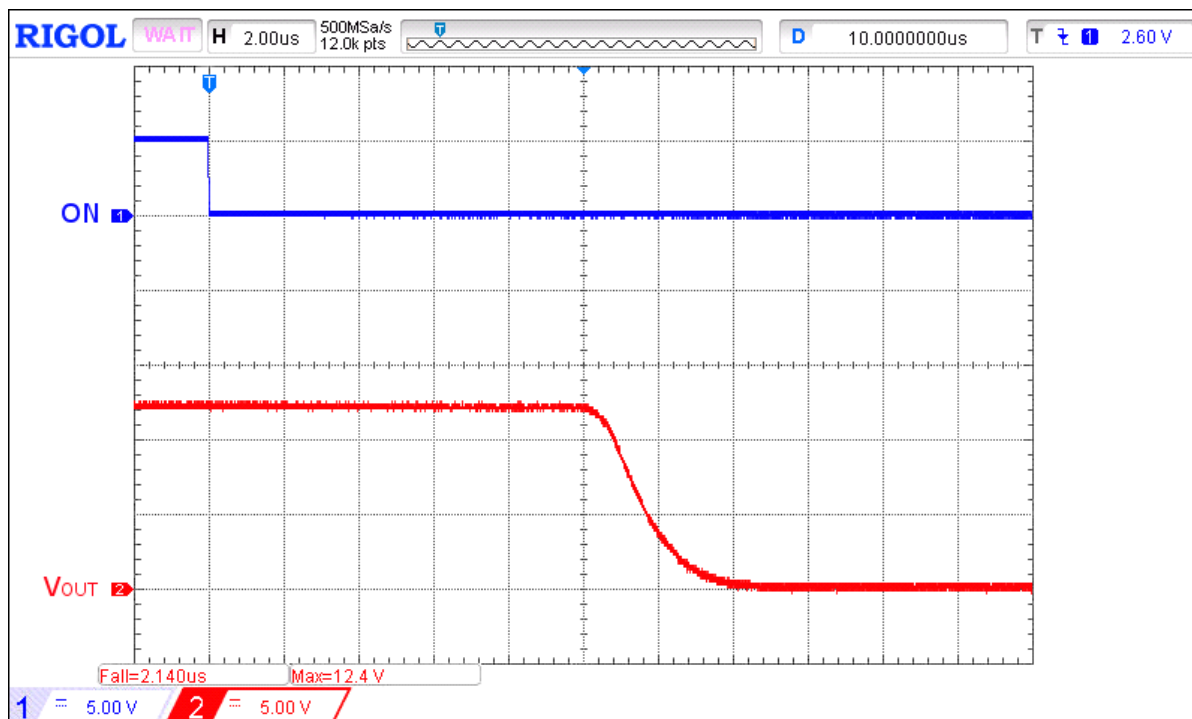


Figure 14. Typical Turn OFF operation waveform for  $V_{IN} = 12\text{ V}$ ,  $C_{SLEW} = 10\text{ nF}$ , no  $C_{LOAD}$ ,  $R_{LOAD} = 100\text{ }\Omega$

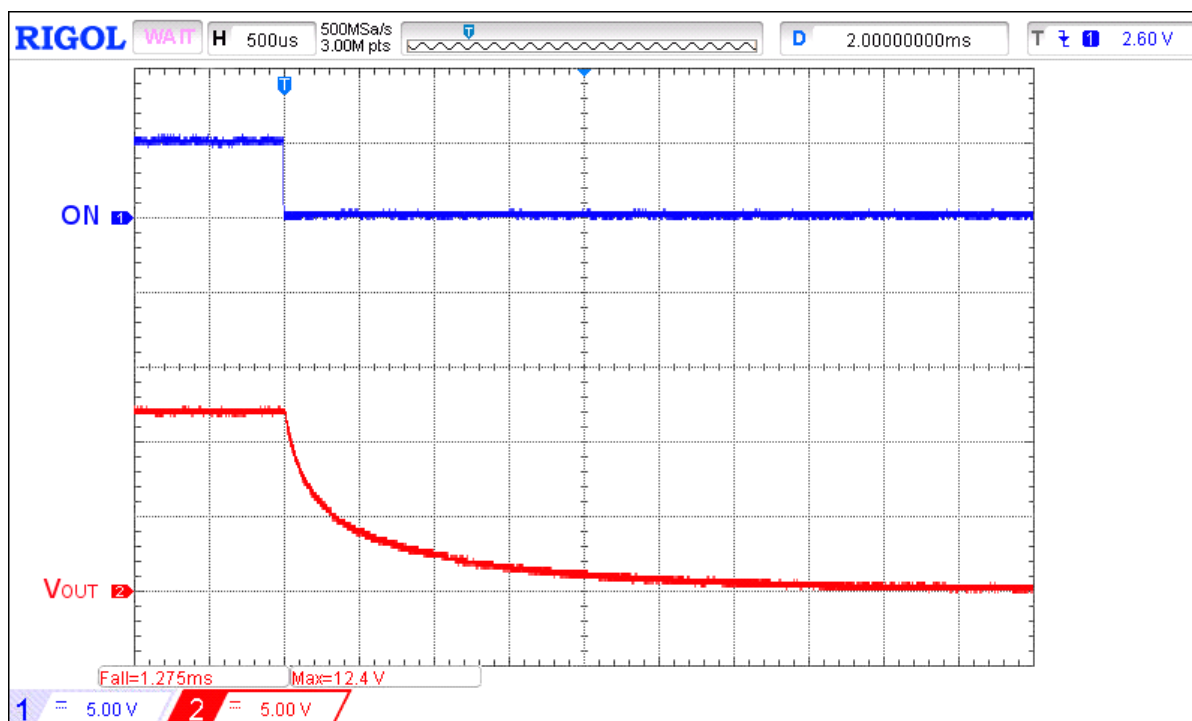


Figure 15. Typical Turn OFF operation waveform for  $V_{IN} = 12\text{ V}$ ,  $C_{SLEW} = 10\text{ nF}$ ,  $C_{LOAD} = 10\text{ }\mu\text{F}$ ,  $R_{LOAD} = 100\text{ }\Omega$

A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch  
 with  $V_{IN}$  Lockout Select and MOSFET Current Monitor Output

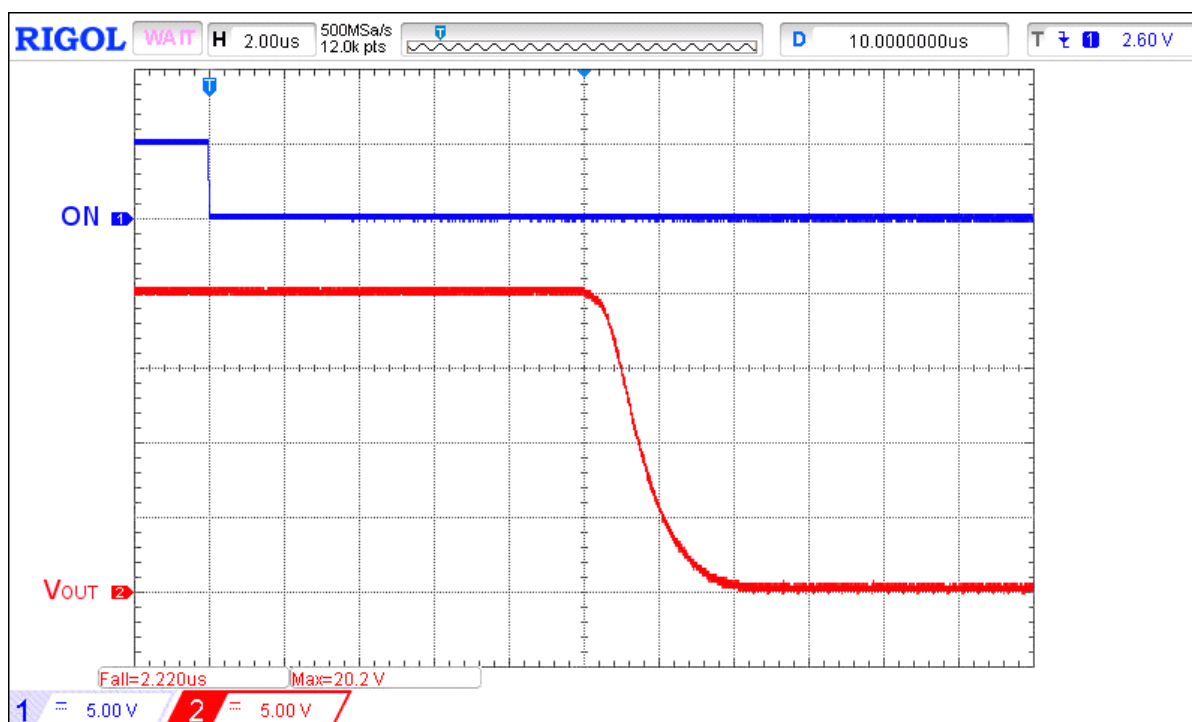


Figure 16. Typical Turn OFF operation waveform for  $V_{IN} = 20\text{ V}$ ,  $C_{SLEW} = 10\text{ nF}$ , no  $C_{LOAD}$ ,  $R_{LOAD} = 100\text{ }\Omega$

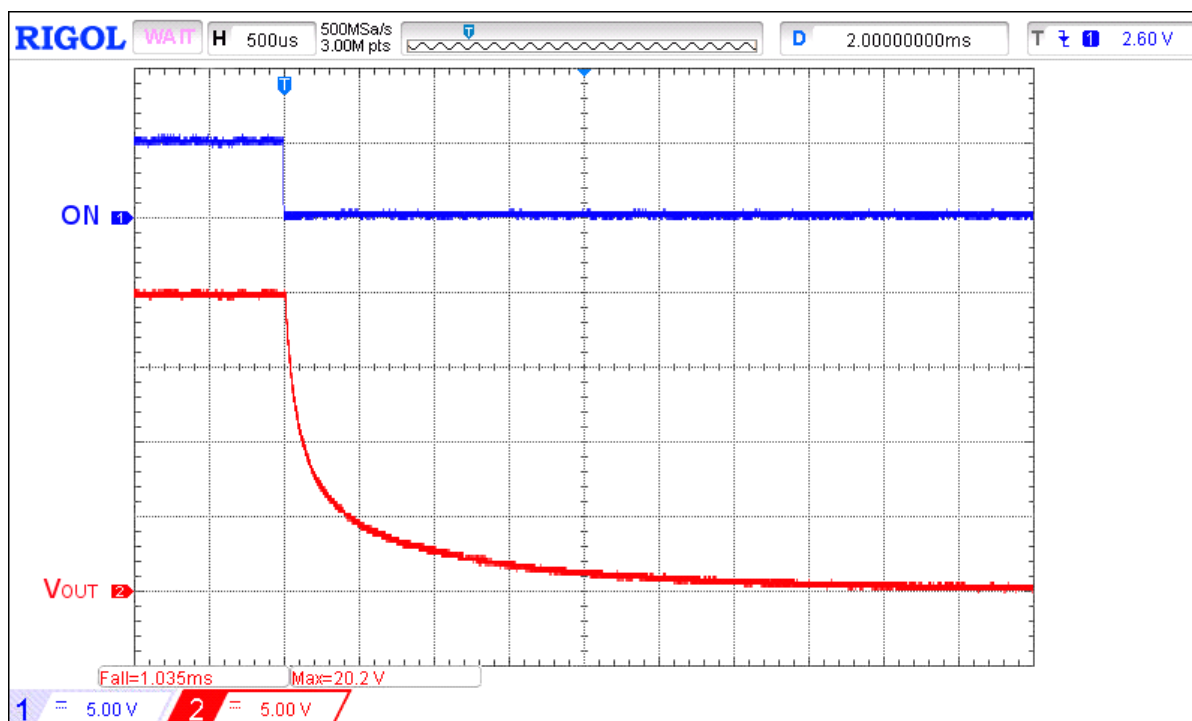


Figure 17. Typical Turn OFF operation waveform for  $V_{IN} = 20\text{ V}$ ,  $C_{SLEW} = 10\text{ nF}$ ,  $C_{LOAD} = 10\text{ }\mu\text{F}$ ,  $R_{LOAD} = 100\text{ }\Omega$

A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch  
 with  $V_{IN}$  Lockout Select and MOSFET Current Monitor Output

### Typical ACL Operation Waveforms

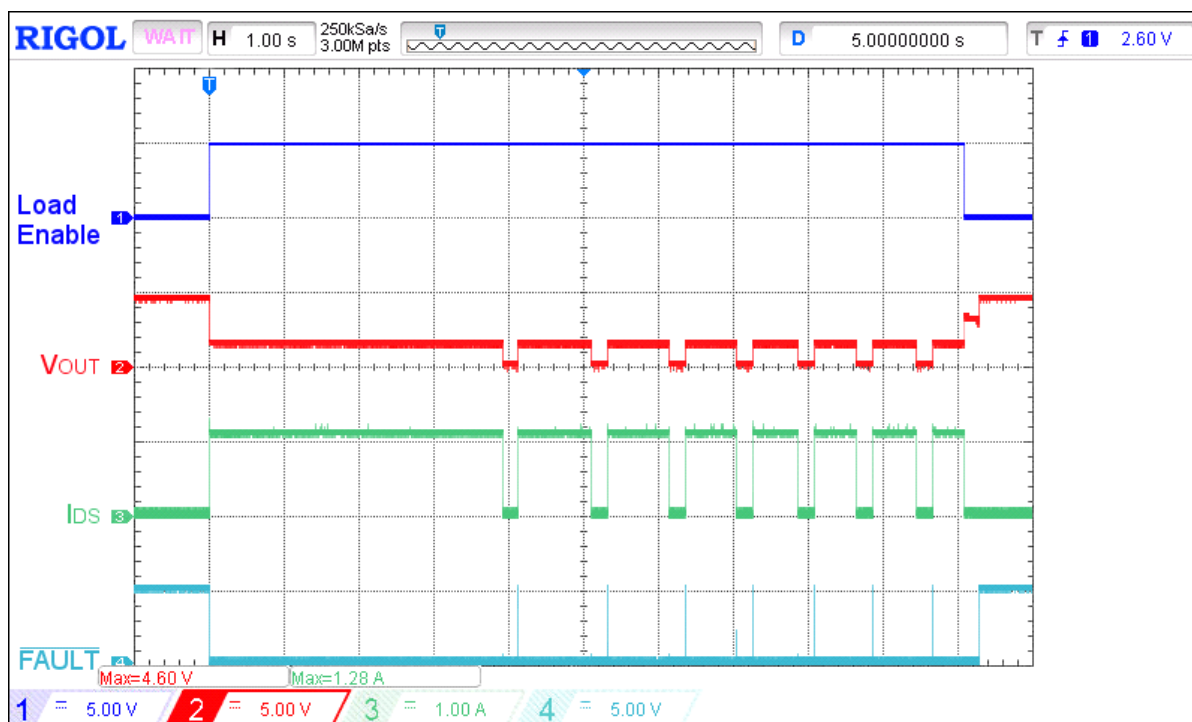


Figure 18. Typical ACL operation waveform for  $V_{IN} = 4.5$  V,  $C_{LOAD} = 10$   $\mu$ F,  $I_{ACL} = 1$  A,  $R_{SET} = 91$  k $\Omega$

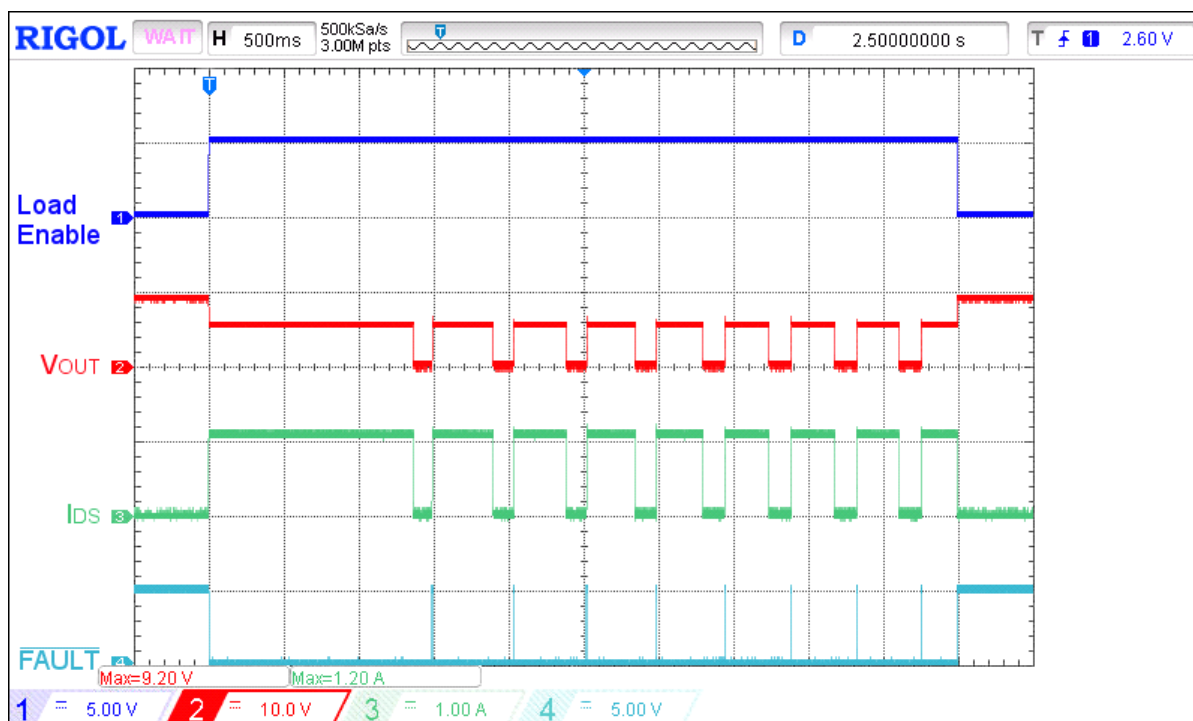


Figure 19. Typical ACL operation waveform for  $V_{IN} = 9$  V,  $C_{LOAD} = 10$   $\mu$ F,  $I_{ACL} = 1$  A,  $R_{SET} = 91$  k $\Omega$

A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch  
 with  $V_{IN}$  Lockout Select and MOSFET Current Monitor Output

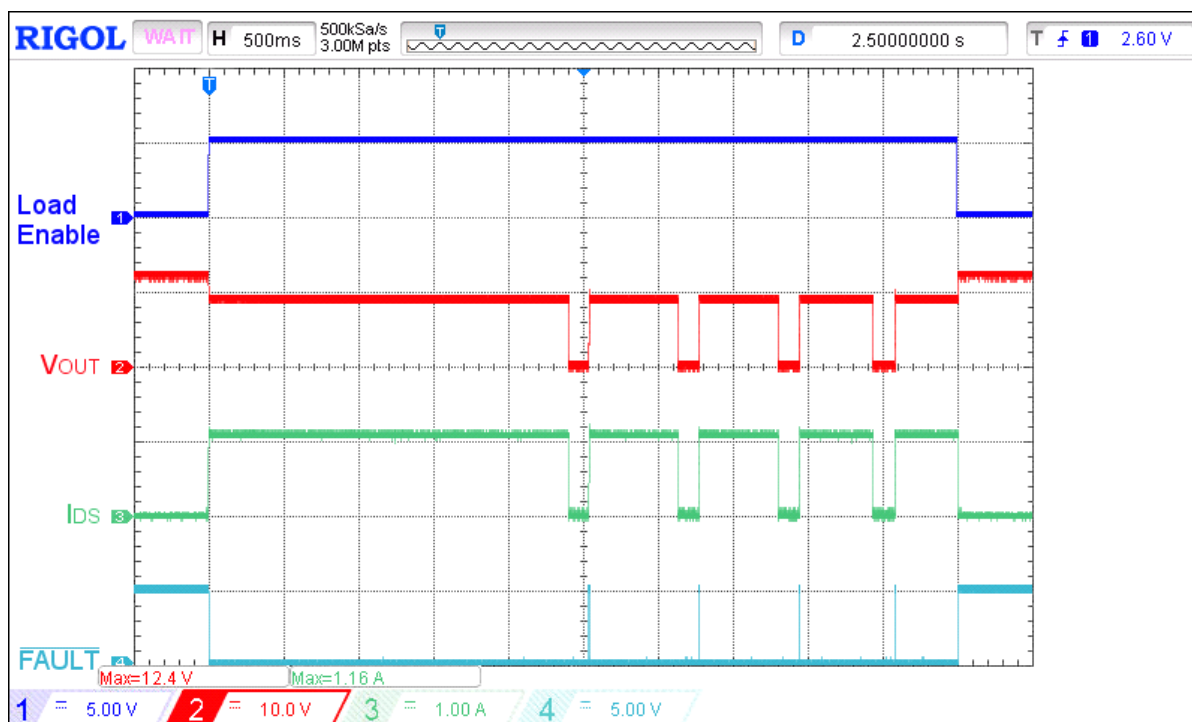


Figure 20. Typical ACL operation waveform for  $V_{IN} = 12\text{ V}$ ,  $C_{LOAD} = 10\text{ }\mu\text{F}$ ,  $I_{ACL} = 1\text{ A}$ ,  $R_{SET} = 91\text{ k}\Omega$

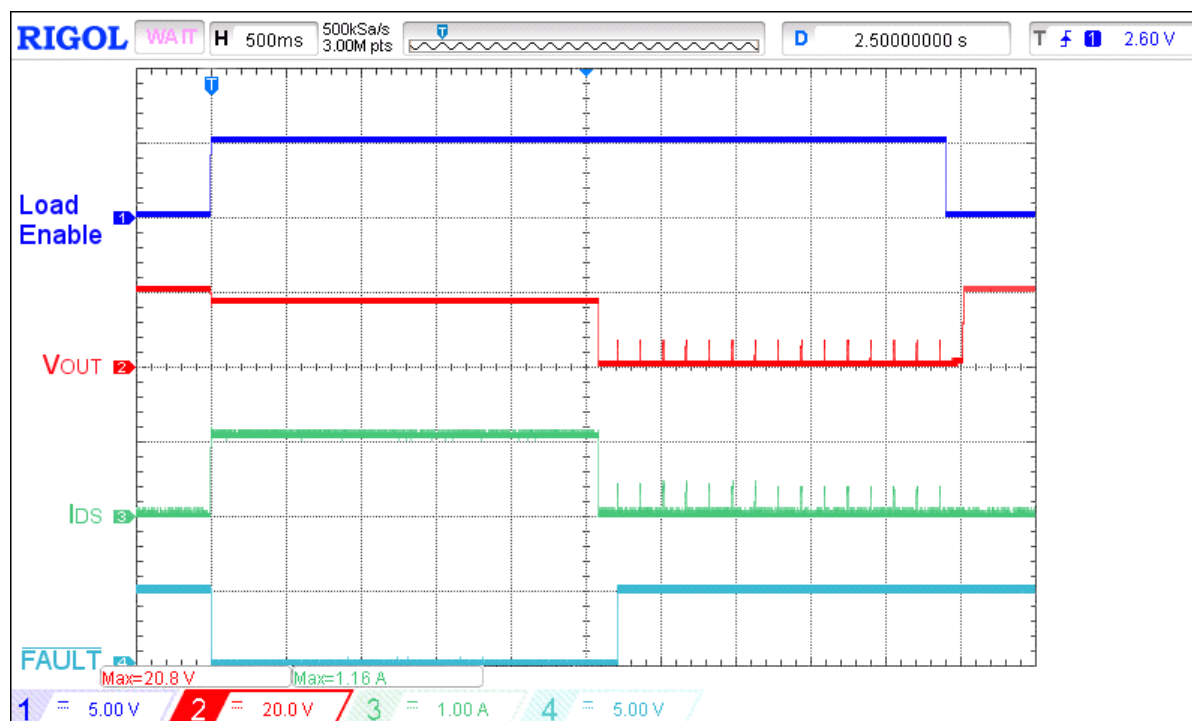


Figure 21. Typical ACL operation waveform for  $V_{IN} = 20\text{ V}$ ,  $C_{LOAD} = 10\text{ }\mu\text{F}$ ,  $I_{ACL} = 1\text{ A}$ ,  $R_{SET} = 91\text{ k}\Omega$

A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch  
 with  $V_{IN}$  Lockout Select and MOSFET Current Monitor Output

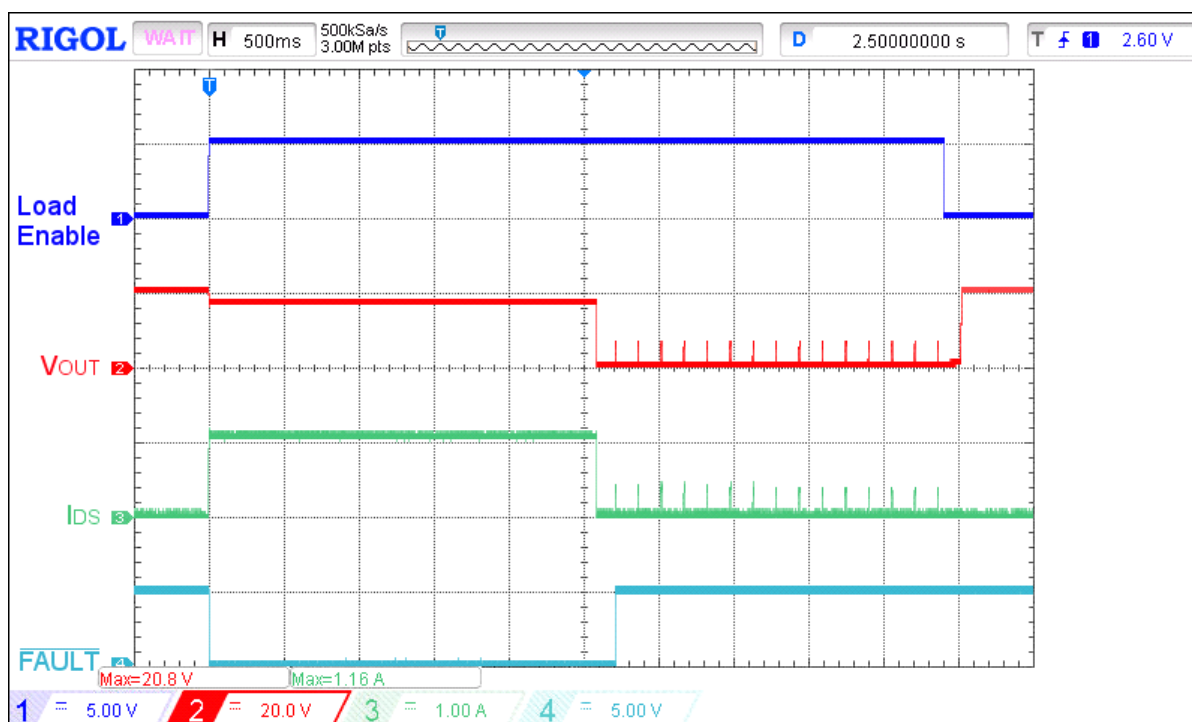


Figure 22. Thermally induced SOA shutdown for  $V_{IN} = 20$  V,  $C_{LOAD} = 10$   $\mu$ F,  $I_{ACL} = 1$  A,  $R_{SET} = 91$  k $\Omega$

A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch  
with  $V_{IN}$  Lockout Select and MOSFET Current Monitor Output

### Typical FAULT Operation Waveforms

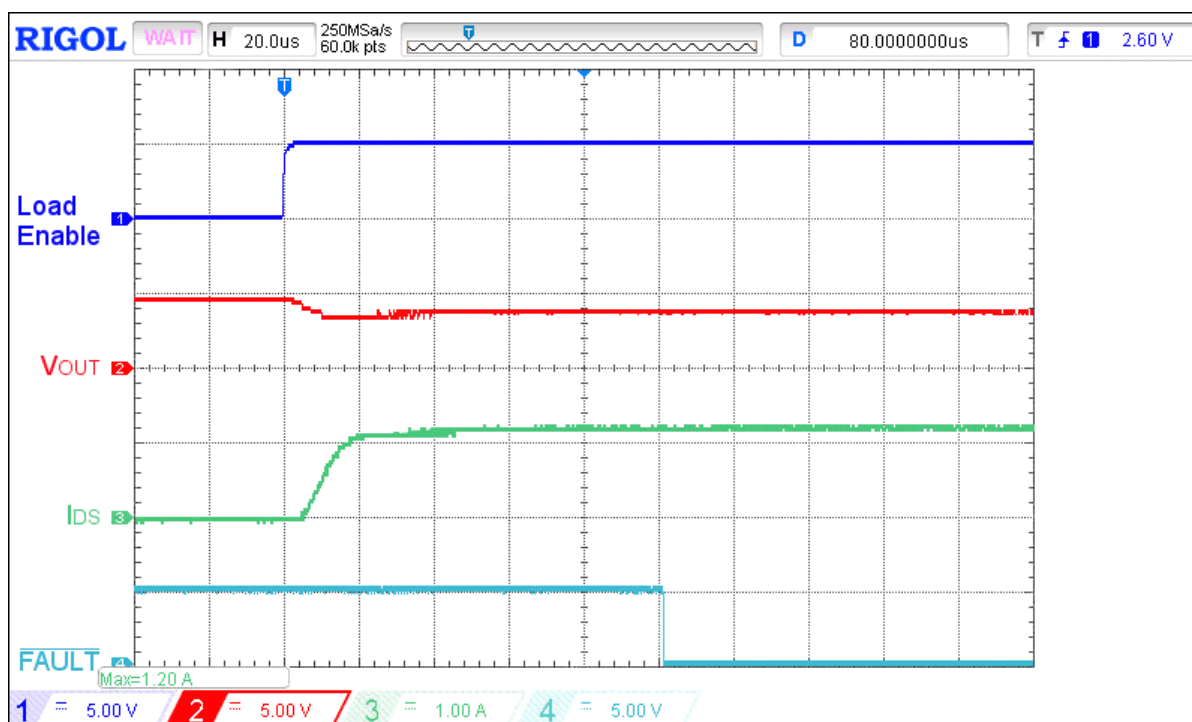


Figure 23. Typical FAULT assertion waveform for  $V_{IN} = 4.5\text{ V}$ ,  $C_{LOAD} = 10\text{ }\mu\text{F}$ ,  $I_{ACL} = 1\text{ A}$ ,  $R_{SET} = 91\text{ k}\Omega$ , switch on  $3.8\text{ }\Omega$  load

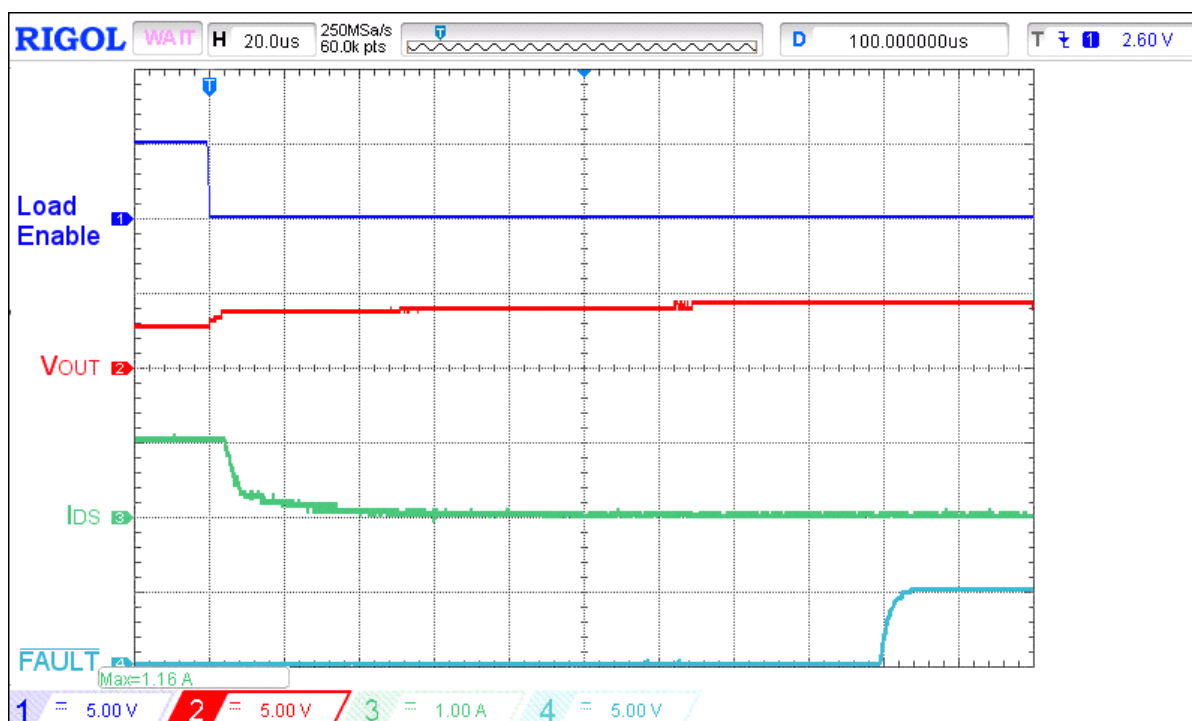


Figure 24. Typical FAULT de-assertion waveform for  $V_{IN} = 4.5\text{ V}$ ,  $C_{LOAD} = 10\text{ }\mu\text{F}$ ,  $I_{ACL} = 1\text{ A}$ ,  $R_{SET} = 91\text{ k}\Omega$ , switch out  $3.8\text{ }\Omega$  load



A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch  
 with  $V_{IN}$  Lockout Select and MOSFET Current Monitor Output

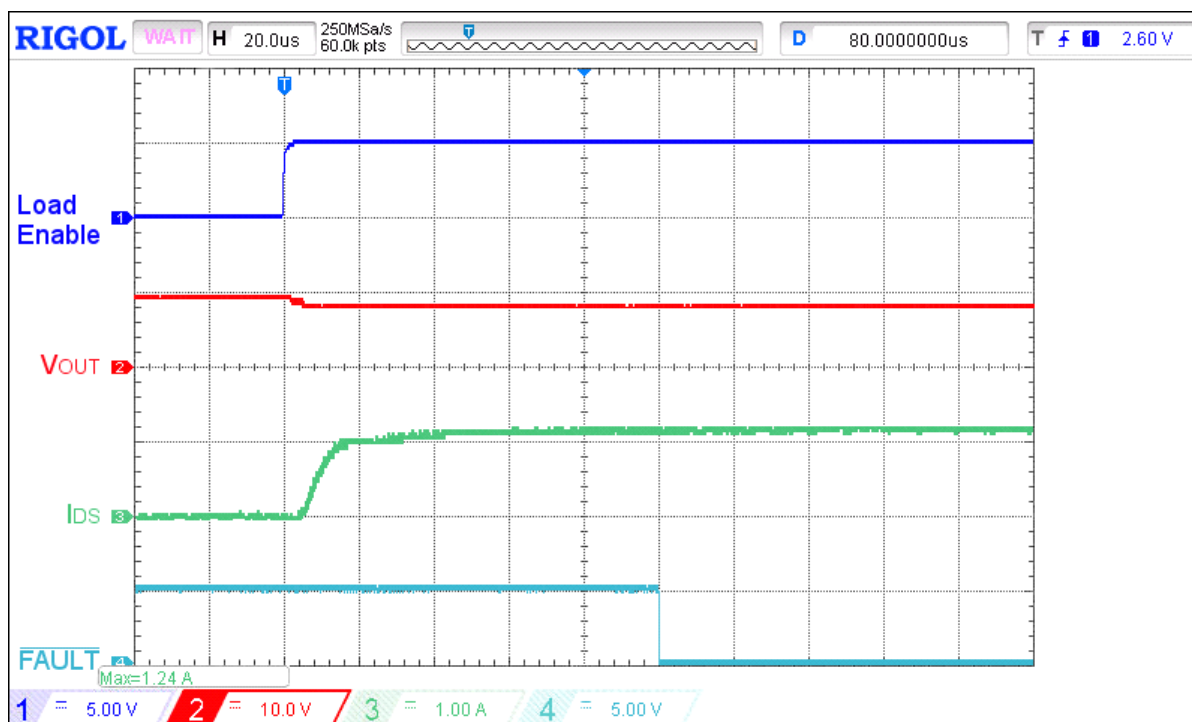


Figure 25. Typical FAULT assertion waveform for  $V_{IN} = 9\text{ V}$ ,  $C_{LOAD} = 10\text{ }\mu\text{F}$ ,  $I_{ACL} = 1\text{ A}$ ,  $R_{SET} = 91\text{ k}\Omega$ , switch on  $6.7\text{ }\Omega$  load

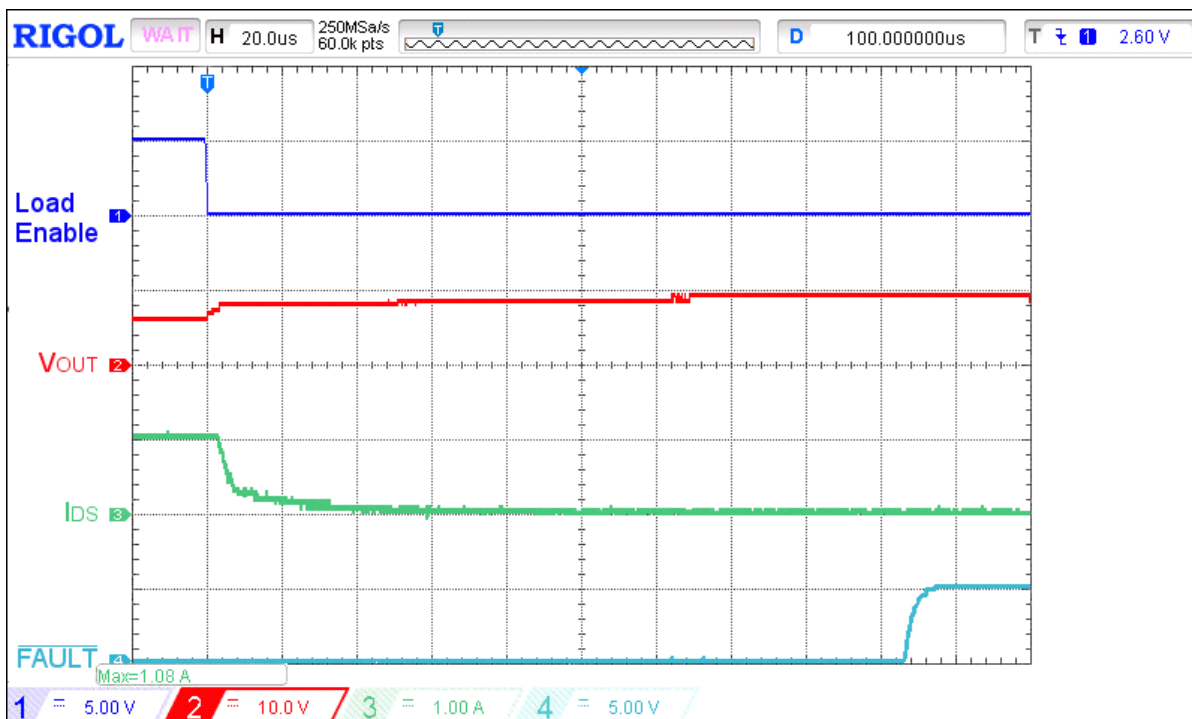


Figure 26. Typical FAULT de-assertion waveform for  $V_{IN} = 9\text{ V}$ ,  $C_{LOAD} = 10\text{ }\mu\text{F}$ ,  $I_{ACL} = 1\text{ A}$ ,  $R_{SET} = 91\text{ k}\Omega$ , switch out  $6.7\text{ }\Omega$  load



A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch  
with  $V_{IN}$  Lockout Select and MOSFET Current Monitor Output

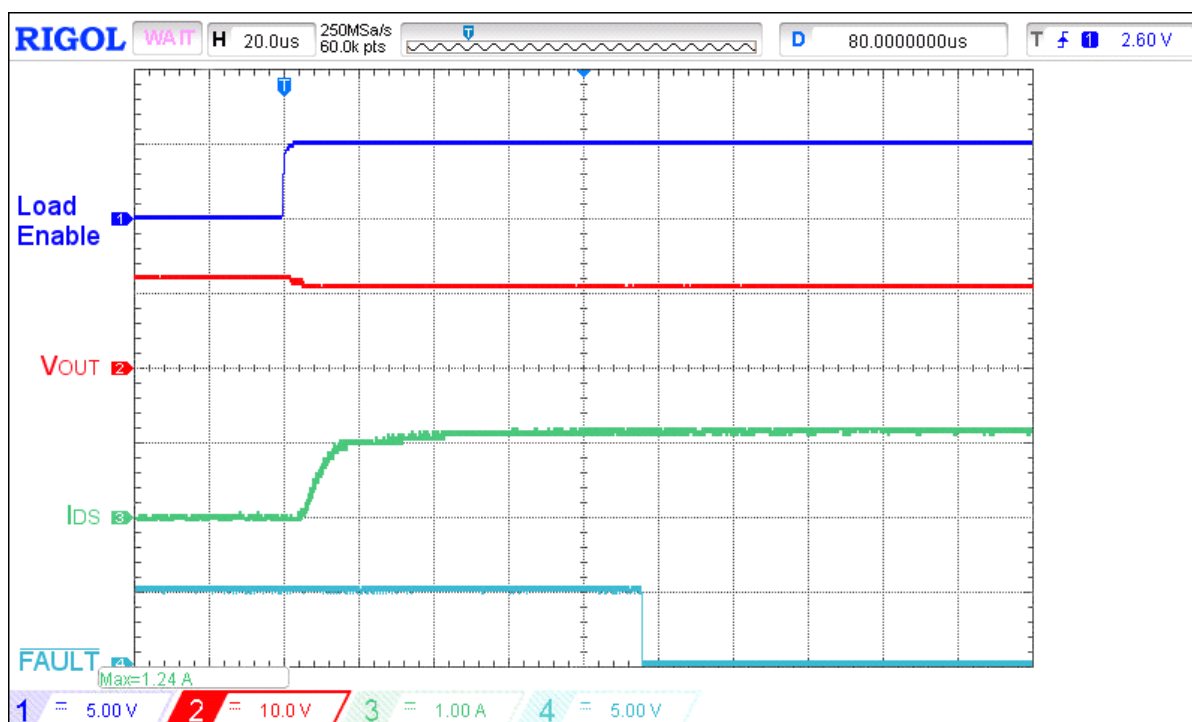


Figure 27. Typical  $\overline{\text{FAULT}}$  assertion waveform for  $V_{IN} = 12\text{ V}$ ,  $C_{LOAD} = 10\text{ }\mu\text{F}$ ,  $I_{ACL} = 1\text{ A}$ ,  $R_{SET} = 91\text{ k}\Omega$ , switch on  $9\text{ }\Omega$  load

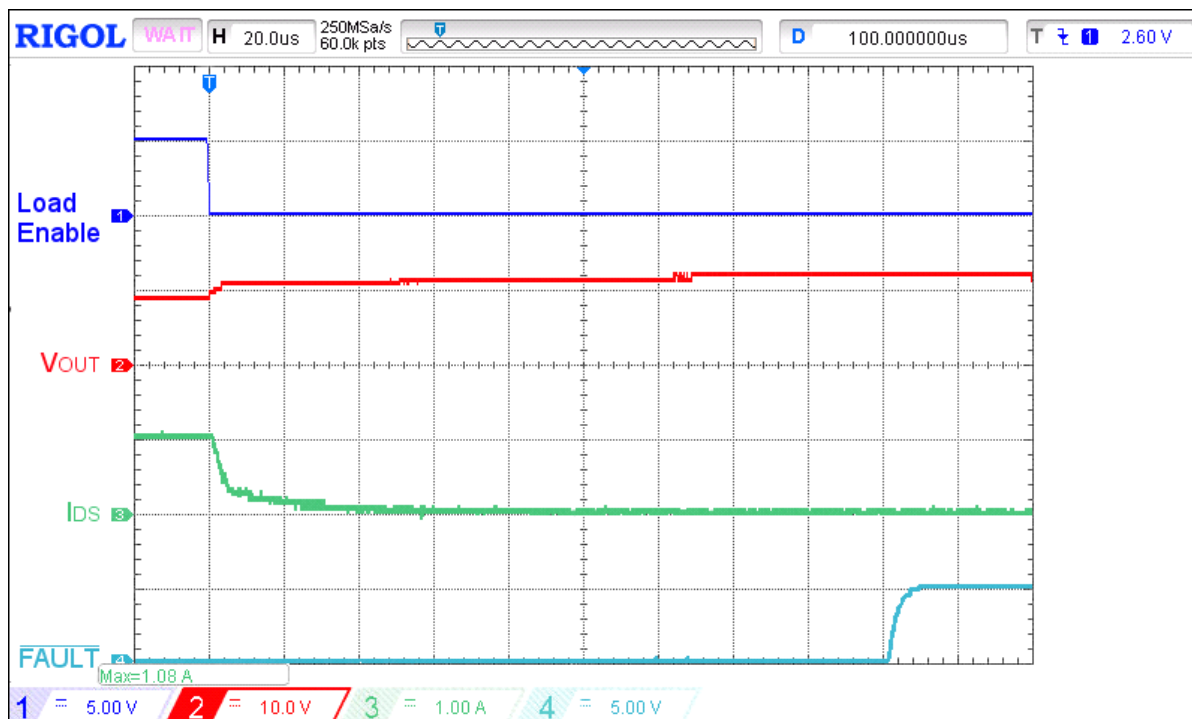


Figure 28. Typical  $\overline{\text{FAULT}}$  de-assertion waveform for  $V_{IN} = 12\text{ V}$ ,  $C_{LOAD} = 10\text{ }\mu\text{F}$ ,  $I_{ACL} = 1\text{ A}$ ,  $R_{SET} = 91\text{ k}\Omega$ , switch out  $9\text{ }\Omega$  load

A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch  
with  $V_{IN}$  Lockout Select and MOSFET Current Monitor Output

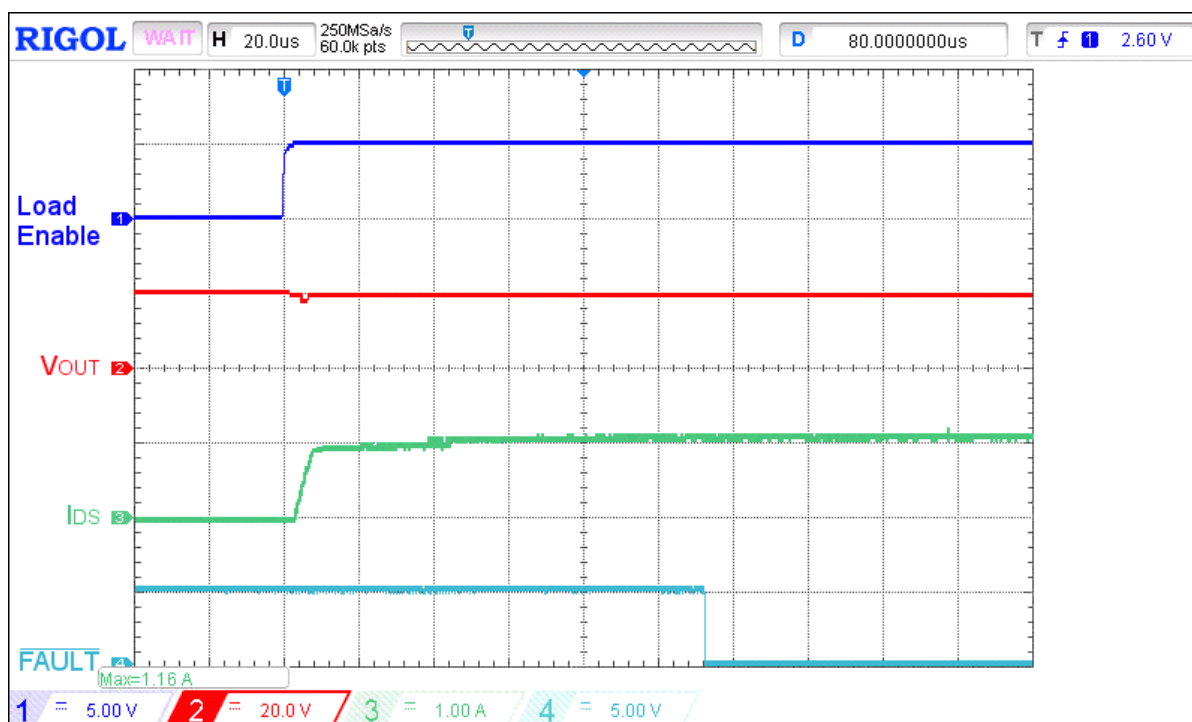


Figure 29. Typical  $\overline{\text{FAULT}}$  assertion waveform for  $V_{IN} = 20\text{ V}$ ,  $C_{LOAD} = 10\text{ }\mu\text{F}$ ,  $I_{ACL} = 1\text{ A}$ ,  $R_{SET} = 91\text{ k}\Omega$ , switch on  $15\text{ }\Omega$  load

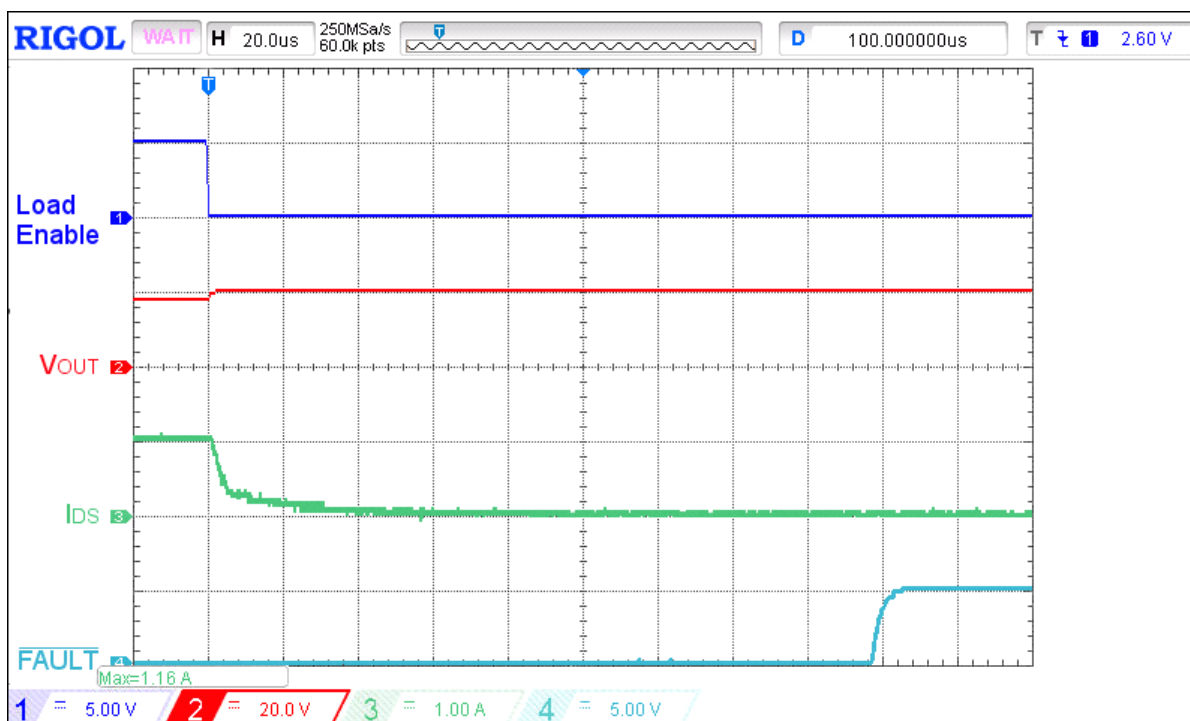


Figure 30. Typical  $\overline{\text{FAULT}}$  de-assertion waveform for  $V_{IN} = 20\text{ V}$ ,  $C_{LOAD} = 10\text{ }\mu\text{F}$ ,  $I_{ACL} = 1\text{ A}$ ,  $R_{SET} = 91\text{ k}\Omega$ , switch out  $15\text{ }\Omega$  load

A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch  
with  $V_{IN}$  Lockout Select and MOSFET Current Monitor Output

### Typical $I_{OUT}$ Response Time Waveforms

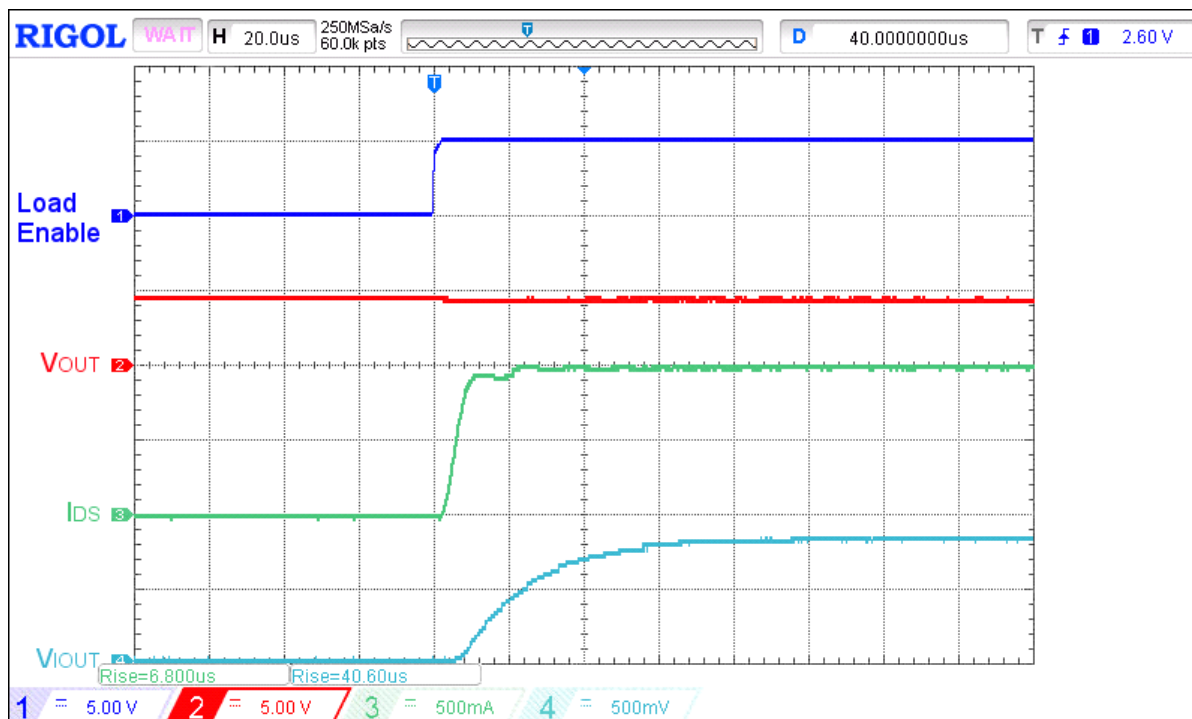


Figure 31. Typical  $I_{OUT}$  response time waveform for  $V_{IN} = 4.5$  V,  $C_{LOAD} = 10$   $\mu$ F,  $R_{LOAD} = 4.5$   $\Omega$ ,  $C_{IOUT} = 0.18$  nF,  $R_{IOUT} = 84.5$  k $\Omega$ , load step 0 A to 1 A

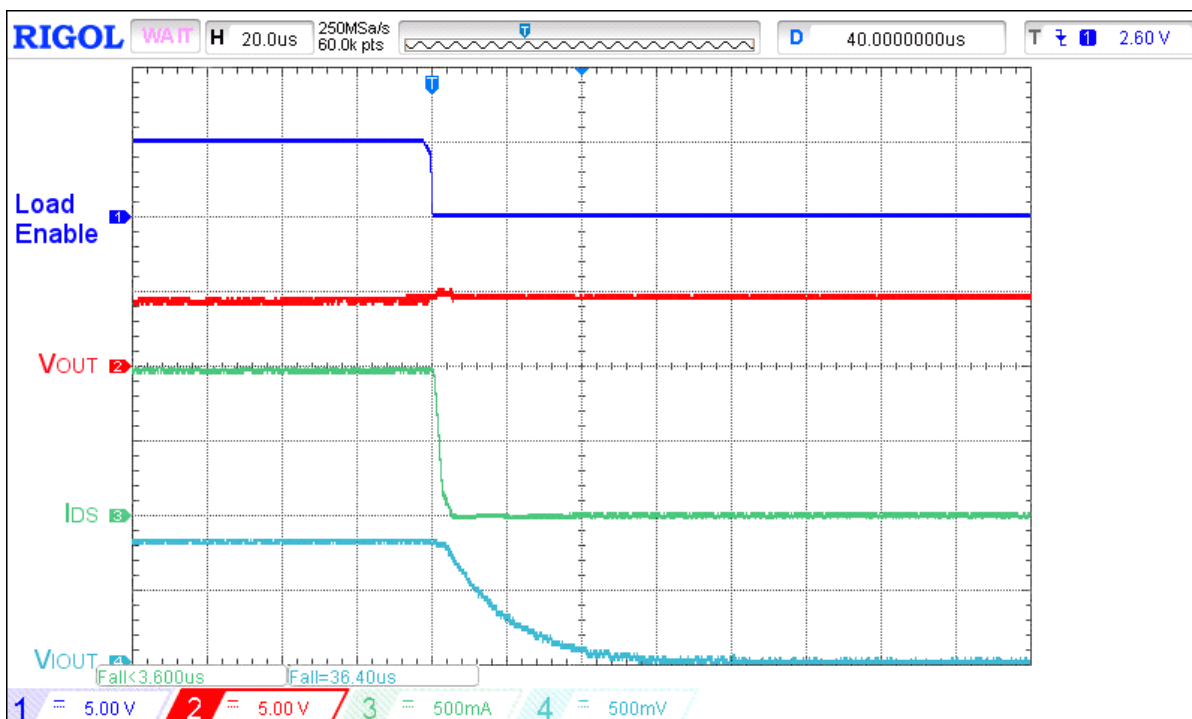


Figure 32. Typical  $I_{OUT}$  response time waveform for  $V_{IN} = 4.5$  V,  $C_{LOAD} = 10$   $\mu$ F,  $R_{LOAD} = 4.5$   $\Omega$ ,  $C_{IOUT} = 0.18$  nF,  $R_{IOUT} = 84.5$  k $\Omega$ , load step 1 A to 0 A

A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch  
 with  $V_{IN}$  Lockout Select and MOSFET Current Monitor Output

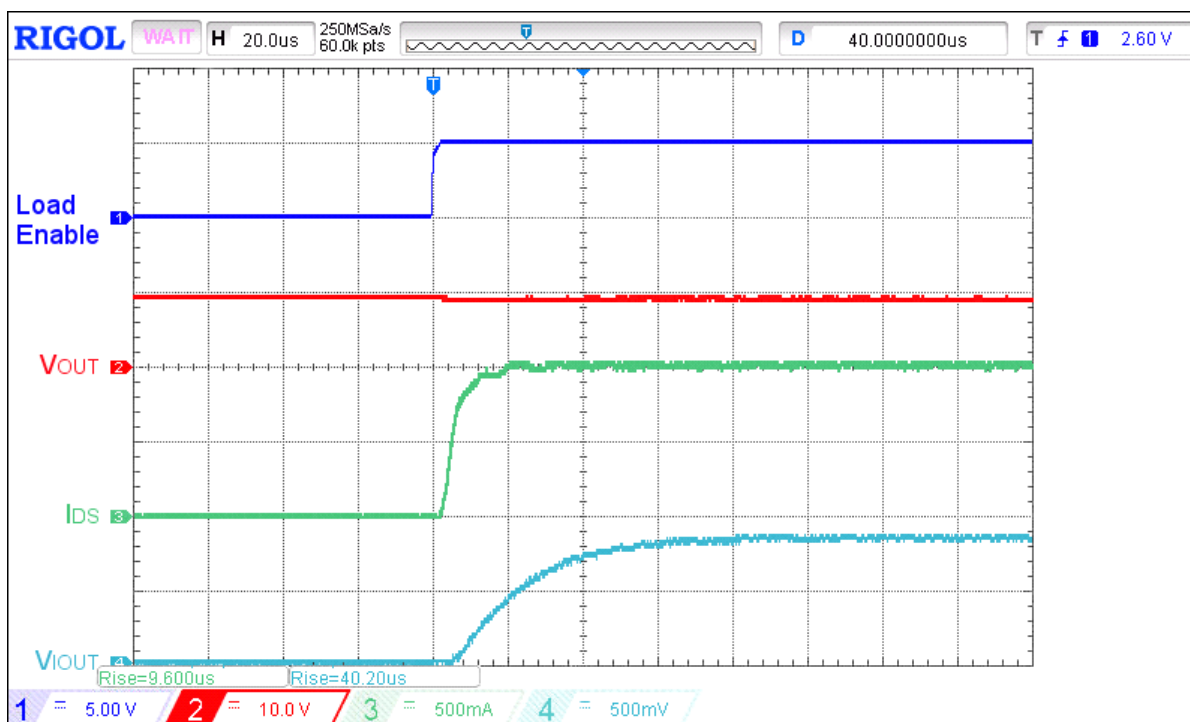


Figure 33. Typical  $I_{OUT}$  response time waveform for  $V_{IN} = 9\text{ V}$ ,  $C_{LOAD} = 10\text{ }\mu\text{F}$ ,  $R_{LOAD} = 9\text{ }\Omega$ ,  $C_{IOUT} = 0.18\text{ nF}$ ,  $R_{IOUT} = 84.5\text{ k}\Omega$ , load step 0 A to 1 A

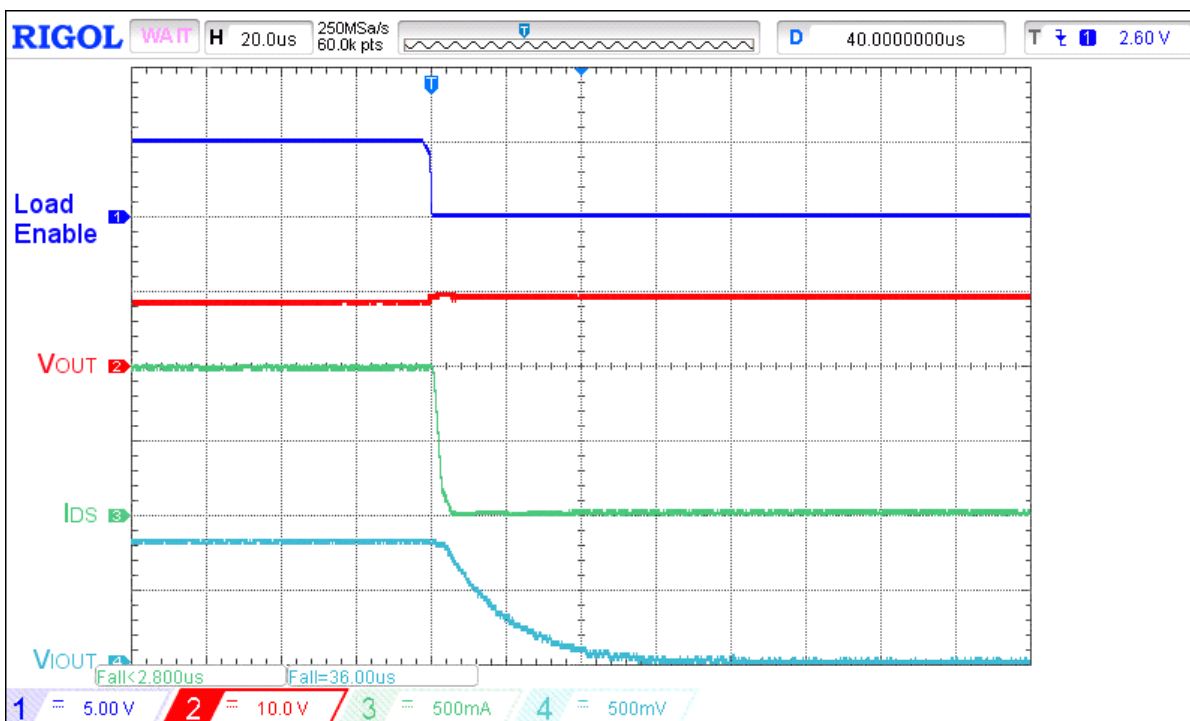


Figure 34. Typical  $I_{OUT}$  response time waveform for  $V_{IN} = 9\text{ V}$ ,  $C_{LOAD} = 10\text{ }\mu\text{F}$ ,  $R_{LOAD} = 9\text{ }\Omega$ ,  $C_{IOUT} = 0.18\text{ nF}$ ,  $R_{IOUT} = 84.5\text{ k}\Omega$ , load step 1 A to 0 A

A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch  
with  $V_{IN}$  Lockout Select and MOSFET Current Monitor Output

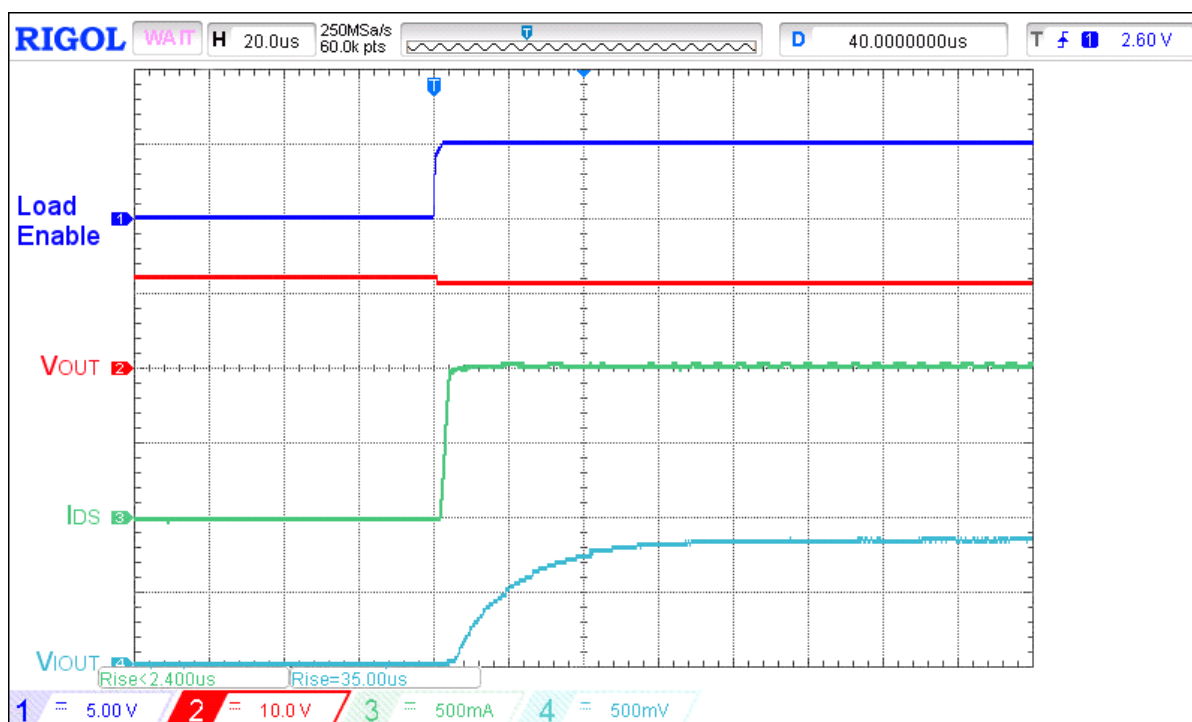


Figure 35. Typical  $I_{OUT}$  response time waveform for  $V_{IN} = 12\text{ V}$ ,  $C_{LOAD} = 10\text{ }\mu\text{F}$ ,  $R_{LOAD} = 12\text{ }\Omega$ ,  $C_{IOUT} = 0.18\text{ nF}$ ,  $R_{IOUT} = 84.5\text{ k}\Omega$ , load step 0 A to 1 A

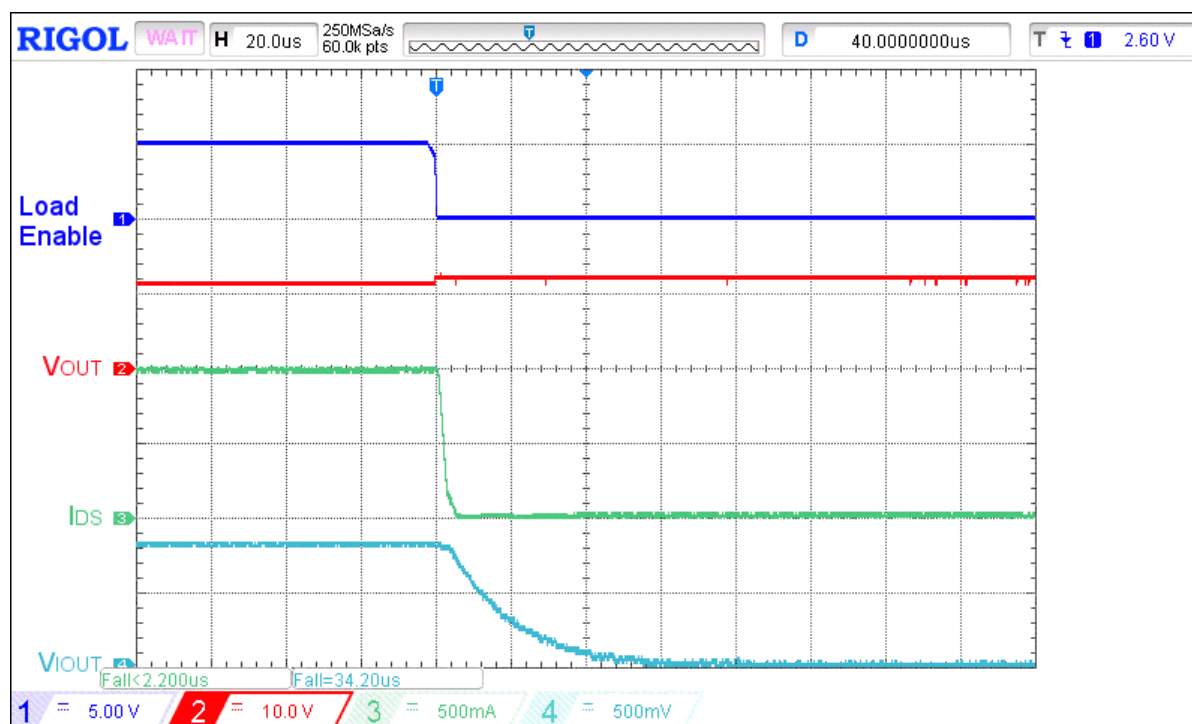


Figure 36. Typical  $I_{OUT}$  response time waveform for  $V_{IN} = 12\text{ V}$ ,  $C_{LOAD} = 10\text{ }\mu\text{F}$ ,  $R_{LOAD} = 12\text{ }\Omega$ ,  $C_{IOUT} = 0.18\text{ nF}$ ,  $R_{IOUT} = 84.5\text{ k}\Omega$ , load step 1 A to 0 A

A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch  
with  $V_{IN}$  Lockout Select and MOSFET Current Monitor Output

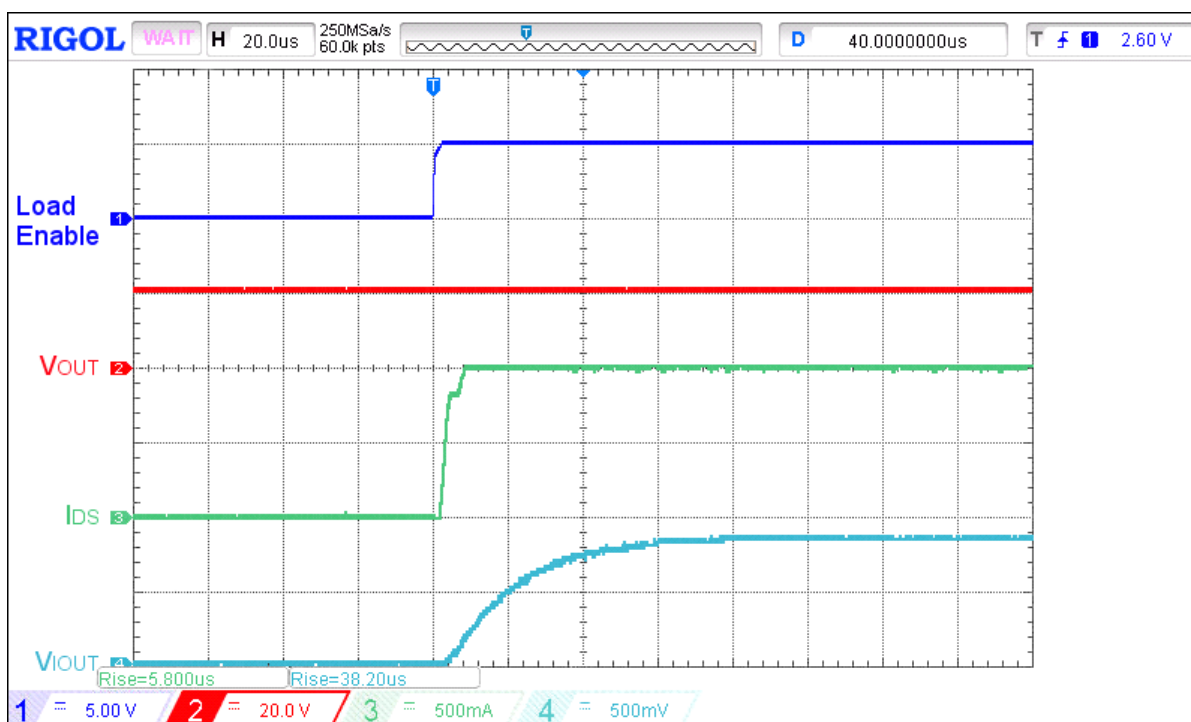


Figure 37. Typical  $I_{OUT}$  response time waveform for  $V_{IN} = 20\text{ V}$ ,  $C_{LOAD} = 10\text{ }\mu\text{F}$ ,  $R_{LOAD} = 20\text{ }\Omega$ ,  $C_{IOUT} = 0.18\text{ nF}$ ,  $R_{IOUT} = 84.5\text{ k}\Omega$ , load step 0 A to 1 A

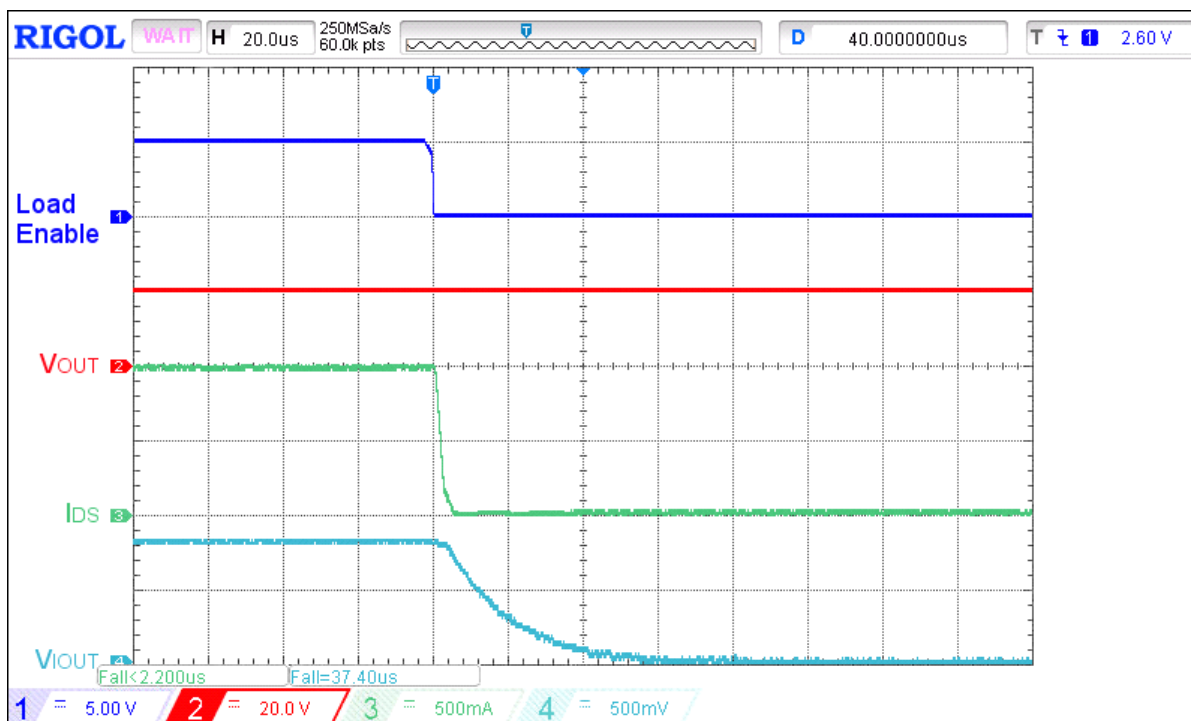


Figure 38. Typical  $I_{OUT}$  response time waveform for  $V_{IN} = 20\text{ V}$ ,  $C_{LOAD} = 10\text{ }\mu\text{F}$ ,  $R_{LOAD} = 20\text{ }\Omega$ ,  $C_{IOUT} = 0.18\text{ nF}$ ,  $R_{IOUT} = 84.5\text{ k}\Omega$ , load step 1 A to 0 A

A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch  
with  $V_{IN}$  Lockout Select and MOSFET Current Monitor Output

### Typical SOA Waveforms

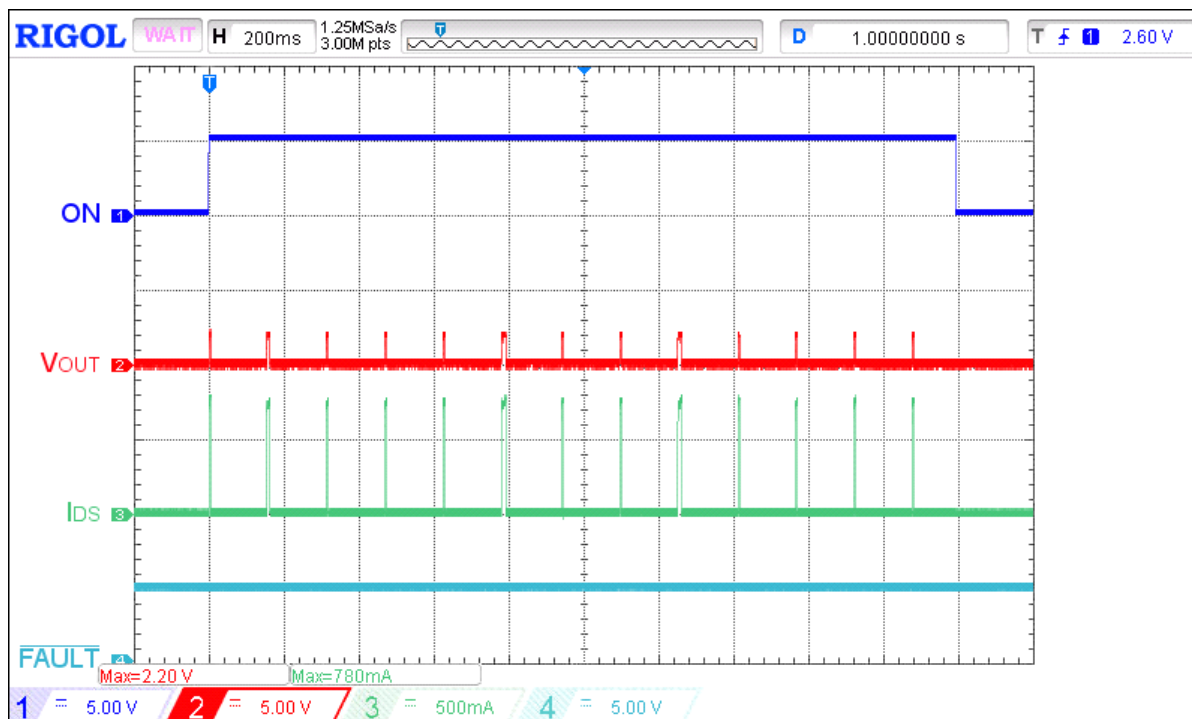


Figure 39. Typical SOA waveform during power up under heavy load for  $V_{IN} = 9\text{ V}$ ,  
 $C_{LOAD} = 10\text{ }\mu\text{F}$ ,  $R_{SET} = 30.1\text{ k}\Omega$ ,  $R_{LOAD} = 3.8\text{ }\Omega$

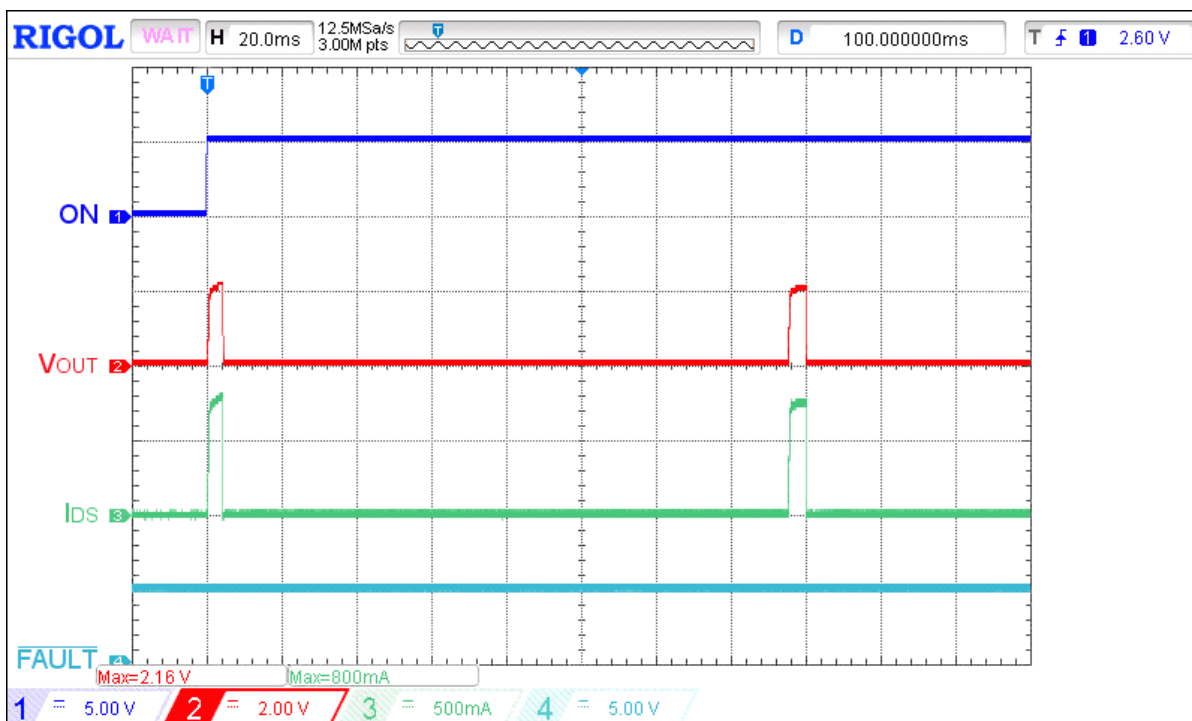


Figure 40. Extended typical SOA waveform during power up under heavy load for  $V_{IN} = 9\text{ V}$ ,  
 $C_{LOAD} = 10\text{ }\mu\text{F}$ ,  $R_{SET} = 30.1\text{ k}\Omega$ ,  $R_{LOAD} = 3.8\text{ }\Omega$



A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch  
 with  $V_{IN}$  Lockout Select and MOSFET Current Monitor Output

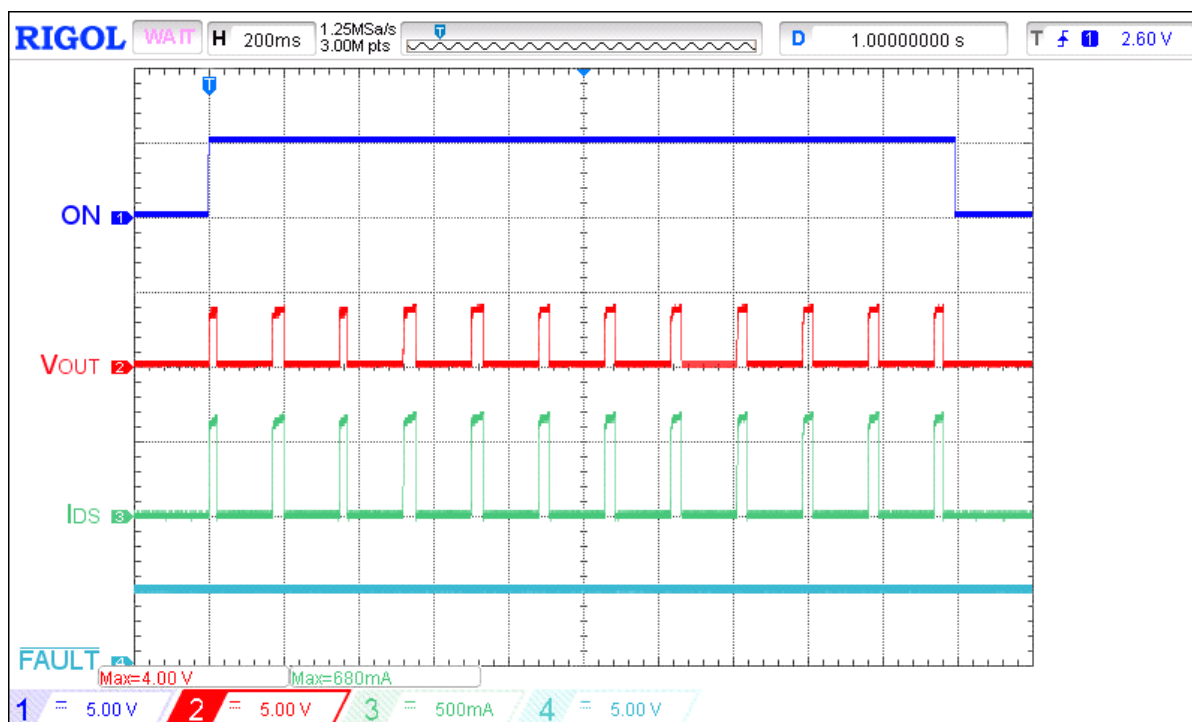


Figure 41. Typical SOA waveform during power up under heavy load for  $V_{IN} = 12\text{ V}$ ,  
 $C_{LOAD} = 10\text{ }\mu\text{F}$ ,  $R_{SET} = 30.1\text{ k}\Omega$ ,  $R_{LOAD} = 5\text{ }\Omega$

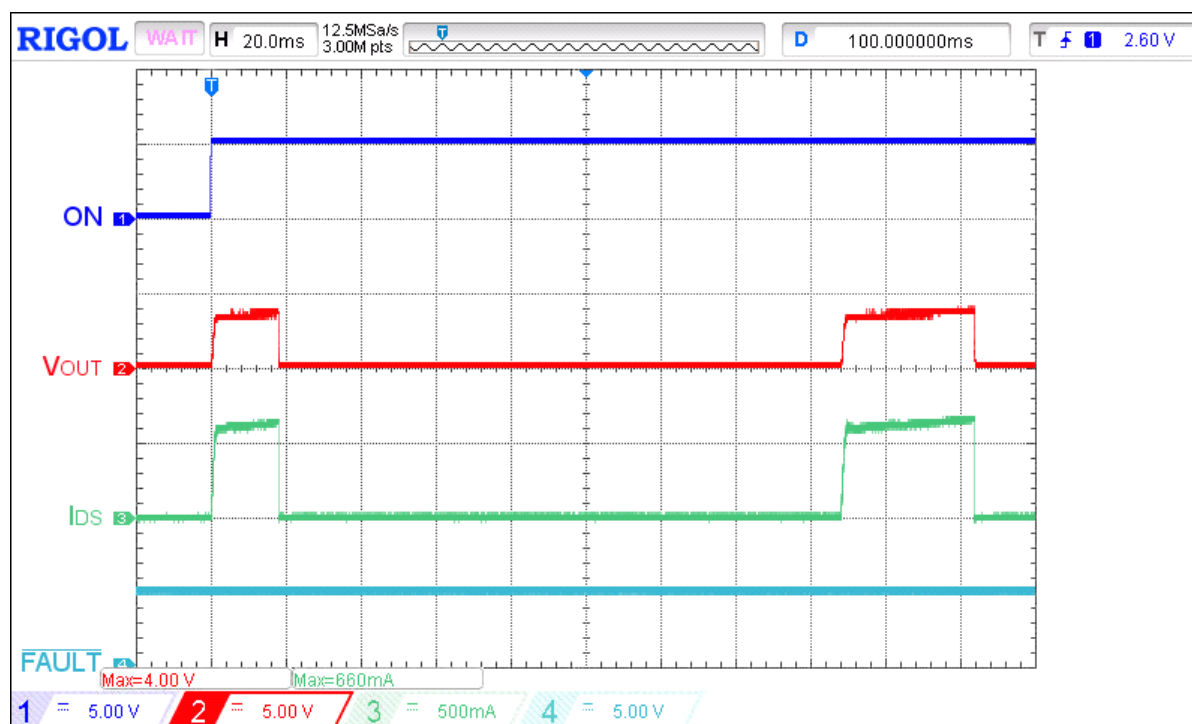


Figure 42. Extended typical SOA waveform during power up under heavy load for  $V_{IN} = 12\text{ V}$ ,  
 $C_{LOAD} = 10\text{ }\mu\text{F}$ ,  $R_{SET} = 30.1\text{ k}\Omega$ ,  $R_{LOAD} = 5\text{ }\Omega$



A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch  
 with  $V_{IN}$  Lockout Select and MOSFET Current Monitor Output

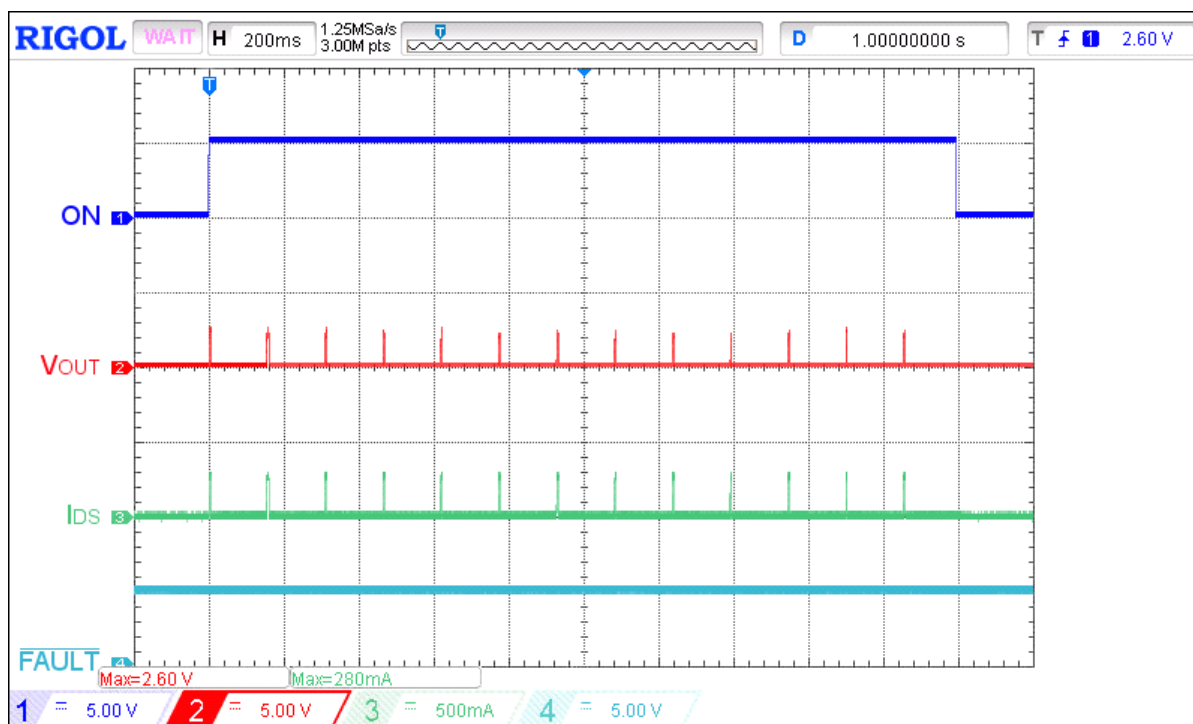


Figure 43. Typical SOA waveform during power up under heavy load for  $V_{IN} = 20\text{ V}$ ,  
 $C_{LOAD} = 10\text{ }\mu\text{F}$ ,  $R_{SET} = 30.1\text{ k}\Omega$ ,  $R_{LOAD} = 8\text{ }\Omega$

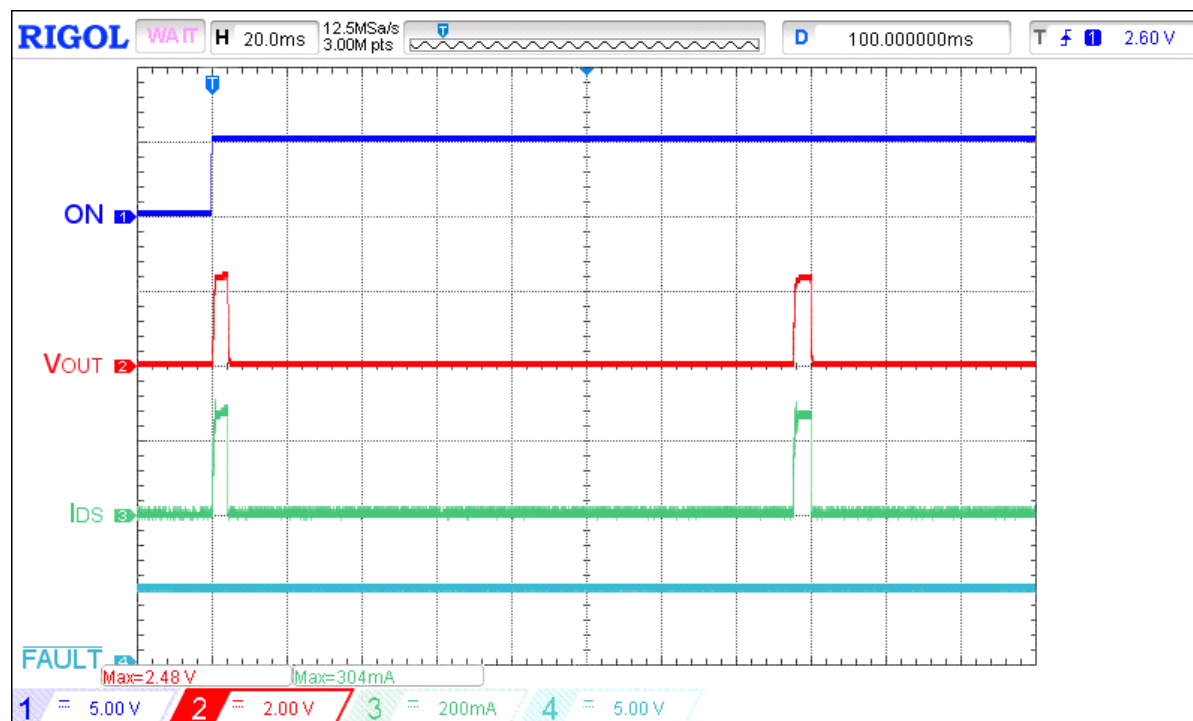


Figure 44. Extended typical SOA waveform during power up under heavy load for  $V_{IN} = 20\text{ V}$ ,  
 $C_{LOAD} = 10\text{ }\mu\text{F}$ ,  $R_{SET} = 30.1\text{ k}\Omega$ ,  $R_{LOAD} = 8\text{ }\Omega$

## A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch with $V_{IN}$ Lockout Select and MOSFET Current Monitor Output

### Applications Information

#### HFET1 Safe Operating Area Explained

Dialog's HFET1 integrated power controllers incorporate a number of internal protection features that prevents them from damaging themselves or any other circuit or subcircuit downstream of them. One particular protection feature is their Safe Operation Area (SOA) protection. SOA protection is automatically activated under overpower and, in some cases, under overcurrent conditions. Overpower SOA is activated if package power dissipation exceeds an internal 5 W threshold longer than 2.5 ms. HFET1 devices will quickly switch off (open circuit) upon overpower detection and automatically resume (close) nominal operation once overpower condition no longer exists.

One possible way to have an overpower condition trigger SOA protection is when HFET1 products are enabled into heavy output resistive loads and/or into large load capacitors. It is under these conditions to follow carefully the "Safe Start-up Loading" guidance in the Applications section of the datasheet. During an overcurrent condition, HFET1 devices will try to limit the output current to the level set by the external  $R_{SET}$  resistor. Limiting the output current, however, causes an increased voltage drop across the FET's channel because the FET's  $R_{DS(ON)}$  increased as well. Since the FET's  $R_{DS(ON)}$  is larger, package power dissipation also increases. If the resultant increase in package power dissipation is higher/equal than 5 W for longer than 2.5 ms, internal SOA protection will be triggered and the FET will open circuit (switch off). Every time SOA protection is triggered, all HFET1 devices will automatically attempt to resume nominal operation after 160 ms.

#### Safe Start-up Condition

SLG59H1020V has built-in protection to prevent over-heating during start-up into a heavy load. Overloading the  $V_{OUT}$  pin with a capacitor and a resistor may result in non-monotonic  $V_{OUT}$  ramping. In general, under light loading on  $V_{OUT}$ ,  $V_{OUT}$  ramping can be controlled with  $C_{SLEW}$  value. The following equation serves as a guide:

$$C_{SLEW} = \frac{T_{RISE}}{V_{IN}} \times 4.9 \mu A \times \frac{20}{3}$$

where

$T_{RISE}$  = Total rise time from 10%  $V_{OUT}$  to 90%  $V_{OUT}$

$V_{IN}$  = Input Voltage

$C_{SLEW}$  = Capacitor value for CAP pin

When capacitor and resistor loading on  $V_{OUT}$  during start up, the following tables will ensure  $V_{OUT}$  ramping is monotonic without triggering internal protection:

Safe Start-up Loading for $V_{IN} = 12$ V (Monotonic Ramp)			
Slew Rate (V/ms)	$C_{SLEW}$ (nF) <sup>2</sup>	$C_{LOAD}$ (μF)	$R_{LOAD}$ (Ω)
1	33.3	500	20
2	16.7	250	20
3	11.1	160	20
4	8.3	120	20
5	6.7	100	20

## A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch with $V_{IN}$ Lockout Select and MOSFET Current Monitor Output

Safe Start-up Loading for $V_{IN} = 22\text{ V}$ (Monotonic Ramp)			
Slew Rate (V/ms)	$C_{SLEW}$ (nF) <sup>2</sup>	$C_{LOAD}$ (μF)	$R_{LOAD}$ (Ω)
0.5	66.7	500	80
1.0	33.3	250	80
1.5	22.2	160	80
2.0	16.7	120	80
2.5	13.3	100	80

Note 2: Select the closest-value tolerance capacitor.

### Setting the SLG59H1020V's Active Current Limit

$R_{SET}$ (kΩ)	Active Current Limit (A) <sup>3</sup>
91	1
45	2
30	3

Note 3: Active Current Limit accuracy is  $\pm 15\%$  over voltage range and over temperature range.

### Setting the SLG59H1020V's Input Overvoltage Lockout Threshold

As shown in the table below, SEL[1,0] selects the  $V_{IN}$  overvoltage threshold at which the SLG59H1020V's internal state machine will turn OFF (open circuit) the power MOSFET if  $V_{IN}$  exceeds the selected threshold.

SEL1	SEL0	$V_{IN(OVLO)}$ (Typ)
0	0	6.0
0	1	10.8
1	0	17.0
1	1	22.0

For example, SEL[1,1] would be the most appropriate setting for applications where the steady-state  $V_{IN}$  can extend up to 20 V without causing any damage to the SLG59H1020V since the IC is 29-V tolerant.

With an activated SLG59H1020V (ON=HIGH) and at any time  $V_{IN}$  crosses the programmed  $V_{IN}$  overvoltage threshold, the state machine opens the power switch and asserts the FAULT pin within  $T_{FAULT\_LOW}$ .

In applications with a deactivated or inactive SLG59H1020V ( $V_{IN} > V_{IN(UVLO)}$  and ON=LOW) and if the applied  $V_{IN}$  is higher than the programmed  $V_{IN(OVLO)}$  threshold, the SLG59H1020V's state machine will keep the power switch open circuited if the ON pin is toggled LOW-to-HIGH. In these cases, the FAULT pin will also be asserted within  $T_{FAULT\_LOW}$  and will remain asserted until  $V_{IN}$  resumes nominal, steady-state operation.

In all cases, the SLG59H1020V's  $V_{IN}$  undervoltage lockout threshold is fixed at  $V_{IN(UVLO)}$ .

## A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch with $V_{IN}$ Lockout Select and MOSFET Current Monitor Output

### Power Dissipation

The junction temperature of the SLG59H1020V depends on different factors such as board layout, ambient temperature, and other environmental factors. The primary contributor to the increase in the junction temperature of the SLG59H1020V is the power dissipation of its power MOSFET. Its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD = RDS_{ON} \times I_{DS}^2$$

where:

PD = Power dissipation, in Watts (W)

$RDS_{ON}$  = Power MOSFET ON resistance, in Ohms ( $\Omega$ )

$I_{DS}$  = Output current, in Amps (A)

and

$$T_J = PD \times \theta_{JA} + T_A$$

where:

$T_J$  = Junction temperature, in Celsius degrees ( $^{\circ}\text{C}$ )

$\theta_{JA}$  = Package thermal resistance, in Celsius degrees per Watt ( $^{\circ}\text{C}/\text{W}$ )

$T_A$  = Ambient temperature, in Celsius degrees ( $^{\circ}\text{C}$ )

In current-limit mode, the SLG59H1020V's power dissipation can be calculated by taking into account the voltage drop across the power switch ( $V_{IN}-V_{OUT}$ ) and the magnitude of the output current in current-limit mode ( $I_{ACL}$ ):

$$PD = (V_{IN}-V_{OUT}) \times I_{ACL} \text{ or}$$

$$PD = (V_{IN} - (R_{LOAD} \times I_{ACL})) \times I_{ACL}$$

where:

PD = Power dissipation, in Watts (W)

$V_{IN}$  = Input Voltage, in Volts (V)

$R_{LOAD}$  = Load Resistance, in Ohms ( $\Omega$ )

$I_{ACL}$  = Output limited current, in Amps (A)

$V_{OUT} = R_{LOAD} \times I_{ACL}$

## A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch with $V_{IN}$ Lockout Select and MOSFET Current Monitor Output

### Layout Guidelines:

1. Since the VIN and VOUT pins dissipate most of the heat generated during high-load current operation, it is highly recommended to make power traces as short, direct, and wide as possible. A good practice is to make power traces with absolute minimum widths of 15 mils (0.381 mm) per Ampere. A representative layout, shown in [Figure 45](#), illustrates proper techniques for heat to transfer as efficiently as possible out of the device;
2. To minimize the effects of parasitic trace inductance on normal operation, it is recommended to connect input  $C_{IN}$  and output  $C_{LOAD}$  low-ESR capacitors as close as possible to the SLG59H1020V's VIN and VOUT pins;
3. The GND pin should be connected to system analog or power ground plane.
4. 2 oz. copper is recommended for high current operation.

### SLG59H1020V Evaluation Board:

A HFET1 Evaluation Board for SLG59H1020V is designed according to the statements above and is illustrated on [Figure 45](#). Please note that evaluation board has D\_Sense and S\_Sense pads. They cannot carry high currents and dedicated only for  $RDS_{ON}$  evaluation.

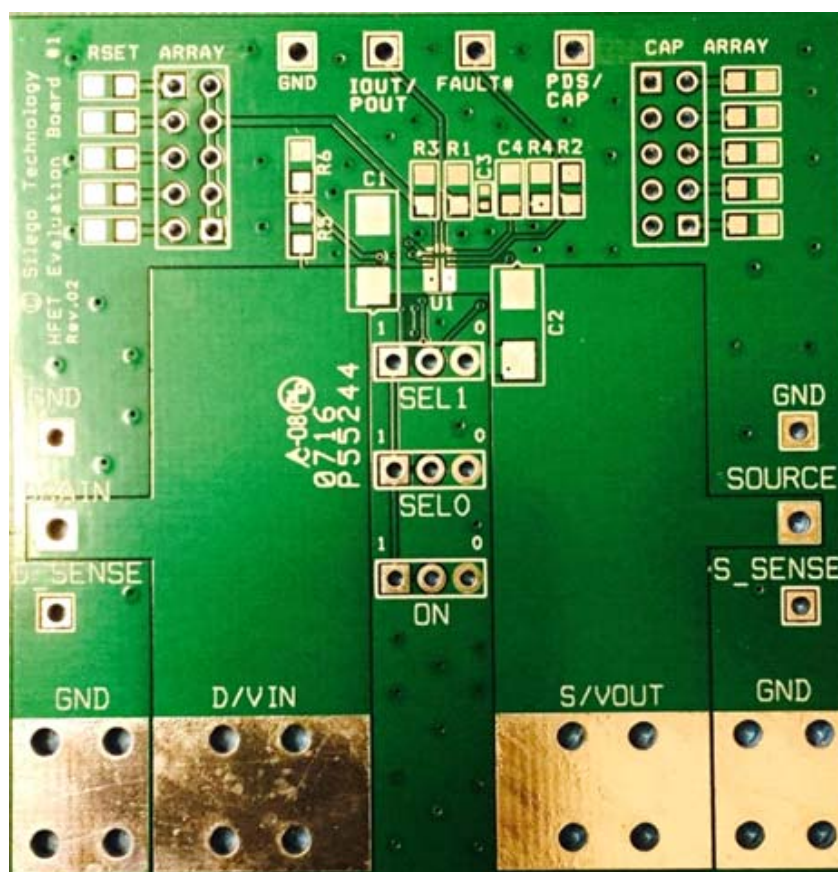


Figure 45. SLG59H1020V Evaluation Board

## A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch with $V_{IN}$ Lockout Select and MOSFET Current Monitor Output

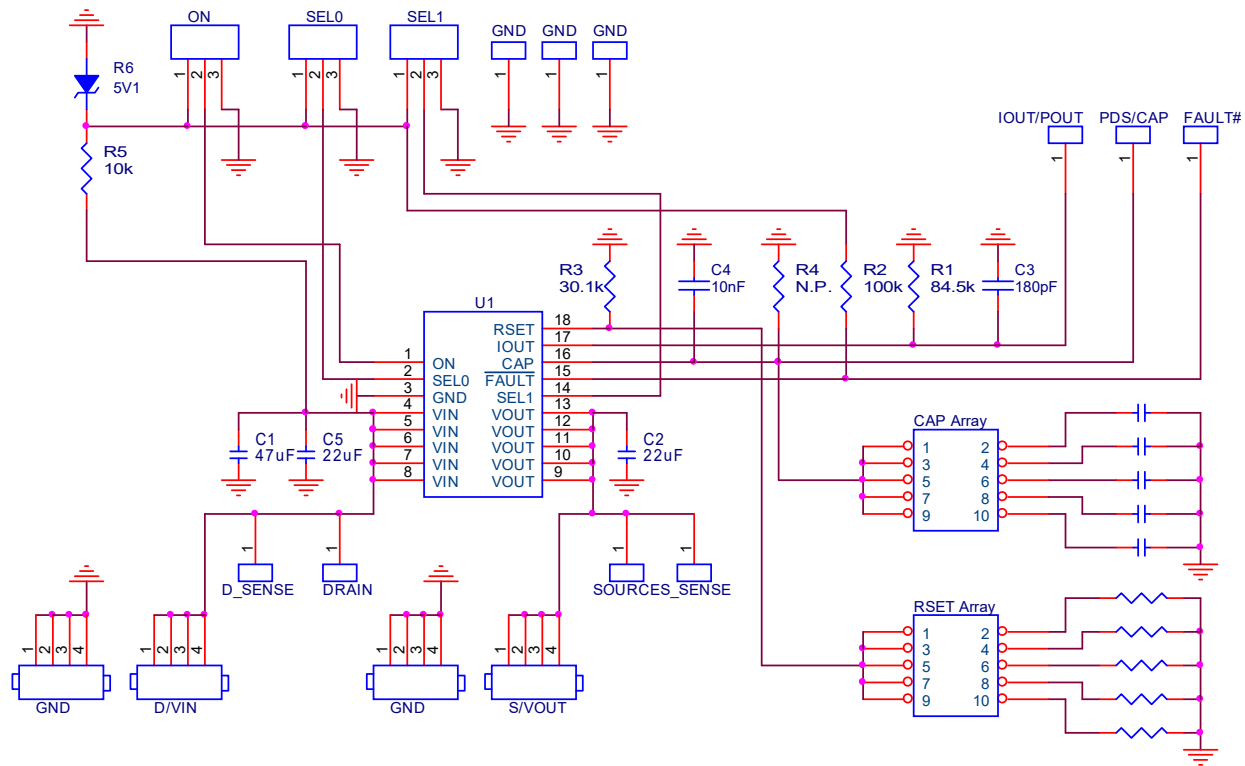


Figure 46. SLG59H1020V Evaluation Board Connection Circuit

### Basic Test Setup and Connections

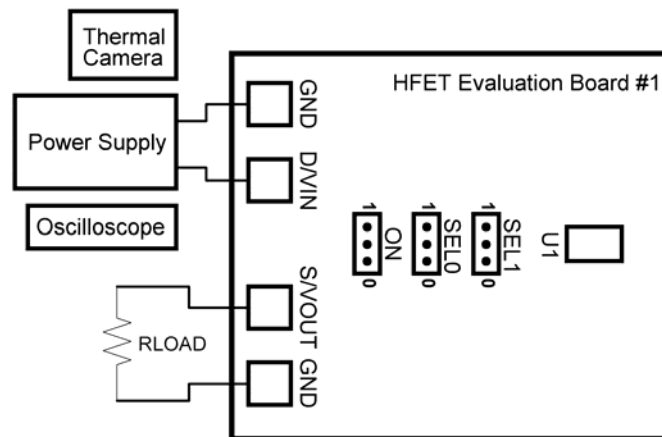


Figure 47. SLG59H1020V Evaluation Board Connection Circuit

### EVB Configuration

1. Based on  $V_{IN}$  voltage, set SEL0, SEL1 to GND or 5 V to configure OVLO;
2. Connect oscilloscope probes to D/VIN, S/VOUT, ON, etc.;
3. Turn on Power Supply and set desired  $V_{IN}$  from 4.5 V...20 V range;
4. Toggle the ON signal High or Low to observe SLG59H1020V operation.

A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch  
 with  $V_{IN}$  Lockout Select and MOSFET Current Monitor Output

### Package Top Marking System Definition



1020V - Part ID Field  
 WW - Date Code Field<sup>1</sup>  
 NNN - Lot Traceability Code Field<sup>1</sup>  
 A - Assembly Site Code Field<sup>2</sup>  
 RR - Part Revision Code Field<sup>2</sup>

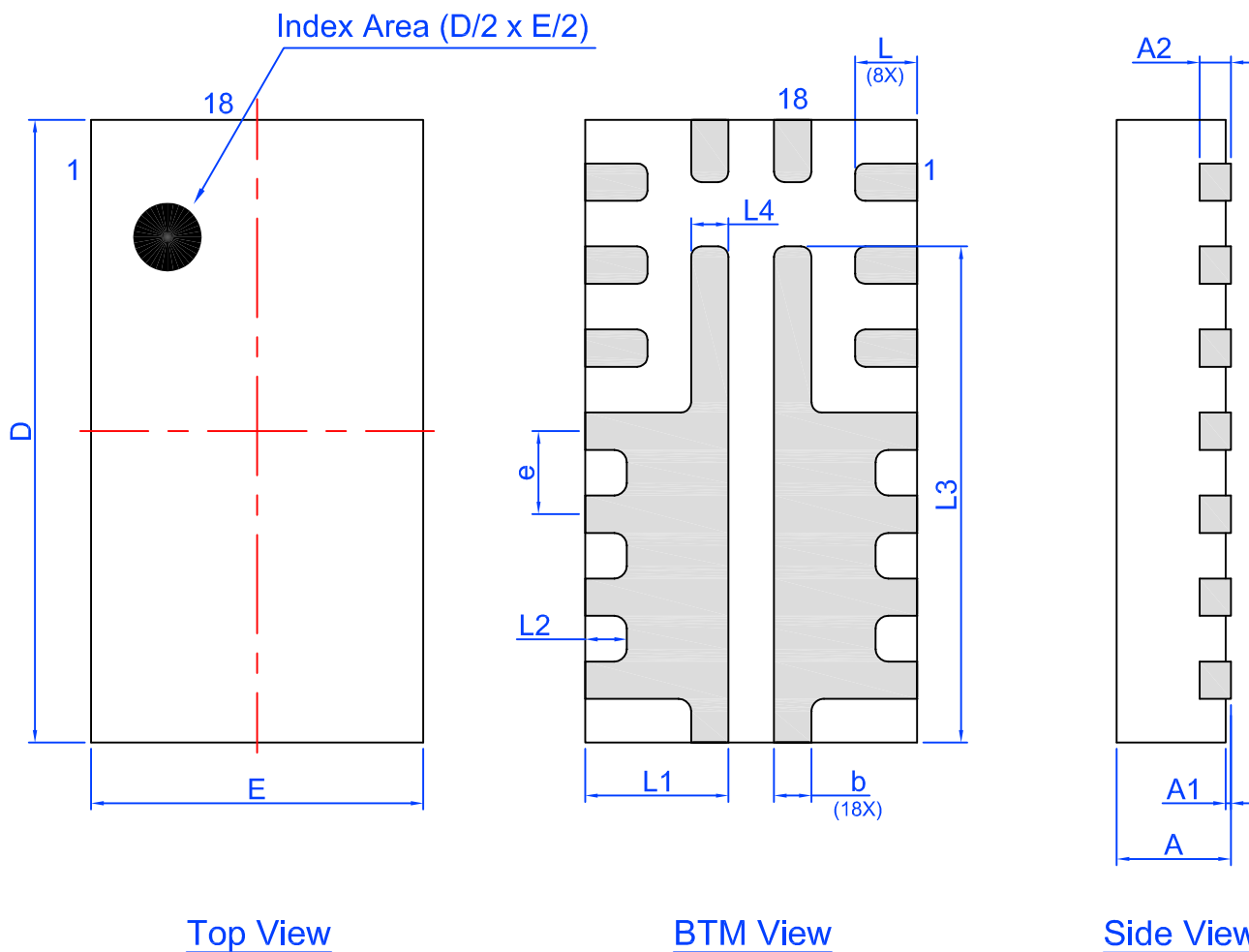
Note 1: Each character in code field can be alphanumeric A-Z and 0-9

Note 2: Character in code field can be alphabetic A-Z

A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch  
with  $V_{IN}$  Lockout Select and MOSFET Current Monitor Output

## Package Drawing and Dimensions

18 Lead TQFN Package 1.6 x 3 mm (Fused Lead)  
JEDEC MO-220, Variation WCEE



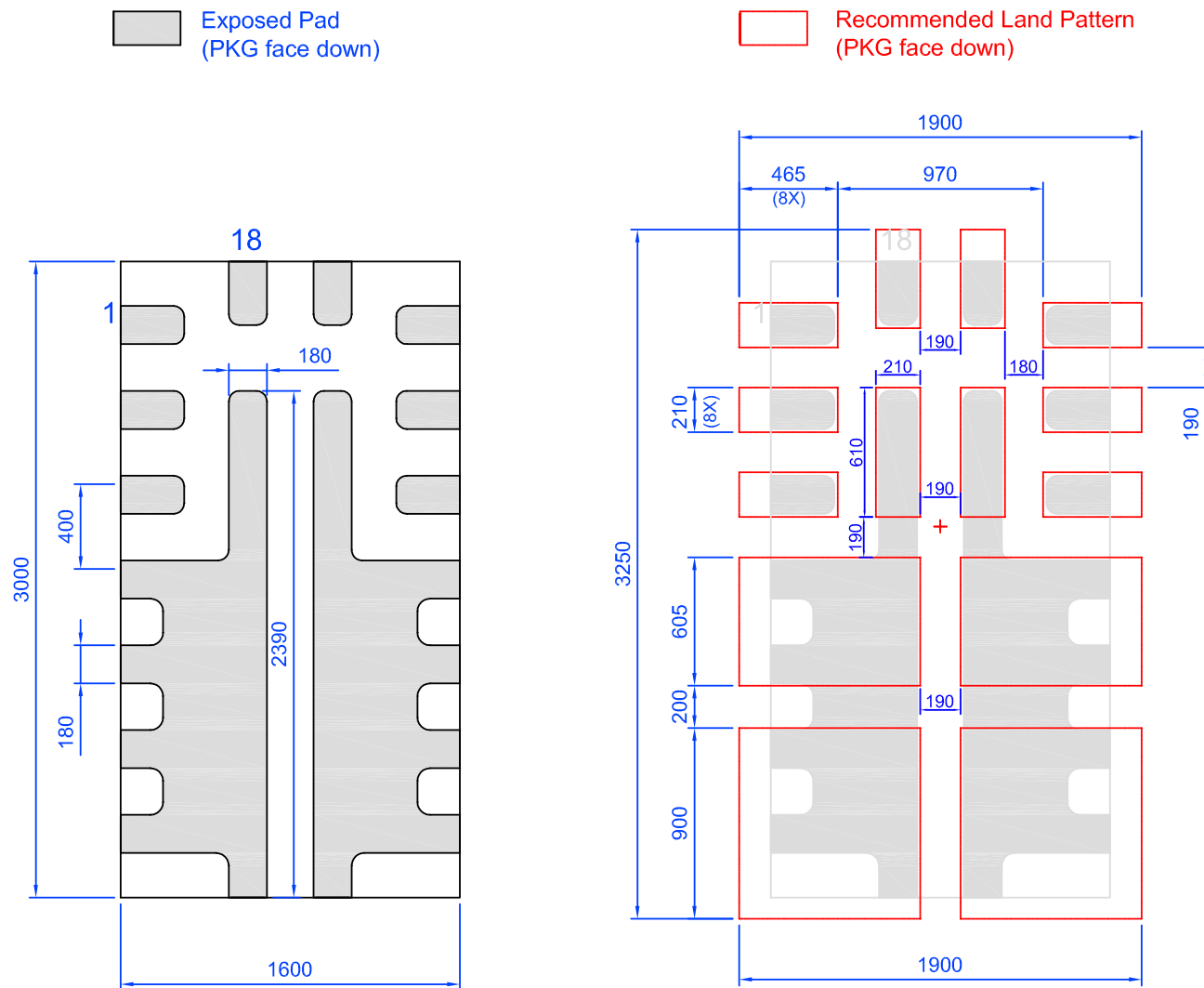
Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.05	E	1.55	1.60	1.65
A2	0.10	0.15	0.20	L	0.25	0.30	0.35
b	0.13	0.18	0.23	L1	0.64	0.69	0.74
e	0.40 BSC			L2	0.15	0.20	0.25
L3	2.34	2.39	2.44	L4	0.13	0.18	0.23



A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch  
with  $V_{IN}$  Lockout Select and MOSFET Current Monitor Output

## SLG59H1020V 18-pin STQFN PCB Landing Pattern



Note: All dimensions shown in micrometers (μm)

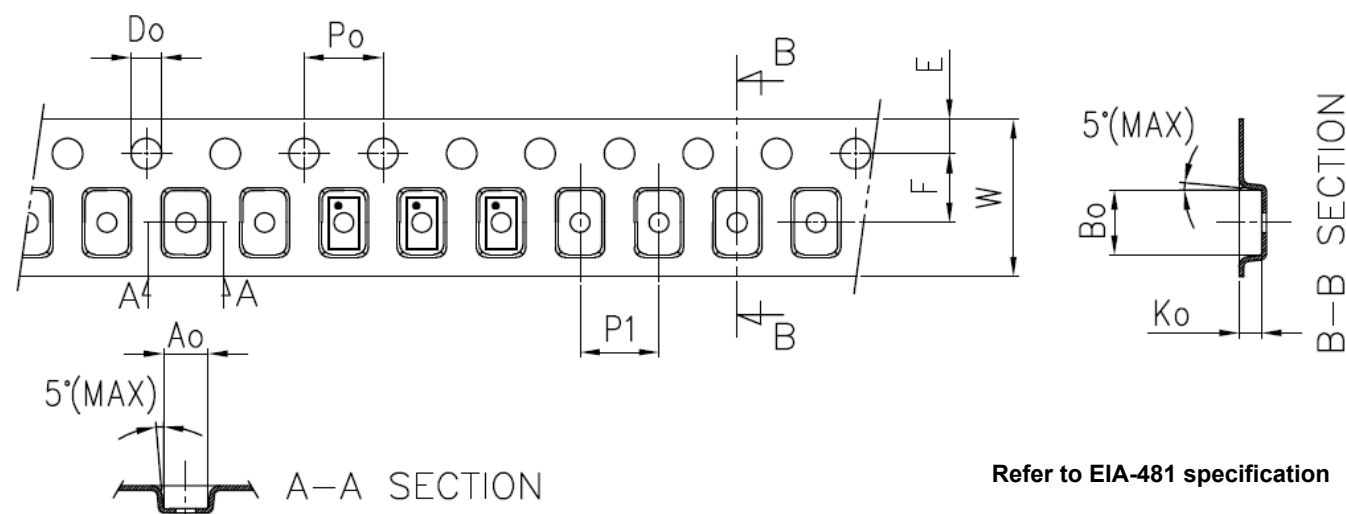
A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch  
 with  $V_{IN}$  Lockout Select and MOSFET Current Monitor Output

### Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 18L 1.6x3mm 0.4P FC Green	18	1.6 x 3 x 0.55	3,000	3,000	178 / 60	100	400	100	400	8	4

### Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 18L 1.6x3mm 0.4P FC Green	1.78	3.18	0.76	4	4	1.5	1.75	3.5	8



### Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.64 mm<sup>3</sup> (nominal). More information can be found at [www.jedec.org](http://www.jedec.org).

A 20 V, 50 mΩ, 3 A, Reverse Blocking Integrated Power Switch  
with  $V_{IN}$  Lockout Select and MOSFET Current Monitor Output

### Revision History

Date	Version	Change
12/20/2018	1.01	Updated style and formatting Updated Charts Added Layout Guidelines Fixed typos
10/19/2017	1.00	Production Release

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Dialog Semiconductor:](#)

[SLG59H1020V](#) [SLG59H1020V-EVB](#)