

SLG59H1010V

A 13.3 mΩ, 5 A Integrated Power Switch with 12 V / 24 V V_{IN} Lockout Select and MOSFET Current Monitor Output

General Description

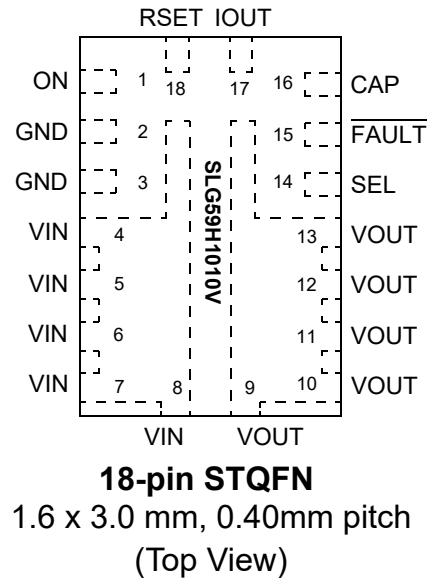
The SLG59H1010V is a high-performance 13.3 mΩ NMOS power switch designed to control 12 V or 24 V power rails up to 5 A. Using a proprietary MOSFET design, the SLG59H1010V achieves a stable 13.3 mΩ $R_{DS(ON)}$ across a wide input voltage range. In combining novel FET design and copper pillar interconnects, the SLG59H1010V package also exhibits a low thermal resistance for high-current operation.

Designed to operate over a -40 °C to 85 °C range, the SLG59H1010V is available in a low thermal resistance, RoHS-compliant, 1.6 x 3.0 mm STQFN package.

Features

- Wide Operating Input Voltage: 12 V or 24 V
- Maximum Continuous Current: 5 A
- Automatic nFET SOA Protection
- High-performance MOSFET Switch
 - Low $R_{DS(ON)}$: 13.3 mΩ at $V_{IN} = 24$ V
 - Low $\Delta R_{DS(ON)}/\Delta V_{IN}$: < 0.05 mΩ/V
 - Low $\Delta R_{DS(ON)}/\Delta T$: < 0.06 mΩ/°C
- Pin-selectable 12V/24V Input Overvoltage and Undervoltage Lockout
- Capacitor-adjustable Inrush Current Control
- Two stage Current Limit Protection:
 - Resistor-adjustable Active Current Limit
 - Internal Short-circuit Current limit
- Open Drain FAULT Signaling
- MOSFET Current Analog Output Monitor: 10 μA/A
- Fast 4 kΩ Output Discharge
 - Pb-Free / Halogen-Free / RoHS Compliant Packaging

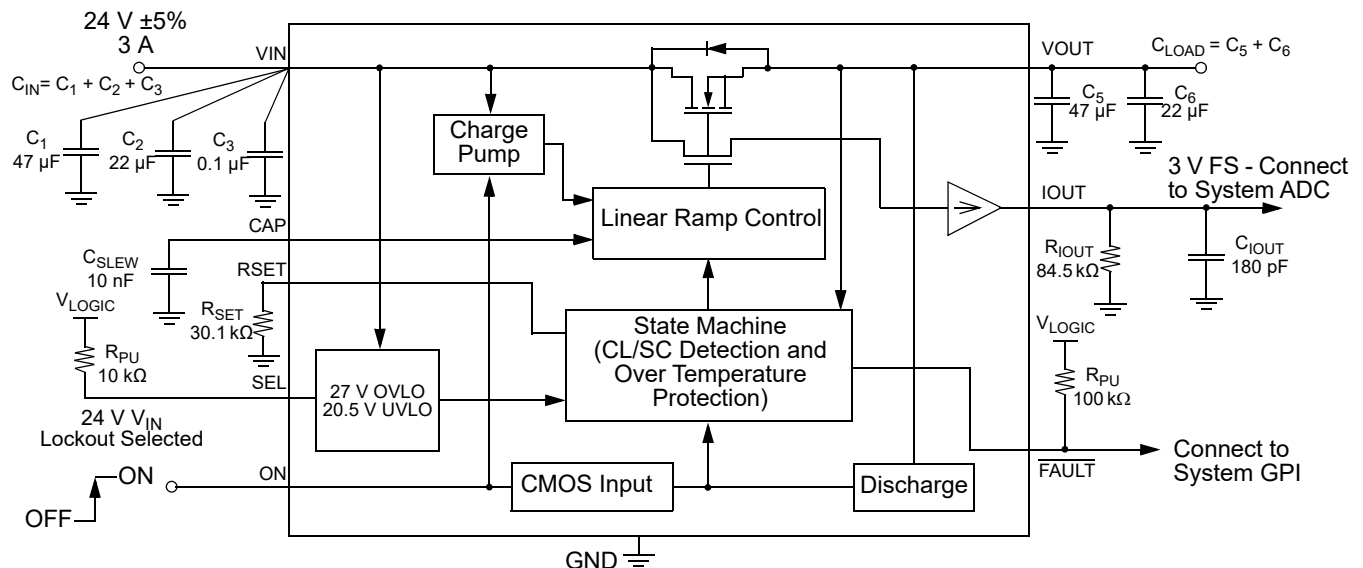
Pin Configuration



Applications

- Power-Rail Switching
- Multifunction Printers
- Large-format Copiers
- Telecommunications Equipment
- High-performance Computing
- 12 V and 24 V Point-of-Load Power Distribution
- Motor Drives

Block Diagram and 3 A Typical Application Circuit



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Pin Description

Pin #	Pin Name	Type	Pin Description
1	ON	Input	A low-to-high transition on this pin initiates the operation of the SLG59H1010V's state machine. ON is an asserted HIGH, level-sensitive CMOS input with ON_V _{IL} < 0.3 V and ON_V _{IH} > 0.9 V. As the ON pin input circuit does not have an internal pull-down resistor, connect this pin to a general-purpose output (GPO) of a microcontroller, an application processor, or a system controller, do not allow this pin to be open-circuited.
2	GND	GND	Pin 2 is a low-current GND terminal for the SLG59H1010V. Connect directly to Pin 3.
3	GND	GND	Pin 3 is the main ground connection for the SLG59H1010V's internal charge pump, its gate driver and current-limit circuits as well as its internal state machine. Therefore, use a short, stout connection from Pin 3 to the system's analog or power plane.
4-8	VIN	MOSFET	VIN supplies the power for the operation of the SLG59H1010V, its internal control circuitry, and the drain terminal of the nFET power switch. With 5 pins fused together at VIN, connect a 47 μF (or larger) low-ESR capacitor from this pin to ground. Capacitors used at VIN should be rated at 50 V or higher.
9-13	VOUT	MOSFET	Source terminal of n-channel MOSFET (5 pins fused for VOUT). Connect a 47 μF (or larger) low-ESR capacitor from this pin to ground. Capacitors used at VOUT should be rated at 50 V or higher.
14	SEL	Input	As a low logic-level CMOS input with SEL_V _{IL} < 0.3 V and SEL_V _{IH} > 1.65 V, SEL selects one of two undervoltage/overvoltage lockout windows. When SEL = LOW, the V _{IN} undervoltage/overvoltage lockout window is set for 12 V ±10% applications. When SEL = HIGH, the V _{IN} undervoltage/overvoltage lockout window is set for 24 V ± 5% applications. See the Electrical Characteristics table for additional information.
15	$\overline{\text{FAULT}}$	Output	An open drain output, $\overline{\text{FAULT}}$ is asserted within T _{FAULT} _{LOW} when a V _{IN} undervoltage, V _{IN} overvoltage, a current-limit, or an over-temperature condition is detected. $\overline{\text{FAULT}}$ is deasserted within T _{FAULT} _{HIGH} when the fault condition is removed. Connect an external resistor from the $\overline{\text{FAULT}}$ pin to local system logic supply.
16	CAP	Output	A low-ESR, stable dielectric, ceramic surface-mount capacitor connected from CAP pin to GND sets the V _{OUT} slew rate and overall turn-on time of the SLG59H1010V. For best performance, the range for C _{SLEW} values are 10 nF ≤ C _{SLEW} ≤ 20 nF – please see typical characteristics for additional information. Capacitors used at the CAP pin should be rated at 10 V or higher. Please consult Applications Section on how to select C _{SLEW} based on V _{OUT} slew rate and loading conditions.
17	IOUT	Output	IOUT is the SLG59H1010V's power MOSFET load current monitor output. As an analog current output, this signal when applied to a ground-reference resistor generates a voltage proportional to the current through the n-channel MOSFET. The I _{OUT} transfer characteristic is typically 10 μA/A with a voltage compliance range of 0.5 V ≤ V _{IOUT} ≤ 4 V. Optimal I _{OUT} linearity is exhibited for 0.5 A ≤ I _{DS} ≤ 5 A. In addition, it is recommended to bypass the IOUT pin to GND with a 0.18 nF capacitor.
18	RSET	Input	A 1%-tolerance, metal-film resistor between 18 kΩ and 91 kΩ sets the SLG59H1010V's active current limit. A 91 kΩ resistor sets the SLG59H1010V's active current limit to 1 A and a 18 kΩ resistor sets the active current limit to 5 A.

Ordering Information

Part Number	Type	Production Flow
SLG59H1010V	STQFN 18L FC	Industrial, -40 °C to 85 °C
SLG59H1010VTR	STQFN 18L FC (Tape and Reel)	Industrial, -40 °C to 85 °C

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Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V _{IN} to GND	Power Switch Input Voltage to GND	Continuous	-0.3	--	30	V
		Maximum pulsed V _{IN} , pulse width < 0.1 s	--	--	32	V
V _{OUT} to GND	Power Switch Output Voltage to GND		-0.3	--	V _{IN}	V
ON, SEL, CAP, RSET, IOUT, and FAULT to GND	ON, SEL, CAP, RSET, IOUT, and FAULT Pin Voltages to GND		-0.3	--	7	V
T _S	Storage Temperature		-65	--	150	°C
ESD _{HBM}	ESD Protection	Human Body Model	2000	--	--	V
ESD _{CDM}	ESD Protection	Charged Device Model	500	--	--	V
MSL	Moisture Sensitivity Level		1			
θ _{JA}	Thermal Resistance	1.6 x 3.0 mm 18L STQFN; Determined with the device mounted onto a 1 in ² , 1 oz. copper pad of FR-4 material	--	40	--	°C/W
MOSFET IDS _{CONT}	Continuous Current from VIN to VOUT	T _J < 150 °C	--	--	5	A
MOSFET IDS _{PEAK}	Peak Current from VIN to VOUT	Maximum pulsed switch current, pulse width < 1 ms	--	--	6	A

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

12 V ≤ V_{IN} ≤ 24 V; C_{IN} = 47 μF, T_A = -40 °C to 85 °C, unless otherwise noted. Typical values are at T_A = 25 °C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V _{IN}	Operating Input Voltage		10.8	--	25.2	V
V _{IN(OVLO)}	V _{IN} Overvoltage Lockout Threshold	V _{IN} ↑; SEL = HIGH	25.3	27	28.5	V
		V _{IN} ↑; SEL = LOW	13.3	13.7	14.5	V
V _{IN(UVLO)}	V _{IN} Undervoltage Lockout Threshold	V _{IN} ↓; SEL = HIGH	19.5	20.5	21.5	V
		V _{IN} ↓; SEL = LOW	9.7	10.2	10.7	V
I _Q	Quiescent Supply Current	ON = HIGH; I _{DS} = 0 A	--	0.5	0.6	mA
I _{SHDN}	OFF Mode Supply Current	ON = LOW; I _{DS} = 0 A	--	1	3	μA
RDS _{ON}	ON Resistance	T _A = 25 °C; I _{DS} = 0.1 A	--	13.3	14.5	mΩ
		T _A = 85 °C; I _{DS} = 0.1 A	--	17.2	18	mΩ
MOSFET IDS	Current from VIN to VOUT	Continuous	--	--	5	A
I _{LIMIT}	Active Current Limit, I _{ACL}	V _{OUT} > 0.5 V; R _{SET} = 30.1 kΩ	3.0	3.19	3.5	A
	Short-circuit Current Limit, I _{SCL}	V _{OUT} < 0.5 V	--	0.5	-	A
T _{ACL}	Active Current Limit Response Time	R _{SET} = 51.6 kΩ	--	120	--	μs
R _{DISCHRG}	Output Discharge Resistance		3.5	4.4	5.3	kΩ
I _{OUT}	MOSFET Current Analog Monitor Output	I _{DS} = 1 A	9.3	10	10.9	μA
		I _{DS} = 3 A	28.5	30	31.7	μA

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Electrical Characteristics (continued)

12 V ≤ V_{IN} ≤ 24 V; C_{IN} = 47 μF, T_A = -40 °C to 85 °C, unless otherwise noted. Typical values are at T_A = 25 °C

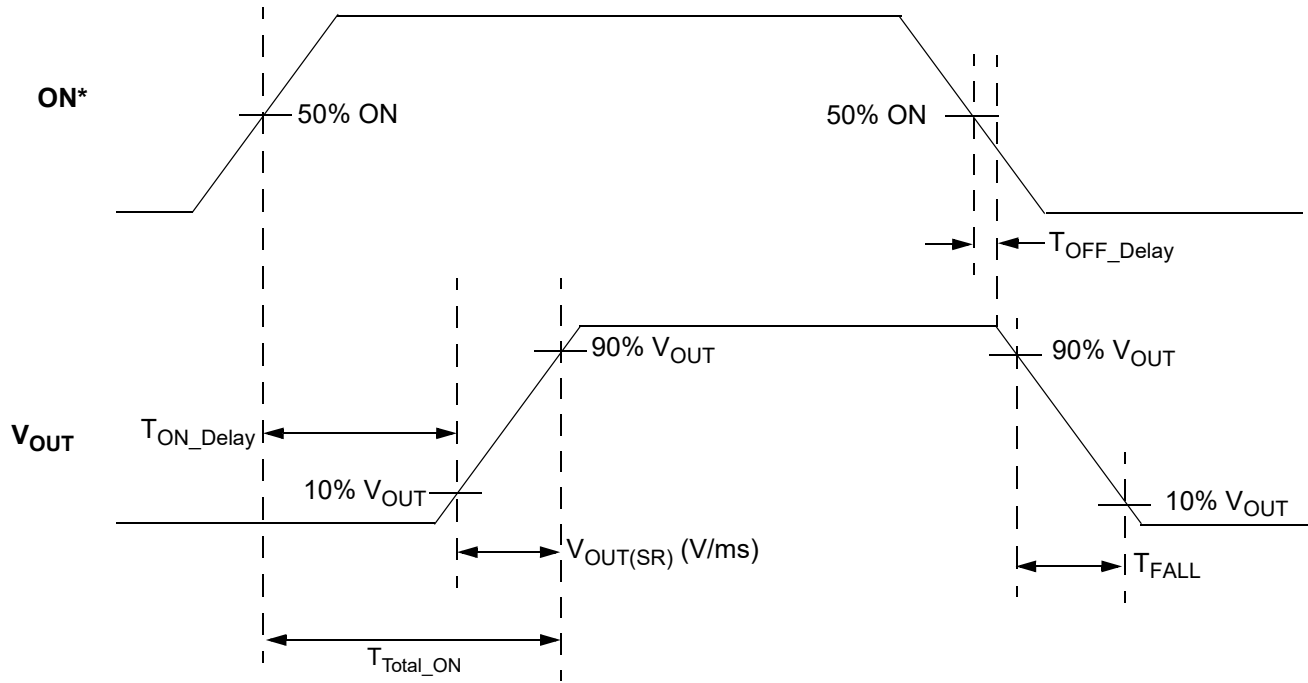
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
T _{IOUT}	I _{OUT} Response Time to Change in Main MOSFET Current	C _{IOUT} = 180 pF; Step load 0 to 2.4 A; 0% to 90% I _{OUT}	--	45	--	μs
C _{LOAD}	Output Load Capacitance	C _{LOAD} connected from V _{OUT} to GND	--	47	--	μF
T _{ON_Delay}	ON Delay Time	50% ON to 10% V _{OUT} ↑; V _{IN} = 12 V; C _{SLEW} = 10 nF; R _{LOAD} = 100 Ω, C _{LOAD} = 10 μF	480	600	720	μs
		50% ON to 10% V _{OUT} ↑; V _{IN} = 24 V; C _{SLEW} = 10 nF; R _{LOAD} = 100 Ω, C _{LOAD} = 10 μF	0.8	1.0	1.2	ms
T _{Total_ON}	Total Turn ON Time	50% ON to 90% V _{OUT} ↑	Set by External C _{SLEW} ¹			ms
		50% ON to 90% V _{OUT} ↑; V _{IN} = 12 V; C _{SLEW} = 10 nF; R _{LOAD} = 100 Ω, C _{LOAD} = 10 μF	2.9	3.6	4.3	ms
		50% ON to 90% V _{OUT} ↑; V _{IN} = 24 V; C _{SLEW} = 10 nF; R _{LOAD} = 100 Ω, C _{LOAD} = 10 μF	5.7	7.1	8.5	ms
V _{OUT(SR)}	V _{OUT} Slew rate	10% V _{OUT} to 90% V _{OUT} ↑	Set by External C _{SLEW} ¹			V/ms
		10% V _{OUT} to 90% V _{OUT} ↑; V _{IN} = 12 V or 24 V; C _{SLEW} = 10 nF; R _{LOAD} = 100 Ω, C _{LOAD} = 10 μF	2.7	3.2	3.9	V/ms
T _{OFF_Delay}	OFF Delay Time	50% ON to V _{OUT} Fall Start ↓; V _{IN} = 12 V or 24 V; R _{LOAD} = 100 Ω, No C _{LOAD}	--	15	--	μs
T _{FALL}	V _{OUT} Fall Time	90% V _{OUT} to 10% V _{OUT} ; ON = HIGH-to-LOW; V _{IN} = 12 V or 24 V; R _{LOAD} = 100 Ω, No C _{LOAD}	10.4	12.7	15	μs
T _{FAULT_LOW}	FAULT Assertion Time	Abnormal Step Load Current event to FAULT ↓; I _{ACL} = 1 A; V _{IN} = 24 V; R _{SET} = 91 kΩ; switch in 20 Ω load	--	80	--	μs
T _{FAULT_HIGH}	FAULT De-assertion Time	Delay to FAULT ↑ after fault condition is removed; I _{ACL} = 1 A; V _{IN} = 24 V; R _{SET} = 91 kΩ; switch out 20 Ω load	--	180	--	μs
FAULT _{VOL}	FAULT Output Low Voltage	I _{FAULT} = 1 mA	--	0.2	--	V
ON_V _{IH}	ON Pin Input High Voltage		0.9	--	5	V
ON_V _{IL}	ON Pin Input Low Voltage		-0.3	0	0.3	V
SEL_V _{IH}	SEL pin Input High Voltage		1.65	--	4.5	V
SEL_V _{IL}	SEL pin Input Low Voltage		-0.3	--	0.3	V
I _{ON(Leakage)}	ON Pin Leakage Current	1 V ≤ ON ≤ 5 V or ON = GND	--	--	1	μA
THERM _{ON}	Thermal Protection Shutdown Threshold		--	125	--	°C
THERM _{OFF}	Thermal Protection Restart Threshold		--	100	--	°C

Notes:

1. Refer to typical Timing Parameter vs. C_{SLEW} performance charts for additional information.

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T_{Total_ON} , T_{ON_Delay} and Slew Rate Measurement

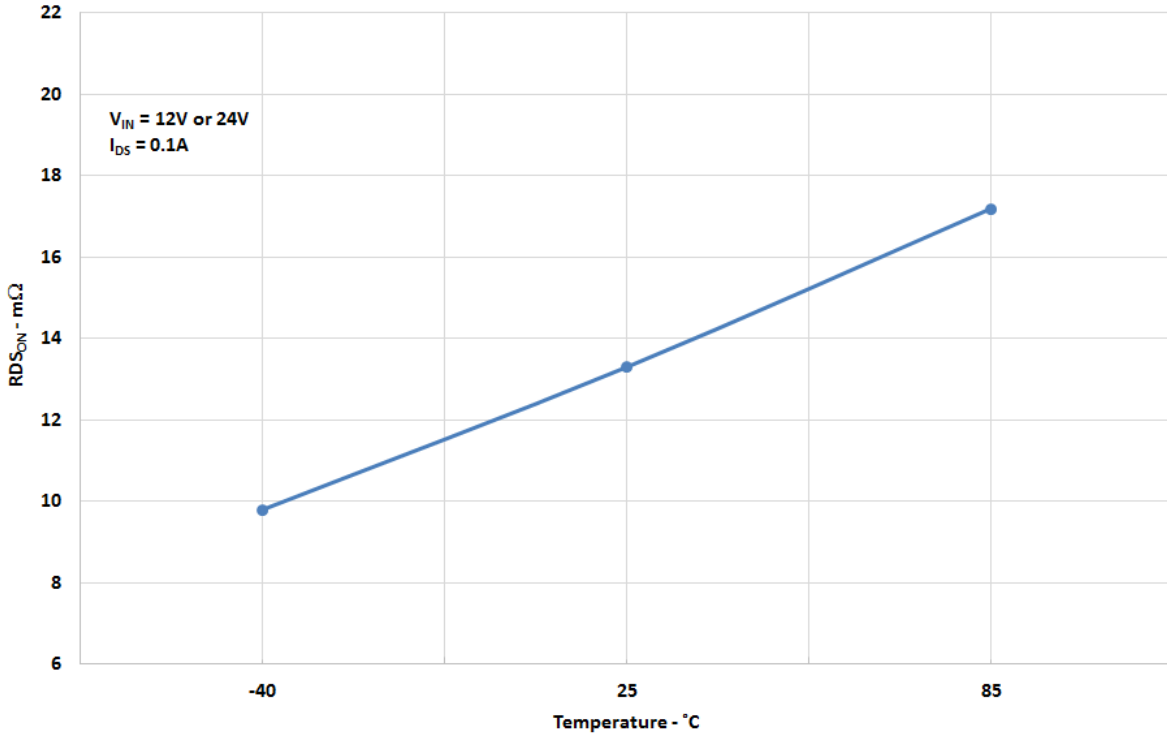


*Rise and Fall Times of the ON Signal are 100 ns

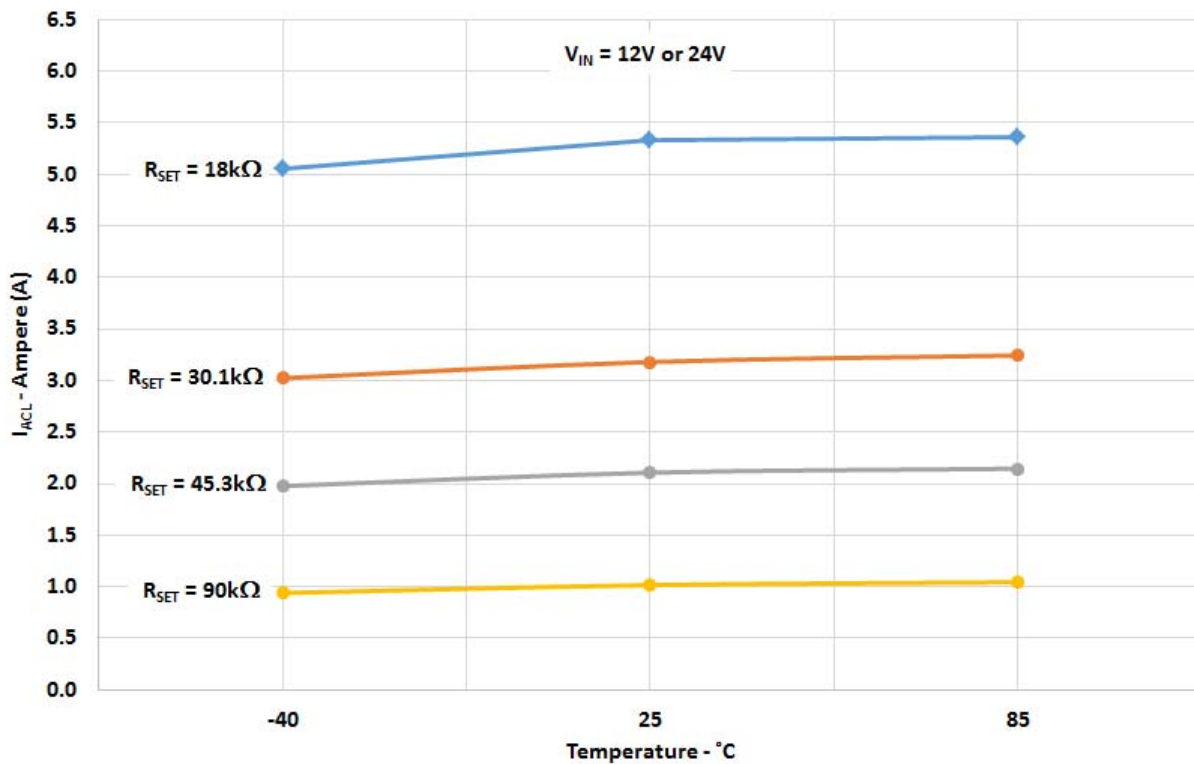
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Typical Performance Characteristics

$R_{DS(ON)}$ vs. Temperature and V_{IN}

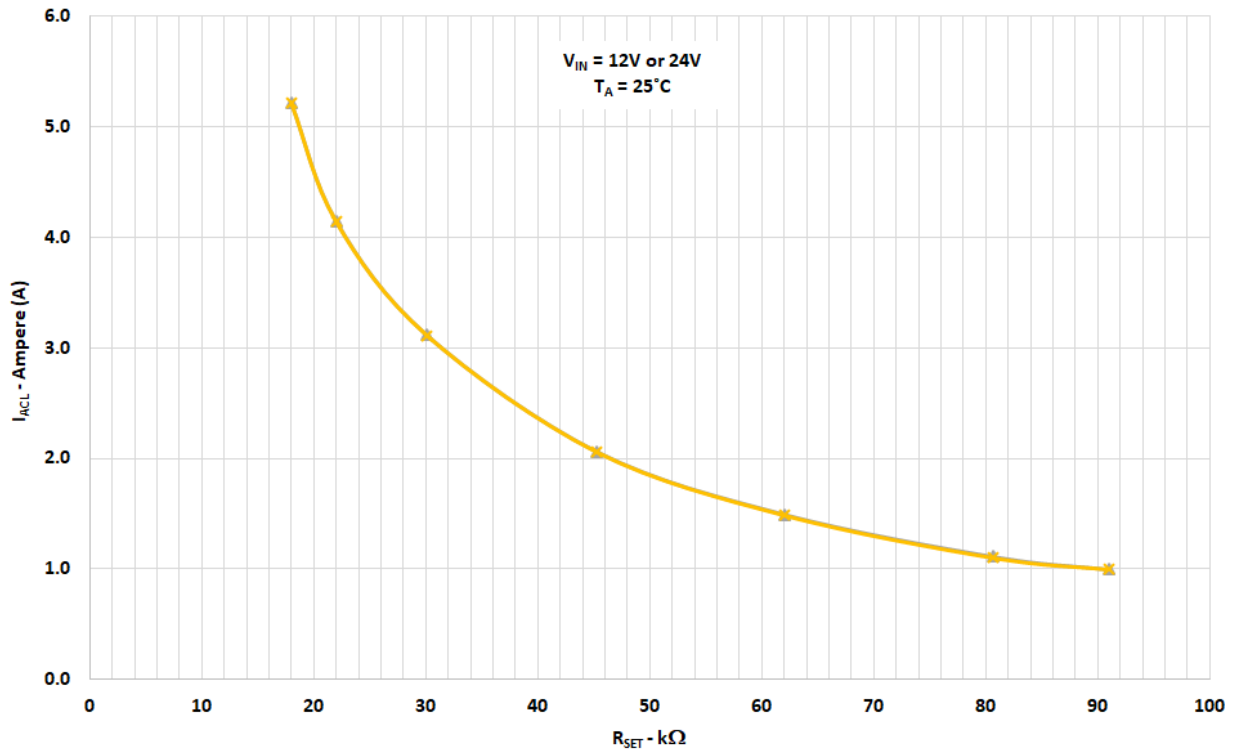


I_{ACL} vs. Temperature and R_{SET}

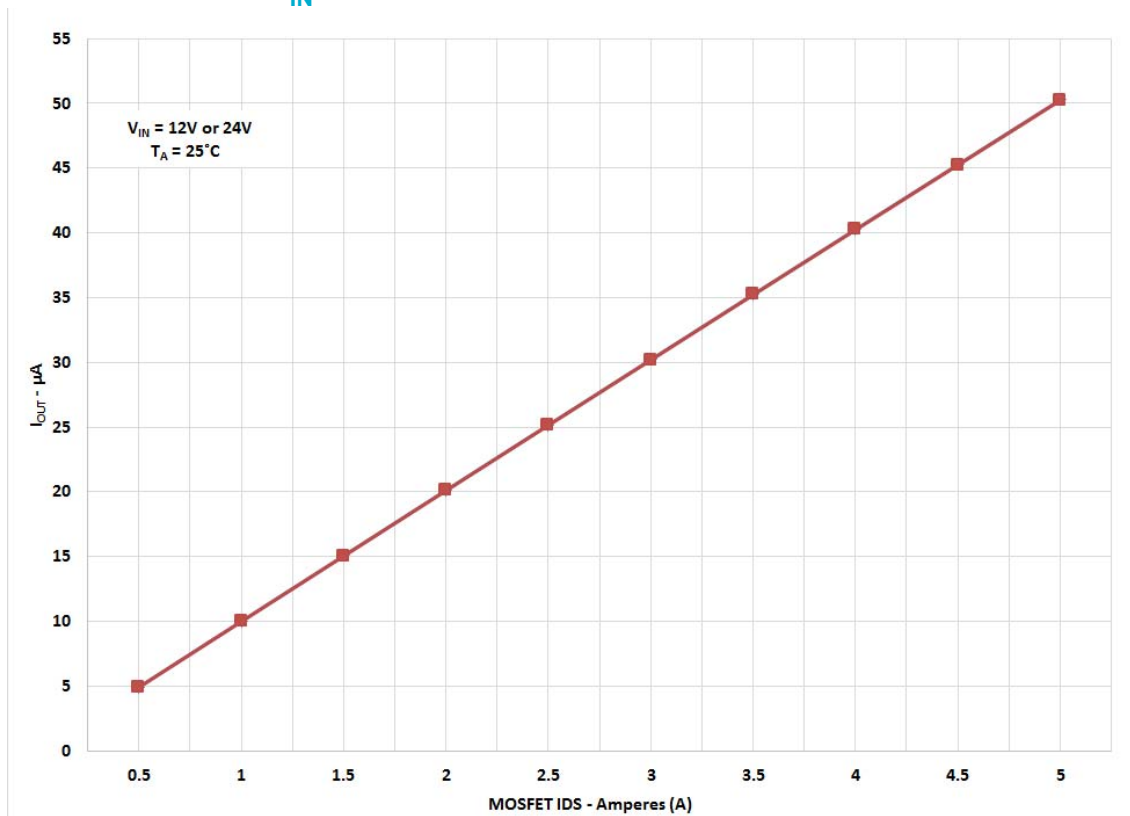


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I_{ACL} vs. R_{SET} and V_{IN}

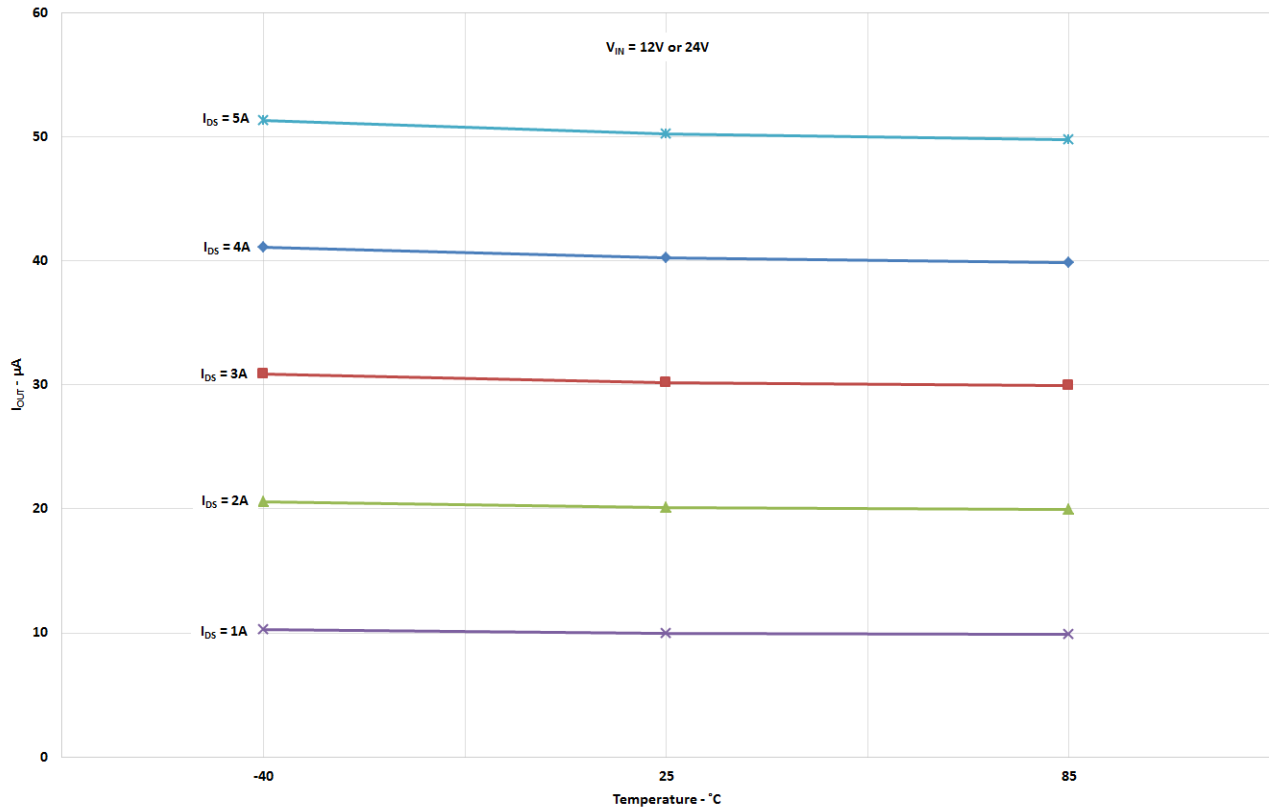


I_{OUT} vs. MOSFET I_{DS} and V_{IN}

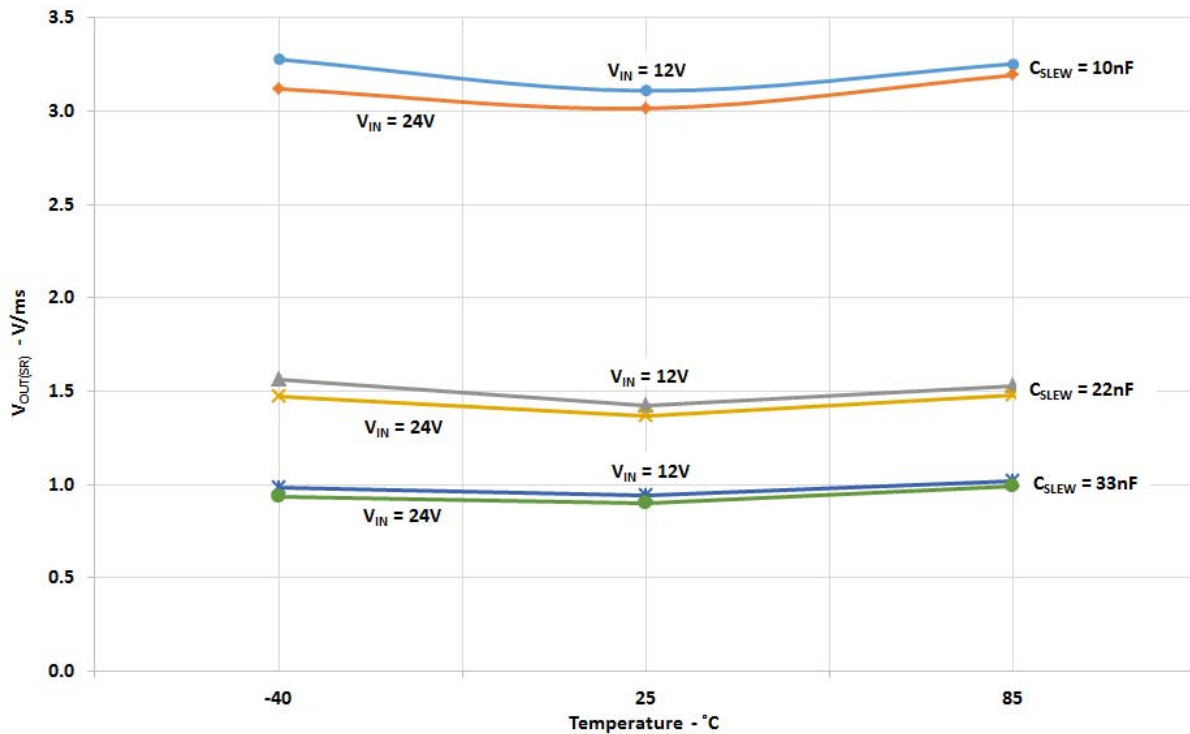


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I_{OUT} vs. Temperature and MOSFET I_{DS}

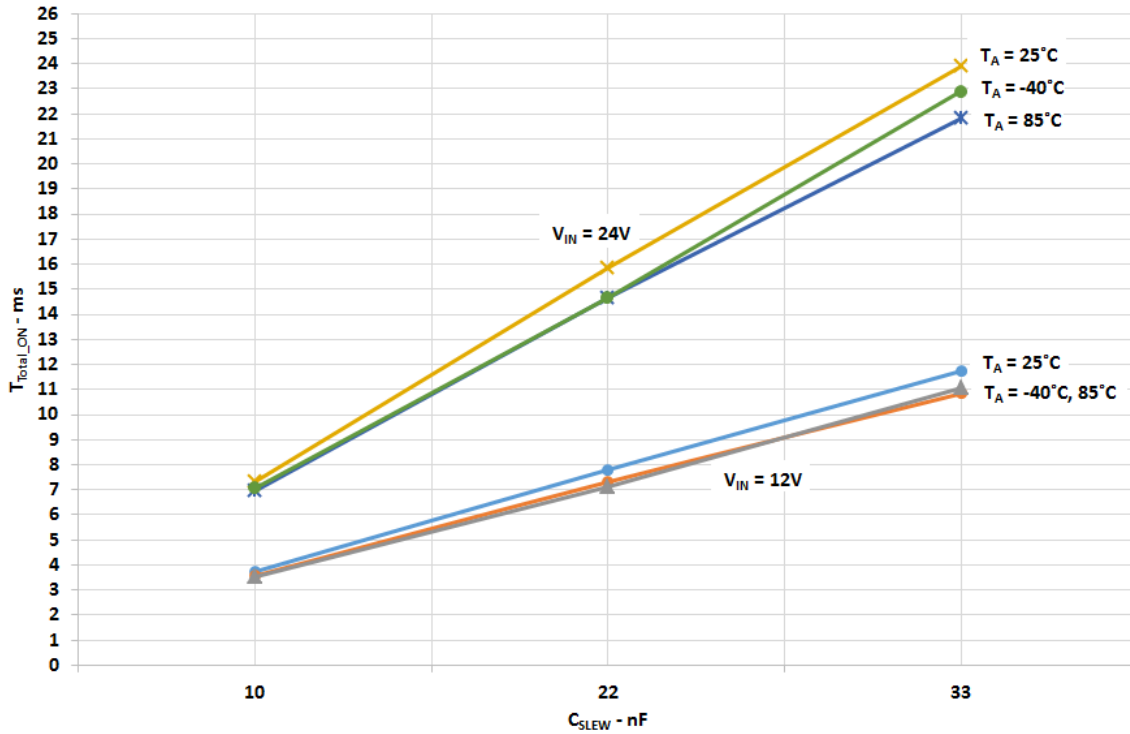


V_{OUT} Slew Rate vs. Temperature, V_{IN} , and C_{SLEW}

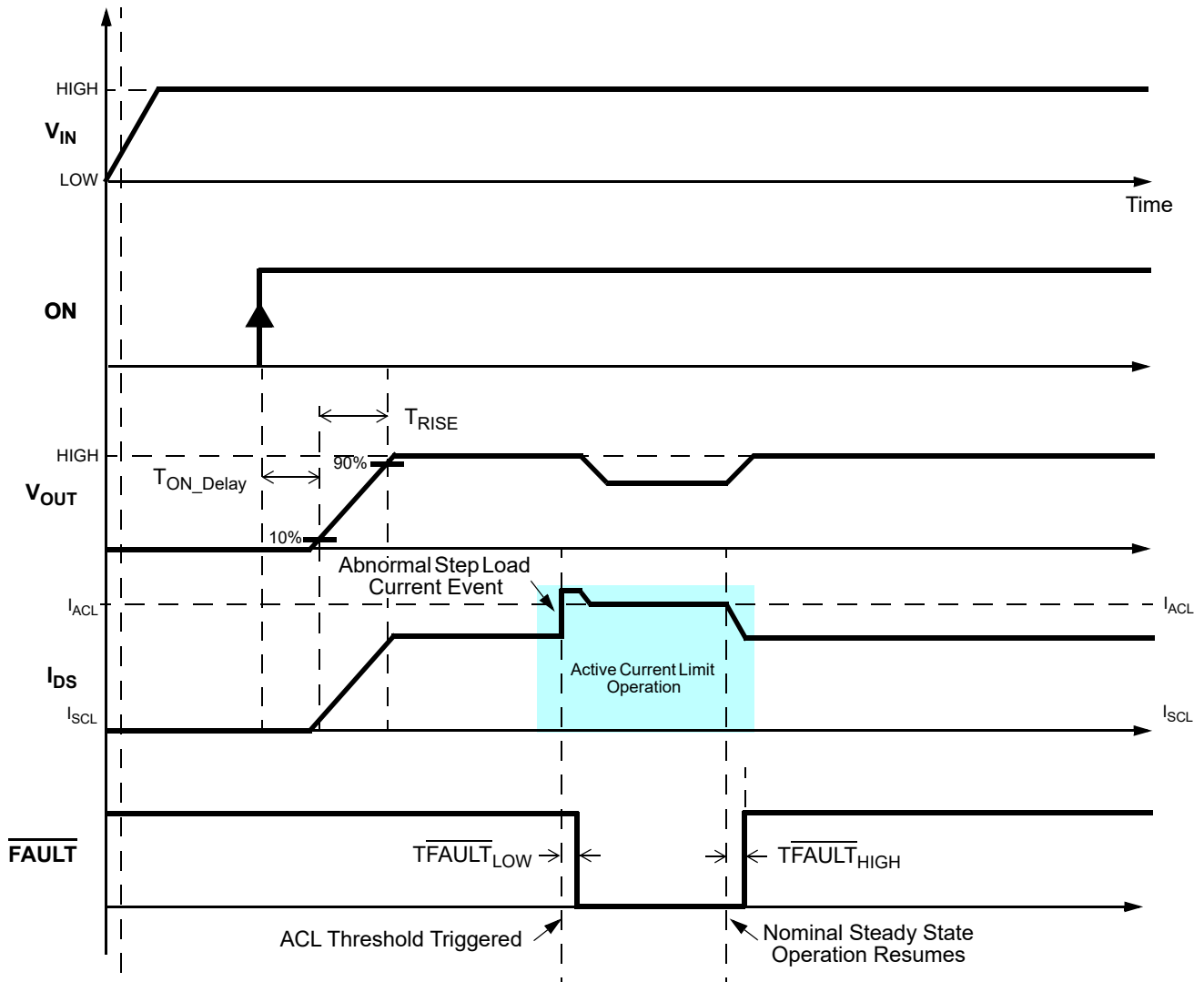


A 13.3 mΩ, 5 A Integrated Power Switch with 12 V / 24 V
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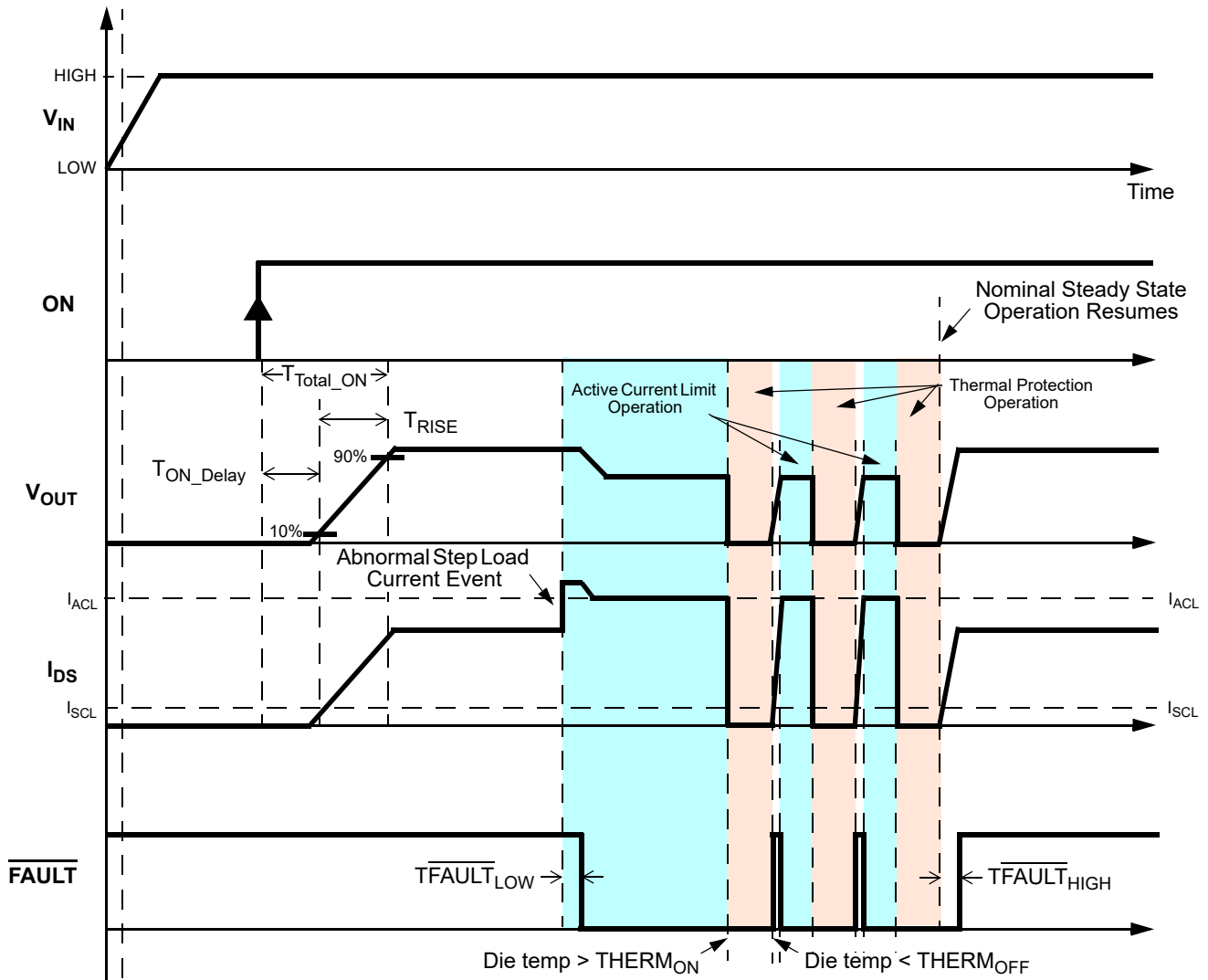
T_{Total_ON} vs. C_{SLEW} , V_{IN} , and Temperature



Timing Diagram - Basic Operation including Active Current Limit Protection

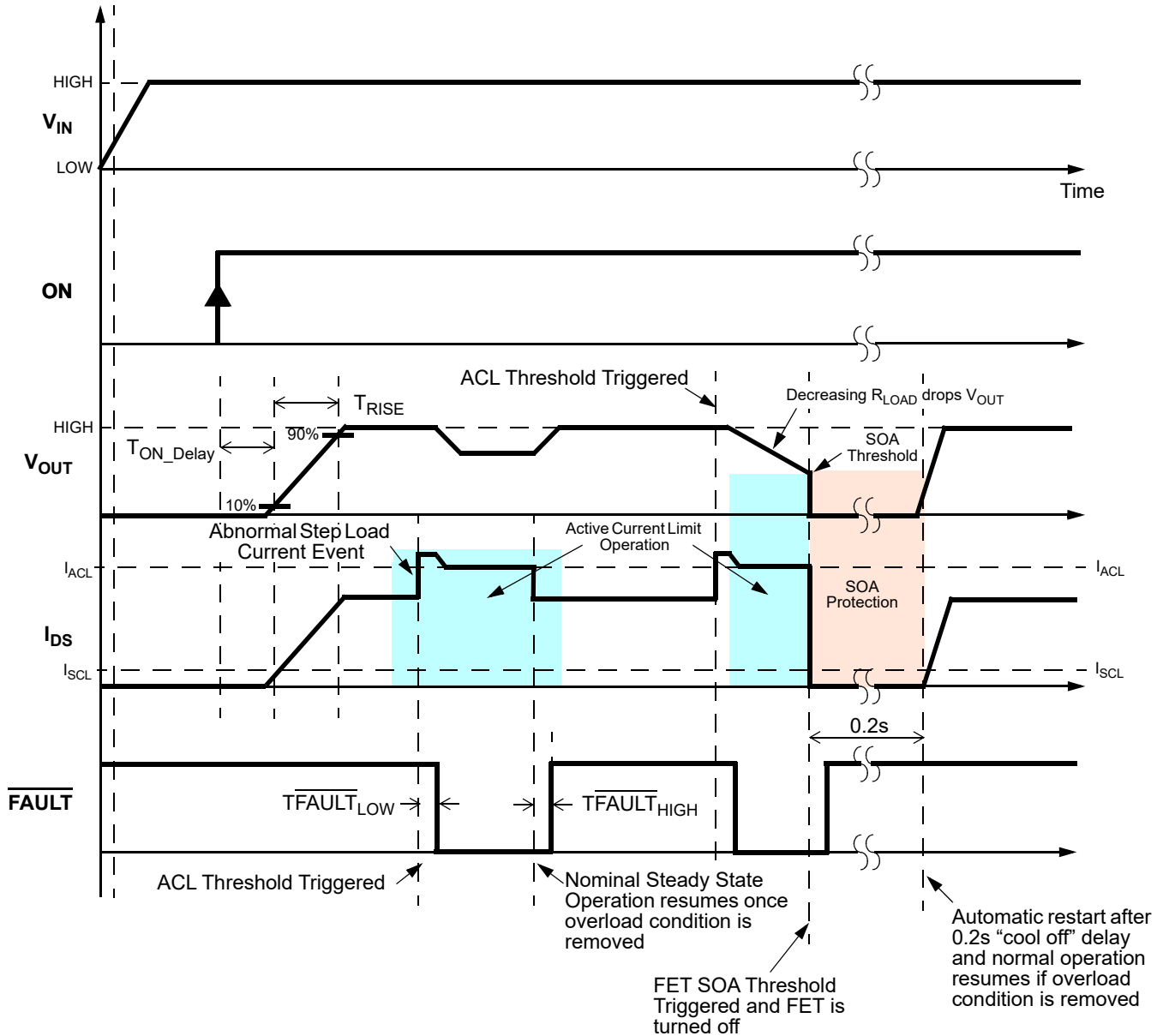


Timing Diagram - Active Current Limit & Thermal Protection Operation



A 13.3 mΩ, 5 A Integrated Power Switch with 12 V / 24 V
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Timing Diagram - Basic Operation including Active Current + Internal FET SOA Protection



A 13.3 mΩ, 5 A Integrated Power Switch with 12 V / 24 V
 V_{IN} Lockout Select and MOSFET Current Monitor Output

SLG59H1010V Application Diagram

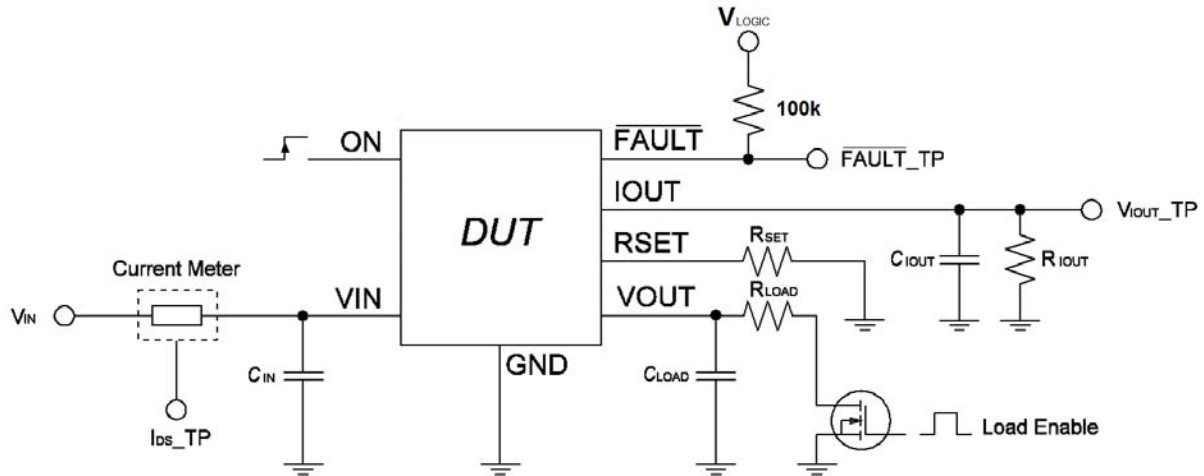


Figure 1. Test setup Application Diagram

Typical Turn-on Waveforms

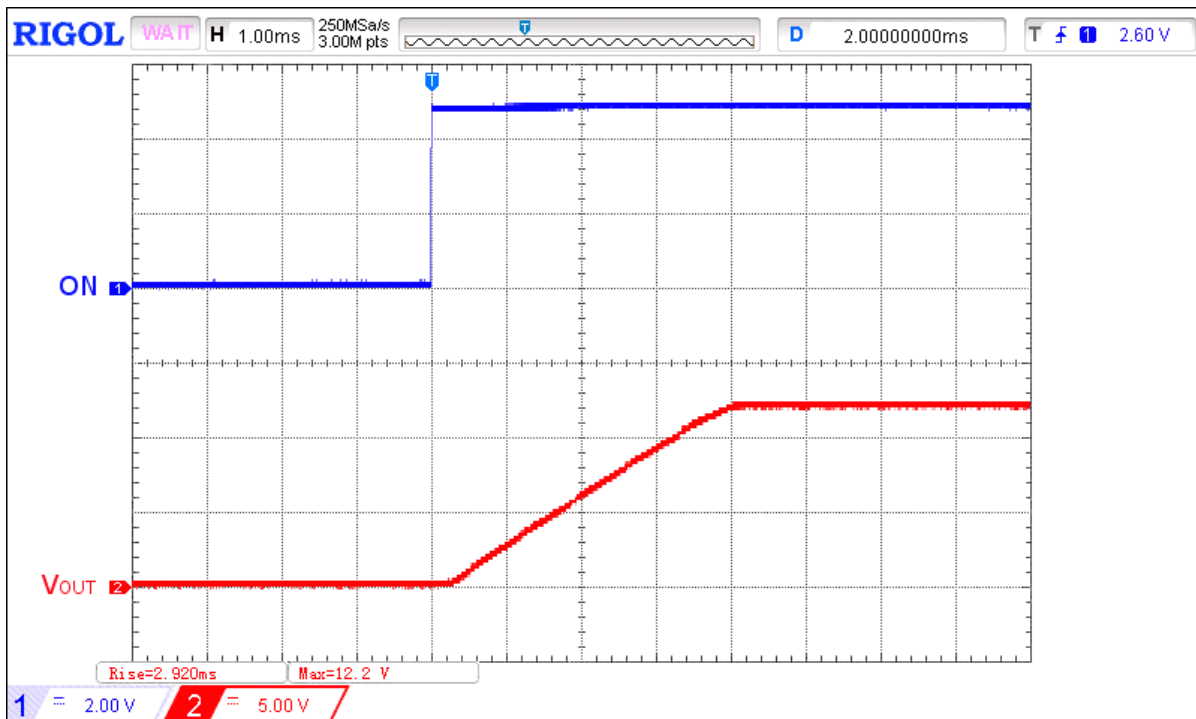


Figure 2. Typical Turn ON operation waveform for $V_{IN} = 12\text{ V}$, $C_{SLEW} = 10\text{ nF}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{LOAD} = 100\text{ }\Omega$

A 13.3 mΩ, 5 A Integrated Power Switch with 12 V / 24 V
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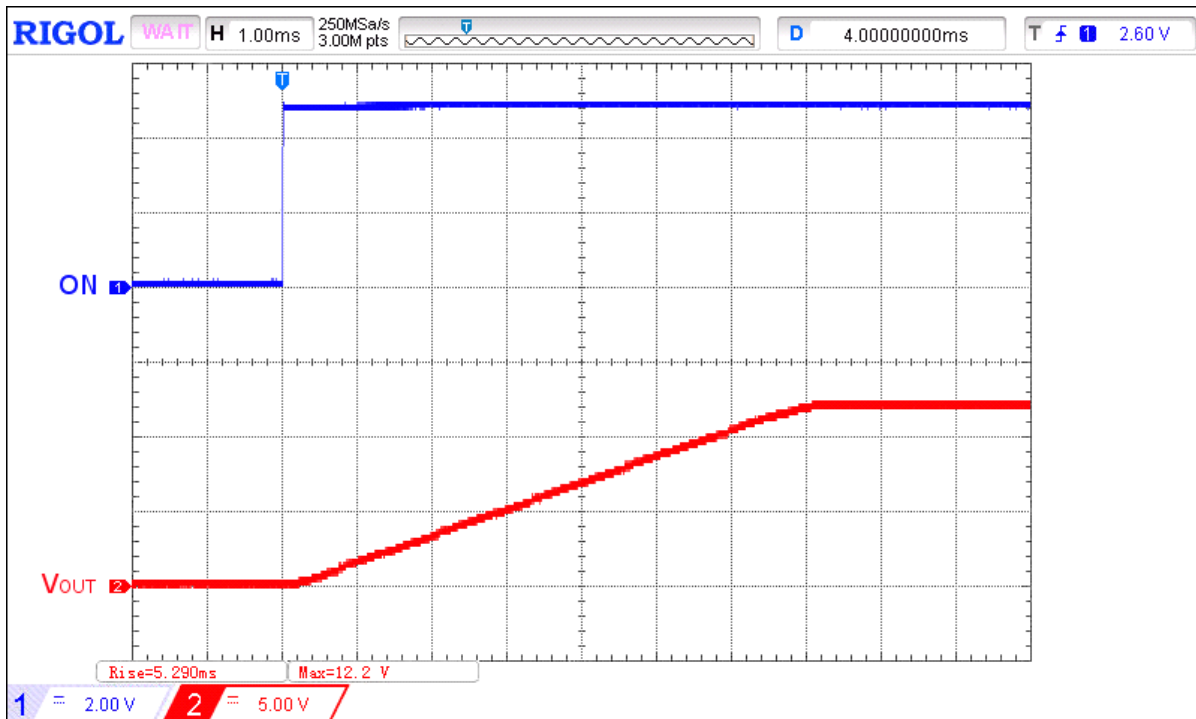


Figure 3. Typical Turn ON operation waveform for $V_{IN} = 12\text{ V}$, $C_{SLEW} = 18\text{ nF}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{LOAD} = 100\text{ }\Omega$

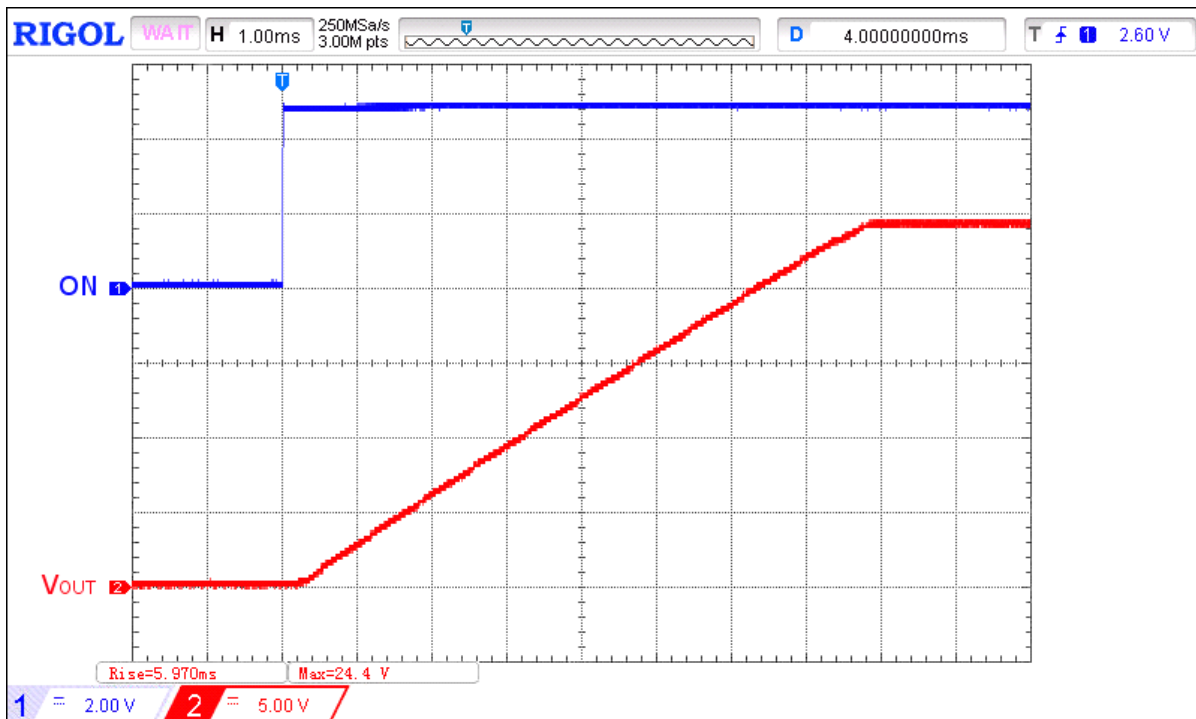


Figure 4. Typical Turn ON operation waveform for $V_{IN} = 24\text{ V}$, $C_{SLEW} = 10\text{ nF}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{LOAD} = 100\text{ }\Omega$

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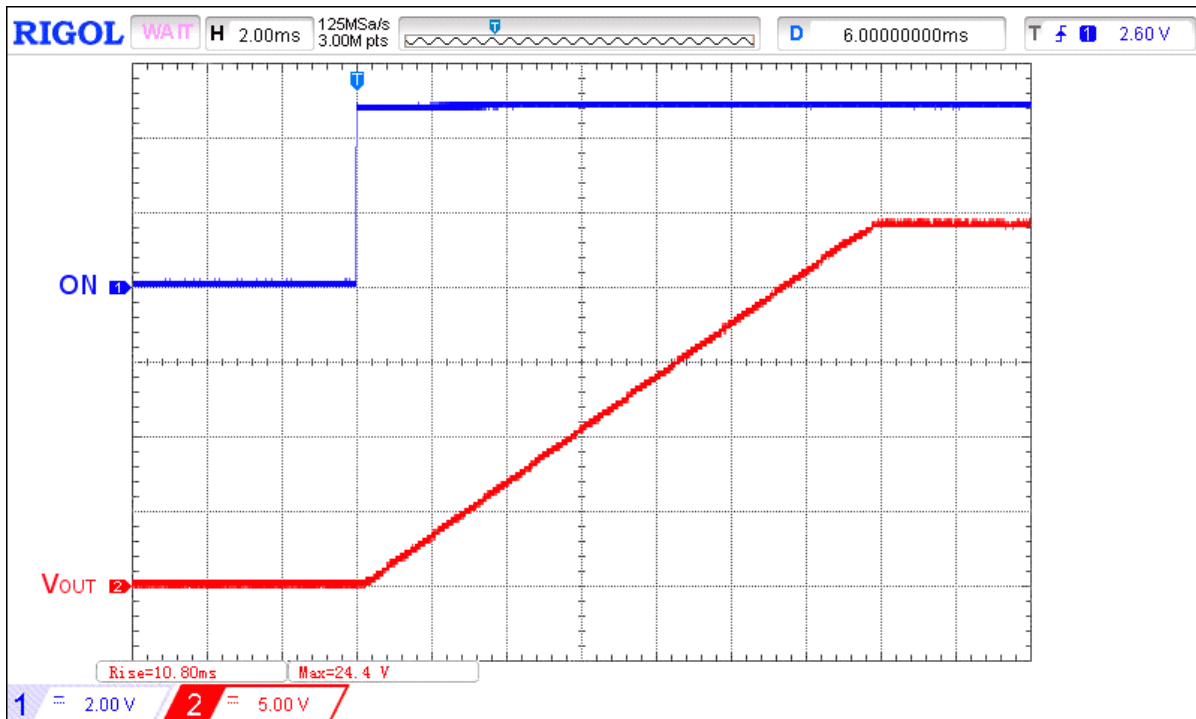


Figure 5. Typical Turn ON operation waveform for $V_{IN} = 24\text{ V}$, $C_{SLEW} = 18\text{ nF}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{LOAD} = 100\text{ }\Omega$

Typical Turn-off Waveforms

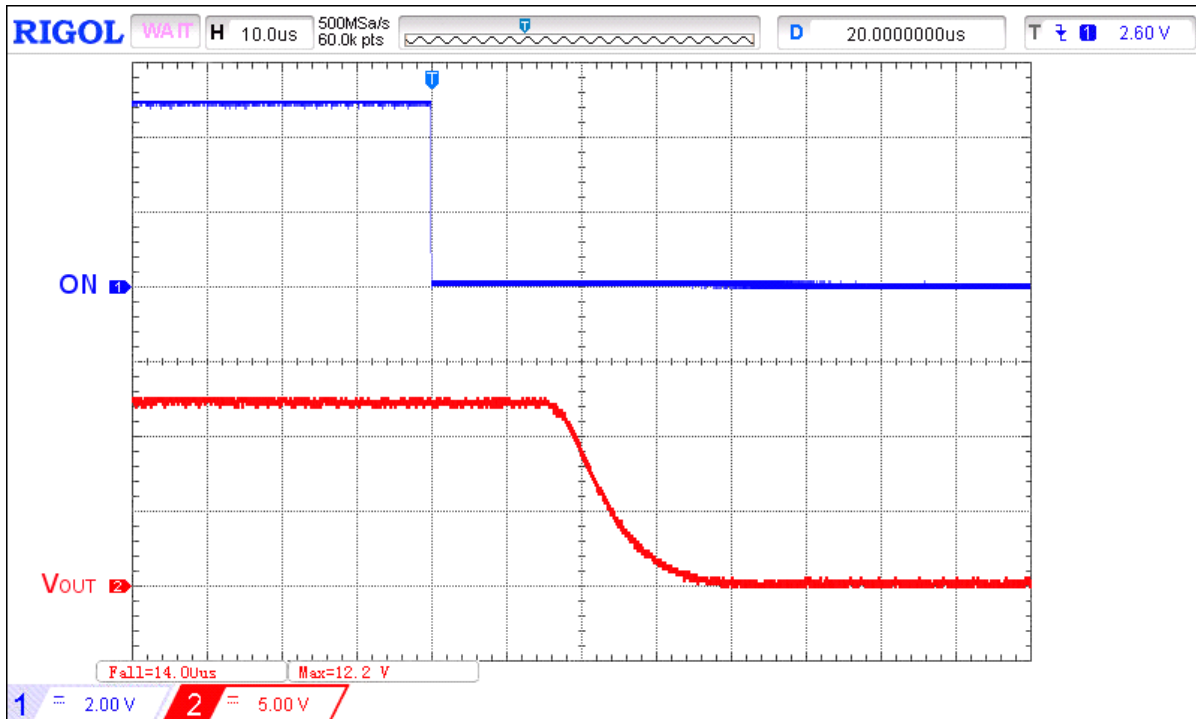


Figure 6. Typical Turn OFF operation waveform for $V_{IN} = 12\text{ V}$, $C_{SLEW} = 10\text{ nF}$, no C_{LOAD} , $R_{LOAD} = 100\text{ }\Omega$

A 13.3 mΩ, 5 A Integrated Power Switch with 12 V / 24 V
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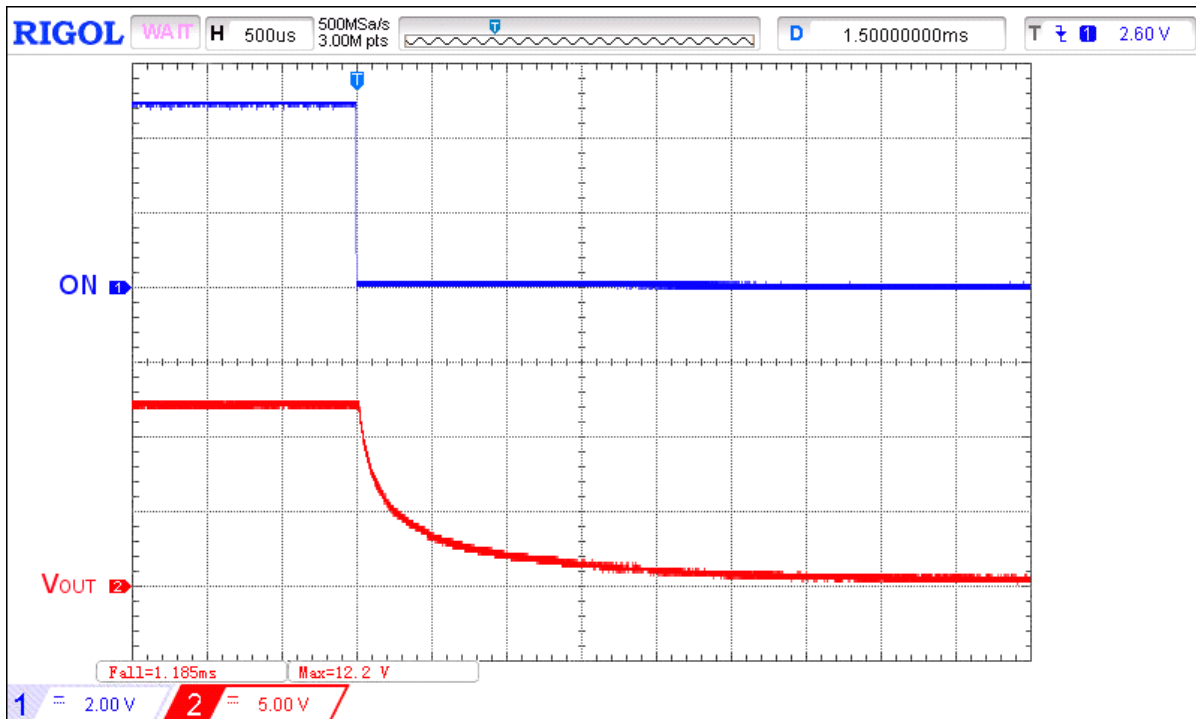


Figure 7. Typical Turn OFF operation waveform for $V_{IN} = 12V$, $C_{SLEW} = 10\text{ nF}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{LOAD} = 100\text{ }\Omega$

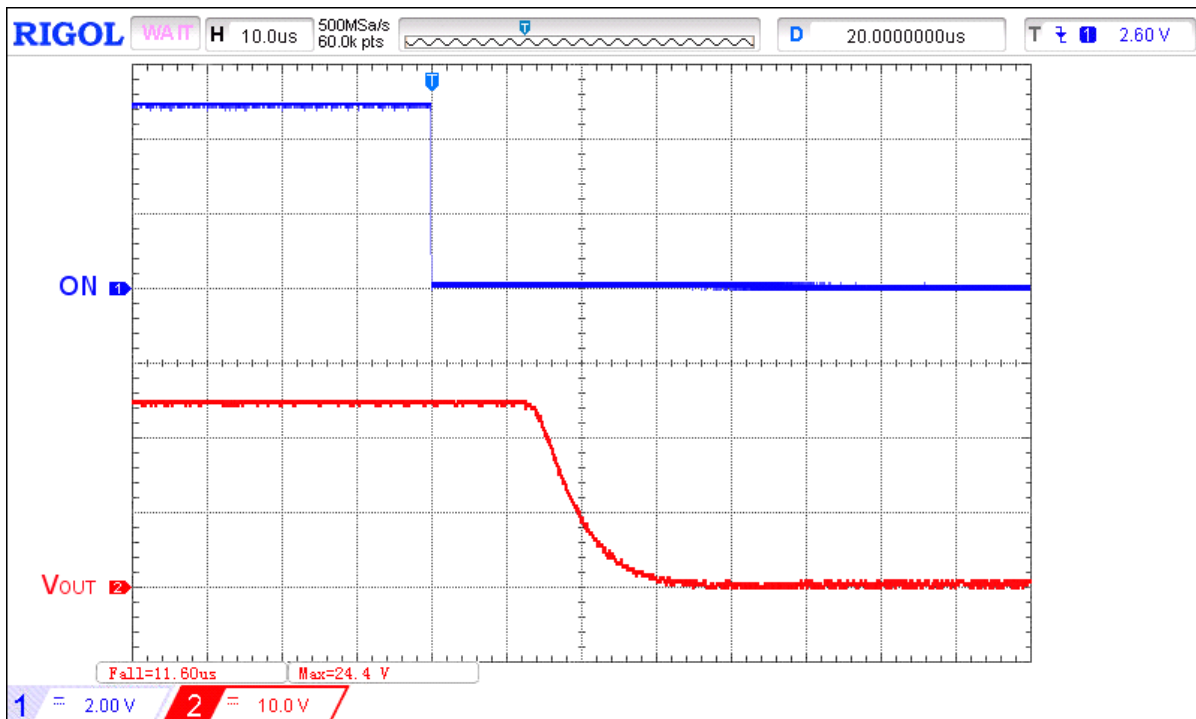


Figure 8. Typical Turn OFF operation waveform for $V_{IN} = 24\text{ V}$, $C_{SLEW} = 10\text{ nF}$, no C_{LOAD} , $R_{LOAD} = 100\text{ }\Omega$

A 13.3 mΩ, 5 A Integrated Power Switch with 12 V / 24 V
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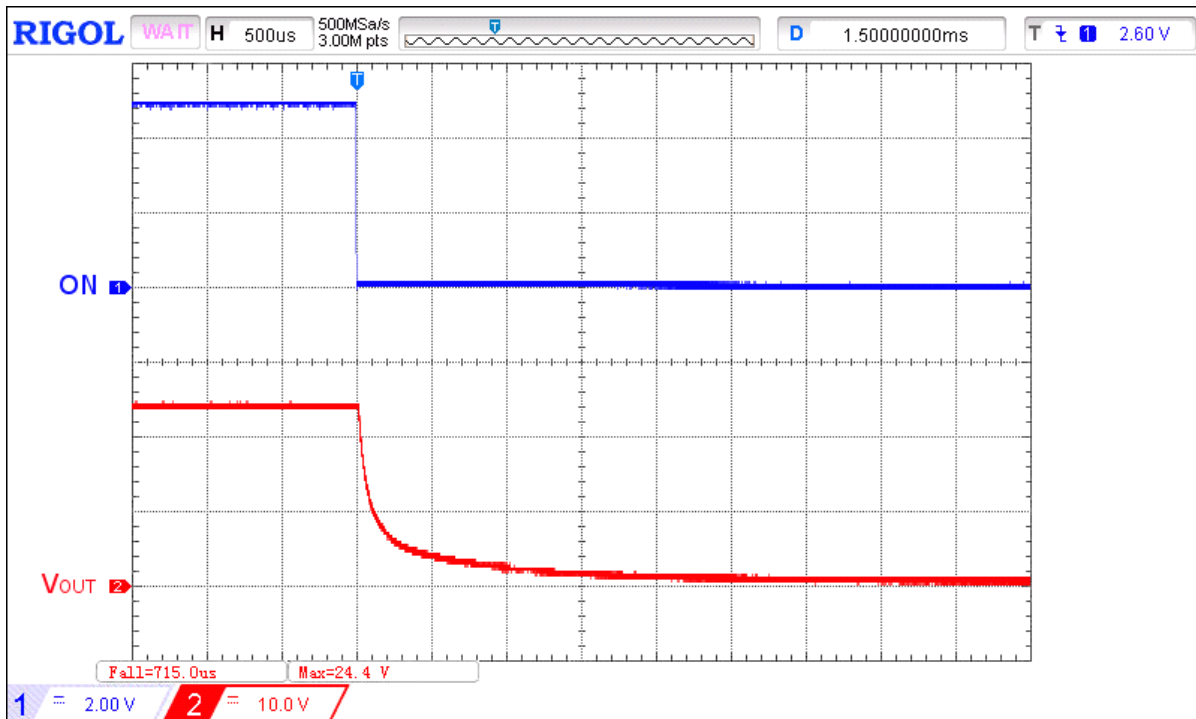


Figure 9. Typical Turn OFF operation waveform for $V_{IN} = 24\text{ V}$, $C_{SLEW} = 10\text{ nF}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{LOAD} = 100\text{ }\Omega$

Typical ACL Operation Waveforms

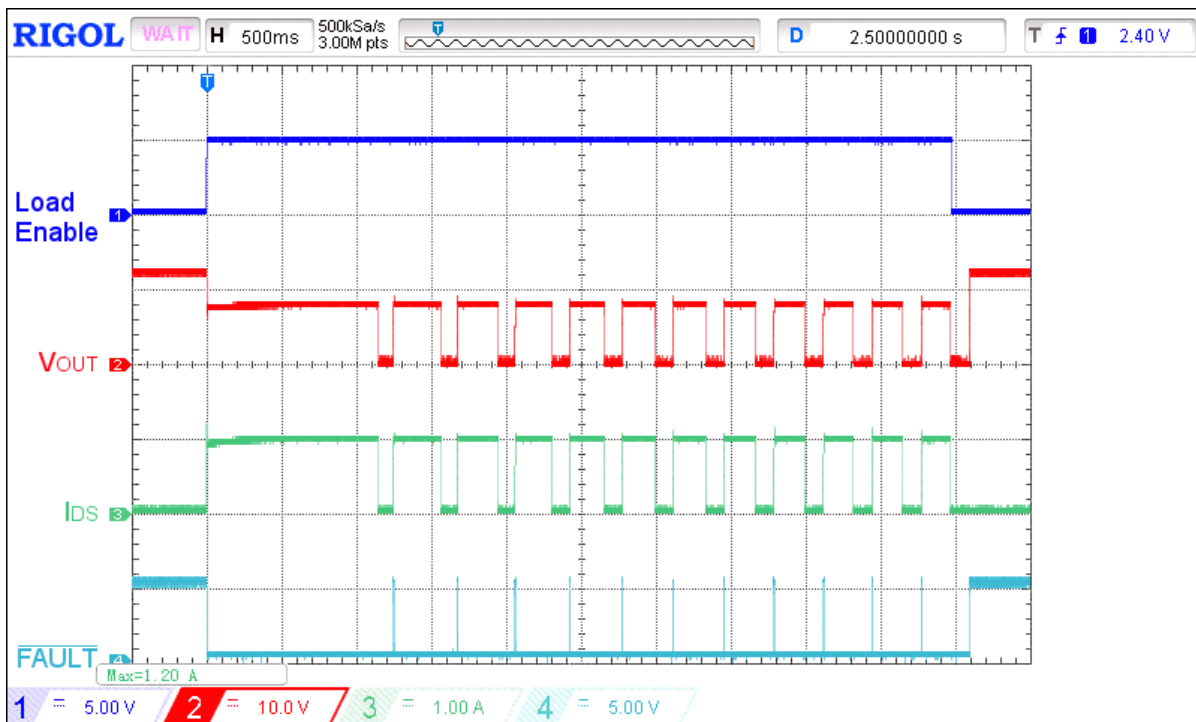


Figure 10. Typical ACL operation waveform for $V_{IN} = 12\text{ V}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $I_{ACL} = 1\text{ A}$, $R_{SET} = 91\text{ k}\Omega$

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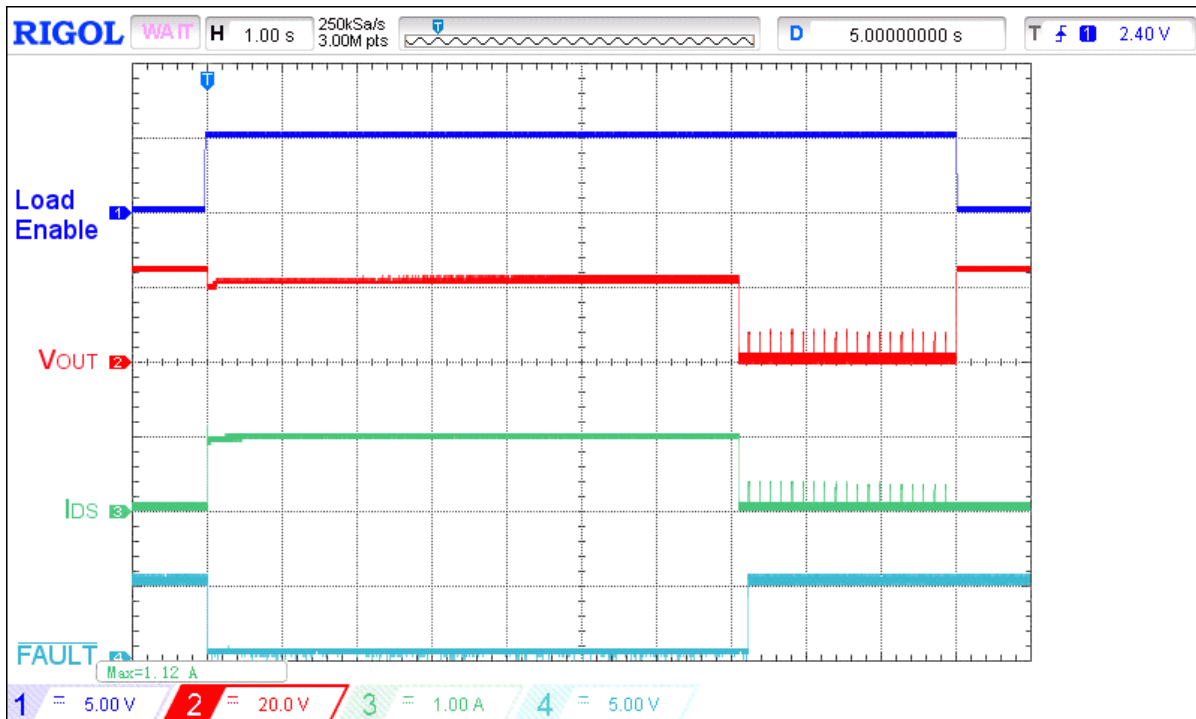


Figure 11. Thermally induced SOA shutdown for $V_{IN} = 24\text{ V}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $I_{ACL} = 1\text{ A}$, $R_{SET} = 91\text{ k}\Omega$

Typical FAULT Operation Waveforms

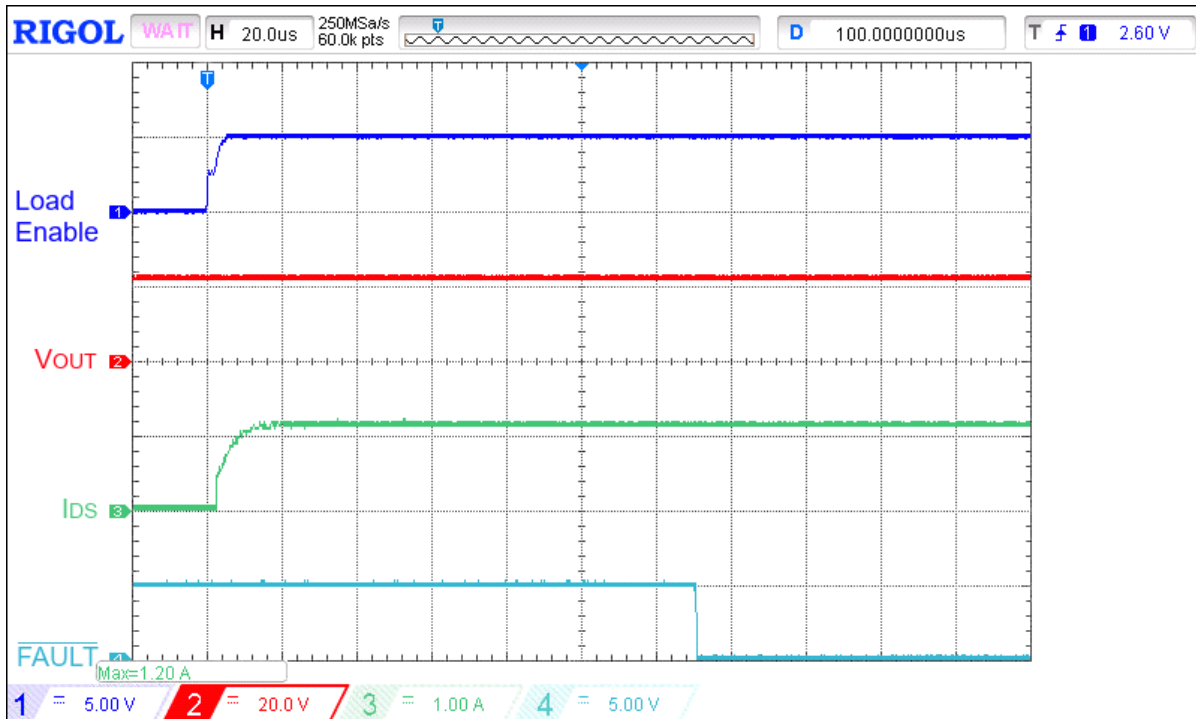


Figure 12. Typical FAULT assertion waveform for $V_{IN} = 24\text{ V}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $I_{ACL} = 1\text{ A}$, $R_{SET} = 91\text{ k}\Omega$, switch on $18.5\text{ }\Omega$ load

A 13.3 mΩ, 5 A Integrated Power Switch with 12 V / 24 V
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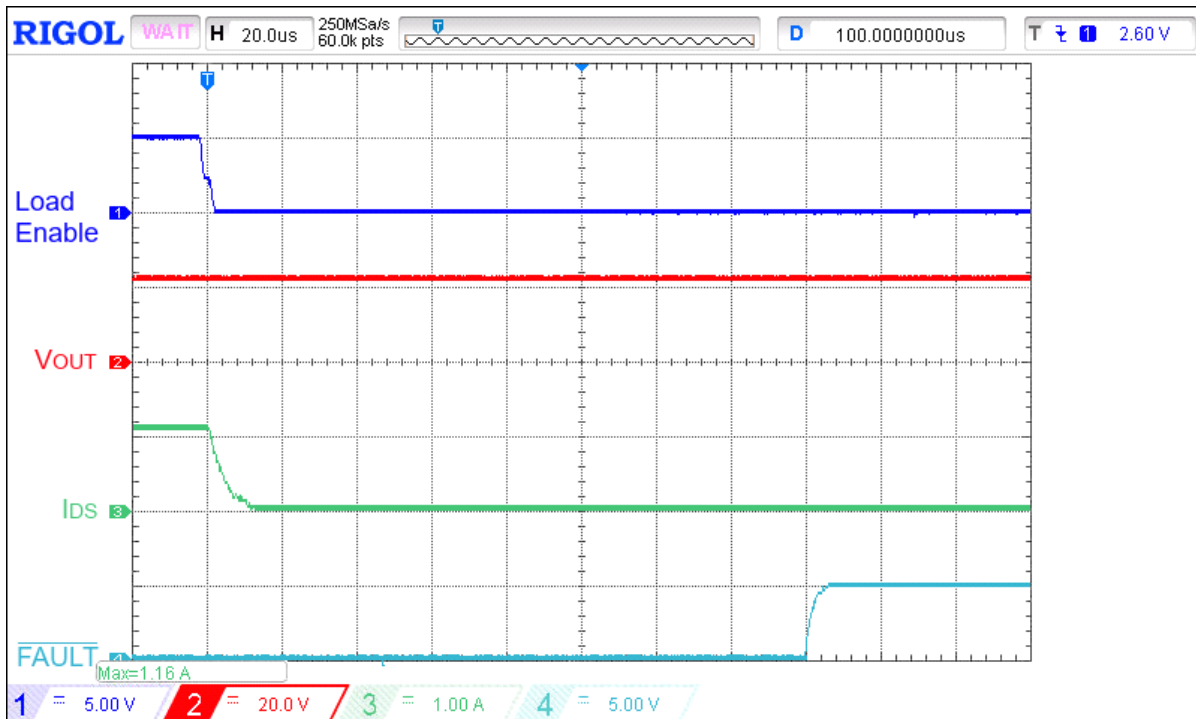


Figure 13. Typical $\overline{\text{FAULT}}$ de-assertion waveform for $V_{IN} = 24 \text{ V}$, $C_{LOAD} = 10 \mu\text{F}$, $I_{ACL} = 1 \text{ A}$, $R_{SET} = 91 \text{ k}\Omega$, switch out 18.5Ω load

A 13.3 mΩ, 5 A Integrated Power Switch with 12 V / 24 V
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Applications Information

HFET1 Safe Operating Area Explained

Dialog’s HFET1 integrated power controllers incorporate a number of internal protection features that prevents them from damaging themselves or any other circuit or subcircuit downstream of them. One particular protection feature is their Safe Operation Area (SOA) protection. SOA protection is automatically activated under overpower and, in some cases, under overcurrent conditions. Overpower SOA is activated if package power dissipation exceeds an internal 5W threshold longer than 2.5 ms. HFET1 devices will quickly switch off (open circuit) upon overpower detection and automatically resume (close) nominal operation once overpower condition no longer exists.

One possible way to have an overpower condition trigger SOA protection is when HFET1 products are enabled into heavy output resistive loads and/or into large load capacitors. It is under these conditions to follow carefully the “Safe Start-up Loading” guidance in the Applications section of the datasheet. During an overcurrent condition, HFET1 devices will try to limit the output current to the level set by the external R_{SET} resistor. Limiting the output current, however, causes an increased voltage drop across the FET’s channel because the FET’s R_{DS(ON)} increased as well. Since the FET’s R_{DS(ON)} is larger, package power dissipation also increases. If the resultant increase in package power dissipation is higher/equal than 5 W for longer than 2.5 ms, internal SOA protection will be triggered and the FET will open circuit (switch off). Every time SOA protection is triggered, all HFET1 devices will automatically attempt to resume nominal operation after 160 ms.

Safe Start-up Condition

SLG59H1010V has built-in protection to prevent over-heating during start-up into a heavy load. Overloading the V_{OUT} pin with a capacitor and a resistor may result in non-monotonic V_{OUT} ramping. In general, under light loading on V_{OUT}, V_{OUT} ramping can be controlled with C_{SLEW} value. The following equation serves as a guide:

$$C_{SLEW} = \frac{T_{RISE}}{V_{IN}} \times 4.9 \mu A \times \frac{20}{3}$$

where

T_{RISE} = Total rise time from 10% V_{OUT} to 90% V_{OUT}

V_{IN} = Input Voltage

C_{SLEW} = Capacitor value for CAP pin

When capacitor and resistor loading on V_{OUT} during start up, the following tables will ensure V_{OUT} ramping is monotonic without triggering internal protection:

Safe Start-up Loading for V _{IN} = 12 V (Monotonic Ramp)			
Slew Rate (V/ms)	C _{SLEW} (nF) ²	C _{LOAD} (μF)	R _{LOAD} (Ω)
1	33.3	500	20
2	16.7	250	20
3	11.1	160	20
4	8.3	120	20
5	6.7	100	20

A 13.3 mΩ, 5 A Integrated Power Switch with 12 V / 24 V V_{IN} Lockout Select and MOSFET Current Monitor Output

Safe Start-up Loading for $V_{IN} = 24\text{ V}$ (Monotonic Ramp)			
Slew Rate (V/ms)	C_{SLEW} (nF) ²	C_{LOAD} (μF)	R_{LOAD} (Ω)
0.5	66.7	500	80
1.0	33.3	250	80
1.5	22.2	160	80
2.0	16.7	120	80
2.5	13.3	100	80

Note 2: Select the closest-value tolerance capacitor.

Setting the SLG59H1010V's Active Current Limit

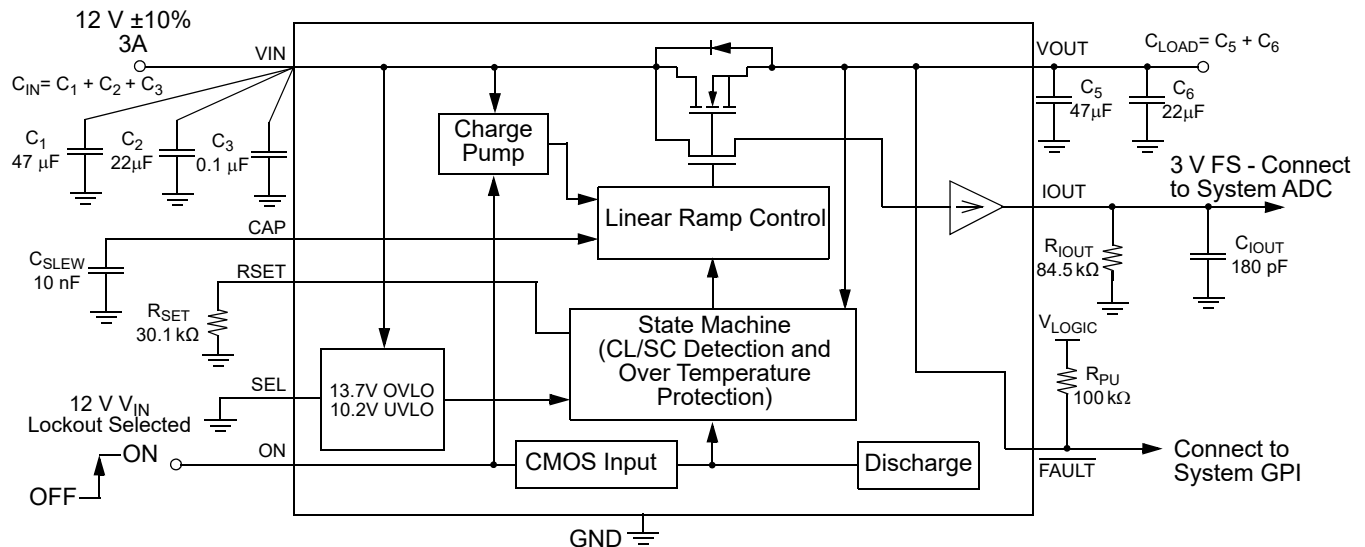
R_{SET} (kΩ)	Active Current Limit (A) ³
91	1
45	2
30	3
18	5

Note 3: Active Current Limit accuracy is ±15% over voltage range and over temperature range.

Configuring the SLG59H1010V for 12 V V_{IN} Lockout Applications

To configure the SLG59H1010V for conditioned 12 V ±10% V_{IN} applications is simply a matter of connecting the SEL pin to GND as shown in Figure A. For other V_{IN} lockout window applications, please consult Dialog for additional information.

Figure A.



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24 V V_{IN} and 12 V V_{IN} Lockout Window Thresholds

Shown in Figure B and Figure C are the two sets of V_{IN} overvoltage/undervoltage lockout windows – one for conditioned 24 V ±5% V_{IN} systems and the second for conditioned 12 V ±10% V_{IN} systems. To avoid lockout threshold collision with nominal operation, the SLG59H1010V's V_{IN(OVLO)} min and V_{IN(UVLO)} max thresholds were set 0.1 V correspondingly higher than the system's nominal V_{IN} max or lower than the system's V_{IN} min range.

Figure B.

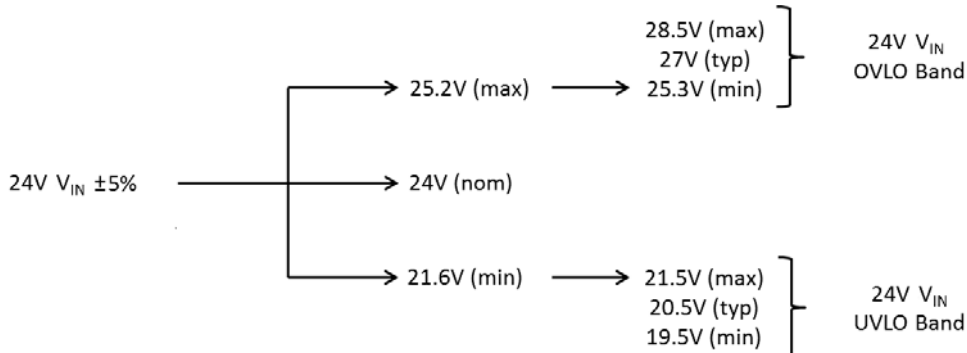
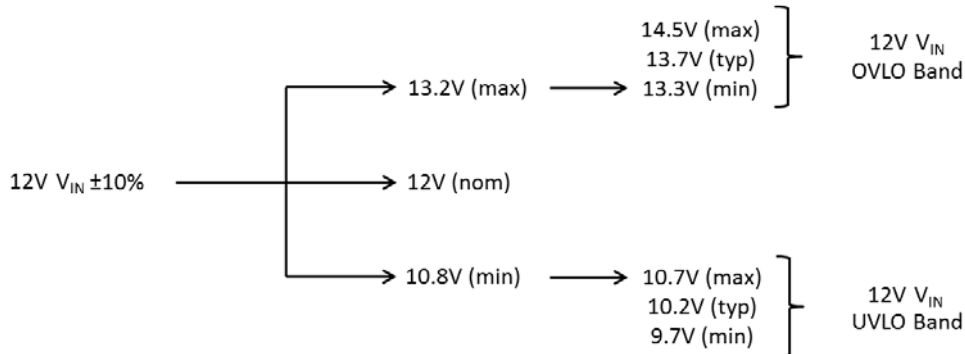


Figure C.



Power Dissipation

The junction temperature of the SLG59H1010V depends on different factors such as board layout, ambient temperature, and other environmental factors. The primary contributor to the increase in the junction temperature of the SLG59H1010V is the power dissipation of its power MOSFET. Its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD = RDS_{ON} \times I_{DS}^2$$

where:

- PD = Power dissipation, in Watts (W)
- RDS_{ON} = Power MOSFET ON resistance, in Ohms (Ω)
- I_{DS} = Output current, in Amps (A)

and

$$T_J = PD \times \theta_{JA} + T_A$$

where:

- T_J = Junction temperature, in Celsius degrees (°C)
- θ_{JA} = Package thermal resistance, in Celsius degrees per Watt (°C/W)
- T_A = Ambient temperature, in Celsius degrees (°C)

**A 13.3 mΩ, 5 A Integrated Power Switch with 12 V / 24 V
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In current-limit mode, the SLG59H1010V's power dissipation can be calculated by taking into account the voltage drop across the power switch (V_{IN}-V_{OUT}) and the magnitude of the output current in current-limit mode (I_{ACL}):

$$PD = (V_{IN} - V_{OUT}) \times I_{ACL} \text{ or}$$
$$PD = (V_{IN} - (R_{LOAD} \times I_{ACL})) \times I_{ACL}$$

where:

PD = Power dissipation, in Watts (W)
V_{IN} = Input Voltage, in Volts (V)
R_{LOAD} = Load Resistance, in Ohms (Ω)
I_{ACL} = Output limited current, in Amps (A)
V_{OUT} = R_{LOAD} × I_{ACL}

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Layout Guidelines:

1. Since the V_{IN} and V_{OUT} pins dissipate most of the heat generated during high-load current operation, it is highly recommended to make power traces as short, direct, and wide as possible. A good practice is to make power traces with absolute minimum widths of 15 mils (0.381 mm) per Ampere. A representative layout, shown in Figure 14, illustrates proper techniques for heat to transfer as efficiently as possible out of the device;
2. To minimize the effects of parasitic trace inductance on normal operation, it is recommended to connect input C_{IN} and output C_{LOAD} low-ESR capacitors as close as possible to the SLG59H1010V's V_{IN} and V_{OUT} pins;
3. The GND pin should be connected to system analog or power ground plane.
4. 2 oz. copper is recommended for high current operation.

SLG59H1010V Evaluation Board:

A HFET1 Evaluation Board for SLG59H1010V is designed according to the statements above and is illustrated on Figure 14. Please note that evaluation board has D_Sense and S_Sense pads. They cannot carry high currents and dedicated only for $R_{DS(ON)}$ evaluation.

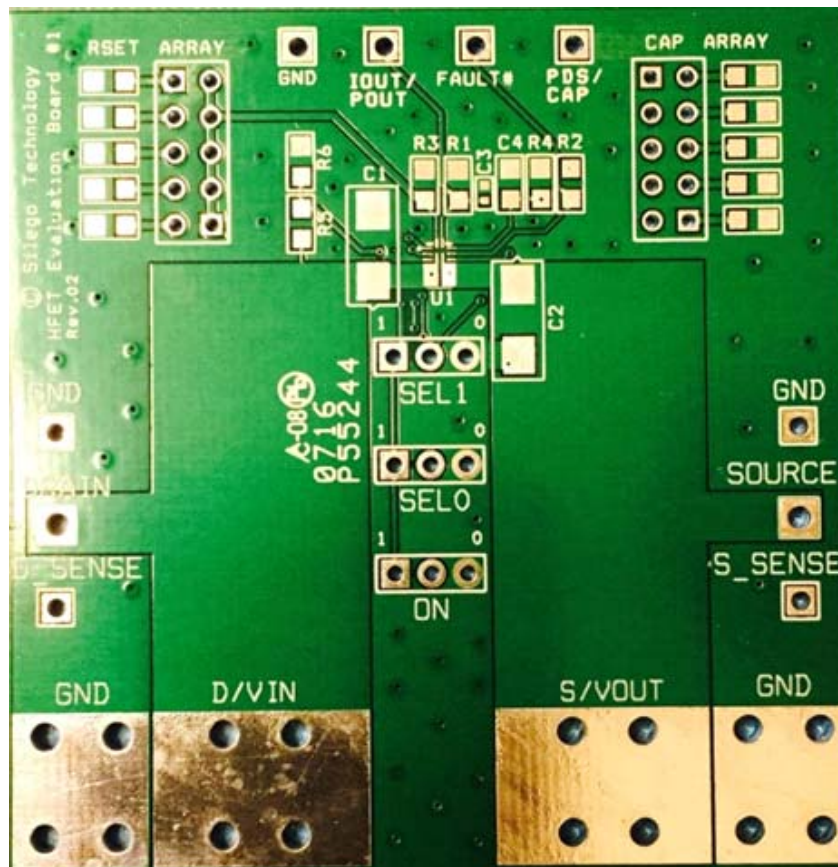


Figure 14. SLG59H1010V Evaluation Board

A 13.3 mΩ, 5 A Integrated Power Switch with 12 V / 24 V V_{IN} Lockout Select and MOSFET Current Monitor Output

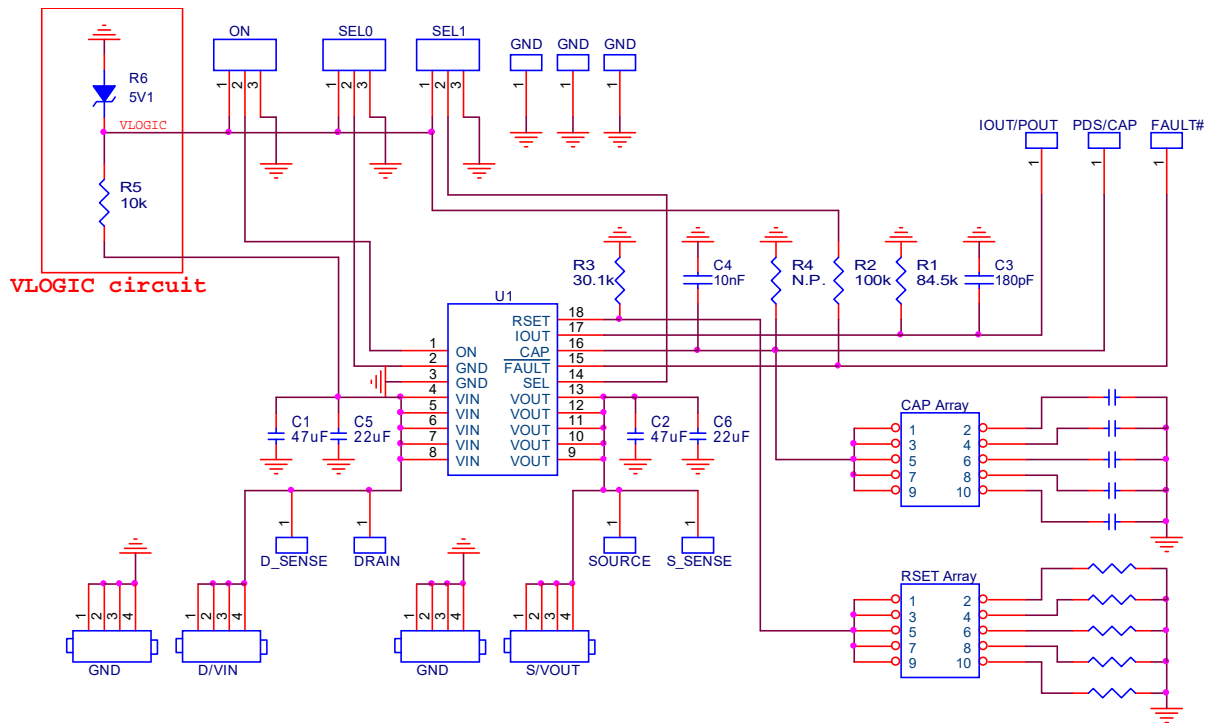


Figure 15. SLG59H1010V Evaluation Board Connection Circuit

Basic Test Setup and Connections

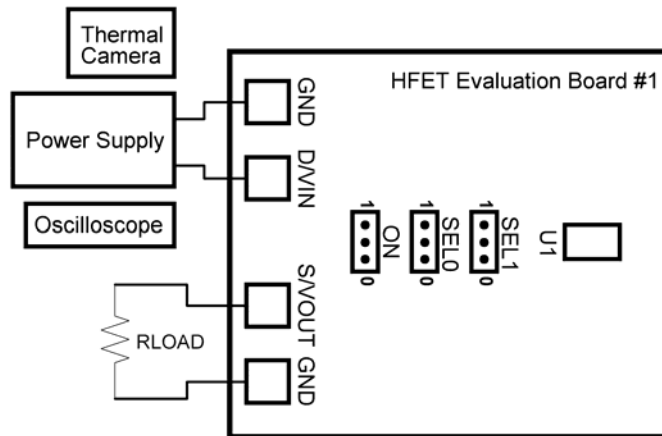


Figure 16. SLG59H1010V Evaluation Board Connection Circuit

EVB Configuration

1. Set SEL0 to GND;
2. Based on V_{IN} voltage, set SEL1 to GND or 5 V to configure OVLO;
3. Connect oscilloscope probes to D/VIN, S/VOUT, ON, etc.;
4. Turn on Power Supply and set V_{IN} to 12 V or 24 V;
5. Toggle the ON signal High or Low to observe SLG59H1010V operation.

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Test Result

Using thermal camera, we tested thermal distribution on the PCB after 2 min power up at $V_{IN} = 24\text{ V}$ and $I_{DS} = 4.5\text{ A}$. Please note how evenly temperature is distributed on the PCB that prove a proper design of PCB and thus other components around HFET will be not overheated. HFET temperature is only 17 °C above the lab ambient temperature. Top left corner displays temperature in the “x” position of thermal camera. Right corner from top to bottom displays full scale of temperatures.

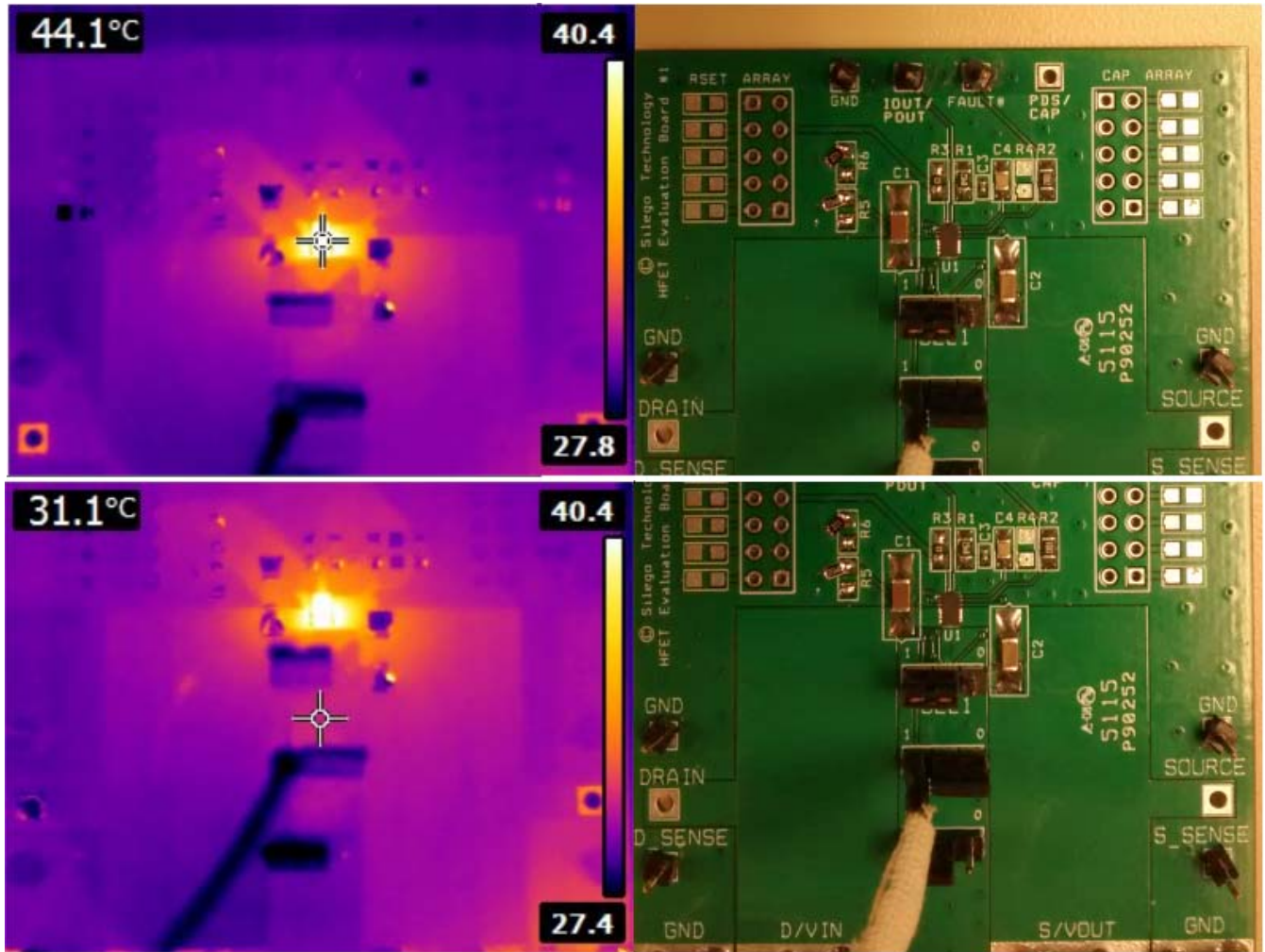
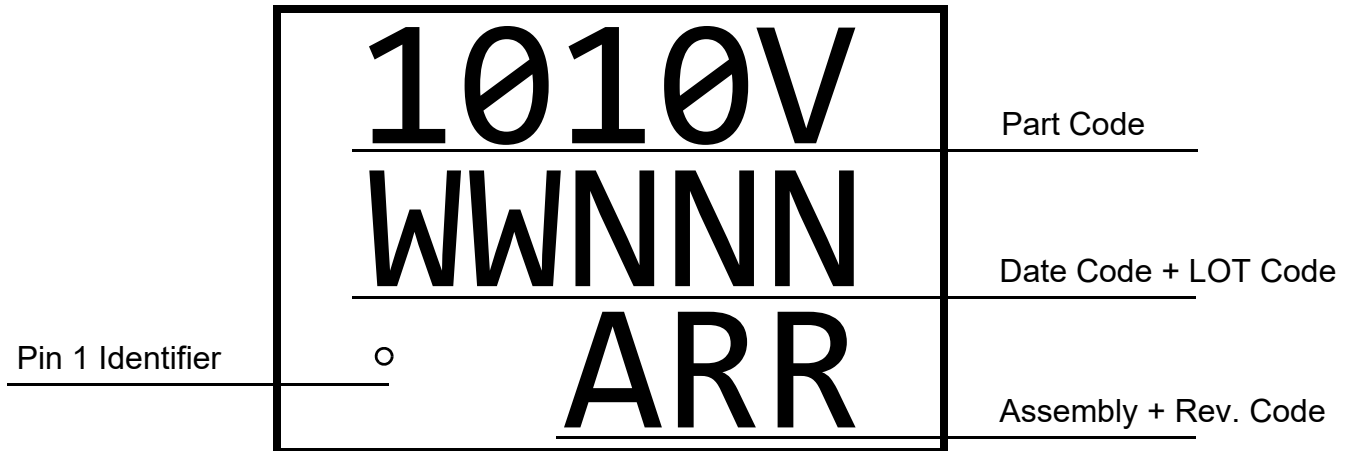


Figure 17. Thermal distribution for $V_{IN} = 24\text{ V}$, $I_{DS} = 4.5\text{ A}$ after 2 min power up

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V_{IN} Lockout Select and MOSFET Current Monitor Output

Package Top Marking System Definition



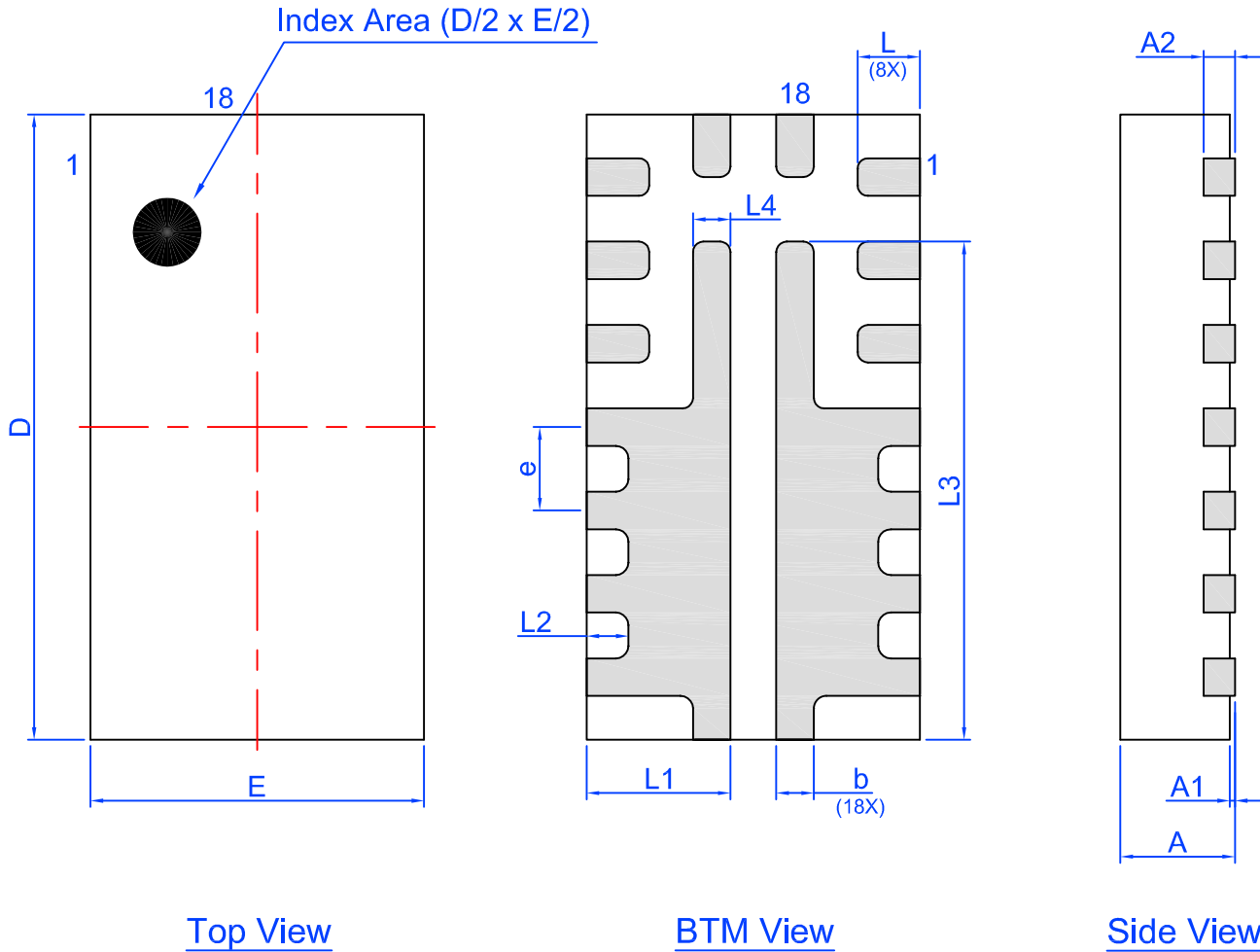
1010V - Part ID Field
WW - Date Code Field¹
NNN - Lot Traceability Code Field¹
A - Assembly Site Code Field²
RR - Part Revision Code Field²

Note 1: Each character in code field can be alphanumeric A-Z and 0-9
Note 2: Character in code field can be alphabetic A-Z

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Package Drawing and Dimensions

18 Lead TQFN Package 1.6 x 3 mm (Fused Lead)
 JEDEC MO-220, Variation WCEE



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.05	E	1.55	1.60	1.65
A2	0.10	0.15	0.20	L	0.25	0.30	0.35
b	0.13	0.18	0.23	L1	0.64	0.69	0.74
e	0.40 BSC			L2	0.15	0.20	0.25
L3	2.34	2.39	2.44	L4	0.13	0.18	0.23

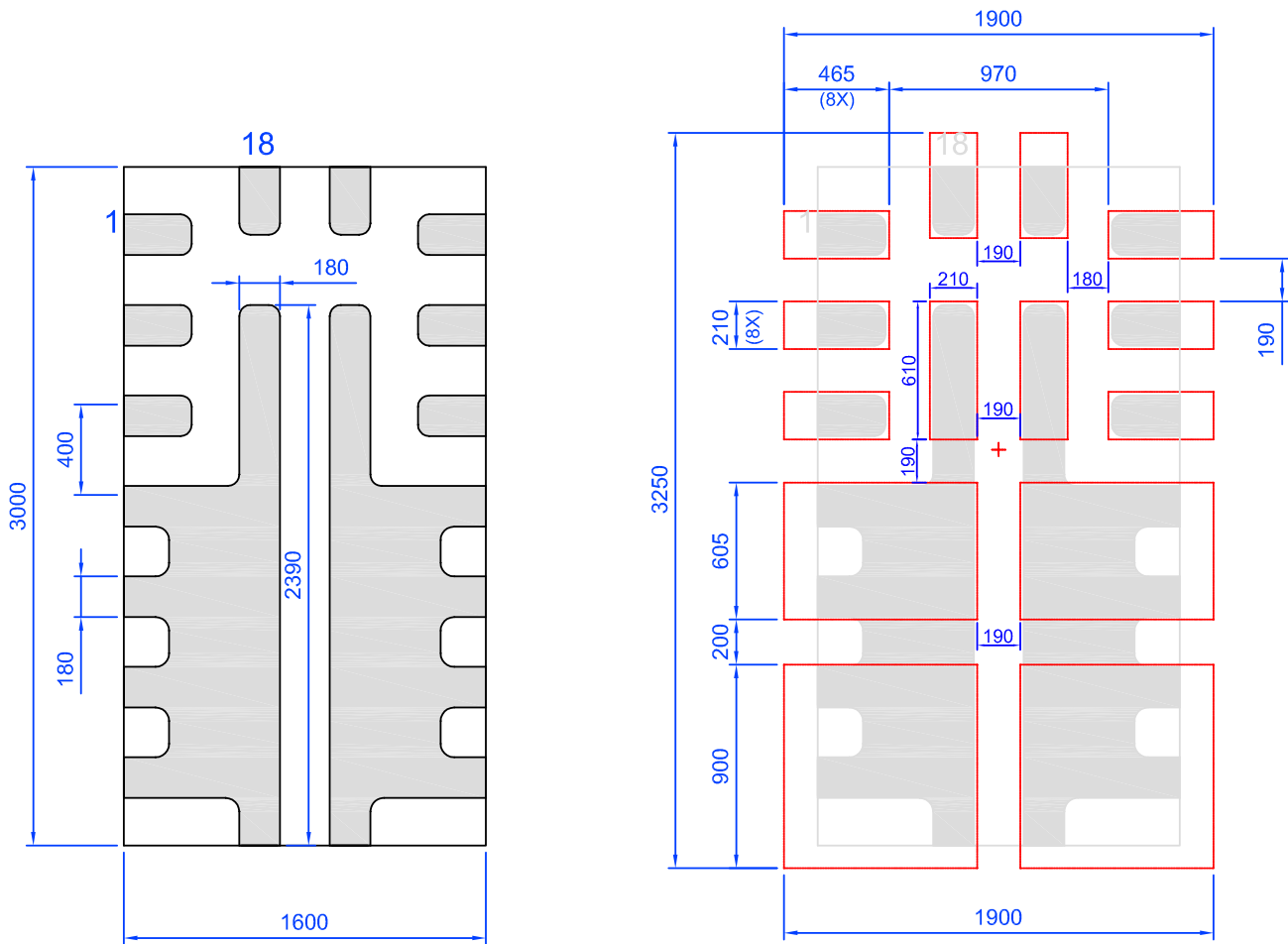
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SLG59H1010V 18-pin STQFN PCB Landing Pattern

 Exposed Pad
(PKG face down)

 Recommended Land Pattern
(PKG face down)



Note: All dimensions shown in micrometers (μm)

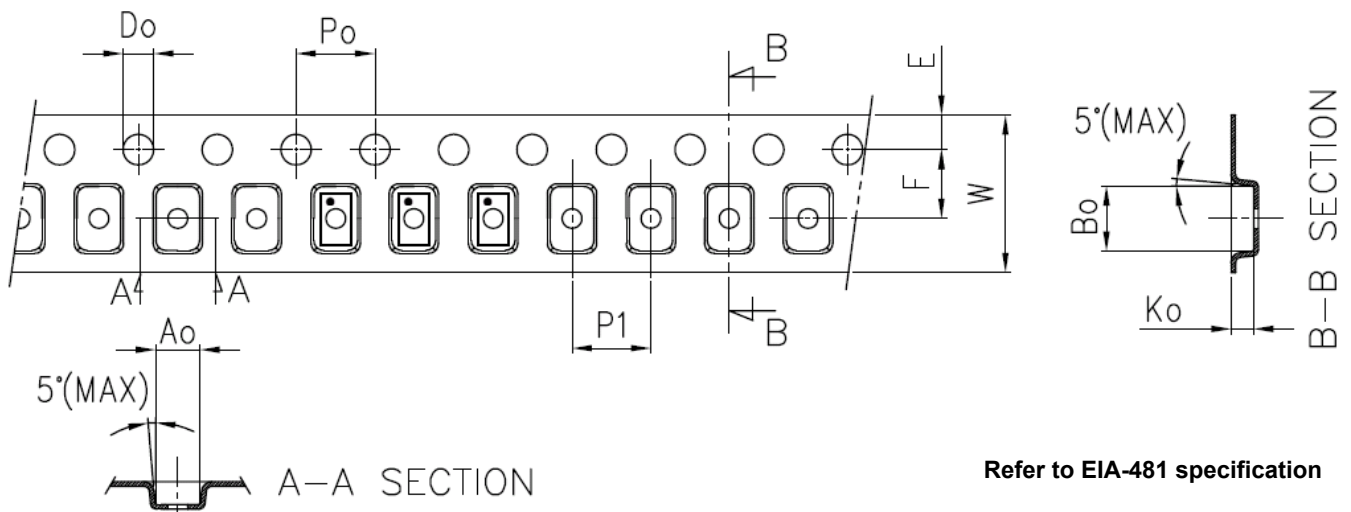
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Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 18L 1.6x3mm 0.4P FC Green	18	1.6 x 3 x 0.55	3,000	3,000	178 / 60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 18L 1.6x3mm 0.4P FC Green	1.78	3.18	0.76	4	4	1.5	1.75	3.5	8



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.64 mm³ (nominal). More information can be found at www.jedec.org.

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Revision History

Date	Version	Change
12/12/2018	1.02	Updated style and formatting Updated Charts Added Scopeshots Added Layout Guidelines Fixed typos
11/2/2017	1.01	Updated V_{IN} Max and $V_{IN(OVLO)}$ Min Updated Charts Fixed typos and formatting
2/24/2017	1.00	Production Release

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