HIGHLY INTEGRATED POWER AND CLOCK SUPPLY IC FOR NEW GENERATION INTEL® ATOM™ PROCESSOR E6XX SERIES PLATFORM

Integrated power management

Dialog Semiconductor's new DA6011 includes low noise supplies to all CPU- and IO-Hub voltage domains and provides current to supply system DDR2 memory as well as the Boot SPI Flash and is sourced by a single input voltage.

The DA6011 integrates 11 high performance low dropout (LDO) voltage regulators using Dialog's patented Smart Mirror™ technology for very low quiescent current and includes 3 pass devices for platform power distribution simplification.

Three DC-DC buck converters with external FETs and three buck converters with integrated FETs provide high current to several low voltage domains of the Intel® Atom™processor E6xx series platform.

These 6 high efficient buck converters are supplying the CPU and graphic core according to Intel® IMVP-6 specification, providing energy to the system memories the IO-Hub and further high current parts of the platform.

The power domain architecture has been carefully optimized to deliver enhanced power efficiency to the platform at lowest power dissipation, thereby maximizing battery life time and reducing thermal impact. The architecture also takes several IO-Hubs with their different power requirements into account.

System Management Controller

The integrated system management controller takes care of the platform start-up, state-transitioning and power-down procedures. It operates autonomously and reduces the overall system power consumption when going into stand-by or power down mode. The flexible state-machine implementation is designed to control E6xx processor, Intel® Platform Controller Hub EG20T, ST Microelectronics® ConneXt, OKI Semiconductor® IVI (ML7213) as well as MP (ML7223) IO-Hubs.

Clock Supplies

A further feature of the DA6011 is the clock supply for the Atom™ processor E6xx platform. Four Fractional division featured PLL's two including spread spectrum capability are included, driving with low-power push-pull amplifiers the platform. The PLL's provide the clocks to the E6xx processor as well as to one of the above mentioned IO-Hubs enabling a platform at lowest component count. The reference clock for the PLL's is generated via a 14.31818MHz crystal oscillator.

Auxiliary function

An analog to digital converter (ADC) with 10-bit resolution, combined with an input multiplexer and track and hold circuitry is implemented. 2 inputs can be used to measure signals manually or automatically.

Operating conditions

The DA6011 is designed for the automotive ambient temperature range of -40 .. +85°C. The die temperature and the output currents of each source will be monitored to ensure proper and safe operation.

Key Features

- Power supplies & Power management for Atom™ processor E6xx series processor and one of the following ST Microelectronics® ConneXt, Intel® Platform Controller Hub EG20T, OKI Semiconductor® IVI (ML7213) or MP (ML7223) IO-Hubs.
- Programmable Clock supplies
- Automotive temperature range, on the basis of the AEC-Q100

Key functions

- 6 high efficient DC-DC buck converter, two according IMVP-6 specification for the Atom™ processor E6xx series
- 11 high performance LDOs
- 3 integrated pass devices
- A push-pull reference source/sink for DDR2 RAM termination
- Autonomous, flexible state machine for complete system start-up and shut-down procedure
- 4 fractional divider PLL's including spread spectrum capability according to Intel/IO-Hub supplier specification
- 2 input 10-bit ADC for signal measurements

Applications

- Vehicle Command Systems
- Telematics Devices
- Car Navigation Systems
- Mobile Internet Devices
- UMPCs
- High End PNDs
- Netbooks
- Nettops
- Multimedia phones
- …

Block Diagram

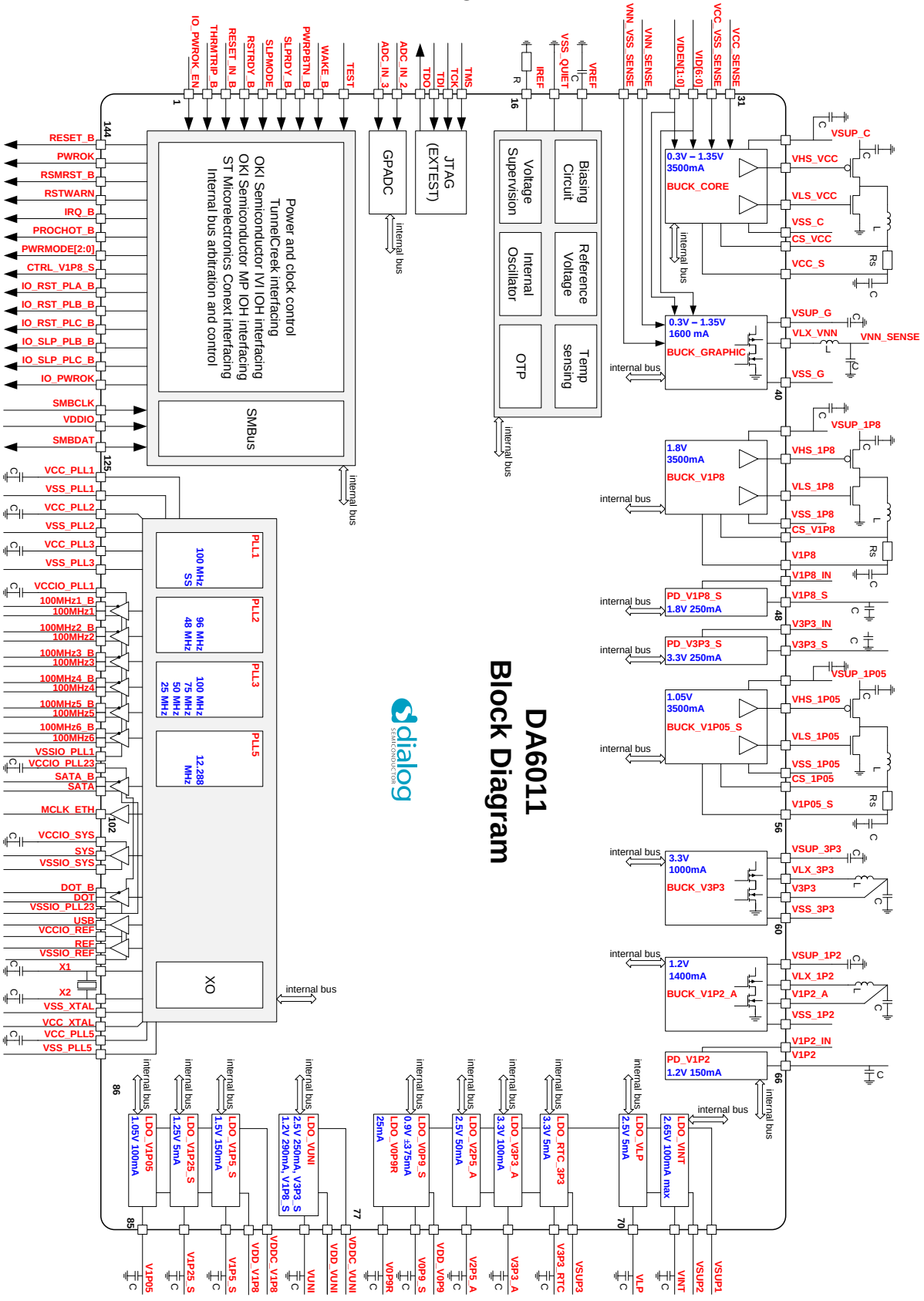


Figure 1 : DA6011 Block diagram

Revision history

Revision	Description	Revision date
0.1	• First internal draft datasheet	2009.07.31
0.2	• Release for first internal reviews	2009.08.07
0.23	• Version with updated PLL and dedicated current information for each power domain	2009.09.18
0.30	• First customer draft datasheet	2009.11.06
0.31	• Updated package drawing, PLL4 removed	2009.11.23
0.5	• After Intel review • Updated Block diagram • LDO_V0P9R included • General purpose ADC section updated • Updated LDO electrical characteristics • Editorial updates • Updated timings • Included Registers description • Updates pin-list & ball-out	2010.02.04
0.8	• Editorial updates • Updated Pin/Ball-out (swap of DOT/DOT_B and SATA/SATA_B as well as DOT_B with DOT) • Update of timing diagrams • S3 -> S0 diagrams extended for internal and external wake up events • Register addresses updated • Additional enable bit for external reference clock in XTALCTRL2 register	2010.03.31
0.81	• Inductance change of Graphic buck converter! • Inductance and Capacity change of 1.2V buck converter! • Updated digital IO voltage levels • Minor editorial updates	2010.04.21
1.0	• First released datasheet revision 1.0 • Renamed Tunnel Creek by Atom E6xx processor series • Renamed TopCliff by Intel Platform Controller Hub EG20T • Updates for clarification of the power domains • Timing diagrams and tables reworked and updated • Naming of 100MHz clock output signals changed, providing most simple layout option, as all differential 100MHz clock signals are identical • Characteristic of THRMTRIP_B input signal corrected • POWOK toggling function included	2010.09.22
1.1	• Updated clock synthesizer/driver layout • Editorial correction pin list • Added missing stabilization capacitors for Buck_V1P05 • Internal pull-up/-down resistor information added in Digital IO Characteristics • Maximum voltage for BUCK_CORE and BUCK_GRAPHICS increased to 1.35V • Updated parameters for BUCK_CORE, BUCK_GRAPHICS, BUCK_1P05, BUCK_1P2, BUCK_1P8 and BUCK_3P3 • PLL section: output frequency accuracy added • Register map & register content update due to CA-silicon	2011.01.19
1.2	• Timing diagrams and tables chapter 7.6 updated • Debouncing feature added for WAKE_B & RESET_IN_B pin description	2011.06.20

Revision	Description	Revision date
	• Editorial correction for LDO_0P9R • IO_PWROKEN with a new feature waiting for stable ATX power supplies for EG20T and ML7223 • PWROK toggling feature updated • Soldering profile adder • Component proposal updated	

1. OPERATING CONDITIONS

All Voltages are referenced to VSS unless otherwise stated. Currents flowing into DA6011 are deemed positive, currents flowing out are deemed negative.

All parameters are valid over the full operating temperature range and power supply range unless otherwise noted. Please note that the power dissipation must be limited to avoid overheating of DA6011. The maximum power dissipation should not be reached with maximum ambient temperature.

1.1 Absolute maximum ratings

Parameter	Conditions	Min	Max	Unit
Storage Temperature	TSTOR	-65	+150	°C
Operating Temperature	TAMB	-40	+85	°C
Power Supply Input	VSUP	-0.3	+5.5	V
IO Input	(All unless otherwise stated)	-0.3	VSUP+0.3	V
Maximum power dissipation			1.5	W
Package thermal resistance			30	K/W
ESD CDM (Charge Device Model)	All pins unless otherwise stated.		500	V
ESD HBM (Human Body Model)	All pins unless otherwise stated.		2	kV

Table 1: DA6011 absolute maximum ratings

1.2 Recommended Operating Condition

Parameter	Conditions	Min	Max	Unit
Operating Temperature	TAMB	-40	+85	°C
Power Supply Input	VSUP	4.5	5.25	V

Table 2: DA6011 recommended operating condition

1.3 Digital I/O Characteristics

The “_B” symbol at the end of a signal name indicates that the active or asserted state occurs when the signal is at a low voltage level (active low). When the “_B” is not present after the signal name the signal is asserted when the signal is at a high voltage level.

Electrical Characteristics (Ta = -40 to +85 °C)

PARAMETER	Parameter	MIN	TYP	MAX	UNIT
PWRPBTN_B Input high voltage	VIH	0.8 * VDDIO		VSUP	V
PWRPBTN_B Input low voltage	VIL	0		0.2*VDDIO	V
RESET_B Output high voltage	VOH	0.8 * VDDIO		VDDIO	V
RESET_B Output low voltage	VOL	0		0.2*VDDIO	V
PWROK Output high voltage	VOH	0.8 * VDDIO		VDDIO	V
PWROK Output low voltage	VOL	0		0.2*VDDIO	V

PARAMETER	Parameter	MIN	TYP	MAX	UNIT
RSMRST_B Output high voltage	VOH	0.8 * VDDIO		VDDIO	V
RSMRST_B Output low voltage	VOL	0		0.2*VDDIO	V
WAKE_B Input High Voltage	VIH	0.8*VDDIO		VSUP	V
WAKE_B Input Low Voltage	VIL	0		0.2*VDDIO	V
WAKE_B internal resistor to VDDIO		10	20	30	kΩ
SLPMODE Input high voltage	VIH	0.8 * VDDIO		VDDIO	V
SLPMODE Input low voltage	VIL	0		0.2*VDDIO	V
RSTWARN Output high voltage	VOH	0.8 * VDDIO		VDDIO	V
RSTWARN Output low voltage	VOL	0		0.2*VDDIO	V
SLPRDY_B Input high voltage	VIH	0.8 * VDDIO		VDDIO	V
SLPRDY_B Input low voltage	VIL	0		0.2*VDDIO	V
SLPRDY_B internal resistor to VDDIO		10	20	30	kΩ
RSTRDY_B Input high voltage	VIH	0.8 * VDDIO		VDDIO	V
RSTRDY_B Input low voltage	VIL	0		0.2*VDDIO	V
RSTRDY_B internal resistor to VDDIO		10	20	30	kΩ
SMBUSDATA Output Low Voltage	VOL @350µA		Open drain	0.4	V
SMBUSDATA Input Low Voltage	VIL			0.5	V
SMBUSDATA Input High Voltage	VIH	1.4		VDDIO	V
SMBUSCLK Input High Voltage	VIH	1.4		VDDIO	V
SMBUSCLK Input Low Voltage	VIL			0.6	V
SMBUSDATA Leakage Current		-1		1	µA
SMBUSCLK Leakage Current		-1		1	µA
IRQ_B Output low voltage	VOL @350µA		Open drain	0.4V	V
PROCHOT_B Output low voltage	VOL @350µA		Open drain	0.4V	V
PWRMODE[2:0] Input high voltage	VOH	0.8 *V1P05_S		V1P05_S	V
PWRMODE[2:0] Input low voltage	VOL	0		0.2*V1P05_S	V
VID[6:0] Input high voltage	VIH	0.8 * V1P05		V1P05_S	V

PARAMETER	Parameter	MIN	TYP	MAX	UNIT
VID[6:0] Input low voltage	VIL	0		0.2*V1P05_S	V
VIDEN[1:0] Input high voltage	VIH	0.8 * V1P05_S		V1P05_S	V
VIDEN[1:0] Input low voltage	VIL	0		0.2*V1P05_S	V
CTRL_V1P8_S Output high voltage	VOH	0.8*VDDIO		VDDIO	V
CTRL_V1P8_S Output low voltage	VOL	0		0.2*VDDIO	V
IO_RESET_PLA_B Output high voltage	VOH	0.8*VDDIO		VDDIO	V
IO_RESET_PLA_B Output low voltage	VOL	0		0.2*VDDIO	V
IO_RESET_PLB_B Output high voltage	VOH	0.8*VDDIO		VDDIO	V
IO_RESET_PLB_B Output low voltage	VOL	0		0.2*VDDIO	V
IO_RESET_PLC_B Output high voltage	VOH	0.8*VDDIO		VDDIO	V
IO_RESET_PLC_B Output low voltage	VOL	0		0.2*VDDIO	V
IO_SLP_PLB_B Output high voltage	VOH	0.8*VDDIO		VDDIO	V
IO_SLP_PLB_B Output low voltage	VOL	0		0.2*VDDIO	V
IO_SLP_PLC_B Output high voltage	VOH	0.8*VDDIO		VDDIO	V
IO_SLP_PLC_B Output low voltage	VOL	0		0.2*VDDIO	V
IO_PWROK Output high voltage	VOH	0.8*VDDIO		VDDIO	V
IO_PWROK Output low voltage	VOL	0		0.2*VDDIO	V
IO_PWROKEN Input high voltage	VIH	0.8*VDDIO		VSUP	V
IO_PWROKEN Input low voltage	VIL	0		0.2*VDDIO	V
RESET_IN_B Input high voltage	VIH	0.8* VDDIO		VDDIO	V
RESET_IN_B Input low voltage	VIL	0		0.2*VDDIO	V
RESET_IN_B internal resistor to VDDIO		10	20	30	kΩ
THRMTRIP_B Input low voltage	VIL	0		0.2*V1P05_S	V
THRMTRIP_B Input high voltage	VIH	0.8*V1P05_S		V1P05_S	V
TDI Input high voltage	VIH	0.8*VDDIO		VDDIO	V
TDI Input low voltage	VIL	0		0.2*VDDIO	V
TDI Internal resistor to	Pull-up resistance	10	20	30	kΩ

PARAMETER	Parameter	MIN	TYP	MAX	UNIT
TDO Output high voltage	VOH	0.8*VDDIO		VDDIO	V
TDO Output low voltage	VOL	0		0.2*VDDIO	V
TCLK Input high voltage	VIH	0.8*VDDIO		VDDIO	V
TCLK Input low voltage	VIL	0		0.2*VDDIO	V
TMS Input high voltage	VIH	0.8*VDDIO		VDDIO	V
TMS Input low voltage	VIL	0		0.2*VDDIO	V
TMS Internal resistor to VDDIO	Pull-up resistance	10	20	30	kΩ

Table 3: Digital I/O electrical conditions

1.4 Digital IO Pin descriptions

1.4.1 PWRPBTN_B

Power Push Button. The PWRPBTN_B pin is implemented with 2 functionalities. DA6011 can be order with power push button or switching functionality. For further details, see chapter 7.3. For power push button variants a pull-up resistor to VDD is requested.

1.4.2 RESET_B

E6xx processor Reset. The RESET_B is an active-low input signal to the processor. When asserted, E6xx processor will initiate a reset sequence and return to its default state.

In designs with the ST IO-Hub the TC_RESET_B signal generation will be triggered by the IO_PWROKEN input signal.

1.4.3 PWROK

E6xx processor Power OK. When asserted, PWROK is an indication to E6XX that the power up sequence is finished and all power supplies are stable. PWROK is de-asserted during S3, S4 and S5 state. PWROK can be driven asynchronously.

In designs with the ST IO-Hub the PWROK signal generation will be triggered by the IO_PWROKEN input signal.

1.4.4 RSMRST_B

Resume domain Reset. The RSMRST_B is an active-low signal from DA6011 to E6XX which indicates the CPU-Hub resetting the resume domain. A minimum delay of 5ms is required to ensure the resume power domains are valid prior to RSMRST_B going high.

1.4.5 WAKE_B

Wakeup event. This signal indicates an external event to wake up the system if it is in S4/5 mode or S3.

This is a single signal that can be driven by any devices on the board to wake up the platform if it is in S4/5 state. It is normally pulled high by the device, but any device that need to wake the DA6011 has to drive the signal for at least 16ms to low (debouncing filter), followed by a low to high transition which generates the internal wake event. The signal will only be active if the system is in S3 or S4/5 mode.

1.4.6 SLPMODE

Sleep mode. SLPMODE determines which sleep state is entered. When SLPMODE is asserted, S3 state will be chosen. Negating of SLPMODE, S4/S5 will be the selected sleep mode.

1.4.7 RSTWARN

Reset Warning. The RSTWARN is an active-high signal from DA6011 to the E6XX CPU Hub. Asserting the RSTWARN signal tells the E6XX to enter a sleep state or begin to power down. The DA6011 will assert this signal after an external event, such as pressing the power button or the occurrence of a thermal event.

1.4.8 SLPRDY_B

Sleep ready. The SLPRDY_B signal is an active-low input to DA6011 that indicates E6XX is awake and able to be placed into the sleep state (S0 -> S3 transition). De-asserting of SLPRDY_B indicates a wake up request from a system device.

1.4.9 RSTRDY_B

Reset ready. The RSTRDY_B signal is an active-low input to DA6011 that indicates to set Atom™E6xx processor platform into low power state (S3, S4/5 mode). The E6XX asserts RSTRDY_B after detecting assertion of the RSTWARN signal from external.

1.4.10 SMBDAT

System Management Bus Data. The SMBDAT is the power manager SMBus data signal to DA6011. It functions as an open drain signal, requesting a system pull-up resistor so either component can pull it down to a logic low level.

1.4.11 SMBCLK

System Management Bus Clock. The SMBCLK signal is the power manager SMBus clock to DA6011. The serial SMBus should operate at a minimum 10 kHz and maximum 100 kHz clock rate and requests a system pull-up resistor.

1.4.12 IRQ_B

DA6011 Interrupt. The IRQ_B signal (active low with external pull-up resistor) is an open drain output signal that indicates that an interrupt causing event has occurred, and that event status information is available in the status register.

The following interrupts will be provided and set if the according event occurs. These interrupts can be masked via the according bits. Each interrupt can be cleared by writing to the corresponding clear register. For more details see the register definitions in Section 8.5.

- Over temperature event
- Under voltage event
- Over voltage event
- Power-push-button event if push-button functionality is enabled and system is in S0 or S3

1.4.13 PROCHOT_B

Processor Hot. Active low input to E6XX indicates the CPU-Hub to start the thermal control circuit (E6XX). PROCHOT_B is used for thermal protection of the DA6011. PROCHOT_B, pulled up via resistor to V1P05_S power domain, will be asserted when the temperature limit of the DA6011 is reached. By asserting PROCHOT_B (pulled low) and activating the TCC, the DA6011 will cool down as a result of reduced processor power drain. This protects the DA6011 from overheating. The minimum assertion time of PROCHOT_B is specified to be 500µs. The PROCHOT_B threshold should be at 110°C junction temperature of DA6011.

1.4.14 PWRMODE[2:0]

Power Mode. DA6011 is generating these signals to sequence the processor through various states such as cold and warm reset.

1.4.15 VID[6:0]

Voltage Identifier. Indicates a desired voltage for either VCC_S or the VNN_S depending on the VIDEN pins. Resolution of 12.5mV according to Intel's IMVP-VI specification.

1.4.16 VIDEN[1:0]

Voltage Identifier Enable. Indicates which voltage domain is being specified on the VID pins

1.4.17 CTRL_V1P8_S

Control suspend 1.8 voltage. This output pin can optionally control an external FET transistor disabling the Atom™ E6xx processor VCC180 voltage domain during S3, S4 and S5 state.

1.4.18 IO_RESET_PLA_B

IO-Hub reset plane A. DA6011 provides this signal to reset the plane A of the EG20T Platform Controller Hub during the power on sequence towards S4/5 state. For other IO-Hubs this signal will not be used and can be left unconnected.

1.4.19 IO_RESET_PLB_B

IO-Hub reset plane B. DA6011 provides this signal to reset the plane B of the EG20T Platform Controller Hub during the state transition from S4/5 towards S3 state or vice versa. For other IO-Hubs this signal will not be used and can be left unconnected.

1.4.20 IO_RESET_PLC_B

IO-Hub reset plane C. DA6011 provides this signal to reset the plane C of EG20T Platform Controller Hub during the state transition from S3 towards S0 or vice versa. This signal can also be used for other IO-Hubs like the ST ConneXt or the OKI IVI to bring the IO-Hub out or into reset. If not used this pin can be left unconnected.

1.4.21 IO_SLP_PLB_B

IO-Hub Sleep Plane B. DA6011 provides this signal to bring the plane B of EG20T Platform Controller Hub into/out-of sleep mode. Signal is only used for EG20T Platform Controller Hub, for other IO-Hubs it won't be necessary and can be left unconnected.

1.4.22 IO_SLP_PLC_B

IO-Hub Sleep Plane C. DA6011 provides this signal to bring the plane C of EG20T Platform Controller Hub into/out-of sleep mode. Signal is only used for EG20T Platform Controller Hub, for other IO-Hubs it won't be necessary and can be left unconnected.

1.4.23 IO_PWROK

IO-Hub power OK. DA6011 provides this signal to the IO-Hubs, indicating that all necessary IO-Hub power domains are up and stable.

1.4.24 IO_PWROKEN

IO-Hub power OK enable. Multi-functional input signal. STA2x11: DA6011 receives this signal from the ST ConneXt IO-Hub and enables the trigger for E6xx processor activation. EG20T & ML7223: DA6011 provides the function to wait during S3 to S0 transition for a stable ATX switched power supply (details see FAQ document)

1.4.25 RESET_IN_B

Reset in DA6011. This reset is used to initiate an external warm reset to the platform. This signal is enabled only if the platform/DA6011 is in S0 state. The RESET_IN_B pin is internally pulled up and includes a debouncing filter, requesting the RESET_IN_B signal to be pulled low for at least 16ms plus a signal low to high transition before detecting such event.

1.4.26 THRMTRIP_B

Catastrophic Thermal Trip. This pin indicates that Atom™E6xx processor has reached an operating temperature that may damage the part. DA6011 immediately cuts off the power to the platform

1.4.27 TCK

JTAG Test Clock. TCK is a clock input, used to drive the Test Access Port (TAP).

1.4.28 TDI

JTAG Test Data In. TDI is used for serial input data shift, data and instructions into the TAP.

1.4.29 TDO

JTAG Test Data Out. TDO is used for serial output data shift of the TAP.

1.4.30 TMS

JTAG Test Mode Select. This signal is used to control the status of the TAP controller.

2 POWER SUPPLIES

2.1 Power supply module summary

The power supply part of the DA6011 PMIC consists of various power supplies modules. The definition of the PMC Power Supply Modules is based on the data derived from the table of the following paragraphs:

Most of the power supplies are programmable via the serial SMBus.

Power Supply Module	DA6011 Supplied Pins	Supplied Voltage	Supplied Current	Notes
BUCK_CORE DC to DC Buck Converter with DVC With external switching transistor	VCC_S	0.30 – 1.35V ±1.5% accuracy Default: 1.1V ±1.5%	3500 mA	A DC to DC Buck Converter that will supply 0.3V – 1.35V at 3500 mA with ±1.5% accuracy. The Converter will operate at a high frequency (1MHz) in order to allow the use of a 1.5µH inductor
BUCK_GRAPHIC DC to DC Buck Converter with DVC	VNN_S	0.30 – 1.35V ±1.5% accuracy Default: 0,9V ±1.5%	1600 mA	A DC to DC Buck Converter that will supply 0.3V – 1.35V at 1600 mA with ±1.5% accuracy. The Converter will operate at a high frequency (1MHz) in order to allow the use of a 1.5µH inductor.
BUCK_1P05 With external switching transistor	V1P05_S	1.05V ±2% accuracy	3500mA	A DC to DC Buck Converter that will supply 1.05V at 3500mA with ±2% accuracy. The Converter will operate at a high frequency (1MHz) in order to allow the use of a 1.5µH inductor.
BUCK_1P2	V1P2_S STA2X11 ML7213 V1P2_A EG20T ML7223	1.2V ±3% accuracy	1600mA	A DC to DC Buck Converter that will supply 1.2V at 1600mA with ±3% accuracy. The Converter will operate at a high frequency (1MHz) in order to allow the use of a 1.5µH inductor.
BUCK_1P8 With external switching transistor	V1P8	1.8V ±2% accuracy	3200mA	A DC to DC Buck Converter that will supply 1.8V at 3200mA with ±2% accuracy. The Converter will operate at a high frequency (1MHz) in order to allow the use of a 1.5µH inductor.
BUCK_3P3 DC to DC Buck Converter	V3P3_S	3.3V ±3% accuracy	1000mA	A DC to DC Buck Converter that will supply 3.3V at 1000mA with ±3% accuracy. The Converter will operate at a high frequency (1MHz) in order to allow the use of a 4.7µH inductor
LDO_RTC_V3P3	V3P3_RTC	3.3V ±3% accuracy	5mA	Supply for the RTC island
LDO_V3P3	V3P3_A	3.3V ±3% accuracy	100mA	A 100mA 3.3V LDO supplied by the input voltage
LDO_V2P5	V2P5_A	2,5V ±3% accuracy	50mA	A 50mA 2.5V LDO supplied by the input voltage
LDO_V1P5	V1P5_S	1.5V ±3% accuracy	150mA	A 150mA LDO supplied from BUCK_V1P8
LDO_V1P25	V1P25_S	1.25V ±2% accuracy	5mA	A 5mA LDO supplied from BUCK_V1P8
LDO_V1P05	V1P05	1.05V ±2% accuracy	100mA	A 100mA LDO supplied from BUCK_V1P8
LDO_V0P9	V0P9_S	0.9V	±375mA	Output is derived from BUCK_V1P8

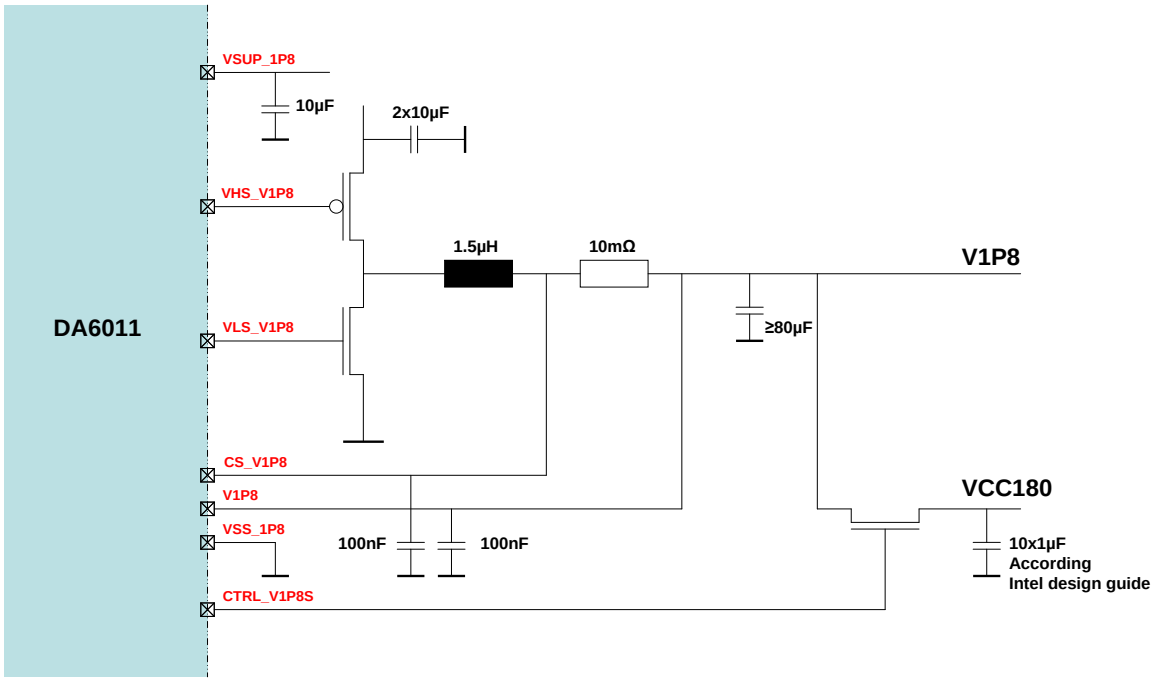
Power Supply Module	DA6011 Supplied Pins	Supplied Voltage	Supplied Current	Notes
		±2% accuracy		and is always half of it. The pass device is supplied by BUCK_V1P2.
LDO_V0P9R	V0P9R	0.9V ±2% accuracy	20mA	A 20mA LDO supplying 0.9V towards the DDR2 memory as a reference
LDO_VUNI	V1P2/V2P5	1.2V/2.5V ±3% accuracy	290/250mA	A LDO supplied either from BUCK_V1P8 (output voltage 1.2V) or BUCK_V3P3 (output voltage 2.5V)
PD_V3P3	V3P3_S	3.3V	250mA	Pass device supplied by BUCK_V3P3
PD_V1P8	V1P8_S	1.8V	250mA	Pass device supplied by BUCK_V1P8
PD_V1P2	V1P2_S	1.2V	150mA	Pass device supplied by BUCK_V1P2
LDO_V2P65	VINT	2.65V	100mA	A 100mA LDO supplied from input voltage
LDO_V2P5	VLP	2.5V	5mA	A 5mA low power LDO for internal purpose

Table 4: DA6011 power domains

2.2 Platform Power Distribution

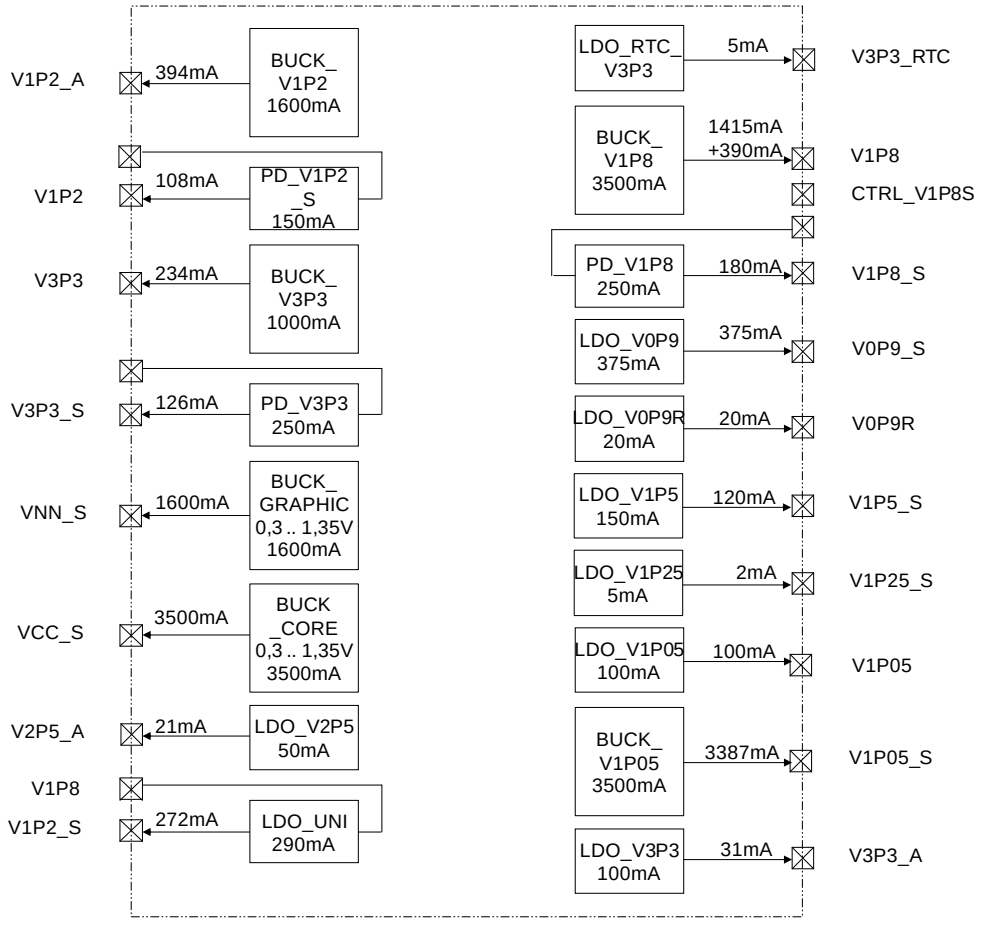
Below you can find the information which power module supplies the corresponding voltage domain dependant on the IO-Hub (ST ConneXt, OKI Semiconductor IVI and MP as well as Intel's EG20T Platform Controller Hub).

Note:
For power distribution and power dissipation reason, the Atom™ processor E6xx voltage domain VCC180 (DDR IO) with its max. current consumption of 390mA shall be directly connected to the DA6011 power supply V1P8 or via a switching FET which is controlled by the output pin CTRL_V1P8S.



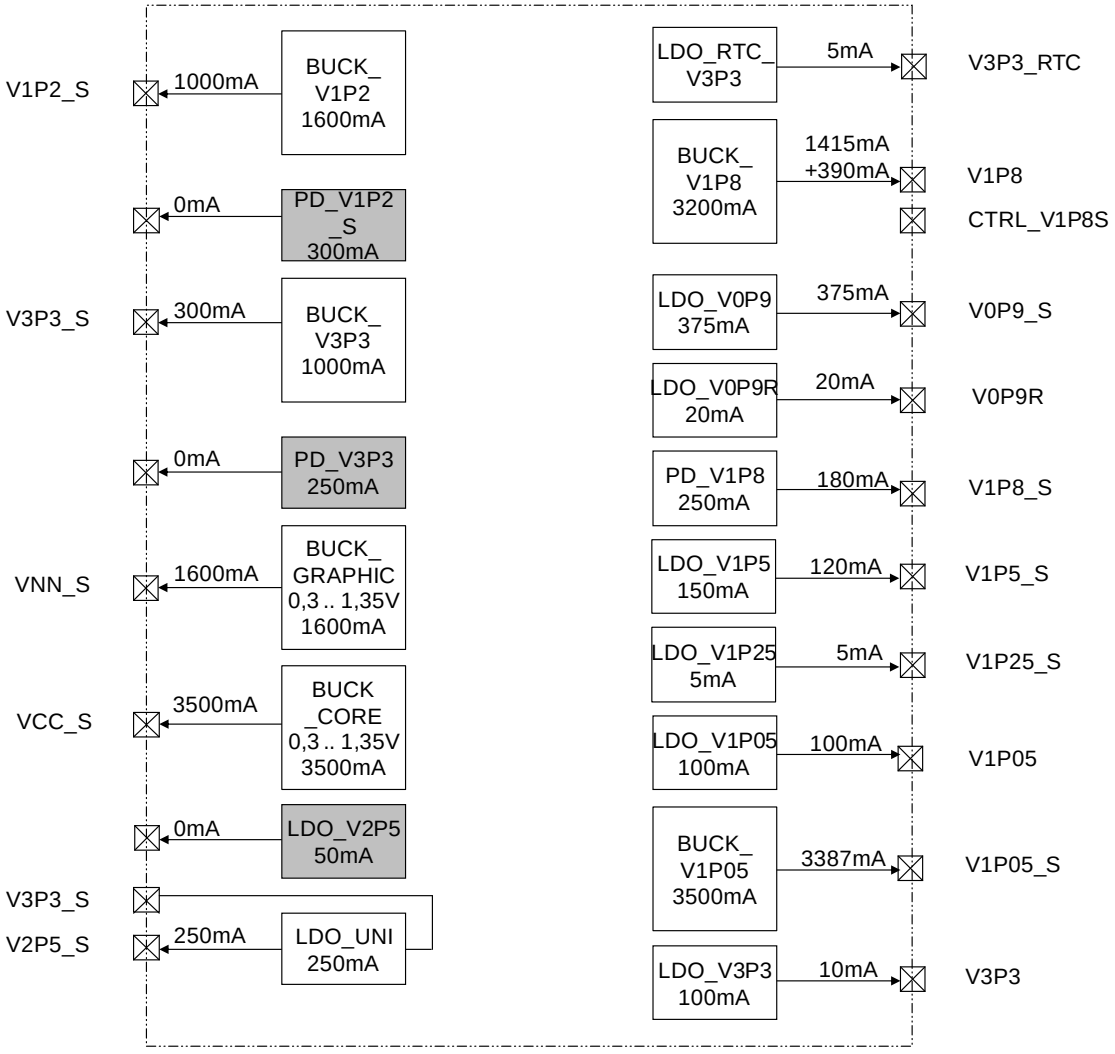
2.2.1 Atom™ E6xx processor & Intel's EG20T Platform Controller Hub

Supply Module	Voltage domain	First active state	Sequence	Current [mA]	Current EG20T [mA]
LDO_RTC_V3P3	V3P3_RTC	S4/5	0 (E6XX)	5	0
BUCK_V1P2	V1P2_A	S4/5	1 (PCH)	0	394
LDO_V2P5	V2P5_A	S4/5	2 (PCH)	0	21
LDO_V3P3	V3P3_A	S4/5	3 (PCH)	0	31
PD_V1P2	V1P2	S3	4 (PCH)	0	108
BUCK_V3P3	V3P3	S3	5 (E6XX & PCH)	10	224
BUCK_V1P8	V1P8	S3	6 (E6XX & DDR2)	1415	0
LDO_V0P9R	V0P9	S3	7 (DDR2)	20	0
LDO_V1P05	V1P05	S3	8 (E6XX)	100	0
LDO_VUNI	V1P2_S	S0	9 (PCH)	0	272
PD_V3P3	V3P3_S	S0	10 (E6XX & PCH)	100	26
LDO_V1P5	V1P5_S	S0	11 (E6XX)	120	0
BUCK_V1P05	V1P05_S	S0	12 (E6XX)	3387	0
BUCK_GRAPHIC	VNN_S	S0	13 (E6XX)	1600	0
PD_V1P8	V1P8_S	S0	14 (E6XX)	180+(390)	0
LDO_V0P9	V0P9_S	S0	15 (DDR2)	375	0
LDO_V1P25	V1P25_S	S0	16 (E6XX)	2	0
BUCK_CORE	VCC_S	S0	17 (E6XX)	3500	0



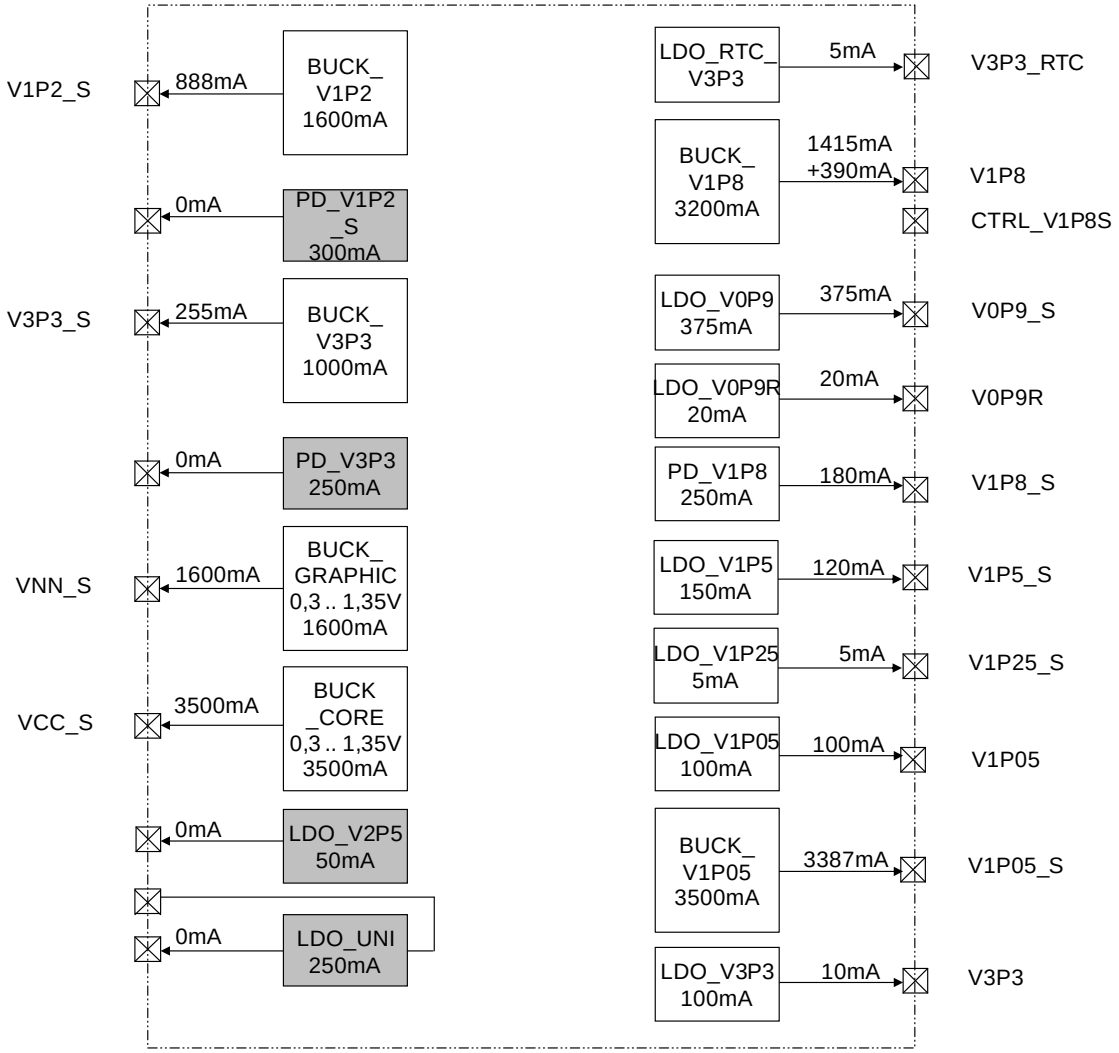
2.2.2 Atom™ E6xx processor & ST STA2X11 ConneXt IO-Hub

Supply Module	Voltage domain	First active state	Sequence	Current E6XX [mA]	Current IO_Hub [mA]
LDO_RTC_V3P3	V3P3_RTC	S4/5	0 (E6XX)	5	0
LDO_V3P3	V3P3	S3	1 (E6XX)	10	0
BUCK_V1P8	V1P8	S3	2 (E6XX & DDR2)	1415	0
LDO_V0P9R	V0P9R	S3	3 (DDR2)	20	0
LDO_V1P05	V1P05	S3	4 (E6XX)	100	0
BUCK_V3P3	V3P3_S	S0	5 (E6XX & ST)	100	200
LDO_V1P5	V1P5_S	S0	6 (E6XX)	120	0
BUCK_V1P05	V1P05_S	S0	7 (E6XX)	3387	0
BUCK_GRAPHIC	VNN_S	S0	8 (E6XX)	1600	0
LDO_VUNI	V2P5_S	S0	9 (ST)	0	250
PD_V1P8	V1P8_S	S0	10 (E6XX & ST)	180+(390)	50
BUCK_V1P2	V1P2_S	S0	11 (ST)	0	1000
LDO_V0P9	V0P9_S	S0	12 (DDR2)	375	0
LDO_V1P25	V1P25_S	S0	13 (E6XX)	2	0
BUCK_CORE	VCC_S	S0	14 (E6XX)	3500	0



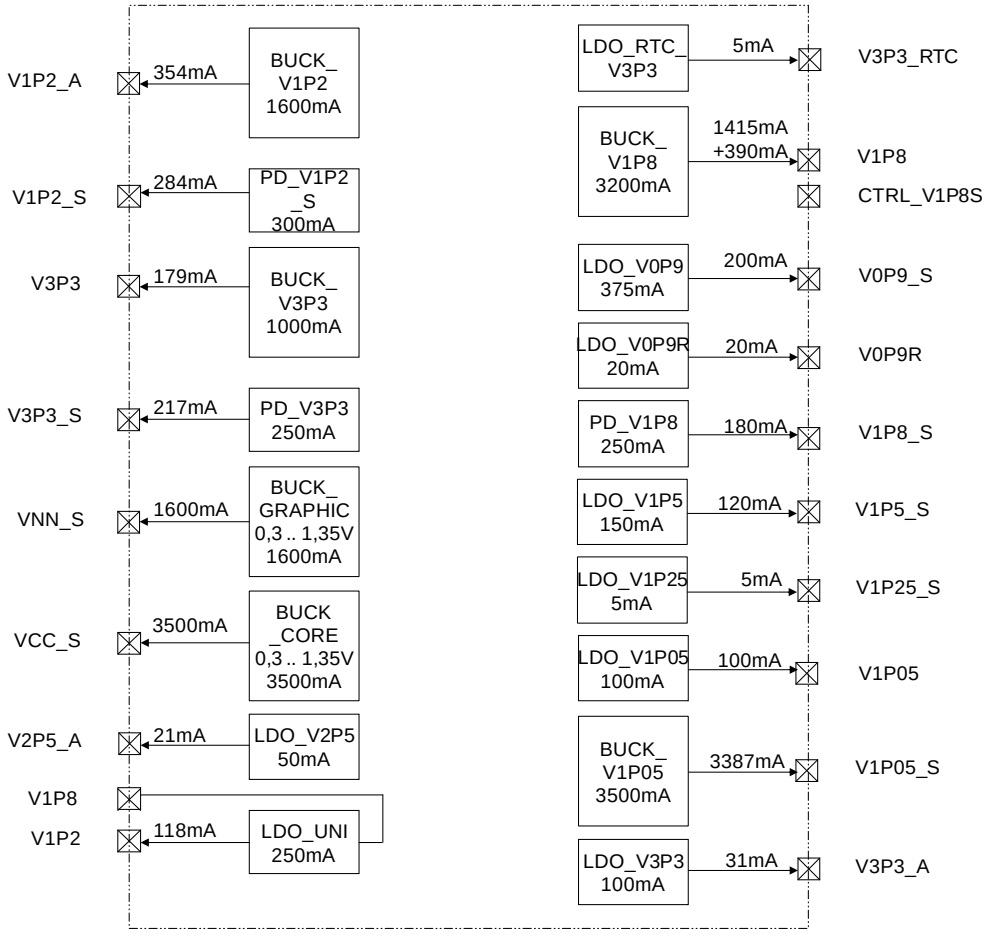
2.2.3 Atom™ E6xx processor & OKI Semiconductor ML7213 IVI IO-Hub

Supply Module	Voltage domain	First active state	Sequence	Current E6XX [mA]	Current IO-Hub [mA]
LDO_RTC_V3P3	V3P3_RTC	S4/5	0 (E6XX)	5	0
LDO_V3P3	V3P3	S3	1 (E6XX)	10	0
BUCK_V1P8	V1P8	S3	2 (E6XX & DDR2)	1415	0
LDO_V0P9R	V0P9R	S3	3 (DDR2)	20	0
LDO_V1P05	V1P05	S3	4 (E6XX)	100	0
BUCK_V3P3	V3P3_S	S0	5 (E6XX & OKI)	100	155
LDO_V1P5	V1P5_S	S0	6 (E6XX)	120	0
BUCK_V1P2	V1P2_S	S0	7 (OKI)	0	888
BUCK_V1P05	V1P05_S	S0	8 (E6XX)	3387	0
BUCK_GRAPHIC	VNN_S	S0	9 (E6XX)	1600	0
PD_V1P8	V1P8_S	S0	10 (E6XX)	180+(390)	0
LDO_V0P9	V0P9_S	S0	11 (DDR2)	375	0
LDO_V1P25	V1P25_S	S0	12 (E6XX)	2	0
BUCK_CORE	VCC_S	S0	13 (E6XX)	3500	0



2.2.4 Atom™ E6xx processor & OKI Semiconductor ML7223 MP IO-Hub

Supply Module	Voltage domain	First active state	Sequence	Current [mA]	Current IO-Hub [mA]
LDO_RTC_V3P3	V3P3_RTC	S4/5	0 (E6XX)	5	0
BUCK_V1P2	V1P2_A	S4/5	1 (OKI MP)	0	354
LDO_V2P5	V2P5_A	S4/5	2 (OKI MP)	0	21
LDO_V3P3	V3P3_A	S4/5	3 (OKI MP)	0	31
PD_V1P2	V1P2	S3	4 (OKI MP)	0	118
BUCK_V3P3	V3P3	S3	5 (E6XX & OKI)	10	269
BUCK_V1P8	V1P8	S3	6 (E6XX & DDR2)	1415	0
LDO_V0P9R	V0P9R	S3	7 (DDR2)	20	0
LDO_V1P05	V1P05	S3	8 (E6XX)	100	0
LDO_VUNI	V1P2_S	S0	9 (OKI MP)	0	284
PD_V3P3	V3P3_S	S0	10 (E6XX & OKI)	100	17
LDO_V1P5	V1P5_S	S0	11 (E6XX)	120	0
BUCK_V1P05	V1P05_S	S0	12 (E6XX)	3387	0
BUCK_GRAPHIC	VNN_S	S0	13 (E6XX)	1600	0
PD_V1P8	V1P8_S	S0	14 (E6XX)	180+(390)	0
LDO_V0P9	V0P9_S	S0	15 (DDR2)	375	0
LDO_V1P25	V1P25_S	S0	16 (E6XX)	2	0
BUCK_CORE	VCC_S	S0	17 (E6XX)	3500	0



2.3 ELECTRICAL CHARACTERISTICS

The DA6011 PMIC includes six DC-to-DC Buck converters, two with DVC (Dynamic voltage control), and four generating a fixed output voltage.

Phase Shift

A 4 phase clock is used for clocking the buck regulators. The input clock of the phase shifter is the clock output from the spread spectrum clock generator. This is graphically illustrated in Figure 2.

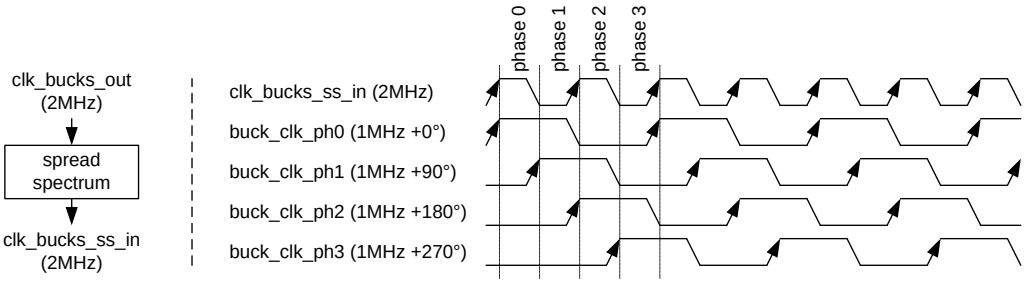


Figure 2: Phase shifting for buck convertors

Since there are in total 6 buck convertors, the phases will be distributed as follows:

- buck_clk_ph0: BUCK_CORE
- buck_clk_ph1: BUCK_GRAPHIC, BUCK_3P3, BUCK_1P2
- buck_clk_ph2: BUCK_1P05
- buck_clk_ph3: BUCK_1P8

Spread Spectrum

All buck regulators should run with a spread spectrum frequency to avoid EMI. The spread is defined to be around ± 45 kHz.

DA6011 will also include low noise, high performance LDO voltage regulators.

The LDO's will have two modes of operation:

Disabled (OFF mode)
Enabled (ON mode)
A power saving mode is not required for the LDO's due to the use of dynamic biasing in the LDO internal circuitry

2.3.1 BUCK_CORE with DVC

The BUCK_CORE converter is a high efficiency synchronous step down regulator operating at a high frequency (1 MHz) supplying a voltage (VCC_S) of 0.3 … 1.35V 3500mA max, with ±3% voltage accuracy at 1.1V. As the output current is 3,5A this buck regulator needs external switching devices.

The DVC controller allows the following features:

1. The Buck converter output voltage to be programmable over the VID [6:0] interface in the range 0.30V to 1.35V in 12.5mV steps.
2. The buck switches automatically from the synchronous mode into pulse skipping mode according the load applied to the output of the buck converter.

The supply current during PWM (synchronous rectification) operation is in the order of 1mA (Quiescent current and charge/discharge current) and drops to <1µA in shutdown. Switching frequency is chosen to be high enough to allow the usage of a small 1.5µH inductor.

DVC control of the Buck:

The output voltage of the buck regulator is controlled by the VID signal. The DAC of the regulator should be controlled by the VID bits, with VID0 as LSB and VID6 as the MSB. A de-bounce time of 100ns between the steps is required.

Electrical Characteristics (Ta = -40 to +85 ºC)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VSUP_C	Input Voltage		4.5		5.25	V
VCC_S	Output Voltage		0.30	[Note1]	1.35	V
VCC_S ○ VID >= 0.75v ○ VID < 0.75v	Output Accuracy	[NOTE2]	 -1.5 -11.5		 1.5 +11.5	 % mV
○ Static load regulation		Iout = 0…3500mA		-5.9		mV/A
○ IMAX	Maximum Output Current		3500			mA
ILIMIT	Current limitation			5900±20%		mA
TON	Turn on time				2	ms
IQ_OFF Mode	Quiescent Current in Off				1	µA
Rpd power-down	Pull down resistor in	Measured @ Vout=0.5V			200	Ω
Normal Mode – Synchronous rectification (PWM)						
F_BUCK	Frequency of operation			1		MHz
IQ_ON current	normal mode static	Internal quiescent current		**0.**4		mA
VBOOT	Boot up voltage			1.1±1.5%		V
dI_{VCC}/dt V_{VCC} power supply current slew rate		dI_{OUT}/dt		2.5		A/µs
Efficiency		[NOTE3]	70	80	85	%
Sleep Mode – Pulse skipping						
The output voltage ripple				20		mV
Efficiency		[NOTE3]		80		%
Gate Driver						
Minimum pulse width			100			ns
Non overlapping time (dead time)			20		100	ns
High side driver source resistance		I_{VHS} = 100mA			1.0	Ω
High side driver sink resistance		I_{VHS} = -100mA			0.5	Ω

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Low side driver source resistance	I_{VLS} = 100mA			1.0	Ω
Low side driver sink resistance	I_{VLS} = -100mA			0.5	Ω
Suggested External components					
Cout Output Capacitor ○ low frequency polymer covered Al SPCap, AO Cap 1 * 220µF ○ Mid frequency 0603MLCC 1*47µ XR7 ○ High frequency 0402 MLCC 6*1µF XR7	Valid for the Intel E6xx series platform	-20% -10% -10%	1x220 1x47 6x1	+20% +10% +10%	µF
ESR of output capacitor ○ Low frequency ○ Mid frequency ○ High frequency	Valid for the Intel E6xx series platform		9 7.7 30		mΩ
ESL of output capacitor ○ Mid frequency ○ High frequency			551 400		pH
L_BUCK inductor value		-20%	1.5	+20%	µH
L_ESR inductor resistance			0.050		Ω
R_SENSE current sense resistor			10		mΩ
R_PMOS external PMOS on resistance	SI7540DP µPA1890 µPA2792 FDS8858CZ			0.05	Ω
R_NMOS external NMOS on resistance	SI7540DP µPA1890 µPA2792 FDS8858CZ			0.046	Ω
VCC/VSS_sense [NOTE4]				10	mΩ

Table 5: electrical parameters for BUCK_CORE

[Note 1] Programmable in 12.5mV steps up to 1.35V
[Note 2] The output voltage accuracy is measured from ideal load line, which is defined in load regulation.
[Note 3] Typical condition, all suggested external components are used
[Note 4] Impedance of PCB sense trace from CPU power pin to device pad

The buck core is controlled via the VID[6:0] and VIDEN[1:0] pins see chapter 2.3.2.1

2.3.2 BUCK_GRAPHIC with DVC

The BUCK_Graphic converter is a high efficiency synchronous step down regulator operating at a high frequency (1 MHz) supplying a voltage (VNN_S) of 0.3 … 1.35V 1600mA max, with ±3% voltage accuracy at 0.9V. As the output current is 1,6A this buck regulator can run with internal switching devices.

The DVC controller allows the following features:

1. The Buck converter output voltage to be programmable over the VID [6:0] interface in the range 0.30V to 1.35V in 12.5mV steps.
2. The buck switches automatically from the synchronous mode into pulse skipping mode according the load applied to the output of the buck converter.

The supply current during PWM (synchronous rectification) operation is in the order of 1mA (Quiescent current and charge/discharge current) and drops to <1µA in shutdown. Switching frequency is chosen to be high enough to allow the usage of a small 1.5µH inductor.

DVC control of the Buck:

The output voltage of the buck regulator is controlled by the VID signal. The DAC of the regulator should be controlled by the VID bits, with VID0 as LSB and VID6 as the MSB. A de-bounce time of 100ns between the steps is required.

Electrical Characteristics (Ta = -40 to +85 ºC)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VSUP_G	Input Voltage		4.5		5.25	V
Cout ○ Intel Platform Design Guide ○ low frequency polymer covered Al SPCap, AO Cap 1 * 220µF ○ Mid frequency 0402 MLCC 1*47µ XR7 ○ High frequency 0402 MLCC 4*1µ XR5		Valid for the Intel E6xx series platform	 -20% -10% -10%	 1x220 1x47 4x1	 +20% +10% +10%	µF
ESR of output capacitor ○ Low frequency ○ Mid frequency ○ High frequency		Valid for the Intel E6xx series platform			 9 7.7 30	mΩ
ESL of output capacitor ○ Mid frequency ○ High frequency		Valid for the Intel E6xx series platform			 551 400	pH
L_BUCK	inductor value		-20%	1.5µ	+20%	µH
L_ESR	inductor resistance			0.05		Ω
VNN_S	Output Voltage	IOUT= Imax	0.30	[Note1]	1.35	V
VNN_S	Output Accuracy	IOUT= Imax VID ≥ 0.75V VID < 0.75V	 -1.5 -11.5		 1.5 11.5	 % mV
F_BUCK	Frequency of operation			1		MHz
Ton	Turn on time				2	ms
VNN/VSS_sense from Graphic CPU	impedance of sense wire to VR	Kelvin point measurement			5.7	m Ω
IQ_OFF Mode	Quiescent Current in Off				1	µA
Rpd power-down	Pull down resistor in	Measured @ Vout=0.5V			200	Ω

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Normal Mode – Synchronous rectification (PWM)					
Maximum Output Current (Imax)		1600			mA
ILIMIT Current limitation			2000 ±20%		mA
Boot up voltage for V_{NN_S} V_{BOOT}			0.9		V
Maximum overshoot voltage	No load			100	mV
$dI_{NN\ Graphic}/dt$ $V_{NN\_Graphic}$ power supply current slew rate				2.5	A/µs
Static load regulation	Iout = 0…1200mA		-5,9		mV/A
Efficiency	Iout = 600 to 1200mA Vbuck=0.9V	70	80	85	%
Sleep Mode – Pulse skipping (PSK)					
Output Voltage Ripple			20		mV
Efficiency		60			%

Table 6: electrical parameters for BUCK_GRAPHIC

[Note 1] Programmable in 12.5mV steps up to 1.35V

2.3.2.1 VID settings for DC/DC converters with DVC

The core and the graphic buck converter are controlled VID[6:0] setting plus the Voltage ID Enable signals VIDEN[1:0]. The following table shows the digital representation and the corresponding output voltage of the buck regulators including DVC.

PARAMETER	Bus contents	Output voltage	comments
VID<6:0>	0001100	1.350V	Max programmable core & graphic voltage
	0001101	1.3375V	
	0001110	1.325V	
	…	…	
	010 0000	**1.100V**	Initial core voltage
	010 0001	1.0875V	
	010 0010	1.075	
	….	….	
	010 1111	0.9125V	
	011 0000	**0.900V**	Initial graphic voltage
	011 0001	0.8875V	
	….	….	
	1011011	0.3625V	
	1011100	0.350V	
	…	…	
	1100000	0.3V	

Table 7: VID output voltage mapping

The VIDEN[1:0] pins will indicate which voltage is being specified with the VID[6:0] pins. Following table represents the allocation

VIDEN[1:0]	Regulator
0 0	VID invalid
0 1	VID = BUCK_CORE
1 0	VID = BUCK_GRAPHIC
1 1	VID invalid

If VIDEN is invalid, the output voltage of the CORE and GRAPHIC buck convertors remains at the last valid setting (initial: VCC_S = 1.1V, VNN_ = 0.9V).

2.3.3 BUCK_1P05

The BUCK_V1P05 converter is a high efficiency synchronous step down regulator operating at a frequency (1MHz) supplying a default voltage of 1.05V, 3500mA max, with ±3% voltage accuracy. This regulator is using external switching devices (P/NMOS) as the output current which is too high to be integrated on a quarter micron CMOS process. Current sensing will be done via a sense resistor (10 mΩ) in series to the coil. During abrupt changes in the load current, the bulk and decoupling capacitors must supply current for the brief period before the regulator circuit can respond.

Electrical Characteristics (Ta = -40 to +85 ºC)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VSUP_1P05	Input Voltage		4.5		5.25	V
V1P05_S	Output Voltage			1.05		V
	Output Accuracy	[NOTE1]	-3		3	%
Static load regulation		Iout = 0…3500mA		-5.9		mV/A
IMAX Current	Maximum Output			3500		mA
ILIMIT	Current limitation			5900±20%		mA
TON	Turn on time				2	ms
IQ_OFF Mode	Quiescent Current in Off				1	µA
Rpd power-down	Pull down resistor in	Measured @ Vout=0.5V			200	Ω
Normal Mode – Synchronous rectification (PWM)						
F_BUCK	Frequency of operation			1		MHz
IQ_ON current	normal mode static	Internal quiescent current		**0.**4		mA
Efficiency		[NOTE2]	70	80	85	%
Sleep Mode – Pulse skipping						
The output voltage ripple				20		mV
Efficiency		[NOTE2]	70	80	85	%
Gate Driver						
Minimum pulse width			100			ns
Non overlapping time (dead time)			20		100	ns
High side driver source resistance		I_{VHS} = 100mA			1.0	Ω
High side driver sink resistance		I_{VHS} = -100mA			0.5	Ω
Low side driver source resistance		I_{VLS} = 100mA			1.0	Ω
Low side driver sink resistance		I_{VLS} = -100mA			0.5	Ω
Suggested External components						
Cout			-20%	2x22 Or	+20%	µF
			-20%	1x47µ	+20%	
○ VCCD		Valid for the Intel E6xx series platform	-10%	10x1	+10%	
○ VCCQ			-10%	6x1	+10%	
○ VCCP			-10%	6x1	+10%	
○ VCCPAOAC			-10%	4x1	+10%	
○ VCCRTCEXT			-10%	0.1	+10%	
○ VCCDPL			-10%	1	+10%	
○ VCCQHPLL			-20%	22	+20%	
			-10%	0.1	+10%	
○ VCCPDDR			-5%	47p	5%	
ESR of output capacitor		F > 100kHz (all cap's + track impedance			10	mΩ
L_BUCK	inductor value		-20%	1.5	+20%	µH

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L_ESR	inductor resistance				0.050	Ω
R_SENSE	current sense resistor			10		mΩ
R_PMOS external	PMOS on resistance	SI7540DP µPA1890 µPA2792 FDS8858CZ			0.05	Ω
R_NMOS external	NMOS on resistance	SI7540DP µPA1890 µPA2792 FDS8858CZ			0.046	Ω

Table 8: Electrical parameter for BUCK_1P05

2.3.4 BUCK_1P2

The BUCK_V1P2 converter is a high efficiency synchronous step down regulator operating at a frequency (1MHz) supplying a default voltage of 1.2V, 1600mA max, with ±3% voltage accuracy.

Electrical Characteristics (Ta = -40 to +85 ºC)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VSUP_1P2	Input Voltage		4.5		5.25	V
Cout ○ Low frequency polymer covered AL SPCap, AO Cap 1 * 220µF ○ Mid frequency 0402 MLCC 1 * 47µF XR7 ○ High frequency 0402 MLCC 4 * 1µF XR5			 -20% -10% -10%	 220 47 4x1	 +20% +10% +10%	 µF µF µF
ESR of output capacitor		F > 100kHz (all cap's + track impedance		20	50	mΩ
L_BUCK	inductor value		-30%	1.5	+30%	µH
L_ESR	inductor resistance			0.03	0.12	Ω
V1P2_A V1P2_S	Output Voltage (EG20T/ML7223) (STA2X11/ML7213)	IOUT= Imax		1.2 ±3%		V
F_BUCK	Frequency of operation			1		MHz
Ton	Turn on time				2	ms
IQ_OFF Mode	Quiescent Current in Off				1	µA
Rpd power-down	Pull down resistor in				200	Ω
Normal Mode – Synchronous rectification (PWM)						
Maximum Output Current (Imax)			1600			mA
ILIMIT	Current limitation			2000 ±20%		mA
Static load regulation		Iout = 0…Imax		-5.9		mV/A
Efficiency				80		%
Sleep Mode – Pulse skipping (PSK)						
Output Voltage Ripple				20		mV
Efficiency		IOUT	60			%

Table 9: Electrical parameter for BUCK_1P2

2.3.5 BUCK_1P8.

The BUCK_V1P8 converter is a high efficiency synchronous step down regulator operating at a high frequency (1MHz) supplying a default voltage of 1.8V, 3500mA max, with ±3% voltage accuracy.

This regulator is using external switching devices (P/NMOS) as the output current is too high to be integrated on a quarter micron CMOS process. The supply current during PWM (synchronous rectification) operation is in the order of 1mA (Quiescent current and charge/discharge current) and drops to <1µA in shutdown.

A power saving sleep mode is entered automatically. In sleep mode, the buck converter switches to a pulse-skipping mode that will allow it to operate at high efficiency during very low current operations.

Electrical Characteristics (Ta = -40 to +85 ºC)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VSUP_1P8	Input Voltage		4.5		5.25	V
V1P8	Output Voltage			1.8		V
	Output Accuracy	[NOTE1]	-2		2	%
Static load regulation		Iout = 0…3500mA		-5.9		mV/A
IMAX	Maximum Output Current		3200			mA
ILIMIT	Current limitation			5000±20%		mA
TON	Turn on time				2	ms
IQ_OFF Mode	Quiescent Current in Off				1	µA
Rpd down	Pull down resistor in power-down	Measured @ Vout=0.5V			200	Ω
Normal Mode – Synchronous rectification (PWM)						
F_BUCK	Frequency of operation			1		MHz
IQ_ON	normal mode static current	Internal quiescent current		400		µA
Efficiency		[NOTE2]	75	80	85	%
Sleep Mode – Pulse skipping						
The output voltage ripple				20		mV
Efficiency		[NOTE2]	60			%
Gate Driver						
Minimum pulse width					100	ns
Non overlapping time (dead time)				30		ns
High side driver source resistance		I_{VHS} = 100mA		1.0		Ω
High side driver sink resistance		I_{VHS} = -100mA		0.5		Ω
Low side driver source resistance		I_{VLS} = 100mA		1.0		Ω
Low side driver sink resistance		I_{VLS} = -100mA		0.5		Ω
Suggested External components						
Cout	Output Capacitor		80			µF
ESR of output capacitor		F > 100kHz (all cap's + track impedance			10	mΩ
L_BUCK	inductor value		-20%	1.5	+20%	µH
L_ESR	inductor resistance				0.050	Ω
R_SENSE	current sense resistor				10	mΩ
R_PMOS external	PMOS on resistance	SI7540DP µPA1890 µPA2792 FDS8858CZ			0.05	Ω
R_NMOS external	NMOS on resistance	SI7540DP µPA1890 µPA2792 FDS8858CZ			0.046	Ω

Table 10: Electrical parameter for BUCK_1P8

2.3.6 BUCK_3P3

The BUCK_V3P3 Converter is a high efficiency synchronous step down regulator operating at a high frequency (1MHz) supplying a default voltage of 3.3V, 1000mA max, with a ±3% voltage accuracy.

The supply current during PWM (synchronous rectification) operation is in the order of 1.5mA (Quiescent current and charge/discharge current) and drops to <1µA in shutdown. Switching frequency is chosen to be high enough to allow the usage of a small 4.7µH inductor.

A power saving sleep mode is entered automatically. In sleep mode, the buck converter switches to a pulse-skipping mode that will allow it to operate at high efficiency during very low current operations.

Characteristics (Ta = -40 to +85 ºC)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VSUP_3P3	Input Voltage		4.5		5.25	V
Cout ○ Low frequency polymer covered AL SPCap, AO Cap 1 * 220µF ○ Mid frequency 0402 MLCC 1 * 47µF XR7 ○ High frequency 0402 MLCC 4 * 1µF XR5			 -20% -10% -10%	 220 47 4x1	 +20% +10% +10%	 µF µF µF
ESR of output capacitor ○ Low frequency ○ Mid frequency ○ High frequency					 9 7.7 30	mΩ
ESL of output capacitor ○ Mid frequency ○ High frequency					 551 400	pH
L_BUCK	inductor value		-30%	4.7	+30%	µH
L_ESR	inductor resistance			0.05		Ω
V3P3 V3P3_S	Output Voltage EG20T/ML7223 STA2X11/ML7213	IOUT= Imax		3.3 ±3%		V
F_BUCK	Frequency of operation			1		MHz
Ton	Turn on time				2	ms
IQ_OFF Mode	Quiescent Current in Off				1	µA
Rpd power-down	Pull down resistor in	Measured @ Vout=0.5V			200	Ω
Normal Mode – Synchronous rectification (PWM)						
Maximum Output Current (Imax)			1000			mA
ILIMIT	Current limitation			2000 ±20%		mA
Static load regulation		Iout = 0…Imax		-5.9		mV/A
Efficiency		Iout = 400 to 1000mA Vbuck=3.3V		80		%
Sleep Mode – Pulse skipping (PSK)						
Output Voltage Ripple				20		mV
Efficiency		IOUT	60			%

Table 11: Electrical Parameter for BUCK_3P3

2.3.7 Voltage Regulator LDO_RTC_V3P3

Electrical Characteristics (Ta = -40 to +85 ºC)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VSUP_1 VSUP_3	Input Voltage	Depends on output voltage	4.5 4.5		5.25 5.25	V
V3P3_RTC	Output Voltage	IOUT= Imax		3.3		V
	Output Accuracy	IOUT= Imax	-3		+3	%
Cext	Stabilization capacitor	Tolerance of ± 30%		1.0		µF
IMAX	Maximum Output Current		5			mA
Cesr	ESR of capacitor	F > 1MHz			0.1	Ω
ISHORT	Short Circuit Current				100	mA
VSLINE	Static Line Regulation	VSUP=4.5V to 5.25V, IOUT=IMAX		10	30	mV
VSLOAD	Static Load Regulation	VSUP=4.5V to 5.25V, IOUT = 1mA to IOUT=IMAX		5	30	mV
VTRLINE	Line transient response	VSUP=4.5V to 5.25V, IOUT=IMAX tr = tf = 10µs		5	10	mV
VTRLOAD	Load transient response	VSUP=4.5V IOUT = 1mA to IOUT=IMAX tr = tf = 10µs		15	30	mV
PSRR	Power Supply ratio rejection	F=1kHz	50			dB
IQ_ON	Quiescent Current in ON MODE			25uA + 1% of IOUT		µA
IQ_OFF	Quiescent Current in Off Mode				1	µA
Ton	Turn on time	Max Load			200	µsec
Toff	Turn off time	No Load			1	ms

Table 12: Electrical parameter for LDO_RTC_3V3

2.3.8 Voltage Regulator LDO_V3P3

Electrical Characteristics (Ta = -40 to +85 ºC)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VSUP_1 VSUP_3	Input Voltage	Depends on output voltage	4.5		5.25	V
V3P3 V3P3_A	Output Voltage EG20T/ML7223 STA2X11/ML7213	IOUT= Imax		3.3		V
	Output Accuracy	IOUT= Imax	-3		+3	%
Cext	Stabilization capacitor	Tolerance of ± 30%		1		µF
Cesr	ESR of capacitor	F > 1MHz			0.1	Ω
IMAX	Maximum Output Current		100			mA
ISHORT	Short Circuit Current				300	mA
VSLINE	Static Line Regulation	VSUP=4.5V to 5.25V, IOUT=IMAX		5	20	mV
VSLOAD	Static Load Regulation	VSUP=4.5V to 5.25V IOUT = 1mA to IOUT=IMAX		5	20	mV
VTRLINE	Line transient response	VSUP=4.5V to 5.25V		5	20	mV

		IOUT=IMAX tr = tf = 10µs			
VTRLOAD	Load transient response	VSUP=4.5V IOUT = 1mA to IOUT=IMAX tr = tf = 10µs		15 50	mV
PSRR	Power supply ratio rejection	F =1KHz	50		dB
IQ_ON	Quiescent Current in ON MODE		20µA +1% of IOUT		µA
IQ_OFF	Quiescent Current in Off Mode			1	µA
Ton	Turn on time	Max Load		200	µsec
Toff	Turn off time	No Load		1	ms

Table 13: Electrical parameter for LDO_V3P

2.3.9 Voltage Regulator LDO_V2P5

Electrical Characteristics (Ta = -40 to +85 ºC)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VSUP_1 VSUP_3	Input Voltage	Depends on output voltage	4.5		5.25	V
V2P5_A	Output Voltage EG20T/ML7223	IOUT= Imax		2.5		V
	Output Accuracy	IOUT= Imax	-3		3	%
Cext	Stabilization capacitor	Tolerance of ± 30%		1		µF
Cesr	ESR of capacitor	F > 1MHz			0.1	Ω
IMAX	Maximum Output Current		50			mA
ISHORT	Short Circuit Current				150	mA
VSLINE	Static Line Regulation	VSUP=4.5V to 5.25V, IOUT=IMAX		5	20	mV
VSLOAD	Static Load Regulation	VSUP=4.5V to 5.25V IOUT = 1mA to IOUT=IMAX		5	20	mV
VTRLINE	Line transient response	VSUP=4.5V to 5.25V IOUT=IMAX tr = tf = 10µs		5	20	mV
VTRLOAD	Load transient response	VSUP=4.5V IOUT = 1mA to IOUT=IMAX tr = tf = 10µs		15	50	mV
PSRR	Power supply ratio rejection	F =1KHz	50			dB
IQ_ON	Quiescent Current in ON MODE		20µA +1% of IOUT			µA
IQ_OFF	Quiescent Current in Off Mode				1	µA
Ton	Turn on time	Max Load			200	µsec
Toff	Turn off time	No Load			1	ms

Table 14: Electrical parameter for LDO_V2P5

2.3.10 Voltage Regulator LDO_V1P5

Electrical Characteristics (Ta = -40 to +85 ºC)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD_V1P8	Input Voltage			1.8		V
V1P5_S	Output Voltage	IOUT= Imax		1.5		V
	Output Accuracy	IOUT= Imax	-3		+3	%
Cext	VCCA		-10% -10%	3x1 0.1	+10% +10%	µF
Cesr	ESR of capacitor	F > 1MHz			0.1	Ω
IMAX	Maximum Output Current		150			mA
ISHORT	Short Circuit Current				450	mA
VSLINE	Static Line Regulation	VDD_V1P8 ±2%, IOUT=IMAX		5	20	mV
VSLOAD	Static Load Regulation	VDD_V1P8 ±2%, IOUT = 1mA to IOUT=IMAX		5	20	mV
VTRLINE	Line transient response	VDD_V1P8 ±2%, IOUT=IMAX tr = tf = 10µs		15	50	mV
VTRLOAD	Load transient response	VDD_V1P8 ±2%, IOUT = 1mA to IOUT=IMAX tr = tf = 1µs		15	30	mV
PSRR	Power supply ratio rejection	F =1KHz	50			dB
IQ_ON	Quiescent Current in ON MODE			20µA +1% of IOUT		µA
IQ_OFF	Quiescent Current in Off Mode				1	µA
Ton	Turn on time	Max Load			200	µsec
Toff	Turn off time	No Load			1	ms

Table 15: Electrical parameter for LDO_V1P5

2.3.11 Voltage Regulator LDO_V1P25

Electrical Characteristics (Ta = -40 to +85 ºC)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD_V1P8	Input Voltage			1.8		V
V1P25_S	Output Voltage	IOUT= Imax		1.25		V
	Output Accuracy	IOUT= Imax	-2		+2	%
Cext	Stabilization capacitor	Tolerance of ± 30%		0.22		µF
Cesr	ESR of capacitor	F > 1MHz			0.1	Ω
IMAX	Maximum Output Current		5			mA
ISHORT	Short Circuit Current				50	mA
VSLINE	Static Line Regulation	VDD_V1P8 ±2%, IOUT=IMAX		5	20	mV
VSLOAD	Static Load Regulation	VDD_V1P8 ±2%, IOUT = 1mA to IOUT=IMAX		5	20	mV
VTRLINE	Line transient response	VDD_V1P8 ±2%, IOUT=IMAX tr = tf = 10µs		15	30	mV

VTRLOAD	Load transient response	VDD_V1P8 ±2%, IOUT = 1mA to IOUT=IMAX tr = tf = 1µs	15	50	mV
PSRR	Power supply ratio rejection	F =1KHz	50		dB
IQ_ON	Quiescent Current in ON MODE		20µA +1% of IOUT		µA
IQ_OFF	Quiescent Current in Off Mode			1	µA
Ton	Turn on time	Max Load		200	µsec
Toff	Turn off time	No Load		1	ms

Table 16: Electrical parameter for LDO_V1P25

2.3.12 Voltage Regulator LDO_V1P05

Electrical Characteristics (Ta = -40 to +85 ºC)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD_V1P8	Input Voltage			1.8		V
V1P05_S	Output Voltage	IOUT= Imax		1.05		V
	Output Accuracy	IOUT= Imax	-2		+2	%
Cext	Stabilization capacitor	Tolerance of ± 30%		1		µF
Cesr	ESR of capacitor	F > 1MHz			0.1	Ω
IMAX	Maximum Output Current		100			mA
ISHORT	Short Circuit Current				450	mA
VSLINE	Static Line Regulation	VDD_V1P8 ±2%, IOUT=IMAX		5	20	mV
VSLOAD	Static Load Regulation	VDD_V1P8 ±2%, IOUT = 1mA to IOUT=IMAX		5	20	mV
VTRLINE	Line transient response	VDD_V1P8 ±2%, IOUT=IMAX tr = tf = 10µs		15	50	mV
VTRLOAD	Load transient response	VDD_V1P8 ±2%, IOUT = 1mA to IOUT=IMAX tr = tf = 1µs		15	30	mV
PSRR	Power supply ratio rejection	F =1KHz	50			dB
IQ_ON	Quiescent Current in ON MODE		20µA +1% of IOUT			µA
IQ_OFF	Quiescent Current in Off Mode				1	µA
Ton	Turn on time	Max Load			200	µsec
Toff	Turn off time	No Load			1	ms

Table 17: Electrical parameter for LDO_V1P05

2.3.13 Voltage Regulator LDO_V0P9

The LDO_V0P9 is a bi-directional LDO, designed to meet the JEDEC specifications (JESD79-C2) at S3/S5 sleep state for termination of DDR/DDR2 memory bus. The regulator is a high speed operational amplifier to provide excellent response to load transients.

Suspend to RAM (STR) is maintained as well. In the STR mode the output of the regulator will tri-state providing a high impedance output while the reference voltage will remain active.

Electrical Characteristics (Ta = -40 to +85 ºC)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VSUP1 VDD_V0P9	Input Voltage	Core voltage Pass device voltage	4.5	 1.8	5.25	V V
V0P9_S	Output Voltage	IOUT= Imax		0.9		V
	Output Accuracy	IOUT= Imax	-2		+2	%
Cext	Stabilization capacitor	Tolerance of ± 30%		10		µF
IMAX	Maximum Output Current		±375			mA
Cesr	ESR of capacitor	F > 1MHz			0.1	Ω
ISHORT	Short Circuit Current				±600	mA
VSLINE	Static Line Regulation	VDD_V1P2 ±2%, IOUT=IMAX		5	30	mV
VSLOAD	Static Load Regulation	VDD_V1P2 ±2%, IOUT = 1mA to IOUT=IMAX		5	30	mV
VTRLINE	Line transient response	VDD_V1P2 ±2%, IOUT=IMAX tr = tf = 10µs		5	10	mV
VTRLOAD	Load transient response	VDD_V1P2 ±2%, IOUT = 1mA to IOUT=IMAX tr = tf = 10µs		15	30	mV
PSRR	Power supply ratio rejection	F =1KHz	50			dB
IQ_ON	Quiescent Current in ON MODE			25uA + 1% of IOUT		µA
IQ_OFF	Quiescent Current in Off Mode				1	µA
Ton	Turn on time	Max Load			200	µs
Toff	Turn off time	No Load			1	ms

Table 18: Electrical parameter for LDO_V0P9

2.3.14 Voltage Regulator LDO_V0P9R

Buffered reference voltage of V1P8/2. In the STR Mode this amplifier remains active.
Default at start-up is enabled at V1P8/2

Electrical Characteristics (Ta = -40 to +85 ºC)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V1P8	Input Voltage			1.8		V
V0P9R	Output Voltage	IOUT= Imax		0.9		V
	Output Accuracy	IOUT= Imax	-2		+2	%
Cext	Stabilization capacitor	Tolerance of ± 30%		1.0		µF
IMAX	Maximum Output Current		25			mA
Cesr	ESR of capacitor	F > 1MHz			0.1	Ω
ISHORT	Short Circuit Current				60	mA
VSLINE	Static Line Regulation	VDD_V1P2 ±2%, IOUT=IMAX		5	30	mV
VSLOAD	Static Load Regulation	VDD_V1P2 ±2%, IOUT = 1mA to IOUT=IMAX		5	30	mV
VTRLINE	Line transient response	VDD_V1P2 ±2%, IOUT=IMAX tr = tf = 10µs		5	10	mV
VTRLOAD	Load transient response	VDD_V1P2 ±2%, IOUT = 1mA to IOUT=IMAX tr = tf = 10µs		15	30	mV
PSRR	Power supply ratio rejection	F=1kHz	50			dB
IQ_ON	Quiescent Current in ON MODE			25uA + 1% of IOUT		µA
IQ_OFF	Quiescent Current in Off Mode				1	µA
Ton	Turn on time	Max Load			200	µs
Toff	Turn off time	No Load			1	Ms

Table 19: Electrical parameter for LDO_0V9R

2.3.15 Voltage Regulator LDO_VUNI

Default at start-up is 2.5/1.2V depending on the OTP setting and the supply voltage.

Electrical Characteristics (Ta = -40 to +85 ºC)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD_VUNI	Input Voltage	Depends on output voltage		1.8 3.3		V
VUNI V1P2_S V2P5_S	Output Voltage EG20T/ML7223 STA2X11	IOUT= Imax		 1.2 2.5		V
	Output Accuracy	IOUT= Imax	-2		2	%
Cext	Stabilization capacitor	Tolerance of ± 30%		2.2		µF
Cesr	ESR of capacitor	F > 1MHz			0.1	Ω
IMAX	Maximum Output Current	Vout = 2.5V Vout = 1.2V	250 290			mA mA
ISHORT	Short Circuit Current				450	mA
VSLINE	Static Line Regulation	VDD-UNI, IOUT=IMAX		5	20	mV

VSLOAD	Static Load Regulation	VDD_UNI, IOUT = 1mA to IOUT=IMAX	5	20	mV
VTRLINE	Line transient response	VDD_UNI, IOUT=IMAX tr = tf = 10µs	15	30	mV
VTRLOAD	Load transient response	VDD_UNI, IOUT = 1mA to IOUT=IMAX tr = tf = 10µs	15	50	mV
PSRR	Power supply ratio rejection	F=1kHz	50		dB
IQ_ON	Quiescent Current in ON MODE		20µA +1% of IOUT		µA
IQ_OFF	Quiescent Current in Off Mode			1	µA
Ton	Turn on time	Max Load		200	µsec
Toff	Turn off time	No Load		1	ms

Table 20: Electrical parameter for LDO_VUNI

2.3.16 Pass Device PD_V3P3

Electrical Characteristics (Ta = -40 to +85 ºC)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V3P3_IN	Input Voltage	Depends on output voltage		3.3		V
V3P3_S	Output Voltage	IOUT= Imax		3.3		V
	Output Accuracy	IOUT= Imax	-5		+3	%
Cext	Stabilization capacitor VCCP33 VCCP33SUS	 Tolerance of ± 10% Tolerance of ± 10%		 4x1 2x0.1		µF
IMAX	Maximum Output Current		250			mA
VDROPOUT	Dropout Voltage	IOUT= Imax			54	mV

Table 21: Electrical parameter for PD_V3P3

2.3.17 Pass Device PD_V1P8

Electrical Characteristics (Ta = -40 to +85 ºC)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V1P8_IN	Input Voltage	Depends on output voltage		1.8V		V
V1P8_S	Output Voltage	IOUT= Imax		1.8V		V
	Output Accuracy	IOUT= Imax	-5			%
Cext	Stabilization capacitor VCCD180 VCCA180 VCCSFRDPLL VCCSFR_EXP VCCSDFRHPLL	 Tolerance of ± 10% Tolerance of ± 20% Tolerance of ± 10% Tolerance of ± 10% Tolerance of ± 10% Tolerance of ± 20%		 2x1 10 0.1 0.1 1 22		µF
IMAX	Maximum Output Current		250			mA

VDROPOUT	Dropout Voltage	IOUT= Imax		54	mV
IQOFF	Quiescent Current in Off Mode			1	µA

Table 22: Electrical parameter for PD_V1P8

2.3.18 Pass Device PD_V1P2

Electrical Characteristics (Ta = -40 to +85 ºC)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V1P2_IN	Input Voltage			1.2		V
V1P2	Output Voltage	IOUT= Imax		1.2		V
	Output Accuracy	IOUT= Imax	-5			%
Cext	Stabilization capacitor	Tolerance of ± 30%		4.7		µF
IMAX	Maximum Output Current		150			mA
VDROPOUT	Dropout Voltage	IOUT= Imax			24	mV
IQOFF	Quiescent Current in Off Mode				1	µA

Table 23: Electrical parameter for PD_V1P2_S

2.3.19 Low Noise Voltage Regulator LDO_VINT

The regulator LDO_VINT is always switched on. Default at start-up is 2.65V, enabled. OTP trimmed to achieve the 1% accuracy. Electrical Characteristics (Ta = -40 to +85 ºC)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VSUP_1 VSUP_2	Input Voltage		4.5		5.25	V
VINT	Output Voltage	IOUT= Imax		2.65		V
	Output Accuracy	IOUT= Imax	-1		1	%
Cext	Stabilization capacitor	Tolerance of ± 30%		1.0		µF
Cesr	ESR of capacitor	F > 1MHz			0.1	Ω
IMAX	Maximum Output Current		100			mA
ISHORT	Short Circuit Current				450	mA
VSLINE	Static Line Regulation	VSUP=4.5V to 5.25V, IOUT=IMAX		5	20	mV
VSLOAD	Static Load Regulation	VSUP=4.5V to 5.25V, IOUT = 1mA to IMAX		5	20	mV
VTRLINE	Line transient response	VSUP=4.5V to 5.25V, IOUT=IMAX tr = tf = 10µs		15	30	mV
VTRLOAD	Load transient response	VSUP=4.5V to 5.25V, IOUT = 1mA to IMAX tr = tf = 10µs		15	50	mV
PSRR	Power supply ratio rejection	F =1kHz	50			dB
IQ_ON	Quiescent Current in ON			20µA +1% of IOUT		µA
IQ_OFF	Quiescent Current in Off Mode				1	µA
Ton	Turn on time	Max Load			200	µs
Toff	Turn off time	No Load			1	ms

Table 24: Electrical parameter for LDO_VINT

2.3.20 LDO_LP LOW POWER REGULATOR

The LDO_LP will be used for running the internal sequencer. It is supplied by the system supply voltage VSUP. This allows a power up prior the system power domains. This LDO acts as the supply for the bias, reference, OTP and the SMBus registers.

Electrical Characteristics (Ta = -40 to +85 ºC) VSUP = 4.5 to 5.25V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VSUP_1 VSUP_2	Input Voltage		4.5		5.25	V
VLP	Output Voltage	IOUT= Imax	2.45	2.5	2.55	V
Cext	Stabilization capacitor	Tolerance of ± 35%		220		nF
Cesr	ESR of capacitor	F > 1MHz			0.1	Ω
IMAX	Maximum Output Current		5			mA
ISHORT	Short Circuit Current				50	mA
IQ_ON	Quiescent Current in ON MODE			20µA +1% of IOUT		µA
IQ_OFF	Quiescent Current in Off Mode				1	µA
Ton	Turn on time	Max Load			200	µs
Toff	Turn off time	No Load			1	ms

Table 25: Electrical parameter for LDO_LP

3 Clock Synthesizer/Generator

3.1 Atom™ E6xx Processor Clock Supplies

E6xx processor has to be supplied by several clock frequencies to support its various interfaces. The table below shows the DA6011 clocks which will be provided to the Atom™ processor

Clock Domain	E6xx processor Signal Name	Frequency	Signal type	Usage	Active
CPU	BCLKP/BCLKN	100MHz	differential	Processor reference clock	S0
Overlay	HPLL_REFCLK_P HPLL_REFCLK_N	100MHz	differential	Processor overlay reference clock	S0
ITP	XDP_BCLKP XDP_BCLKN	100MHz	differential	eXtended Debug Port	S0
PCI Express	PCIe_CLKINP PCIe_CLKINN	100MHz	differential	PCIe port	S0
Display reference clock	SDVO_REFCLKP SVDO_REFCLKN	96MHz	differential	Primary clock source for display clocks and HD audio	S0
CLK14	CLK14	14.31818MHz	Unbalanced (3.3V)	Used by the 8254 timers. Clock stops at S4/5 state	S3

3.2 IO-Hub Clock Supplies

3.2.1 EG20T Platform Controller Hub Clock Supplies

EG20T Platform Controller Hub will be supplied by several clocks from DA6011. The table below shows the DA6011 clocks which will be provided to EG20T.

Clock Domain	EG20T Signal Name	Frequency	Signal type	Usage	Active
PCI Express	PCIE_CLKP PCIE_CLKN	100MHz	differential	PCIe port	S0
SATA connection	SATA_CLKP SATA_CLKN	75MHz	differential	SATA reference clock	S0
USB	USB_48MHz	48MHz	Unbalanced (3.3V)	USB reference clock	S0/3
Main Clock	SYS_25MHz	25MHz	Unbalanced (3.3V)	EG20T main Clock supply	S0/3/4/5
UART	MCLK	50MHz	Unbalanced (3.3V)	Audio reference clock	S0

3.2.2 ST ConneXt STA2X11 IO-Hub Clock Supplies

ConneXt IO-Hub will be supplied by several clocks from DA6011. The table below shows the DA6011 clocks which will be provided to ConneXt

Clock Domain	ConneXt Signal Name	Frequency	Signal type	Usage	Active
PCI Express	PCIE_CLK_P PCIE_CLK_N	100MHz	differential	PCIe port	S0
SATA connection	SATA_CLK_P SATA_CLK_N	100MHz	differential	SATA reference clock	S0
Ethernet (optional*)		50MHz	Unbalanced (3.3V)	Ethernet	S0
Main Clock	SXTALI	24MHz	Unbalanced (2.5V)	ConneXt main Clock supply	S0

***) crystal frequency accuracy must be adapted to requested Ethernet frequency accuracy**

3.2.3 OKI Semiconductor ML7213 IVI IO-Hub Clock Supplies

OKI IVI IO-Hub will be supplied by several clocks from DA6011. The table below shows the DA6011 clocks which will be provided to OKI IVI Hub

Clock Domain	ML7213 Signal Name	Frequency	Signal type	Usage	Active
PCI Express	PCIE_CLKP PCIE_CLKN	100MHz	differential	PCIe port	S0
SATA connection	SATA_CLKP SATA_CLKN	75MHz	Differential (LVDS)	SATA reference clock	S0
USB_48MHz	USB_48MHz	48MHz	Unbalanced (3.3V)	USB reference clock	S0
Main Clock	SYS_25MHz	25MHz	Unbalanced (3.3V)	Main Clock supply	S0
Audio	MCLK	12.288MHz	Unbalanced (3.3V)	Audio reference clock	S0

3.2.4 OKI Semiconductor ML7223 MP IO-Hub Clock Supplies

OKI Semiconductor MP IO-Hub will be supplied by several clocks from DA6011. The table below shows the DA6011 clocks which will be provided to OKI Semiconductor MP IO-Hub.

Clock Domain	ML7223 Signal Name	Frequency	Signal type	Usage	Active
PCI Express	PCIE_CLKP PCIE_CLKN	100MHz	differential	PCIe port	S0
SATA connection	SATA_CLKP SATA_CLKN	75MHz	Differential (LVDS)	SATA reference clock	S0
USB	USB_48MHz	48MHz	Unbalanced (3.3V)	USB reference clock	S0/3
Main Clock	SYS_25MHz	25MHz	Unbalanced (3.3V)	OKI MP main Clock supply	S0/3/4/5
Audio	MCLK	12.288MHz	Unbalanced (3.3V)	Audio reference clock	S0

3.3 PLL Clock generation

DA6011 will incorporate 4 fractional/spread spectrums PLL's to provide clock signals to the E6xx processor, an IO-Hub as well as to one additional PCIe device. All output clocks of the PLL are designed to be low power differential push-pull pairs or unbalanced clock signal. Noise shaping fractional divider are used for minimum spurious in the spectrum. The reference clock for the PLL's are generated via the 14.31818MHz crystal oscillator. It is assumed that the reference clock has frequency accuracy better than ±100ppm to source the E6xx processor platform with the appropriate frequencies at the requested accuracy.

3.3.1 Clock generator

Electrical Characteristics (Ta = -40 to +85 ºC)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCC_PLL1 VCC_PLL2 VCC_PLL3 VCC_PLL5	Supply Voltage			2.65±1%		V
VCCIO_REF	3V3 reference clock supply			3.3±5%		V
VCCIO_PLL1 VCCIO_PLL23	diff. push pull pair supply			1.2±5% or 1.8±5%		V
VCCIO_SYS	IO-Hub clock supply			3.3±5% 2.5±5%		V
I_ON	Operating supply current			70		mA
I_OFF Mode	Quiescent Current in Off			1		µA
Output frequency	PLL1 incl. Spread spectrum	f_{XO}=14.31818 MHz		100		MHz
	PLL2			96/48/24		MHz
	PLL3			100/75/25		MHz
	PLL5			12.288/50		MHz
Output frequency accuracy	PLL1 incl. Spread spectrum			±100		ppm
	PLL2			±100		ppm
	PLL3			±300		ppm
	PLL5			±100		ppm
f_{SSMOD} Spread spectrum modulation frequency		Triangular modulation	30		33	kHz
C_{OUT}				5		pF
Ton	Turn on time				1.8	ms
$PLL1_{C2C}$ Cycle 2 Cycle	PLL1 Jitter	Differential measured			85	ps
$PLL2_{C2C}$ Cycle 2 Cycle	PLL2 Jitter				250	ps
$PLL3_{C2C}$ Cycle 2 Cycle	PLL3 Jitter				125	ps
14.σ PLL3 Random Jitter contribution, Jitter Transfer Function filtered for STA2X11				3.18		ps

$PLL5_{C2C}$ PLL5 Jitter Cycle 2 Cycle				250	ps
Differential outputs					
Rising edge slew rate		2.5		8.0	V/ns
Falling edge slew rate		2.5		8.0	V/ns
Rise/Fall Time Variation	Single ended			20	%
Maximum output voltage differential	Overshoot included			1150	mV
Minimum output voltage differential	Undershoot included	-300			mV
Duty cycle	Differential measured	45		55	%
Differential voltage swing		300			mV
Crossing Point Variation	Single ended			140	mV
Cross Point Voltage	Single ended	300		550	mV
Single Ended CLK14,USB output					
Rising slew rate	Measured from 0.8V to 2.0V	1		2	V/ns
Falling slew rate	Measured from 2.0V to 0.8V	1		2	V/ns
Duty cycle		45		55	%
Maximum output voltage		2.4			V
Minimum output voltage				0.4	V

Table 26: Electrical characteristic of the PLL

3.4 Clock Synthesizer/driver overview

The figure below shows the layout of the clock synthesizer/driver

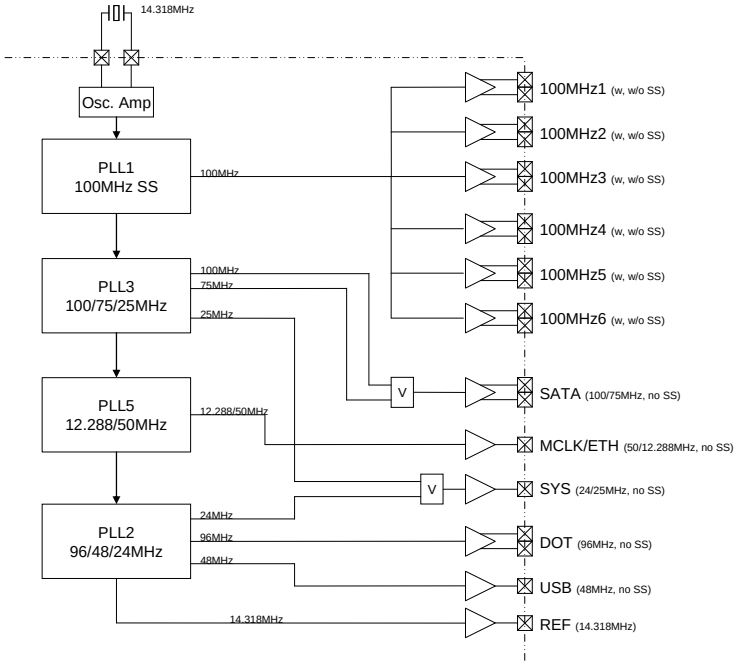


Figure 3 : Clock synthesizer/driver layout

3.5 Reference frequency REF 14.318MHz

A crystal with a frequency accuracy of ±100ppm is required to source the Atom™ E6xx processor platform with the appropriate frequencies at the requested accuracy.

Electrical Characteristics (Ta = -40 to +85 ºC)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Clock period		69.8203		69.8622	ns
Output high Voltage		2.4			V
Output low Voltage				0.4	V
Output high current			33		mA
Output low current		30		38	mA
Rising edge slew rata		1		4	V/ns
Falling edge slew rate		1		4	V/ns
Duty cycle		45		55	%
Jitter Cycle 2 Cycle				1000	ps

Table 27: Electrical characteristic REF clock

4 GENERALPURPOSE ADC

4.1 ADC overview

DA6011 provides a 10-bit GPADC combined with an analog input-multiplexer and track-and-hold circuitry. The analog input-multiplexer will allow conversion of 4 different inputs. The track and hold circuit ensures stable input voltages at the input of the ADC during the conversion.

The ADC is used to measure the following inputs either manually or automatically (or both):

- main supply voltage (VSUP): ADC_IN0 is internally configured to measure the supply voltage by subtracting the ADC reference voltage from the supply voltage before applying the signal to the ADC input
- junction temperature: ADC_IN1 is internally configured to measure the T_{junc} of DA6011.
- user channel A: ADC_IN2 is provided as a channel for measuring external values. For this channel an optional 15µA current source is provided
- user channel B: ADC_IN3 is provided as a channel for measuring external values.

Figure 4 shows the overall block of the GPADC including the registers containing the conversion results of the four channels.

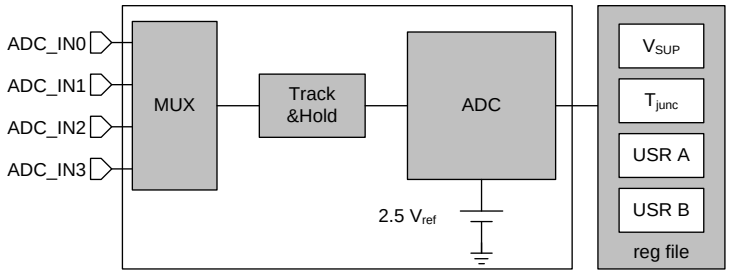


Figure 4: GPADC overall structure

GPADC Electrical Characteristics (Ta = -40 to +85 ºC)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Internal reference voltage	Derived from VLP		2.5		V
Off current				1	µA
ADC operating current	VREF=2.5V		100		µA
ADC resolution			10		Bit
ADC integral non linearity	VREF=2.5V		+/-2.0		LSB
ADC differential non linearity	VREF=2.5V		+/-0.8		LSB
ADC absolute accuracy	VREF=2.5V	12		15	mV
ADC conversion clock			1.0		MHz
Auto-zero time	For VSUP measurements		5		µs
Conversion time			29		µs
Total ADC conversion Time			34		µs
Rint internal MUX-resistance			5		kΩ
Maximum source impedance	Rsource (Note 1)		100		kΩ
Internal sampling capacitor.	Carray		10		pF

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Acquisition time	~7*τ=~7*(Rint+Rsource) *Cint	10	12	14	µs
Input Capacitance (Cint)	Total input capacitance		10		pF
ADC_IN0 voltage range VSUP (internal)	VSUP is measured by subtracting 2.5V	2.5		5.3	V
ADC_IN1 voltage range	Junction temperature of DA6011	0		2.5	V
ADC_IN2 voltage range Tsystem pin	Voltage across a NTC resistor, 15µA biasing	0		2.5	V
ADC_IN3 voltage range	High impedance input	0		2.5	V
MUX cross talk isolation			60		dB

Table 28: GPADC electrical characteristics

Note [1]. R_{source} is the impedance of the external source the ADC is sampling. The minimum acquisition time depends on this impedance.

In order to provide both automatic and manual conversion for all channels a total of 5 slots will be provided. Each slot has assigned a measurement period of 128us. The entire sequence will be repeated cyclically as shown in the following figure:

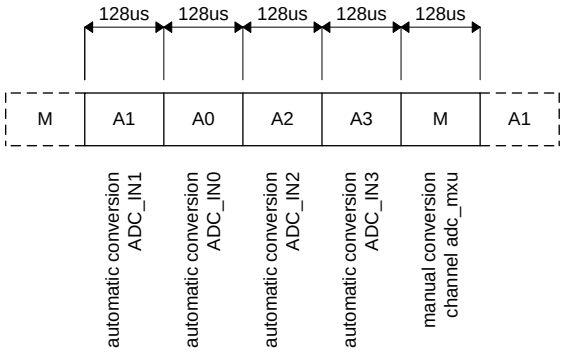


Figure 5: GPADC measurement slots

The automatic conversion of the junction temperature (slot A1) will always be performed, whereby the other conversions need to be enabled by setting the according enable bits in AUTOCTRL register 0xE1:

- AUTOCTRL.VSUPEN
- AUTOCTRL.AD2EN
- AUTOCTRL.AD3EN

4.2 Automatic measurements control

Each channel provides automatic measurements.

In automatic mode, only the 8 MSBs are stored to the corresponding conversion-result registers. For the automatic measurements it is possible to define threshold values which can be used to generate interrupts if the current conversion result is below or beyond this threshold. More details will be given in the next sections.

4.2.1 Automatic measurement of the supply voltage (ADC_IN0)

VSUP is measured and the conversion result compared with the value stored in an internal threshold register. If the conversation result is less than this threshold for 3 consecutive measurements, the bit VSUPUNDER is asserted in ADCSTAT status register 0xE4. In this case the automatic measurements of ADC_IN0 are paused until ADCSTAT.VSUPUNDER gets cleared by a write to register 0xE5 ADCIRQCLR.VSUPUNDER. If the interrupt is not masked, i.e. ADCIRQMASK.VSUPUNDER is not set, a hardware interrupt will be issued.

The 8-bit result of the ADC_IN0 automatic measurement is stored in register VSUPARES, with the following formula to calculate the the supply voltage:

Vsup = 5.5V- ((VSUPARES +3/65*(temp-25))*(5.5V–2.65V)/256) whereas temp is the actual junction temperature.

It is of interest to monitor the DA6011 supply voltage and issue an interrupt if the voltage is below this threshold as the bucks might not work properly on low input voltage

.

4.2.2 Automatic measurement of the junction temperature (ADC_IN1)

This channel measures the output of the on-chip temperature sensor with a gain of 3 and the conversion result is stored in register TJUNCARES. If the conversion result is greater than the value store in TJUNTH for 3 consecutive measurements the status bit TJUNCOVER of the ADCSTAT register 0xE4 is asserted. In this case the automatic measurements of ADC_IN1 are paused until the TJUNCOVER bit gets cleared by writing a 1 to TJUNCOVER of the ADCIRQCLR register 0xE5. If the interrupt is not masked, ADCIRQMASK.TJUNCOVER is not set, a hardware interrupt will be issued.

The register TJUNCOFFSET 0xEB will be used for one-point calibration of the temperature sensor. This register will be programmed individually during ATE testing for each single DA6011. This value can be read by the user in order to determine the junction temperature accurately based on the following formula:

Junc. Temp[°C] = (TJUNCARES –TJUNCOFFSET-0x4D)/0.6+25. The TJUNCOFFSET is the temperature correction value during ATE testing and is stored in the corresponding register. TJUNCARES is the 8bit conversion result.

4.2.3 Automatic measurement of user channels (ADC_IN2 and ADC_IN3)

The results of the ADC_IN2 and ADC_IN3 automatic conversion are stored in register ADCIN2ARES 0xEC and ADCIN3ARES 0xEF, respectively. For both channels the user can set low and high threshold values. If the conversion-result is less than the low-threshold or greater than the high-threshold the according status register is set and if the interrupt is not masked, IRQ_N gets asserted:

```
if (conv_result < ADCINxLTH) or (conv_result > ADCINxHTH) begin
       assert ADCSTAT.ADCINxTH
end
```

Note that it is up to the user to program the correct threshold settings.

As for the other automatic measurements, the automatic conversion is paused if the status bit is asserted. Only once the status bit is cleared the automatic conversion continues (if still enabled).

For each channel, the user has the possibility to enable a de-bouncing feature. If de-bouncing is enabled (register 0xE3 ADCIN23DB.IN2DB or ADCIN23DB.IN3DB set) 3 consecutive conversion results need to exceed the thresholds in order to set the status flag.

As above-mentioned, ADC_IN2 can be used with a 15uA current source that allows automatic measurements of a resistor value. This current source can be controlled via bit ADC2SRCEN of register AUTOCTRL 0xE1. During automatic measurements the enabled current source is dynamically switched-off at the end of the conversion and switched-on one slot prior to the next ADC_IN2 measurement, i.e. the source is switched on in the slot where ADC_IN1 measurements are performed. In order to not impact the measurement of ADC_IN1 the current source is getting enabled after ADC_IN1 measurement is done. If ADC_IN1 measurement is not enabled, the current source is enabled immediately.

4.3 Manual measurement control

Each channel can also undergo a manual conversion. As opposed to the automatic measurement mode, manual mode will store the entire 10-bit conversation result in the registers MANRESHB 0xE8 and MANRESLB 0xE7.

A manual conversion is initiated by setting the bit MANRUN of register MANCTRL 0xE2. In this case a manual measurement is done in slot 5 (see figure 5). The manual measurement channel can be selected via the CHSEL bits of such register. Once the manual conversion is finished, the status bit MANEOC of register ADCSTAT 0xE4 is set and the 10-bit result is stored in registers MANRESHB and MANRESLB. If the MANEOC bit of ADCIRQMASK register 0xE6 is not masked a hardware interrupt is generated. In order to start a new manual conversion the MANEOC bit of register 0xE5 ADCIRQCLR needs to be cleared first, followed by a new setting of the MANRUN bit of register MANCTRL 0xE2.

5 INTERNAL TEMPERATURE SUPERVISION

To protect DA6011 from damage due to excessive power dissipation, an internal temperature measurement will be executed every 1ms. Only after three consecutive temperature measurements indicate a thermal overload (T_{OVER}=130°C) a fault condition (OVERTEMP) will be generated.

If an OVERTEMP is detected, DA6011 will then shut down to shut down mode and record the fault by asserting TEMP_OVER in the FAULT_LOG register. The fault condition will remain as long as the internal temperature will be higher than T_{OVER} minus 10°C.

The internal temperature sensor can also be read out by the GPADC. An 8-bit OTP register is used to store its offset at a known temperature (e.g. 27°C). When subsequently read by software, this will improve the absolute accuracy, which should be ±7°C of the measured die junction temperature. This TJUNCOFFSET can be used by Atom™ E6xx processor to calculate the absolute die temperature, and can only be used in conjunction with the channel it was measured with.

To inform processor that DA6011 is getting hot, the PROTCHOT signal will be asserted. The trigger point is set to a die temperature of 110°C. After the assertion of PROCHOT E6xx processor shall start the temperature throttling. The minimum assertion time of PROCHOT is specified to be >500µs.

The absolute die junction temperature can be calculated by the host using the result from the ADC channel 1 measurement result (gain=3) and the TJUNCOFFSET trim values.

Junc. Temp[°C] = (TJUNCARES –TJUNCOFFSET-0x4D)/0.6+25°C. The TJUNCOFFSET is the temperature correction during ATE testing.

Electrical Characteristics (Ta = -40 to +85 ºC)

PARAMETER	MIN	TYP	MAX	UNIT
Thermal Shutdown	130	140	150	ºC
Hysteresis		10		ºC
PROCHOT		110		ºC
PROCHOT assertion time	500			µs

Table 29: Electrical characteristic internal temperature sensor

PROCHOT_B will be asserted at a junction temperature of 110°C to inform the CPU on Intel processor platform to start the temperature throttling.

6 Intel® Atom™ processor E6xx platform states

6.1 CPU C-state overview

The Atom™ E6xx processor provides support for C1, C2, C4 and C6 state. As added features, E6xx will also support three extended C-States and the ability to enable C4 in the presence of high bandwidth bus mastering devices using popup feature.

DA6011 primary controls the dynamic changing of E6xx processor C-States. The dynamic C-State control is handled internally by the processor.

6.2 System Sleep State Control (S-States)

The E6xx processor supports S3, S4 and S5 sleep states. S4 and S5 states are identical from hardware perspective.

The DA6011 provides the flows of the different states and the state transitions to the E6xx processor platform.

The E6xx processor platform returns to S0 state from S3/4/5 by wake –up events. These wake-up events can be initiated by:

- internal and external events to the E6xx processor, therefore E6xx requires the suspend well power domains on, when it is in S3 state
- DA6011 when the platform is in S4/5 state. Here external events can be detected while the RTC and an internal DA6011 supply are active.

6.2.1 S-State definitions

6.2.1.1 S0 State: Full on

This is the normal operating state of the Atom™E6xx processor. In S0 the core processor will transition in and out of the various processor C-States and P-States.

6.2.1.2 S3 State: Suspend to RAM (STR, Standby)

S3 is a suspend state where the core power planes of the E6xx processor are turned off and the suspend wells remain powered.

- All power wells are disabled, except for the suspend and RTC domains.
- The core processors macro-state is saved in memory
- Memory is held in self-refresh and the memory interface is disabled. Memories power domains are supplied from the VCC180SR voltage well. CKE is driven low.

6.2.1.3 S4 State: Suspend to disk (STD, Hibernate)

S4 is a suspend state where all power domains of the E6xx processor are turned off, except the RTC domain. In this ACPI state the system context is saved to the hard disk.

- No activity allowed
- All power domains are disabled, except the RTC domain
- A full system reset is required to resume from S4

6.2.1.4 S5 State: Soft off

From a hardware perspective the S5 state is identical to the S4 state. The difference is purely software, in that, the software does not write the system context to hard disk when entering S5.

7 DA6011 Operating modes

DA6011 supports the Intel® Atom™E6xx processor specific power states S4/5, S3, and S0. Furthermore there will be a system power down state. This power down state is needed for fault events such as a catastrophic shutdown or a failure event of DA6011 itself since in this case “always-on” supplies of the IOHs shall be disabled which is not the case in normal S4/5. With respect to E6xx processor the power down state SPD and the S4/5 state are the same. For the initial power up sequence, SPD is directly followed by the S4/5 state. During normal operation the lowest power state will always be S4/5 and all defined wake events do apply. After a failure of the system (monitored by either DA6011 directly or any other component communicating failure power-down events) DA6011 will remain in PD and only a power-push-button event (if the failure source has disappeared) can bring DA6011 back into S0 via a transition to S4/5 and S3. In case there is no power button available an external power cycling needs to be done.

7.1 Power-On-Reset generator

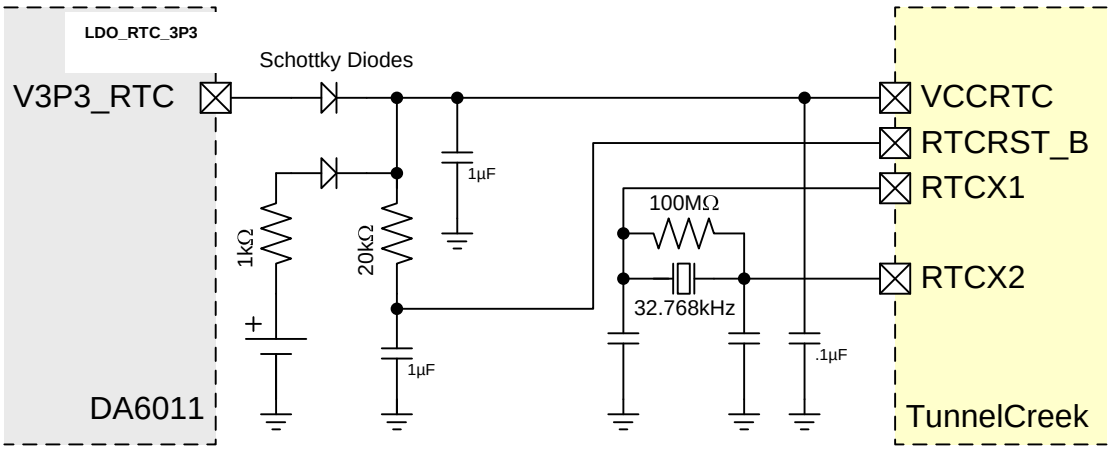
To guarantee the correct start-up of the DA6011, an analog power-on-reset APRST_B signal is generated internally for the first time the supply voltage is connected.
When the DA6011 supply voltage rises above the UVUT threshold voltage, the internal APRST_B is negated and DA6011 will start up the bandgap reference circuit and its internal oscillator in order to read the content of the OTP settings and further internal adjustments.
The internal APRST_B will be asserted if the power supply voltage falls below the UVLT threshold. De-assertion of APRST should startup the LDO_VLP.

PARAMETER	Parameter Name	MIN	TYP	MAX	UNIT
Under Voltage Lower Threshold	UVLT	3.6			V
Under Voltage Upper Threshold	UVUT		UVLT+ 0.5		V

7.2 RTC Domain

Generally there are two systems configurations: platforms with RTC battery (coin cell) available and platforms without RTC battery. The RTC domain consists of the RTC supply, the RTC clock and the reset signal RTCRST_B.

DA6011 will provide the RTC supply (LDO_RTC_3P3) only; the RTC clock (crystal) and the RTCRST_B signal need to be generated externally. As an example how the RTC domain can be implemented we refer to a solution suggested by Intel in [1].



[1] Intel ICH Family, Real Time Clock (RTC). Accuracy and Considerations under Test Conditions, October 2007. Application Note – AP-728

7.3 Power push-button

DA6011 will support an external power push-button for powering up/down the single components. The push button will include the following functionality:

- Short pulse detection (debounce time t_{db} >= 16ms)
- Long pulse detection (debounce time t_{db} > 4sec)
- Switching behavior (debounce time t_{db} >= 16ms; assertion triggers power up, de-assertion triggers power down)

Pulse detection is active low while switching behavior is active high.

7.3.1 Push button functionality

DA6011 can be ordered with push button functionality. In the case of a short pulse the action taken depends on the current state of DA6011 and the Atom™ processor.

- Long pulse (4sec) in S0, S3, or S4/5 will bring DA6011 into SPD without any handshaking.
- System in SPD: short pulse on PWRPBT_B will bring DA6011 into S0 state.
- System in S4/5: short pulse will bring DA6011 into S0
- System in S3: short pulse will bring DA6011 into S0
- System in S0: short pulse will generate IRQ_B event and provides status bit that can be accessed by software via SMBus. This interrupt bit will be cleared by DA6011 if leaving S0 state.

Providing the interrupt triggered by a short pulse event in S0, allows a software controlled action such as “standby”, “hibernate”, “shutdown”, or “do nothing”.

- If a long pulse gets detected by DA6011 then the entire system will be brought into SPD in the same way as it is done if THRMTRIP_B signal gets asserted by the E6xx processor.

7.3.2 Switching functionality

For the IVI hubs, the push-button functionality as described in Section 7.3.1 is not required. For these applications a switching behavior is requested. In this case, asserting PWRPBT_B will power-up the system. De-asserting PWRPBT_B will power down the system (if in S0, S3 or S4/5). If the system reaches SPD after a failure event toggling the power button is required in order to leave SPD.

If there is no power push button or power switch available, the input PWRPBT_B needs to be tied to a high level.

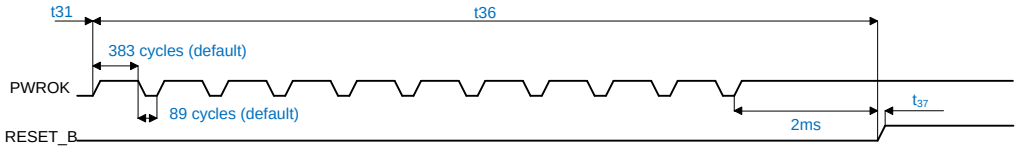
7.4 PWROK signal

For proper system power up feature Intel Atom processor E6xx series B0 silicon requests a dedicated PWROK signal cycling as described below. Intel's B1 silicon won't need such kind of procedure, according to Intel PWROK toggling will not disturb B1 silicon.
DA6011 includes the PWROK toggling feature as described below. On request DA6011 can be delivered with disabled PWROK toggling feature.

7.4.1 PWROK toggling

Based on Intel's description E6xx B0-silicon requests a PWROK toggling sequence of 10 pulses decreasing the start-up failure rate. DA6011 includes such kind of PWROK toggling feature with 15 pulse, furthermore decreasing the probability of the start-up issue:

15 pulses, where each pulse is
194.5µs high and
44.5µs



The PWROK toggling feature will always be performed when the system moves from S3 to S0, except for warm reset (both internal and external). Here the PWROK toggling feature is not executed.

7.4.2 PWROK blanking period

In case the PWROK toggling was not successful, Intel Atom E6xx will issue a cold reset in order to repeat the power up sequence. Once the system is in S0, a so-called "blanking period" will start. The duration of this blanking period is defined to be 1280ms. If during this phase the processor issues a cold reset, DA6011 will perform a cold reset without disabling the supplies and clocks. After the "special" cold reset has been completed and the system is in S0 the blanking period starts from scratch. If other handshaking commands are being received during the blanking period the blanking period stops and the received command is being executed.

Note that the blanking period will always be active if the system moves from S3 towards S0. Only during a warm reset (both internal and external) no blanking period will be initiated.

Theoretically it can occur that there is an endless loop of toggling and a reset in the blanking period. Such failure situation can be solved via a long pulse of PWRBTN_B, generating a catastrophic shut-down event and bringing down the system into SPD. Similar if the PWRBTN_B is configured as a power switch, here de-asserting PWRBTN_B will power down the system.

7.5 S-state corresponding power domains

The following tables give an overview about the active power domains during different S-states of the Intel platform.

7.5.1 E6xx processor & Platform Controller Hub EG20T

Voltage Regulator	Power domain	S0	S3	S4/5
LDO_RTC_V3P3	V3P3_RTC	X	X	X
LDO_LP	VLP	X	X	X
LDO_VINT	VINT	X	X	X
BUCK_1P2	V1P2_A	X	X	X
LDO_V2P5	V2P5_A	X	X	X
LDO_V3P3	V3P3_A	X	X	X
PD_V1P2	V1P2	X	X	
BUCK_V3P3	V3P3	X	X	
BUCK_V1P8	V1P8	X	X	
LDO_V0P9R	V0P9R	X	X	
LDO_V1P05	V1P05	X	X	
LDO_VUNI	V1P2_S	X		
PD_V3P3	V3P3_S	X		
LDO_V1P5	V1P5_S	X		
BUCK_V1P05	V1P05_S	X		
BUCK_GRAPHIC	VNN_S	X		
PD_V1P8	V1P8_S	X		
LDO_V0P9	V0P9_S	X		
LDO_V1P25	V1P25_S	X		
BUCK_CORE	VCC_S	X		

Table 30: Power domains in S-states for Intel Platform Controller Hub EG20T application

7.5.2 E6xx processor & ST ConneXt STA2X11 IO-Hub

Voltage Regulator	Power domain	S0	S3	S4/5
LDO_RTC_3P3	V3P3_RTC	X	X	X
LDO_VLP	VLP	X	X	X
LDO_VINT	VINT	X	X	
LDO_V3P3	V3P3	X	X	
BUCK_V1P8	V1P8	X	X	
LDO_V0P9R	V0P9R	X	X	
LDO_V1P05	V1P05	X	X	
BUCK_V3P3	V3P3_S	X		
LDO_V1P5	V1P5_S	X		
BUCK_V1P2	V1P2_S	X		
BUCK_V1P05	V1P05_S	X		
BUCK_GRAPHIC	VNN_S	X		
LDO_VUNI	V2P5_S	X		
PD_V1P8	V1P8_S	X		
LDO_V0P9	V0P9_S	X		
LDO_V1P25	V1P25_S	X		
BUCK_CORE	VCC_S	X		

Table 31: Power domains in S-states for ST ConneXt IO-Hub application

7.5.3 E6xx processor & OKI Semiconductor ML7213 IVI IO-Hub

Voltage Regulator	Power domain	S0	S3	S4/5
LDO_RTC_3P3	V3P3_RTC	X	X	X
LDO_LP	VLP	X	X	X
LDO_VINT	VINT	X	X	
LDO_V3P3	V3P3	X	X	
BUCK_V1P8	V1P8	X	X	
LDO_V0P9R	V0P9R	X	X	
LDO_V1P05	V1P05	X	X	
BUCK_V3P3	V3P3_S	X		
LDO_V1P5	V1P5_S	X		
BUCK_V1P2	V1P2_S	X		
BUCK_V1P05	V1P05_S	X		
BUCK_GRAPHIC	VNN_S	X		
PD_V1P8	V1P8_S	X		
LDO_V0P9	V0P9_S	X		
LDO_V1P25	V1P25_S	X		
BUCK_CORE	VCC_S	X		

Table 32: Power domains in S-states for OKI Semiconductor IVI IO-Hub application

7.5.4 E6xx processor & OKI Semiconductor ML7223 MP IO-Hub

Voltage Regulator	Power domain	S0	S3	S4/5
LDO_RTC_3P3	V3P3_RTC	X	X	X
LDO_LP	VLP	X	X	X
LDO_VINT	VINT	X	X	X
BUCK_V1P2	V1P2_A	X	X	X
LDO_V2P5	V2P5_A	X	X	X
LDO_V3P3	V3P3_A	X	X	X
PD_V1P2	V1P2	X	X	
BUCK_V3P3	V3P3	X	X	
BUCK_V1P8	V1P8	X	X	
LDO_V0P9R	V0P9R	X	X	
LDO_V1P05	V1P05	X	X	
LDO_VUNI	V1P2_S	X		
PD_V3P3	V3P3_S	X		
LDO_V1P5	V1P5_S	X		
BUCK_V1P05	V1P05_S	X		
BUCK_GRAPHIC	VNN_S	X		
PD_V1P8	V1P8_S	X		
LDO_V0P9	V0P9_S	X		
LDO_V1P25	V1P25_S	X		
BUCK_CORE	VCC_S	X		

Table 33: Power domains in S-states for OKI Semiconductor MP IO-Hub application

7.6 DA6011 power states

7.6.1 Atom™ E6xx processor & Intel Platform Controller Hub EG20T

7.6.1.1 Supplies

The following table lists the supplies for Platform Controller Hub EG20T. This sequence will be used for the S-state transitions from S4/5 to S3 to S0 and vice versa.

Supply Module	Voltage domain E6XX & EG20T	First active state	Sequence
LDO_RTC_3P3	V3P3_RTC	S4/5	0 (E6xx)
BUCK_V1P2	V1P2_A	S4/5	1 (EG20T)
LDO_V2P5	V2P5_A	S4/5	2 (EG20T)
LDO_V3P3	V3P3_A	S4/5	3 (EG20T)
PD_V1P2	V1P2	S3	4 (EG20T)
BUCK_V3P3	V3P3	S3	5 (E6xx & EG20T)
BUCK_V1P8	V1P8	S3	6 (E6xx & DDR2)
LDO_V0P9R	V0P9R	S3	7 (DDR2)
LDO_V1P05	V1P05	S3	8 (E6xx)
LDO_VUNI	V1P2_S	S0	9 (EG20T)
PD_V3P3	V3P3_S	S0	10 (E6xx & EG20T)
LDO_V1P5	V1P5_S	S0	11 (E6XX)
BUCK_V1P05	V1P05_S	S0	12 (E6XX)
BUCK_GRAPHIC	VNN_S	S0	13 (E6XX)
PD_V1P8	V1P8_S	S0	14 (E6XX)
LDO_V0P9	V0P9_S	S0	15 (DDR2)
LDO_V1P25	V1P25_S	S0	16 (E6XX)
BUCK_CORE	VCC_S	S0	17 (E6XX)

7.6.1.2 PLLs

The following clocks will be provided for the IO hub and E6xx processor. The group label corresponds to the signal name in the timing diagrams.

Source	Clock	First active state	Group
PLL3	SYS_25MHz	S4/5	IO_OBE_SYS
PLL2	USB_48MHz	S3	IO_OBE_USB
PLL3	SATA_CLK	S0	IO_OBE_S0
PLL1	PCIE_CLK	S0	IO_OBE_S0
PLL5	MCLK	S0	IO_OBE_S0
E6xx processor Input clocks		S0	IO_OBE_S0

7.6.1.3 Intel EG20T Platform Controller Hub SPD to S0 timing

Label	Description	Min	Max	Unit	Implementation
t_1	enabling of V3P3_RTC to enabling of V1P2_A	0	-	us	Variant dependent
t_2	enabling of V1P2_A to enabling of V2P5_A	0	-	us	2000
t_3	enabling of V2P5_A to enabling of V3P3_A	0	-	us	2000
t_{3a}	enable PLLs and enable output buffer IO_OBE_SYS			us	26500
t_4	S45 clocks stable to de-assertion of IO_RST_PLA_B	10	-	us	15
t_5	de-assertion of IO_RST_PLA_B to de-assertion of IO_SLP_PLB_B	200	-	us	250
t_6	de-assertion of IO_SLP_PLB_B to enabling of V1P2	0	-	us	250
t_7	enabling of V1P2 to enabling of V3P3	0	-	us	1000
t_8	enable PLLs and enable output buffer IO_OBE_USB		-	us	2500
t_9	S3 clocks stable to de-assertion of IO_RST_PLB_B	10	-	us	15
t_{10}	enabling of PLL output buffer to enabling V0P9R and V1P8	0	-	us	1000
t_{11}	enabling of V0P9R and V1P8 to enabling of V1P05	0	-	us	2000
t_{12}	enabling of V1P05 to de-assertion of RSMRST_B	5000	-	us	6000
t_{13}	de-assertion of RSMRST_B to assertion of IO_SLP_PLC_B	0	-	us	100
t_{14}	de-assertion of IO_SLP_PLC_B to enabling of V1P2_S	0	-	us	50
t_{14a}	enabling of V1P2_S to enabling of V3P3_S	0	-	us	1000
t_{15}	enabling of V3P3_S to enable PLLs and IO_OBE_S0	0	-	us	8000
t_{16}	enabling of V3P3_S to assertion of IO_PWROK	20	-	us	2000
t_{18}	enabling of V3P3_S to enabling of V1P5_S	0	-	us	1000
t_{19}	enabling of V1P5_S to enabling of V1P05_S	0	-	us	1000
t_{20}	enabling of V1P05_S to enabling of VNN_S	0	-	us	500
t_{21}	enabling of VNN_S to enabling of V1P8_S	0	-	us	2000
t_{22}	enabling o f V1P8_S to de-activating V0P9_S(STR)	0	-	us	1000
t_{22a}	de-activating V0P9_S(STR) to enabling of V0P9_S	0	-	us	500
t_{24}	enabling of V0P9_S to enabling of V1P25_S	0	-	us	1000
t_{25}	enabling of V1P25_S to enabling of VCC_S	0	-	us	2500
t_{26}	VCC_S stable to PWRMODE=M2	25	-	us	2000
t_{27}	time in M2	10	20	us	15
t_{28}	timing determined by TC				
t_{29}	VID/VIDen out to new VNN stable delay	45	100	us	100
t_{30}	Required time in M3 (t31+t36+t34)	2500	-	us	6000
t_{31}	Entry to M3 assertion of PWROK			us	500
t_{34}	de-assertion of IO_RST_PLC_B to de-assertion of RESET_B	0	1	us	0.5
t_{36}	PWROK toggling to de-assertion of IO_RSTPLC_B (and 0.5us later RESETB)	250		us	5500
t_{37}	de-assertion of RESET_B to PWRMODE change to M1	5		us	10
t_{42}	time in M1 (includes ramping VCC_S to new target voltage after VIDEN = VCC)			us	200

Table 34: Delays for EG20T Platform Controller Hub

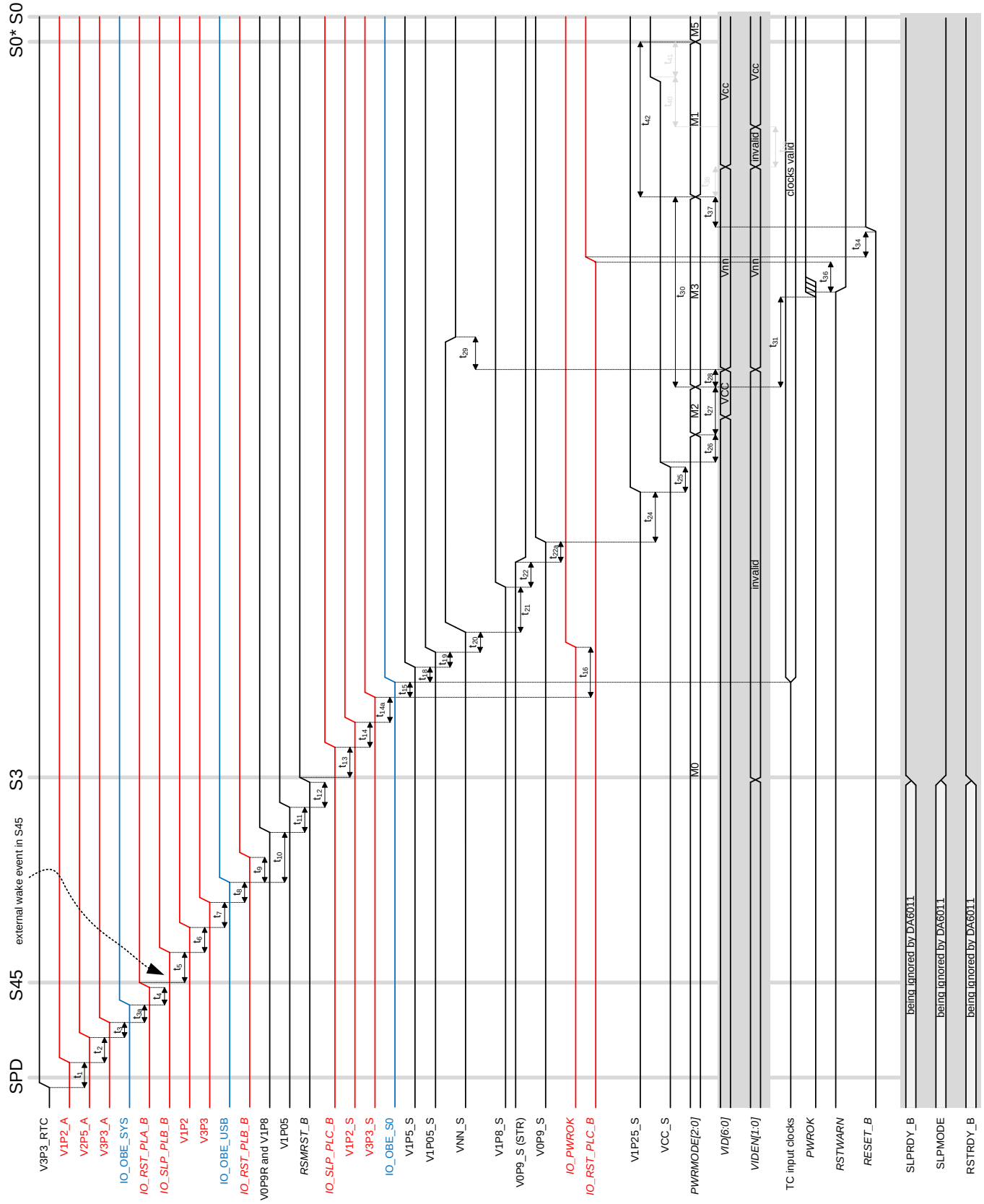


Figure 6 : SPD to S0 timing EG20T Platform Controller Hub

7.6.1.4 Intel EG20T Platform Controller Hub timing for S0 to SPD

Label	Description	Min	Max	Unit	Implementation
t_0	Intel TC timing – not relevant for DA6011				---
t_1	SLPRDY_B assertion to assertion of RSTWARN	0		us	10
t_2	Intel TC timing – not relevant for DA6011				---
t_3	RSTRDY_B assertion to assertion of RESET_B and IO_RST_PLC_B (directly 0.5us after assertion of RESET_B)	0		us	10
t_4	RESET_B assertion to PWROK de-assertion	0		us	20
t_5	RESET_B assertion to M5->M1 transition	0		us	10
t_6	PWROK de-assertion to M1->M0 transition	0		us	10
t_7	PWROK de-assertion to disabling of VCC_S	0		us	20
t_8	disabling of VCC_S to disabling of V1P25_S			us	3000
t_9	disabling of V1P25_S to disabling of V0P9_S			us	1000
t_{10}	disabling of V0P9_S to enabling of V0P9_S (STR)			us	1000
t_{11}	enabling of V0P9_S (STR) to disabling of V1P8_S			us	2000
t_{12}	disabling of V1P8_S to disabling of VNN_S			us	1000
t_{13}	disabling of VNN_S to disabling of V1P05_S			us	1000
t_{13_a}	disabling of V1P05_S to disabling of V1P5_S	0	-	us	1000
t_{13_b}	disabling of VCC_S to disabling of S0 clocks	0	-	us	1000
t_{15}	disabling of V1P05_S to de-assertion of IO_PWROK	0	-	us	1000
t_{16}	Tpwd1; IO_PWROK de-assertion to IO_SLP_PLC_B assertion	0	-	us	10
t_{17}	Disabling of V1P05_S to disabling of V3P3_S	-	-	us	1000
t_{18}	Tpwd3_2; disabling of V3P3_S to disabling of V1P2_S	0	-	us	1000
t_{19}	disabling of V1P2_S to assertion of RSMRST_B (in case of direct transition) plus delay	0	-	us	1000
t_{20}	RSMRST_B assertion to disabling of V1P05	0	-	us	10
t_{21}	disabling V1P05 to disabling of V0P9R and V1P8	0	-	us	1000
t_{22_a}	disabling of V0P9R and V1P8 to disabling of S3 clocks	0	-	us	1000
t_{22}	disabling of V0P9R and V1P8 to assertion of IO_RST_PLB_B	0	-	us	10
t_{23}	Tpwd4; assertion of IO_RST_PLB_B to assertion of IO_SLP_PLB_B	0	-	us	10
t_{24}	S3 clocks disabled to disabling of V3P3	0	-	us	2000
t_{25}	Tpwd4_2; disabling of V3P3 to disabling of V1P2	0	-	us	1000
t_{26}	disabling of V1P2 to assertion of IO_RST_PLA_B (in case of direct transition) plus delay	0	-	us	1010
t_{27}	assertion of IO_RST_PLA_B to disabling of S45 clocks	0	-	us	1000
t_{28}	S45 clocks disabled to disabling of V3P3_A	0	-	us	15000
t_{29}	disabling of V3P3_A to disabling of V2P5_A	0	-	us	1000
t_{30}	disabling o f V2P5_A to disabling of V1P2_A	0	-	us	1000

Table 35: Delays for EG20T Platform Controller Hub for S0 to S4/5 transition

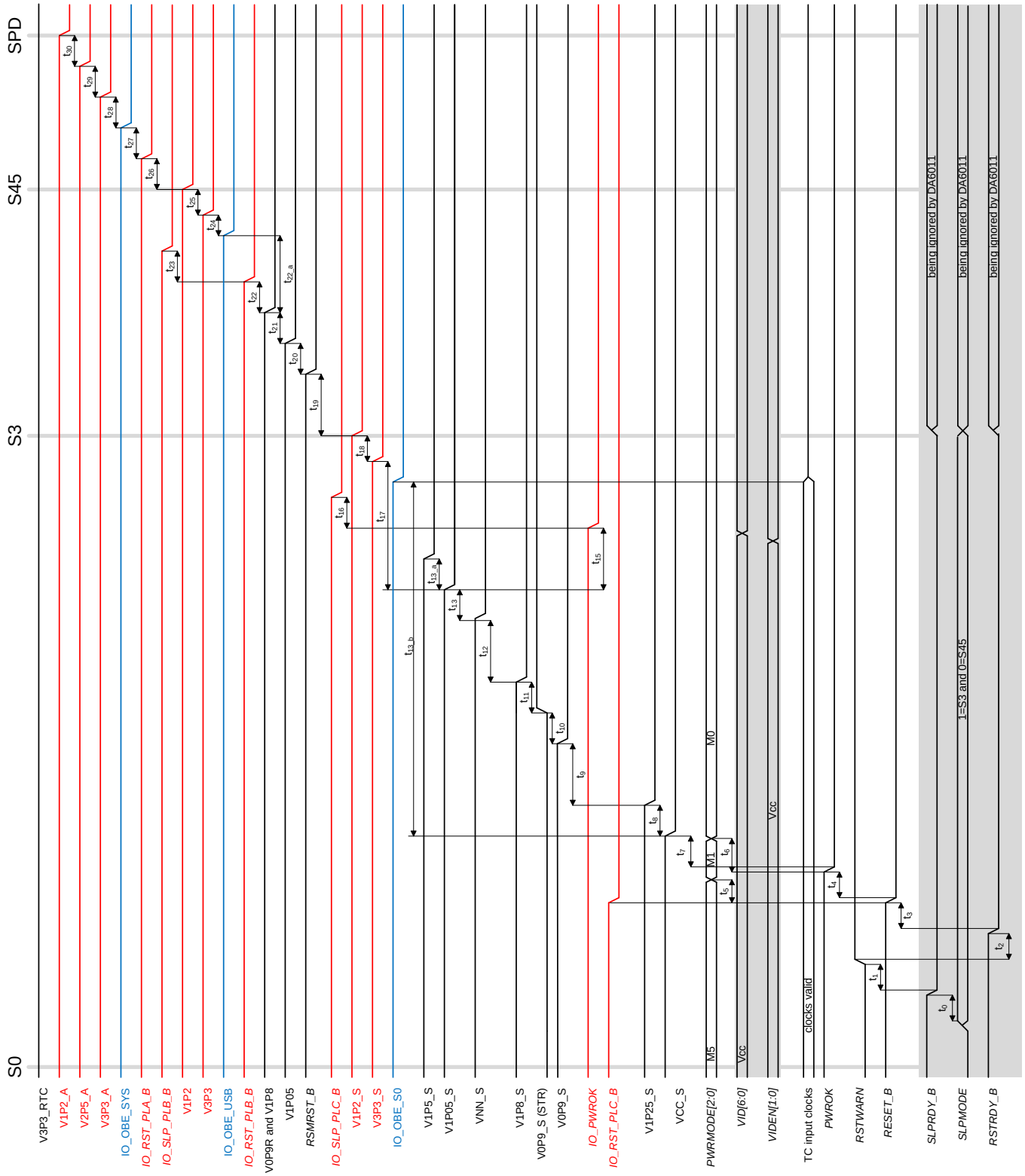


Figure 7 : S0 to SPD timing EG20T Platform Controller Hub

7.6.1.5 Intel EG20T Platform Controller Hub timing for S3 to S0 Sequence

From the sequence described in chapter 7.6.4.4 the S3 to S0 sequence can be derived by including the handshaking signals of Atom™ processor. The timings will be the same as provided for the S4/5 to S0 sequence. The S3 to S0 sequence is given in the following figures, whereas the wake-up event can be a software or an external event if WAKE_B gets asserted. Note that the external wake event will wake-up the system if it is in S3 or in S4/5 state.

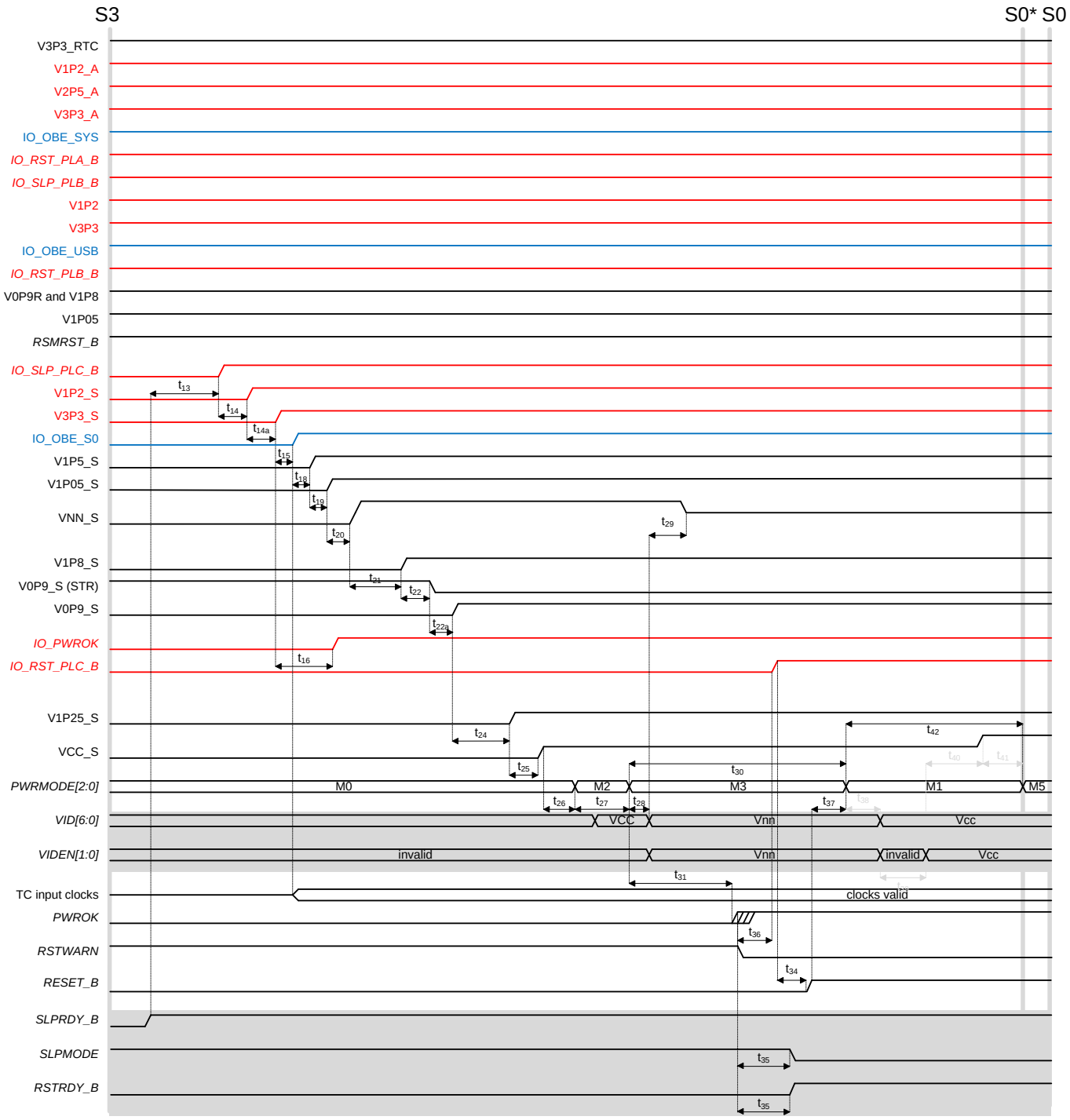


Figure 8 : S3 to S0 timing EG20T Platform Controller Hub Software event

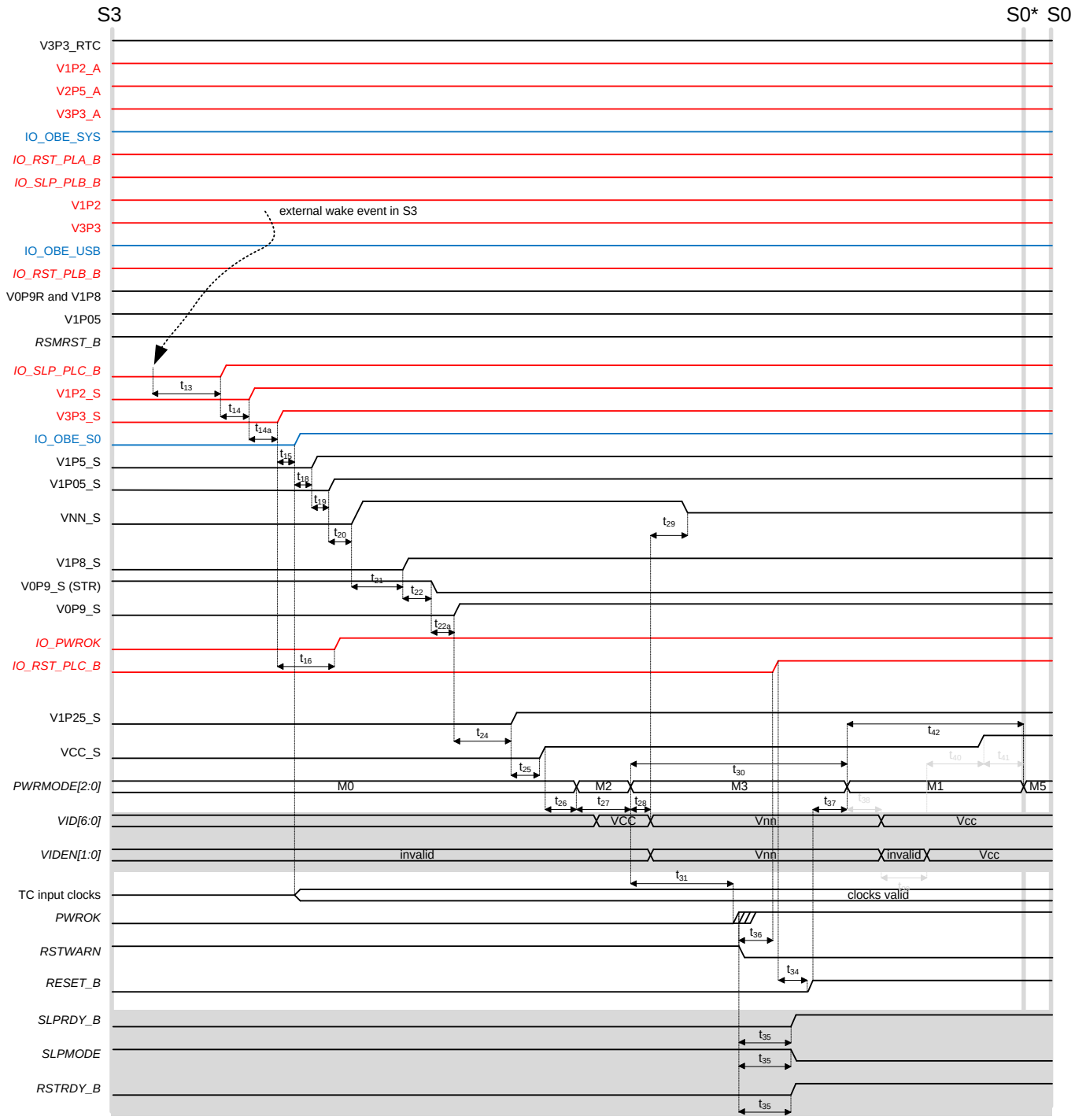


Figure 9 : S3 to S0 timing EG20T Platform Controller Hub external wake event

7.6.1.6 Cold Reset Intel EG20T Platform Controller Hub

During a cold reset Atom™ E6xx processor and the IOH will undergo a power cycling. The timings for the S0 to S4/5 sequence are basically the same as for the sequence described in chapter 7.6.1.4. Once in S4/5 the cold reset period will be 4 seconds before the S4/5 to S0 sequence starts in the same way as defined in chapter 7.6.4.3

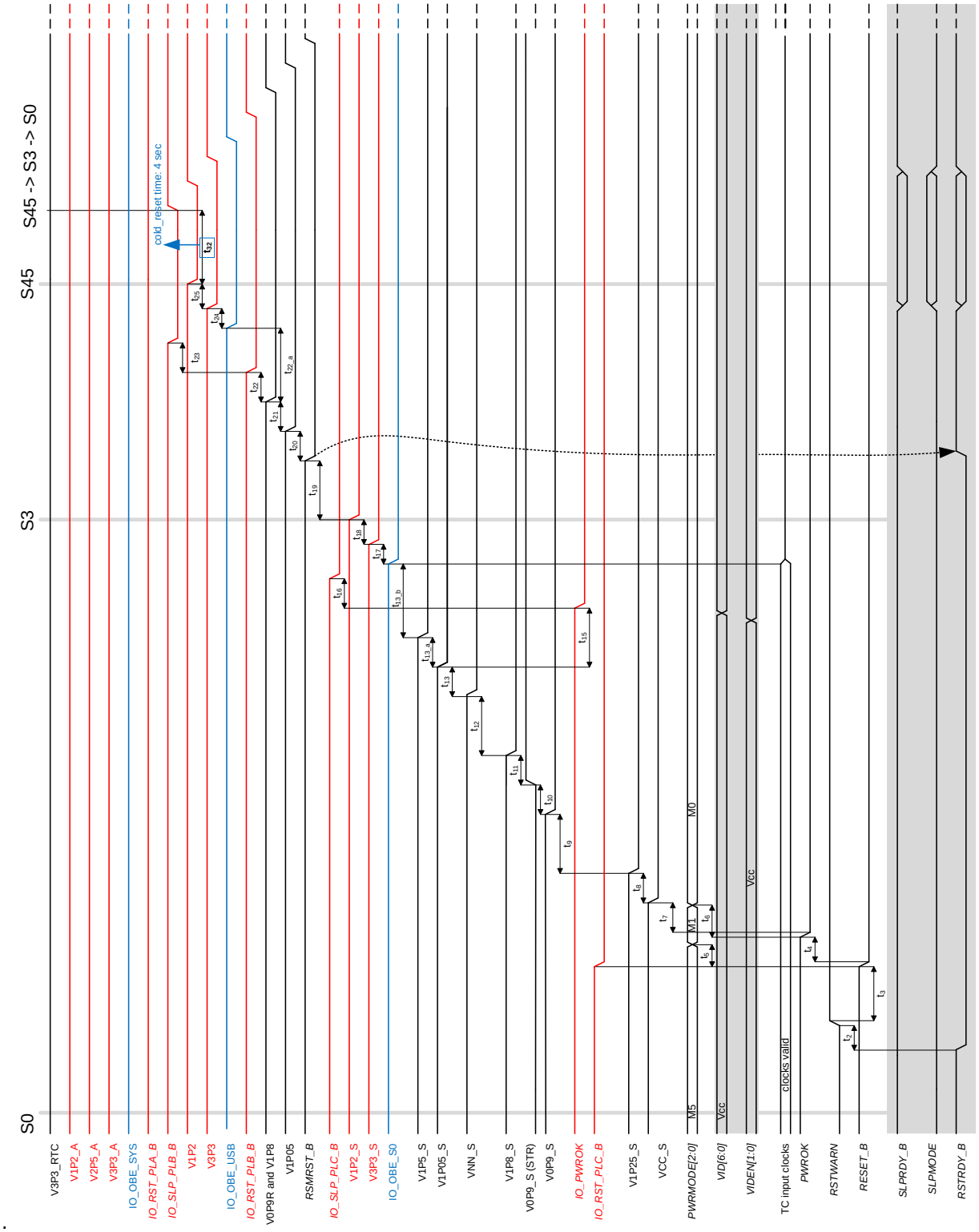


Figure 10 : Cold reset EG20T Platform Controller Hub

7.6.1.7 Warm Reset Intel EG20T Platform Controller Hub (internal & external)

During a warm reset issued by E6xx processor the reset signals of the Platform Controller Hub also get asserted for resetting the internal IO-Hub logic. The following diagram shows the warm reset sequence for EG20T Platform Controller Hub and E6xx processor. The external warm reset is triggered by the assertion of RESET_IN_B instead of the processor handshake signals. In case of the RESET_IN_B assertion DA6011 will assert RSTWARN and after the assertion of RSTRDY_B it continues in the same way as an internal warm reset.

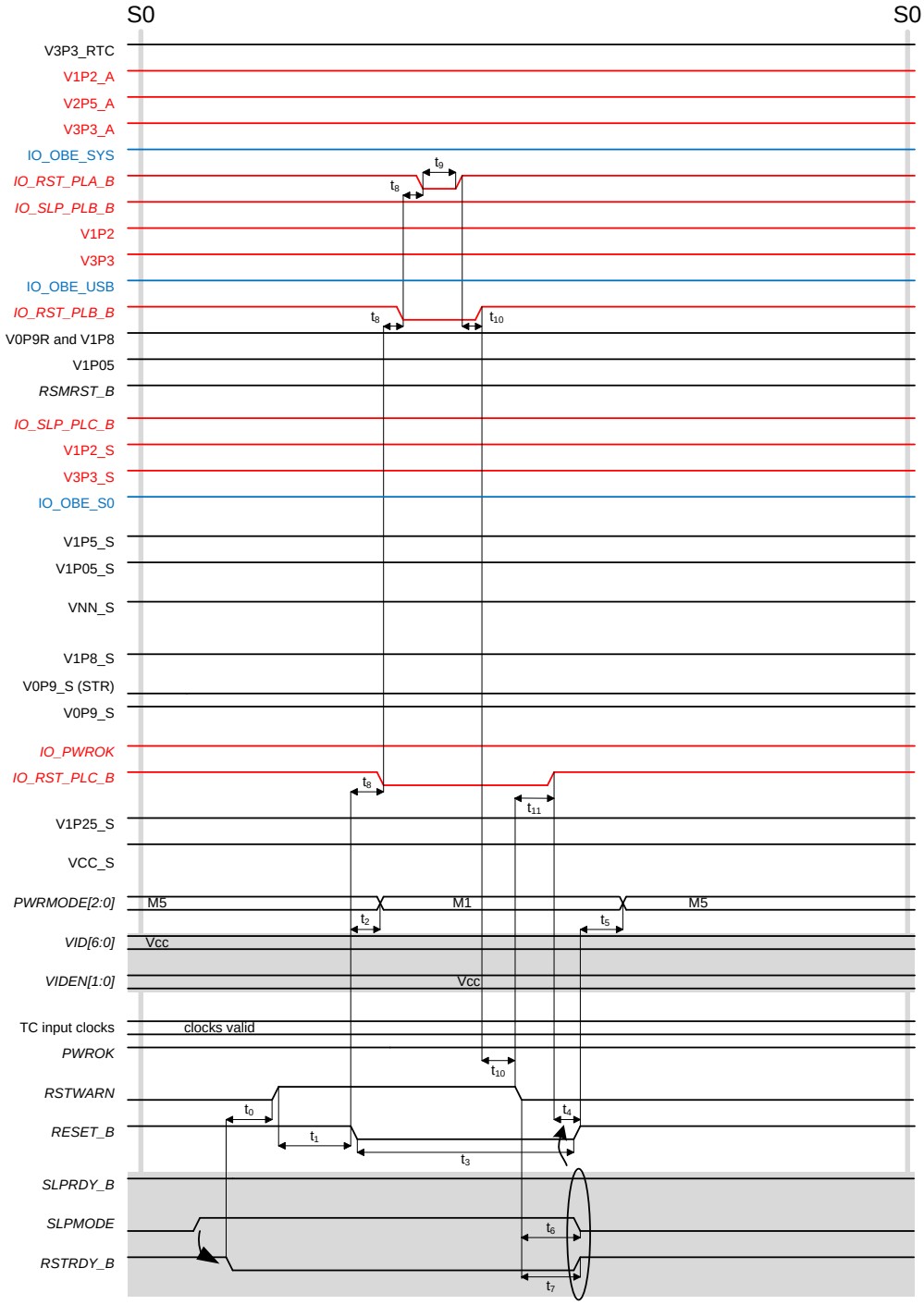


Figure 11 : Warm Reset EG20T Platform Controller Hub internal

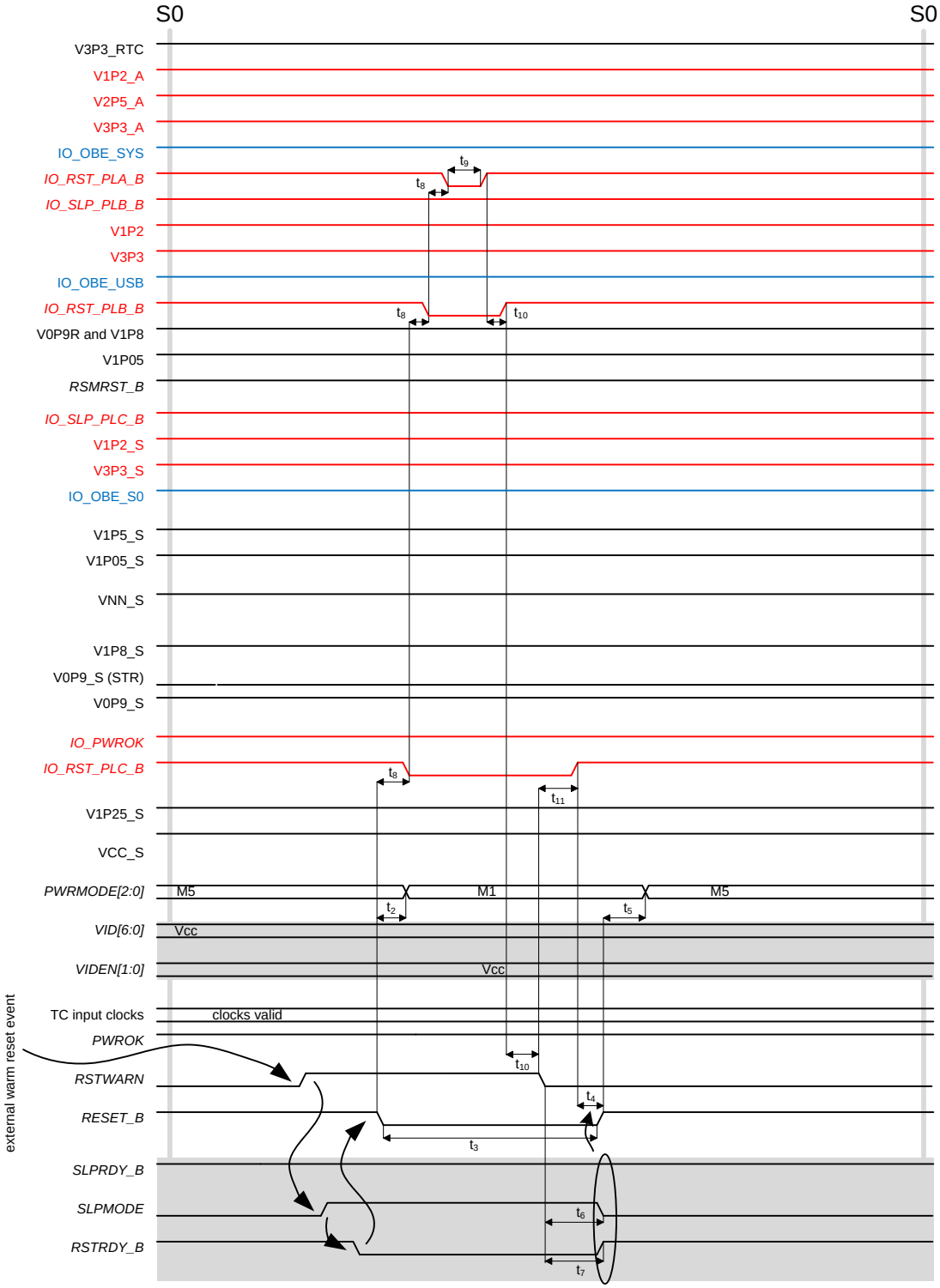


Figure 12 : Warm Reset EG20T Platform Controller Hub external

The delays for the warm reset sequence are given in chapter 7.6.4.7. Note: Intel to provide validated numbers. Therefore, the given timings of the IOH are subject to change. In any case, the reset assertion de-assertion of the EG20T Platform Controller Hub will always be done prior to the release of the RESET_B of E6xx processor.

Label	Description	Min	Max	Unit	Implementation
t_0	RSTRDY_B assertion to RSTWARN assertion	0	>0	us	1
t_1	RSTWARN assertion to RESET_B assertion	-	>0	us	10
t_2	RESET_B assertion to M1 entry	0	-	us	0
t_3	RESET_B assertion period	1000	-	us	1654
t_4	de-assertion of IO_RST_PLC_B to de-assertion of RESET_B			us	0.5
t_5	RESET_B de-assertion to M5 entry	50	-	us	100
t_6	RSTWARN de-assertion to SLPMODE de-assertion	-	100	us	---
t_7	RSTWARN de-assertion to RSTRDY_B de-assertion	-	100	us	---
t_8	RESET_B assertion to IO_RST_PLC_B assertion IO_RST_PLC_B assertion to IO_RST_PLB_B assertion IO_RST_PLB_B assertion to IO_RST_PLA_B assertion			us	100
t_9	IO_RST_PLA_B assertion period			us	1000
t_{10}	IO_RST_PLA_B de-assertion to IO_RST_PLB_B de-assertion IO_RST_PLB_B de-assertion to RSTWARN de-assertion			us	100
t_{11}	de-assertion of RSTWARN to de-assertion of IO_RST_PLC_B. Since t4 is only 0.5 us t11 is set in such a way that the minimum Intel timing of 150us in between the assertion of RSTWARN and the de-assertion of RESET_B is fulfilled.			us	150

Table 36: Warm reset delays

7.6.1.8 Catastrophic Shutdown Intel EG20T Platform Controller Hub

A catastrophic shutdown can be issued by Atom™E6xx processor at any time, asynchronously to all other events occurring on the system. In this case all supplies except the RTC supply (V3P3_RTC) will be disabled. All timings will be set to their minimum value. Note that currently Intel did not specify the timings for the catastrophic shutdown completely.

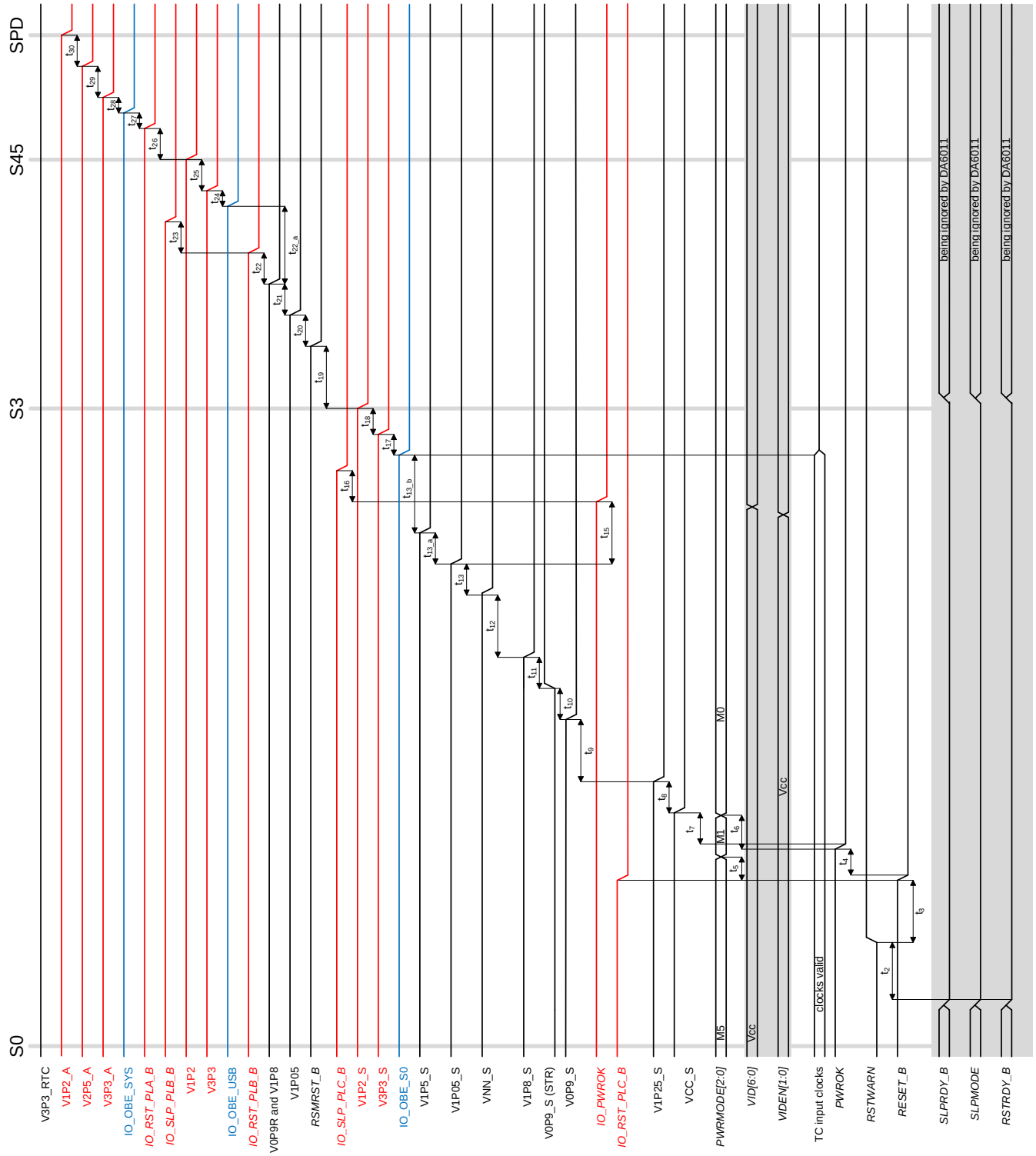


Figure 13 : Catastrophic shut down EG20T Platform Controller Hub

7.6.2 Atom™ E6xx processor & ST ConneXt STA2X11 IO-Hub

DA6011 IO_RST_PLC_B is the connection to STA2X11 RESETn signal!

7.6.2.1 Power Supplies

Supply Module	Voltage domain TC & ST IO-Hub	First active state	Sequence
LDO_RTC_3P3	V3P3_RTC	S4/5	0 (E6XX)
LDO_V3P3	V3P3	S3	1 (E6XX)
BUCK_V1P8	V1P8	S3	2 (E6XX & DDR2)
LDO_V0P9R	V0P9R	S3	3 (DDR2)
LDO_V1P05	V1P05	S3	4 (E6XX)
BUCK_V3P3	V3P3_S	S0	5 (E6XX & ST)
LDO_V1P5	V1P5_S	S0	6 (E6XX)
BUCK_V1P05	V1P05_S	S0	7 (E6XX)
BUCK_GRAPHIC	VNN_S	S0	8 (E6XX)
LDO_VUNI	V2P5_S	S0	9 (ST)
PD_V1P8	V1P8_S	S0	10 (E6XX & ST)
BUCK_V1P2	V1P2_S	S0	11 (ST)
LDO_V0P9	V0P9_S	S0	12 (DDR2)
LDO_V1P25	V1P25_S	S0	13 (E6XX)
BUCK_CORE	VCC_S	S0	14 (E6XX)

7.6.2.2 PLLs

The following clocks will be provided for the IO-Hub and E6xx processor. The group label corresponds to the signal name in the timing diagrams.

Source	Clock	First active state	Group
PLL2	SYS_24MHz	S0	IO_OBE_S0
PLL5	ETH_50MHz	S0	IO_OBE_S0
PLL3	SATA_CLK	S0	IO_OBE_S0
PLL1	PCIE_CLK	S0	IO_OBE_S0
E6xx processor Input clocks		S0	IO_OBE_S0

7.6.2.3 ST ConneXt IO-Hub timing for SPD to S0

Label	Description	Min	Max	Unit	Implementation
t_6	enabling of V3P3_RTC to enabling of V3P3	0		us	Variant dependent
t_{10}	enabling of V3P3 to enabling of V0P9R and V1P8	0			18000
t_{11}	enabling of V0P9R and V1P8 to enabling of V1P05	0		us	2000
t_{12}	enabling of V1P05 to de-assertion of RSMRST_B	5000		us	6000
t_{13}	de-assertion of RSMRST_B to enabling of V3P3_S			us	2
t_{15}	enabling of V3P3_S stable to S0 clocks stable			us	14500
t_{16}	enabling V3P3_S to enabling of V1P5_S	0		us	3500
t_{19}	enabling of V1P5_S to enabling of V1P05_S	0		us	1000
t_{20}	enabling of V1P05_S to enabling of VNN_S	0		us	500
t_{21}	enabling of VNN_S to enabling of V2P5_S	0		us	2000
$t_{21\ a}$	enabling of V2P5_s to enabling of V1P8_S	0		us	1000

Label	Description	Min	Max	Unit	Implementation
t_{22}	enabling of V1P8_S to enabling of V1P2_S	0		us	1000
t_{22a}	enabling of V1P2_S to disabling V0P9R (STR)	0		us	2000
t_{23}	disabling of V0P9R (STR) to enabling of V0P9_S	0		us	500
t_{24}	enabling of V0P9_S to enabling of V1P25_S	0		us	1000
t_{25}	enabling of V1P25_S to enabling of VCC_S	0		us	2500
t_{26}	VCC_S stable to PWRMODE=M2	25	-	us	2050
t_{27}	time in M2	10	20	us	15
t_{28}	timing determined by TC				---
t_{29}	VID/VIDen out to new VNN stable delay	45	100	us	100
t_{30}	Required time in M3(t31+t36+t34)	2500	-	us	4860.5
t_{31}	Entry to M3 assertion of PWROK			us	500
t_{34}	de-assertion of RESETn to de-assertion of RESET_B (min, timing, max until IO_PWROK_EN=1)	0		us	0.5
t_{36}	PWROK toggling to de-assertion of RESETn (and 0.5us later RESET_B if IO_PWROKEN=1)	250		us	4361
t_{37}	de-assertion of RESET_B to PWRMODE change to M1	5		us	10
t_{42}	time in M1 (includes ramping VCC_S to new target voltage after VIDEN = VCC)			us	200

Table 37: E6XX & ST IO-Hub SPD to S0 timing

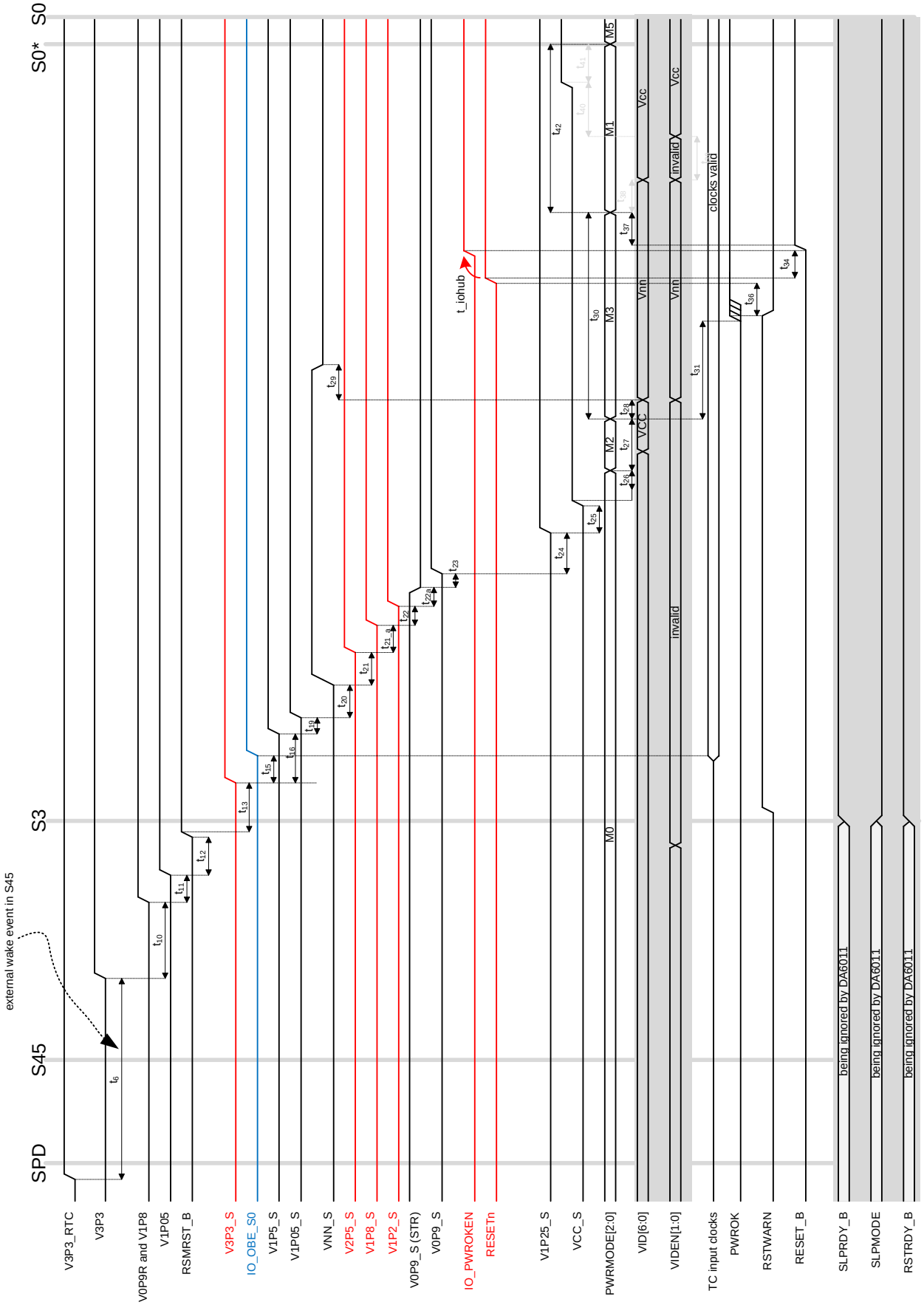


Figure 14 : E6xx & ST IO-Hub SPD to S0 timing

7.6.2.4 ST ConneXt IO-Hub timing for S0 to SPD

Label	Description	Min	Max	Unit	Implementation
t_0	Intel E6xx timing – not relevant for DA6011				---
t_1	SLPRDY_B assertion to assertion of RSTWARN	0		us	10
t_2	Intel TC timing – not relevant for DA6011				---
t_3	RSTRDY_B assertion to assertion of RESET_B and RESETn (directly 0.5us after assertion of RESET_B)	0		us	10
t_4	RESET_B assertion to PWROK de-assertion	0		us	20
t_5	RESET_B assertion to M5->M1 transition	0		us	10
t_6	PWROK de-assertion to M1->M0 transition	0		us	10
t_7	PWROK de-assertion to disabling of VCC_S	0		us	20
t_8	disabling of VCC_S to disabling of V1P25_S			us	3000
t_{10}	disabling of V1P25_S to disabling of V0P9_S	0		us	1000
t_{12}	disabling of V0P9_S to enabling of V0P9_S (STR)	0		us	1000
t_{13}	enabling of V0P9_S (STR) to disabling of V1P2_S	0		us	2000
t_{14}	disabling of V1P2_S to disabling of V1P8_S	0		us	1000
t_{15}	disabling of V1P8_S to disabling V2P5_S	0		us	1000
t_{16}	disabling of V2P5_S to disabling of VNN_S	0		us	1000
t_{17}	disabling of VNN_S to disabling of V1P05_S	0		us	1000
t_{17a}	disabling of V1P05_S to disabling of V1P5_S	0		us	1000
t_{18}	disabling of VCC_S to disabling of S0 clocks	0		us	1000
t_{18a}	disabling of V1P5_S to disabling of V3P3_S	0		us	3000
t_{19}	disabling of V3P3_S to assertion of RSMRST_B (in case of direct transition) plus delay	0	-	us	1010
t_{20}	assertion of RSMRST_B to disabling of V1P05	0		us	10
t_{21}	disabling of V1P05 to disabling of V0P9R and V1P8	0		us	1000
t_{22}	disabling of V0P9R and V1P8 to disabling of V3P3	0		us	9000
t_{25}, t_{26}, t_{27}	determined by Atom E6xx				

Table 38: S0 to SPD timings for ST IOH

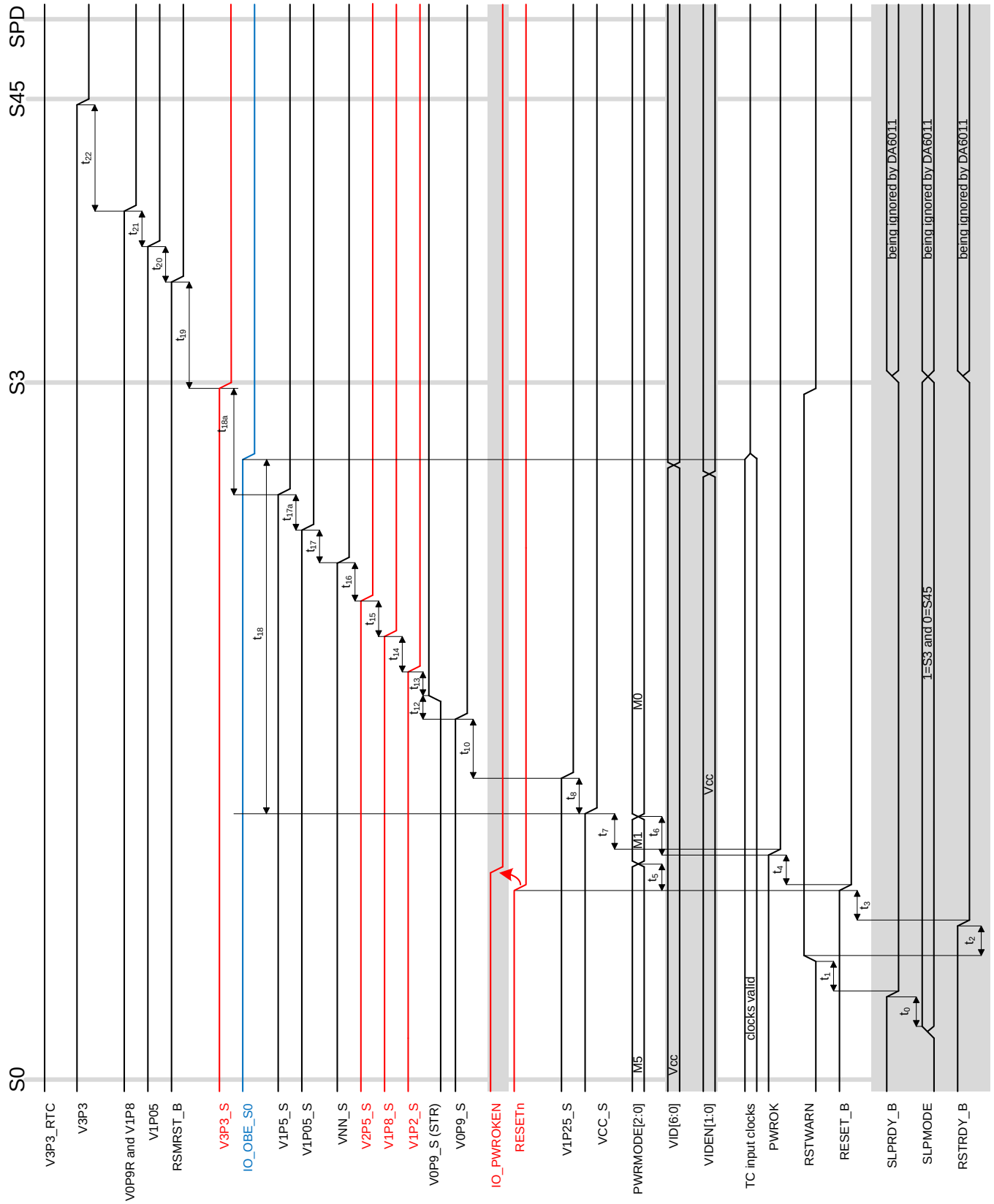


Figure 15 : S0 to SPD timings for ST IOH

7.6.2.5 ST ConneXt IO-Hub timing for S3 to S0 (internal & external)

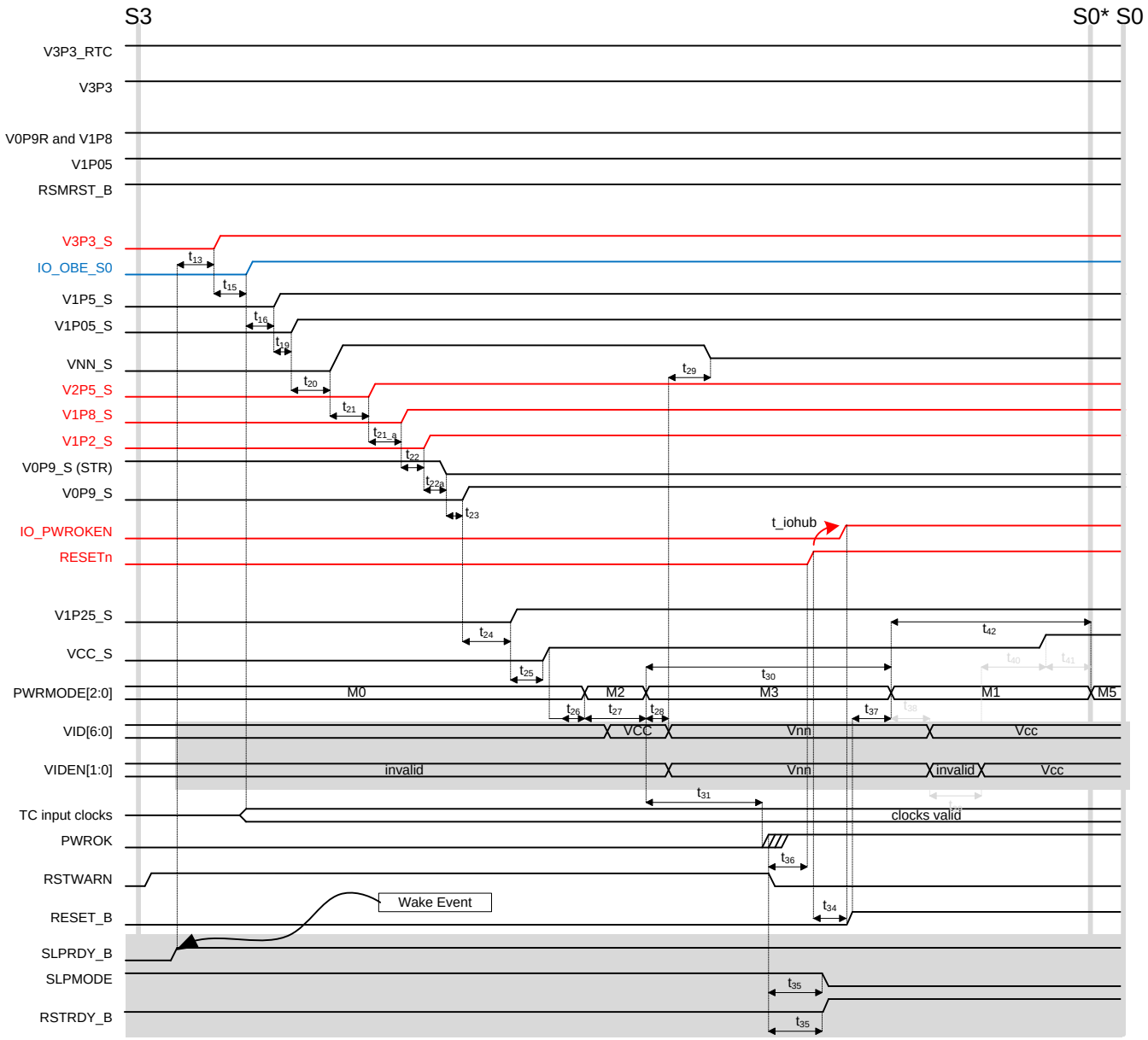


Figure 16 : S3 to S0 delays for ST IOH internal event

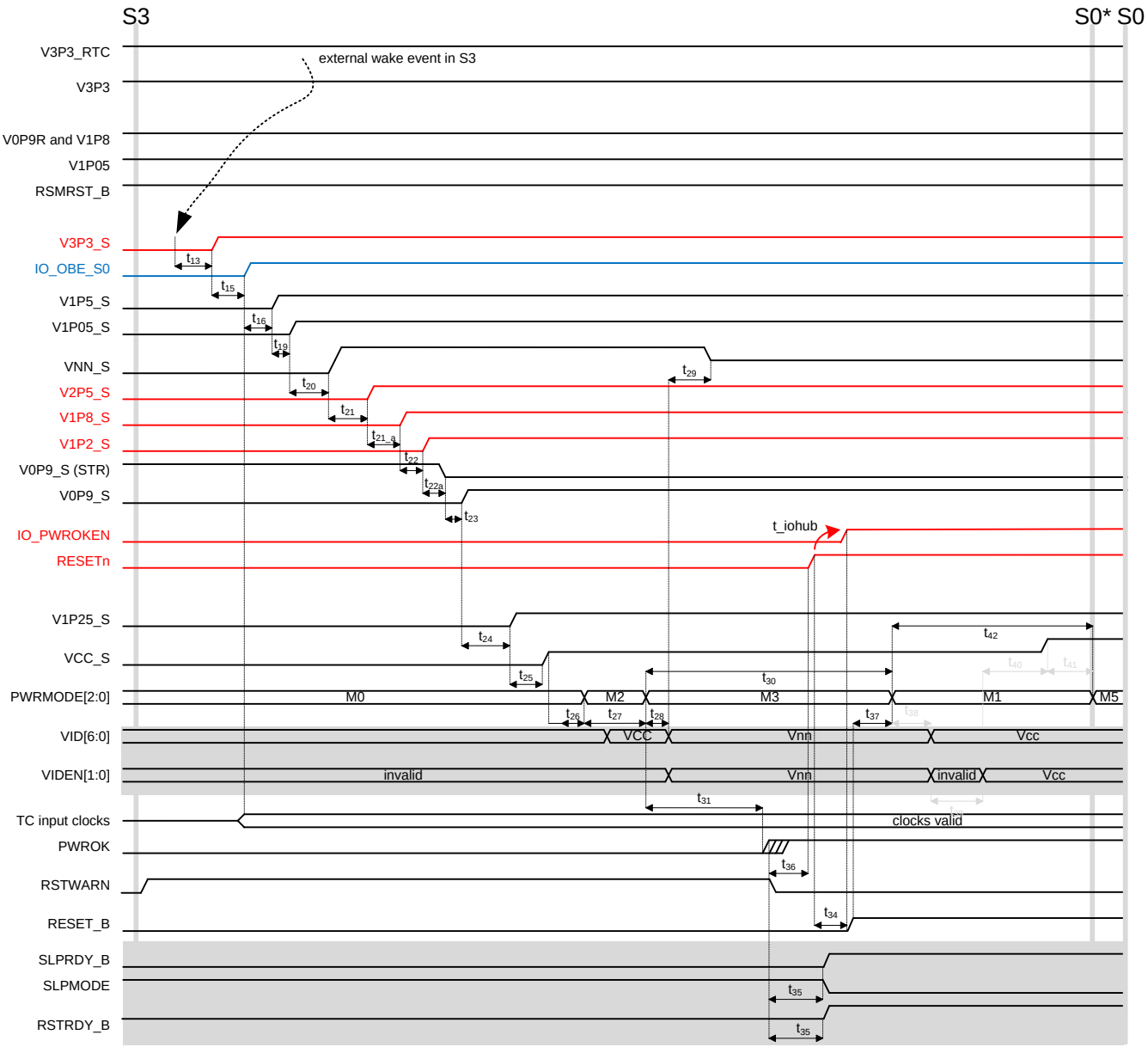


Figure 17 : S3 to S0 delays for ST IOH external event

7.6.2.6 Cold Reset ST IO hub

During a cold reset E6xx processor and the IO hub will undergo a power cycling. The timings for the S0 to S4/5 sequence are basically the same as for the sequence described in Section 7.6.2.4. Once in S4/5 the cold reset period will be 4 seconds. After this delay the S4/5 to S0 sequence starts in the same way as defined in Section 7.6.2.3.

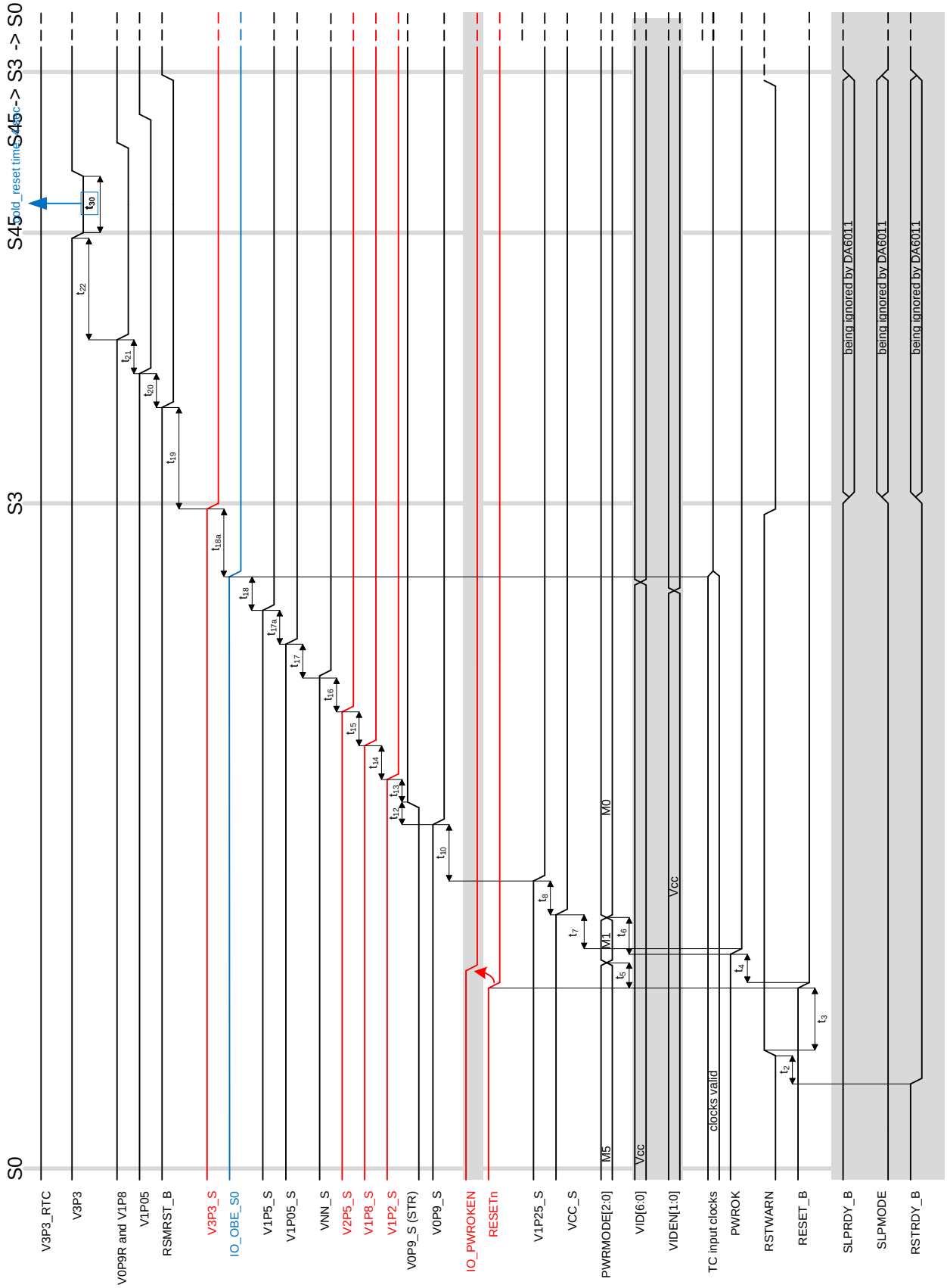


Figure 18 : Cold reset ST IOH

7.6.2.7 Warm Reset ST IOH (internal & external)

During a warm reset issued by Atom™E6xx processor the reset signal of the ST IOH also gets asserted for resetting the internal IOH logic. The following diagram shows the warm reset sequence for both ST IOH and E6xx processor. The supplies and PLLs remain fully enable. The external warm reset is triggered by the assertion of RESET_IN_B instead of the processor handshake signals.

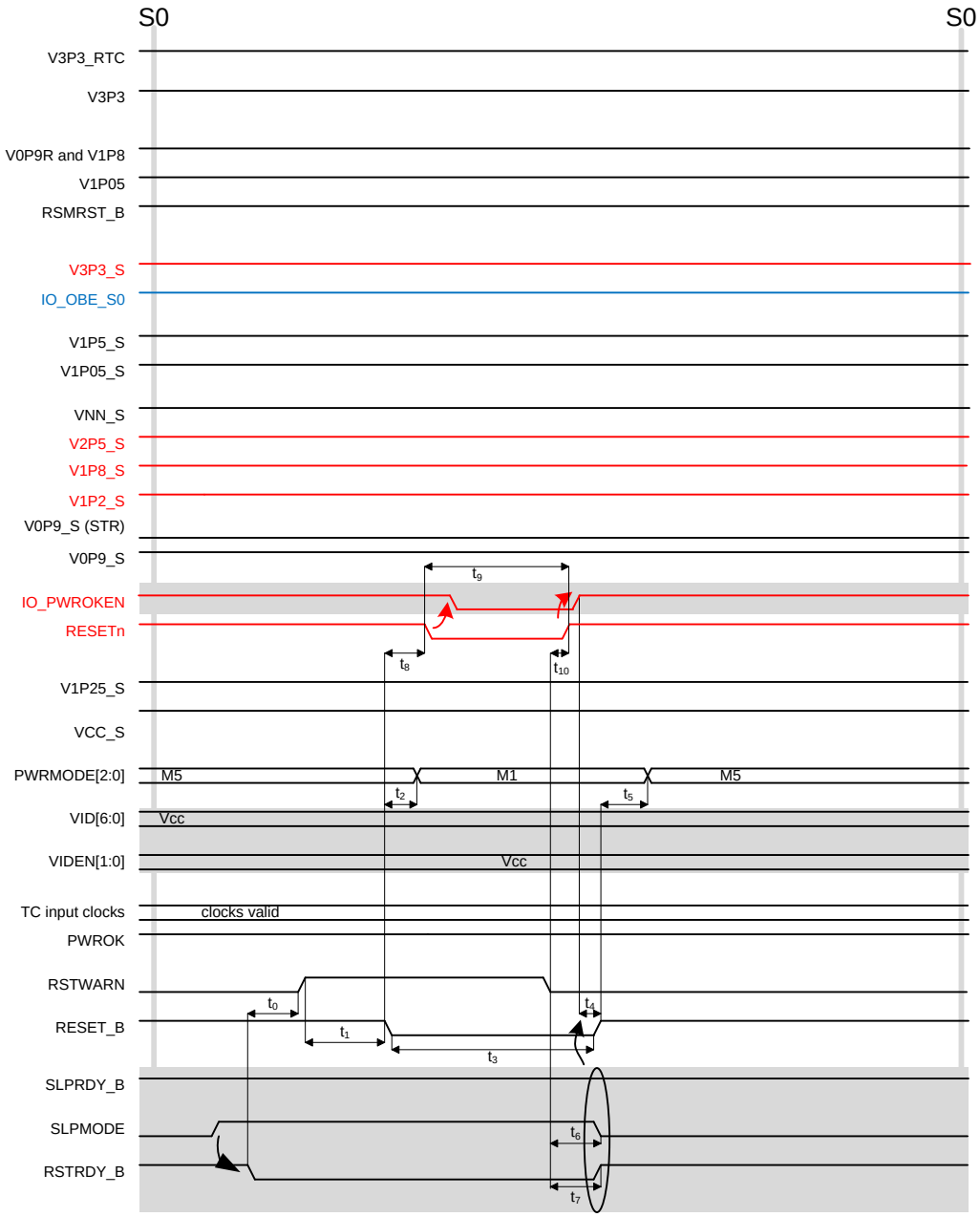


Figure 19 : Warm reset ST IOH internal triggered

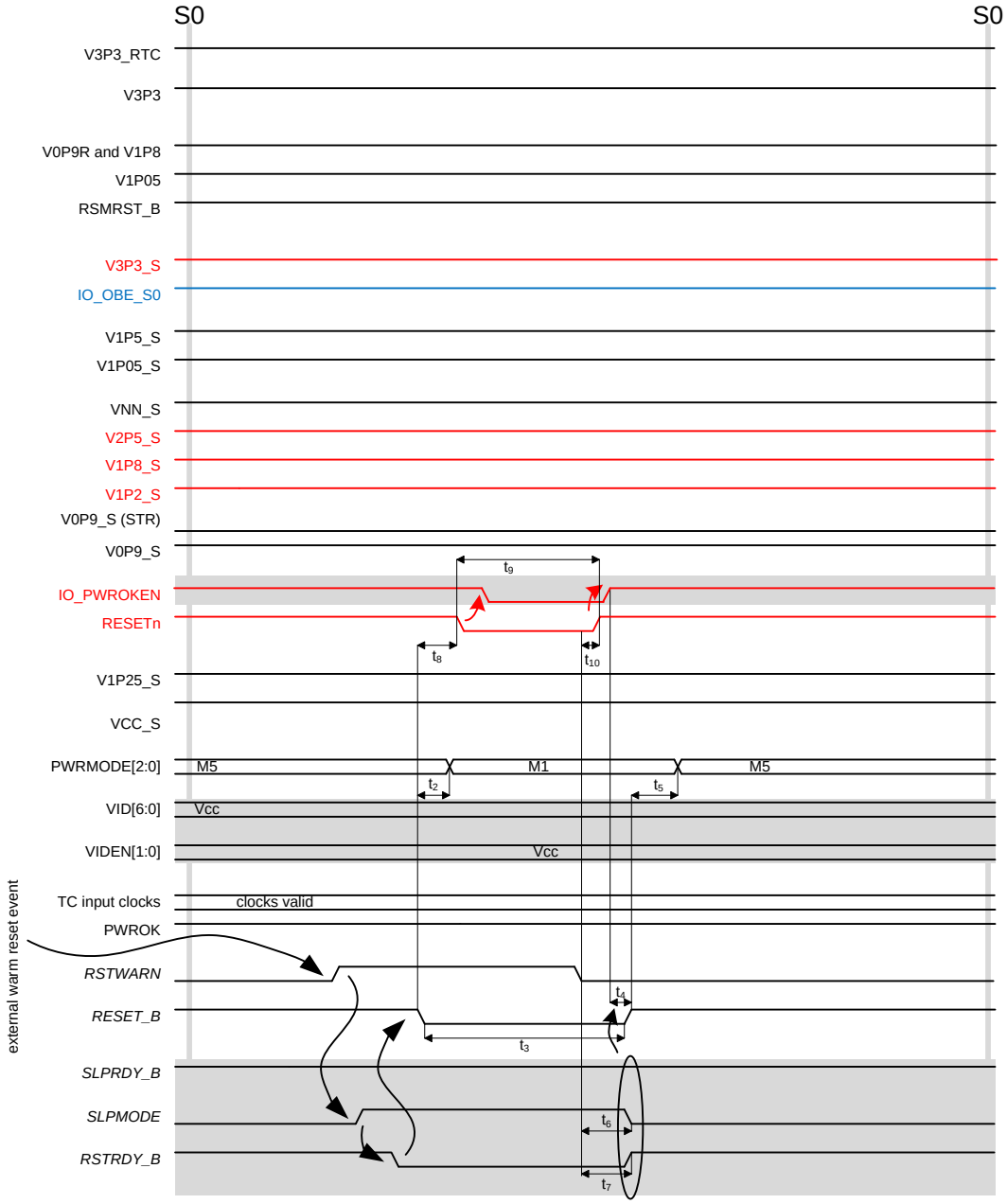


Figure 20 : Warm reset ST IOH external triggered

The delays for the warm reset sequence are given in Table 39: Warm reset timings. Note that most of the delays have not yet been specified properly by Intel. Therefore, the given timings of the IOH are subject to change. In any case, the reset assertion/de-assertion of the ST IOH will always be done prior to the release of the RESET_B of E6xx processor.

Label	Description	Min	Max	Unit	Implementation
t_0	RSTRDY_B assertion to RSTWARN assertion	0	>0	us	2
t_1	RSTWARN assertion to RESET_B assertion	0	>0	us	10
t_2	RESET_B assertion to M1 entry	0	-	us	0
t_3	RESET_B assertion period	1000	-	us	1654
t_4	Assertion of IO_PWROKEN to de-assertion to			us	0.5

Label	Description	Min	Max	Unit	Implementation
	RESET_B				
t_5	RESET_B de-assertion to M5 entry	50	-	us	100
t_6	RSTWARN de-assertion to SLPMODE assertion	-	100	us	---
t_7	RSTWARN de-assertion to RSTRDY_B de-assertion	-	100	us	---
t_8	RESET_B assertion to RESETn assertion			us	100
t_9	RESETn assertion period			us	1553
t_{10}	de-assertion of RSTWARN to de-assertion of RESETn. Since t4 is only 0.5us, t10 is set in such a way that the minimum Intel timing of 150us in between the assertion of RSTWARN and the de-assertion of RESET_B is fulfilled.			us	150

Table 39: Warm reset timings

7.6.2.8 ST ConneXt IO-Hub timing for the catastrophic shutdown

A catastrophic shutdown can be issued by the E6xx processor at any time, asynchronously to all other events occurring on the system. In this case all supplies except the RTC supply (V3P3_RTC) are being disabled. All timings will be set to their minimum value. The maximum power down sequence shall not exceed 500ms.

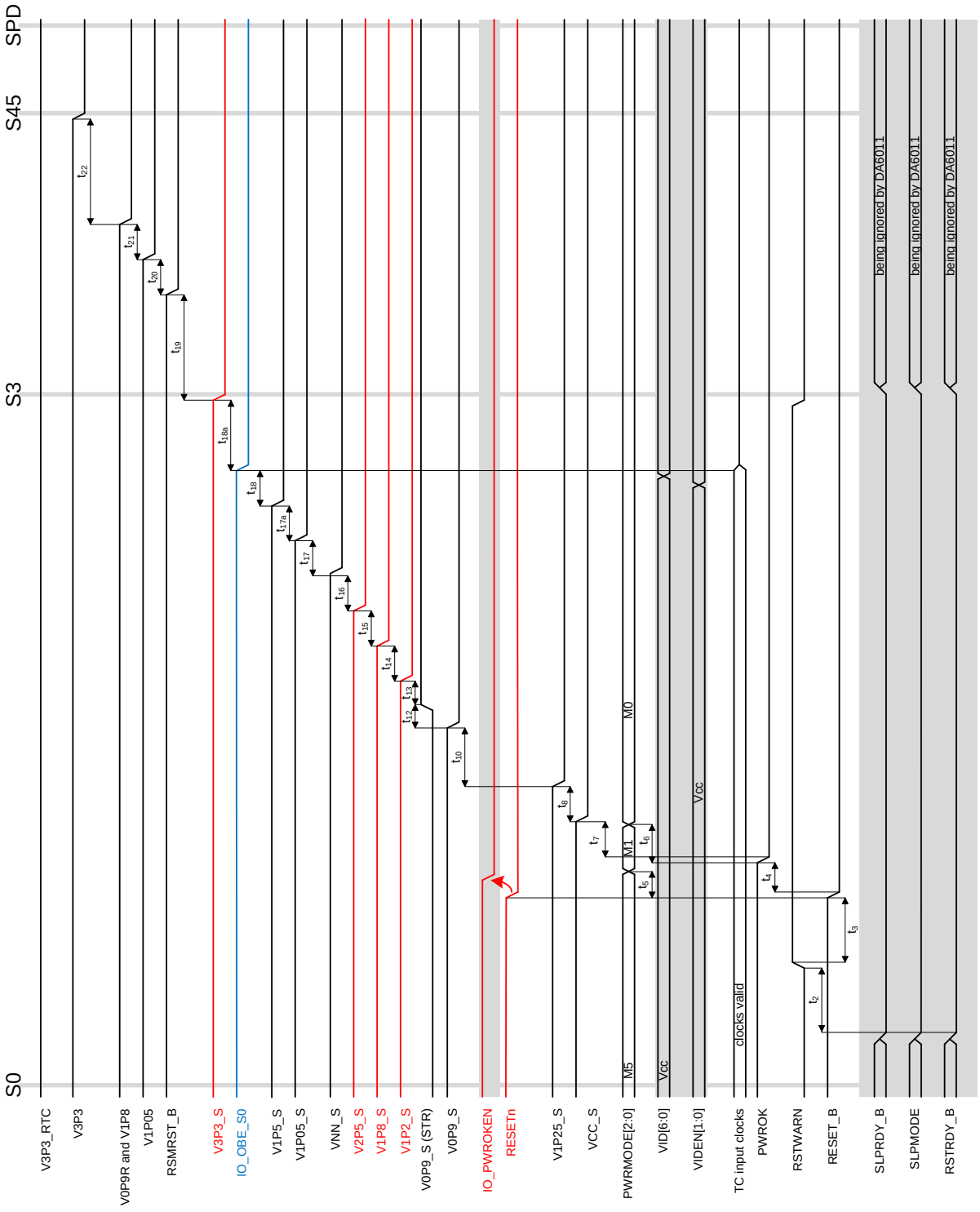


Figure 21: Catastrophic shut down ST IOH

7.6.3 Atom™ E6xx processor & OKI Semiconductor ML7213 IVI IO-Hub

7.6.3.1 Power Supplies

The following table lists the supplies for both E6xx processor and OKI Semiconductor IVI IOH. The red rows denote supplies provided to the IOH. This sequence will be used for the S-state transitions from S4/5 to S3 to S0 and vice versa.

Supply Module	Voltage domain E6XX & OKI IVI	First active state	Sequence
LDO_RTC_3P3	V3P3_RTC	S4/5	0 (E6XX)
LDO_V3P3	V3P3	S3	1 (E6XX)
BUCK_V1P8	V1P8	S3	2 (E6XX & DDR2)
LDO_V0P9R	V0P9R	S3	3 (DDR2)
LDO_V1P05	V1P05	S3	4 (E6XX)
BUCK_V1P2	V1P2_S	S0	5 (IVI_IOH)
BUCK_V3P3	V3P3_S	S0	6 (E6XX & IVI_IOH)
LDO_V1P5	V1P5_S	S0	7 (E6XX)
BUCK_V1P05	V1P05_S	S0	8 (E6XX)
BUCK_GRAPHIC	VNN_S	S0	9 (E6XX)
PD_V1P8	V1P8_S	S0	10 (E6XX)
LDO_V0P9	V0P9_S	S0	11 (DDR2)
LDO_V1P25	V1P25_S	S0	12 (E6XX)
BUCK_CORE	VCC_S	S0	13 (E6XX)

7.6.3.2 PLLs

The following clocks will be provided for the IO-Hub and the processor. The group label corresponds to the signal name in the timing diagrams.

Source	Clock	First active state	Group
PLL3	SYS_25MHz	S0	IO_OBE_S0
PLL2	USB_48MHz	S0	IO_OBE_S0
PLL3	SATA_CLK	S0	IO_OBE_S0
PLL1	PCIE_CLK	S0	IO_OBE_S0
PLL5	MCLK	S0	IO_OBE_S0
E6xx processor Input clocks		S0	IO_OBE_S0

7.6.3.3 OKI Semiconductor IVI IO-Hub timing for SPD to S0

Label	Description	Min	Max	Unit	Implementation
t_{10}	enabling of V3P3_RTC to enabling of V3P3		-	us	1000
t_{10a}	enabling of V3P3 to enabling of V0P9R and V1P8			us	1000
t_{11}	enabling of V0P9R and V1P8 to enabling of V1P05		-	us	2000
t_{12}	enabling of V1P05 to de-assertion of RSMRST_B	5000	-	us	6000
t_{13}	de-assertion of RSMRST_B to S3 and S0 clocks stable			us	11000
t_{13a}	S3 and S0 clocks stable to enabling of V1P2_S			us	1000
t_{14}	enabling of V1P2_S to enabling of V3P3_S			us	1000
t_{15}	enabling of V3P3_S to enabling of V1P5_S			us	1000
t_{19}	enabling of V1P5_S to enabling of V1P05_S			us	1000

Label	Description	Min	Max	Unit	Implementation
t_{20}	enabling of V1P05_S to enabling of VNN_S			us	500
t_{21}	enabling of VNN_S to enabling of V1P8_S			us	1000
t_{21a}	enabling of V1P8_S to de-activating V0P9_S (STR)			us	1000
t_{22}	de-activating V0P9_S (STR) to enabling of V0P9_S			us	1000
t_{24}	enabling of V0P9_S to enabling of V1P25_S			us	1000
t_{25}	enabling of V1P25_S to enabling of VCC_S			us	1000
t_{26}	VCC_S stable to PWRMODE=M2	25	-	us	2050
t_{27}	time in M2	10	20	us	15
t_{28}	timing determined by TC				
t_{29}	VID/VIDen out to new VNN stable delay	45	100	us	100
t_{30}	Required time in M3 (t31+t36+t34)	2500	-	us	4860.5
t_{31}	Entry to M3 assertion of PWROK			us	500
t_{34}	de-assertion of IO_RESET_B to de-assertion of RESET_B	0	1	us	0.5
t_{36}	PWROK toggling to de-assertion of IO_RESET_B (and 0.5us later RESET_B)	250		us	4360.5
t_{37}	de-assertion of RESET_B to PWRMODE change to M1	5		us	10
t_{42}	time in M1 (includes ramping VCC_S to new target voltage after VIDEN = VCC)			us	200

Table 40: Timings for OKI Semiconductor IVI IOH

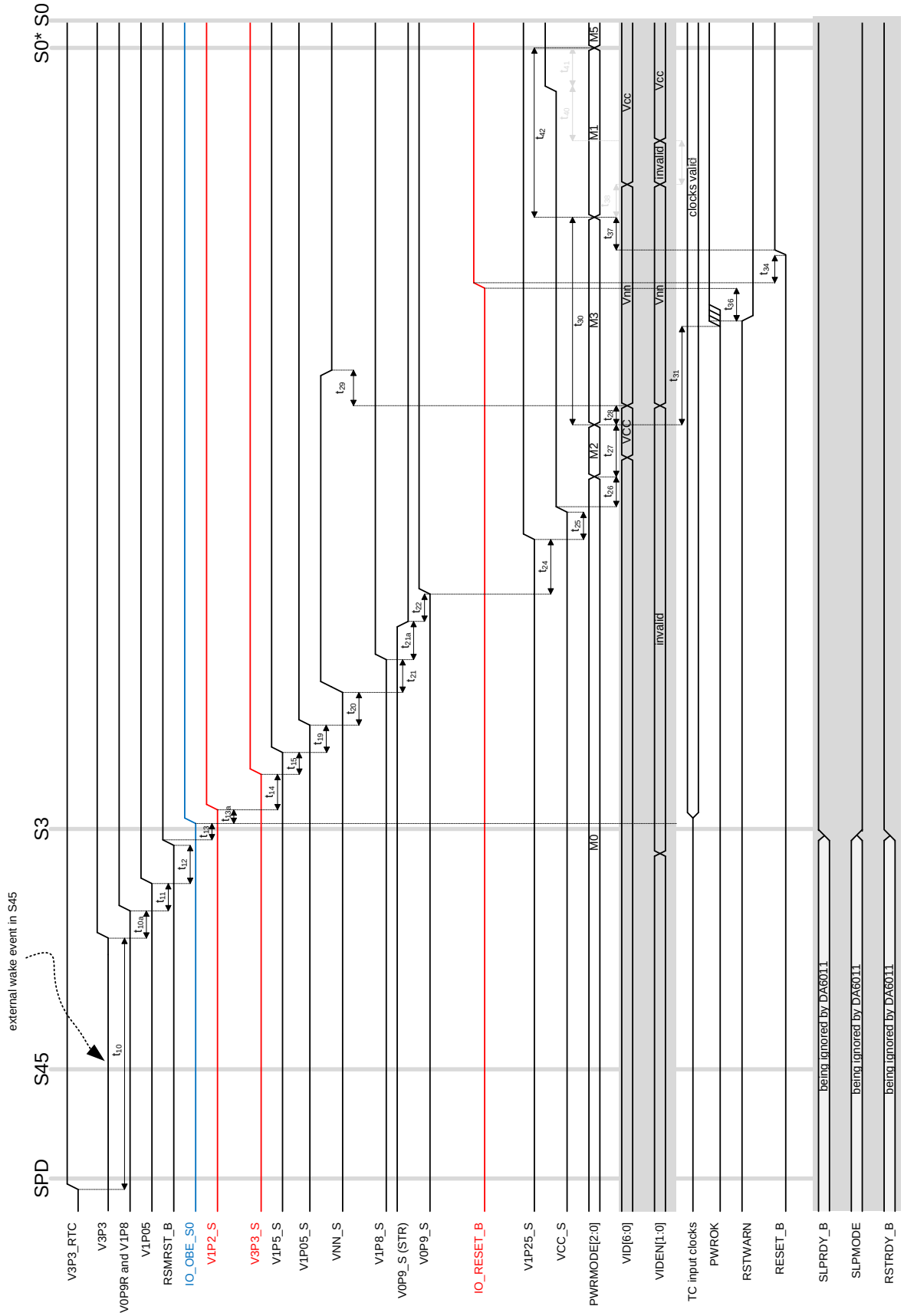


Figure 22 : SPD to S0 timing E6XX & OKI IVI IO-Hub

7.6.3.4 OKI Semiconductor IVI IO-Hub timing for S0 to SPD

Label	Description	Min	Max	Unit	Implementation
t_0	Intel TC timing – not relevant for DA6011				---
t_1	SLPRDY_B assertion to assertion of RSTWARN	0		us	10
t_2	Intel TC timing – not relevant for DA6011				---
t_3	RSTRDY_B assertion to assertion of RESET_B and IO_RESET_B (directly 0.5us after assertion of RESET_B)	0		us	10
t_4	RESET_B assertion to PWROK de-assertion	0		us	20
t_5	RESET_B assertion to M5->M1 transition	0		us	10
t_6	PWROK de-assertion to M1->M0 transition	0		us	10
t_7	PWROK de-assertion to disabling of VCC_S	0		us	20
t_8	disabling of VCC_S to disabling of V1P25_S			us	1000
t_{10}	disabling of V1P25_S to disabling of V0P9_S			us	1000
t_{10a}	disabling of V0P9_S to enabling V0P9_S (STR)			us	1000
t_{11}	enabling of V0P9_S (STR) to disabling of V1P8_S			us	1000
t_{12}	disabling of V1P8_S to disabling of VNN_S			us	1000
t_{13}	disabling of VNN_S to disabling of V1P05_S			us	1000
t_{13a}	disabling of V1P05_S to disabling of V1P5_S			us	1000
t_{16}	disabling of V1P5_S to disabling of V3P3_S			us	1000
t_{17}	disabling of V3P3_S to disabling of V1P2_S	0	-	us	1000
t_{18}	disabling of V1P2_S to disabling of S0 clocks			us	10000
t_{19}	disabling of S0 clocks to assertion of RSMRST_B (in case of direct transition) plus delay	0	-	us	1010
t_{20}	assertion of RSMRST_B to disabling of V1P05	0	-	us	10
t_{21}	disabling of V1P05 to disabling of V0P9R and V1P8	0	-	us	1000
t_{22}	disabling of V0P9R and V1P8 to disabling of V3P3	0	-	us	1000
t_{26}	determined by Atom E6xx				---
t_{27}	determined by Atom E6xx				---
t_{28}	determined by Atom E6xx				---

Table 41: Timings for OKI Semiconductor IVI IOH for S0 to SPD transition

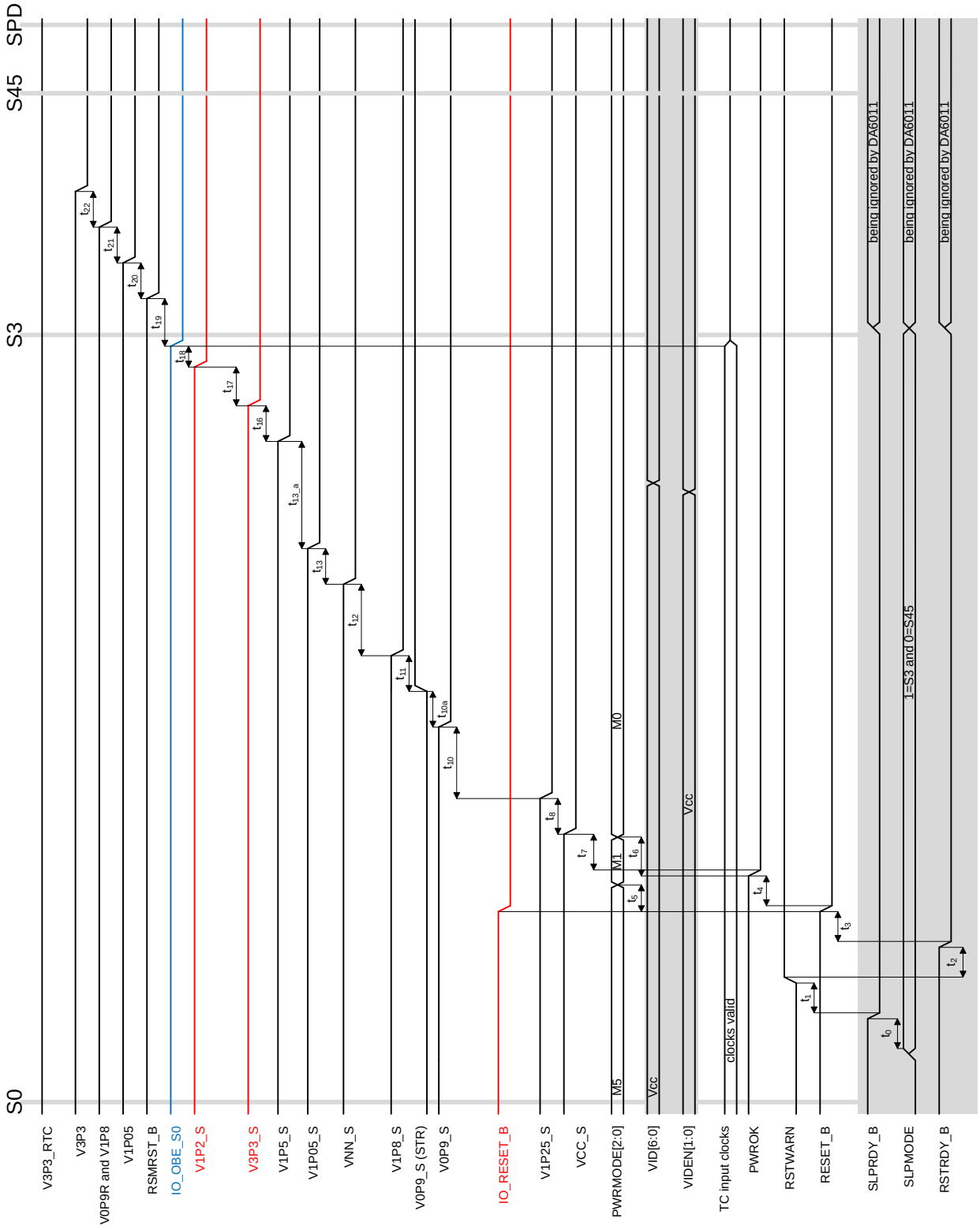


Figure 23 : S0 to SPD timing OKI IVI IOH

7.6.3.5 OKI Semiconductor IVI IO-Hub timing for S3 to S0 Sequence (internal & external)

From the sequence described in Chapter OKI Semiconductor MP IO-Hub timing for SPD to S0, the S3 to S0 sequence can be derived by including the handshaking signals of the E6xx processor. The timings will be the same as provided for the S4/5 to S0 sequence. The S3 to S0 sequence is given in the following figure.

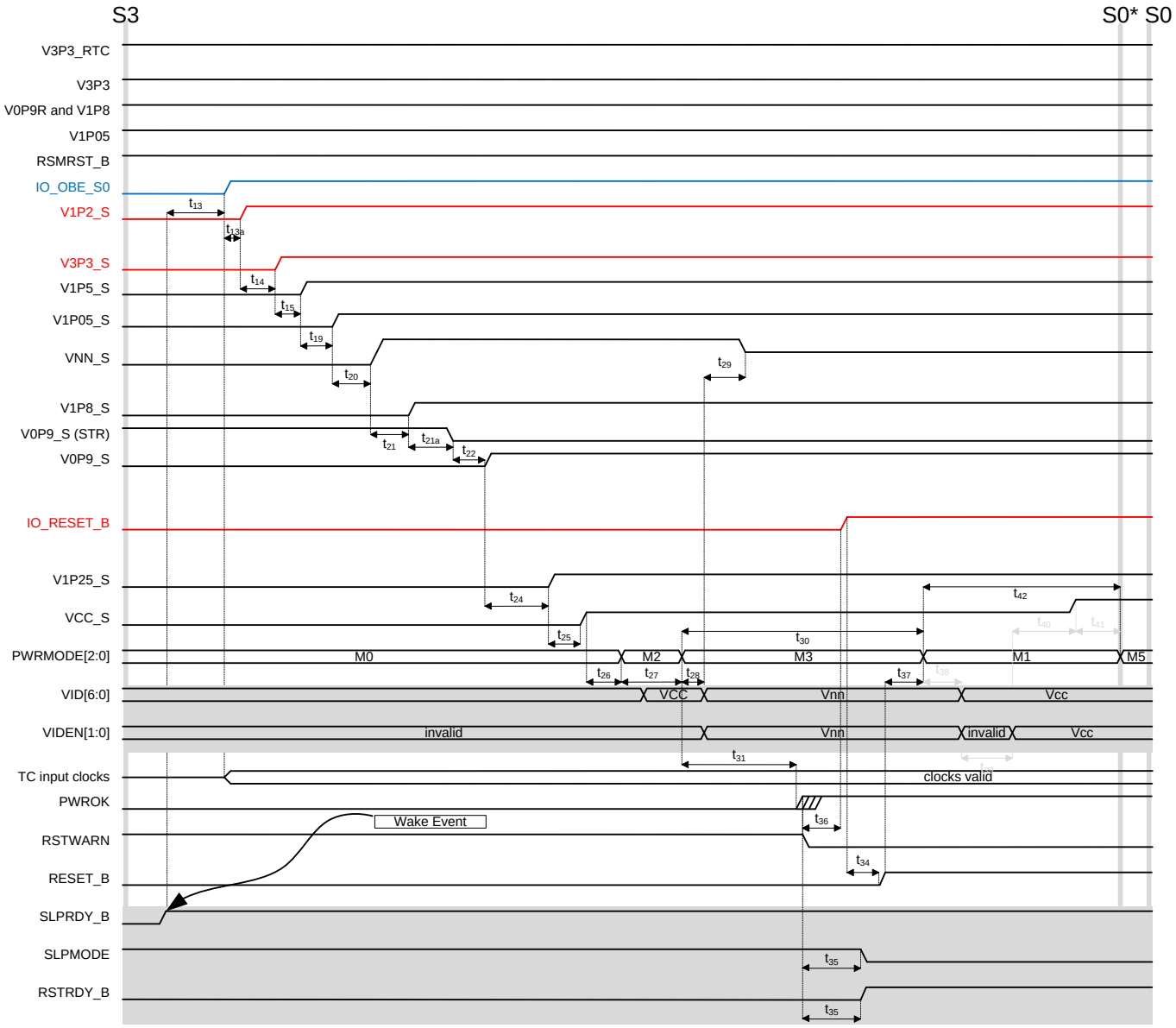


Figure 24 : S3 to S0 timing OKI IVI IOH internal

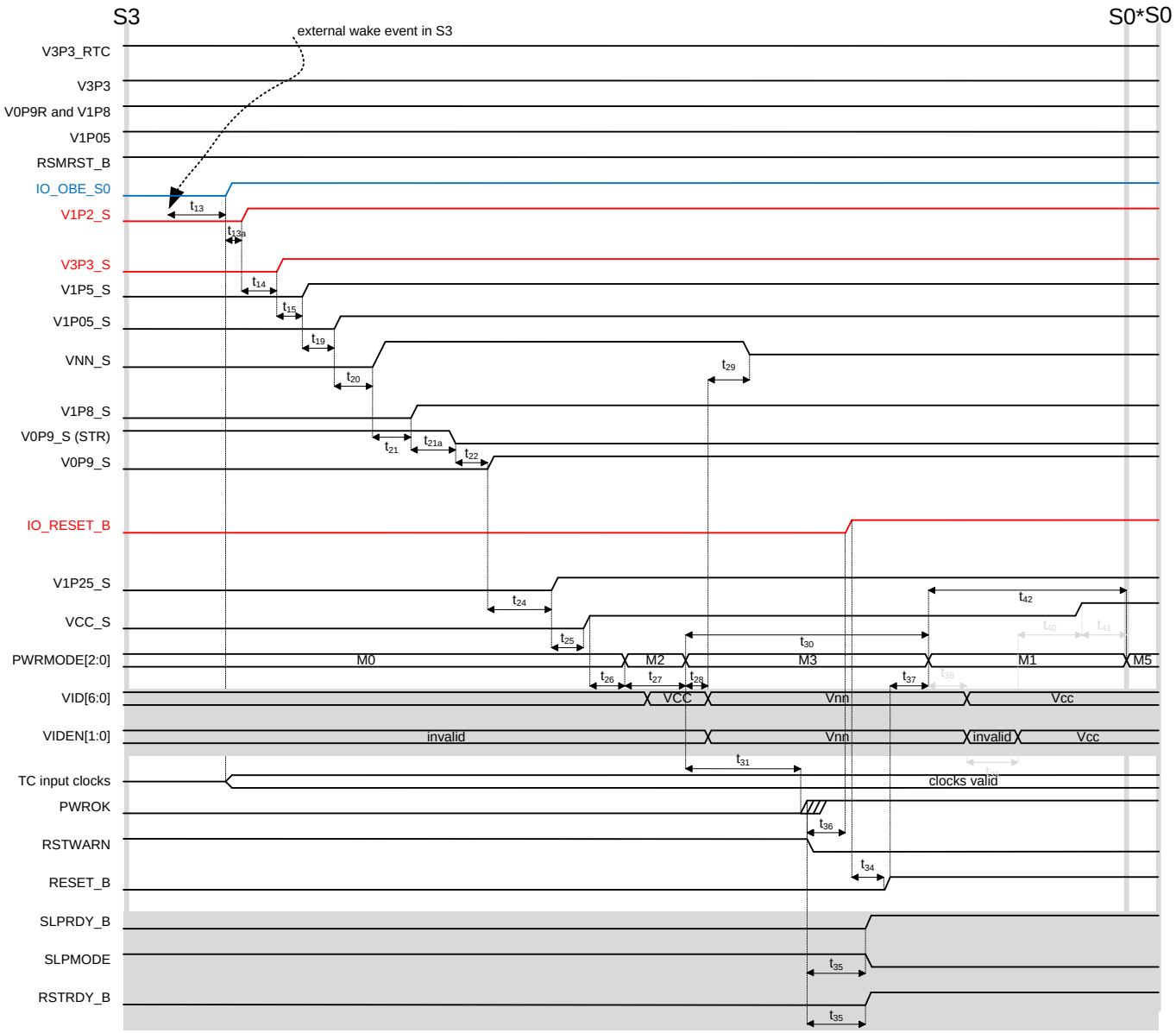


Figure 25 : S3 to S0 timing OKI IVI IOH external

7.6.3.6 OKI Semiconductor IVI IO-Hub timing for Cold Reset

During a cold reset E6xx processor and the IOH will undergo a power cycling. The timings for the S0 to S4/5 sequence are basically the same as for the sequence described in chapter 7.6.4.4. Once in S4/5 the cold reset period will be 4 seconds before the S4/5 to S0 sequence starts in the same way as defined in chapter 7.6.4.3.

Label	Description	Min	Max	Unit	Implementation
t_2	RSTRDY_B assertion to RSTWARN assertion	0		µs	10
t_3	RSTWARN assertion to RESET_B assertion	-		µs	10
t_{30}	Cold reset period			ms	4000

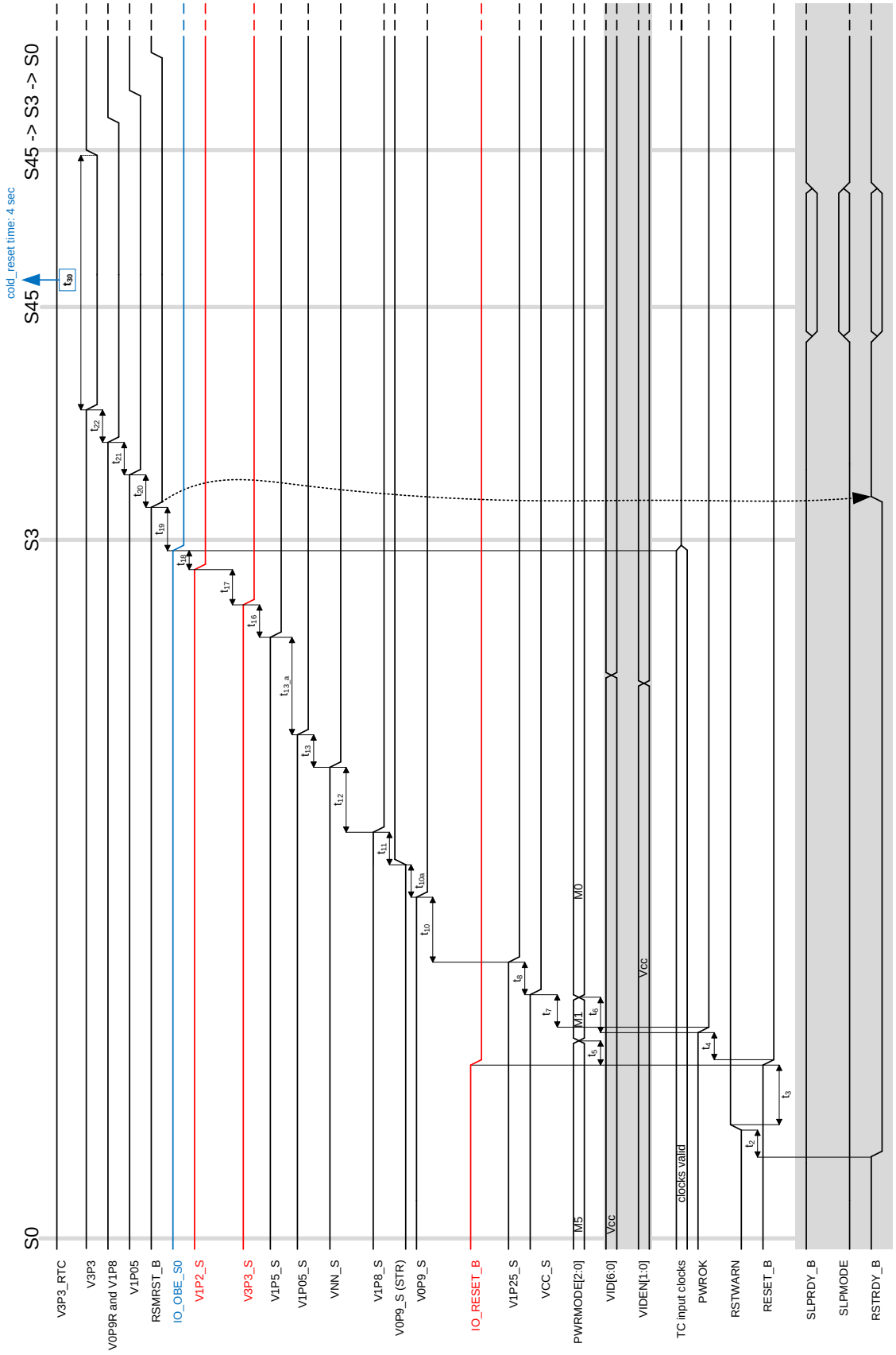


Figure 26 : Cold reset OKI IVI IOH

7.6.3.7 OKI Semiconductor IVI IO-Hub timing for Warm Reset (internal & external)

During a warm reset issued by Atom™ E6xx processor the reset signal of the OKI Semiconductor IVI IOH also gets asserted for resetting the internal IOH logic. The following diagram shows the warm reset sequence for OKI Semiconductor IVI IOH and E6xx processor. The external warm reset is triggered by the assertion of RESET_IN_B instead of the processor handshake signals. After such assertion of RESET_IN_B DA6011 asserts RSTWARN and after the assertion of RSTRDY_B it continues in the same way as during an internal warm reset.

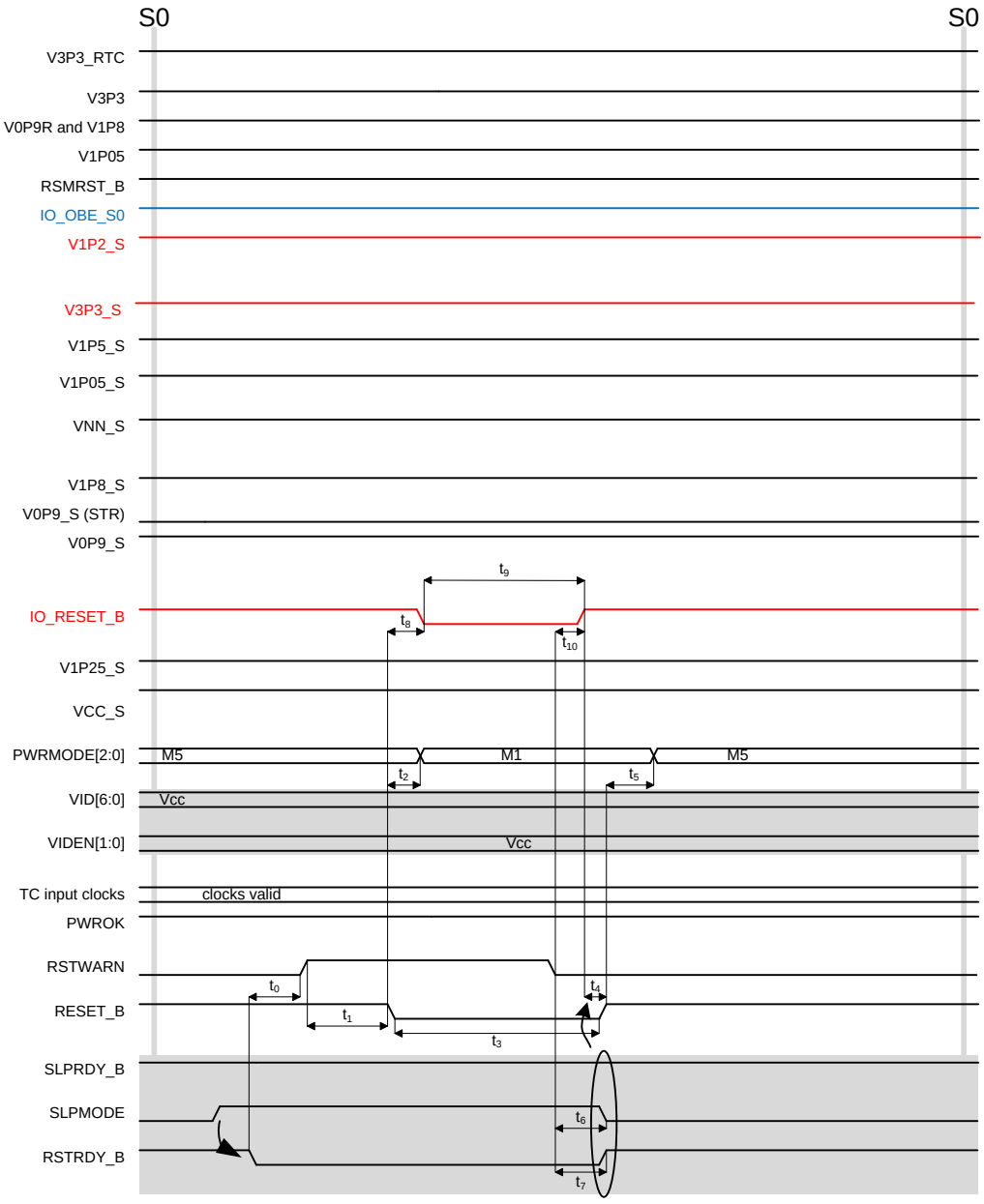


Figure 27: Warm reset OKI IVI IOH internal

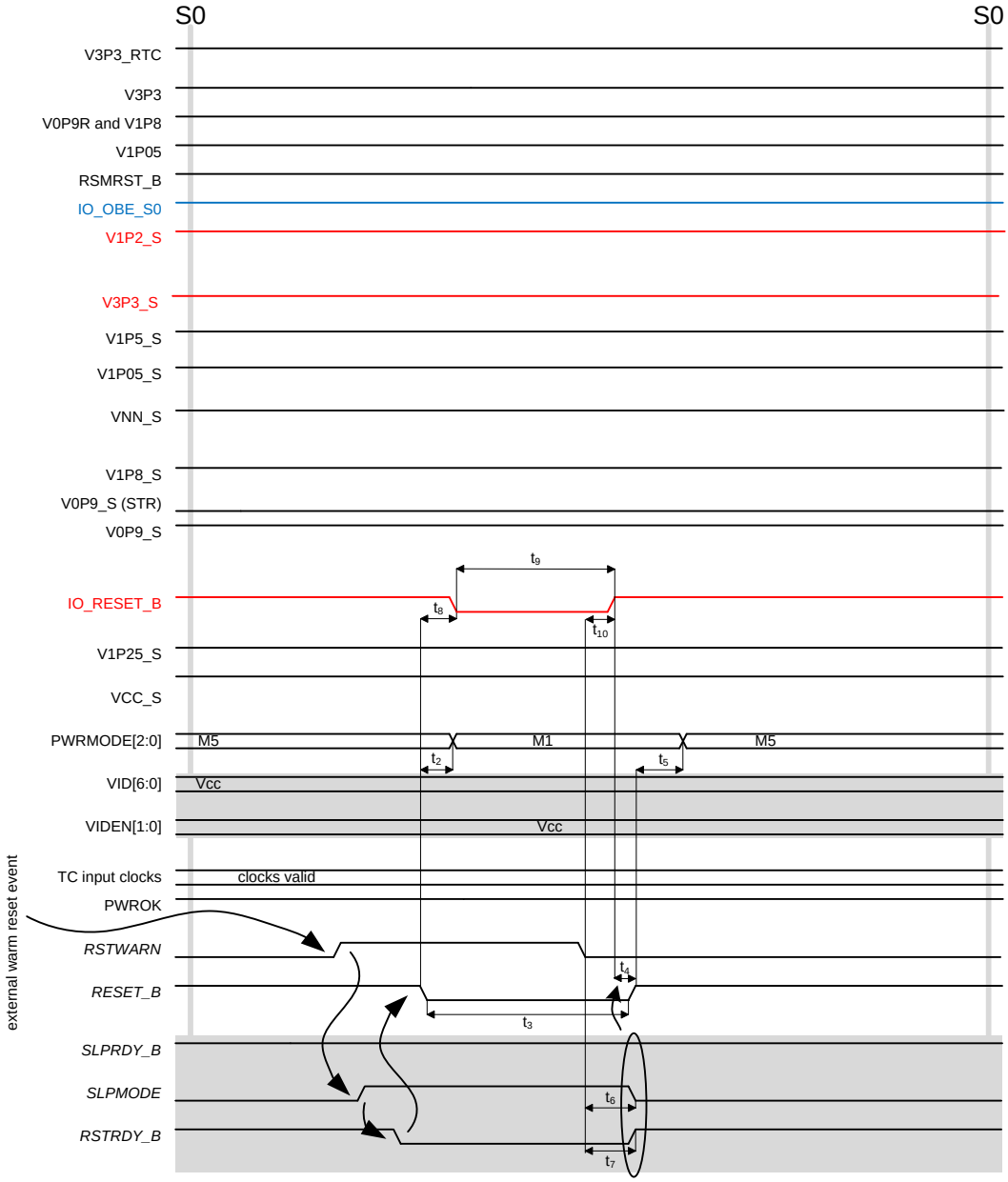


Figure 28: Warm reset OKI IVI IOH external

The delays for the warm reset sequence are given in chapter 7.6.4.4. Note: Intel to provide validated results. Therefore, the given timings of the IOH are subject to change. In any case, the reset assertion de-assertion of the OKI Semiconductor IVI IOH will always be done prior to the release of the RESET_B of E6xx processor E6XX.

Label	Description	Min	Max	Unit	Implementation
t_0	RSTRDY_B assertion to RSTWARN assertion	0	>0	us	>0
t_1	RSTWARN assertion to RESET_B assertion	0	>0	us	10
t_2	RESET_B assertion to M1 entry	0	-	us	0
t_3	RESET_B assertion period	1000	-	us	1654
t_4	de-assertion of IO_RESET_B to de-assertion of RESET_B			us	0.5

Label	Description	Min	Max	Unit	Implementation
t_5	RESET_B de-assertion to M5 entry	50	-	us	100
t_6	RSTWARN de-assertion to SLPMODE assertion		100	us	---
t_7	RSTWARN de-assertion to RSTRDY_B de-assertion		100	us	---
t_8	RESET_B assertion to IO_RESET_B assertion			us	100
t_9	IO_RESET_B assertion period			us	1553
t_{10}	de-assertion of RSTWARN to de-assertion of IO_RESET_B. Since t4 is only 0.5 us, t10 is set in such a way that the minimum Intel timing of 150us in between the assertion of RSTWARN and the de-assertion of RESET_B is fulfilled.			us	150

Table 42: Warm reset delays E6XX & OKI IVI IOH

7.6.3.8 OKI Semiconductor IVI IO-Hub Catastrophic Shutdown

A catastrophic shutdown can be issued by E6xx processor at any time, asynchronously to all other events occurring on the system. In this case all supplies except the RTC supply (V3P3_RTC) are being disabled. All timings will be set to their minimum value. The power down sequence will not exceed 500ms.

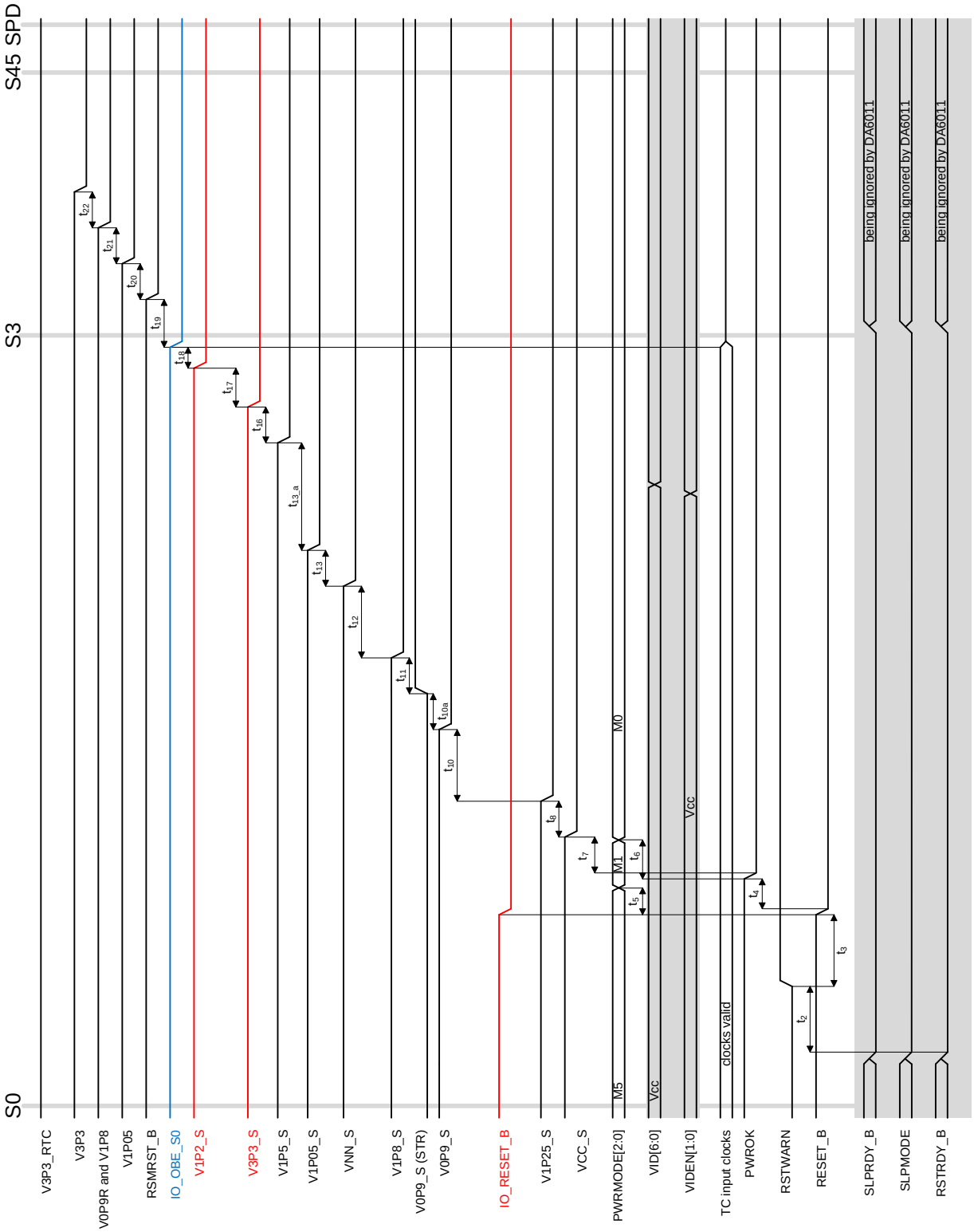


Figure 29 : Catastrophic shutdown OKI IVI IOH

7.6.4 Atom™ E6xx processor & OKI Semiconductor ML7223 MP IO-Hub

7.6.4.1 Supplies

The following table lists the supplies for OKI Semiconductor MP IO-Hub. This sequence will be used for the S-state transitions from S4/5 to S3 to S0 and vice versa.

Supply Module	Voltage domain TC & OKI MP	First active state	Sequence
LDO_RTC_3P3	V3P3_RTC	S4/5	0 (E6XX)
BUCK_V1P2	V1P2_A	S4/5	1 (OKI MP)
LDO_V2P5	V2P5_A	S4/5	2 (OKI MP)
LDO_V3P3	V3P3_A	S4/5	3 (OKI MP)
PD_V1P2	V1P2	S3	4 (OKI MP)
BUCK_V3P3	V3P3	S3	5 (E6XX & OKI MP)
BUCK_1P8	V1P8	S3	6 (E6XX & DDR2)
LDO_0P9R	V0P9R	S3	7 (DDR2)
LDO_V1P05	V1P05	S3	8 (E6XX)
LDO_VUNI	V1P2_S	S0	9 (OKI MP)
PD_V3P3	V3P3_S	S0	10 (E6XX & OKI MP)
LDO_V1P5	V1P5_S	S0	11 (E6XX)
BUCK_V1P05	V1P05_S	S0	12 (E6XX)
BUCK_GRAPHIC	VNN_S	S0	13 (E6XX)
PD_V1P8	V1P8_S	S0	14 (E6XX)
LDO_V0P9	V0P9_S	S0	15 (DDR2)
LDO_V1P25	V1P25_S	S0	16 (E6XX)
BUCK_CORE	VCC_S	S0	17 (E6XX)

7.6.4.2 PLLs

The following clocks will be provided for the IO hub and processor. The group label corresponds to the signal name in the timing diagrams.

Source	Clock	First active state	Group
PLL3	SYS_25MHz	S4/5	IO_OBE_SYS
PLL2	USB_48MHz	S3	IO_OBE_USB
PLL3	SATA_CLK	S0	IO_OBE_S0
PLL1	PCIE_CLK	S0	IO_OBE_S0
PLL5	MCLK	S0	IO_OBE_S0
E6xx processor Input clocks		S0	IO_OBE_S0

7.6.4.3 OKI Semiconductor MP IO-Hub timing for SPD to S0

Label	Description	Min	Max	Unit	Implementation
t_1	enabling of V3P3_RTC to enabling of V1P2_A	0	-	us	variant dependent
t_2	enabling of V1P2_A to enabling of V2P5_A	0	-	us	2000
t_3	enabling of V2P5_A to enabling of V3P3_A	0	-	us	2000
t_{3a}	enable PLLs and enable output buffer IO_OBE_SYS			us	26500
t_4	S45 clocks stable to de-assertion of IO_RST_PLA_B	10	-	us	15
t_5	de-assertion of IO_RST_PLA_B to de-assertion of IO_SLP_PLB_B	200	-	us	250
t_6	de-assertion of IO_SLP_PLB_B to enabling of V1P2	0	-	us	250
t_7	enabling of V1P2 to enabling of V3P3	0	-	us	1000
t_8	enable PLLs and enable output buffer IO_OBE_USB		-	us	2500
t_9	S3 clocks stable to de-assertion of IO_RST_PLB_B	10	-	us	15
t_{10}	enabling of PLL output buffer to enabling V0P9R and V1P8	0	-	us	1000
t_{11}	enabling of V0P9R and V1P8 to enabling of V1P05	0	-	us	2000
t_{12}	enabling of V1P05 to de-assertion of RSMRST_B	5000	-	us	6000
t_{13}	de-assertion of RSMRST_B to assertion of IO_SLP_PLC_B	0	-	us	100
t_{14}	de-assertion of IO_SLP_PLC_B to enabling of V1P2_S	0	-	us	50
t_{14a}	enabling of V1P2_S to enabling of V3P3_S	0	-	us	1000
t_{15}	enabling of V3P3_S to enable PLLs and IO_OBE_S0	0	-	us	8000
t_{16}	enabling of V3P3_S to assertion of IO_PWROK	20	-	us	2000
t_{18}	enabling of V3P3_S to enabling of V1P5_S	0	-	us	1000
t_{19}	enabling of V1P5_S to enabling of V1P05_S	0	-	us	1000
t_{20}	enabling of V1P05_S to enabling of VNN_S	0	-	us	500
t_{21}	enabling of VNN_S to enabling of V1P8_S	0	-	us	2000
t_{22}	enabling o f V1P8_S to de-activating V0P9_S(STR)	0	-	us	1000
t_{22a}	de-activating V0P9_S(STR) to enabling of V0P9_S	0	-	us	500
t_{24}	enabling of V0P9_S to enabling of V1P25_S	0	-	us	1000
t_{25}	enabling of V1P25_S to enabling of VCC_S	0	-	us	2500
t_{26}	VCC_S stable to PWRMODE=M2	25	-	us	2000
t_{27}	time in M2	10	20	us	15
t_{28}	timing determined by TC				
t_{29}	VID/VIDen out to new VNN stable delay	45	100	us	100
t_{30}	Required time in M3 (t31+t36+t34)	2500	-	us	6000
t_{31}	Entry to M3 assertion of PWROK			us	500
t_{34}	de-assertion of IO_RST_PLC_B to de-assertion of RESET_B	0	1	us	0.5
t_{36}	PWROK toggling to de-assertion of IO_RSTPLC_B (and 0.5us later RESETB)	250		us	5500
t_{37}	de-assertion of RESET_B to PWRMODE change to M1	5		us	10
t_{42}	time in M1 (includes ramping VCC_S to new target voltage after VIDEN = VCC)			us	200

Table 43: Timings for OKI Semiconductor MP IO-Hub

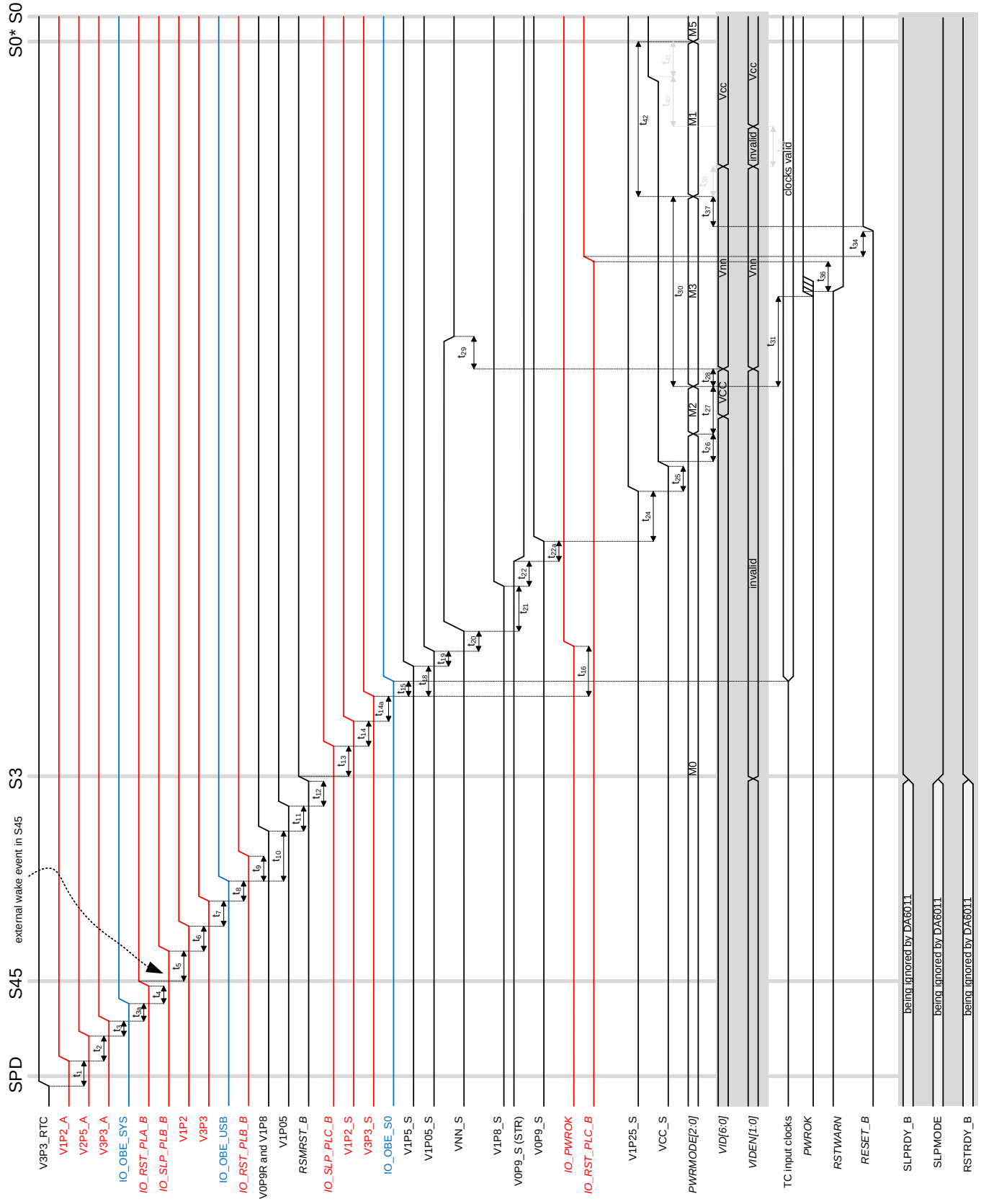


Figure 30: SPD to S0 timing for E6XX & OKI MP IOH

7.6.4.4 OKI Semiconductor MP IO-Hub timing for S0 to SPD

Label	Description	Min	Max	Unit	Implementation
t_0	Intel TC timing – not relevant for DA6011				---
t_1	SLPRDY_B assertion to assertion of RSTWARN	0		us	10
t_2	Intel TC timing – not relevant for DA6011				---
t_3	RSTRDY_B assertion to assertion of RESET_B and IO_RST_PLC_B (directly 0.5us after assertion of RESET_B)	0		us	10
t_4	RESET_B assertion to PWROK de-assertion	0		us	20
t_5	RESET_B assertion to M5->M1 transition	0		us	10
t_6	PWROK de-assertion to M1->M0 transition	0		us	10
t_7	PWROK de-assertion to disabling of VCC_S	0		us	20
t_8	disabling of VCC_S to disabling of V1P25_S			us	3000
t_9	disabling of V1P25_S to disabling of V0P9_S			us	1000
t_{10}	disabling of V0P9_S to enabling of V0P9_S (STR)			us	1000
t_{11}	enabling of V0P9_S (STR) to disabling of V1P8_S			us	2000
t_{12}	disabling of V1P8_S to disabling of VNN_S			us	1000
t_{13}	disabling of VNN_S to disabling of V1P05_S			us	1000
t_{13_a}	disabling of V1P05_S to disabling of V1P5_S	0	-	us	1000
t_{13_b}	disabling of VCC_S to disabling of S0 clocks	0	-	us	1000
t_{15}	disabling of V1P05_S to de-assertion of IO_PWROK	0	-	us	1000
t_{16}	Tpwd1; IO_PWROK de-assertion to IO_SLP_PLC_B assertion	0	-	us	10
t_{17}	Disabling of V1P05_S to disabling of V3P3_S	-	-	us	1000
t_{18}	Tpwd3_2; disabling of V3P3_S to disabling of V1P2_S	0	-	us	1000
t_{19}	disabling of V1P2_S to assertion of RSMRST_B (in case of direct transition) plus delay	0	-	us	1000
t_{20}	RSMRST_B assertion to disabling of V1P05	0	-	us	10
t_{21}	disabling V1P05 to disabling of V0P9R and V1P8	0	-	us	1000
t_{22_a}	disabling of V0P9R and V1P8 to disabling of S3 clocks	0	-	us	1000
t_{22}	disabling of V0P9R and V1P8 to assertion of IO_RST_PLB_B	0	-	us	10
t_{23}	Tpwd4; assertion of IO_RST_PLB_B to assertion of IO_SLP_PLB_B	0	-	us	10
t_{24}	S3 clocks disabled to disabling of V3P3	0	-	us	2000
t_{25}	Tpwd4_2; disabling of V3P3 to disabling of V1P2	0	-	us	1000
t_{26}	disabling of V1P2 to assertion of IO_RST_PLA_B (in case of direct transition) plus delay	0	-	us	1010
t_{27}	assertion of IO_RST_PLA_B to disabling of S45 clocks	0	-	us	1000
t_{28}	S45 clocks disabled to disabling of V3P3_A	0	-	us	15000
t_{29}	disabling of V3P3_A to disabling of V2P5_A	0	-	us	1000
t_{30}	disabling o f V2P5_A to disabling of V1P2_A	0	-	us	1000

Table 44: Timings for OKI Semiconductor MP IO-Hub for S0 to SPD transition

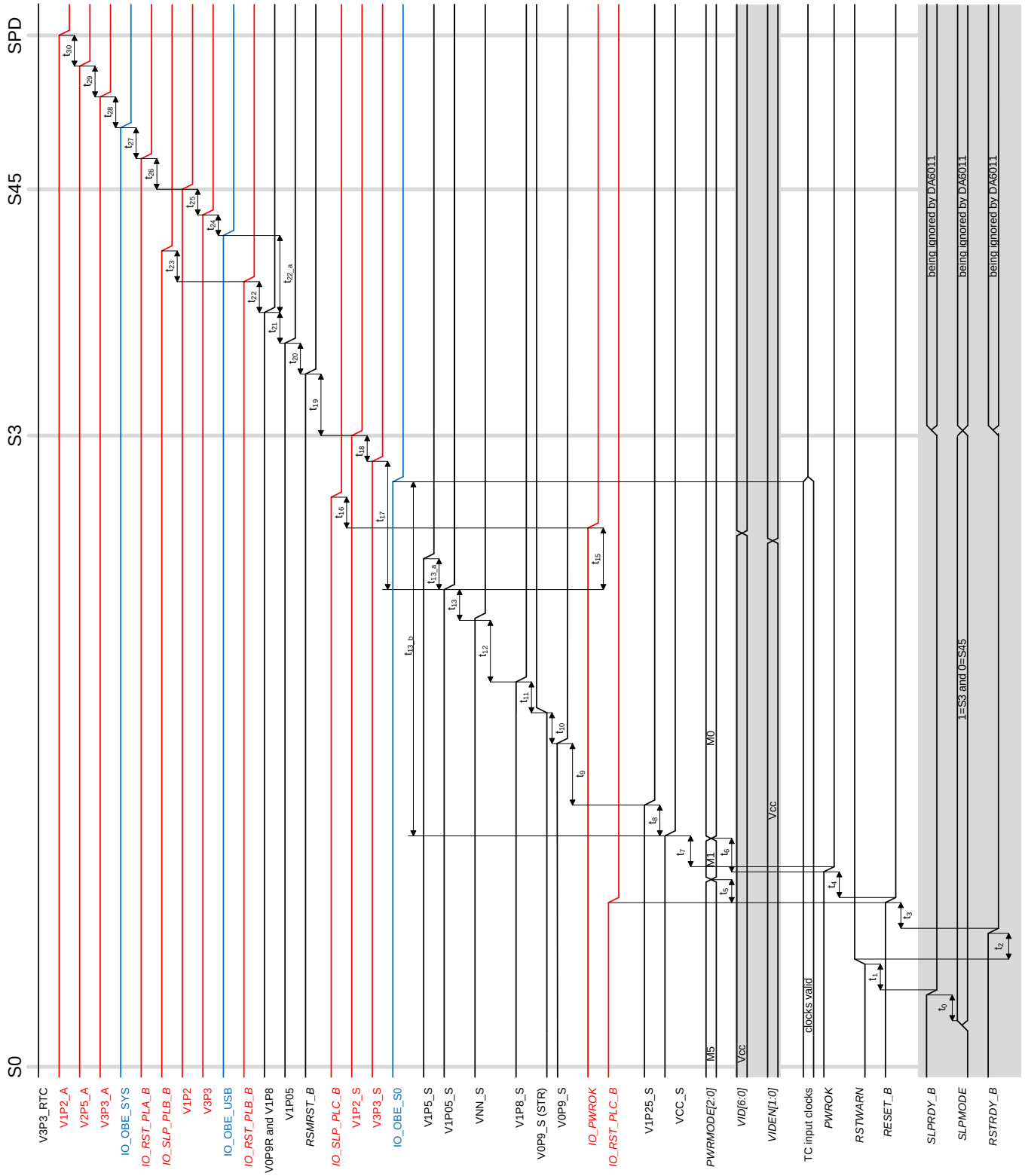


Figure 31 : S0 to SPD timing OKI MP IOH

7.6.4.5 OKI Semiconductor MP IO-Hub timing for S3 to S0 Sequence (internal & external)

From the sequence described in chapter 7.6.4.3 the S3 to S0 sequence can be derived by including the handshaking signals of E6xx processor. The timings will be the same as provided for the S4/5 to S0 sequence. The S3 to S0 sequence is given in the following figure.

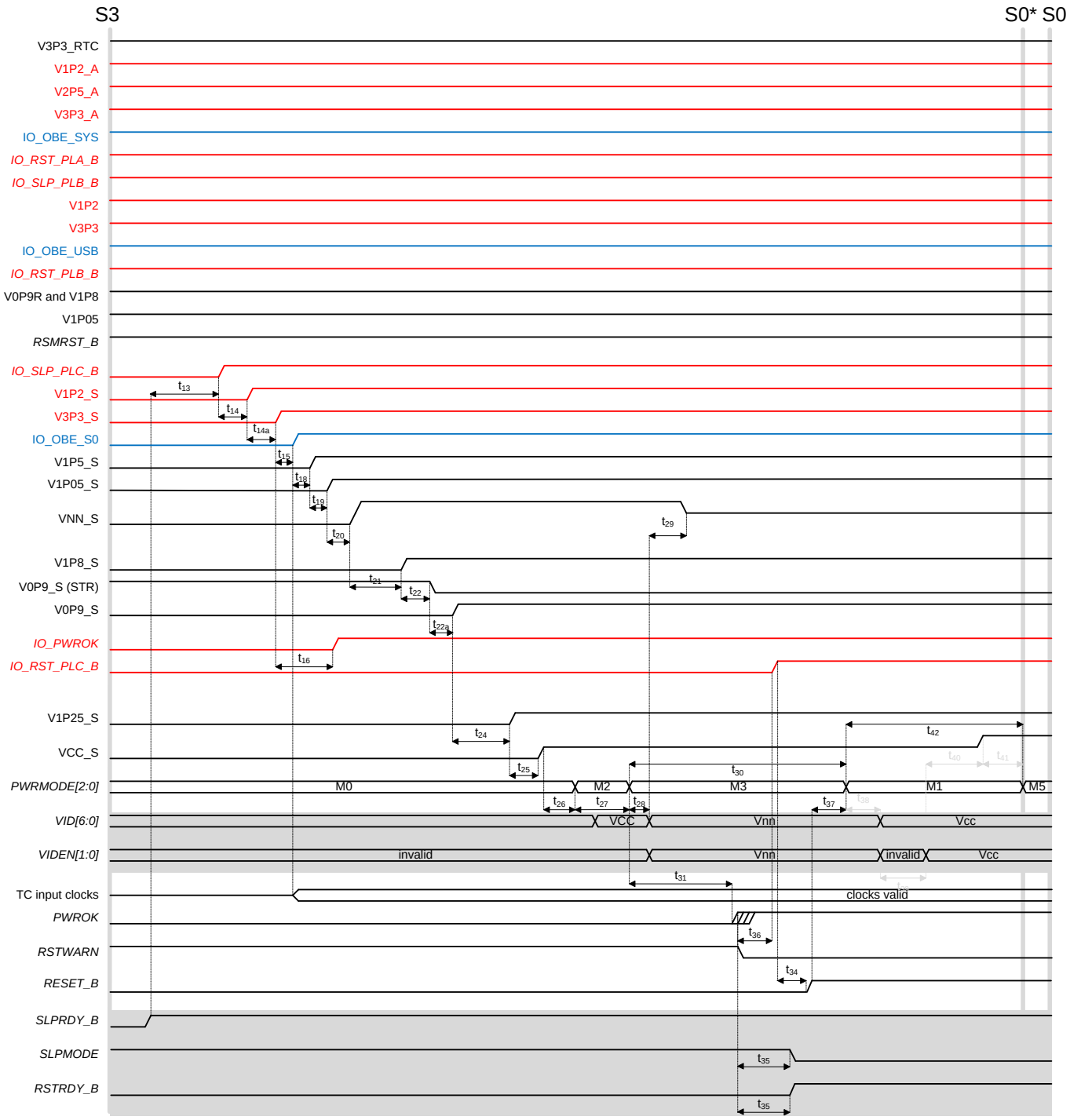


Figure 32 : S3 to S0 timing OKI MP IOH internal

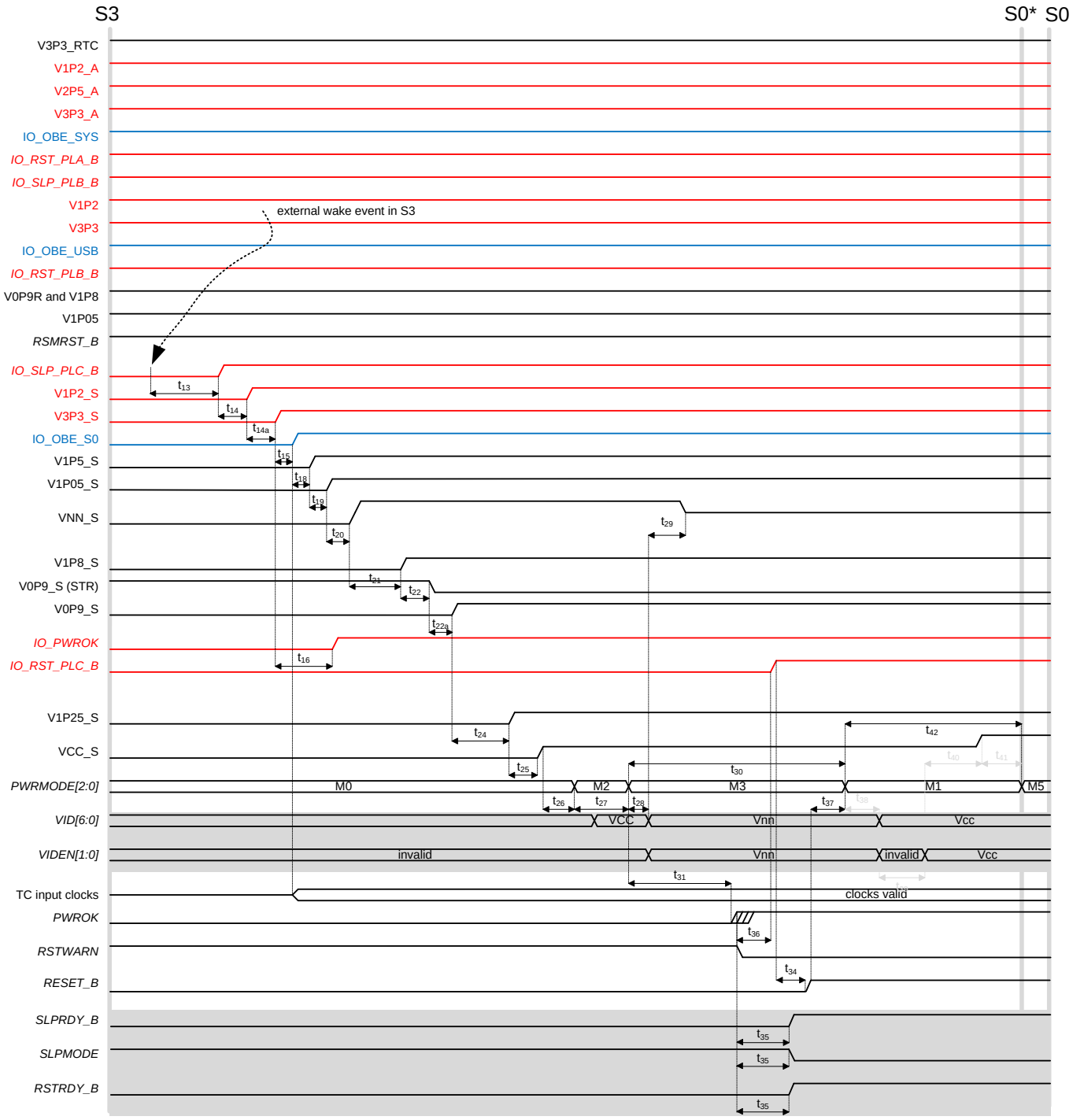


Figure 33 : S3 to S0 timing OKI MP IOH external

7.6.4.6 Cold Reset OKI Semiconductor MP IO-Hub

During a cold reset Atom™ E6xx processor and the IO-Hub will undergo a power cycling. The timings for the S0 to S4/5 sequence are basically the same as for the sequence described in Section chapter 7.6.4.3. Once in S4/5 the cold reset period will be 4 seconds before the S4/5 to S0 sequence starts in the same way as defined in Chapter 7.6.3.3.

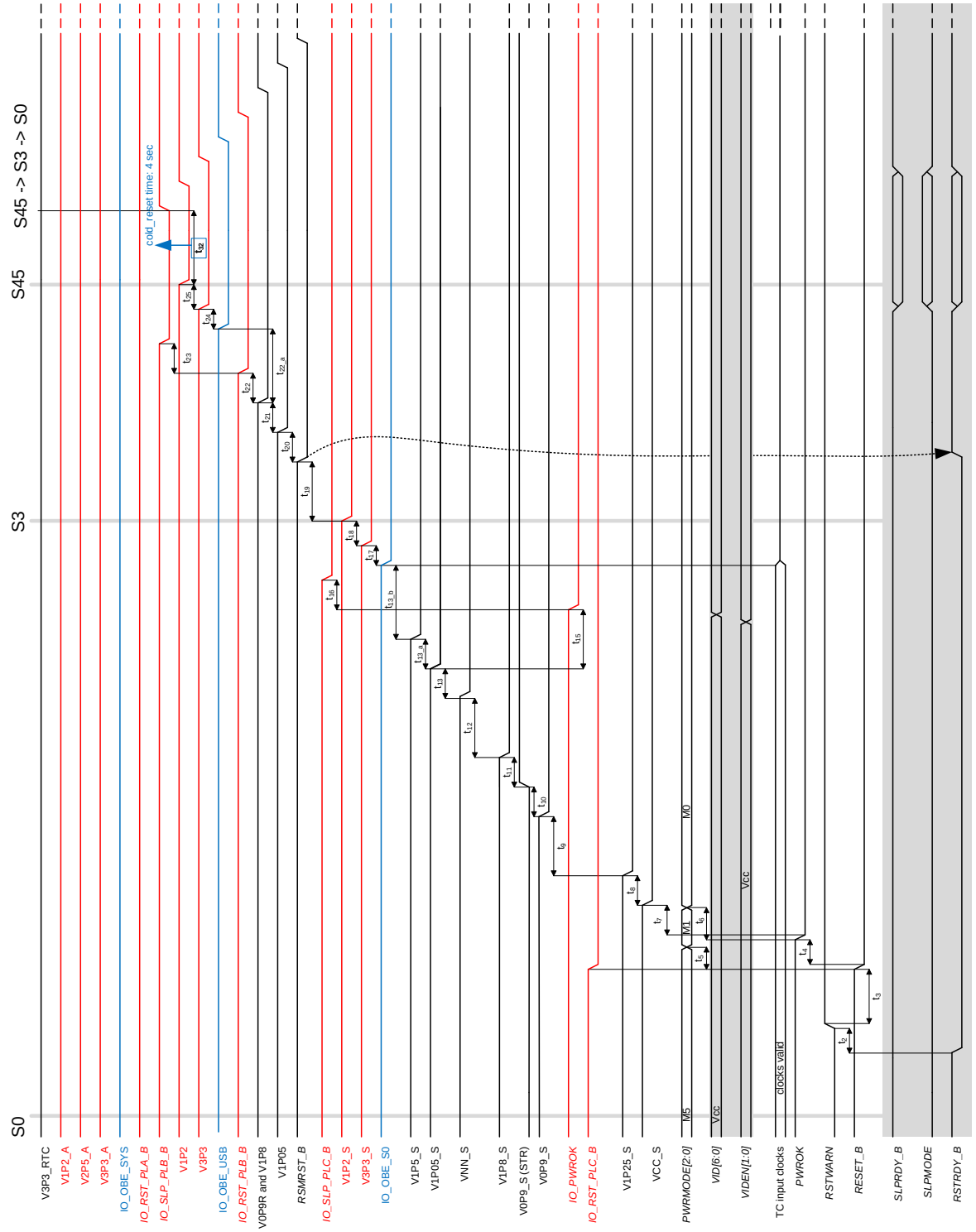


Figure 34 : Cold reset OKI MP IOH

7.6.4.7 Warm Reset OKI Semiconductor MP IO-Hub (external & internal)

During a warm reset issued by E6xx processor the reset signals of the OKI Semiconductor MP IO-Hub also get asserted for resetting the internal IO-Hub logic. The following diagram shows the warm reset sequence for OKI Semiconductor MP IO-Hub and E6xx processor. The external warm reset is triggered by the assertion of RESET_IN_B instead of the processor handshake signals. If such RESET_IN_B signal is asserted DA6011 will assert RSTWARN and after the assertion of RSTRDY_B it continues in the same way as during internal warm reset.

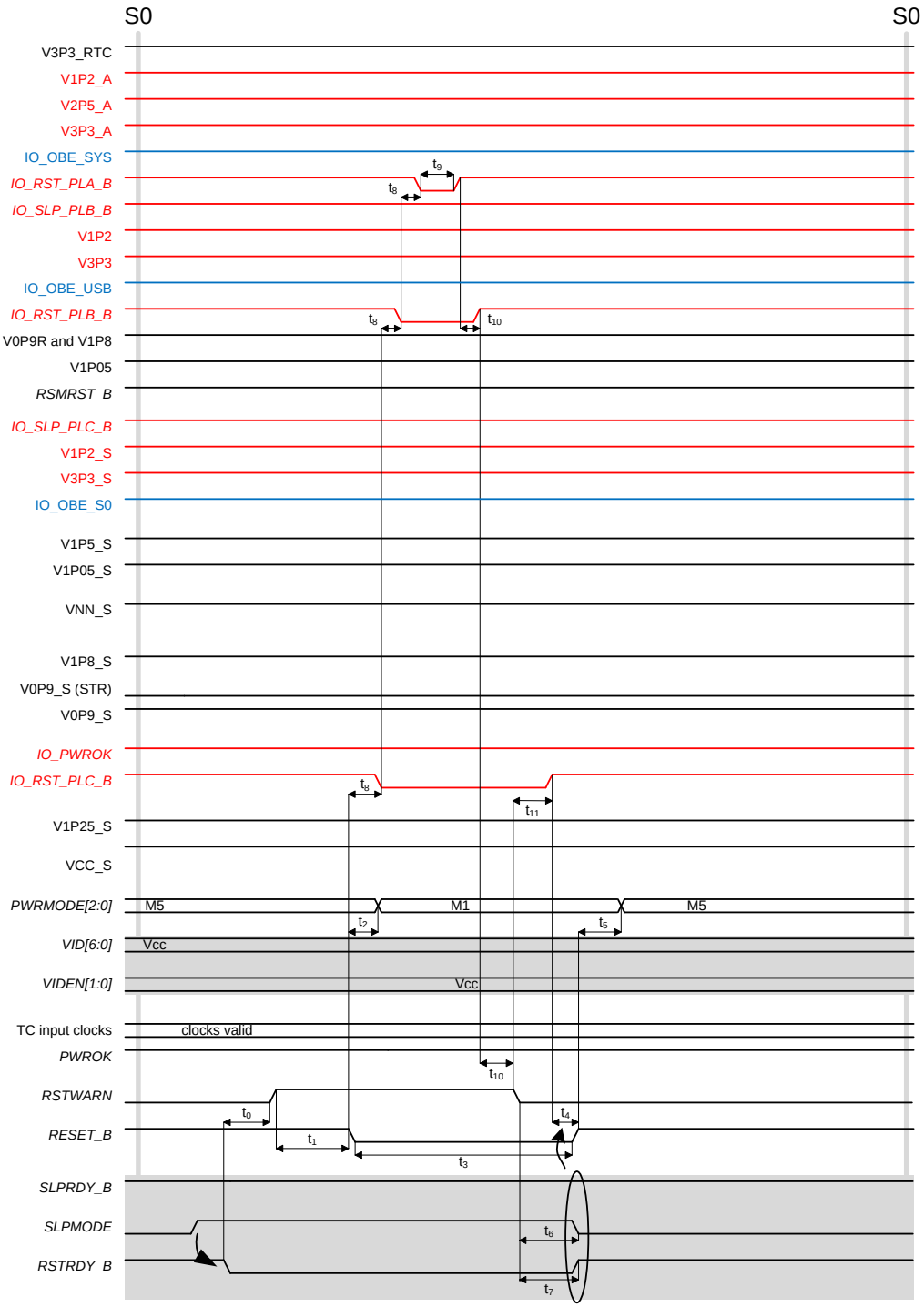


Figure 35 : Warm reset OKI MP IOH internal

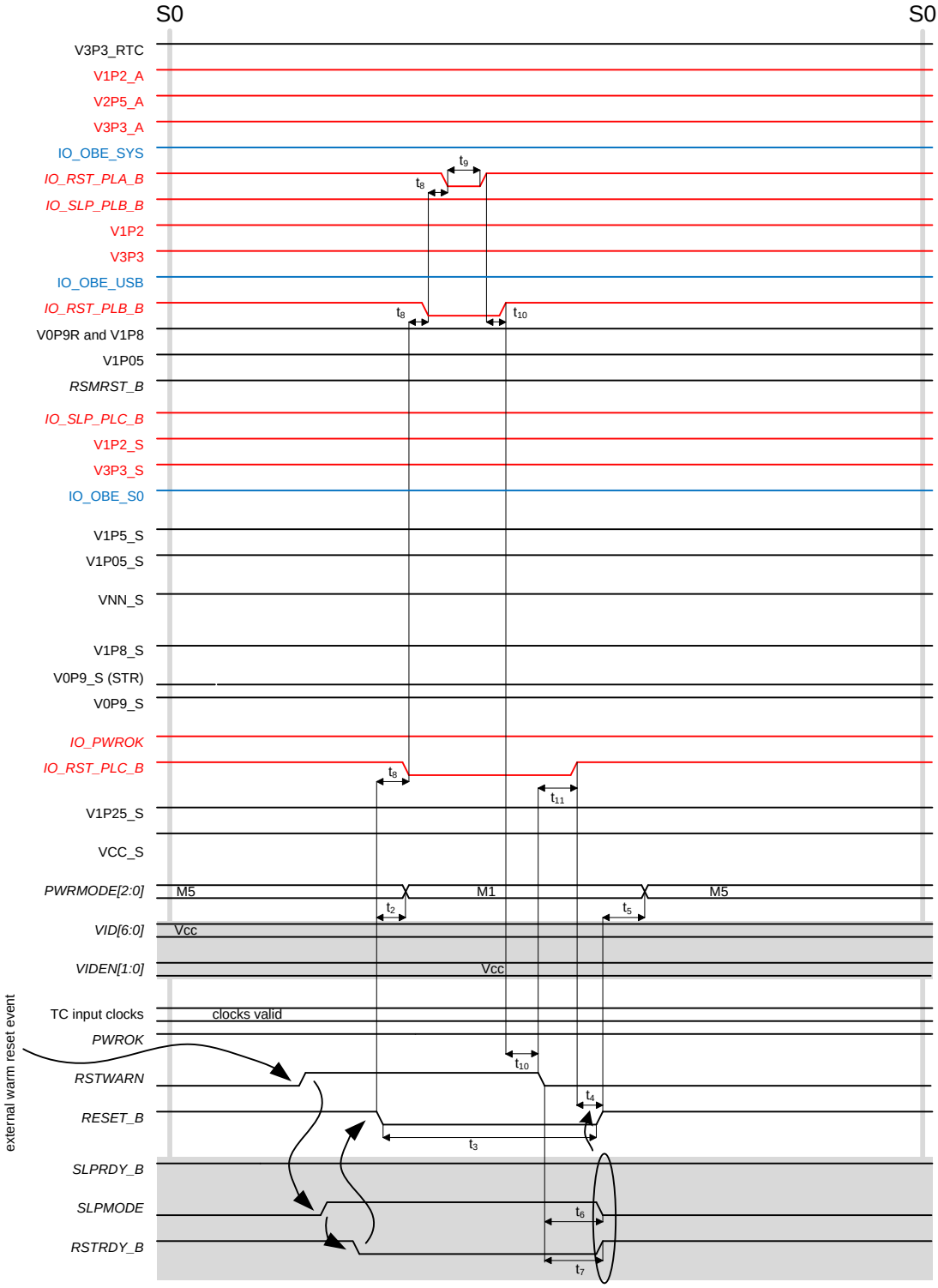


Figure 36 : Warm reset OKI MP IOH external

The delays for the warm reset sequence are given in the table below. Note: Intel to provide validated numbers. Therefore, the given timings of the IO-Hub are subject to change. In any case, the reset assertion de-assertion of the OKI Semiconductor MP IO-Hub will always be done prior to the release of the RESET_B of E6xx processor.

Label	Description	Min	Max	Unit	Implementation
t_0	RSTRDY_B assertion to RSTWARN assertion	0	>0	us	1
t_1	RSTWARN assertion to RESET_B assertion	-	>0	us	10
t_2	RESET_B assertion to M1 entry	0	-	us	0
t_3	RESET_B assertion period	1000	-	us	1654
t_4	de-assertion of IO_RST_PLC_B to de-assertion of RESET_B			us	0.5
t_5	RESET_B de-assertion to M5 entry	50	-	us	100
t_6	RSTWARN de-assertion to SLPMODE de-assertion	-	100	us	---
t_7	RSTWARN de-assertion to RSTRDY_B de-assertion	-	100	us	---
t_8	RESET_B assertion to IO_RST_PLC_B assertion IO_RST_PLC_B assertion to IO_RST_PLB_B assertion IO_RST_PLB_B assertion to IO_RST_PLA_B assertion			us	100
t_9	IO_RST_PLA_B assertion period			us	1000
t_{10}	IO_RST_PLA_B de-assertion to IO_RST_PLB_B de-assertion IO_RST_PLB_B de-assertion to RSTWARN de-assertion			us	100
t_{11}	de-assertion of RSTWARN to de-assertion of IO_RST_PLC_B. Since t4 is only 0.5 us t11 is set in such a way that the minimum Intel timing of 150us in between the assertion of RSTWARN and the de-assertion of RESET_B is fulfilled.			us	150

Table 45: Warm reset delays

7.6.4.8 Catastrophic Shutdown OKI Semiconductor MP IO-Hub

A catastrophic shutdown can be issued by E6xx processor at any time, asynchronously to all other events occurring on the system. In this case all supplies except the RTC supply (V3P3_RTC) are being disabled. All timings will be set to their minimum value. The maximum time for the catastrophic shut down sequence will not exceed 500ms.

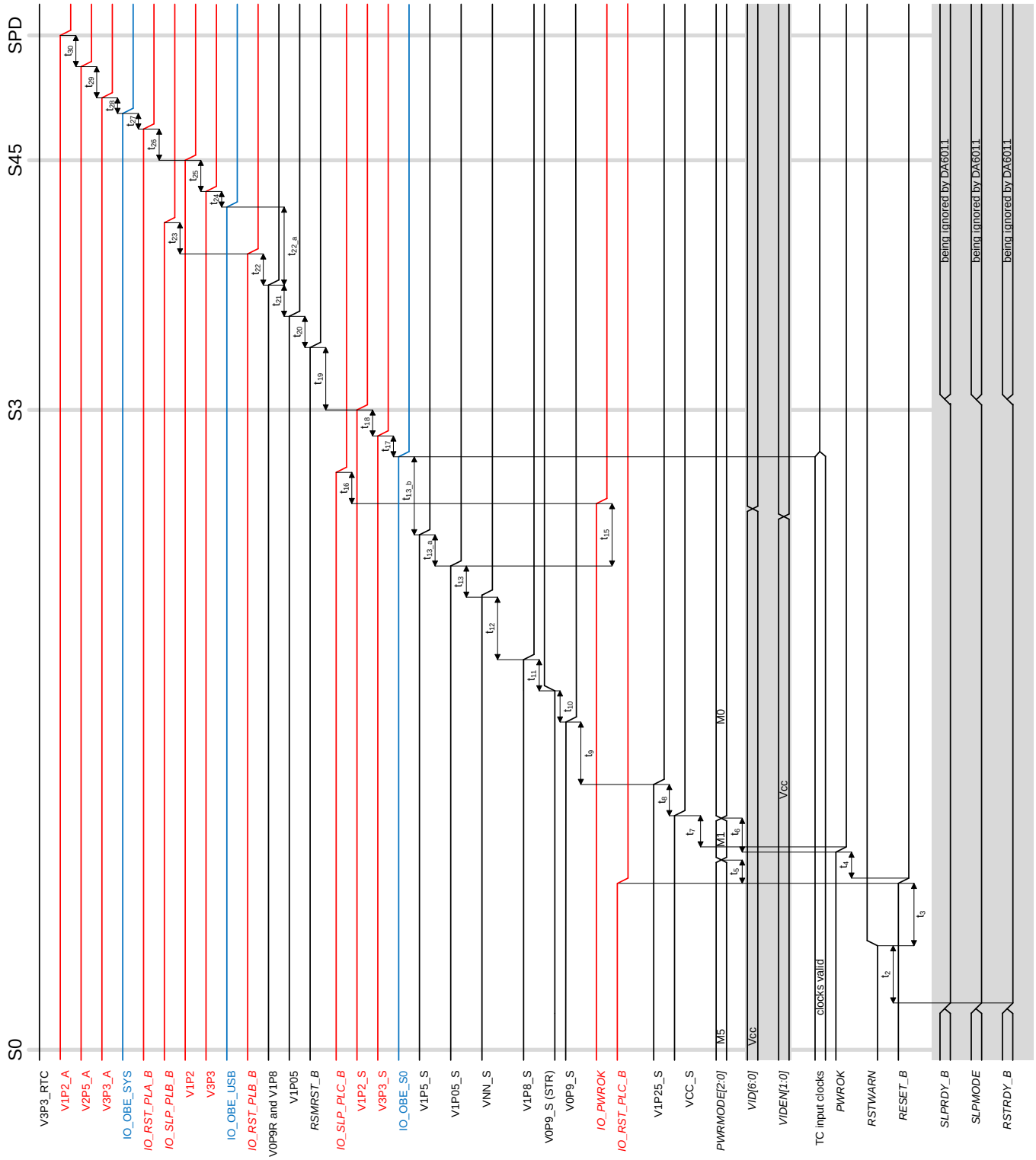


Figure 37 : Catastrophic shutdown OKI MP IOH

8 DA6011 SMBus INTERFACE

DA6011 features a SMBus v1.0-compliant[2] interface which can be used by external devices to access selected registers in the register bank. The SMBus acts as slave only and hence gets its clock from the external master module. The following signals are defined:

- SMBCLK: clock provided by master device
- SMBDAT: serial data

The frequency of the SMBus is defined to be between 10 kHz and 100 kHz. The SMBus will operate at V3P3_RTC voltage levels. The 7-bit slave address is 0x69, resulting in the 8-bit write-address 0xD2 and the read address 0xD3. DA6011 will return the all-zero byte if the provided address points to an unspecified SMBus address.

The SMBus slave features configuration of the DA6011 system parameters. Furthermore, it can be used for reading out status information.

The SMBus implementation of DA6011 does not implement clock stretching on the slave side and therefore, SMBCLK is provided as an input only. The SMBus slave will implement the low-clock period monitoring of the master clock. If the low-clock period of the master (or host) exceeds 25ms (see $T_{TIMEOUT,min}$), the SMBus slave stops driving SMBDAT and releases the data signal SMBDAT. After this the slave must be able to react on the next start condition at the latest after 35ms (see $T_{TIMEOUT,max}$).

8.1 SMBus AC specification

The figure below defines the AC characteristics of the SMBus interface; timing requirements can be found in the following table.

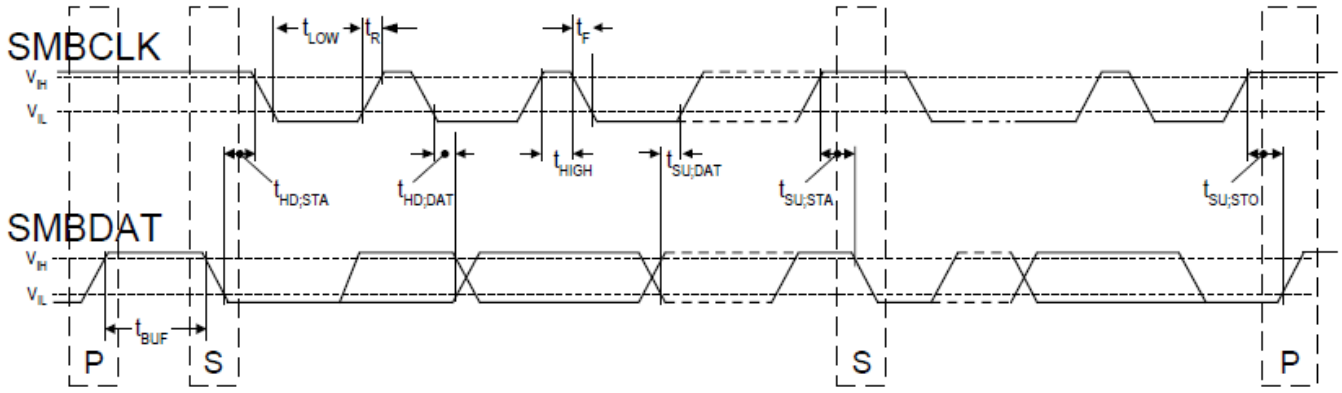


Figure 38: Timing definitions for SMBus

PARAMETER	MIN	MAX	UNIT
SMBCLK clock frequency	10	100	kHz
Data hold time $T_{HD:DAT}$	300		ns
Data setup time $T_{SU:DAT}$	250		ns
Bus free time between STOP and START condition T_{BUF}	4.7		µs

[2] Note that error correction features (PEC) and address resolution mechanisms have been specified only in version 2.0 of the SMBus. Therefore, these features will not be implemented on DA6011.

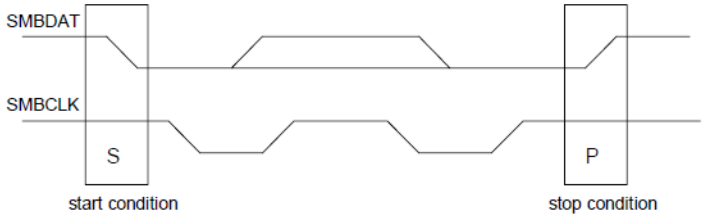
PARAMETER	MIN	MAX	UNIT
Start condition set-up time $T_{SU:STA}$	4.7		µs
Start condition hold time $T_{HD:STA}$	4.0		µs
Stop condition setup time $T_{SU:STO}$	4.0		µs
Clock low time T_{LOW}	4.7		µs
Clock high time T_{HIGH}	4.0	50	µs
Clock and DATA rise time T_F		1000	ns
Clock and DATA fall time T_R		300	ns
Timeout	25	35	ms
Cumulative clock low extend (slave device) $T_{LOW:SEXT}$		25	ms
Cumulative clock low extend (master device) $T_{LOW.MEXT}$		10	ms

Table 8-1: SMBus timings

In Table 8-1Table 8-1 the last three rows define timeouts for the SMBus, whereby the last two are timing constraints for clock stretching and hence not relevant for DA6011.

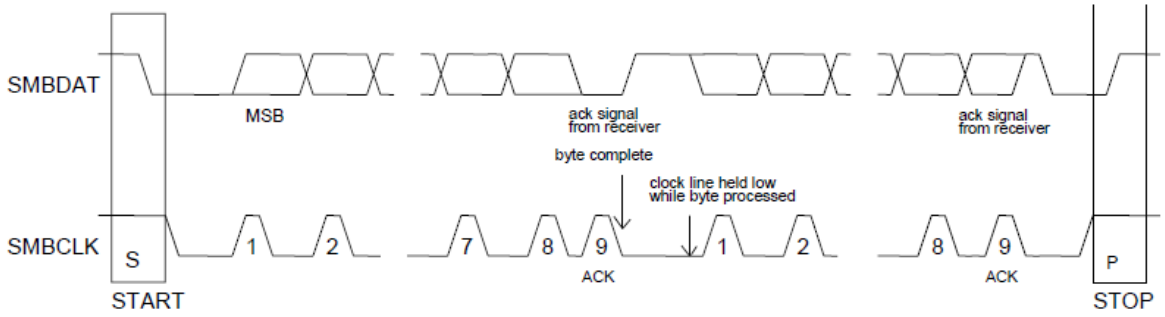
8.2 SMBus Start and Stop condition

A START condition is initiated by a high-to-low transition on the SMBDAT line while the SMBCLK is high. A STOP condition is indicated by a low-to-high transition on the SMBDAT line while the SMBCLK is in the high state; see diagram below.



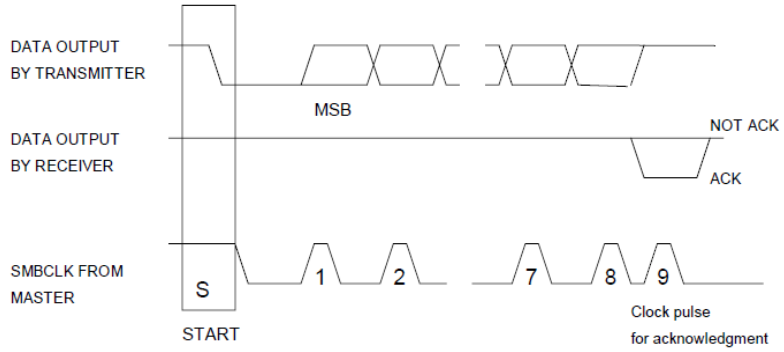
START and STOP conditions are always generated by the bus master. After a START condition the bus is considered to be busy. The bus becomes idle again after certain time following a STOP condition or after both SMBCLK and SMBDAT lines remain high for more than 50µs. This timing does not have any impact on the slave.

8.3 Data transfer on the SMBus



Every byte consists of 8 bits. Each byte transferred on the bus must be followed by an acknowledge bit. Bytes are transferred with the most significant bit (MSB) first. If a new START or STOP condition occurs within a message the bus will return to IDLE-mode.

The following diagram illustrates the acknowledge (ACK) and not acknowledge (NACK) pulses relative to the data and clock signals.



The acknowledge-related clock pulse is generated by the master. The transmitter releases the SMBDAT line during the acknowledge clock cycle. In order to acknowledge a byte, DA6011 pulls SMBDAT low during the high period of the clock pulse according to the SMBus timing information. For reading data (see Section 8.4.2) DA6011 needs to issue a not acknowledge (NACK), meaning that DA6011 does not pull SMBDAT low.

8.4 SMBus Protocol

The SMBus protocols supported by DA6011 are “Block Read” and “Block Write”. No other protocols are supported.

8.4.1 Block Write Operation

When data is written to a register in DA6011 the following sequence (see Figure 39) shall occur, where shaded fields are bits driven by the slave and white fields driven by the master.

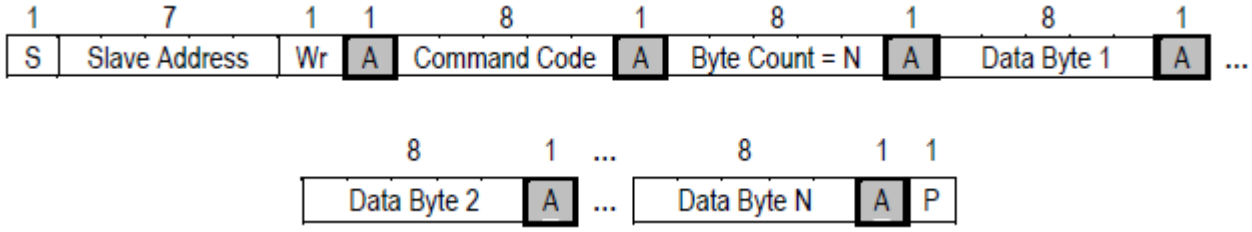


Figure 39: Block write operation

Note that Command Code refers to the address in which the data will be stored. Byte Count will be the number of bytes to be stored in the DA6011 registers; Byte count is constrained by $1 \leq N \leq 32$. DA6011 will perform an auto-increment for the address, i.e. Command Code, after receiving each byte until the last byte has been received. This allows writing several bytes without resending the address.

8.4.2 Block Read Operation

When data is read from a register in DA6011 the following sequence (see) shall occur, where shaded fields are bits driven by the slave and white fields driven by the master. Furthermore, the “1” beneath the last acknowledge of the master (A) stands for a not acknowledge.

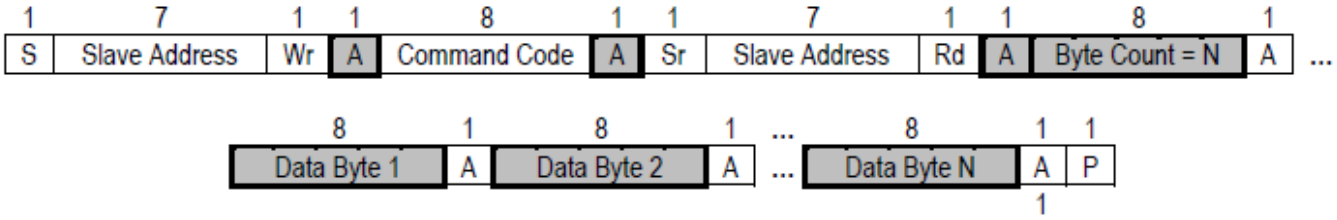


Figure 40: Block read operation

8.5 Register Map

Addr	Function	7	6	5	4	3	2	1	0
PLL									
0xBC	XTALCTRL2	Reserved							BYPASSEN
0xBE	PLLSSCTRL	Reserved			SPREAD1[2:0]			Reserved	PLL1SSEN
System									
0xD6	STATUS	IRQ	Reserved		PWRBTEVTS0	PWRBTEVTS3	OVERTEMP	VBATOVER	VBATUNDER
0xD7	IRQCLR	Reserved			PWRBTEVTS0	PWRBTEVTS3	OVERTEMP	VBATOVER	VBATUNDER
0xD8	IRQMASK	Reserved			PWRBTEVTS0	PWRBTEVTS3	OVERTEMP	VBATOVER	VBATUNDER
GPADC									
0xE1	AUTOCTRL	Reserved		AD2ISREN[1:0]		Reserved	AD3EN	AD2EN	VSUPEN
0xE2	MANCTRL	CHSEL[1:0]		Reserved	MANRUN	Reserved			
0xE3	ADCIN23DB	Reserved					AD3DBEN	AD2DBEN	Reserved
0xE4	ADCSTAT	Reserved			MANEOC	ADCIN3TH	ADCIN2TH	TJUNCOVER	VSUPUNDER
0xE5	ADCIRQCLR	Reserved			MANEOC	ADCIN3TH	ADCIN2TH	TJUNCOVER	VSUPUNDER
0xE6	ADCIRQMASK	Reserved			MANEOC	ADCIN3TH	ADCIN2TH	TJUNCOVER	VSUPUNDER
0xE7	MANRESLB	MANRESLB[7:0]							
0xE8	MANRESHB	Reserved						MANRESHB[1:0]	
0xE9	VSUPARES	VSUPARES[7:0]							
0xEA	TJUNCARES	TJUNCARES[7:0]							
0xEB	TJUNCOFFSET	TJUNCOFFSET[7:0]							
0xEC	ADCIN2ARES	ADCIN2ARES[7:0]							
0xED	ADCIN2HTH	ADCIN2HTH[7:0]							
0xEE	ADCIN2LTH	ADCIN2LTH[7:0]							
0xEF	ADCIN3ARES	ADCIN3ARES[7:0]							

Addr	Function	7	6	5	4	3	2	1	0
0xF0	ADCIN3HTH	ADCIN3HTH[7:0]							
0xF1	ADCIN3LTH	ADCIN3LTH[7:0]							
Version									
0xF2	CHIPID	NRC[3:0]				MRC[3:0]			

Table 2: DA6011 register map

8.5.1 XTALCTRL2

Register Name	XTALCTRL2			Address	0xBC	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R	R	R	R	R	R/W	R/W
Reserved							BYPASSEN
EXTREFEN	**0** 1	Enable external reference. External clock can be provided via X2 pin					

8.5.2 PLLSSCTRL

Register Name	PLLSSCTRL			Address	0xBE	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R	R	R	R	R	R/W	R/W
Reserved			SPREAD1[2:0]			Reserved	PLL1SSEN
PLL1SSEN	**0** 1	Enables spread spectrum feature of PLL1					
SPREAD1[2:0]	**000** 001 010 011 100 101 110 111	Down spread 0.3% Down spread 1% Down spread 1.5% Down spread 2% Centre spread 0.3% Centre spread 1% Centre spread 1.5% Centre spread 2%					

8.5.3 STATUS

Register Name	STATUS			Address	0xD6	Read	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R	R	R
IRQ	reserved		PWRPBT EVTS0	PWRPBT EVTS3	OVER TEMP	VBAT OVER	VBAT UNDER

VBATUNDER	**0** 1	Supply voltage drops below 4V
VBATOVER	**0** 1	Supply voltage above 5.5V
OVERTEMP	**0** 1	Over temperature has been detected
PWRPBTEVTS3	**0** 1	Power Button short pulse has been detected in S3 state
PWRPBTEVTS0	**0** 1	Power Button short pulse has been detected in S0 state
IRQ	**0** 1	System or GPADC interrupt is asserted

8.5.4 IRQCLR

Register Name	IRQCLR			Address	0xD7	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R	R	R	R/W	R/W	R/W	R/W
reserved			PWRBPT EVTS0	PWRBPT EVTS3	OVER TEMP	VBAT OVER	VBAT UNDER

VBATUNDER	**0** 1	Write clears this bit and de-asserts it by hardware
VBATOVER	**0** 1	Write clears this bit and de-asserts it by hardware
OVERTEMP	**0** 1	Write clears this bit and de-asserts it by hardware
PWRBPTEVTS3	**0** 1	Write clears this bit and de-asserts it by hardware
PWRBPTEVTS0	**0** 1	Write clears this bit and de-asserts it by hardware

8.5.5 IRQMASK

Register Name	IRQMASK			Address	0xD8	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R	R	R	R/W	R/W	R/W	R/W
reserved			PWRBPT EVTS0	PWRBPT EVTS3	OVER TEMP	VBAT OVER	VBAT UNDER

VBATUNDER	**0** 1	VBATUNDER IRQ is unmasked VBATUNDER IRQ is masked

VBATOVER	**0** 1	VBATOVER IRQ is unmasked VBATOVER IRQ is masked
OVERTEMP	**0** 1	OVERTEMP IRQ is unmasked OVERTEMP IRQ is masked
PWRBPTEVTS3	**0** 1	PWRBPTEVT IRQ is unmasked PWRBPTEVT IRQ is masked
PWRBPTEVTS0	**0** 1	PWRBPTEVT IRQ is unmasked PWRBPTEVT IRQ is masked

8.5.6 AUTOCTRL

Register Name	**AUTOCTRL**			Address	**0xE1**	Read/Write	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R/W	R/W	R/W	R/W
reserved		AD2ISRCEN[1:0]		reserved	AD3EN	AD2EN	VSUPEN

VSUPEN	**0** 1	Enable automatic measurement of VSUP
AD2EN	**0** 1	Enable automatic measurement of AD2
AD3EN	**0** 1	Enable automatic measurement of AD3
AD2ISRCEN[1:0]	**00** 01 10 11	Current source is disabled Current source is permanently enabled Current source is only enabled while AD2 is measured Current source is disabled

8.5.7 MANCTRL

Register Name	**MANCTRL**			Address	**0xE2**	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R	R/W	R	R	R	R
CHSEL		reserved	MANRUN	reserved			

MANRUN	**0** 1	Starts manual conversion. Bit is cleared when conversion is completed
CHSEL	**00** 01 10 11	VSUP channel TJUNC ADC_IN2 channel ADC_IN3 channel

8.5.8 ADCIN23DB

Register Name	ADCIN23DB			Address	0xE3	Read/Write	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R/W	R/W	R/W
reserved					AD3DBEN	AD2DBEN	Reserved

AD2DBEN	**0** 1	No debounce on ADC_IN channel 2 Result need to exceed threshold 3 times
AD3DBEN	**0** 1	No debounce on ADC_IN channel 3 Result need to exceed threshold 3 times

8.5.9 ADCSTAT

Register Name	ADCSTAT			Address	0xE4	Read/Write	
				Reset Value	0x00		
MSB							LSB
R	R	R	R/W	R/W	R/W	R/W	R/W
reserved			MANEOC	ADCIN3TH	ADCIN2TH	TJUNC OVER	VSUP UNDER

VSUPUNDER	**0** 1	VSUP measurements below threshold during 3 consecutive measurements. Auto measurement stops, bit needs to be cleared
TJUNCOVER	**0** 1	TJUNC measurement above threshold during 3 consecutive measurements. Auto measurement stops, bit needs to be cleared
ADCIN2TH	**0** 1	ADC_IN channel 2 measurement over or under thresholds. Auto measurement stops, bit needs to be cleared
ADCIN3TH	**0** 1	ADC_IN channel 3 measurement over or under thresholds. Auto measurement stops, bit needs to be cleared
MANEOC	**0** 1	Endo of ADC conversion for manual measurement reached. Bit needs to be cleared to start new conversion

8.5.10 ADCIRQCLR

Register Name	ADCIRQCLR			Address	0xE5	Read/Write	
				Reset Value	0x00		
MSB							LSB
R	R	R	R/W	R/W	R/W	R/W	R/W
reserved			MANEOC	ADCIN3TH	ADCIN2TH	TJUNC OVER	VSUP UNDER

VSUPUNDER	**0** 1	Write “1” to clear IRQ bit of ADCSTAT register
TJUNCOVER	**0** 1	Write “1” to clear IRQ bit of ADCSTAT register
ADCIN2TH	**0** 1	Write “1” to clear IRQ bit of ADCSTAT register
ADCIN3TH	**0** 1	Write “1” to clear IRQ bit of ADCSTAT register
MANEOC	**0** 1	Write “1” to clear IRQ bit of ADCSTAT register

8.5.11 ADCIRQMASK

Register Name	ADCIRQMASK			Address	0xE6	Read/Write	
				Reset Value	0x00		
MSB							LSB
R	R	R	R/W	R/W	R/W	R/W	R/W
reserved			MANEOC	ADCIN3TH	ADCIN2TH	TJUNC OVER	VSUP UNDER

VSUPUNDER	**0** 1	Mask VSUPUNDER IRQ
TJUNCOVER	**0** 1	Mask TJUNCOVER IRQ
ADCIN2TH	**0** 1	Mask ADCIN2TH IRQ
ADCIN3TH	**0** 1	Mask ADCIN3TH IRQ
MANEOC	**0** 1	Mask MANEOC IRQ

8.5.12 MANRESLB

Register Name	MANRESLB			Address	0xE7	Read	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R	R	R
MANRESLB[7:0]							

MANRESLB[7:0]	**0..255**	Low part of the 10-bit manual conversion result

8.5.13 MANRESHB

Register Name	MANRESHB			Address	0xE8	Read	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R	R	R
Reserved						MANRESHB[1:0]	
MANRESHB[7:0]		**0..3**	High part of the 10-bit manual conversion result				

8.5.14 VSUPARES

Register Name	VSUPARES			Address	0xE9	Read	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R	R	R
VSUPARES[7:0]							
VSUPARES[7:0]		**0..255**	Result of the automatic VSUP conversion				

8.5.15 TJUNCARES

Register Name	TJUNCARES			Address	0xEA	Read	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R	R	R
TJUNCARES[7:0]							
TJUNCARES[7:0]		**0..255**	Result of the automatic junction temperature measurement				

8.5.16 TJUNCOFFSET

Register Name	TJUNCOFFSET			Address	0xEB	Read	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R	R	R
TJUNCOFFSET[7:0]							
TJUNCOFFSET[7:0]		**0..255**	TJUNC calibration offset				

8.5.17 ADCIN2ARES

Register Name	ADCIN2ARES			Address	0xEC	Read	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R	R	R
ADCIN2ARES[7:0]							
ADCIN2ARES[7:0]		**0..255**	Result of the automatic ADCIN2 measurement				

8.5.18 ADCIN2HTH

Register Name	ADCIN2HTH			Address	0xED	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADCIN2HTH[7:0]							
ADCIN2HTH[7:0]		**0..255**	High level threshold for ADC_IN channel 2				

8.5.19 ADCIN2LTH

Register Name	ADCIN2LTH			Address	0xEE	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADCIN2LTH[7:0]							
ADCIN2LTH[7:0]		**0..255**	Low level threshold for ADC_IN channel 2				

8.5.20 ADCIN3ARES

Register Name	ADCIN3ARES			Address	0xEF	Read	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R	R	R
ADCIN3ARES[7:0]							
ADCIN3ARES[7:0]		**0..255**	Result of the automatic ADCIN3 measurement				

8.5.21 ADCIN3HTH

Register Name	ADCIN3HTH			Address	0xF0	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADCIN3HTH[7:0]							
ADCIN3HTH[7:0]		**0..255**	High level threshold for ADC_IN channel 3				

8.5.22 ADCIN3LTH

Register Name	ADCIN2LTH			Address	0xF1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ADCIN3LTH[7:0]							
ADCIN3LTH[7:0]		**0..255**	Low level threshold for ADC_IN channel 3				

8.5.23 CHIPID

Register Name	CHIPID			Address	0xF2	Read	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R	R	R
NRC[3:0]				MRC[3:0]			

MRC[3:0]	0..15	Chip ID minor revision code (metal mask revision)
NRC[3:0]	0..15	Chip ID new release code

9 JTAG Interface

Signal Name	Type	Description
TCK	DI	JTAG Test Clock: TCK is a clock input used to drive Test Access Port (TAP) state machine during test and debugging.
TDI	DI	JTAG Test Data In: TDI is used to serially shift data and instructions into the TAP
TDO	DO	JTAG Test Data Out: TDI is used to serially shift data out of the device
TMS	DI	Test Mode Select: this signal is used to control the state of the TAP controller

10 DA6011 PACKAGE DETAILS

10.1 Pin Description, Pin out

Below is a pin description list for the DA6011. In the type column the following abbreviations have been used

- PS, VSS Power Supply
- DI, DO, DIO Digital Input, Output, Input/Output
- AI, AO, AIO Analog Input, Output, Input/Output
- OD Open-Drain Output

10.1.1 Ball order

Ball	Ball Name	Type	Pin Description
A1	VSS_1P8	VSS	Ground of Buck_V1P8 output driver
A2	VHS_1P8	AO	provide the gate drive for the external PMOS of Buck_V1P8
A3	VLS_1P8	AO	Provide the gate drive for the external NMOS of Buck_V1P8
A4	VSUP_1P8	PS	Powers the Buck_V1P8 output driver
A5	VSS_C	VSS	Ground the Core output driver
A6	VHS_VCC	AO	provide the gate drive for the external PMOS of Buck_Core
A7	VLS_VCC	AO	Provide the gate drive for the external NMOS of Buck_Core
A8	VSUP_C	PS	Powers the Core output driver
A9	VSS_1P05	VSS	Ground the Buck_B1P05 output driver
A10	VHS_1P05	AO	provide the gate drive for the external PMOS of Buck_V1P05
A11	VLS_1P05	AO	Provide the gate drive for the external NMOS of Buck_V1P05
A12	VSUP_1P05	PS	Powers the Buck_V1P05 output driver
A13	IREF	AIO	Bias current reference node, connect 50kΩ ±1% to GND
B1	V1P8_S	AIO	V1P8_S switch output
B2	V1P8	AIO	Buck_V1P8 sense line, voltage feedback node
B3	CS_1P8	AIO	Current sense of Buck_V1P8
B4	VCC_S	AIO	Buck_Core sense line, voltage feedback node
B5	CS_VCC	AIO	Current sense of Buck_Core
B6	VCC_SENSE	AIO	Power sense of Core CPU
B7	VCC_VSS_SENSE	AIO	Ground sense of Core CPU
B8	CS_1P05	AIO	Current sense of Buck_V1P05
B9	V1P05_S	AIO	Buck_V1P05_S sense line, voltage feedback node
B10	VID[0]	DI	VCC,VNN output voltage control bit[0]
B11	VID[1]	DI	VCC,VNN output voltage control bit[1]
B12	VREF	AIO	Reference voltage connection
B13	V3P3_S	AIO	V3P3_S switch output
C1	V1P8_IN	AIO	V1P8 Switch input
C2	VIDEN[0]	DI	VIDEN[0] pin connection
C3	VIDEN[1]	DI	VIDEN[1] pin connection
C4	IO_RST_PLC_B	DO	IO_RST_PLC_B pin connection
C5	THRMTRIP_B	OD	THRMTRIP_B pin connection
C6	ADC_IN_3	AIO	ADC_IN_3 pin connection
C7	ADC_IN_2	AIO	ADC_IN_2 pin connection
C8	TEST	DI	TEST pin connection, triggers DA6011 test mode

C9	RESET_IN_B	DI	RESET_IN_B pin connection
C10	VID[3]	DI	VCC,VNN output voltage control bit[3]
C11	VID[2]	DI	VCC,VNN output voltage control bit[2]
C12	VID[5]	DI	VCC,VNN output voltage control bit[5]
C13	V3P3_IN	AIO	V3P3 Switch input
D1	V0P9_S	AIO	LDO_V0P9 output node
D2	PROCHOT_B	OD	PROCHOT_B pin connection
D3	IRQ_B	OD	IRQ_B pin connection
D4	IO_SLP_PLB_B	DO	IO_SLP_PLB_B pin connection
D5	IO_RST_PLB_B	DO	IO_RST_PLB_B pin connection
D6	SLPMODE	DI	SLPMODE pin connection, TC Handshake signal
D7	VSS_QUIET	VSS	Ground connection reference ground
D8	SMBCLK	DI	SMBus system clock
D9	VID[4]	DI	VCC,VNN output voltage control bit[4]
D10	VID[6]	DI	VCC,VNN output voltage control bit[6]
D11	VLP	AIO	LDO_VLP output node
D12	VSUP2	PS	Powers the pass device of VINT and VLP regulator
D13	VINT	AIO	LDO_VINT output node
E1	VDD_V0P9	AIO	Powers LDO_V0P9
E2	V0P9R	AIO	Memory reference voltage
E3	V1P25_S	AIO	LDO_V1P25_S output node
E4	VDDC_V1P8	AIO	Powers the controller of V1P5_S, V1P25_S and V1P05 LDOs
E5	VSS	VSS	Thermal VSS connection to ground plane of PCB
E6	VSS	VSS	Thermal VSS connection to ground plane of PCB
E7	VSS	VSS	Thermal VSS connection to ground plane of PCB
E8	VSS	VSS	Thermal VSS connection to ground plane of PCB
E9	VSS	VSS	Thermal VSS connection to ground plane of PCB
E10	V3P3_RTC	AIO	LDO_V3P3_RTC output node
E11	V3P3_A	AIO	LDO_V3P3_A output node
E12	VSUP1	PS	Powers all LDO cores
E13	VSUP_3P3	PS	Powers the Buck_V3P3 output driver
F1	VDD_V1P8	AIO	Powers the pass devices of V1P5_S, V1P25_S and V1P05 LDOs
F2	V1P05	AIO	LDO_V1P05 output node
F3	V1P5_S	AIO	LDO_V01P5_S output node
F4	VDDC_VUNI	AIO	Power the controller of VUNI LDO
F5	VSS	VSS	Thermal VSS connection to ground plane of PCB
F6	VSS	VSS	Thermal VSS connection to ground plane of PCB
F7	VSS	VSS	Thermal VSS connection to ground plane of PCB
F8	VSS	VSS	Thermal VSS connection to ground plane of PCB
F9	VSS	VSS	Thermal VSS connection to ground plane of PCB
F10	V3P3	AIO	Buck_V3P3 sense line, voltage feedback node
F11	V2P5_A	AIO	LDO_V2P5_A output node
F12	VSUP3	PS	Powers the pass device of RTC,V3P3_A, V2P5_A regulator
F13	VLX_3P3	AIO	Switching node of Buck_V3P3

G1	VDD_VUNI	AIO	Powers the pass device of VUNI LDO
G2	VUNI	AIO	LDO_VUNI output node
G3	VNN_VSS_SENSE	AIO	Ground sense of Graphic CPU
G4	VNN_SENSE	AIO	Power sense of Graphic CPU
G5	VSS	VSS	Thermal VSS connection to ground plane of PCB
G6	VSS	VSS	Thermal VSS connection to ground plane of PCB
G7	VSS	VSS	Thermal VSS connection to ground plane of PCB
G8	VSS	VSS	Thermal VSS connection to ground plane of PCB
G9	VSS	VSS	Thermal VSS connection to ground plane of PCB
G10	SMBDAT	DIO	SMBus system data
G11	V1P2	AIO	V1P2 switch output
G12	V1P2_IN	AIO	V1P2 Switch input
G13	VSS_3P3	VSS	Ground of Buck_V3P3 output driver
H1	VSUP_G	PS	Powers the Graphic output driver
H2	IO_PWROK	DO	IO_PWROK pin connection
H3	RSTWARN	DO	RSTWARN pin connection
H4	IO_RST_PLA_B	DO	IO_RST_PLA_B pin connection
H5	VSS	VSS	Thermal VSS connection to ground plane of PCB
H6	VSS	VSS	Thermal VSS connection to ground plane of PCB
H7	VSS	VSS	Thermal VSS connection to ground plane of PCB
H8	VSS	VSS	Thermal VSS connection to ground plane of PCB
H9	VSS	VSS	Thermal VSS connection to ground plane of PCB
H10	SYS	DO	SYS clock pin connection
H11	SLPRDY_B	DI	SLPRDY_B pin connection, E6XX Handshake signal
H12	V1P2_A	AIO	Buck_V1P2_A sense line, voltage feedback node
H13	VSUP_1P2	PS	Powers the Buck_V1P2 output driver
J1	VLX_VNN	AIO	switching node of Buck_Graphic
J2	PWRMODE[1]	DO	PWRMODE[1] pin connection
J3	PWRMODE[0]	DO	PWRMODE[0] pin connection
J4	IO_PWROK_EN	DI	IO_PWROK_EN multifunctional pin
J5	VSS	VSS	Thermal VSS connection to ground plane of PCB
J6	VSS	VSS	Thermal VSS connection to ground plane of PCB
J7	VSS	VSS	Thermal VSS connection to ground plane of PCB
J8	VSS	VSS	Thermal VSS connection to ground plane of PCB
J9	VSS	VSS	Thermal VSS connection to ground plane of PCB
J10	VCCIO_SYS	AIO	Powers the SYS clock driver
J11	PWRBTN_B	DI	PWRBTN_B pin connection
J12	TDO	DI	TDO pin connection JTAG
J13	VLX_1P2	AIO	Switching node of Buck_V1P2
K1	VSS_G	VSS	Ground of Buck_Graphic output driver
K2	TDI	VSS	TDI pin connection JTAG
K3	RSMRST_B	DO	RSMRST_B pin connection
K4	PWRMODE[2]	DO	PWRMODE[2] pin connection
K5	VSS_PLL1	VSS	Ground connection for PLL1
K6	VCCIO_PLL23	AIO	Powers the PLL23 clock driver

K7	VSS_PLL2	VSS	Ground connection for PLL2
K8	VSSIO_REF	VSS	Ground connection for REF clock driver
K9	VCCIO_REF	AIO	Powers the REF clock driver
K10	MCLK/ETH	DO	MCLK/ETH clock pin connection
K11	PWROK	DO	PWROK pin connection
K12	RSTRDY_B	DI	RSTRDY_B pin connection, E6XX handshake signal
K13	VSS_1P2	VSS	Ground of Buck_V1P2 output driver
L1	TCLK	DI	TCLK pin connection JTAG
L2	TMS	DI	TMS pin connection JTAG
L3	VSSIO_PLL1	VSS	Ground connection for PLL1 clock driver
L4	VCCIO_PLL1	AIO	Powers the PLL1 clock driver
L5	VCC_PLL1	AIO	Powers the PLL1
L6	VCC_PLL2	AIO	Powers the PLL2
L7	VSSIO_PLL23	VSS	Ground connection for PLL23 clock driver
L8	VSS_PLL3	VSS	Ground connection for PLL3
L9	VCC_PLL3	AIO	Powers the PLL3
L10	VCC_PLL5	AIO	Powers the PLL5 Powers the REF clock driver
L11	IO_SLP_PLC_B	DO	IO_SLP_PLC_B pin connection
L12	WAKE_B	DI	WAKE_B pin connection low active
L13	CTRL_V1P8_S	DO	CTRL_V1P8_S pin connection, controls external switch to save power
M1	100MHz1_B	DO	100MHz negative output 1 pin connection
M2	100MHz2_B	DO	100MHz negative output 2 pin connection
M3	100MHz3_B	DO	100MHz negative output 3 pin connection
M4	100MHz4_B	DO	100MHz negative output 4 pin connection
M5	100MHz5_B	DO	100MHz negative output 5 pin connection
M6	100MHz6_B	DO	100MHz negative output 6 pin connection
M7	DOT_B	DO	DOT_B clock pin connection
M8	SATA_B	DO	SATA_B clock pin connection
M9	USB	DO	USB clock pin connection
M10	VSS_XTAL	VSS	Ground connection for XO
M11	VSSIO_SYS	VSS	Ground connection for SYS clock driver
M12	RESET_B	DO	RESET_B pin connection
M13	REF	DO	REF clock pin
N1	100MHz1	DO	100MHz positive output 1 pin connection
N2	100MHz2	DO	100MHz positive output 2 pin connection
N3	100MHz3	DO	100MHz positive output 3 pin connection
N4	100MHz4	DO	100MHz positive output 4 pin connection
N5	100MHz5	DO	100MHz positive output 5 pin connection
N6	100MHz6	DO	100MHz positive output 6 pin connection
N7	DOT	DO	DOT clock pin connection
N8	SATA	DO	SATA clock pin connection
N9	VSS_PLL5	VSS	Ground connection for PLL5
N10	X1	AI	X1 pin connection
N11	VCC_XTAL	AIO	Power for XO

N12	X2	AIO	X2 pin connection
N13	VDDIO	PS	IO communication supply. Connect to V3P3_RTC or V3P3_A or V3P3 depending on the application

Table 3: DA6011 Pin out, Ball order

10.1.2 Alphabetic ball name order

Ball	Ball Name	Type	Pin Description
N1	100MHz1	DO	100MHz positive output 1 pin connection
M1	100MHz1_B	DO	100MHz negative output 1 pin connection
N2	100MHz2	DO	100MHz positive output 1 pin connection
M2	100MHz2_B	DO	100MHz negative output 1 pin connection
N3	100MHz3	DO	100MHz positive output 1 pin connection
M3	100MHz3_B	DO	100MHz negative output 1 pin connection
N4	100MHz4	DO	100MHz positive output 1 pin connection
M4	100MHz4_B	DO	100MHz negative output 1 pin connection
N5	100MHz5	DO	100MHz positive output 1 pin connection
M5	100MHz5_B	DO	100MHz negative output 1 pin connection
N6	100MHz6	DO	100MHz positive output 1 pin connection
M6	100MHz6_B	DO	100MHz negative output 1 pin connection
C7	ADC_IN_2	AIO	ADC_IN_2 pin connection
C6	ADC_IN_3	AIO	ADC_IN_3 pin connection
B8	CS_1P05	AIO	Current sense of Buck_V1P05
B3	CS_1P8	AIO	Current sense of Buck_V1P8
B5	CS_VCC	AIO	Current sense of Buck_Core
L13	CTRL_V1P8_S	DO	CTRL_V1P8_S pin connection, controls external switch to save power
N7	DOT	DO	DOT clock pin connection
M7	DOT_B	DO	DOT_B clock pin connection
H2	IO_PWROK	DO	IO_PWROK pin connection
J4	IO_PWROK_EN	DI	IO_PWROK_EN multifunctional pin
H4	IO_RST_PLA_B	DO	IO_RST_PLA_B pin connection
D5	IO_RST_PLB_B	DO	IO_RST_PLB_B pin connection
C4	IO_RST_PLC_B	DO	IO_RST_PLC_B pin connection
D4	IO_SLP_PLB_B	DO	IO_SLP_PLB_B pin connection
L11	IO_SLP_PLC_B	DO	IO_SLP_PLC_B pin connection
A13	IREF	AIO	Bias current reference node, connect 50kΩ ±1% to GND
D3	IRQ_B	OD	IRQ_B pin connection
K10	MCLK/ETH	DO	MCLK/ETH clock pin connection
D2	PROCHOT_B	OD	PROCHOT_B pin connection
J11	PWRBTN_B	DI	PWRBTN_B pin connection
J3	PWRMODE[0]	DO	PWRMODE[0] pin connection
J2	PWRMODE[1]	DO	PWRMODE[1] pin connection
K4	PWRMODE[2]	DO	PWRMODE[2] pin connection
K11	PWROK	DO	PWROK pin connection
M13	REF	DO	REF clock pin

M12	RESET_B	DO	RESET_B pin connection
C9	RESET_IN_B	DI	RESET_IN_B pin connection
K3	RSMRST_B	DO	RSMRST_B pin connection
K12	RSTRDY_B	DI	RSTRDY_B pin connection, E6XX handshake signal
H3	RSTWARN	DO	RSTWARN pin connection
N8	SATA	DO	SATA clock pin connection
M8	SATA_B	DO	SATA_B clock pin connection
D6	SLPMODE	DI	SLPMODE pin connection, E6XX Handshake signal
H11	SLPRDY_B	DI	SLPRDY_B pin connection, E6XX Handshake signal
D8	SMBCLK	DI	SMBus system clock
G10	SMBDAT	DIO	SMBus system data
H10	SYS	DO	SYS clock pin connection
L1	TCLK	DI	TCLK pin connection JTAG
K2	TDI	VSS	TDI pin connection JTAG
J12	TDO	DI	TDO pin connection JTAG
C8	TEST	DI	TEST pin connection, triggers DA6011 test mode
C5	THRMTRIP_B	OD	THRMTRIP_B pin connection
L2	TMS	DI	TMS pin connection JTAG
M9	USB	DO	USB clock pin connection
D1	V0P9_S	AIO	LDO_V0P9 output node
E2	V0P9R	AIO	Memory reference voltage
F2	V1P05	AIO	LDO_V1P05 output node
B9	V1P05_S	AIO	Buck_V1P05_S sense line, voltage feedback node
G11	V1P2	AIO	V1P2 switch output
H12	V1P2_A	AIO	Buck_V1P2_A sense line, voltage feedback node
G12	V1P2_IN	AIO	V1P2 Switch input
E3	V1P25_S	AIO	LDO_V1P25_S output node
F3	V1P5_S	AIO	LDO_V01P5_S output node
B2	V1P8	AIO	Buck_V1P8 sense line, voltage feedback node
C1	V1P8_IN	AIO	V1P8 Switch input
B1	V1P8_S	AIO	V1P8_S switch output
F11	V2P5_A	AIO	LDO_V2P5_A output node
F10	V3P3	AIO	Buck_V3P3 sense line, voltage feedback node
E11	V3P3_A	AIO	LDO_V3P3_A output node
C13	V3P3_IN	AIO	V3P3 Switch input
E10	V3P3_RTC	AIO	LDO_V3P3_RTC output node
B13	V3P3_S	AIO	V3P3_S switch output
L5	VCC_PLL1	AIO	Powers the PLL1
L6	VCC_PLL2	AIO	Powers the PLL2
L9	VCC_PLL3	AIO	Powers the PLL3
L10	VCC_PLL5	AIO	Powers the PLL5 Powers the REF clock driver
B4	VCC_S	AIO	Buck_Core sense line, voltage feedback node
B6	VCC_SENSE	AIO	Power sense of Core CPU
B7	VCC_VSS_SENSE	AIO	Ground sense of Core CPU
N11	VCC_XTAL	AIO	Power for XO

L4	VCCIO_PLL1	AIO	Powers the PLL1 clock driver
K6	VCCIO_PLL23	AIO	Powers the PLL23 clock driver
K9	VCCIO_REF	AIO	Powers the REF clock driver
J10	VCCIO_SYS	AIO	Powers the SYS clock driver
F1	VDD_V1P8	AIO	Powers the pass devices of V1P5_S, V1P25_S and V1P05 LDOs
E1	VDD_V0P9	AIO	Powers LDO_V0P9
G1	VDD_VUNI	AIO	Powers the pass device of VUNI LDO
F4	VDDC_VUNI	AIO	Power the controller of VUNI LDO
E4	VDDC_V1P8	AIO	Powers the controller of V1P5_S, V1P25_S and V1P05 LDOs
N13	VDDIO	PS	IO communication supply. Connect to V3P3_RTC or V3P3_A or V3P3 depending on the application
A10	VHS_1P05	AO	provide the gate drive for the external PMOS of Buck_V1P05
A2	VHS_1P8	AO	provide the gate drive for the external PMOS of Buck_V1P8
A6	VHS_VCC	AO	provide the gate drive for the external PMOS of Buck_Core
B10	VID[0]	DI	VCC,VNN output voltage control bit[0]
B11	VID[1]	DI	VCC,VNN output voltage control bit[1]
C11	VID[2]	DI	VCC,VNN output voltage control bit[2]
C10	VID[3]	DI	VCC,VNN output voltage control bit[3]
D9	VID[4]	DI	VCC,VNN output voltage control bit[4]
C12	VID[5]	DI	VCC,VNN output voltage control bit[5]
D10	VID[6]	DI	VCC,VNN output voltage control bit[6]
C2	VIDEN[0]	DI	VIDEN[0] pin connection
C3	VIDEN[1]	DI	VIDEN[1] pin connection
D13	VINT	AIO	LDO_VINT output node
D11	VLP	AIO	LDO_VLP output node
A11	VLS_1P05	AO	Provide the gate drive for the external NMOS of Buck_V1P05
A3	VLS_1P8	AO	Provide the gate drive for the external NMOS of Buck_V1P8
A7	VLS_VCC	AO	Provide the gate drive for the external NMOS of Buck_Core
J13	VLX_1P2	AIO	Switching node of Buck_V1P2
F13	VLX_3P3	AIO	Switching node of Buck_V3P3
J1	VLX_VNN	AIO	switching node of Buck_Graphic
G4	VNN_SENSE	AIO	Power sense of Graphic CPU
G3	VNN_VSS_SENSE	AIO	Ground sense of Graphic CPU
B12	VREF	AIO	Reference voltage connection
E5	VSS	VSS	Thermal VSS connection to ground plane of PCB
E6	VSS	VSS	Thermal VSS connection to ground plane of PCB
E7	VSS	VSS	Thermal VSS connection to ground plane of PCB
E8	VSS	VSS	Thermal VSS connection to ground plane of PCB
E9	VSS	VSS	Thermal VSS connection to ground plane of PCB
F5	VSS	VSS	Thermal VSS connection to ground plane of PCB
F6	VSS	VSS	Thermal VSS connection to ground plane of PCB
F7	VSS	VSS	Thermal VSS connection to ground plane of PCB
F8	VSS	VSS	Thermal VSS connection to ground plane of PCB
F9	VSS	VSS	Thermal VSS connection to ground plane of PCB
G5	VSS	VSS	Thermal VSS connection to ground plane of PCB

G6	VSS	VSS	Thermal VSS connection to ground plane of PCB
G7	VSS	VSS	Thermal VSS connection to ground plane of PCB
G8	VSS	VSS	Thermal VSS connection to ground plane of PCB
G9	VSS	VSS	Thermal VSS connection to ground plane of PCB
H5	VSS	VSS	Thermal VSS connection to ground plane of PCB
H6	VSS	VSS	Thermal VSS connection to ground plane of PCB
H7	VSS	VSS	Thermal VSS connection to ground plane of PCB
H8	VSS	VSS	Thermal VSS connection to ground plane of PCB
H9	VSS	VSS	Thermal VSS connection to ground plane of PCB
J5	VSS	VSS	Thermal VSS connection to ground plane of PCB
J6	VSS	VSS	Thermal VSS connection to ground plane of PCB
J7	VSS	VSS	Thermal VSS connection to ground plane of PCB
J8	VSS	VSS	Thermal VSS connection to ground plane of PCB
J9	VSS	VSS	Thermal VSS connection to ground plane of PCB
A9	VSS_1P05	VSS	Ground the Buck_B1P05 output driver
K13	VSS_1P2	VSS	Ground of Buck_V1P2 output driver
A1	VSS_1P8	VSS	Ground of Buck_V1P8 output driver
G13	VSS_3P3	VSS	Ground of Buck_V3P3 output driver
A5	VSS_C	VSS	Ground the Core output driver
K1	VSS_G	VSS	Ground of Buck_Graphic output driver
K5	VSS_PLL1	VSS	Ground connection for PLL1
K7	VSS_PLL2	VSS	Ground connection for PLL2
L8	VSS_PLL3	VSS	Ground connection for PLL3
N9	VSS_PLL5	VSS	Ground connection for PLL5
D7	VSS_QUIET	VSS	Ground connection reference ground
M10	VSS_XTAL	VSS	Ground connection for XO
L3	VSSIO_PLL1	VSS	Ground connection for PLL1 clock driver
L7	VSSIO_PLL23	VSS	Ground connection for PLL23 clock driver
K8	VSSIO_REF	VSS	Ground connection for REF clock driver
M11	VSSIO_SYS	VSS	Ground connection for SYS clock driver
A12	VSUP_1P05	PS	Powers the Buck_V1P05 output driver
H13	VSUP_1P2	PS	Powers the Buck_V1P2 output driver
A4	VSUP_1P8	PS	Powers the Buck_V1P8 output driver
E13	VSUP_3P3	PS	Powers the Buck_V3P3 output driver
A8	VSUP_C	PS	Powers the Core output driver
H1	VSUP_G	PS	Powers the Graphic output driver
E12	VSUP1	PS	Powers all LDO cores
D12	VSUP2	PS	Powers the pass device of VINT and VLP regulator
F12	VSUP3	PS	Powers the pass device of RTC,V3P3_A, V2P5_A regulator
G2	VUNI	AIO	LDO_VUNI output node
L12	WAKE_B	DI	WAKE_B pin connection low active
N10	X1	AI	X1 pin connection
N12	X2	AIO	X2 pin connection

Table 4: DA6011 Pin out, alphabetic Ball name order

10.2 DA6011 169 pin BGA package

Map of ball allocations as seen from above the package.

Please note that this ball out is preliminary and is a matter of change

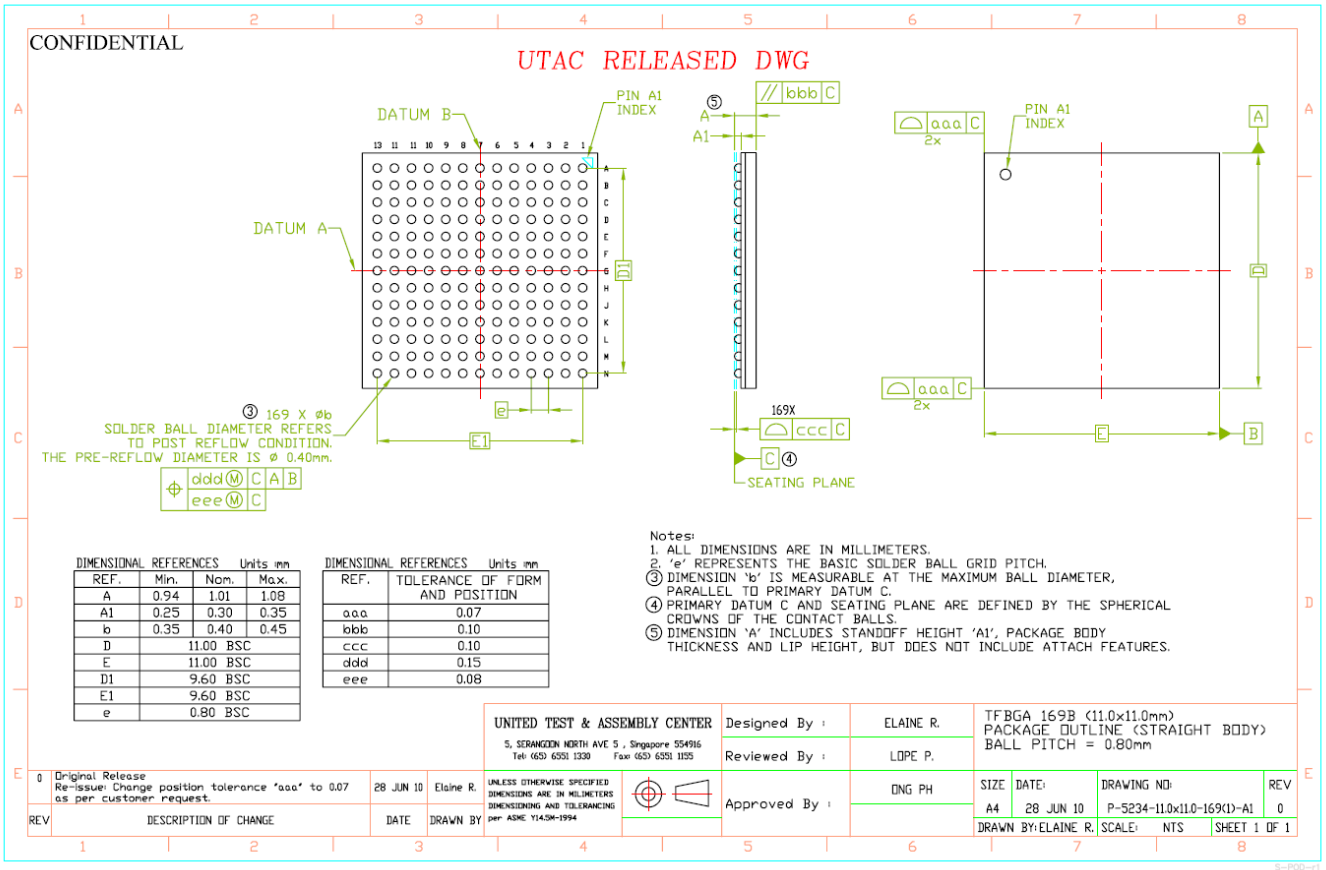
	1	2	3	4	5	6	7	8	9	10	11	12	13
A	VSS_1P8	VHS_1P8	VLS_1P8	VSUP_1P8	VSS_C	VHS_VCC	VLS_VCC	VSUP_C	VSS_1P05	VHS_1P05	VLS_1P05	VSUP_1P05	IREF
B	V1P8_S	V1P8	CS_1P8	VCC_S	CS_VCC	VCC_SENSE	VCC_VSS_SENSE	CS_1P05	V1P05_S	VID[0]	VID[1]	VREF	V3P3_S
C	V1P8_IN	VIDEN[0]	VIDEN[1]	IO_RST_PLC_B	THRMTRIP_B	ADC_IN_3	ADC_IN_2	TEST	RESET_IN_B	VID[3]	VID[2]	VID[5]	V3P3_IN
D	V0P9S	PROCHOT_B	IRQ_B	IO_SLP_PLB_B	IO_RST_PLB_B	SLPMODE	VSS_QUIET	SMB_CLK	VID[4]	VID[6]	VLP	VSUP2	VINT
E	VDD_V0P9	V0P9R	V1P25_S	VDDC_V1P8	VSS	VSS	VSS	VSS	VSS	V3P3_RTC	V3P3_A	VSUP1	VSUP_3P3
F	VDD_V1P8	V1P05	V1P5_S	VDDC_VUNI	VSS	VSS	VSS	VSS	VSS	V3P3	V2P5_A	VSUP3	VLX_3P3
G	VDD_VUNI	VUNI	VNN_VSS_SENSE	VNN_SENSE	VSS	VSS	VSS	VSS	VSS	SMB_DAT	V1P2	V1P2_IN	VSS_3P3
H	VSUP_G	IO_PWROK	RSTWARN	IO_RST_PLA_B	VSS	VSS	VSS	VSS	VSS	SYS	SLPRDY_B	V1P2_A	VSUP_1P2
J	VLX_VNN	PWRMODE[1]	PWRMODE[0]	IO_PWROK_EN	VSS	VSS	VSS	VSS	VSS	VCCIO_SYS	PWRBTN_B	TDO	VLX_1P2
K	VSS_G	TDI	RSMRST_B	PWRMODE[2]	VSS_PLL1	VCCIO_PLL23	VSS_PLL2	VSSIO_REF	VCCIO_REF	MCLK/ETH	PWROK	RSTRDY_B	VSS_1P2
L	TCLK	TMS	VSSIO_PLL1	VCCIO_PLL1	VCC_PLL1	VCC_PLL2	VSSIO_PLL23	VSS_PLL3	VCC_PLL3	VCC_PLL5	IO_SLP_PLC_B	WAKE_B	CTRL_V1P8_S
M	100MHz1_B	100MHz2_B	100MHz3_B	100MHz4_B	100MHz5_B	100MHz6_B	DOT_B	SATA_B	USB	VSS_XTAL	VSSIO_SYS	RESET_B	REF
N	100MHz1	100MHz2	100MHz3	100MHz4	100MHz5	100MHz6	DOT	SATA	VSS_PLL5	X1	VCC_XTAL	X2	VDDIO

10.3 Component Marking

Every component will be marked according to the following:

- Product code – DA6011, as referred to in the relevant purchase order.
- Dialog logo.
- Date of manufacture, in a four digit code of the form WWYY (e.g. 3504) or other codes as agreed upon.
- An identification index on the case to identify pin one.

10.4 Package outline

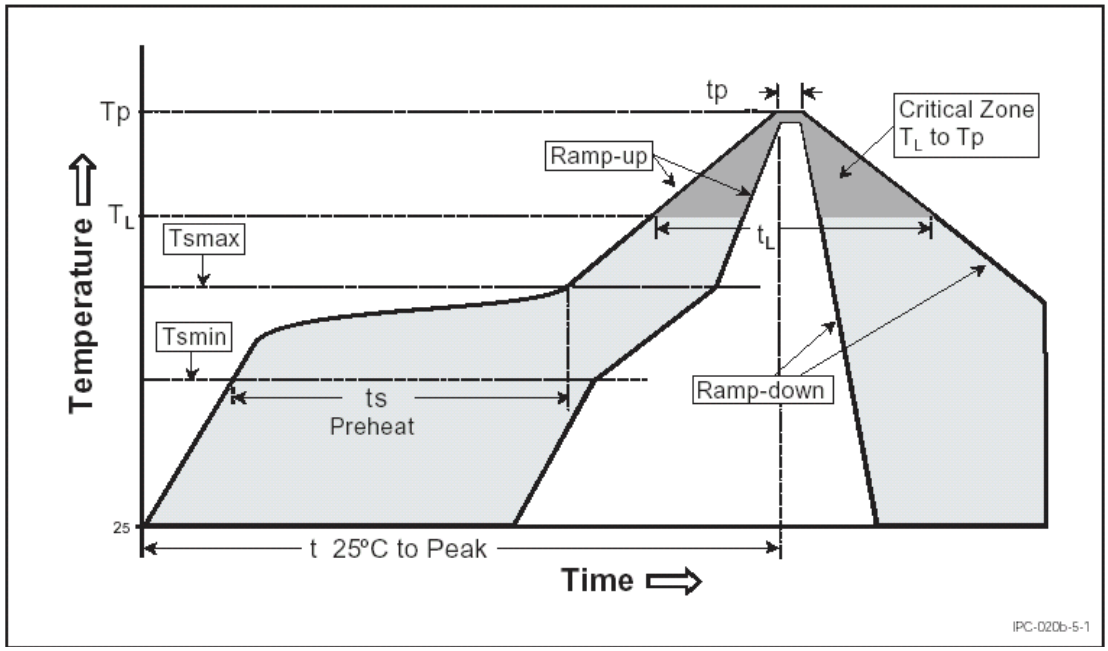


10.5 Soldering profile

A PCBA reflow profile depends on the thermal mass of the entire populated board. The actual temperature used in the reflow oven is a function of:

- Solder paste types
- Board density
- Component location
- Component mass
- Board finish

The figure and table below show the recommended reflow profile condition for 3Sn/37Pb and lead free solder.



Profile Feature	Pb-Free Assembly	
	Large Body	Small Body
Average ramp-up rate (T_L to T_p)	2℃/second max.	
Preheat -Temperature Min (Ts_{min}) -Temperature Max (Ts_{max}) -Time (min to max) (ts)	150℃ 200℃ 60-120 seconds	
Time maintained above: -Temperature (T_L) -Time (t_L)	217℃ 60-150 seconds	
Peak Temperature (Tp)	245+5/-5℃	
Time within 5℃ of actual Peak Temperature (tp)	10-30 seconds	
Ramp-down Rate	3℃/second max.	
Time 25℃ to Peak Temperature	8 minutes max.	

Note: 1.All temperatures refer to topside of the package, measured on the package body surface.
2.Depends on other parts on board density and follower solder paste manufacturer's guideline.

Appendix

DA6011 Component proposal

The proposal below includes components which are required by Intel® Atom™ processor E6xx series as well as components required by DA6011. Components requested by the IO-Hubs are not covered in this proposal list.

Due to the extended temperature range, DA6011 capacitors are proposed in X7R quality. The E6xx processor required components are taken out of the E6xx processor Platform Design Guide

The list below is seen as proposal and no guarantee on completeness can be given.

	Stabilization Capacitors								
		Domain	no	value	tol			type	
Intel E6XX	VCC	VCC_S	1	220µF	±20%			SP Cap AO Cap	
			1	47µ	±10%	16V		X7R	
			6	1µ	±10%	6,3V		X5R	
	VNN	VNN_S	1	220µF	±20%			SP Cap AO Cap	
			1	47µ	±10%	16V		X7R	
			4	1µ	±10%	6,3V		X5R	
	VCCD	V1P05_S	10	1µ	±10%	6,3V		X5R	
	VCCQ		6	1µ	±10%	6,3V		X5R	
	VCCP		6	1µ	±10%	6,3V		X5R	
	VCCPA		4	1µ	±10%	6,3V		X5R	
	VCCPDDR		1	47pF	±5%			COG	
	VCCD_DPL		1	1µF	±10%	6,3V		X5R	
			1	120	0,5A				
	VCCQHPLL		1	100nF	±10%	16V		X7R	
			1	22µF	±20%	6,3V		X5R	
			1	120	0,5A				
	VCCA_PEG		6	1µF	±10%	6,3V		X5R	
	LVD_VBG	V1P25_S	1	47pF	±5%			COG	
	VCCA	V1P5_S	4	1µ	±10%	6,3V		X5R	
			1	1µH	0,22A				
	VCC180	V1P8_S	3	1µ	±10%	6,3V		X5R	
	VCCD180		2	1µ	±10%	6,3V		X5R	
	VCCA180		1	10µF	±20%	6,3V		X5R	
			1	1,8µH	0,05A				
	VCCSFRDPLL		1	100nF	±10%	16V		X7R	
			1	120	0,5A				
	VCCSFR_EXP		1	100nF	±10%	16V		X7R	
	VCCSFRHPLL		1	1µ	±10%	6,3V		X5R	
			1	22µF	±20%	6,3V		X5R	
	VCCP33	V3P3_S	4	1µ	±10%	6,3V		X5R	
	VCCRTCEXT	V1P05	1	100nF	±10%	16V		X7R	
	VCC180SR	V1P8	1	1µ	±10%	6,3V		X5R	
	VCCP33SUS	V3P3	1	100nF	±10%	16V		X7R	
	VCCPSUS		1	100nF	±10%	16V		X7R	

DA6011		V0P9_S	1	10µF	±20%	6,3V		X7R	
		V0P9R	1	1µF	±10%	6,3V		X7R	
		V1P05_S	1	47µF	±20%	6,3V		X7R	or
			2	22µF	±20%	6,3V		X7R	or
			4	10µF	±20%	6,3V		X7R	
		V1P2_S	1	4.7µF	±20%	6,3V		X7R	
		V1P25_S	1	220nF	±10%	6,3V		X7R	
		V3P3_S	1	10µF	±20%	6,3V		X7R	
		V1P05	1	1µF	±10%	6,3V		X7R	
		V1P8	1	100µF	±20%			SP Cap AO Cap	or
			2	47µF	±20%	6,3V		X7R	or
			4	22µF	±20%	6,3V		X7R	or
			8	10µF	±20%	6,3V		X7R	
		V3P3	1	220µF	±20%	6,3V		SP Cap AO Cap	
		V1P2_A	1	220µF	±20%	6,3V		X7R	
		V2P5_A	1	1µF	±10%	6,3V		X7R	
		V3P3_A	1	1µF	±10%	6,3V		X7R	
		V3P3_RTC	1	1µF	±10%	6,3V		X7R	
		VINT	1	1µF	±10%	6,3V		X7R	
		VLP	1	220nF	±10%	6,3V		X7R	
	Input decoupling Capacitors								
	Buck_CORE	VCC_S	2	10µF	±20%	6,3V		X7R	
			1	10µF	±20%	10V		X7R	
	Buck_GRAPHIC	VNN_S	1	10µF	±20%	10V		X7R	
	VDD_V0P9	V0P9_S	1	100nF	±10%	6,3V		X7R	
	Buck_V1P05	V1P05_S	2	10µF	±20%	6,3V		X7R	
			1	10µF	±20%	10V		X7R	
	Buck_V1P2	V1P2_S	1	10µF	±20%	10V		X7R	
	VDD_V1P8	V1P8_S	1	100nF	±10%	6,3V		X7R	
	Buck_V1P8	V1P8	2	10µF	±20%	6,3V		X7R	
			1	10µF	±20%	10V		X7R	
	VDD_UNI	VUNI	1	100nF	±10%	6,3V		X7R	
	Buck_V3P3	V3P3	1	10µF	±20%	10V		X7R	
	VSUP1		1	4,7µF	±20%	10V		X7R	
			1	100nF	±10%	10V		X7R	
	VSUP2		1	4,7µF	±20%	10V		X7R	
			1	100nF	±10%	10V		X7R	
	VSUP3		1	4,7µF	±20%	10V		X7R	
			1	100nF	±10%	10V		X7R	
	VCC_PLL1	VINT	1	4,7µF	±20%	6,3V		X7R	
			1	100nF	±10%	6,3V		X7R	
	VCC_PLL2	VINT	1	100nF	±10%	6,3V		X7R	
	VCC_PLL3	VINT	1	100nF	±10%	6,3V		X7R	
	VCC_PLL5	VINT	1	100nF	±10%	6,3V		X7R	

VCCIO_PLL1	V1P8	1	4,7µF	±20%	6,3V		X7R	
		1	100nF	±10%	6,3V		X7R	
VCCIO_PLL23	V1P8	1	100nF	±10%	6,3V		X7R	
VCCIO_REF	V3P3_S*	1	4,7µF	±20%	6,3V		X7R	
		1	100nF	±10%	6,3V		X7R	
VCCIO_SYS	V3P3_S or VUNI*	1	100nF	±10%	6,3V		X7R	
VREF		1	100nF	±10%	6,3V		X7R	
		2	5,6pF	±5%			NP0	
Resistors								
Gate Resistors IREF	VCC_S, V1P05_S, V1P8	6 2	0..10Ω 100kΩ	±1% ±1%				
Resistors for sensing	VCC_S VNN_S V1P05_S	5	100Ω	±1%				
		1	10Ω	±1%				
		2	383Ω	±1%				
Pull-up	V1P05_S	1	10kΩ	±5%			PROCHOT_B	
Pull-up	V1P05_S	1	10kΩ	±5%			THERMTRIP_B	
Current measurement	VCC_S, V1P05_S, V1P8	3	10mΩ	±1%				
Inductors								
	VCC_S, V1P05_S, V1P8	3	1,5µH	±20%	~50mΩ		Saturation current ≥8A	
	VNN_S, V1P2	2	1,5µH	±20%	~50mΩ		Saturation current ≥3A	
	V3P3	1	4,7µH	±20%	~50mΩ		Saturation current ≥3A	
FETs								
	VCC_S, V1P05_S, V1P8	3	SI 7540DP µPA1890 µPA2792 FDS8858CZ					
Crystal								
		1	14,31818 MHz					

* application depending

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