High-Performance, 10 A, Dual-Phase DC-DC Converter

General Description

DA9121 is a power management unit (PMU) suitable for supplying CPUs, GPUs, DDR memory rails in single in-line pin package (SIPP) modules, smartphones, tablets, and other handheld applications.

DA9121 operates as a single-channel dual-phase buck converter, each phase requiring a small external 0.10 µH inductor. It is capable of delivering up to 10 A output current at a 0.3 V to 1.9 V output voltage range. The 2.5 V to 5.5 V input voltage range is suitable for a wide variety of low-voltage systems, including, but not limited to, all Li-Ion battery supplied applications.

With remote sensing, the DA9121 guarantees the highest accuracy and supports multiple PCB routing scenarios without loss of performance.

The pass devices are fully integrated, so no external FETs or Schottky diodes are needed.

A programmable soft start-up can be enabled, which limits the inrush current from the input node and secures a slope-controlled rail activation.

The dynamic voltage control (DVC) supports adaptive adjustment of the supply voltage dependent on the processor load, via either a direct register write using the communication interface (I^2C-compatible) or with a programmable input pin.

A configurable GPI allows multiple I^2C address selection for multiple instances of DA9121 in the same application.

DA9121 has integrated over-temperature and over-current protection for increased system reliability, without the need for external sensing components.

Key Features

- 2.5 V to 5.5 V input voltage
- 0.3 V to 1.9 V output voltage
- 4 MHz nominal switching frequency
- ±1 % accuracy (static)
- ±5 % accuracy (dynamic)
- I^2C-compatible interface (FM+)
- Programmable GPIOs
- Programmable soft-start
- Voltage, current, and temperature supervision
- -40 °C to +85 ºC ambient temperature range
- Package:
  24WLCSP 2.5 mm x 1.7 mm (0.4 mm pitch)
- 24WLP 2.7 mm x 1.9 mm (0.4 mm pitch)

Applications

- SIPP modules (SoC, DRAM)
- Smartphones
- Tablet PCs
- Infotainment
- Ultrabooks™
- Wi-Fi Modules
- Game Consoles

System Diagrams

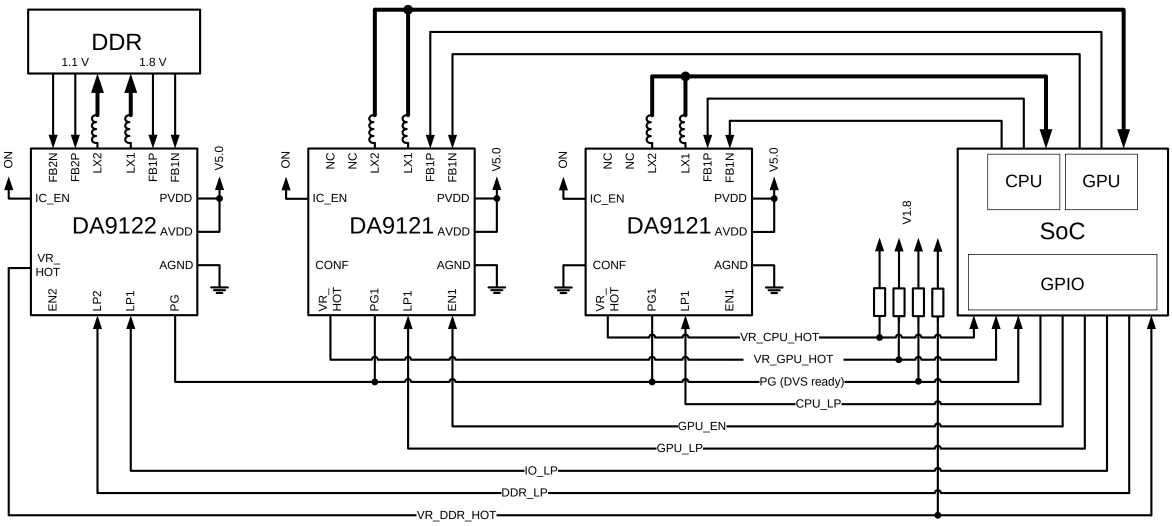


Figure 1: Typical Application Diagram (Port Control)

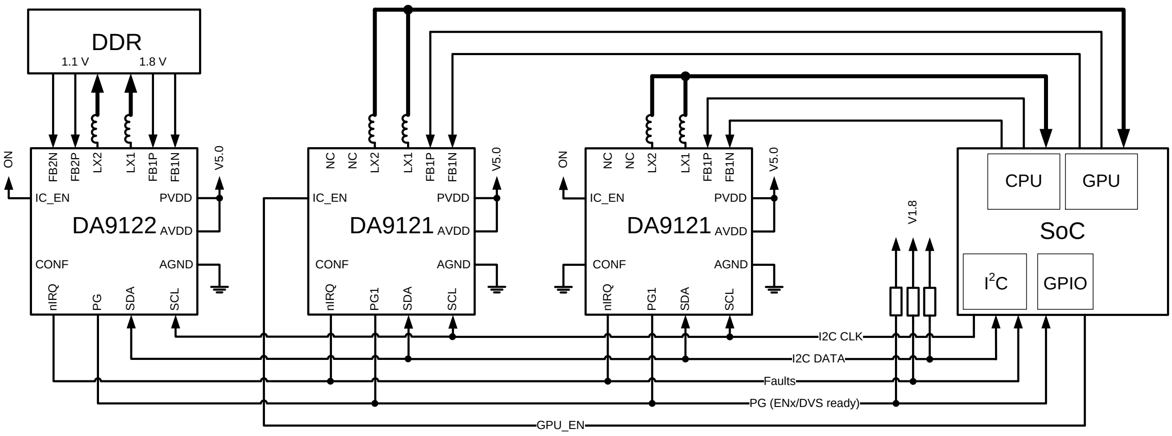


Figure 2: Typical Application Diagram (I²C Control)

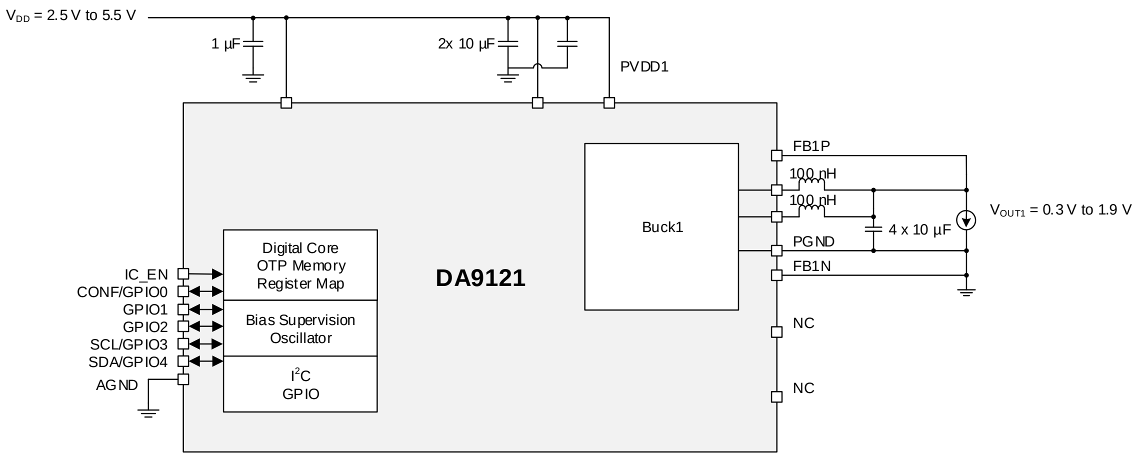


Figure 3: Simplified Schematic Diagram

Contents

1 Terms and Definitions

ATE	Automated test equipment
CPU	Central processing unit
DDR	Dual data rate
DVC	Dynamic voltage control
FET	Field effect transistor
FM+	Fast mode plus
GBD	Guaranteed by design
GBQ	Guaranteed by qualification
GBSPC	Guaranteed by statistical process characterization
GPI	General purpose input
GPIO	General purpose input/output
GPU	Graphics processing unit
IC	Integrated circuit
HW	Hardware
Li-Ion	Lithium-ion
OTP	One time programmable
PCB	Printed circuit board
PRS	Product requirements specification
SCL	Serial clock
SDA	Serial data
SIPP	Single in-line pin package
SW	Software

2 Pinout

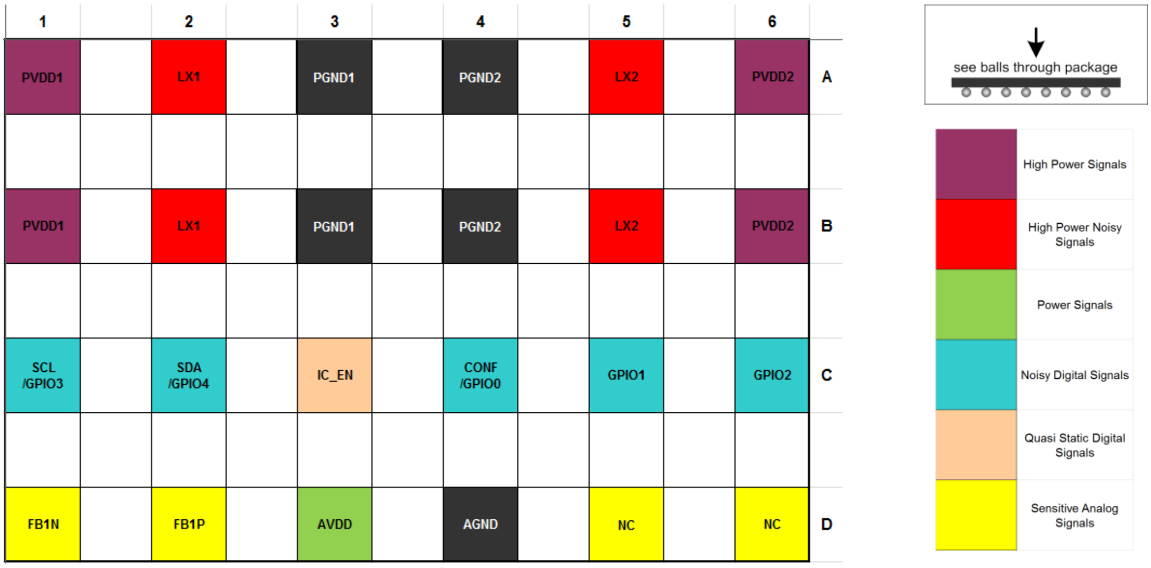


Figure 4: DA9121 Pinout Diagram (Top View)

Table 1: Pin Description

Pin No.	Pin Name	Type (Table 2)	Drive (mA)	Reset State	Description
A1, B1	PVDD1	PWR	5000		Supply voltage for buck power stage, decouple with 10 µF and connect to same source as AVDD
A2, B2	LX1	AIO	5000		Switch node of buck, connect a 100 nH inductor between LX1 and output capacitor
A3, B3	PGND1	GND	5000		Buck power stage VSS rail
A4, B4	PGND2	GND	5000		Buck power stage VSS rail
A5, B5	LX2	AIO	5000		Switch node of buck, connect a 100 nH inductor between LX1 and output capacitor
A6, B6	PVDD2	PWR	5000		Supply voltage for buck power stage, decouple with 10 µF and connect to same source as AVDD
C1	SCL/GPIO3	DIO	15		I^2C clock or general purpose I/O
C2	SDA/GPIO4	DIO	15		I^2C data or general purpose I/O
C3	IC_EN	AI	10		Powers up SW control interface and auxiliary circuitry (including bandgap, oscillator, and references).
C4	CONF/GPIO0	AI/DIO	10		Chip configuration or general purpose I/O
C5	GPIO1	DIO	10		General purpose I/O
C6	GPIO2	DIO	10		General purpose I/O
D1	FB1N	AI	10		Buck negative node of differential voltage feedback, connect to VSS at point of load
D2	FB1P	AI	10		Buck positive node of differential voltage feedback, connect to V_{OUT1} at point of load
D3	AVDD	PWR	10		Supply rail for analog control circuitry, decouple with 1 µF and connect to same source as PVDD

Pin No.	Pin Name	Type (Table 2)	Drive (mA)	Reset State	Description
D4	AGND	GND	10		Analog control and auxiliary circuitry VSS
D5	NC	AI			Not used
D6	NC	AI			Not used

Table 2: Pin Type Definition

Pin Type	Description	Pin Type	Description
DI	Digital input	AI	Analog input
DO	Digital output	AO	Analog output
DIO	Digital input/output	AIO	Analog input/output
PWR	Power	GND	Ground

3 Characteristics

3.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 3: Absolute Maximum Ratings

Parameter	Description	Conditions	Min	Max	Unit
T_{STG}	Storage temperature		-65	150	°C
T_J	Junction temperature		-40	150	°C
V_{SYS}	System supply voltage		-0.3	6.0	V
V_{PIN}	Voltage on pins		-0.3	6.0	V

3.2 Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Parameter	Description	Conditions (Note 1)	Min	Typ	Max	Unit
V_{SYS}	System supply voltage		2.5		5.5	V
V_{PIN}	Voltage on pins		-0.3		V_{SYS} + 0.3	V
T_J	Junction temperature		-40		125	°C
T_A	Ambient temperature		-40		85	°C

Note 1 Within the specified limits, a lifetime of 10 years is guaranteed. If operating outside of these recommended conditions, please consult with Dialog Semiconductor.

3.3 Thermal Characteristics

3.3.1 Thermal Ratings

Table 5: Package Ratings

Parameter	Description	Conditions	Min	Typ	Max	Unit
θ_{JA_WLCSP}	WLCSP Package thermal resistance Note 1			32.7		°C/W
θ_{JA_WLP}	WLP Package thermal resistance Note 1			34.8		°C/W

Note 1 Obtained from package thermal simulation, 2S2P4L board (JEDEC), influenced by PCB technology and layout.

3.3.2 Power Dissipation

Table 6: Power Dissipation

Parameter	Description	Conditions	Min	Typ	Max	Unit
P_D	Power dissipation	Derating factor above T_A = 70°C : 30.6 mW/°C ($1/\theta_{JA}$)		2140		mW

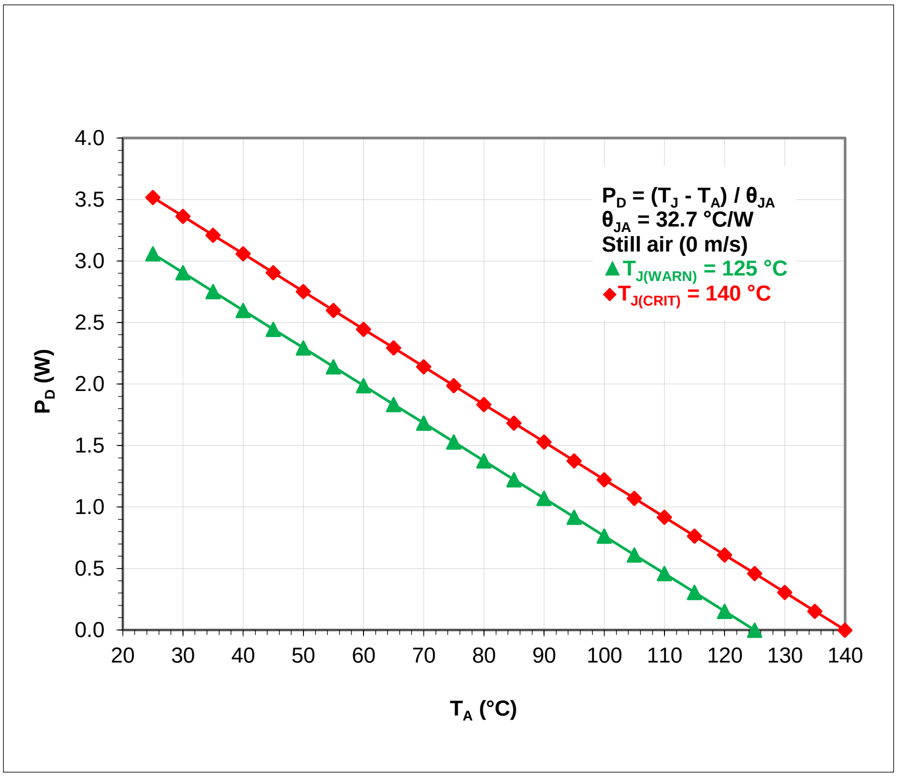


Figure 5: 24WLCSP Power Derating Curve

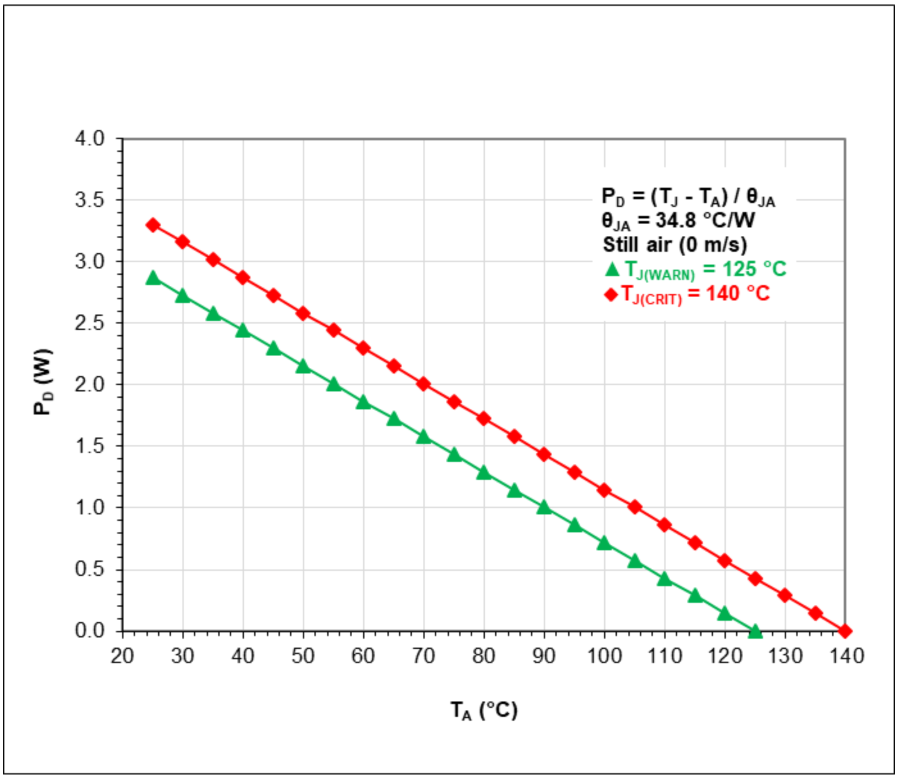


Figure 6: 24WLP Power Derating Curve

3.4 ESD Characteristics

Table 7: ESD Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{ESD_HBM}	ESD protection, human body model (HBM)				2	kV

3.5 Buck Characteristics

Unless otherwise noted, the following is valid for T_J = -40 °C to +125 °C, V_{SYS} = 2.5 V to 5.5 V.

Table 8: Buck Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External Electrical Conditions						
V_{IN}	Input voltage	$V_{IN} = V_{SYS}$	2.5		5.5	V
C_{OUT}	Output capacitance, per phase, including voltage and temperature coefficient		-40 %	2 x 10	+30 %	µF
ESR_{COUT}	Output capacitor series resistance, per phase	f > 100 kHz		2		mΩ
L	Inductor value, per phase, including current and temperature dependence		-50 %	0.1	+20 %	µH
DCR_L	Inductor DC resistance			30	50	mΩ

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
V_{OUT}	Output voltage, programmable in 10 mV steps	I_{OUT} = 0 mA to I_{MAX} V_{IN} = 2.5 V to 5.5 V	0.3		1.57	V
V_{OUT_LIM}	Output voltage, programmable in 10 mV steps	I_{OUT} = 0 mA to I_{MAX} V_{IN} = 3.0 V to 5.5 V	0.3		1.9	V
I_{LIM}	Current limit, programmable per phase Note 1	CHx_ILIM = 1010	-20 %	8	+20 %	A
V_{OUT_ACC}	Output voltage accuracy, including static line and load regulation	V_{OUT} ≥ 1 V	-1		1	%
V_{OUT_ACC}	Output voltage accuracy, including static line and load regulation	V_{OUT} < 1 V	-10		10	mV
$V_{THR\_PG\_RISE}$	Power good voltage threshold for rising	V_{OUT} = V_{BUCK}	-80	-50	-20	mV
$V_{THR\_PG\_DWN}$	Power good voltage threshold for falling	V_{OUT} = V_{BUCK}	-160	-130	-100	mV
V_{THR_HV}	High V_{OUT} voltage threshold	V_{OUT} = V_{BUCK}	100	150	200	mV
$V_{OUT\_TR\_LINE}$	Line transient response	V_{IN} = 3 V to 3.6 V I_{OUT} = 0.5 * I_{MAX} dt = 10 µs		15		mV
f_{SW}	Switching frequency, post-trim			4		MHz
t_{ON_MIN}	Minimum turn-on pulse 0 % duty is also supported			20		ns
t_{BUCK_EN}	Turn-on time	CHx_EN = high			20	µs
R_{PD}	Output pull-down resistance for each phase at the LX node, see BUCK<x>_PD_DIS	V_{IN} = 3.7 V V_{OUT} = 0.5 V	100	150	200	Ω
R_{ON_PMOS}	On resistance of switching PMOS, per phase	V_{IN} = 3.7 V		36		mΩ
R_{ON_NMOS}	On resistance of switching NMOS, per phase	V_{IN} = 3.7 V		17		mΩ
AUTO Mode						
$V_{OUT\_TR\_LD\_2PH}$	Load transient response, phase shedding enabled	V_{OUT} = 1 V I_{OUT} = 0 A to 10 A dI/dt = 10 A/µs		±5		%

Parameter	Description	Conditions	Min	Typ	Max	Unit
PFM Mode						
$I_{Q\_PFM\_2PH}$	Quiescent current in PFM	V_{IN} = 3.7 V No load No switching		164		µA

Note 1 t_{ON} > 40 ns

3.6 Performance and Supervision Characteristics

Table 9: Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
V_{THR_POR}	Power-on-reset threshold	Threshold for AVDD falling		2.1	2.25	V
$V_{THR\_POR\_HYS}$	Power-on-reset hysteresis			200		mV
T_{WARN}	Thermal warning temperature threshold		115	125	135	°C
T_{CRIT}	Thermal shutdown temperature threshold		130	140	150	°C
I_{IN_OFF}	Supply current	OFF state T_A = 27 °C IC_EN = 0		0.1	1	µA
I_{IN_ON}	Supply current	ON state T_A = 27 °C IC_EN = 1 Buck off	5	10	20	µA

3.7 Digital IO Characteristics

Table 10: Digital I/O Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
V_{IH_EN}	Input high voltage, IC enable		1.2		AVDD	V
V_{IL_EN}	Input low voltage, IC enable				0.4	V
t_{IC_EN}	IC enable time				1000	µs
$V_{IH\_GPIO\_SCL\_SDA}$	Input high voltage GPIO, SCL, SDA		1.2		AVDD	V

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{IL\_GPIO\_SCL\_SDA}$	Input low voltage GPIO, SCL, SDA				0.4	V
V_{OH_GPIO}	Output high voltage GPIO	Push-pull mode I_{OUT} = 1 mA	0.8*AVDD		AVDD	V
V_{OL_GPIO}	Output low voltage GPIO	Push-pull mode I_{OUT} = 1 mA			0.2*AVDD	V
V_{OL_SDA}	Output low voltage SDA	I_{OUT} = 3 mA		0.24		V
R_{PD}	GPIO pull-down resistor		2	10	120	kΩ
R_{PU}	GPIO pull-up resistor		2	10	120	kΩ

3.8 Timing Characteristics

Table 11: I2C Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
t_{BUS}	Bus free time between a STOP and START condition		0.5			µs
C_{BUS}	Bus line capacitive load				150	pF
f_{SCL}	SCL clock frequency		20 Note 1		1000	kHz
t_{LO_SCL}	SCL low time		0.5			µs
t_{HI_SCL}	SCL high time		0.26			µs
t_{RISE}	SCL and SDA rise time	Requirement for input			1000	ns
t_{FALL}	SCL and SDA fall time	Requirement for input			300	ns
t_{SETUP_START}	Start condition setup time		0.26			µs
t_{HOLD_START}	Start condition hold time		0.26			µs
t_{SETUP_STOP}	Stop condition setup time		0.26			µs
t_{DATA}	Data valid time				0.45	µs
t_{DATA_ACK}	Data valid acknowledge time				0.45	µs
t_{SETUP_DATA}	Data setup time		50			ns
t_{HOLD_DATA}	Data hold time		0			ns

Note 1 Minimum clock frequency is limited to 20 kHz if I2C_TIMEOUT is enabled

3.9 Typical Performance

Unless otherwise noted, V_{IN} = 3.7 V, V_{OUT} = 1.0 V, T_A = 25 °C, 2.0 mm x 1.6 mm 0.1 µH per-phase output inductors (DCR = typ. 11.5 mΩ) and 4 x 10 µF output capacitors.

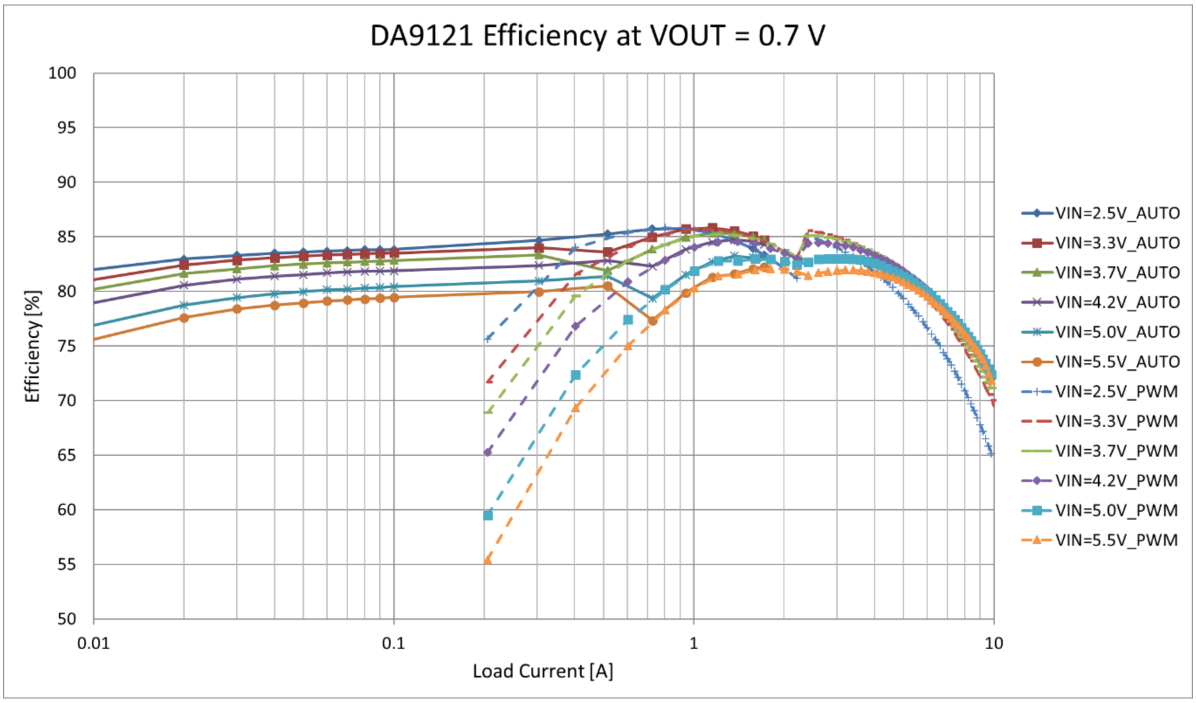


Figure 7: Efficiency v Load, V_{OUT} = 0.7 V

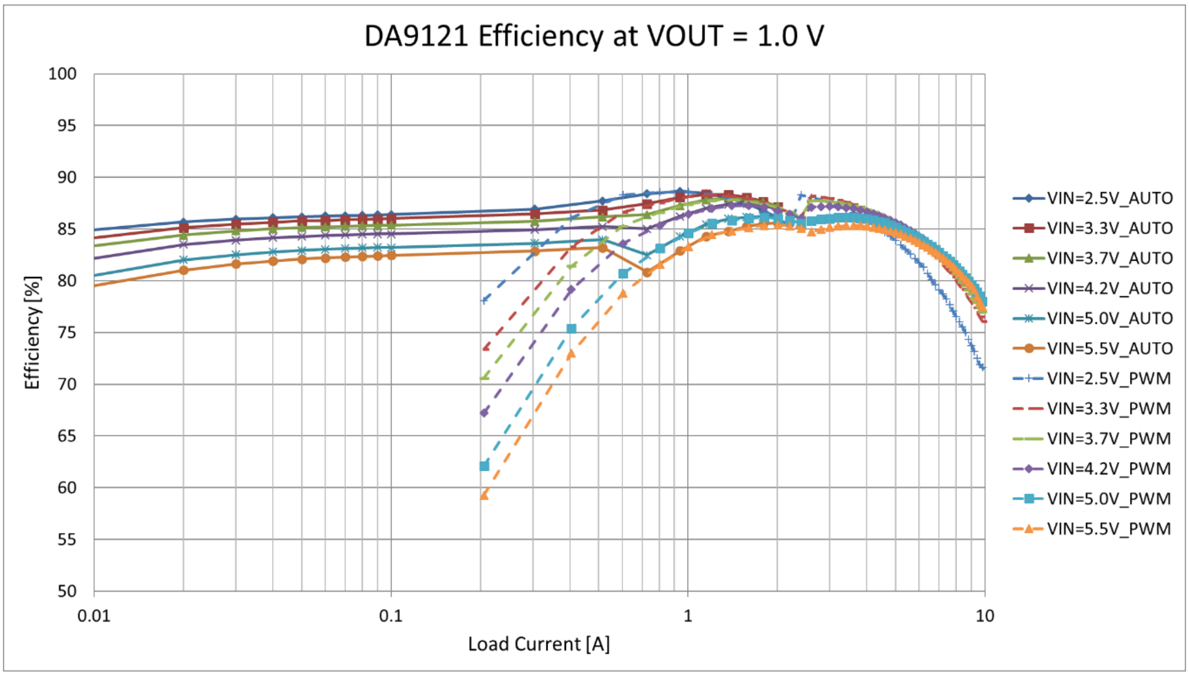


Figure 8: Efficiency vs Load, V_{OUT} = 1.0 V

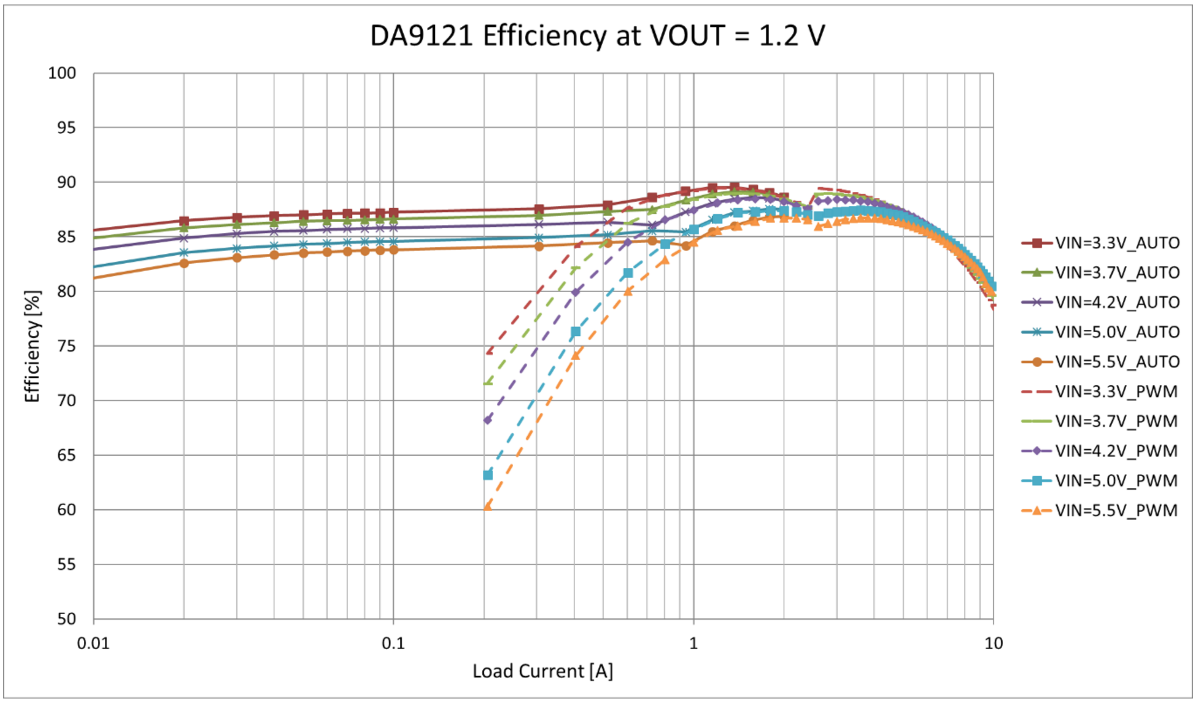


Figure 9: Efficiency vs Load, V_{OUT} = 1.2 V

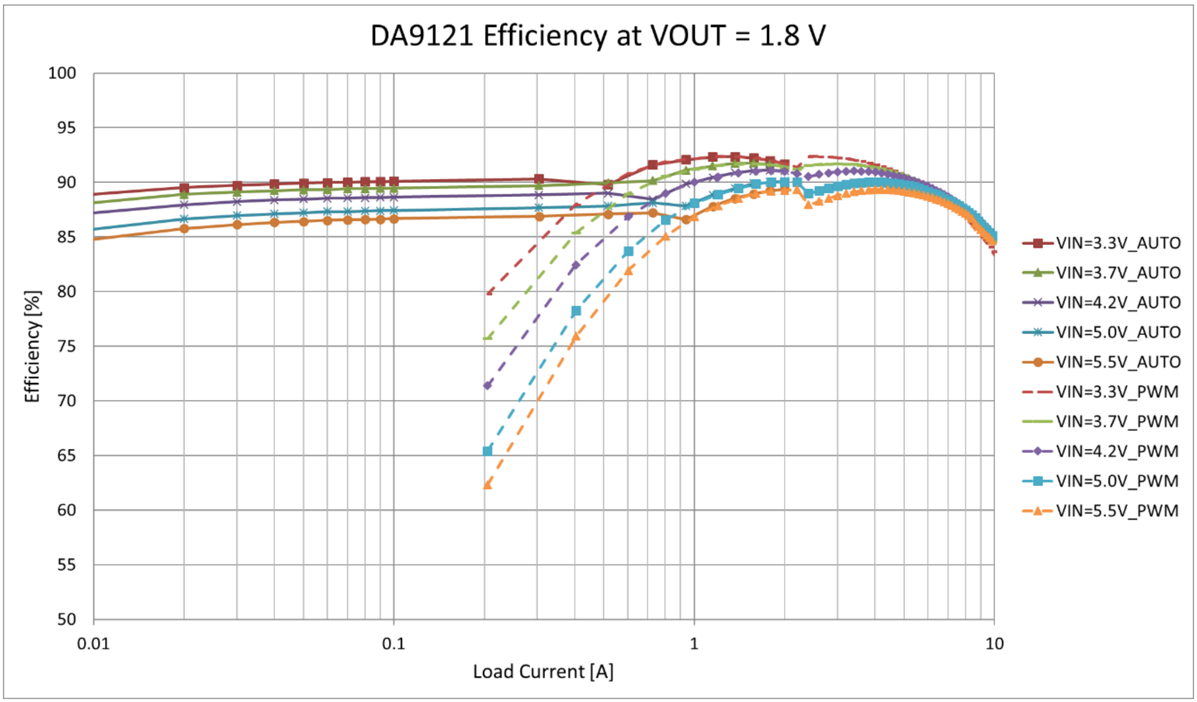


Figure 10: Efficiency vs Load, V_{OUT} = 1.8 V

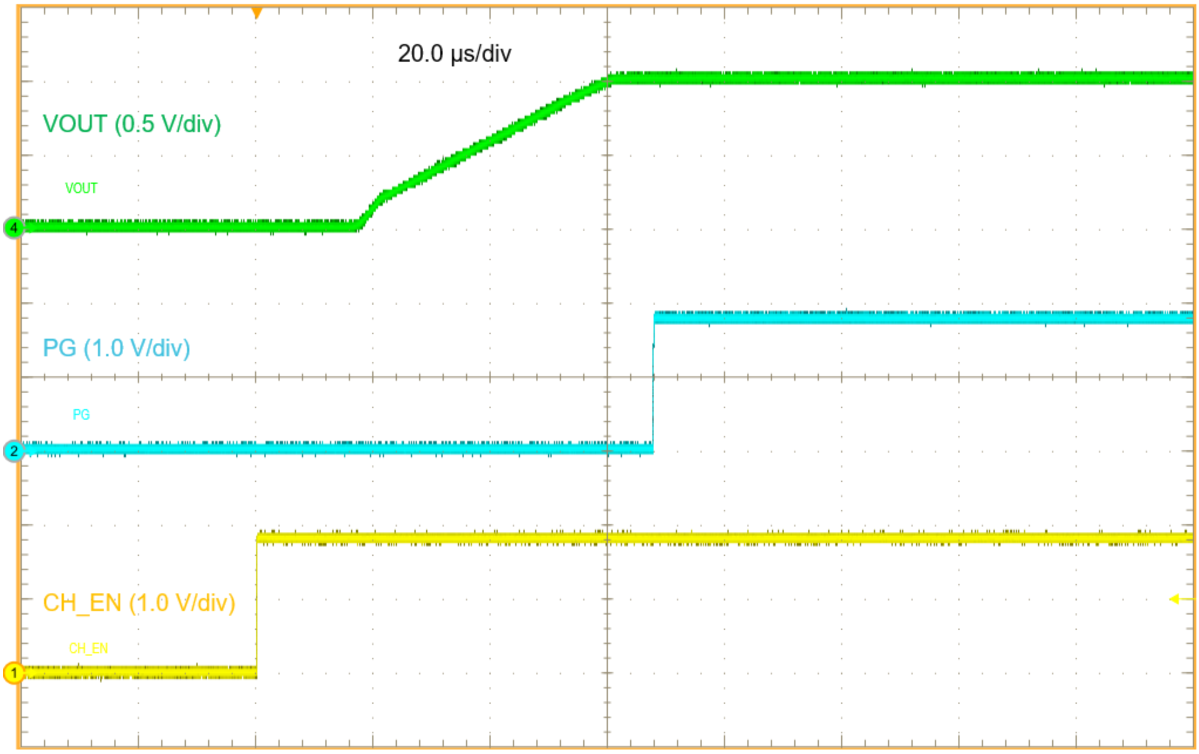


Figure 11: Buck Soft Start-up at 20 mV/µs Slew Rate

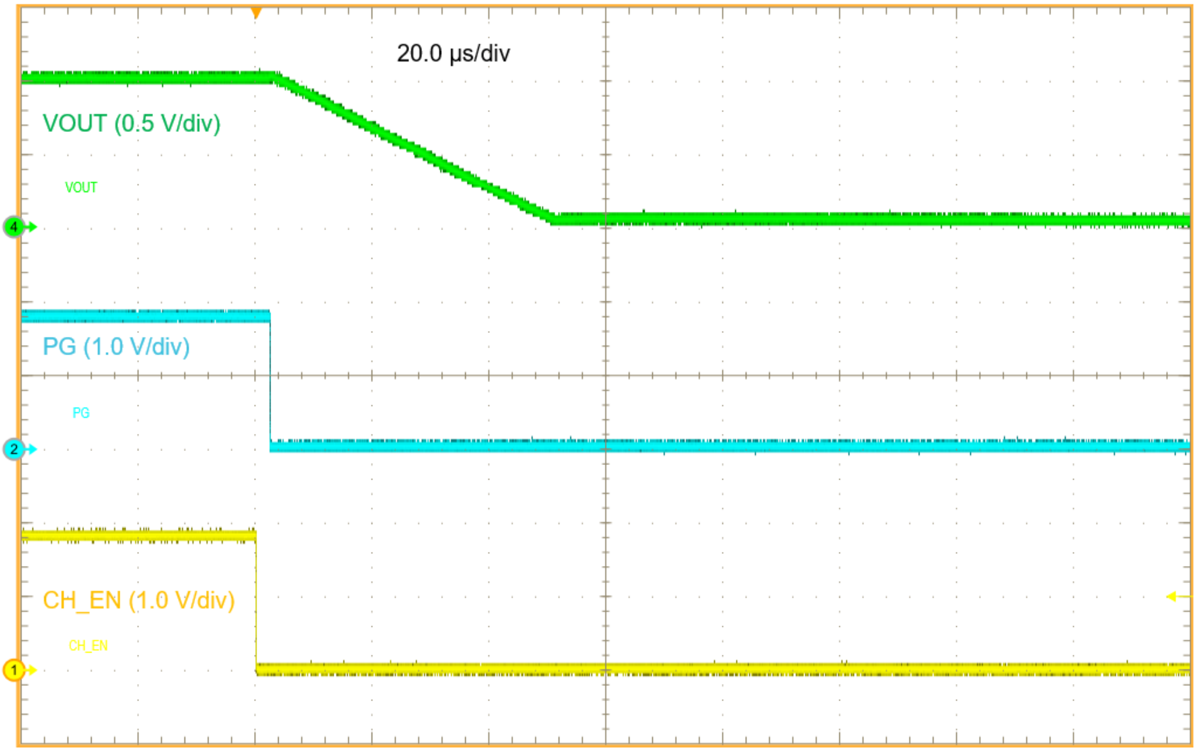


Figure 12: Buck Active Shutdown at 20 mV/µs Slew Rate

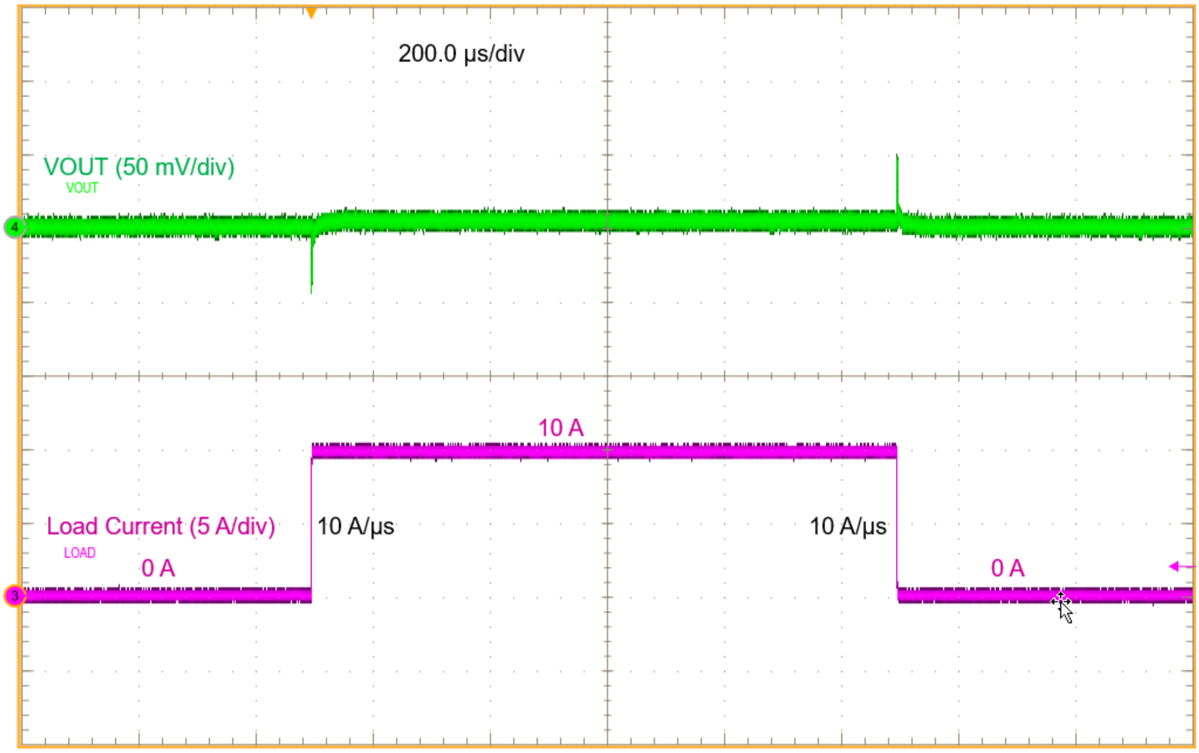


Figure 13: Buck Load Transient Response in PWM Mode, 0 A to 10 A at 10 A/µs

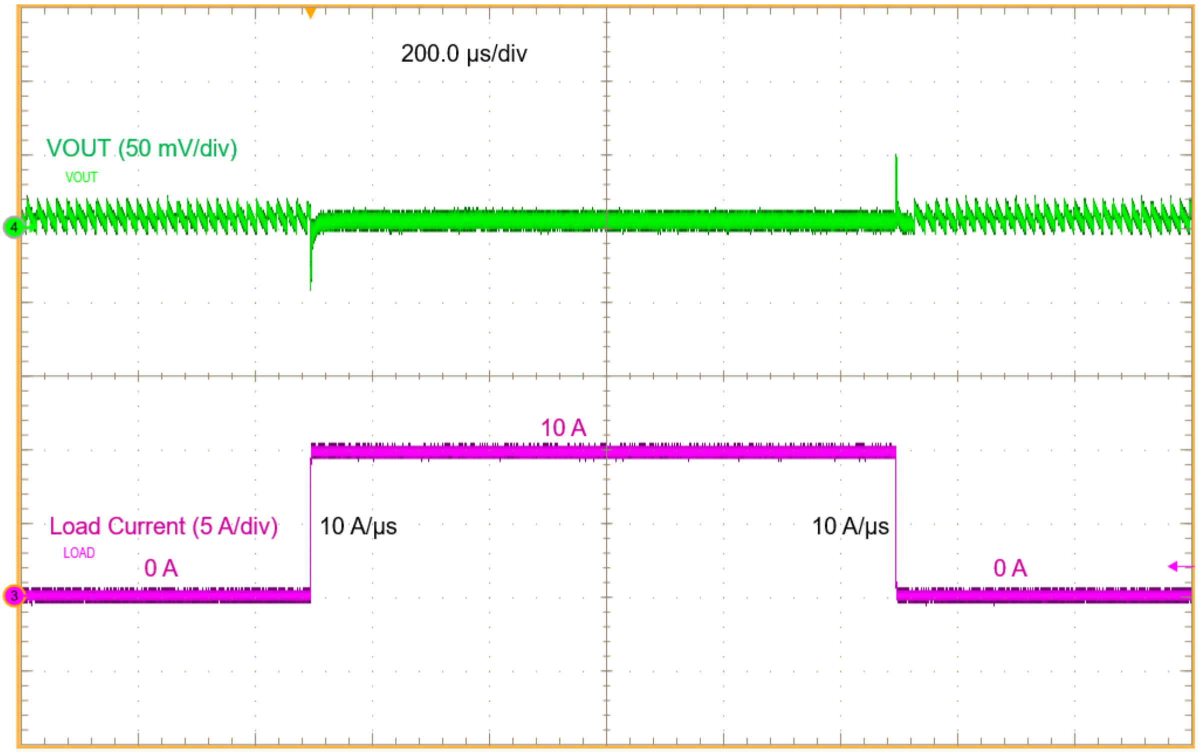


Figure 14: Buck Load Transient Response in AUTO Mode, 0 A to 10 A at 10 A/µs

4 Functional Description

4.1 DC-DC Buck Converter

DA9121 operates as a single-channel dual-phase buck converter capable of delivering up to 10 A output current at a 0.3 V to 1.9 V output voltage range.

The buck converter has two voltage registers. One defines the normal output voltage, while the other offers an alternative retention voltage. In this way, different application power modes can easily be supported. The voltage selection can be operated either via GPI or via control interface to guarantee the maximum flexibility according to the specific host processor status in the application.

When a buck is enabled, its output voltage is monitored and a power good signal indicates that the buck output voltage has reached a level higher than the $V_{THR\_PG\_RISE}$ threshold. The power good status is lost when the voltage drops below $V_{THR\_PG\_DWN}$ or increases above V_{THR_HV}. The status of the power good indicator can be read back via I^2C from the PG1 status bit. It can be also individually assigned to any of the GPIOs by setting the GPIO mode registers to PG1 output.

The buck converter is capable of supporting DVC transitions that occur when:

- the active and selected A- or B-voltage is updated to a new target value
- the voltage selection is changed from the A- to B-voltage (or B- to A-voltage) using CH1_VSEL

The DVC controller operates in pulse width modulation (PWM) mode with synchronous rectification.

The slew rate of the DVC transition is programmed at 10 mV per 8 µs, 4 µs, 2 µs, 1 µs, or 0.5 µs in register bits CH1_SR_DVC.

A pull-down resistor (typically 150 Ω) for each phase is always activated unless it is disabled by setting register bits CH1_PD_DIS to 1.

4.1.1 Switching Frequency

The buck switching frequency can be tuned using register bit OSC_TUNE. The internal 8 MHz oscillator frequency is tuned in ±160 kHz steps. This impacts the buck converter frequency in steps of 80 kHz and helps to mitigate possible disturbances to other high frequency systems in the application.

4.1.2 Operation Modes and Phase Selection

The buck converters can operate in PWM and PFM modes. The operating mode is selected using register bits CH1_<A or B>_MODE.

Phase shedding automatically changes between 1- and 2-phase operation at a typical current of 2.0 A.

If the automatic operation mode is selected on CH1_<A or B>_MODE, the buck converter automatically changes between synchronous PWM mode and PFM depending on the load current. This improves the efficiency across the whole range of output load currents.

4.1.3 Output Voltage Selection

The switching converter can be configured using the I²C interface.

Two output voltages can be pre-configured in registers CH1_<A or B>_VOUT. The output voltage can be selected by either toggling register bit CH1_VSEL or by re-programming the selected voltage control register. Both changes will result in ramped voltage transitions. After being enabled, the buck converter will, by default, use the register settings in CH1_A_VOUT unless the output voltage selection is configured via the GPI port.

Registers CH1_VMAX limit the output voltage that can be set for each of the respective buck converters.

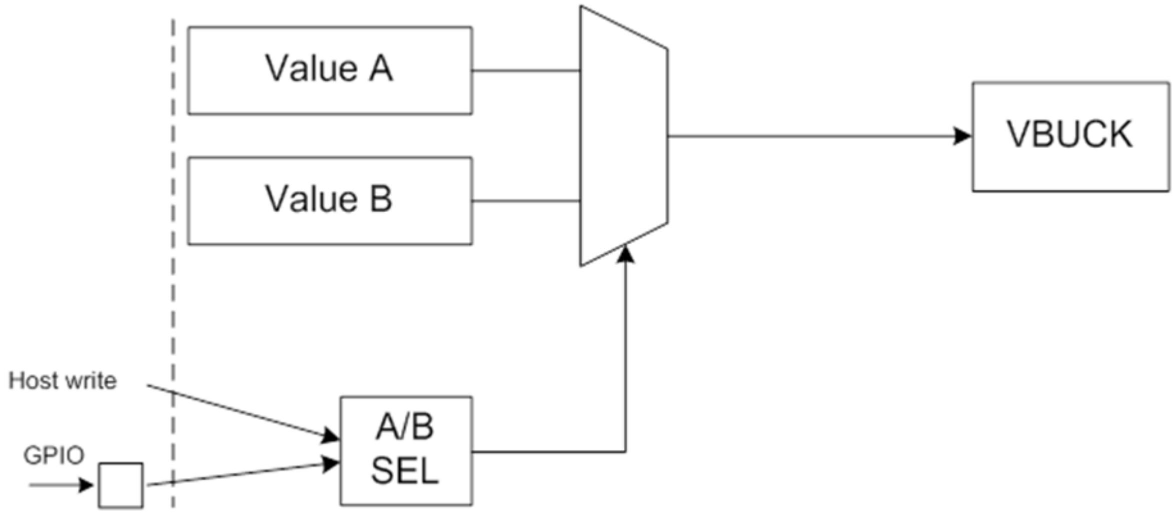


Figure 15: Buck Output Voltage Control Concept

4.1.4 Soft Start-Up and Shutdown

To limit in-rush current from VSYS, the buck converter can perform a soft-start after being enabled. The start-up behavior is a compromise between acceptable inrush current from the battery and turn-on time. Ramp times can be configured in register CH1_SR_STARTUP. Rates higher than 20 mV/µs may produce overshoot during the start-up phase, so it should be considered carefully.

A ramped power down can be selected in register bits CH1_SR_SHDN. When no ramp is selected (immediate power down), the output node will be discharged only by the pull-down resistor, if enabled in register CH1_PD_DIS.

4.1.5 Current Limit

The integrated current limit protects the power stages and external coil from excessive current. The buck current limit should be configured to at least 40 % higher than the required maximum output current.

When the current limit is reached, the buck converter generates an event and an interrupt to the host processor unless the interrupt has been masked using register M_OC1 in SYS_MASK_1. Register bit OC_DVC_MASK is used to mask over-current events during DVC transitions.

4.1.6 Thermal Protection

DA9121 is protected from internal overheating by thermal shutdown.

There are two kinds of flags concerning thermal protection, thermal warning and thermal critical. The warning flag is asserted when $T_J > T_{WARN}$ and the critical flag is asserted when $T_J > T_{CRIT}$. When the critical flag is asserted, Buck1 is shut down immediately.

Table 12: Thermal Protection Control Registers

Category	Register name	Description
Status	TEMP_WARN	Asserted as long as the thermal warning threshold is reached
	TEMP_CRIT	Asserted as long as the thermal shutdown threshold is reached
IRQ event	E_TEMP_WARN	TEMP_WARN caused event
	E_TEMP_CRIT	TEMP_CRIT caused event
IRQ mask	M_TEMP_WARN	TEMP_WARN event IRQ mask
	M_TEMP_CRIT	TEMP_CRIT event IRQ mask
	M_VR_HOT	TEMP_WARN status IRQ mask

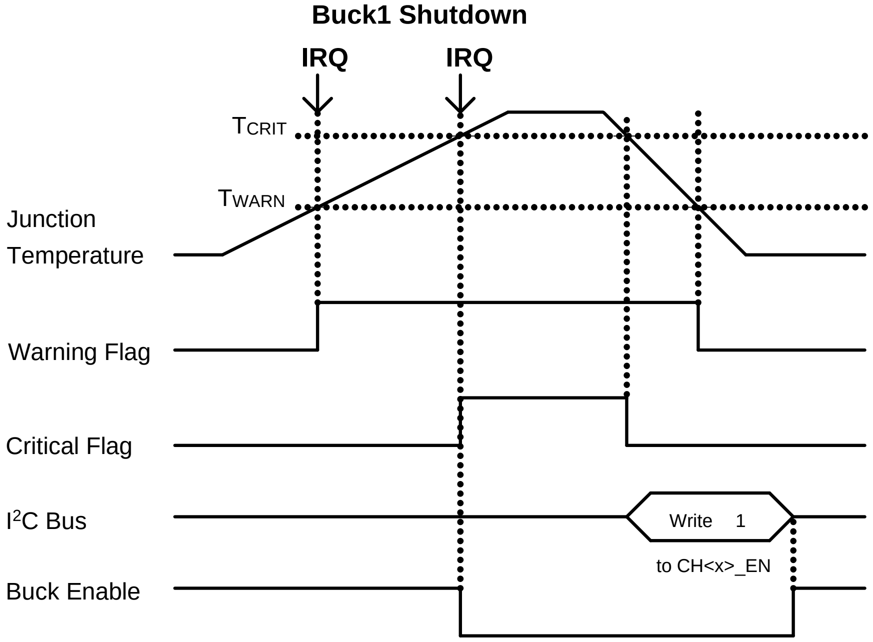


Figure 16: Thermal Protection Operation

4.2 Internal Circuits

4.2.1 IC_EN/Chip Enable/Disable

IC_EN is chip enable/disable control input. When IC_EN = 0, all blocks except for low I_Q POR are powered-down and buck output is pulled-down.

4.2.2 nIRQ/Interrupt

The interrupt triggers events. Trigger conditions and control registers for each interrupt event are listed in Table 13.

Some of these events are categorized as fault events and affect device operation (for example, buck disable), see Section 4.1.6.

Table 13: Interrupt List

Name	Polarity (Note 1)	Trigger	IRQ Status Register	IRQ Mask Register	Deglitch Period
Thermal warning (event)	N	T_J rising above T_{WARN}	E_TEMP_WARN	M_TEMP_WARN	0 s
Thermal critical (event)	N	T_J rising above T_{CRIT}	E_TEMP_CRIT	M_TEMP_CRIT	0 s
Buck1 power-good (event)	P	Buck1 V_{OUT} is in power-good voltage range (not under- or over-voltage)	E_PG1	M_PG1	0 s
Buck1 over-voltage (event)	N	Buck1 V_{OUT} rising above over-voltage threshold (target voltage + 150 mV)	E_OV1	M_OV1	Rise:8 µs Fall:8 µs
Buck1 under-voltage (event)	N	Buck1 V_{OUT} falling below under-voltage threshold (target voltage - V_{TH_PG})	E_UV1	M_UV1	0 s
Buck1 over-current (event)	N	Buck1 current rising above over-current threshold	E_OC1	M_OC1	0 s
Buck1 power-good (status) (Note 2)	P	Buck1 V_{OUT} is in power-good voltage range (not under- or over-voltage)	PG1	M_PG1_STAT (Note 3)	0 s
Thermal warning (status) (Note 2)	N	T_J rising above T_{WARN}	TEMP_WARN	M_VR_HOT (Note 3)	0 s
GPIO0 change (event)	N	Detect GPIO0 change for active trigger selected GPIO0_TRIG register	E_GPIO0	M_GPIO0	100 µs/ 1 ms/ 10 ms/ 100 ms
GPIO1 change (event)	N	Detect GPIO1 change for active trigger selected GPIO1_TRIG register	E_GPIO1	M_GPIO1	

Name	Polarity (Note 1)	Trigger	IRQ Status Register	IRQ Mask Register	Deglitch Period
GPIO2 change (event)	N	Detect GPIO2 change for active trigger selected GPIO2_TRIG register	E_GPIO2	M_GPIO2	

Note 1 Polarity at the source of the flag: P = active-high, N = active-low.
General rule is: normal system state is high, and abnormal system state is low (for example, PG = high means power-good, TEMP_CRIT = low when TEMP critical state).

Note 2 Interrupt outputs the status as is. I^2C write is not required for interrupt clear.

Note 3 OTP load value defined by CONF pin setting if CONF_EN = 1.

Table 14: Interrupt Registers Except for Power Good Status

Register	Description
E_<name>	Read-only interrupt event register 0: No interrupt 1: Interrupt occurred **Cleared after being written to I^2C**. Set until IRQ is removed.
M_<name>	Interrupt mask register 0: Not masked 1: Masked. No IRQ signal sent. Event register (E_<name>) is updated.

Table 15: Interrupt Registers for Power Good and Temp Warning Status

Register	Description
PG<x>	Buck<x> power good status. Asserted as long as the buck<x> output voltage is in range (under-voltage threshold < buck output voltage < over-voltage threshold) 0: Not power good 1: Power good
M_PG<x>_STAT	Power good status interrupt mask register 0: Not masked 1: Masked. No IRQ signal sent. Power good status register (PG<x>) is updated
TEMP_WARN	Asserted as long as the thermal warning threshold (T_{WARN}) is reached 0: Junction temperature is below T_{WARN} 1: Junction temperature is above T_{WARN}
M_VR_HOT	Temperature warning status (TEMP_WARN) interrupt mask register 0: Not masked 1: Masked. No IRQ signal sent. Temperature warning status register (TEMP_WARN) is updated

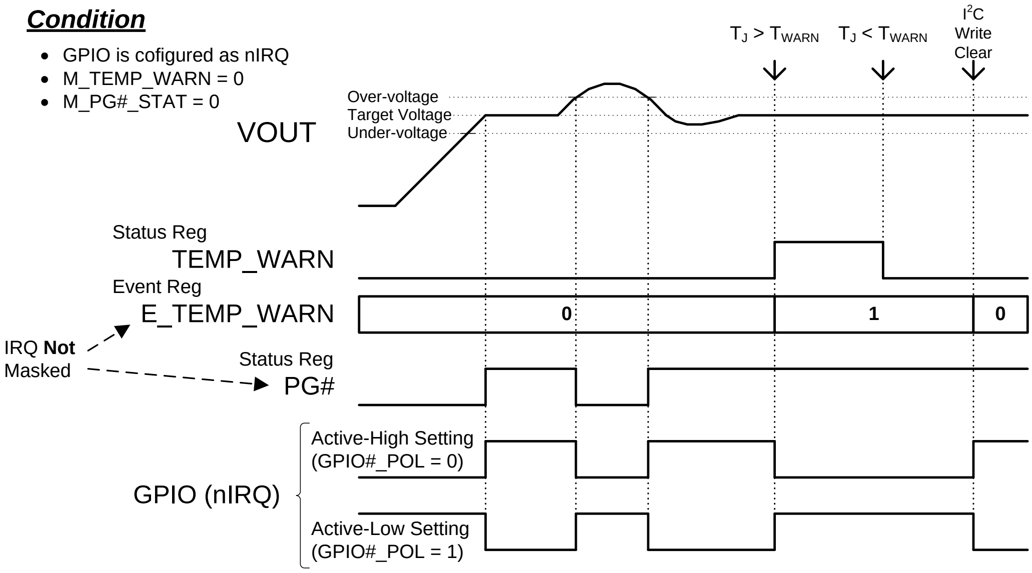


Figure 17: Interrupt Operation Example

4.2.3 GPIO

4.2.3.1 GPIO Pin Assignment

The DA9121 provides up to five GPIO pins, three if the I^{2}C is enabled, see Table 16. These registers are OTP programmable. When CONF_EN = 1 GPIO0 can be used for chip configuration.

Any register settings for GPIO3 and GPIO4 are ignored and GPIO3 and GPIO4 function as SCL and SDA respectively if I2C_EN = 1.

Table 16: GPIO Pin Assignment

OTP Option		GPIO Pin					Available GPIOs
I2C_EN	CONF_EN	CONF/ GPIO0	GPIO1	GPIO2	SCL/ GPIO3	SDA/ GPIO4	
1'b0	1'b0	GPIO0	GPIO1	GPIO2	GPIO3	GPIO4	5
	1'b1	CONF	GPIO1	GPIO2	GPIO3	GPIO4	4
1'b1	1'b0	GPIO0	GPIO1	GPIO2	SCL	SDA	3
	1'b1	CONF	GPIO1	GPIO2	SCL	SDA	2

4.2.3.2 GPIO Function

The GPIOs pins are configurable as the following functions in register GPIO<x>_MODE (x = 0 to 4):

- Buck1 enable input (EN1)
- Buck1 DVC control input (DVC1)
- Buck1 OTP setting reload input (RELOAD)
- Buck1 power good output (PG1)
- Interrupt output (nIRQ)

Table 17: GPIO Function Configuration

GPIO<x>_MODE[3:0]	Function	IO Condition
4'h0	GPIO disable	HiZ
4'h1	EN1	In
4'h2	Reserved	In
4'h3	Reserved	In
4'h4	DVC1	In
4'h5	Reserved	In
4'h6	Reserved	In
4'h7	RELOAD	In
4'h8	PG1	Out
4'h9	Reserved	Out
4'hA	Reserved	Out
4'hB	Reserved	Out
4'hC	nIRQ	Out
4'hD	Reserved	HiZ
4'hE	Low level	Out
4'hF	High level	Out

4.2.3.3 Chip Configuration Select (CONF)

GPIO0 functions as chip configuration select (CONF) input when CONF_EN = 1.

Three different chip configurations can be selected according to the CONF pin level, whether it is HIGH, LOW, or Hi-Z.

Table 18: GPIO0-Configurable Registers when CONF_EN = 1

Register Name	Description
IF_SLAVE_ADDR[6:0]	I2C slave address
CH1_A_MODE[1:0]	CH1_A Operation mode select
CH1_B_MODE[1:0]	CH1_B Operation mode select
CH1_VSEL	CH1 output voltage and operation selection
CH1_EN	CH1 enable
CH1_A_VOUT[7:0]	CH1 output voltage setting A
CH1_B_VOUT[7:0]	CH1 output voltage setting B
M_PG1_STAT	IRQ mask setting for CH1 power good status
M_VR_HOT	IRQ mask setting for temp warning status
GPIO1_MODE[3:0]	GPIO1 mode setting
GPIO2_MODE[3:0]	GPIO2 mode setting
GPIO1_OBUF	GPIO1 output buffer select
GPIO2_OBUF	GPIO2 output buffer select
GPIO1_TRIG[1:0]	GPIO1 input trigger select
GPIO1_POL	GPIO1 polarity select
GPIO1_PUPD	GPIO1 pull-up/pull-down enable
GPIO1_DEB[1:0]	GPIO1 input debounce time setting
GPIO1_DEB_RISE	GPIO1 input debounce rising edge enable
GPIO1_DEB_FALL	GPIO1 input debounce falling edge enable
GPIO2_TRIG[1:0]	GPIO2 input trigger select
GPIO2_POL	GPIO2 polarity select
GPIO2_PUPD	GPIO2 pull-up/pull-down enable
GPIO2_DEB[1:0]	GPIO2 input debounce time setting
GPIO2_DEB_RISE	GPIO2 input debounce rising edge enable
GPIO2_DEB_FALL	GPIO2 input debounce falling edge enable

4.2.3.4 OTP Reload (RELOAD)

Buck settings listed in Table 19 are reloaded from CONF registers by triggering GPIO configured as RELOAD input.

The OTP reload happens at the same time for Buck1 settings. During reloading, Buck1 keeps operating as configured without shut-down.

Table 19: OTP Reload Registers

Register Name	Description
CH#_VSEL	CH# output voltage and operation selection. 0: A, 1: B

Register Name	Description
CH#_A_VOUT[7:0]	CH# output voltage setting A : CH#_A_VOUT * 10 mV Setting under 0.3V is clamped to 0.3V, and setting over 1.9V is clamped to 1.9 V
CH#_B_VOUT[7:0]	CH# output voltage setting B : CH#_A_VOUT * 10 mV Setting under 0.3 V is clamped to 0.3 V, and setting over 1.9V is clamped to 1.9 V
CH#_A_MODE[1:0]	Operation mode selection 0: Force PFM 1: Force PWM. full phase 2: Force PWM with phase shedding 3: Auto mode
CH#_B_MODE[1:0]	Operation mode selection 0: Force PFM 1: Force PWM. full phase 2: Force PWM with phase shedding 3: Auto mode

4.3 Operating Modes

4.3.1 ON

DA9121 is ON when the IC_EN port is higher than V_{IH_EN} and the supply voltage is higher than V_{THR_POR}. Once enabled, the host processor can start communicating with DA9121 using the control interface, after the t_{IC_EN} delay.

4.3.2 OFF

DA9121 is OFF when the IC_EN port is lower than V_{IL_EN}. In OFF, the bucks are always disabled and LX nodes are pulled down by (typically 150 Ω) internal pull-down resistors.

4.4 I²C Communication

All features of DA9121 can be controlled with the I²C interface which is enabled or disabled in register I2C_EN.

I2C_EN	Description
0	I²C disable: SCL/GPIO3 and SDA/GPIO4 pins can be used as GPIO
1	I²C enable: SCL/GPIO3 and SDA/GPIO4 pins are used as I²C clock input and I²C data input/output.

GPIO3 functions as the I²C clock and GPIO4 carries all the power manager bidirectional I²C data. The I²C interface is open-drain supporting multiple devices on a single line. The bus lines have to be pulled high by external pull-up resistors (2 kΩ to 20 kΩ). The standard frequency of the I²C bus is 1 MHz in fast-mode plus (FM+), 400 kHz in fast-mode, or 100 kHz in standard mode.

4.4.1 I²C Protocol

All data is transmitted across the I²C bus in eight-bit groups. To send a bit, the SDA line is driven towards the intended state while the SCL is low (a low SDA indicates a zero bit). Once the SDA has settled, the SCL line is brought high and then low. This pulse on SCL clocks the SDA bit into the receiver's shift register.

A two-byte serial protocol is used containing one byte for address and one byte data. Data and address transfer are transmitted MSB first for both read and write operations. All transmissions begin with the START condition from the master while the bus is in idle state (the bus is free). It is initiated by a high to low transition on the SDA line while the SCL is in the high state (a STOP condition is indicated by a low to high transition on the SDA line while the SCL is in the high state).

Figure 18: I²C START and STOP Condition Timing

The I²C bus is monitored for a valid slave address whenever the interface is enabled. It responds immediately when it receives its own slave address. The acknowledge is done by pulling the SDA line low during the following clock cycle (white blocks marked with A in Figure 19 and Figure 20).

The protocol for a register write from master to slave consists of a START condition, a slave address with read/write bit, and the eight-bit register address followed by eight bits of data, terminated by a STOP condition. DA9121 responds to all bytes with acknowledge (A), see Figure 19.

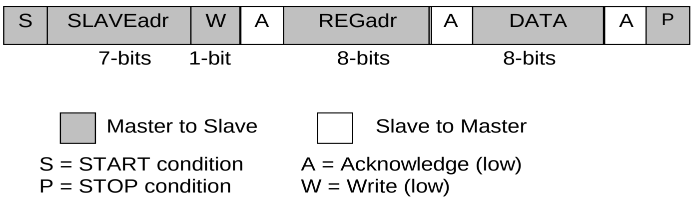


Figure 19: I²C Byte Write (SDA Line)

When the host reads data from a register it first has to write to DA9121 with the target register address and then read from DA9121 with a repeated START, or alternatively a second START, condition. After receiving the data, the host sends no acknowledge (A*) and terminates the transmission with a STOP condition, see Figure 20.

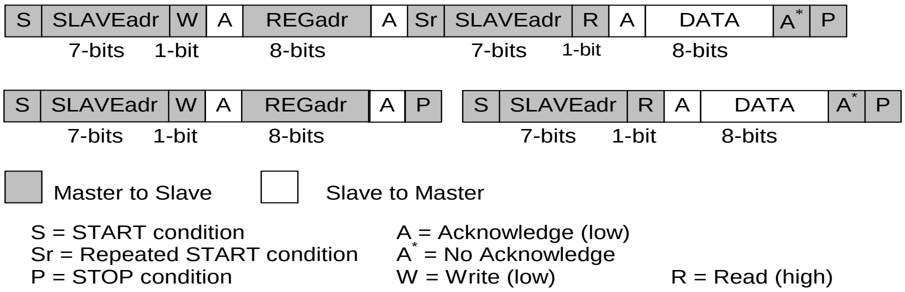


Figure 20: I²C Byte Read (SDA Line) Examples

5 Register Definitions

5.1 Register Map

Table 20: Register Map

Addr	Register	7	6	5	4	3	2	1	0
System Module									
System									
0x0001	SYS_STATUS_0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	TEMP_CRIT	TEMP_WARN
0x0002	SYS_STATUS_1	Reserved	Reserved	Reserved	Reserved	PG1	OV1	UV1	OC1
0x0003	SYS_STATUS_2	Reserved	Reserved	Reserved	Reserved	Reserved	GPIO2	GPIO1	GPIO0
0x0004	SYS_EVENT_0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	E_TEMP_CRIT	E_TEMP_WARN
0x0005	SYS_EVENT_1	Reserved	Reserved	Reserved	Reserved	E_PG1	E_OV1	E_UV1	E_OC1
0x0006	SYS_EVENT_2	Reserved	Reserved	Reserved	Reserved	Reserved	E_GPIO2	E_GPIO1	E_GPIO0
0x0007	SYS_MASK_0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	M_TEMP_CRIT	M_TEMP_WARN
0x0008	SYS_MASK_1	Reserved	Reserved	Reserved	Reserved	M_PG1	M_OV1	M_UV1	M_OC1
0x0009	SYS_MASK_2	Reserved	Reserved	Reserved	Reserved	Reserved	M_GPIO2	M_GPIO1	M_GPIO0
0x000A	SYS_MASK_3	Reserved	Reserved	Reserved	Reserved	M_VR_HOT	Reserved	Reserved	M_PG1_STAT
0x000B	SYS_CONFIG_0	Reserved				Reserved			
0x000C	SYS_CONFIG_1	Reserved				Reserved			
0x000D	SYS_CONFIG_2	Reserved	OC_LATCHOFF<1:0>		OC_DVC_MASK	PG_DVC_MASK<1:0>		Reserved	Reserved
0x000E	SYS_CONFIG_3	Reserved	OSC_TUNE<2:0>			Reserved	Reserved	I2C_TIMEOUT	Reserved
0x0010	SYS_GPIO0_0	Reserved	Reserved	Reserved	GPIO0_MODE<3:0>				GPIO0_OBUF
0x0011	SYS_GPIO0_1	GPIO0_DEB_FALL	GPIO0_DEB_RISE	GPIO0_DEB<1:0>		GPIO0_PUPD	GPIO0_POL	GPIO0_TRIG<1:0>	
0x0012	SYS_GPIO1_0	Reserved	Reserved	Reserved	GPIO1_MODE<3:0>				GPIO1_OBUF
0x0013	SYS_GPIO1_1	GPIO1_DEB_FALL	GPIO1_DEB_RISE	GPIO1_DEB<1:0>		GPIO1_PUPD	GPIO1_POL	GPIO1_TRIG<1:0>	
0x0014	SYS_GPIO2_0	Reserved	Reserved	Reserved	GPIO2_MODE<3:0>				GPIO2_OBUF
0x0015	SYS_GPIO2_1	GPIO2_DEB_FALL	GPIO2_DEB_RISE	GPIO2_DEB<1:0>		GPIO2_PUPD	GPIO2_POL	GPIO2_TRIG<1:0>	

Addr	Register	7	6	5	4	3	2	1	0
Buck Control									
Buck1									
0x0020	BUCK_BUCK1_0	Reserved	CH1_SR_DVC_DWN<2:0>			CH1_SR_DVC_UP<2:0>			CH1_EN
0x0021	BUCK_BUCK1_1	Reserved	CH1_SR_SHDN<2:0>			CH1_SR_STARTUP<2:0>			CH1_PD_DIS
0x0022	BUCK_BUCK1_2	Reserved	Reserved	Reserved	Reserved	CH1_ILIM<3:0>			
0x0023	BUCK_BUCK1_3	CH1_VMAX<7:0>							
0x0024	BUCK_BUCK1_4	Reserved	Reserved	Reserved	CH1_VSEL	CH1_B_MODE<1:0>		CH1_A_MODE<1:0>	
0x0025	BUCK_BUCK1_5	CH1_A_VOUT<7:0>							
0x0026	BUCK_BUCK1_6	CH1_B_VOUT<7:0>							
0x0027	BUCK_BUCK1_7	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	
Serialization									
0x0048	OTP_DEVICE_ID	DEV_ID<7:0>							
0x0049	OTP_VARIANT_ID	MRC<3:0>				VRC<3:0>			
0x004A	OTP_CUSTOMER_ID	CUST_ID<7:0>							
0x004B	OTP_CONFIG_ID	CONFIG_REV<7:0>							

5.1.1 System

Table 21: SYS_STATUS_0 (0x0001)

Bit	Symbol	Description
[1]	TEMP_CRIT	Asserted as long as the thermal shutdown threshold is reached
[0]	TEMP_WARN	Asserted as long as the thermal warning threshold is reached

Table 22: SYS_STATUS_1 (0x0002)

Bit	Symbol	Description
[3]	PG1	Asserted as long as the Buck1 output voltage is in range
[2]	OV1	Asserted as long as Buck1 hitting over-voltage
[1]	UV1	Asserted as long as Buck1 hitting under-voltage
[0]	OC1	Asserted as long as Buck1 hitting over-current

Table 23: SYS_STATUS_2 (0x0003)

Bit	Symbol	Description
[2]	GPIO2	GPIO2 status
[1]	GPIO1	GPIO1 status
[0]	GPIO0	GPIO0 status

Table 24: SYS_EVENT_0 (0x0004)

Bit	Symbol	Description
[1]	E_TEMP_CRIT	TEMP_CRIT caused event. Writing 1 action clear this bit into 0 if event source has been released.
[0]	E_TEMP_WARN	TEMP_WARN caused event. Writing 1 action clear this bit into 0 if event source has been released.

Table 25: SYS_EVENT_1 (0x0005)

Bit	Symbol	Description
[3]	E_PG1	PG1 caused event. Writing 1 action clear this bit into 0 if event source has been released.
[2]	E_OV1	OV1 caused event. Writing 1 action clear this bit into 0 if event source has been released.
[1]	E_UV1	UV1 caused event. Writing 1 action clear this bit into 0 if event source has been released.
[0]	E_OC1	OC1 caused event. Writing 1 action clear this bit into 0 if event source has been released.

Table 26: SYS_EVENT_2 (0x0006)

Bit	Symbol	Description
[2]	E_GPIO2	GPIO2 event. Writing 1 action clear this bit into 0 if event source has been released.
[1]	E_GPIO1	GPIO1 event. Writing 1 action clear this bit into 0 if event source has been released.
[0]	E_GPIO0	GPIO0 event. Writing 1 action clear this bit into 0 if event source has been released.

Table 27: SYS_MASK_0 (0x0007)

Bit	Symbol	Description
[1]	M_TEMP_CRIT	TEMP_CRIT IRQ mask
[0]	M_TEMP_WARN	TEMP_WARN IRQ mask

Table 28: SYS_MASK_1 (0x0008)

Bit	Symbol	Description
[3]	M_PG1	PG1 event IRQ mask
[2]	M_OV1	OV1 event IRQ mask
[1]	M_UV1	UV1 event IRQ mask
[0]	M_OC1	OC1 event IRQ mask

Table 29: SYS_MASK_2 (0x0009)

Bit	Symbol	Description
[2]	M_GPIO2	GPIO2 IRQ mask
[1]	M_GPIO1	GPIO1 IRQ mask
[0]	M_GPIO0	GPIO0 IRQ mask

Table 30: SYS_MASK_3 (0x000A)

Bit	Symbol	Description
[3]	M_VR_HOT	Temp warning status IRQ mask. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1
[0]	M_PG1_STAT	PG1 status IRQ mask. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1

Table 31: SYS_CONFIG_2 (0x000D)

Bit	Symbol	Description
[6:5]	OC_LATCHOFF	Over-current latch-off setting. BUCK shut-down after OCP for 8 µs/1 ms/3 ms unless disable setting. IRQ is generated unless IRQ is masked. **Value** **Description** **0x0** **Latch off disable** 0x1 Latch off after 8 µs of OCP signal 0x2 Latch off after 1 ms of OCP signal 0x3 Latch off after 3 ms of OCP signal
[4]	OC_DVC_MASK	Over-current event (IRQ and latch-off feature) mask during DVC ramp-up and ramp-down
[3:2]	PG_DVC_MASK	Power-good mask during DVC **Value** **Description** **0x0** **No mask** 0x1 Mask as not power good during DVC 0x2 Mask as power good during DVC 0x3 Reserved

Table 32: SYS_CONFIG_3 (0x000E)

Bit	Symbol	Description
[6:4]	OSC_TUNE	Tune oscillator frequency, tuned frequency = Current + OSC_TUNE * 160 kHz **Value** **Description** 0x3 3 0x2 2 0x1 1 **0x0** **0** 0x7 -1 0x6 -2 0x5 -3 0x4 -4
[1]	I2C_TIMEOUT	Enable automatic reset of 2-wire interface (if SDA stays low for >50 ms).

Table 33: SYS_GPIO0_0 (0x0010)

Bit	Symbol	Description
[4:1]	GPIO0_MODE	GPIO function mode select **Value** **Description** **0x0** **GPIO disable** 0x1 EN1 input 0x2 Reserved 0x3 Reserved 0x4 DVC1 input 0x5 Reserved 0x6 Reserved 0x7 RELOAD input 0x8 PG1 output 0x9 Reserved 0xA Reserved 0xB Reserved 0xC nIRQ output 0xD Reserved 0xE Low output 0xF High output
[0]	GPIO0_OBUF	GPIO output buffer select **Value** **Description** **0x0** **open-drain output** 0x1 push-pull output

Table 34: SYS_GPIO0_1 (0x0011)

Bit	Symbol	Description
[7]	GPIO0_DEB_FALL	GPI debouce falling edge
[6]	GPIO0_DEB_RISE	GPI debounce rising edge
[5:4]	GPIO0_DEB	GPI debounce time **Value** **Description** **0x0** **100 µs debouce** 0x1 1 ms debouce 0x2 10 ms debounce 0x3 100 ms debounce

Bit	Symbol	Description
[3]	GPIO0_PUPD	GPIO pull-up/pull-down enable **Value** / **Description** **0x0**: **GPI: pull-down disabled, GPO: pull-up to AVDD disabled** 0x1: GPI: pull-down enabled, GPO: pull-up to AVDD enabled
[2]	GPIO0_POL	GPIO polarity **Value** / **Description** **0x0**: **GPIO is active-high** 0x1: GPIO is active-low
[1:0]	GPIO0_TRIG	GPI trigger type **Value** / **Description** **0x0**: **Dual-edge triggered** 0x1: Pos-edge triggered 0x2: Neg-edge triggered 0x3: Reserved (No trigger)

Table 35: SYS_GPIO1_0 (0x0012)

Bit	Symbol	Description
[4:1]	GPIO1_MODE	GPIO function mode select. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1 **Value** / **Description** **0x0**: **GPIO disable** 0x1: EN1 input 0x2: Reserved 0x3: Reserved 0x4: DVC1 input 0x5: Reserved 0x6: Reserved 0x7: RELOAD input 0x8: PG1 output 0x9: Reserved 0xA: Reserved 0xB: Reserved 0xC: nIRQ output 0xD: Reserved 0xE: Low output 0xF: High output

Bit	Symbol	Description
[0]	GPIO1_OBUF	GPIO output buffer select. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1 **Value** **Description** **0x0** **open-drain output** 0x1 push-pull output

Table 36: SYS_GPIO1_1 (0x0013)

Bit	Symbol	Description
[7]	GPIO1_DEB_FALL	GPI debouce falling edge. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1
[6]	GPIO1_DEB_RISE	GPI debounce rising edge. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1
[5:4]	GPIO1_DEB	GPI debounce time. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1 **Value** **Description** **0x0** **100 µs debouce** 0x1 1 ms debouce 0x2 10 ms debounce 0x3 100 ms debounce
[3]	GPIO1_PUPD	GPIO pull-up/pull-down enable. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1 **Value** **Description** **0x0** **GPI: pull-down disabled, GPO: pull-up to AVDD disabled** 0x1 GPI: pull-down enabled, GPO: pull-up to AVDD enabled
[2]	GPIO1_POL	GPIO polarity. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1 **Value** **Description** **0x0** **GPIO is active-high** 0x1 GPIO is active-low
[1:0]	GPIO1_TRIG	GPI trigger type. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1 **Value** **Description** **0x0** **Dual-edge triggered** 0x1 Pos-edge triggered 0x2 Neg-edge triggered 0x3 Reserved (No trigger)

Table 37: SYS_GPIO2_0 (0x0014)

Bit	Symbol	Description
[4:1]	GPIO2_MODE	GPIO function mode select. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1 **Value** **Description** **0x0** **GPIO disable** 0x1 EN1 input 0x2 Reserved 0x3 Reserved 0x4 DVC1 input 0x5 Reserved 0x6 Reserved 0x7 RELOAD input 0x8 PG1 output 0x9 Reserved 0xA Reserved 0xB Reserved 0xC nIRQ output 0xD Reserved 0xE Low output 0xF High output
[0]	GPIO2_OBUF	GPIO output buffer select. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1 **Value** **Description** **0x0** **open-drain output** 0x1 push-pull output

Table 38: SYS_GPIO2_1 (0x0015)

Bit	Symbol	Description
[7]	GPIO2_DEB_FALL	GPI debouce falling edge. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1
[6]	GPIO2_DEB_RISE	GPI debounce rising edge. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1
[5:4]	GPIO2_DEB	GPI debounce time. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1 **Value** **Description** **0x0** **100 µs debouce** 0x1 1 ms debouce 0x2 10 ms debounce 0x3 100 ms debounce

Bit	Symbol	Description
[3]	GPIO2_PUPD	GPIO pull-up/pull-down enable. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1 **Value** **Description** **0x0** **GPI: pull-down disabled, GPO: pull-up to AVDD disabled** 0x1 GPI: pull-down enabled, GPO: pull-up to AVDD enabled
[2]	GPIO2_POL	GPIO polarity. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1 **Value** **Description** **0x0** **GPIO is active-high** 0x1 GPIO is active-low
[1:0]	GPIO2_TRIG	GPI trigger type. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1 **Value** **Description** **0x0** **Dual-edge triggered** 0x1 Pos-edge triggered 0x2 Neg-edge triggered 0x3 Reserved (No trigger)

5.1.2 Buck1

Table 39: BUCK_BUCK1_0 (0x0020)

Bit	Symbol	Description
[6:4]	CH1_SR_DVC_DWN	Voltage slew-rate for DVC ramp-down **Value** **Description** 0x0 10 mV/8 µs 0x1 10 mV/4 µs 0x2 10 mV/2 µs 0x3 10 mV/µs **0x4** **20 mV/µs** 0x5 Reserved 0x6 Reserved 0x7 Reserved
[3:1]	CH1_SR_DVC_UP	Voltage slew-rate for DVC ramp-up **Value** **Description** 0x0 10 mV/8 µs 0x1 10 mV/4 µs 0x2 10 mV/2 µs 0x3 10 mV/µs **0x4** **20 mV/µs** 0x5 40 mV/µs 0x6 Reserved 0x7 Reserved
[0]	CH1_EN	Channel enable. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1

Table 40: BUCK_BUCK1_1 (0x0021)

Bit	Symbol	Description
[6:4]	CH1_SR_SHDN	Voltage slew-rate during shut-down **Value** **Description** 0x0 10 mV/8 µs 0x1 10 mV/4 µs 0x2 10 mV/2 µs 0x3 10 mV/µs **0x4** **20 mV/µs** 0x5 Reserved 0x6 Reserved 0x7 Immediate power-down

Bit	Symbol	Description
[3:1]	CH1_SR_STARTUP	Voltage slew-rate during startup **Value** **Description** 0x0 10 mV/8 µs 0x1 10 mV/4 µs 0x2 10 mV/2 µs 0x3 10 mV/µs **0x4** **20 mV/µs** 0x5 40 mV/µs 0x6 Reserved 0x7 Reserved
[0]	CH1_PD_DIS	Pull-down while buck is disabled. 0: enable, 1: disable

Table 41: BUCK_BUCK1_2 (0x0022)

Bit	Symbol	Description
[3:0]	CH1_ILIM	Select OCP threshold (A) **Value** **Description** 0x0 Reserved 0x1 3.5 0x2 4.0 0x3 4.5 0x4 5.0 0x5 5.5 0x6 6.0 0x7 6.5 0x8 7.0 **0x9** **7.5** 0xA 8.0 0xB 8.5 0xC 9.0 0xD 9.5 0xE 10.0 0xF Disable

Table 42: BUCK_BUCK1_3 (0x0023)

Bit	Symbol	Description
[7:0]	CH1_VMAX	VOUT max setting (V): From 0.30 V (0x1E) to 1.90 V (0xBE) in 10 mV steps. This is a read-only register. **Value** **Description** 0x1E 0.3 0x1F 0.31 0x20 0.32 Continuing through… 0x99 1.53 To… 0xBD 1.89 **0xBE** **1.9**

Table 43: BUCK_BUCK1_4 (0x0024)

Bit	Symbol	Description
[4]	CH1_VSEL	Output voltage and operation selection: 0: A, 1: B. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1
[3:2]	CH1_B_MODE	Operation mode selection. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1 **Value** **Description** 0x0 Force PFM operation 0x1 Force PWM operation (full phase) 0x2 Force PWM operation (with phase shedding) **0x3** **Auto mode**
[1:0]	CH1_A_MODE	Operation mode selection. Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1 **Value** **Description** 0x0 Force PFM operation 0x1 Force PWM operation (full phase) 0x2 Force PWM operation (with phase shedding) **0x3** **Auto mode**

Table 44: BUCK_BUCK1_5 (0x0025)

Bit	Symbol	Description
[7:0]	CH1_A_VOUT	Output voltage setting A: Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1 From 0.30 V (0x1E) to 1.90 V (0xBE) in steps of 10 mV (default 1.0 V) Write-protected when value is written below 0.30 V or above 1.90 V **Value** **Description** 0x1E 0.3 0x1F 0.31 0x20 0.32 Continuing through… **0x64** **1** To… 0xBC 1.88 0xBD 1.89 0xBE 1.9

Table 45: BUCK_BUCK1_6 (0x0026)

Bit	Symbol	Description
[7:0]	CH1_B_VOUT	Output voltage setting B: Initial value is determined by CONF pin setting at the start-up in CONF_EN = 1 From 0.30 V (0x1E) to 1.90 V (0xBE) in steps of 10 mV (default 1.0 V) Write-protected when value is written below 0.30 V or above 1.90 V **Value** **Description** 0x1E 0.3 0x1F 0.31 0x20 0.32 Continuing through… **0x64** **1** To… 0xBC 1.88 0xBD 1.89 0xBE 1.9

5.1.3 Serialization

Table 46: OTP_DEVICE_ID (0x0048)

Bit	Symbol	Description
[7:0]	DEV_ID	Device ID

Table 47: OTP_VARIANT_ID (0x0049)

Bit	Symbol	Description
[7:4]	MRC	Mask Revision Code
[3:0]	VRC	Chip Variant Code

Table 48: OTP_CUSTOMER_ID (0x004A)

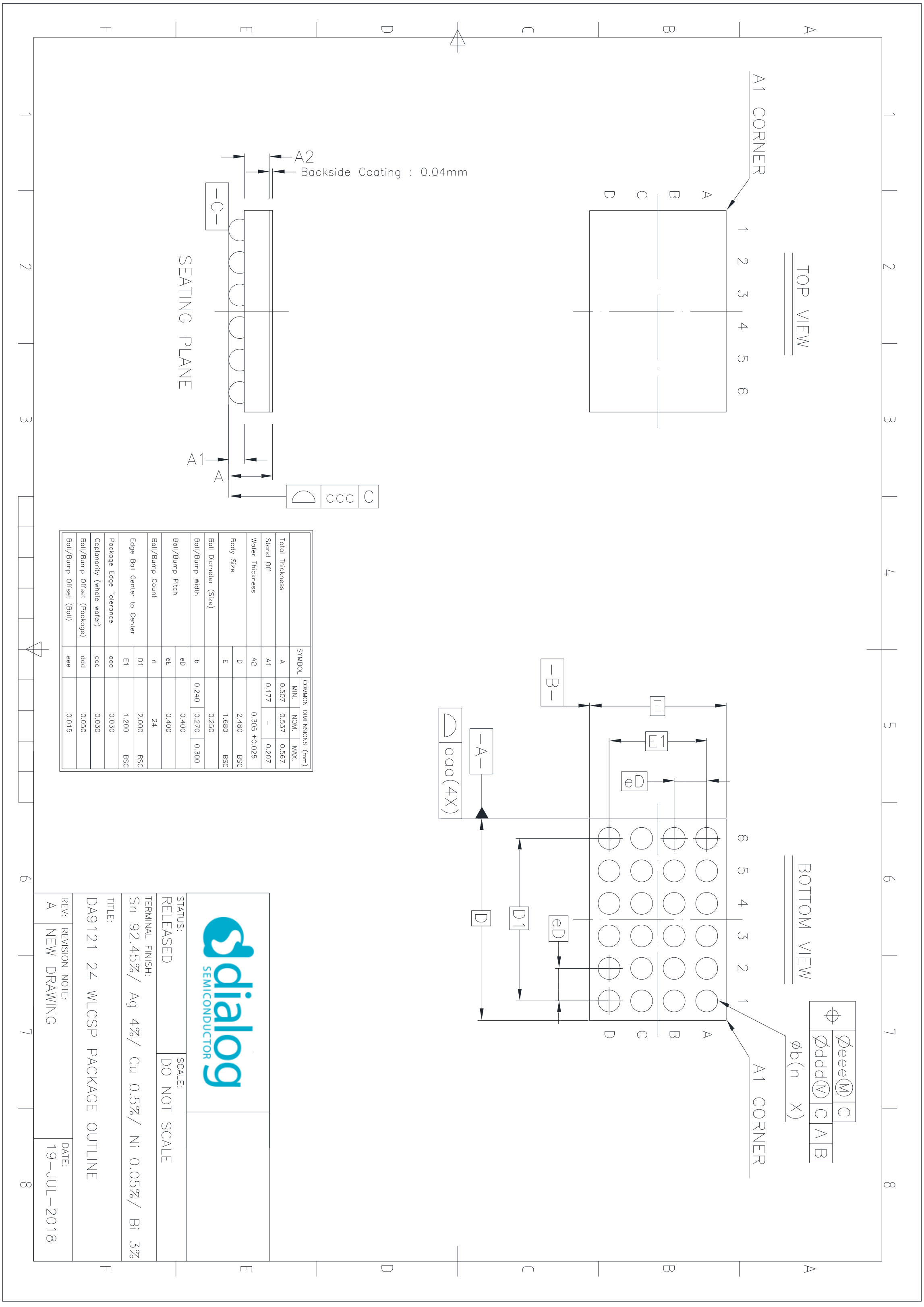
Bit	Symbol	Description
[7:0]	CUST_ID	Customer ID

Table 49: OTP_CONFIG_ID (0x004B)

Bit	Symbol	Description
[7:0]	CONFIG_REV	OTP Variant

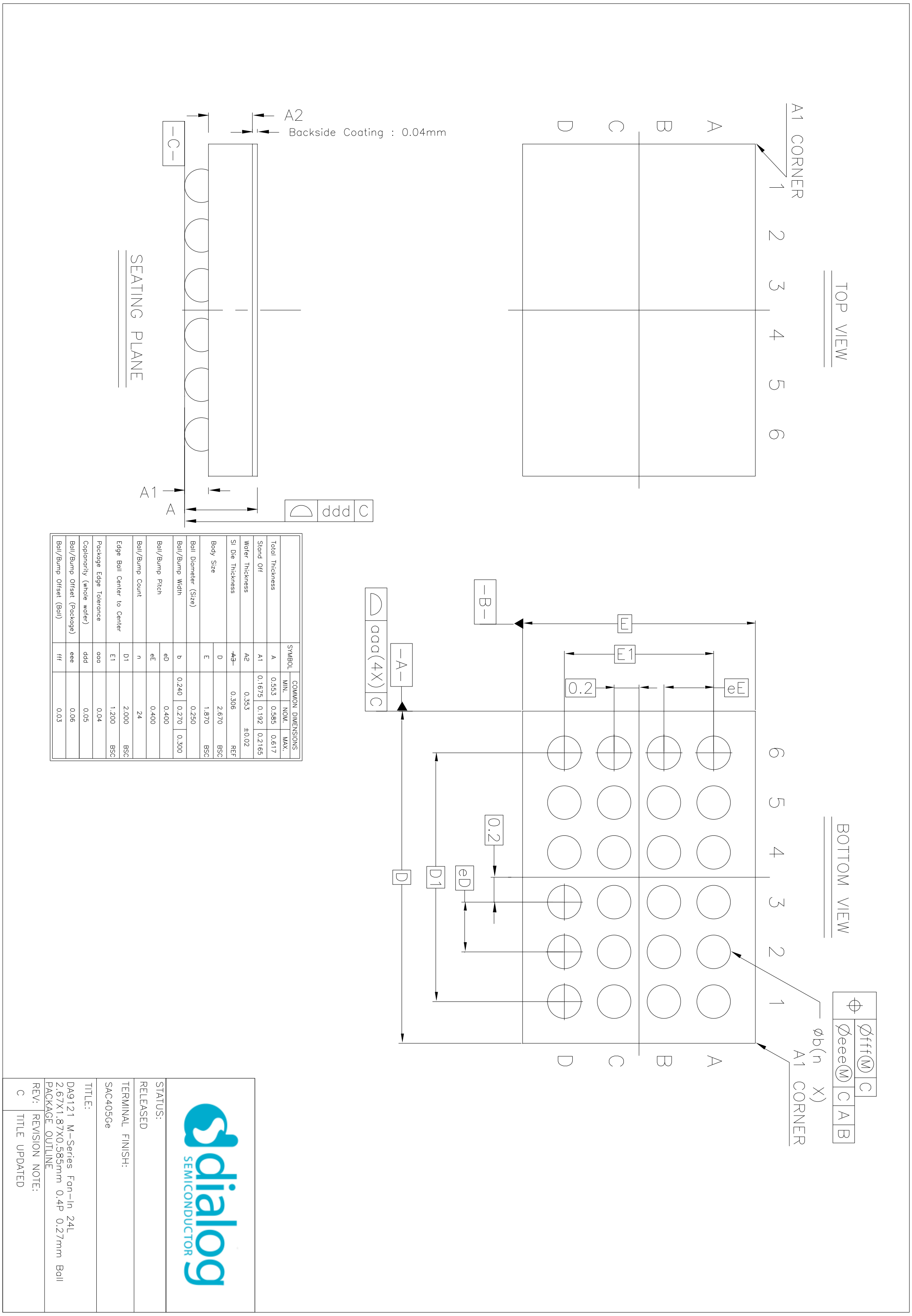
6 Package Information

6.1 Package Outlines



	SYMBOL	COMMON DIMENSIONS (mm) MIN.	NOM.	MAX.
Total Thickness	A	0.507	0.537	0.567
Stand Off	A1	0.177	–	0.207
Wafer Thickness	A2		0.305 ±0.025	
Body Size	D		2.480	BSC
	E		1.680	BSC
Ball Diameter (Size)			0.250	
Ball/Bump Width	b	0.240	0.270	0.300
Ball/Bump Pitch	eD		0.400	
	eE		0.400	
Ball/Bump Count	n		24	
Edge Ball Center to Center	D1		2.000	BSC
	E1		1.200	BSC
Package Edge Tolerance	aaa		0.030	
Coplanarity (whole wafer)	ccc		0.030	
Ball/Bump Offset (Package)	ddd		0.050	
Ball/Bump Offset (Ball)	eee		0.015	

Figure 21: WLCSP Package Outline Drawing



	SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.
Total Thickness	A	0.553	0.585	0.617
Stand Off	A1	0.1675	0.192	0.2165
Wafer Thickness	A2		0.353 ±0.02	
SI Die Thickness	~~A3~~		0.306 REF	
Body Size	D		2.670 BSC	
	E		1.870 BSC	
Ball Diameter (Size)			0.250	
Ball/Bump Width	b	0.240	0.270	0.300
Ball/Bump Pitch	eD		0.400	
	eE		0.400	
Ball/Bump Count	n		24	
Edge Ball Center to Center	D1		2.000 BSC	
	E1		1.200 BSC	
Package Edge Tolerance	aaa		0.04	
Coplanarity (whole wafer)	ddd		0.05	
Ball/Bump Offset (Package)	eee		0.06	
Ball/Bump Offset (Ball)	fff		0.03	

Figure 22: WLP Package Outline Drawing

6.2 Moisture Sensitivity Level

The moisture sensitivity level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a specified maximum temperature and a maximum relative humidity before the solder reflow process. The MSL classification is defined in Table 50.

For detailed information on MSL levels refer to the IPC/JEDEC standard J-STD-020, which can be downloaded from http://www.jedec.org.

The DA9121 package is qualified for MSL1.

Table 50: MSL Classification

MSL Level	Floor Lifetime	Conditions
MSL 1	Unlimited	≤30 °C / 85 % RH

6.3 Package Handling

Manual handling of WLCSP packages should be reduced to the absolute minimum. In cases where it is still necessary, a vacuum pick-up tool should be used. In extreme cases plastic tweezers could be used, but metal tweezers are not acceptable, since contact may easily damage the silicon chip.

Removal of a WLP or WLCSP package will cause damage to the solder balls. Therefore a removed sample cannot be reused.

WLCSP packages are sensitive to visible and infrared light. For light sensitive applications, the WLP package should be used.

6.4 Soldering Information

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from http://www.jedec.org.

7 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult Dialog Semiconductor's customer support portal or your local sales representative.

Table 51: Ordering Information

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
DA9121-xxV72	24 WLCSP	2.5 x 1.7	T&R	4500
DA9121-xxV76	24 WLCSP	2.5 x 1.7	Waffle Tray	140
DA9121-B0V72 Standard OTP Variant V_{OUT1} = 1.0 V	24 WLCSP	2.5 x 1.7	T&R	4500
DA9121-B0V76 Standard OTP Variant V_{OUT1} = 1.0 V	24 WLCSP	2.5 x 1.7	Waffle Tray	140
DA9121-xxOZ2	24 WLP	2.7 x 1.9	T&R	TBD
DA9121-xxOZ6	24 WLP	2.7 x 1.9	Waffle Tray	TBD
DA9121-B0OZ2 Standard OTP Variant V_{OUT1} = 1.0 V	24 WLP	2.7 x 1.9	T&R	TBD

8 Application Information

The following recommended components are examples selected from requirements of a typical application.

8.1 Capacitor Selection

Ceramic capacitors are used as bypass capacitors at all VDD and output rails. When selecting a capacitor, especially for types with high capacitance at smallest physical dimension, the DC bias characteristic has to be taken into account.

Table 52: Recommended Capacitor Types

Application	Value	Size	Temp. Char.	Tol. (%)	V-Rate	Type
VOUT output bypass	10 µF	0402	X5R ±15 %	±20	6.3 V	Murata GRM155R60J106ME15
PVDDx bypass	10 µF	0603	X5R ±15 %	±20	25 V	Murata GRM188R61E106MA73
AVDD bypass	1 µF	0402	X5R ±15 %	±10	10 V	Murata GRM155R61A105KE15

8.2 Inductor Selection

Inductors should be selected based on the following parameters:

- Rated maximum current

  Usually a coil provides two current limits: ISAT specifies the maximum current at which the inductance drops by 30 % of the nominal value, and IMAX is defined by the maximum power dissipation and is applied to the effective current.
- DC resistance

  Critical for the converter efficiency and should therefore be minimized.

Table 53: Recommended Inductor Types

Value (µH)	Size (mm)	I_{MAX} (DC) (A)	I_{SAT} (A)	Tol. (%)	DC Resistance (mΩ)	Type
0.1	2.0 x 1.6 x 1.0	6.5	9.0	±20	11.5	Cyntec HTEN20161T-R10MDR
0.1	1.6 x 0.8 x 1.0	5.2	6.5	±20	17	Taiyo Yuden MEKK1608TR10M
0.1	1.6 x 0.8 x 0.8	4.1	9.4	±20	19	Taiyo Yuden MCHK1608TR10MJN
0.11	2.0 x 1.25 x 0.8	5.8	6.9	±20	9.1	Taiyo Yuden MCHK2012TR11MKG
0.1	2.5 x 2.0 x 1.2	12	13	±20	4	TDK TFM252012ALMAR10MT
0.1	1.6 x 0.8 x 0.95	3.8	4.3	±20	15	Tokyo Coil Engineering TFP160810M-R10N
0.11	2.0 x 1.6 x 0.6	3.0	6.0	±20	24	Wurth Elektronik WE-PMMI 744 799 771 11

High-Performance, 10 A, Dual-Phase DC-DC Converter

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.dialog-semiconductor.com.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

Disclaimer

RoHS Compliance

Dialog Semiconductor's suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

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