General description

iW6401 is a highly versatile digital processor IC for off-line LED drivers in smart lighting applications. With its high degree of configurability it can serve as a platform for a wide range of digital dimming LED applications.

Multiple dimming interfaces connect the iW6401 to home or building automation systems: I^2C-bus, DLT receiver (IEC 62756 compliant), light switch on/off events using a configurable state machine. Lamp dimming curves are programmable.

iW6401 can serve as a power front-end for wireless communication modules, intelligent sensors or generic microcontrollers. An integrated LDO provides a stable supply voltage for external peripherals.

All operating parameters and functions are configurable using unique multi-write OTP programming. Digital control loops provide precise control of both input power and light output. A high power factor can be achieved while maintaining stable and flicker-free light across an ultra-wide dimming range.

iW6401 can actively manage lamp temperature using on-chip or off-chip sensors and a configurable state machine. Accurate temperature settings permit thermal optimization of the lamp design to reduce the cost of cooling parts. Other system supervision functions such as short circuit and open load can be easily configured via register settings.

iW6401 can be configured for AC supply voltages ranging from 90 V to 264 V. It is available in a small leadless DFN12 package.

Although the iW6401 offers ultimate flexibility with full programmability most applications will use predetermined data for programming for fastest time to market. Reference designs can be used to verify ready-made memory profiles.

Key features

- High performance wide range dimming engine
- Quasi-resonant (soft) switching
- Patented PrimAccurate™ LED current control
- IEC62756 data receiver & bypass load
- I2C dimming and control interface
- Programmable dimming curves
- OTP configuration memory
- Software controlled standby/wakeup
- Toggle-switch event driven state machine
- Regulated power for external master
- Programmable soft start
- End-of-Line diagnostics and calibration
- Small leadless 4x4 mm DFN12 package
- Active PFC control with High Power Factor
- Open/short protection with auto-restart
- State machine based temperature de-rating
- Internal/External temperature sensor
- Input overvoltage protection

Applications

- Dimmable retrofit LED bulbs
- Dimmable linear LED tubes
- Standalone AC supply driven LED drivers
- Wireless dimmable LED bulbs and drivers
- IEC62756 compatible LED bulbs and drivers
- Lamps with integrated smart sensors

System and Application diagram

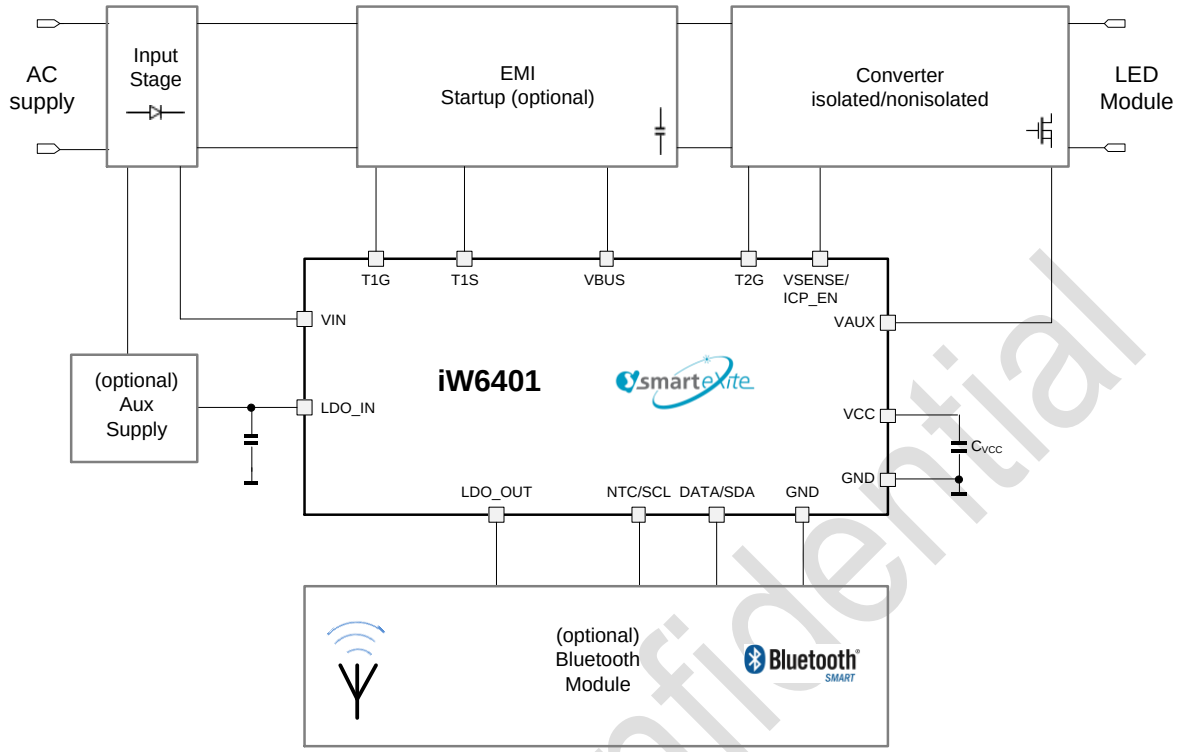

Figure 1: iW6401 system diagram

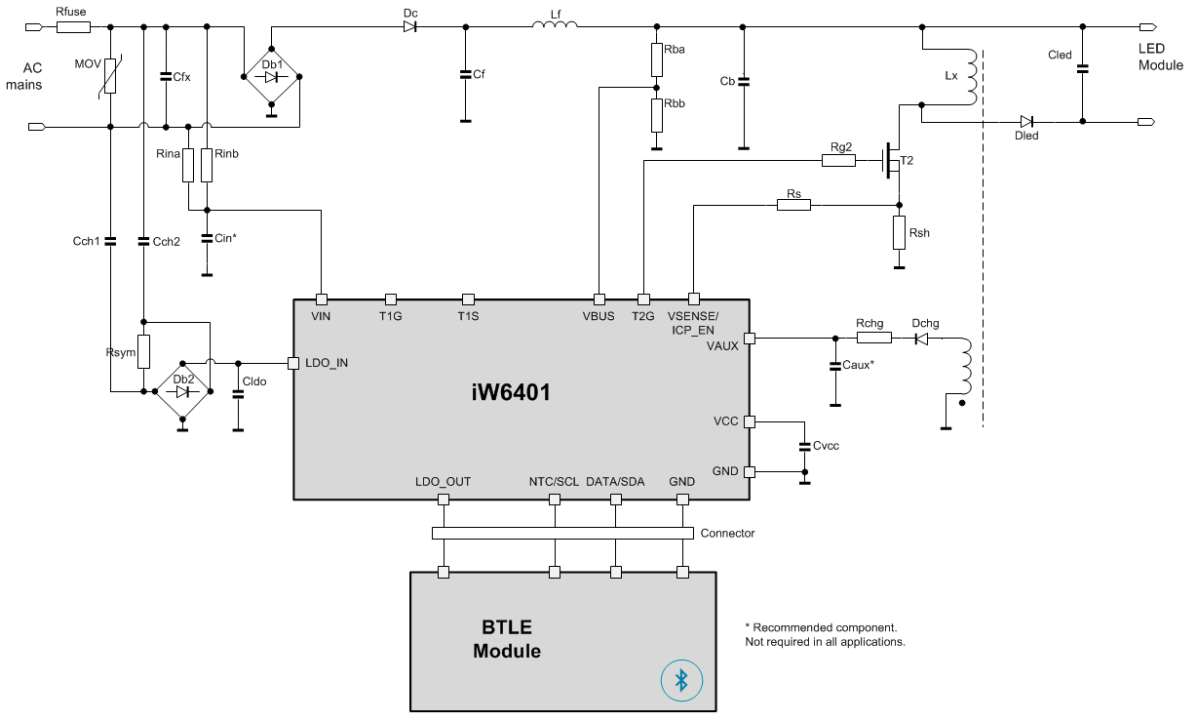

Figure 2: iW6401 typical application

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1 Terms and definitions

DCM	Discontinuous Conduction Mode
DLT	Digital Load Side Transmission (according to IEC 62756-1)
EoL	End of Line (production line)
ICP	In-Circuit Programming
LDO	Low Drop-Out (regulator)
LED	Light Emitting Diode
MCU	Microcontroller
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NTC	Negative Temperature Coefficient (thermistor)
OTP	One Time Programmable (memory)
PFC	Power Factor Correction
PSRR	Power Supply Rejection Ratio
PWM	Pulse Width Modulation
LFPWM	Low Frequency Pulse Width Modulation
SELV	Safety Extra Low Voltage
SOA	Safe Operating Area
SSM	System State Machine
QR	Quasi Resonant (switching mode)

2 References

1. The I^2C-bus specification v2.1, Philips Semiconductors, 9398 393 40011, 2000.
2. I^2C-bus specification and user manual v4.0, NXP Semiconductors, UM10204, 2012.
3. IEC 62756, Digital load side transmission lighting control (DLT) - Part 1: Basic requirement.
4. Bluetooth Module Specification
5. Bluetooth Smart Communication Standard

3 Block diagram

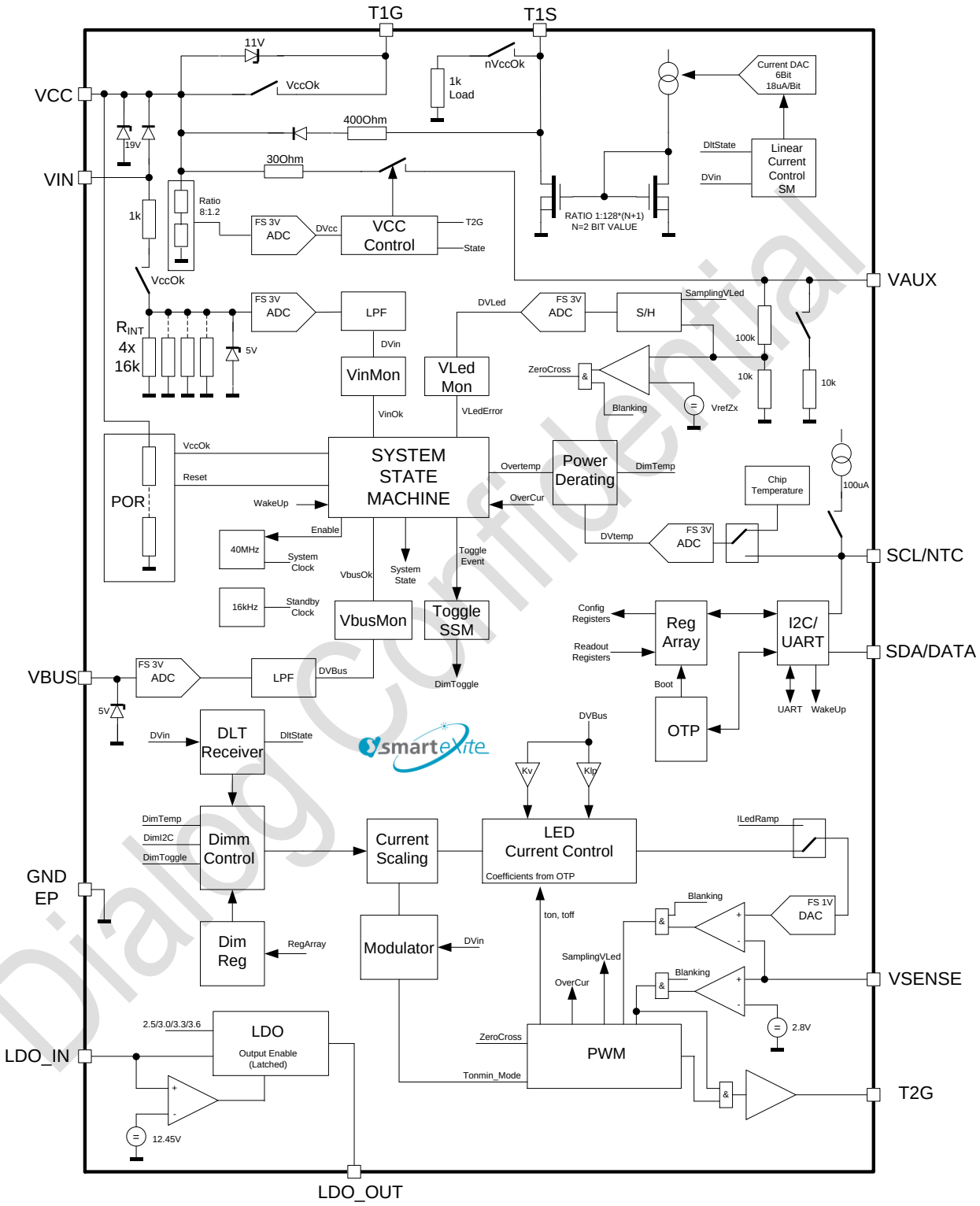


Figure 3: iW6401 block diagram

3.1 Functional Overview

The following chapter summarize all functions of the control chip. More detailled descriptions of each of the subfunctions are given in the corresponding chapters.

Startup and chip power supply

The chip is started up via two parallel methods: passive startup via the upper resistor of the VIN voltage divider and active startup through the external bypass load MOSFET. Active startup is used whenever the external MOSFET is fitted. For active startup the gate of the external bypass load MOSFET is pulled up by a high value resistor limited by an 11V zener allowing current through T1S pin into VCC. Once VCC reaches the turn-on threshold active startup is disabled by connecting the T1G pin to VCC and setting the internal current source to zero. The passive startup is disabled by connecting VIN to the internal load resistor. Once the flyback is in operation chip power is provided through VAUX by controlling the charging switch between VAUX and VCC. The maximum VCC is monitored and if above the programmable limit the charging control switch is disabled. The charging switch alternatings with flyback cycles to allow V_{LED} measurements, the alternating pattern can be configured. Whenever the flyback is in “ton_min” mode charging is enabled every cycle. The amount of charging in each cycle is controlled by setting ton_min, the external charging resistor at VAUX and the actual VAUX voltage.

The switches in the block diagram are set according to the VccOk signal. VccOk is asserted when the VCC reaches the turn-on level Vcc (~17V) and remains asserted until the VCC crosses the lower threshold Vcc (~10V). The capacitor at VCC is recomended to be a minimum of 10µF.

Flyback Operation

The flyback converter stage is operated in two different modes: peak current regulation and ton_min.

1.) Peak current regulation:
The primary peak current is regulated such that the average LED current meets the control setpoint. The control setpoint is created by the current scaling module which translates a relative light level into a current set value. When dimmed, the magnitude of the LED current is reduced until a tripping point is reached. From there on the current is kept constant but the flyback is LFPWM controlled to toggle between peak current mode and ton_min mode.

2.) Ton_min
In this mode the flyback is operated with a constant ton/toff switching signal at the gate of the flyback MOSFET. Both values are programmable. Depending on the programmed setpoint and the design of the auxiliary winding, the VCC supply is powered during ton_min mode.

The detailled operation of both modes is outlined in their corresponding chapters.

During peak current regulation the flyback is protected against overcurrent via a dedicated comparator at VSENSE. The overcurrent detection acts in two different ways: exceeding the overcurrent limit at VSENSE immediately turns off the flyback MOSFET. If consecutive overcurrent events are observed the state machine can be configured to shutdown.

The input voltgae of the flyback converter is monitored against over- and under-voltage to maintain a safe operating condition. VBUS is monitored and the flyback converter is enabled / disbled under control of the system state machine.

Flyback Peak Current Regulation

The peak of the primary current is regulated by means of a dynamic reference voltage provided from a DAC. The digital setpoint of the DAC is generated by a PI-type control loop. The input of the control loop is the difference between the light level as requested by the current scaling unit (LightLevelSet) and the calculated value of the LED current. Please refer to the corresponding chapter on the details

of the control loop calculation. The regulator output can further be modulated by two independent linear gain factors in order to achieve high PSRR to the bus voltage and/or active PFC mode. The control coefficients for the PI control loop are programmable and can have different values for both high and low dim levels.

Current Scaling Unit

The current scaling unit implements the transfer characteristic as shown in the diagram below:

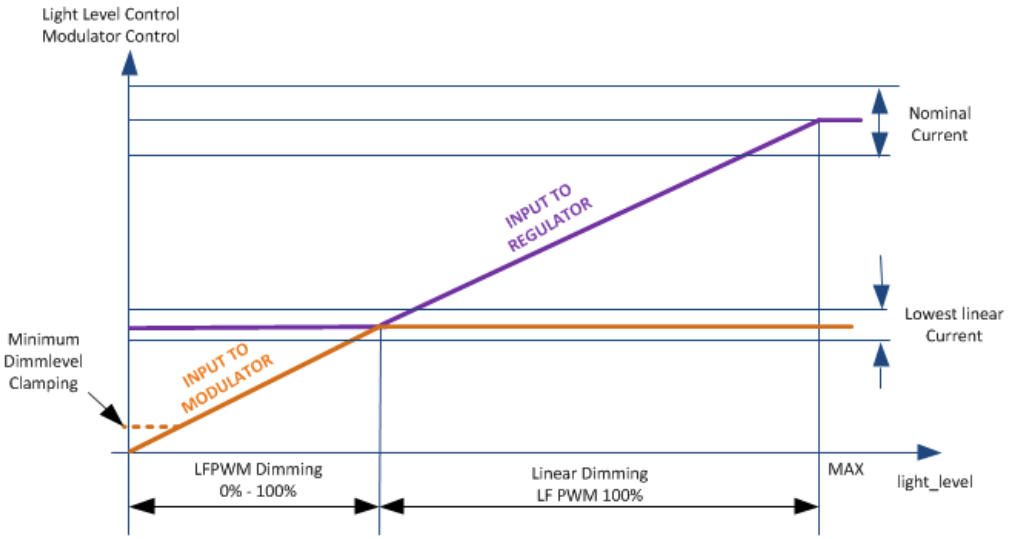


Figure 4: Scaling of LED Current vs. Dim-Level

The input relative light level is defined as a 10-bit value. The output of the scaling unit is a 10-bit setpoint value for the PI control loop. Below a programmable lowest current value, the scaling unit generates an 8-bit value for the LFPWM modulation. Between the maximum and lowest linear current the setpoint value is linearly scaled, below this limit the PWM is linearly scaled to give a resultant linear mapping from input to output. A dim-level clamping value can be set to keep the LED light above a minimum level.

Dim Control Unit:

Several sources can influence the light level which sets the LED output current:

- Data received via DLT
- Data received via I2C, serial
- Dimming setpoint from light-switch control
- Light modulation generated by the end of line programming
- Light Level as requested by the temperature derating unit

The dim control unit combines all data into one relative light level that feeds into the scaling unit. Inside the dim control block low pass filtering is applied to the relative light level to maintain smooth change of light. The filter frequency can be programmed. Data interpolation is applied to the DLT data input and the light-switch data input. This allows the user to calibrate the corresponding dim-curves for a smooth dimming experience.

Power Derating: An internal or external temperature sensor can be selected to perform temperature control. The measured temperature dependant voltage is converted to a digital value and processed in the power derating unit. The module implements a programmable state machine to reduce output power when the system reaches programmable temperature thresholds. A programmable maximum temperature shut-down can be configured to protect the system from overheating.

V_{IN} processing: During start up the external resistors connected to VIN is a charging path to VCC. During run mode a potential divider is formed between the external and the internal resistor. The internal resistor value is programmable.

In run mode the VIN signal is used to:

1.) Monitor the status of AC supply (light switch)
2.) Receive DLT data
3.) Control the bleed state machine
4.) Synchronize the Flyback LFPWM

VIN is digitised by an 8-bit ADC with a 3V full scale range.

V_{BUS} processing:

VBUS is connected to an external potential divider and the voltage digitised by an 8-bit ADC with a 3V full scale range. The digitized values are low-pass filtered to reduce noise. VBUS is used to control the following functions:

1.) PSRR of PI control loop
2.) Active PFC control
3.) VBUS over- and under-voltage protection

OTP and System Clock: The iW6401 has two independent system clocks: 16kHz for controlling the system during low power (standby mode) operation and 40 MHz for the digital processing during normal (run mode) operation.

The OTP memory contains the configuration data, allowing the device to be setup in the application to give the best possible operation; this also allows variations in the external components to be compensated.

The OTP memory is accessible via both I2C/Serial and EoL programming. The iW6401 has default values for all user registers; wherever default values are applicable to the application no reprogramming is required.

***Important**: Changing OTP memory has an effect on the chip operation and invalid settings for a given application can lead to destructive system conditions.*

I2C/Serial Interface

This provides access to the register array via I2C or single-pin serial communication; SDA/SCL and DATA are used as communication pins respectively. For both communication protocols an external pull-up resistor is required – a value between 1.5kΩ and 4.7kΩ is recommended (depending on the communication speed).

The I2C interface operates at 100kHz (standard-mode), 400kHz (fast-mode), 1MHz (fast-mode plus). The iW6401 is configured as a slave device.

The Serial interface is configurable over a wide range of operating speeds.

Changing register settings "on the fly" while the chip is active can lead to invalid configurations which can lead to destructive system conditions.

Source Controlled MOSFET driver (SCMD)

This uses the bypass load MOSFET as a linear bleed current with an internal current source. The current profile is controlled via a programmable state machine. The source controlled driver is only active during the run mode of the chip. By default the state machine is programmed to serve as a bypass load according to the DLT specification IEC62756.

Whenever the chip is in standby mode, for example during start up, the external MOSFET is used for active start up.

The SCMD has 4 ranges each with 6-bits of current resolution; this results in an 8-bit value setting both range and current. The state machine can be configured for independent currents where state transitions are triggered based on VIN voltage and/or timeout.

LDO

A linear voltage regulator provides power to an external controller (MCU/Bluetooth/etc.). The output voltage can be set to be 2.5 V, 3 V, 3.3 V or 3.6 V. The LDO can be programmed to keep the output voltage disabled until the LDO_IN input has reached a threshold value of 12.5V; this allows the load to draw higher currents during initialization by using the stored charge in the decoupling capacitor.

Zero Cross and V_{LED}/VCC control

The voltage on VAUX serves multiple functions:

1.) To establish QR operation of the flyback converter

2.) To charge VCC via a low impedance switch

3.) Monitoring the LED voltage during peak current regulation

Typically the voltage applied to this pin is generated by an auxiliary winding of the flyback converter transformer. The winding must be designed to have positive voltage levels during the period where the energy of the flyback converter is transferred into the LED. The target voltage level shall be proportional to the LED voltage and shall have a level of typically 25V. The transformer winding is connected to the chip via a current limiting resistor and a diode. Any potential ringing on the auxiliary winding must be clamped external to the chip to avoid any voltage overstress.

The different functions of the VAUX are controlled by a programmable alternating pattern of measure and charge cycles.

During measure cycle the VAUX input is internally loaded by a 10kΩ resistor in order to discharge any parasitic pin capacitance. An internal 11:1 potential divider is used to measure and sense the VAUX voltage. A comparator with a programmable reference triggers on the negative going edge to detect the zero-crossing of the flyback current; this establishes quasi resonant mode of the converter. The divided VAUX voltage digitised by an 8-bit ADC with a 3V full scale range, this sampled voltage is proportional to the LED voltage.

During charge cycles the internal switch between VAUX and VCC is activated in order to charge the decoupling capacitor. Due to the fact that Vaux is now connected to VCC, detection of zero cross is no longer possible. The timing for the flyback switching and the V_{LED} voltage uses the values from the most recent measure cycle.

During 'ton_min' mode only charge cycles are executed as all measurements are not required as there is no power transferred to the LED.

The VCC voltage is monitored and the system keeps this within its upper and lower limits.

Whenever VCC reaches its upper threshold the internal charging switch is disabled as no more charging is required.

Whenever Vcc reaches its lower threshold the 'ton_min' is changed to a higher value in order to provide more charging current. An effective average 'ton_min' is established by letting the system sweep between these two levels. This is a self-adaptive control to overcome any tolerance issues related to 'ton_min' switching.

System State Machine

All iW6401 operating states are managed by the system state machine. Based on system events and timeouts, state transitions are triggered. The detailed state chart is given in the corresponding chapter.

Based on the detection of light switch events (a short AC supply off/on switch event) a dimming request is transferred to the dim control unit.

When a light switch is used to control the LED lamp, this block manages the timing of AC supply off/on period and uses a programmable state machine to dim the lamp according to the selected method. Eight states can be used to configure combinations of steps/levels or ramps of LED light level.

DLT Receiver

Receives modulated data via the AC supply input, this supports telegrams to control the LED current according to IEC 62756.

For good reception the VIN signal has to make full use of the 3V input range. Care must be taken in designing PCB layout to have low noise signals to reduce coupling from the flyback switching. The default register values can be used in most cases to get low reception error rates.

4 Chip Configuration and Programming

4.1 Pinout

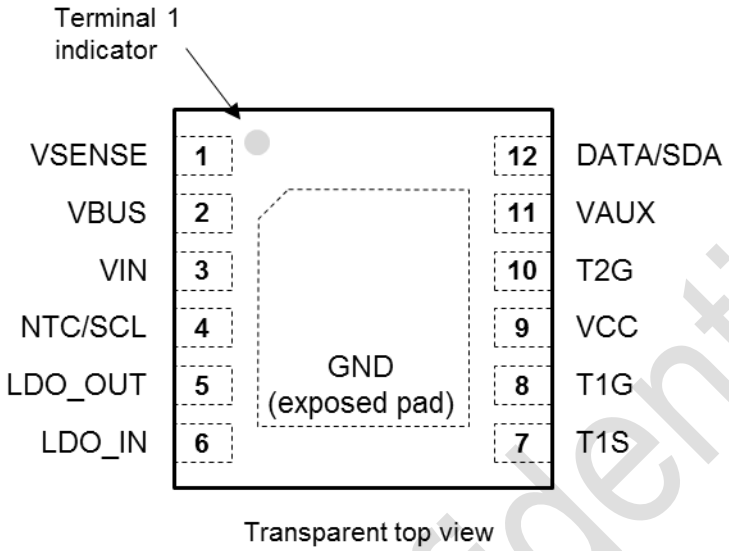


Figure 5: Connection diagram DFN12 package

Table 1: Pin description

Pin no.	Pin name	Type (Table 2)	Description
1	VSENSE	AI	Current sense input for flyback current.
2	VBUS	AI	Voltage sense input for flyback input voltage. Digitised by an 8-bit ADC with a 3V full scale range.
3	VIN	HVI	AC supply voltage sense input. During start up this pin is used to charge VCC via a input resistor. Digitised by an 8-bit ADC with a 3V full scale range.
4	NTC SCL	AI DI	Input for external NTC temperature sensor. Connected to an internal current source of 100 µA. Digitised by an 8-bit ADC with a 3V full scale range. I^2C-bus clock input. Requires external pull-up resistor. When used as NTC input, I2C cannot be used.
5	LDO_OUT	AO	Output of LDO regulator. Programmable output voltage of 2.5V, 3.0V, 3.3V or 3.6V
6	LDO_IN	HVI	Input for LDO regulator. Input voltage range from 5V to V_{CC_LIM}. Input threshold detect at 12.5V
7	T1S	HVO	Control signal for bypass load MOSFET. Connects to the source of the external MOSFET.
8	T1G	HVO	Control signal for bypass load MOSFET. Connects to the gate of external MOSFET.
9	VCC	PS	Supply voltage (typ. 15 V). Requires external decoupling capacitor of 10µF to GND.
10	T2G	HVO	Control signal for flyback MOSFET. Connects to the gate of external MOSFET.

Pin no.	Pin name	Type (Table 2)	Description
11	VAUX	HVI	Auxiliary voltage sense input. Connected to auxiliary winding of flyback transformer. Additionally used to charge VCC in run mode.
12	DATA SDA	DIO DIO	Serial data interface input/output. Requires external pull-up resistor. I^2C-bus data input/output. Requires external pull-up resistor. When used as NTC input, I2C cannot be used.
Exposed pad	GND	-	Ground (0V). Common ground for all functions. Must be connected to PCB ground plane for thermal management.

Table 2: Pin type definition

Pin type	Description	Pin type	Description
DI	Digital Input	AI	Analog Input
DIO	Digital Input/Output	PS	Power Supply
HVI	High Voltage Input	HVO	High Voltage Output
AO	Analog Output		

Note:

1. The I2C and serial data interfaces have no internal pull-up resistors, When SDA/DATA or SCL pins are not used, connect them to GND or via a 100kΩ resistor to GND if communication interface is removable.
2. If the bypass load is not used, leave pins T1G and T1S open.
3. If the VBUS input is not used, connect the pin to GND.
4. If the LDO is not used, connect LDO_IN to GND and leave LDO_OUT open.

4.2 Internal circuits

4.2.1 Pin VCC: supply voltage

The VCC pin is the supply voltage (typically 15V) of the iW6401. All other supply voltages are generated internally, the analog circuits operating at approximately 5V. No external components are needed, except for the VCC decoupling capacitor, typically 10 µF.

When VCC exceeds V_{CC_LOCK} (17V) the iW6401 switches to run mode.

When VCC drops below V_{CC_UVLO} (10V) the iW6401 switches to standby mode.

4.2.2 Pin DATA/SDA

The DATA/SDA pin is used for both I2C and serial data input/output. It has a Schmitt trigger input with enable function. The input circuit is designed to operate with external devices at supply voltages ranging from 2.5V to 5V; with a typical threshold voltage of 1.2 V.

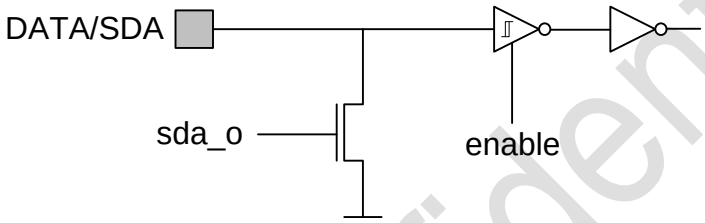


Figure 6: Pin DATA/SDA internal circuit

4.2.3 Pin NTC/SCL

The NTC/SCL pin has an internal current source of 100µA and is typically connected to an external 10kΩ or 22kΩ NTC thermistor, which gives a voltage between 0V and 3V (corresponding with the ADC range) at the temperatures of interest. This allows the temperature of the LED substrate to be measured and the output power to be controlled to maintain the maximum operating temperature; typically this is set at 85°C for an optimal LED life time.

Internally, the NTC voltage is digitised by the ADC with a 3V full scale range, and the resulting digital value logically inverted to give a positive slope with temperature, for use with the temperature event state machine and look-up table. Since the 100 µA current source is internally supplied at 5V, the digitised code at low temperatures will be 00h (after inversion).

The NTC/SCL pin is used for the I2C clock input. It has a Schmitt trigger input with enable function. The input circuit is designed to operate with external devices at supply voltages ranging from 2.5V to 5V; with a typical threshold voltage of 1.2 V.

When the 100µA current source is turned on, the Schmitt trigger input is disabled.

Note: In I^2C interface mode either uses the internal temperature sensor or uses an external processor to sense the temperature and control the relevant registers to reduce the output power and/or turn off the LED drive.

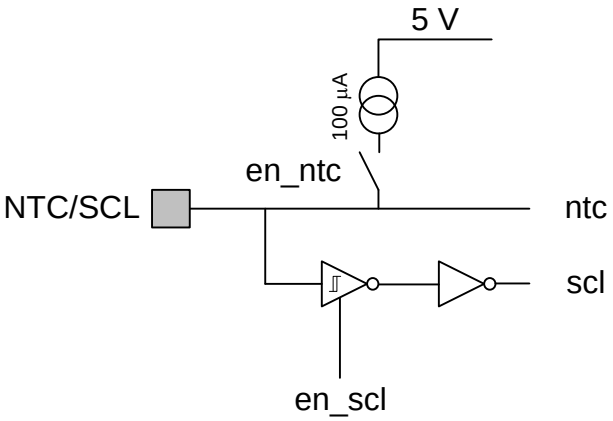


Figure 7: Pin NTC/SCL internal circuit

4.2.4 Pins T1G and T1S: source controlled MOSFET driver

The iW6401 contains a Source Controlled MOSFET Driver (SCMD) at pins T1G (gate) and T1S (source) to realise the bypass load function. This is a programmable current source with the additional circuitry to give the fast charge capability. The output current has four ranges: up to 125mA, 250mA, 375mA and 550mA. Within each current range a 6-bit control parameter (ISET) sets the current in linear steps. This function controls the AC supply load current during DLT dimming. The current range and setting are programmable via the corresponding registers of the DLT state machine.

In standby mode the switch across the zener is opened and pin T1G is pulled approximately 11V above VCC to turn on the external MOSFET, while pin T1S charges the VCC decoupling capacitor via an internal diode (and a 400Ω resistor to limit the current). In run mode the switch is closed and T1G is connected to VCC.

The following table lists the typical SCMD current values for Cur_Value, for all four Cur_Range=0,1,2,3.

	Iscmd (mA)			
Value	Range=0	Range=1	Range=2	Range=3
0	0.0	0.0	0.0	0.0
1	3.7	7.3	11.0	14.6
2	6.6	13.3	19.9	26.6
3	9.5	19.0	28.4	37.9
4	12.2	24.4	36.6	48.8
5	14.9	29.7	44.6	59.5
6	17.5	35.0	52.5	70.0
7	20.1	40.1	60.2	80.2
8	22.6	45.2	67.8	90.4
9	25.1	50.2	75.3	100.4
10	27.6	55.2	82.8	110.4
11	30.1	60.1	90.2	120.2
12	32.5	65.0	97.5	130.0
13	34.9	69.9	104.8	139.7
14	37.3	74.7	112.0	149.3
15	39.7	79.5	119.2	158.9
16	42.1	84.2	126.3	168.4
17	44.5	88.9	133.4	177.8
18	46.8	93.6	140.5	187.3
19	49.2	98.3	147.5	196.6
20	51.5	103.0	154.4	205.9
21	53.8	107.6	161.4	215.2
22	56.1	112.2	168.3	224.4

	Iscmd (mA)			
Value	Range=0	Range=1	Range=2	Range=3
23	58.4	116.8	175.1	233.5
24	60.7	121.4	182.1	242.8
25	63.0	126.0	188.9	251.9
26	65.3	130.5	195.8	261.0
27	67.5	134.9	202.4	269.9
28	69.8	139.6	209.3	279.1
29	72.0	144.0	216.0	288.0
30	74.3	148.5	222.8	297.1
31	76.5	153.0	229.5	306.0
32	78.7	157.4	236.1	314.8
33	80.9	161.9	242.8	323.7
34	83.2	166.4	249.6	332.8
35	85.4	170.8	256.2	341.6
36	87.6	175.2	262.8	350.4
37	89.8	179.6	269.4	359.2
38	92.0	184.0	276.0	368.0
39	94.2	188.4	282.6	376.8
40	96.4	192.8	289.2	385.6
41	98.6	197.2	295.7	394.3
42	100.8	201.6	302.4	403.2
43	102.9	205.8	308.7	411.6
44	105.1	210.2	315.3	420.4
45	107.3	214.6	321.9	429.2
46	109.4	218.8	328.2	437.6
47	111.6	223.2	334.8	446.4
48	113.7	227.4	341.1	454.8
49	115.9	231.8	347.7	463.6
50	118.0	236.0	354.0	472.0
51	120.2	240.4	360.6	480.8
52	122.3	244.6	366.9	489.2
53	124.4	248.8	373.2	497.6
54	126.6	253.2	379.8	506.4
55	128.7	257.4	386.1	514.8
56	130.8	261.6	392.4	523.2
57	132.9	265.8	398.7	531.6
58	135.0	270.0	405.0	540.0
59	137.1	274.2	411.3	548.4
60	139.3	278.6	417.9	557.2
61	141.4	282.8	424.2	565.6
62	143.5	287.0	430.5	574.0
63	145.6	291.2	436.8	582.4

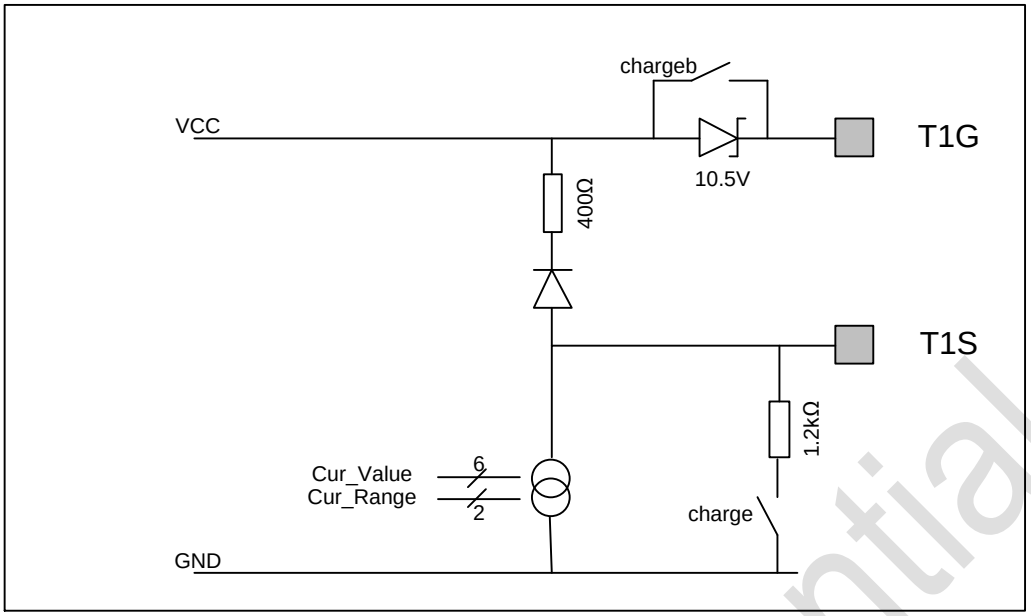


Figure 8: Pins T1G and T1S internal circuit

4.2.5 Pin T2G: flyback driver output

The T2G pin is a push-pull driver operating from the VCC supply voltage, driving the gate of the external flyback MOSFET. The driver has a typical source impedance of 50Ω.

4.2.6 Internal temperature sensor

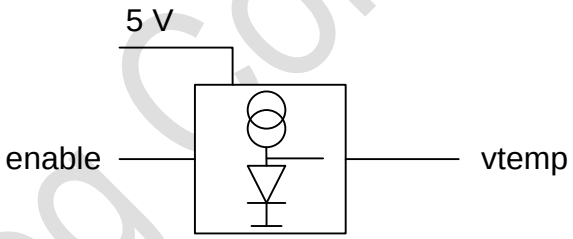


Figure 9: Internal temperature sensor

The internal temperature sensor is available for power de-rating and safety shutdown. The high and low temperature thresholds are programmable using the corresponding registers in the temperature event state machine.

Note: In order to select an external NTC as the temperature sensor the register TEMP_NTC has to be set accordingly. The external NTC sensor value or the internal temperature sensor value can be used by the temperature control state machine and is used for power de-rating. The internal temperature sensor is always used for the over-temperature shut down.

Register	Description
TEMP_NTC	Configure system for use of external temperature sensor. I2C cannot be used for communication.

4.2.7 Pins LDO_IN, LDO_OUT

The internal voltage regulator (LDO) supplies power to an external wireless module or microprocessor for remote control of the LED dimming. The regulator requires a minimum load capacitance of 10µF on pin LDO_OUT.

The LDO has a programmable output voltage of 2.5V, 3.0V, 3.3V or 3.6V. Internally the driver stage is supplied from VCC and only the output stage from pin LDO_IN. This allows the dissipated power in the output stage to be optimised depending on the load current requirement.

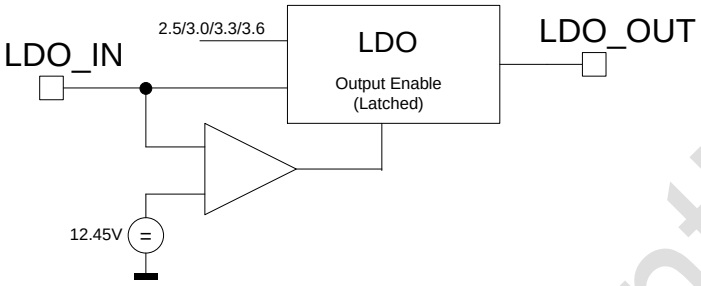


Figure 10: Pins LDO_IN and LDO_out internal circuit

The LDO output current can be up to 500mA for V_{LDO_IN} = 15 V and V_{CC} = 15 V. Figure 11 shows the rated output current capability as a function of V_{CC} for V_{LDO_IN}=5V. Below VCC=10V the current capability drops until the output is limited by the input supply voltage. Note that any external circuit that requires power to maintain operation when VCC<10V must limit its operating current (i.e. use a sleep mode).

The total dissipated power (P_{TOT}) for the DFN12 package must be limited to keep the junction temperature below 125°C. Refer to application guidelines for PCB design recommendations.

	LDO setting			
VCC	*2.5*	*3*	*3.3*	*3.6*
17	>500mA	>500mA	>500mA	>500mA
15	>500mA	>500mA	>500mA	>500mA
12	>500mA	>500mA	>500mA	>500mA
10	>100mA	>100mA	>100mA	>100mA
9	>100mA	>100mA	>100mA	>100mA
8	>100mA	>100mA	87mA	43mA
7	>100mA	33mA	5mA	3,34V
6	15mA	2.70V	2.70V	2.70V

Figure 11: Typical LDO output current vs. V_{LDO_IN} and V_{CC}

Configuring the LDO

The LDO is configured using the register LDO_CONFIG.

The following options can be configured:

- Output voltage (2.5, 3.0, 3.3, 3.6V)
- Select LDO_IN threshold detect before activating the output
- Enable LDO

Register	Description
LDO_CONF	Configuration for LDO mode and output voltage.

4.3 Pin T2G: flyback driver output

The T2G pin is a push-pull driver operating from the VCC supply voltage, driving the gate of the external flyback MOSFET. The driver has a typical source impedance of about 35Ω.

4.4 Vin and Vbus Sense

The VIN input has 2 functions: to charge the VCC capacitor on start-up and standby mode, and provide AC supply voltage information in run mode.

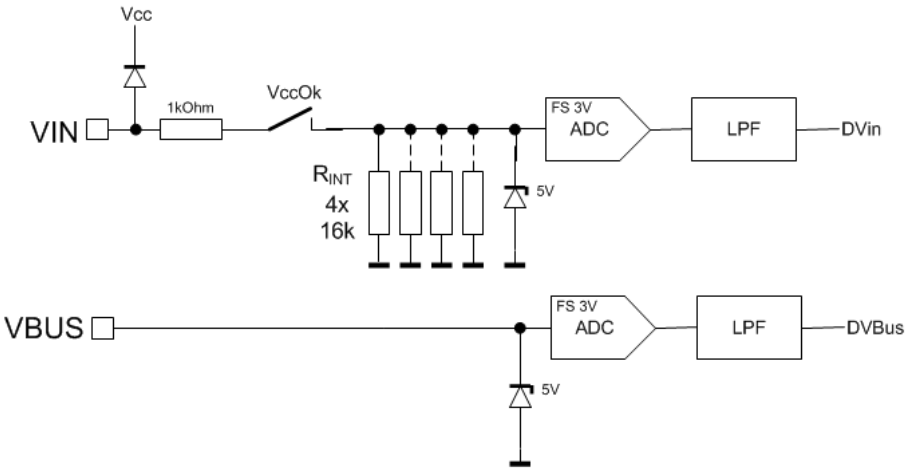


Figure 12: Vin and Vbus Sensing Scheme

This block also contains the input circuitry for the VBUS pin.

The VBUS input digitizes the supply voltage to the fly-back converter; this is used as an input to the PI control loop in order to increase the PSRR to Ac supply voltage fluctuations. It requires an external potential divider as the voltage digitized by the ADC with a 3V full scale range.

The VIN input charges the VCC voltage when the RIN switch is open on start-up and standby mode. in run mode the switch is closed and the internal RIN forms a potential divider with the external resistor. The table shows the resistances that can be selected:

Table 3: Selection of Resistors at Pin Vin

Ctrl	*RIN*
000	16kΩ
001	8kΩ
011	5.33kΩ
111	4kΩ

Register	Description
VIN_RESISTOR_SELECT	Select one configuration for the Vin divider.

4.5 Pin VSENSE

The VSENSE/ICP_EN pin is used to monitor the coil current in the flyback output stage via an external sense resistor. The pin has a peak coil current comparator programmable from 0 to 1V (set by the PI control loop) and an overcurrent detection comparator programmable from 0 to 3V.

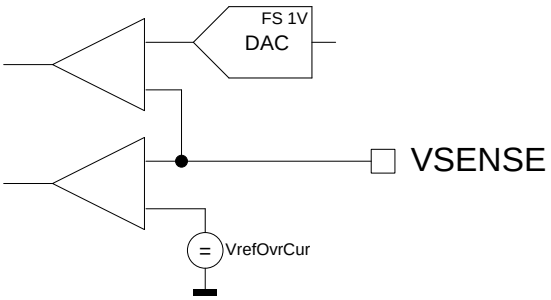


Figure 13: Pin VSENSE

The overcurrent protection continuously monitors the peak current and immediately turns off the flyback MOSFET in overcurrent conditions. When the overcurrent condition remains for a longer time, the system state machine enters the stop mode.

4.6 VAUX

The VAUX pin has three functions: to detect the coil zero-current condition to establish QR switching operation; to measure the LED voltage; to provide power to VCC.

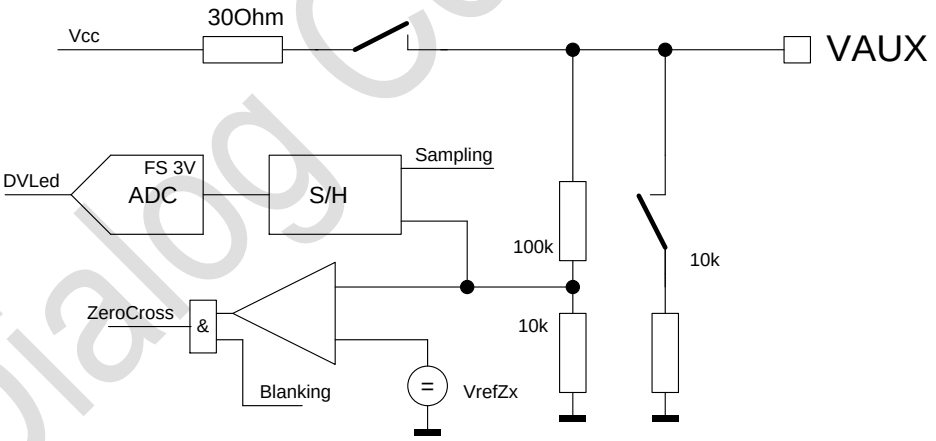


Figure 14: Internal circuit at Vaux

The VAUX input has a HV switch to isolate the input from the VCC supply; this allows the VAUX to be independent of VCC without taking any current. When the switch is open, the VAUX input is loaded by a fixed 10kΩ resistor to ensure that the measured signal follows the voltage of the auxiliary winding.

During measure cycles the zero cross of the secondary current of the converter is detected by sensing the falling edge at VAUX. The measurement and zero-cross comparator are connected to an 11:1 potential divider, so giving a 32V input capability at the pin.

The reference value for the zero cross detection is set using the register VAUX_VREF_ZX.

The divided voltage at Vaux is sampled and held using a fixed time delay after the negative edge of T2G. The time is set using the register VAUX_TSTART_SHVLED. Please be aware that the real LED voltage is measured indirectly and several terms have to be taken into account to scale this to the actual voltage:

- The voltage drop across 2 diodes
- The internal voltage divider
- The turns ration between Nsec and Naux
- The 8-bit ADC conversion with 3V full scale

In order to prevent from premature detection of zero cross a blanking time is set after the falling edge of T2G. During this time no zero cross event is detected.

The logic that controls the Vaux processing switches between charge and measure cycles. During measure cycles a normal zero-cross is performed and the V_{LED} is measured. During charge cycles the switch to VCC is closed and no sensing takes place. The default register settings does a sequence of 1 measure and 3 charge cycles.

Register	Description
VAUX_VREF_ZX	Set the reference voltage for the zero cross
VAUX_TSTART_SHVLED	Set the sampling time for the LED voltage
VAUX_BLANK_OFF	Set the blanking times for zero cross.

5 Absolute maximum ratings

Table 4: Absolute maximum ratings

Symbol	Parameter	Conditions	Min	Max	Unit
T_{STG}	storage temperature		-65	150	°C
T_J	junction temperature		-40	+125	°C
V_{CC_LIM}	limiting supply voltage	Pin: VCC	-0.3	25	V
V_{HV_LIM}	limiting voltage (HV pins)	Pins: T1S T1G (5mA max) T2G VIN (5mA max) VAUX LDO_IN	 -0.3 VCC-0.3 -0.3 -0.3 -0.3 -0.3	 VCC+5 32 VCC+0.3 VCC+5 32 32	 V V V V V V
V_{LV_LIM}	limiting voltage (LV pins)	Pins: DATA/SDA, NTC/SCL, VBUS, VSENSE	-0.3	5.5	V
I_{CC_MAX}	maximum supply current	V_{CC} = 25 V	-	30	mA
V_{ESD_HBM}	electrostatic discharge voltage	Human Body Model; JS-001-2012, Class 1B	-2000	+2000	V
V_{ESD_CDM}	electrostatic discharge voltage	Charged Device Model; JESD22-C101C, Class II	-500	+500	V

Stresses beyond those listed under “Absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6 Recommended operating conditions

Table 5: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_J	junction temperature		-30	-	125	°C
T_{JPROG}	junction temp for chip programming	any OTP write access	-30		85	°C
V_{CC}	supply voltage		12	15	17	V
V_{LDO_IN}	Regulator supply			15		V
V_{IN_RAMP}	input voltage during start up	supply ramp up	-0.3	-	V_{CC}+5	V
V_{IN_OPER}	input voltage during operation	Operating	-0.3	-	3.6	V
V_{AUX}	auxiliary winding voltage		-0.3	-	28	V
V_{SENSE}	current sensing voltage		-0.3	-	1.1	V
V_{BUS}	Bus voltage sensing		-0.3	-	3.6	V
P_{DIS}	Expected power dissipation	V_{CC}=15V, V_{LDO_IN}=15V V_{LDO_OUT}=3.0V, 2mA load No SCMD current V_{AUX}=28V, 50% duty		120		mW

7 Electrical characteristics

Table 6: Electrical characteristics

Unless otherwise stated, T_J=-30°C to +125°C. Typical T_J=25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply (pin VCC)						
V_{CC_LOCK}	lock-in supply voltage	Initial power up Re-start after switch event	16.5 -1%	17.2 17.0	18.0 +1%	V V
V_{CC_UVLO}	under-voltage lock-out supply voltage		-1%	10.0	+1%	V
V_{CC_CL}	clamping supply voltage		-	18.5	-	V
R_{CC_CL}	Clamping resistance			5		kΩ
V_{CC_POR}	power-on reset		-1%	5.0	+1%	V
I_{CC}	supply current	Active state	-	3.3	5	mA
I_{CC_OFF}	off-state supply current	Vcc charge state	-	35	70	µA
C_{DEC_VCC}	decoupling capacitance	from pin VCC to GND; V_{CC} = 15 V; Note 1	3.3	10	100	µF
AC supply sensing (pin VIN)						
V_{ADC_VIN}	ADC conversion range		0	-	3	V
V_{IK_VIN}	input clamp voltage	I_{IN} = 1 mA	5.5	-	5.9	V
I_{IK_VIN}	input clamp current	V_{IN} = 5 V	-	-	0.26	mA
I_{CHG_VIN}	charge current (V_{CC})	V_{IN} < 32 V; V_{CC} = 15 V	-	-	5	mA
$R_{I\_VIN\_NOM}$	input resistance	V_{IN} = 3 V; T_J = 25 °C; VIN_RESISTOR_SELECT=0	15.2	16	16.8	kΩ
$R_{I\_VIN\_TC}$	TC of input resistance	$R_{VIN}=(TC2*(T_J-25)^2 + TC1*(T_J-25))*R_{I\_VIN\_nom}$		-2.5e-5 4.3e-7		/°C /(°C)^2
SCMD control (pins T1G and T1S)						
I_{Z_T1G}	zener current	V_{T1G} < 32 V; V_{CC} = 15 V	-	-	5	mA
V_{Z_T1G}	zener voltage	T_J = 25 °C I_{Z_T1G}=5mA	9.6	10.5	11.1	V
$V_{Z\_T1G\_TC}$	TC of zener voltage			-23		mV/°C
I_{CHG_T1S}	charge current (V_{CC})	V_{T1S} = VCC+5 V; V_{CC} = 15 V	-	-	20	mA
R_{DLT}	DLT load during power up	V_{CC} < V_{CC_LOCK}		1.2		kΩ
I_{S_T1S}	source current	CUR_RANGE = 00b; IDAC = 100000b; V_{CC} = 15 V; V_{T1S}=10V; T_J = 25 °C	73	76.5	81	mA
I_{S_R0}	source current DLT_CUR_RANGE = 0	IDAC=01d		2.93		mA
I_{S_R1}	source current DLT_CUR_RANGE = 1	IDAC=01d		5.86		mA
I_{S_R2}	source current DLT_CUR_RANGE = 2	IDAC=01d		8.79		mA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{S_R3}	source current DLT_CUR_RANGE = 3	IDAC=01d		11.72		mA
$I_{S\_MAX\_T1S}$	maximum source current	V_{T1S} = 10 V; T_{J_MAX} must not be exceeded	500	560	-	mA
I_{S_TC}	TC of source current			-0.035		%/°C
Flyback sensing (pin VSENSE)						
V_{OV_SNS}	Over-voltage threshold	Default value		1.0		V
I_{I_VSENSE}	input leakage current (pin VSENSE/ICP_EN)	V_{SENSE} = 1 V	-	-	0.1	µA
Flyback control (pin T2G)						
R_{OH_T2G}	HIGH level output resistance	$V_{T2G} = V_{CC}$ – 0.3 V; V_{CC} = 15 V	22	35	58	Ω
R_{OL_T2G}	LOW level output resistance	V_{T2G} = 0.3 V; V_{CC} = 15 V	21	32	54	Ω
Bus voltage sensing (pin VBUS)						
V_{ADC_BUS}	ADC conversion range		0	-	3	V
I_{IK_VBUS}	input clamp current	V_{BUS} = 5 V	0.26	-	-	mA
I_{I_VBUS}	input leakage current (pin VBUS)	V_{BUS} = 3 V	-	-	0.1	µA
Auxiliary winding sensing (pin VAUX)						
VDR_{VAUX}	voltage divider ratio		10.8	10.9	11.0	ratio
V_{ADC_AUX}	ADC conversion range	After voltage divider	0	-	3	V
R_{L_VAUX}	Internal load impedance	V_{AUX} = 3 V to 25 V; V_{CC} = 10 V to 17.5 V	8.5	9.2	10	kΩ
R_{SW_CHG}	charge switch resistance	V_{CC} = 15 V; I_{CHG} = 10 mA	20	32	55	Ω
NTC current source (pin NTC/SCL)						
I_{O_NTC}	NTC output current	R_{NTC} = 20 kΩ	96	99	102	mA
V_{ADC_NTC}	ADC conversion range		0	-	3	V
I_{I_NTC}	input leakage current	NTC current source disabled	-	-	0.1	µA
Digital input/output pins						
V_{IH}	HIGH level input voltage	Pins: DATA/SDA, NTC/SCL	2.25	-	3.96	V
V_{IL}	LOW level input voltage	Pins: DATA/SDA, NTC/SCL	-	-	0.3	V
V_{OL}	LOW level output voltage	Pin DATA/SDA; I_{OL} = 2 mA	-	0.37	0.6	V
LDO regulator						
V_{IT_LDO}	input threshold voltage		-2%	12.5	+2%	V
V_{LDO_2V5}	LDO output voltage	MODE = 00b	2.43	2.5	2.58	V
V_{LDO_3V0}	LDO output voltage	MODE = 01b	2.91	3.0	3.09	V
V_{LDO_3V3}	LDO output voltage	MODE = 10b	3.20	3.3	3.40	V
V_{LDO_3V6}	LDO output voltage	MODE = 11b	3.49	3.6	3.71	V
I_{LDO_10V}	LDO output current	V_{LDO_IN} = 15 V; V_{CC} = 10 V T_{J_MAX} must not be exceeded			100	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{LDO_15V}	LDO output current	V_{LDO_IN} = 15 V; V_{CC} = 15 V T_{J_MAX} must not be exceeded			500	mA
System						
f_{CLK_HS}	high speed clock frequency	main system clock		40		MHz
	TC of system clock			+0.045		%/°C
f_{CLK_LS}	low speed clock frequency	event counter clock	-3%	16	+3%	kHz
	TC of event clock			+0.078		%/°C
ADC_{range}	ADC conversion range	Code 00h Code FFh	 -1%	0 3.0	 1%	V
ADC_{DNL}	ADC DNL	VIN, VBUS NTC, VTEMP, VAUX	-2 -1		2 1	LSB LSB

Note 1 Decoupling capacitor value is application dependent.

8 Thermal characteristics

Table 7: Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{TH(J-A)}$	thermal resistance from junction to ambient	iW6401 mounted on PCB	74	°C/W

Note 1 A detailed description of the thermal performance and PCB layout requirements will be given in an application note. Contact Dialog for example PCB layout.

The exposed pad of the chip must be soldered on a grounded copper plane with a minimum area of 50mm^2.

The total power dissipated inside the chip is given by:

(i) The power dissipation of the signal processing system
(ii) The power losses inside the LDO supply the external communcation module
(iii) The power dissipated inside the source controlled mosfet driver.

Given by the thermal coupling to the environment and the power dissipated inside the chip temperature is set and may not exceed the maximum rated chip temperature at any time.

9 Functional description

9.1 Overview

The iW6401 uses a single stage flyback configuration to convert the AC supply voltage into a DC current for driving LEDs. A true dimming range from 100 % down to 1 % is realised by linearly reducing the flyback current and at low dimming levels by pulse width modulation.

The integrated Source Controlled MOSFET Driver can be used as a bypass load current sink or load current shunt for DLT dimming applications.

All analog input and output signals are digitally controlled. Multiple 8-bit ADC channels with a 3V full scale are used. State machines control the operation of the various functions. Two internal oscillators (16kHz and 40MHz) provide the clock signals for the digital core.

Precise control of the LED current uses patented numerical methods, including measurement of the flyback input voltage (V_{BUS}) to improve the Power Supply Rejection Ratio (PSRR). This reduces visible LED noise (flicker) even at high AC supply voltage variations and substantially extends the dynamic range of the bus voltage allowing the use of small capacitors.

Dimming can be controlled via light switching, via a serial/I2C data interface or via an IEC 62756 Digital Load side Transmission (DLT) slave interface.

An integrated LDO regulator provides a programmable supply voltage between 2.5 V and 3.6 V for peripheral devices such as wireless communication modules, microcontrollers or intelligent sensors.

Configuration settings are controlled via registers which have default reset values, any register value can be changed by storing the new value in OTP (loaded during power up). Additionally any register can be changed by the serial/I2C interface. The OTP can be programmed via the serial/I2C interface. This allows pre-assembly calibration of the LED driver circuit. Post-assembly calibration of the LED lamp is supported via a AC supply modulation interface.

The iW6401 can be configured for different AC supply voltages between 90 V to 260 V by choosing appropriate external HW components.

9.2 Register read/write and OTP Programming

All functions inside the iW6401 are fully programmable. Programming can be done on 2 levels:

(i) Reading / Writing to the register array using I2C communication. Register can be read and written any time also during operation of the device. A range of registers is available to read internal values. Please refer to the register map for more details.
Any content of the register array is overwritten the next time the device resets and all register values will be overwritten by OTP values.
This mode is very convenient to optimize the system on the fly by changing values during normal operation. Once a correct system configuration is found the values can be programmed into OTP.

(ii) The OTP is organized as a freeform memory where each entry has an address and data information. The address can be any register. During startup of the device at first all registers are set to their default values. Then during initialization the content of the OTP is read and all corresponding registers are updated inside the Register array.

For both cases an ICP programmer us used together with a control SW that allows access to each individual register. A detailed description of all registers can be found in the USER memory map.

To protect any programming a locking scheme can be used. Please refer to the corresponding application note about locking features.

9.2.1 System State MachineSystem States

All operating modes of the chip are controlled via the main system state machine. The system state machine receives event signals from various external blocks and changes states accordingly. Each state uses one of three power modes:

- **Reset Power mode**: V_{CC} below startup level, power-on reset active
  - States: PowerOn
- **Low Power mode**: V_{CC} above startup level, event clock active, flyback stage not active
  - States: VccCharge, Stop, Sleep
- **Normal Power mode**: V_{CC} within locking range, system and event clocks active, flyback stage active
  - States: SystemInit, RampVbus, RampVled, Run, MainsOff

  The total power consumption in Normal Power mode depends on the activated features, operating frequencies and the applied power MOSFETs.

The state diagram in Figure 15 shows the power modes and how they are related via events and conditions.

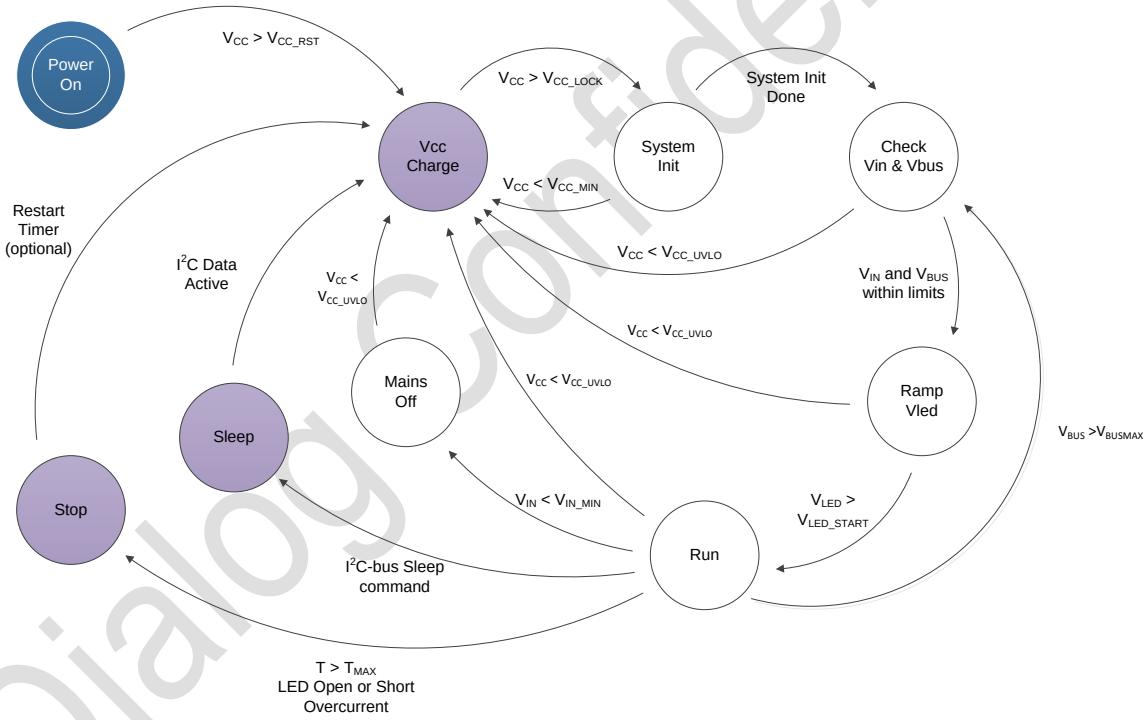


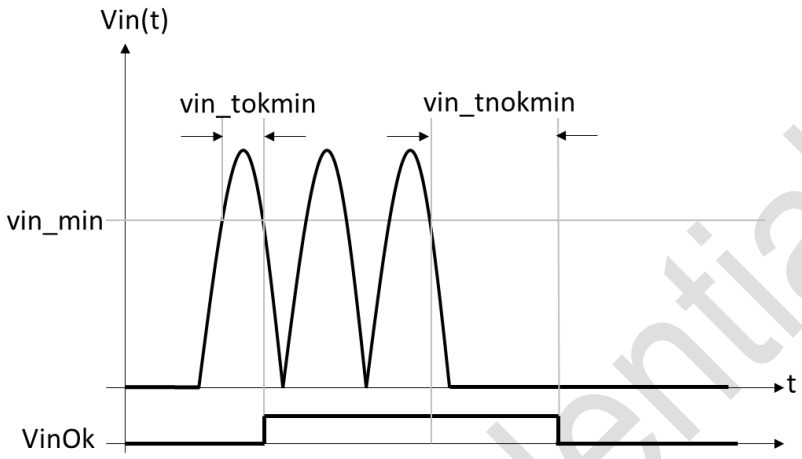
Figure 15: Power modes state diagram

Legend:

- Dark Blue: Reset Power mode
- Cyan: Low Power mode
- White: Normal Power mode

9.2.2 Configuring the state machine

When the chip is first powered on Vcc is charged up via either the external resistor at VIN or via the external active startup MOSFET or a combination of both. The state machine operates under control of several system flags:

VinOk	 **Figure 16: Vin turn on conditions** VIN is converted to an 8-bit digital value with 3V full scale. A digital low-pass filter is applied to the samples for noise filtering. VinOk is asserted when the VIN signal is above the 'vin_min' value for more than 'vin_tokmin' time and de-asserted when it is below the 'vin_min' value for more than 'vin_tnokmin' time. Default values are 'vin_tokmin' = 1ms and 'vin_tnokmin'=4.8ms. Note for correct start-up operation, 'vin_tokmin' should be greater than 100us
VccOk	Asserted whenever VCC crosses above the V_{CC_LOCK} threshold and is de-asserted whenever Vcc crosses below the V_{cc_UVLO} threshold.
VbusOk	Asserted whenever VIN_VBUS_MIN, <= VBUS <= VIN_VBUS_MAX. VBUS is converted to an 8-bit digital value with 3V full scale. A digital low-pass filter is applied to the samples for noise filtering. Default values are 'vin_vbus_min' = 0 and 'vin_vbus_max'=3V.
VLedOk	Asserted whenever VAUX_VLEDMIN, < VAUX < VAUX_VLED_MAX Please refer to the Vaux description for details on the Vled measurement principles. Default values are 'vaux_vledmin' = 14.4V and 'vaux_vledmax'=30.8V.
Overcurrent	Asserted whenever the primary peak current exceeds the protection threshold. See the overcurrent protection section for more details.
OverTemp	Asserted whenever the chip temperature exceeds the upper limit.

VccCharge

At a voltage level of V_{CC_POR} the system executes a Power-On-Reset and the state machine enters the VccCharge state. In this state the chip is set to low power consumption (I_{CC_OFF}). The event clock is active (typ. 16kHz) and the system is waiting for Vcc to reach the turn on threshold.
The active startup is set into charging mode to allow Vcc to be raised to the turn on threshold.

This state is also entered whenever the system is restarting from a previous shutdown condition or when Vcc is discharged below the lock out threshold of V_{CC_UVLO}.
Please refer to the state chart above for more details.

SystemInit

Whenever Vcc reaches the turn on threshold of V_{CC_LOCK} the state machine enters the SystemInit state. In this state the system clock is turned on and the chip enters the normal power mode. During SystemInit the OTP memory is loaded into the register array. The total initialisation procedure takes typically less than 2ms.

Check Vin&Vbus

In the state Check Vin & Vbus the state machine waits for both signals VBUS and VIN to reach the turn-on condition indicated by the corresponding VinOk and VbusOk flags.

Ramp VLed

In this state the converter is turned on for the first time. In order to allow for a rapid charging of the output voltage the converter is driver with a fixed ipeak/toff setting for the primary current control. This allows fast charging of the output.

A fixed reference level is applied to the reference voltage of the PWM unit to limit the current and a fixed off-time is the applied to transfer the current into the output.

The state terminates whenever the minimum LED voltage is reached or when a timeout condition is met. The maximum time is programmed in SSM_T_RAMP_FLYBACK.

The peak current is programmed in FLY_IPK_RAMP and the corresponding off-time is set in FLY_TOFF_RAMP.

The state terminates whenever the measured LED voltage is above VAUX_VLEDMIN.

Run

In run state the system is in normal operation and the state machine remains in this state until failure condition applies. Failure conditions are:

(i) Chip over-temperature

(ii) LED over-voltage

(iii) LED under-voltage

(iv) Primary over-current

(v) VBUS out of range (min/max)

(vi) Loss of VIN input voltage

Mains Off

Whenever VinOk is de-asserted the state machine stops the converter and waits for Vcc to be discharged below the turn off threshold. In this state the chip remains in normal power mode to discharge quickly below the under-voltage lockout threshold.

Sleep

Sleep mode is only entered via a corresponding command from I2C communication interface; write regED=04h.

This mode is a low-power mode and the chip remains in this mode indefinitely waiting for a restart event. A re-start event is 2 consecutive rising edges on the DATA pin within a half-period of the event clock; this is normally triggered by sending at least 4 consecutive edges faster then $2*f_{CLK\_LS}$.

Please refer to the description of I2C communication for more details

Stop

Whenever a failure mode is detected the state machine enters stop state. This state is a low power mode and the chip remains in this mode waiting for a restart event. After the (optional) restart time has elapsed, the system attempts to start again.

Register	Description
VIN_MIN	Minimum V_{IN} threshold voltage
VIN_VBUS_MIN	V_{BUS} lower threshold voltage
VIN_VBUS_MAX	V_{BUS} upper threshold voltage
VAUX_VLEDMAX	Maximum V_{LED} threshold voltage
VAUX_VLEDMIN	Minimum V_{LED} threshold voltage
VIN_TOKMIN	Minimum VinOK=1 time in 4µs steps
VIN_TNOKMAX	Minimum VinOK=0 time in 64µs steps

9.3 Oscillators

The iW6401 operates using two independent oscillators: a fast clock which is active in normal power mode and a slow clock which is always active, except during system reset. Both oscillators are factory-trimmed to their rated accuracy.

9.4 System startup

During startup the iW6401 is supplied from the AC supply via external series resistors at pin VIN and if used via the external bleeder MOSFET. The supply voltage V_{CC} is clamped at typ. 18.5 V and must be decoupled to ground via an external capacitor, typ. 10µF. When the flyback converter stage is active, the iW6401 is supplied from the auxiliary transformer winding via pin VAUX.

In case that an external MOSFET is present as the DLT bleeder this can be used to fast start the device when using decoupling capacitors with higher values.

Charging of VCC via the auxiliary winding is controlled by the iW6401 to maintain voltage within the lock-in and lock-out levels. Only a diode and a current limiting resistor are needed on the VAUX pin, minimizing the component count substantially.

9.4.1 Passive start up

At start up the iW6401 is supplied from the AC supply via the sense resistors at pin VIN. Passive start up can be used for simple low end applications where no external MOSFET is connected to T1S, T1G.

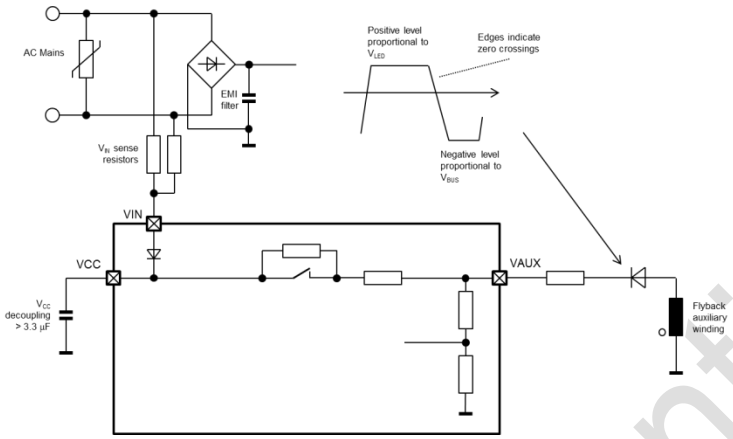


Figure 17: Power supply with passive startup

9.4.2 Active start up

When the V_{CC} decoupling capacitance is too large for charging via the sense resistors, active start up can be realised via the external MOSFET which is controlled by the SCMD (source controlled MOSFET driver). During start up the gate is pulled high via a high impedance resistor of typically 2MΩ; when T1G reaches the threshold voltage of the external MOSFET, the drain current charges VCC through T1S. The current is limited by an internal 400Ohm resistor. This allows very fast start up even with large decoupling capacitor values on VCC.

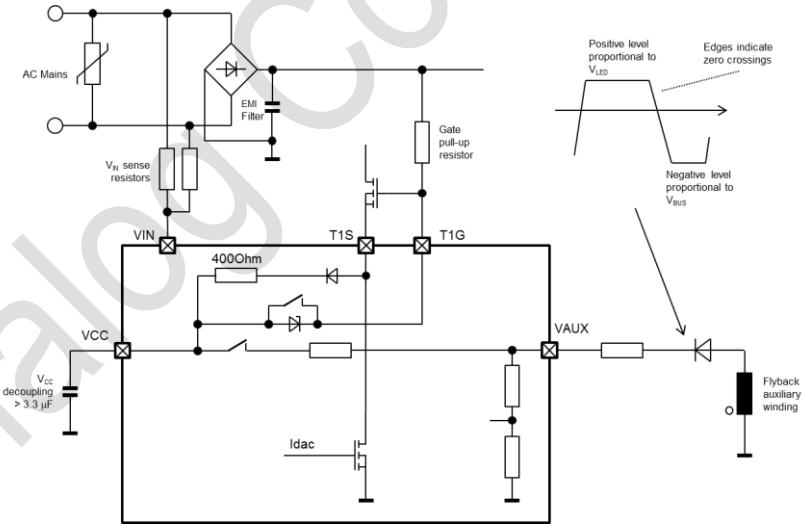


Figure 18: Power supply with active startup

9.4.3 Vcc Clamping

VCC is charged until it reaches the V_{CC_LOCK} threshold. At this point the T1G is internally connected to VCC and stops the charging current; also VIN is now connected to an internal resistor in order to form a voltage divider to measure the input AC supply signal. The internal resistor can be programmed to different values with register VIN_REGISTER_SELECT between 4kΩ and 16kΩ.

If VCC is charged higher than V_{CC_LOCK} an internal shunt resistor switches on at V_{CC_CL}.

9.4.4 Vcc Control

During startup VCC is charged through the external resistor connected to VIN (passive start up) and can also be charge by the external MOSFET connected to T1S/T1G (active start up).
Vcc is charged until the V_{CC_LOCK} level is reached. At this point the system state machine is started (see the chapters on startup and system state machine).
Due to the increase of I_{cc} after starting, V_{cc} will discharge until the flyback is in operation, when V_{cc} is charged from the auxiliary winding via an internal switch between VAUX and VCC. The amount of charge is given by the open circuit voltage of the auxiliary winding as well as the external current limiting resistor. In operation VCC is charged until the V_{CC_MAX} threshold is reached, this level is programmable. Once this level is reached the internal charging switch is turned off. If the charging of VCC through VAUX is too low, which can be the case at very low dim-levels, VCC drops until it is below the threshold V_{CC_MIN}. At this point the t_{on_min} control parameter of the flyback PWM modulator is increased; which increases the charging to VCC until the $V_{CC\_MIN\_UP}$ threshold, when t_{on_min} reverts to its original value. This forms a simple regulator for VCC to ensure proper charging under all conditions.

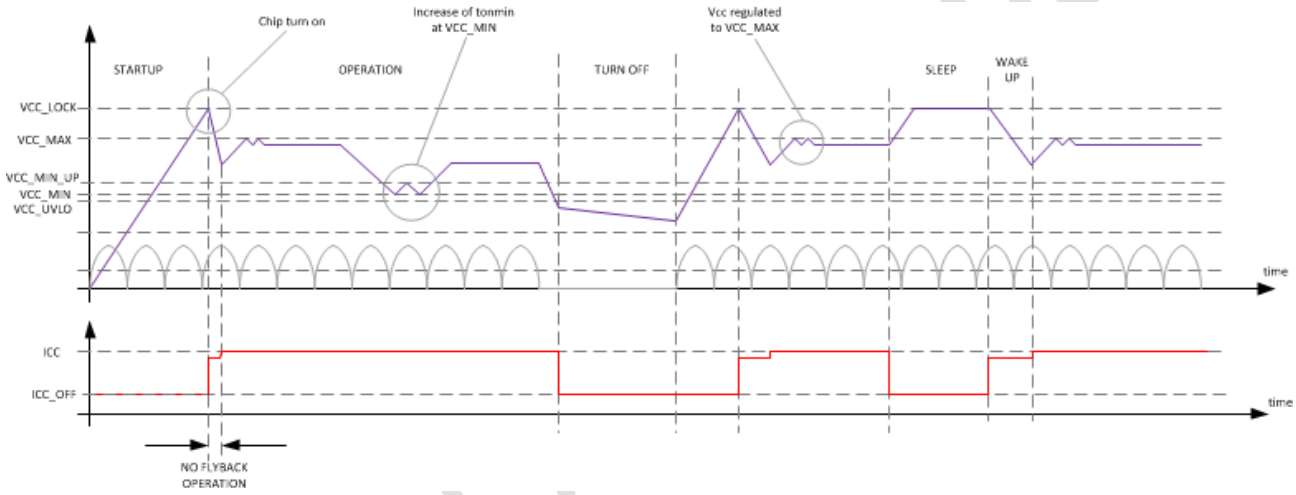


Figure 19: Vcc Control Scheme

When the iW6401 is switched into sleep mode, I_{CC} is reduced to I_{CC_OFF}, the input VIN divider is turned off, which causes VCC to charge up from the external resistor, to the V_{CC_CL} level where the voltage remains constant. When the chip receives a wake up signal from the control interface the system starts normally to the settings prior to sleep.

The following registers are used to control Vcc charging:

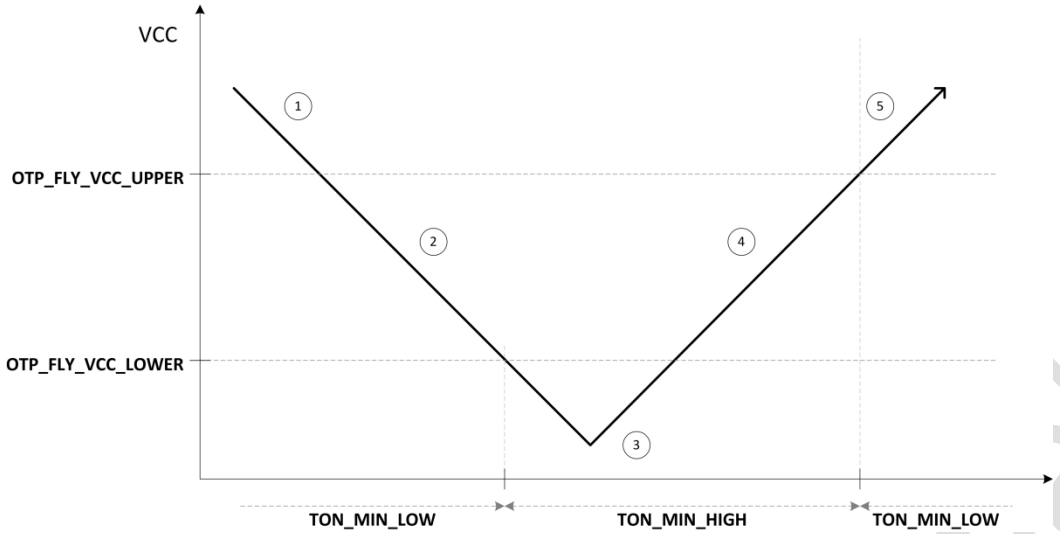


Figure 20: Vcc Control Scheme

FLY_VCC_REGULATION_EN turns the VCC control algorithm on/off. If disabled t_{on_min} remains constant under all conditions.

The following Registers are used to control the chip supply:

FLY_TON_MIN_LOW	Flyback on time in t_{ON_MIN} mode (V_{CC} charging off)
FLY_TON_MIN_HIGH	Flyback on time in t_{ON_MIN} mode (V_{CC} charging on)
FLY_VCC_LOWER	V_{CC} lower threshold voltage in t_{ON_MIN} mode
FLY_VCC_UPPER	V_{CC} upper threshold voltage in t_{ON_MIN} mode
VAUX_VCCMAX	Maximum V_{CC} threshold voltage

It should be noted that when charging VCC from the auxiliary the increase in voltage might exceed 5 mV/µs. In these circumstances the Vcc voltage will show the behavior as depicted in Figure 21.

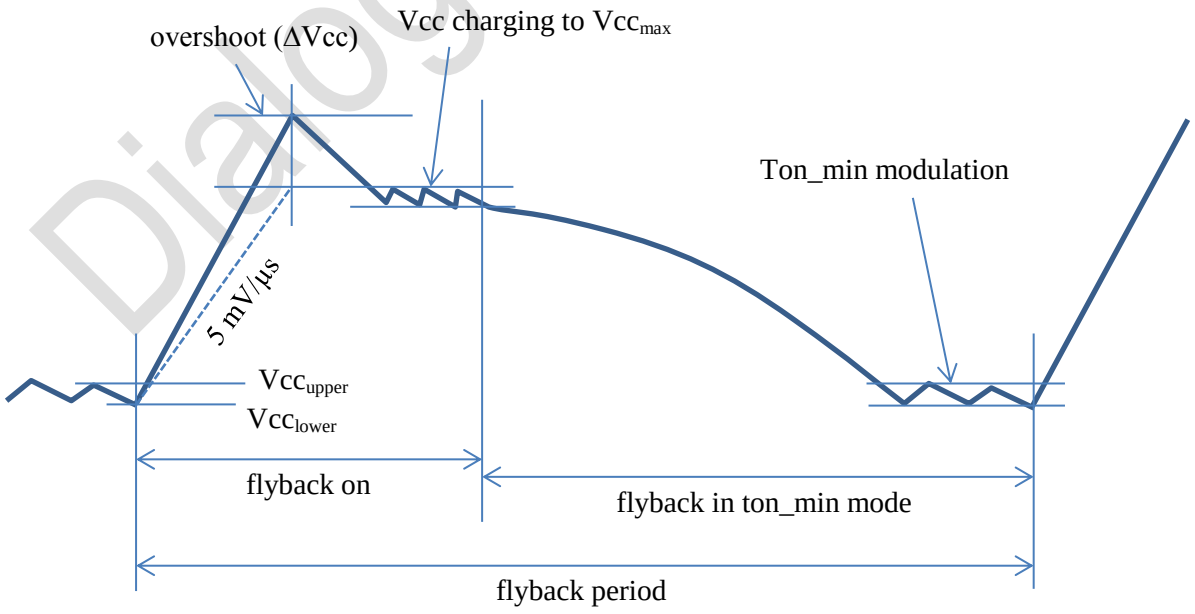


Figure 21: Simplified Vcc waveform in case of charging faster than 5 mV/µs.

The peak voltage due to the overshoot can be estimated by using the following equation:

$$\Delta Vcc \cong \left(\frac{r}{5} - 1\right) \cdot \left(Vcc_{max} - \frac{Vcc_{upper} + Vcc_{lower}}{2}\right)$$

for $r \geq 5$, where r is the voltage rise on the VCC capacitor in mV/µs. Otherwise $\Delta Vcc_{pk} \approx 0$.

9.5 Converter Operation and LED Current Control

The converter is optimized for use as a flyback topology. However, also other topologies can be applied e.g. a buck-boost configuration.

The functionality of the converter stage control is:

- Setting and controlling the LED current
- Maintaining the supply voltage V_{CC} via the auxiliary transformer winding
- MOSFET current control and overcurrent protection
- Suppressing noise or fluctuations from the bus voltage
- Maintain PFC mode

In general the converter stage is operated in one of three possible modes:

- Normal operation (peak current control): Primary peak current is regulated according to the control loop as described below
- Ton_min Mode: Converter is running at minimum on-time and fixed off-time. The ton_min is either fixed or controlled between two values to maintain constant Vcc.
- Off Mode: The converter is not switching

The topology of the flyback stage is shown in Figure 22.

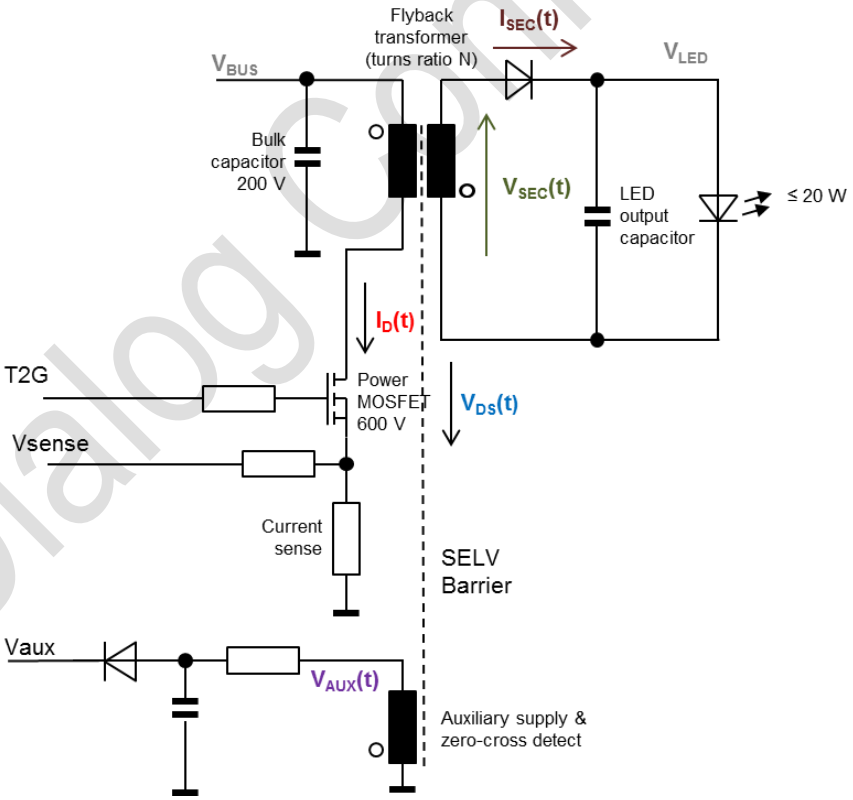


Figure 22: Flyback topology

9.5.1 Flyback operating principle

The flyback stage operates in quasi-resonant Discontinuous Conduction Mode (DCM). The on-time of the MOSFET (t_{ON}) is influenced by the following parameters:

- Minimum MOSFET on-time (t_{ON_MIN})

  Note: The minimum on-time is an important factor for the chip supply control. Please refer to the corresponding chapters for more details.
- Maximum MOSFET on-time (t_{ON_MAX})
- Primary peak current sensing voltage (V_{SENSE_MAX})
- Maximum operating frequency
- Overcurrent protection

During the on-time the drain current of the MOSFET increases almost linearly with a slope given by the input voltage (V_{BUS}) and the total primary inductance (L_1):

$$I_D(t) = \frac{V_{BUS}}{L_1} \times t$$

During the off-time (t_{OFF}) the current through the MOSFET commutates into the parasitic drain-source capacitance. No current is flowing through the secondary winding, so the voltage across the auxiliary winding (V_{AUX}) reflects the voltage across the primary winding, scaled by the turns ratio (Np:Ns) of the transformer. In Normal Power mode, the iW6401 is powered by the auxiliary winding when V_{AUX} has the same polarity as the LED forward voltage (V_{LED}).

As the drain voltage (V_{DS}) increases, the voltage on the secondary winding (V_{SEC}) reverses polarity. When V_{DS} reaches the level of V_{LED}, the rectifier diode starts conducting and current commutates from primary to the secondary winding. The peak current of the secondary winding (I_{SEC_PK}) is proportional to the peak current of the primary winding (I_{D_PK}), multiplied by the turns ratio (N) of the transformer.

Due to the constant output voltage (V_{SEC}), the secondary current (I_{SEC}) will decrease linearly to zero. At the zero crossing of V_{SEC} the rectifier diode stops conducting and the primary voltage (V_{DS}) oscillates and stabilizes around the bus voltage V_{BUS}. This oscillation is also visible on the auxiliary winding, leading to a sharp voltage edge in VAUX at the zero cross point. This edge is detected as zero cross and triggers the next switching cycle of the MOSFET.

Typical waveforms of the flyback stage are shown in Figure 23.

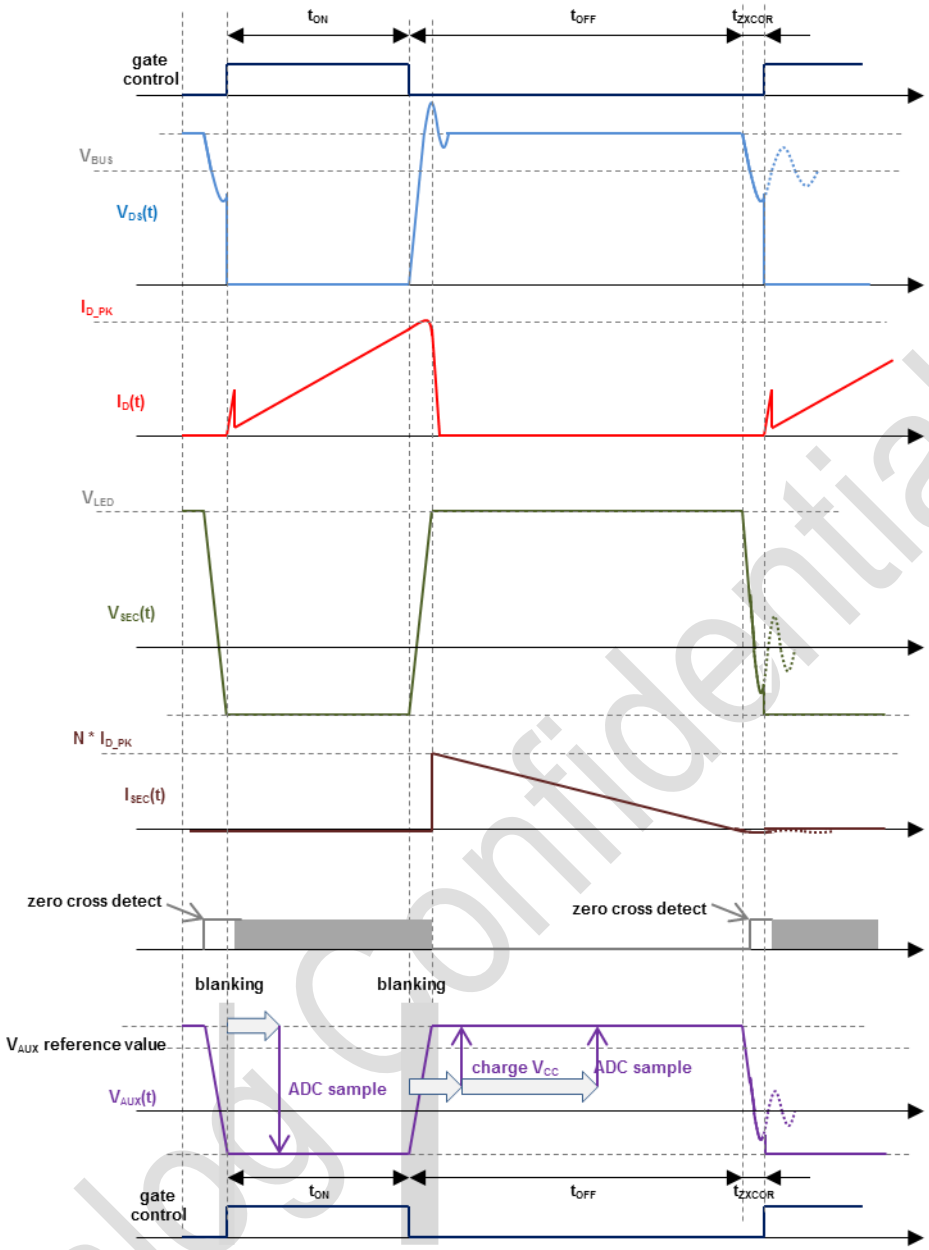


Figure 23: Flyback stage waveforms (typical) in linear mode

9.5.2 Valley switching

In order to minimise the switching losses and the EMI level of the flyback stage, the MOSFET is switched on when the voltage across the MOSFET (V_{DS}) reaches a minimum. This valley occurs a fixed time after a zero crossing is detected in VAUX. This zero cross correction time (t_{ZXCOR}) is MOSFET dependent and user programmable.

When the resulting switching frequency would become too high, valleys are skipped.

9.5.3 Flyback PWM operation

The PWM generator controls the gate drive signal for the flyback power MOSFET at T2G. The MOSFET source current is monitored via an external resistor divider at VSENSE.

The flyback stage operates in Quasi-Resonant Discontinuous Conduction Mode (QR DCM). The gate drive signal is controlled by the on-time t_{ON_T2}, the maximum on-time $t_{ON\_MAX\_T2}$, the zero-cross correction time t_{ZXCOR} and the maximum off-time $t_{OFF\_MAX\_T2}$.

When the voltage at pin VSENSE exceeds the maximum value V_{SENSE_MAX}, the PWM output signal is switched off immediately. An overcurrent condition is ignored during the blanking time $t_{BL\_OC\_T2}$ following the start of t_{ON_T2}.

The off-time is controlled by the occurrence of a zero crossing in the flyback output current (valley in V_{AUX}) and by the maximum off time $t_{OFF\_MAX\_T2}$. A zero crossing condition is ignored during the blanking time $t_{OFF\_MIN\_T2}$ following the end of t_{ON_T2}.

To ensure proper valley switching a delay of t_{ZXCOR} is observed before switching on the MOSFET after a zero crossing.

Typical waveforms are shown in Figure 24.

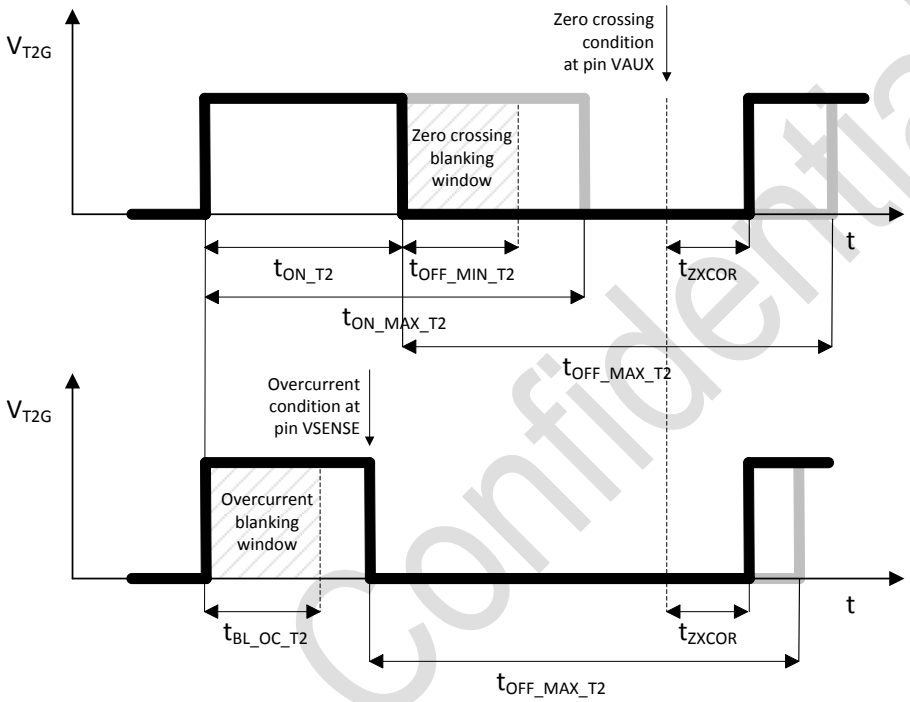


Figure 24: PWM waveforms for QR DCM mode

Please refer to the electrical characteristics for the individual blanking times.

The following registers are used to configure the converter PWM operation:

Register	Function
FLY_TON_MAX	Flyback maximum on time in peak current mode
FLY_TOFF_MAX	Flyback maximum off time in peak current mode
FLY_TON_MIN_LOW	Flyback on time in t_{ON_MIN} mode in fixed mode or lower value in Vcc control mode.
FLY_TON_MIN_HIGH	Flyback on time in t_{ON_MIN} mode high value
FLY_TOFF_MIN	Flyback off time in t_{ON_MIN} mode

9.5.4 Setting up the LED current control loop

According to Figure 25 the LED control system generates a reference signal Vref_Sense that sets the peak value for the primary converter current. This set value is in a range of 0..1V. The LED current control block adjusts this value such that the estimated LED current matches the input value at Iled_set. The scaling of Iled_set is given by an internal constant FLY_KN which is initially calculated as given below and it can be further tuned in the final design as required by the application.

The control loop is updated at regular intervals whenever the converter is operated in normal peak current mode. Whenever the converter is operated in ton_min mode the internal states of the regulator are held and the loop is no longer updated.

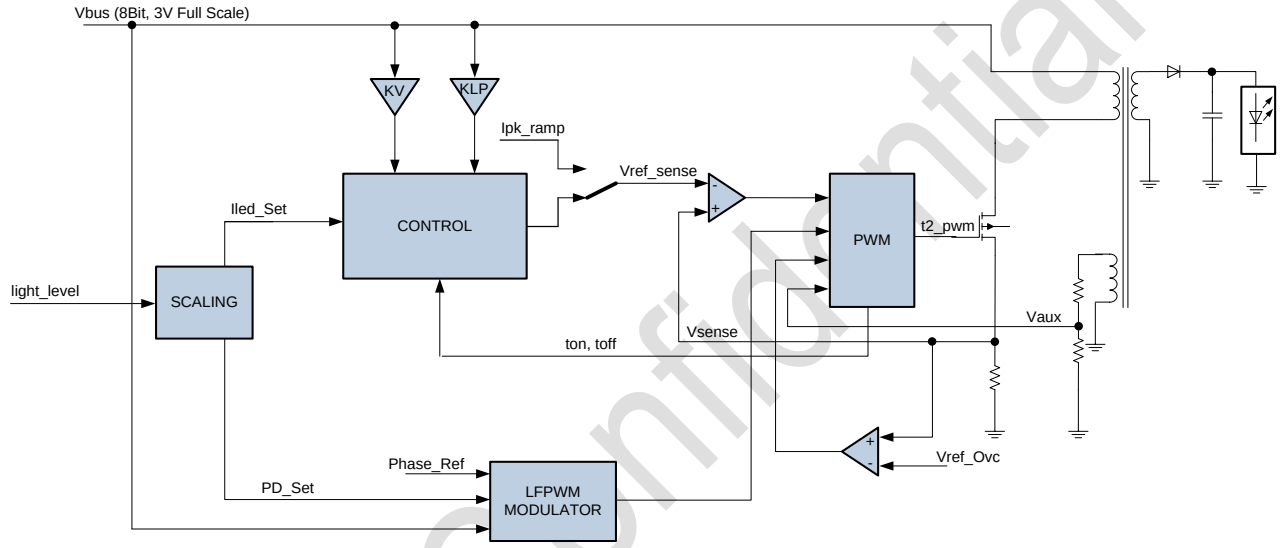


Figure 25: Flyback control system

The following procedure shall be used to configure the LED current feedback loop:

(i) Choose the Shunt Resistor Value such that the expected worst case peak current is within a full scale range of 1V

(ii) Decide about the scaling of the ILed_Set signal. The scaling is given in A/LSB of the corresponding current at the output. Based on the target scaling the internal compensation factor FLY_KN is calculated using the formula:

$$OTP\_FLY\_KN = \frac{\frac{Np}{Ns}}{2 \cdot LSB \cdot 4 \cdot R_S}$$

Where:
Np: Number of turns primary
Ns: Number of turns secondary
LSB: Target resolution for ILed_Set [A/Bit]
Rs: Shunt Resistor

This value is programmed shall be programmed as a 16-bit decimal at the corresponding address.

(iii) Adjust all correction values according to the following chart:

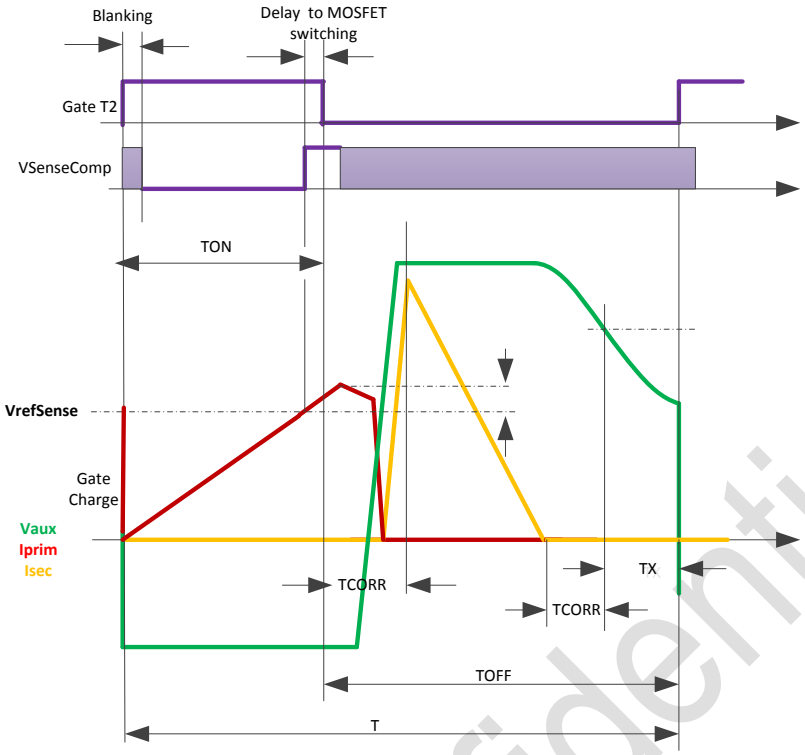


Figure 26: Flyback control timing diagram

Setting the KV factor:

In order to establish high power factor the AC supply input current shall be modulated proportional to the AC supply voltage. This is achieved by setting the KV factor to a non-zero value. In order to optimize the value an iterative approach is recommended.

The instantaneous flyback current is then modulated according to the following control rule based on the average flyback current:

$$I_{prim}(t) = \frac{\bar{I}_{prim} \cdot K_V \cdot DV_{Bus}}{255}$$

Where DVbus is the 8-bit converted signal on VBUS at a 3V full scale. Typical values for KV are in the range of 20..30. Iprim is scaled by the value of the shunt resistor and represented as 10-bit binary number.

Setting the KLP factor:

Purpose of the correction Factor KLP is to compensate for the impact of the comparator delay on the energy transfer. A correction factor is subtracted from the VrefSense signal to compensate for the current overshoot due to the comparator delay.

$$I_{primDAC}(t) = I_{prim}(t) - \frac{K_{LP} \cdot DV_{Bus}}{255}$$

Overcurrent Protection

The signal at Vsense is constantly monitored for overcurrent conditions. A reference can be programmed at which the protection kicks in. The overcurrent protection immediately turns off the switching transistor by pulling the gate low. In addition to this, the number of consecutive overcurrent events is counted and a shutdown event is triggered whenever the value exceeds the register set limit.

Ramp Mode

During startup of the system (see the State Machine Table) the output voltage is built up at a faster rate than the normal LED current would do. This allows the system to ramp up quickly even with very low LED currents. In order to increase the current temporarily the DAC which sets the VrefSense signal is switched to a fixed value given in FLY_IPK_RAMP. The system is monitoring the LED voltage and as soon as the minimum voltage is reached the system changes into normal operation and the regulator takes control of the LED current. A timeout value can be defined at which the system will terminate the ramping unconditionally allowing the system to start up without having reached the minimum threshold. A dedicated fixed off-time can be programmed for this mode.

Soft Start

Once in normal operation mode the LED current is ramped slowly to ensure a soft start of the light output. Duration and starting level of the soft-start can be set in the associated registers; however, the default settings should be suitable for most application cases.

Register	Function
FLY_IPK_MAX	Upper clamping value for regulator
FLY_IPK_MIN	Lower clamping value for regulator
FLY_KLP	Feedforward compensation factor for V_{BUS}
FLY_IPK_RAMP	Fixed flyback shunt voltage in ramp mode
FLY_TCORR	Flyback current transition time
FLY_KV	Power factor correction coefficient for V_{BUS}
FLY_KN	Flyback conversion coefficient
FLY_T_MIN	Minimum flyback switching period
FLY_TON_MAX	Flyback maximum on time
FLY_TOFF_MAX	Flyback maximum off time
SSM_T_RAMP_FLYBACK	Timeout duration of ramp mode.
FLY_TOFF_RAMP	Flyback off time during ramp mode.
FLY_VSENSE_OC_THRESH	Over-current detection threshold

9.5.5 LF Modulation

At low dim-levels the flyback is switching between two different operating modes:

(i) Normal current regulation

(ii) Ton_min mode

During normal current regulation the flyback is operating quasi resonant peak current mode. Regulated average current is supplied to the output. In ton_min mode the flyback is operated using a fixed minimum on-time. In this mode only a limited amount of energy is supplied to the output in order to keep the chip supplied via the auxiliary winding.

The Modulator controls the duty cycle of this low frequency modulation scheme:

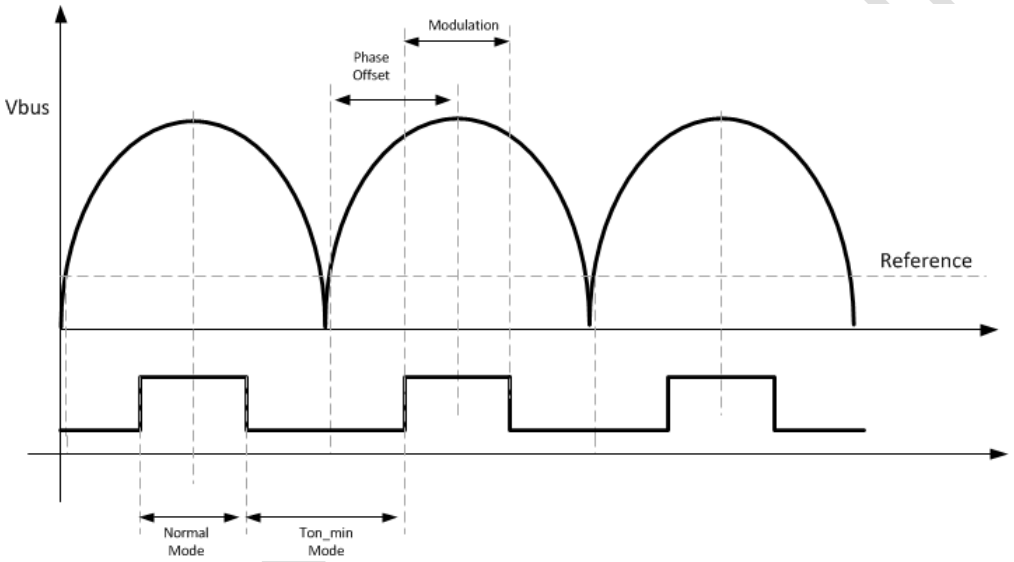


Figure 27: Modulator scheme

The modulation is synchronous to Ac supply voltage. A phase offset is setting the centre point of the modulation window relative to the crossing of the reference. The duty cycle is given by the dim level. A linear dimming characteristic with very low light flicker is achieved using this modulation scheme.

Registers to define the modulation window:

Register	Function
FLY_PWM_PHASE	Defines the centre point of the PWM window relative to the synchronization point given by VIN_SYNC
VIN_SYNC	Voltage level at Vin at which the modulator synchronizes. (in 8-bit, 3V full scale resolution)

9.6 Dimming control

9.6.1 General principle

Various blocks inside the chip can generate data for dimming the LED current. A central arbitration unit takes the various data inputs and generates one consolidated value which feeds into the flyback control unit. The following chart shows the basic architecture:

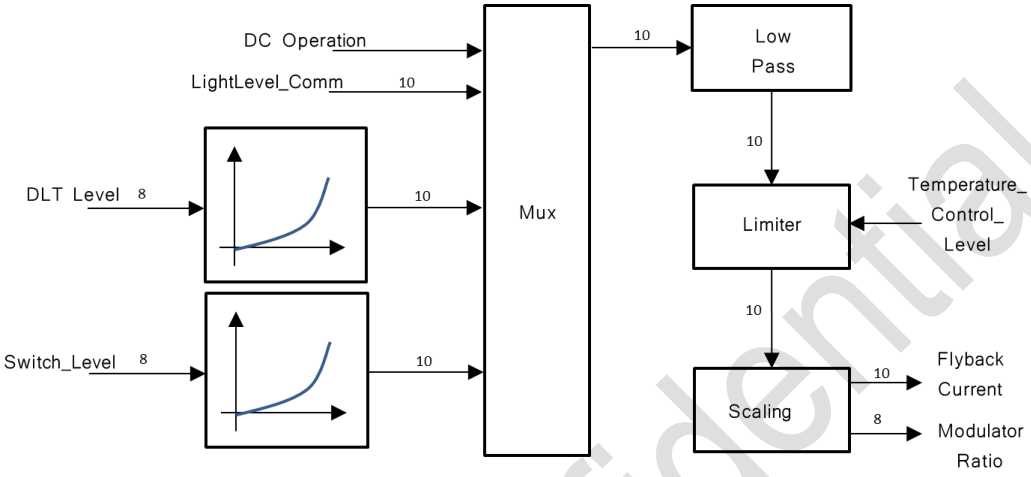


Figure 28: Dimming management scheme

Dimming levels are encoded as 8 or 10-bit binary values where 0x3FF or 0xFF represents a 100% light level. The Dimming Control block combines these signals into one consolidated output of the same format. The Flyback Control block translates the relative light level into a current set point for the LED via the scaling block (see the corresponding chapter for more details).

The rules for arbitration are:

The Limiter sets an upper power limit given by the temperature control state machine. Any change at the input of the multiplexer sets the dim-level to that value. If DC Mode is detected the DC_Level takes precedence over other inputs. The DC_Level is under control of the End of Line calibration unit which can use this value to modulate the light output. The Low pass is smoothing the light output to give the best dimming experience.

Registers used:

Register	Function
DIM_FILT_N	Set the time constant for the low pass filter

9.6.2 Startup

After power up the system state machine is ramps the output voltage to a minimum threshold (see the chapter on Ramp mode). Initially the light output is set to minimum dimming to avoid any flashing at power up. The system then checks for a duration of 200ms if any dimming information is delivered from the DLT receiver. If DLT patterns are detected the system continues to receive DLT data and upon reception of a full brightness telegram it uses that value as the next dimming set point.

If no DLT data is received with the 200ms window the system dims to the target value given by the switch event state machine. The actual value depends on the configuration of the state machine and the most recent state. In any case the light level is smoothly increased to the target level for a clean and smooth startup.

9.6.3 LED Current Scaling

The iW6401 supports a dimming range from 100% down to below 1%. Above a programmable dimming level L_{LINMIN} (typically 30%) the LED current is linearly reduced according to an adjustable straight curve. Below that dimming level the LED current remains constant and a low frequency modulation further reduces the average LED current.

Two modulation methods can be configured: Synchronized LFPWM and free running LFPWM. Both methods yield the same total current but they differ in the frequency domain which can affect the audible noise or light output noise.

The choice of the modulation method depends on the individual application. Both modulation methods can be used with high PFC operation or with non-PFC operation.

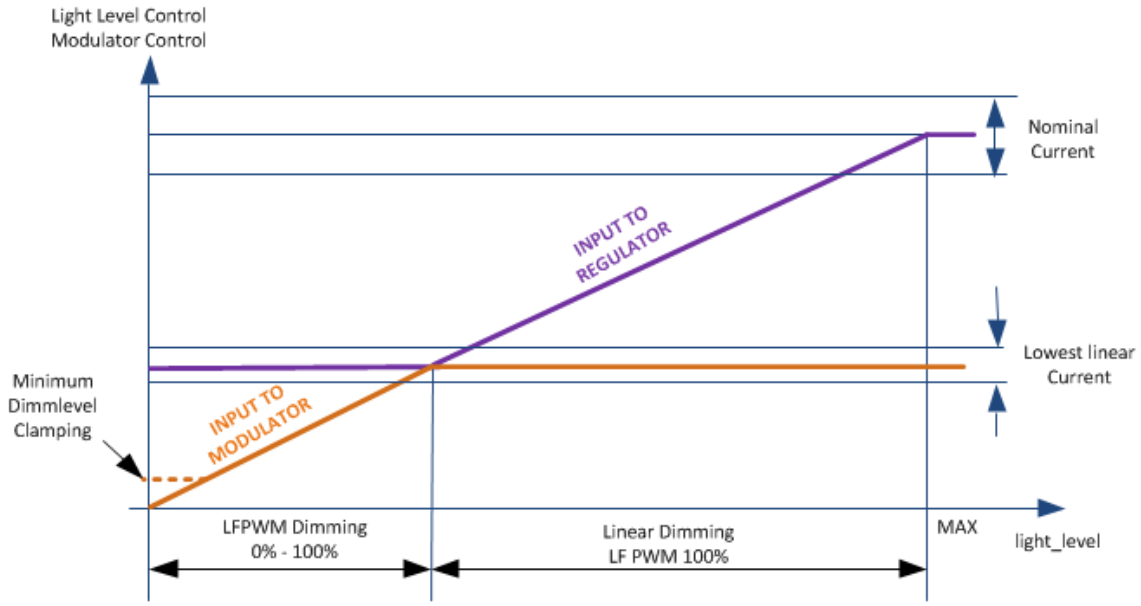


Figure 29: Mapping light level to flyback current setpoint

In the above chart the horizontal axis represents the relative light level that feeds into the flyback control block. The data range lies between 0x3FF (100%) and 0x000 (0.25%). These limits are hard coded and cannot be changed.

The vertical axis represents the LED current set point (iled_set) and the pulse duty cycle (pd_set) that feed into the PWM & I_{LED} Control block. The values are system dependent. The data is represented as binary values (iled_set: 10 bits, pd_set: 9 bits).

The following register settings are used to define the current scaling:

Register	Function
FLY_LLVL_LINMIN	Light level threshold for linear/pulsed current control
FLY_LLVL_MIN	Minimum light level for all dimming methods
FLY_ILED_NOM	Nominal LED current for 100% light level
FLY_ILED_LINMIN	LED current threshold for linear/pulsed current control

9.6.4 Dimming curve lookup tables

Dimming curves are stored in OTP as six 8-bit relative light level values. Output data are based on interpolation and have a 10-bit resolution. Separate dimming curves are available for switch event dimming and DLT dimming.

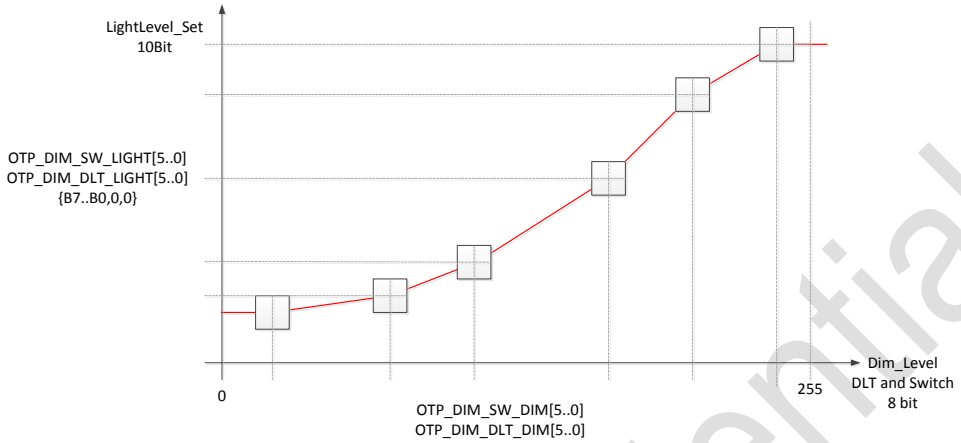


Figure 30: Interpolating points in OTP to set the dimcurves

The dimming curves are set using the following registers:

Register	Function
DIM_SW_LIGHT[5:0]	Switch dimming light level presets
DIM_DLT_LIGHT[5:0]	DLT dimming light level presets
DIM_SW_DIM[5:0]	Switch control dim level presets
DIM_DLT_DIM[5:0]	DLT control dim level presets

9.6.5 Switch event dimming

In Switch Event dimming mode the supply voltage V_{CC} is monitored continuously to detect Ac supply on/off switching. A valid switch event is detected when V_{CC} is below V_{CC_MIN} (10 V) for a certain time. This time is measured by a down-counter in steps of 2ms, the upper and lower threshold values are controlled via registers.

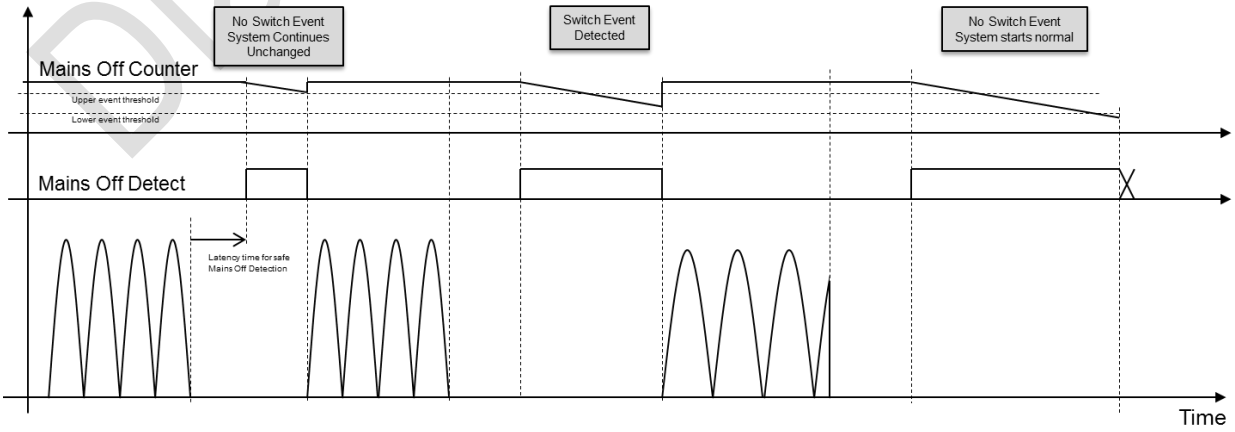


Figure 31: Switch event detection scheme

A programmable state machine controls the dimming behaviour triggered by AC supply switching events. Dimming can be immediate or a linear ramp of specified duration. The duration step size is adjustable between 5ms and 20s, or between 1 and 2000 AC half-wave periods (T_{SYNC}).

States can also hold the previous dim level, which implements the capability of have a dimming ramp then hold the dimming value on the switching event.

To detect Ac supply switching events, the system stops immediately when the AC voltage goes off. The system enters a low-power mode in which the event counter is starts to count downward from FFh. The counter rate is fixed at 4ms. Two threshold levels can be programmed which define the detection process. A first threshold, SWITCH_THRESHOLD_HIGH, initiates the event window; whenever Vcc is recharged before this threshold is reached no event is detected. Then the switch event window is acive until the second threshold, SWITCH_THRESHOLD, is reached. Any duration longer than this second threshold is not detected as an event.

If the VCC reaches the POR reset level, the device is reset and a normal startup occurs.

It is in the responsibility of the system to ensure that the VCC voltage remains above the reset value under all circumstances to have reliable switch-event detection.

9.6.5.1 Switch event states

Up to 8 switch event states can be defined by register settings, each state consisting of 3 bytes. Each state defines a switch-event and/or time-out duration with the associated next states. The target LED light level (in %) is activated immediately or a ramp initiated during the timeout. The state configuration format is shown in Table 8.

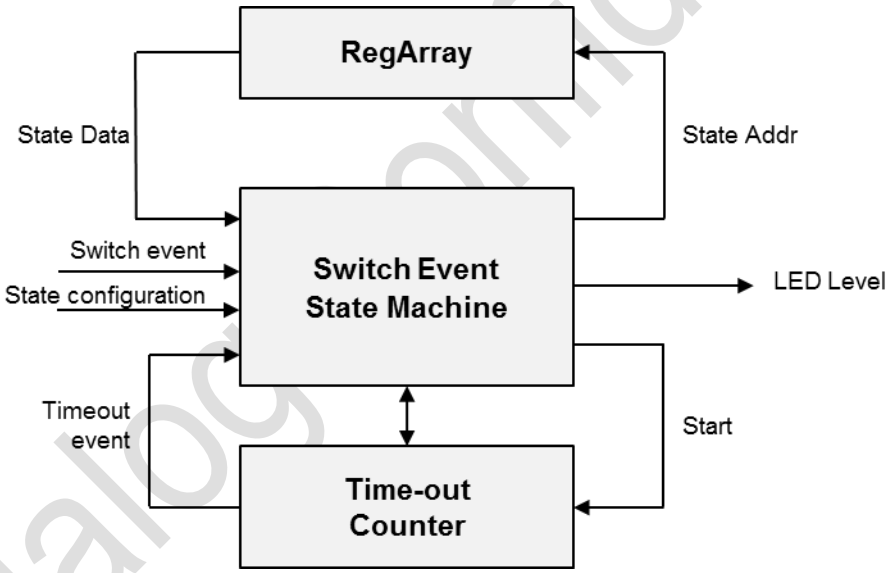


Figure 32: Switch event state machine

Each state is configured by defining the events to which this state is sensitive and which are the subsequent states. The definition of each state:

Table 8: Switch event state configuration

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 2	Timeout Threshold (multiples of 10ms)							
Byte 1	Ramp to Target	Target Light Level (Bit 7..1 of relative light level)						
Byte 0	Timeout Enable	Switch Event Enable	next state after timeout			next state after switch event		

Registers used to define the switch event states:

Register	Function
SWITCH_STATE0[2:0]	Switch event state 0
SWITCH_STATE1[2:0]	Switch event state 1
SWITCH_STATE2[2:0]	Switch event state 2
SWITCH_STATE3[2:0]	Switch event state 3
SWITCH_STATE4[2:0]	Switch event state 4
SWITCH_STATE5[2:0]	Switch event state 5
SWITCH_STATE6[2:0]	Switch event state 6
SWITCH_STATE7[2:0]	Switch event state 7

9.6.6 Dimming over data interface

Dimming via data interface is supported by writing to the register 0xEE; this 16-bit register sets a dimming value which is directly routed to the dim manager block. The control range of this register is 0x0000 to 0x03FF. To turn off the direct light level control the register is set to 0x8000.

.

Register	Function
LIGHT_LEVEL_COM	Direct light level value (0x8000 is off)

9.6.7 DLT dimming

The iW6401 supports dimming according to IEC 62756 Digital Load side Transmission (DLT) standard. This standard uses modulation of the AC supply waveform to transmit data to a lamp control circuit, such as a dimmer. The first part of the waveform supplies the control circuit; the last part contains the data bits. The modulation type is Manchester encoding.

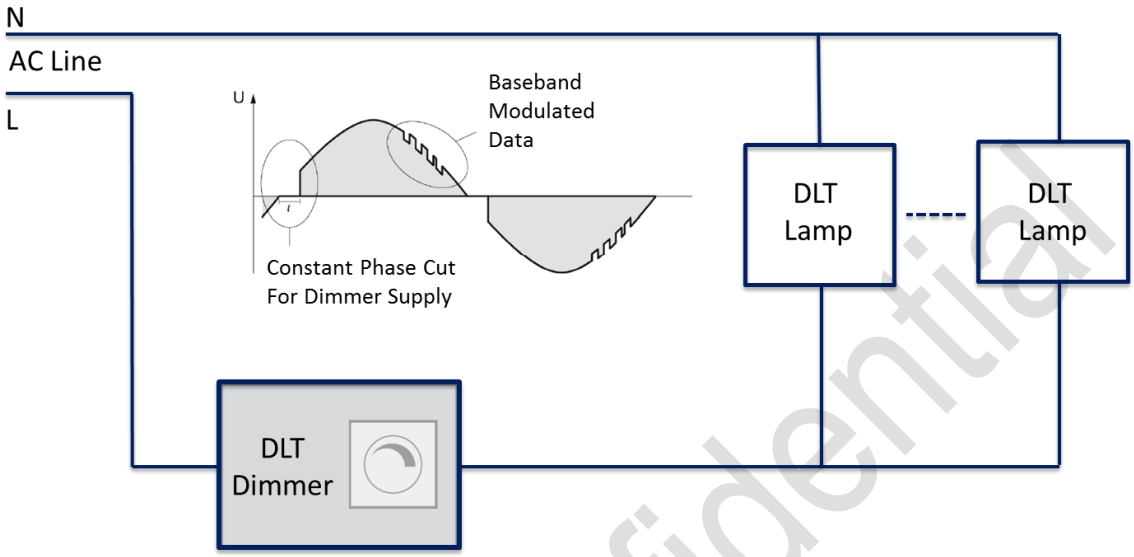


Figure 33: DLT dimming

The iW6401 supports DLT dimming using the Source Controlled MOSFET Driver (SCMD) at pins T1G and T1S, in combination with an external power MOSFET to implement the load current bypass as defined by the standard. A programmable state machine controls the activation of the bypass and the SCMD current level.

The voltage at pin VIN is sampled and digitised. The sample stream is processed, data frames are decoded and the light level is set accordingly once a valid telegram has been received.

A DLT telegram consists of multiple frames, each frame representing two bits. Data are transmitted one frame per half AC period. A telegram always begins with a ‘Start of Telegram’ frame (all 1’s pattern). The iW6401 only supports telegram type 0 (brightness). When a valid DLT brightness telegram has been received, the DLT dimming level (dim_level_dlt) is updated accordingly (see Figure 28).

The DLT slave group number (0 to 3) is programmable either by the I2C or serial interface or by means of the group addressing scheme as defined in IEC62756. The iW6401 responds to messages addressed to group 0 (broadcast) as well as the assigned group number.

All functions according to IEC62756 are implemented inside the control chip. There are 2 main blocks which are relevant to the DLT functionality:

1.) The DLT State machine

2.) The DLT Receiver

9.6.7.1 DLT State Machine

The DLT State machine controls the bypass load according to IEC62756. The state machine uses the stream of samples from the Vin pin to set the bypass current load accordingly.

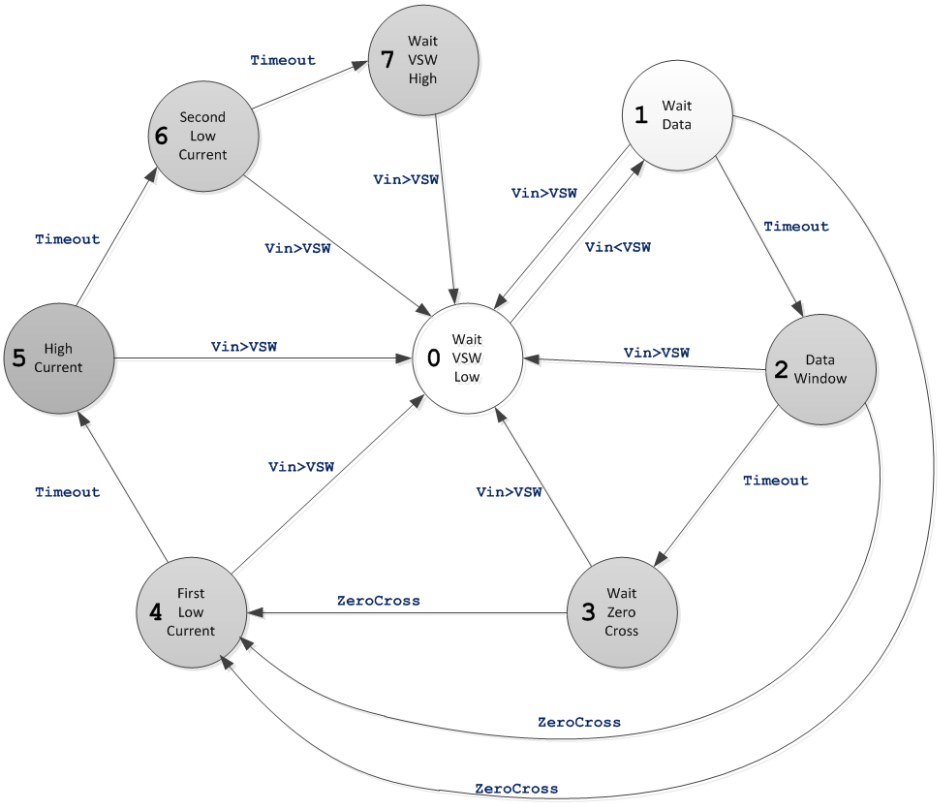


Figure 34: DLT state machine

In Figure 34 the light grey shaded states are low current and the dark shaded state is the high current state. Current levels as well as the timeouts for the individual states can be programmed individually if the default settings are not appropriate for a given design.

9.6.7.2 Bypass Load protection features

In general the bypass current loading is switched off if no valid DLT telegram has been received within 2 minutes.
The high current phase is reduced to 10% of nominal if the system detects that no DLT dimmer is connected. This reduces power losses and improves EMI compatibility during the first 2 minutes of operation with no dimmer attached.

In order to protect the bypass load from excessive instantaneous power a current limiter is activated whenever the voltage across the switch exceeds a preset limit.

The corresponding registers are:

Register	Function
DLT_SCMD_ILIM	Current limit when threshold voltage is exceeded
DLT_SCMD_VLIM	Current limiting threshold voltage

9.6.7.3 Bypass Load energy monitoring

An additional internal counter registers the amount of energy which is processed inside the bypass load MOSFET. Whenever this energy is exceeded the current loading is stooped for the ongoing AC half-cycle. However, under normal conditions that level is never reached.

9.6.7.4 Bypass Load turn off

In order to minimize the thermal loading of the chip and the bypass transistor the high current phase is turned off whenever no DLT dimmer is detected.

9.6.7.5 DLT Receiver

The DLT receiver processes the incoming stream of VIN samples in order to decode the modulated information according to IEC62756. If any error occurs during the reception of the telegram the data is ignored and the system waits for the next telegram. If a full telegram is received any brightness data or group-address assignment data command is actioned. Any other data is ignored. However, in order to process DLT data with an external microprocessor, all received patterns can be read via the register DLT_DATA.

In general all received patterns can be read through the I2C interface. It is therefore possible to use the iW6401 as a simple DLT frontend just delivering decoded patterns to an external processor.

If the data is processed inside the chip the following response is given:

- Receive Error: data is ignored, no change in system
- Brightness Telegram received: Brightness data is propagated to the dim-manager
- Group Address Assignment Telegram: Executes the address assignment according to IEC62756
- Any other telegram: Data is ignored

9.6.7.6 DLT Group Address

The iW6401 has its group address programmed in OTP memory and initialized during start up. The group address can be reconfigured either by reprogramming the corresponding OTP memory or using the telegram based group addressing feature as defined in the IEC standard. According to the IEC standard up to 32 reprogramming of the group address are supported. In order to meet this requirement the device must have sufficient user memory space available (at least 64 bytes of un-programmed OTP memory). The Control Center software has a built in checking feature to ensure this condition.

Register	Function
DLT_GRP_ADDR	Value of 0..3 indicating the group address.

10 Protection mechanisms

10.1 Thermal protection

An internal or external temperature sensor monitors the die temperature of the iW6401 at regular intervals. A programmable state machine controls the behaviour in case of over-temperature, ranging from dimming to immediate shutdown.

10.1.1 Temperature event states

Up to 4 temperature states can be defined in OTP memory, each state consisting of 4 bytes. Each state defines minimum and maximum temperature values with the associated next states. The target LED light level is specified and a timeout period before the next state is entered. All measured values during the timeout period have to meet the trigger criteria in order to change states.

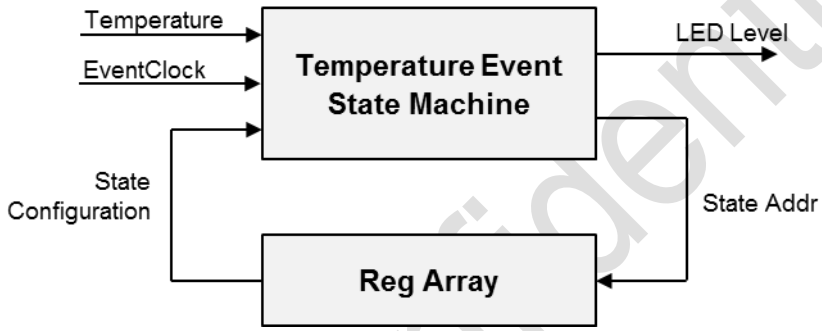


Figure 35: Temperature Event state machine

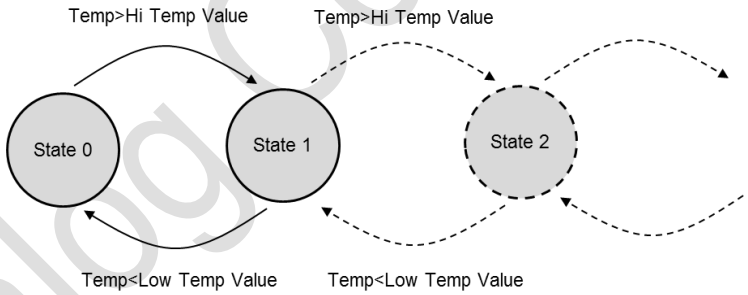


Figure 36: Example implementation

The system resets into state 0. Each state holds upper and lower temperature threshold values. If all samples taken during the timeout window meet the criteria to be above or below the respective state the event is triggered and a new state is set where the process repeats. A different light level is programmed in each state in order to manage the power dissipation.

Table 9: Temperature event state configuration

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 3	Light_Level (0..255)							
Byte 2	LOW_TEMP_VALUE							
Byte 1	HIGH_TEMP_VALUE							
Byte 0	HT_NEXT_STATE			LT_NEXT_STATE			TEMP_TO_VALUE	

The 8-bit HIGH_TEMP_VALUE represents the maximum temperature and LOW_TEMP_VALUE the minimum temperature.

For the internal temperature sensor the temperature is calculated as follows:

$$TEMP_{VALUE} = 255 - (-0.4 * T_J + 206) * TEMP\_GAIN/128$$

Equation 1

For an external temperature sensor at pin NTC/SCL the following applies:

$$TEMP_{VALUE} = 248.5 - 85.7 * VNTC$$

Equation 2

HT_NEXT_STATE specifies the next state after a High Temperature event, LT_NEXT_STATE the next state after a Low Temperature event.

The 2-bit TEMP_TO_VALUE controls the temperature event timeout duration t_{TO_TEV} as shown in Table 10.

The 8-bit LED_LEVEL represents the target light level (in %) to the end of the timeout period. A zero value indicates 'hold last level'.

Table 10: Temperature event timeout

TEMP_TO_VALUE[1:0]	Temperature event timeout t_{TO_TEV} (s)
00	0
01	10
10	60
11	600

Table 11: registers used by the temperature control state machine.

Temperature sensing registers		
0xA6 to 0xA9	TEMP_STATE0[3:0]	Temperature event state 0
0xAA to 0xAD	TEMP_STATE1[3:0]	Temperature event state 1
0xAE to 0xB1	TEMP_STATE2[3:0]	Temperature event state 2
0xB2 to 0xB5	TEMP_STATE3[3:0]	Temperature event state 3

Figure 37 and Figure 38 show the internal and external temperature sensor characteristics used for thermal management. The NTC example shows a 22kΩ NTC with B=4300.

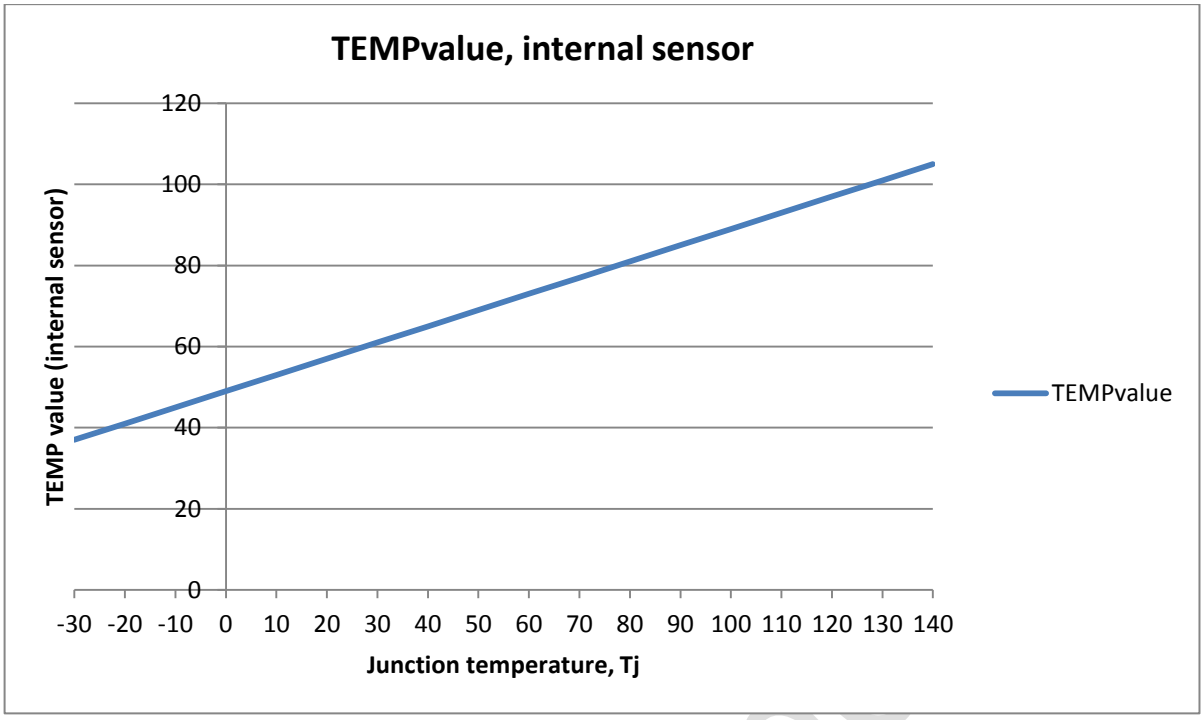


Figure 37: Typical characteristic of the on-chip temperature sensor

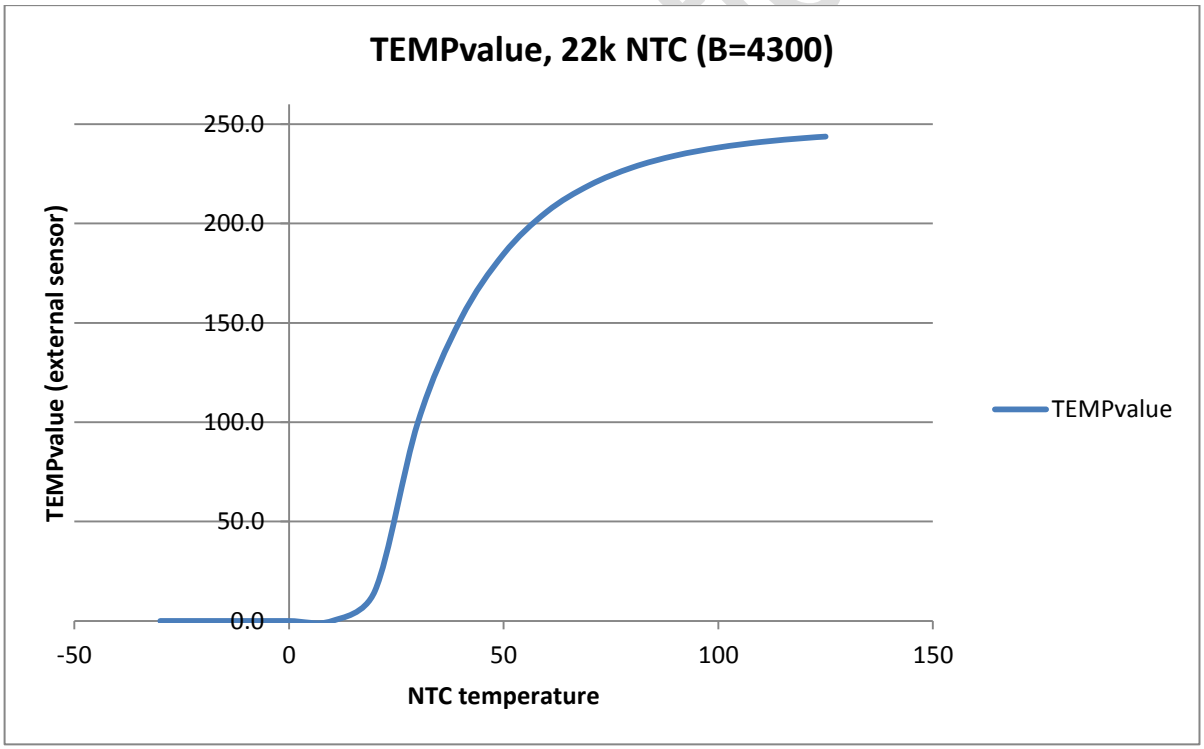


Figure 38: Example characteristic of an external NTC temperature sensor

10.1.2 Configure external temperature sensor

An external NTC can be connected to the SCL pin of the chip; in this case the SCL pin can no longer be used for I2C communication. (As an alternative for this case the data pin can be used for asynchronous communication.)

In order to change the Temperature State Machine to use the external sensor the following register must be programmed:

Register	Function
TEMP_NTC	Configure state machine to use external sensor

10.1.3 Thermal shutdown

Whenever the internal chip temperature reaches an upper limit the system shuts down immediately and enters low current mode. The internal temperature sensor is used for the thermal shutdown regardless of the TEMP_NTC selection. If this limit is set to 255 the shutdown is disabled.

Register	Function
TEMP_LIMIT	T_J temperature shutdown.
TEMP_GAIN	Gain factor of internal sensor, default 128d

10.2 LED open/short protection

In Run state the operating voltage of the LED is continuously monitored and compared against defined minimum and maximum levels. Whenever any of these limits are exceeded for a number of consecutive cycles, the iW6401 stops operating and enters Stop state. This prevents the lamp from operating in an unsafe condition. All shut down levels are programmable.

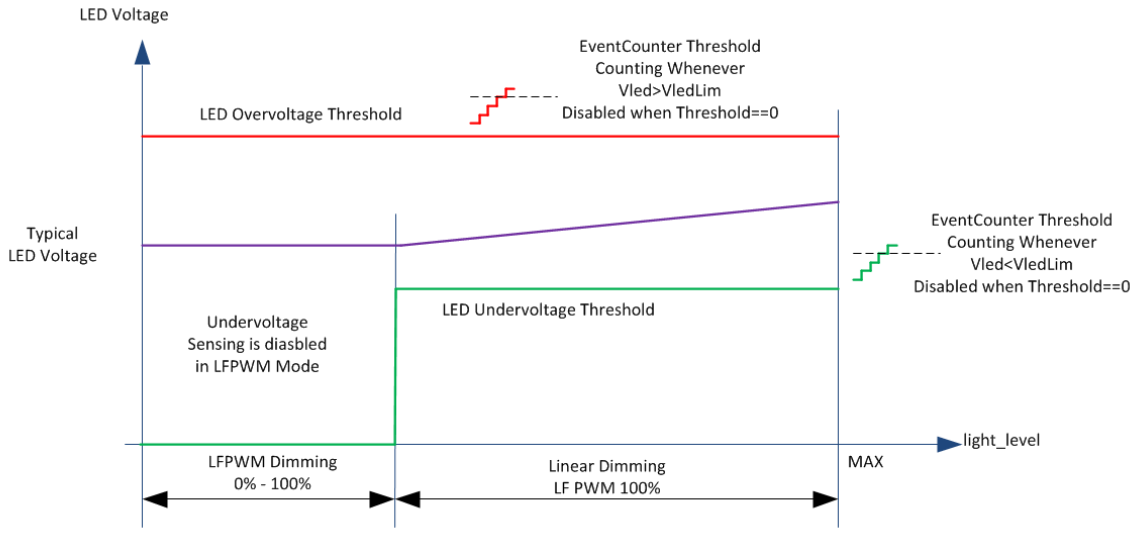


Figure 39: Led monitoring thresholds

In linear control mode both upper and lower limits are active. Independent filters can be configured to prevent the system from premature triggering. In low frequency PWM mode the under voltage

shutdown is disabled as in this mode the LED voltage can be lower than the threshold and the total power is low. For the scaling of these registers the following factors must be taken into account:

- The Winding Ratio between the Secondary and the Auxiliary Winding
- The voltage drop across the forward diodes
- The internal voltage divider

The voltage is samples at a fixed time following the falling edge of T2G:

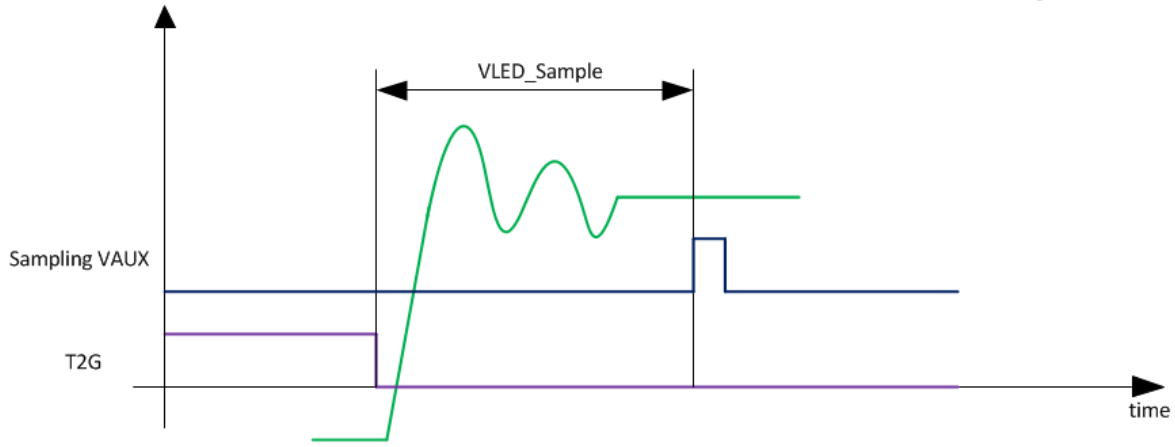


Figure 40: Timing of VLED Sampling

Register	Function
VAUX_VLEDMAX	Upper Limit for equivalent LED Voltage
VAUX_VLEDMIN	Lower Limit for equivalent LED Voltage
VAUX_VLED_SAMPLE	Time at which the equivalent output voltage is sampled.

11 Chip programming and data interfaces

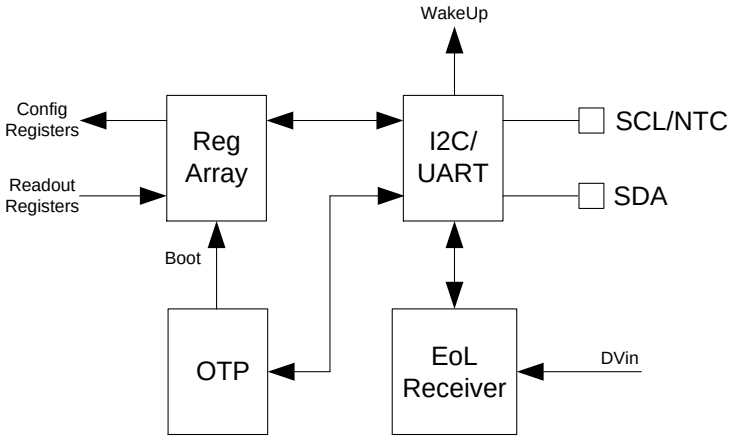


Figure 41: Programming Interfaces

The iW6401 supports 3 different interfaces: I2C (SDA/SCL), bidirectional serial data (DATA) and communication via modulated power line and modulated system power (End Of Line Communication).

All three modes are active and no configuration is required to switch between the different modes. In I2C mode the slave address is programmable to allow up to four iW6401 devices can be controlled and operated on the same interface.

The protocol definition can be found in the respective sections below.

At power-on-reset the chip is initialized with default settings. For many applications the default register values already deliver good performance results.

Following power-on-reset the internal logic reads (boots) the configuration data from OTP memory.. The data in OTP is organized as a list of register/value pairs where each pair indicates a register address and its data. With this free-format structure only register values that need to be changed from the default need to be written to the OTP; additionally it is possible to update the same register multiple times which makes it convenient during system R&D and optimization.

It is recommended to use the programming software provided by Dialog for reading/writing data to the chip. The SW can be downloaded from Dialog's website.

When using interfaces in parallel, the first bit of the communication (serial or I2C) takes priority, until the communication sequence is complete.

When an external temperature sensor is connected to the SCL/NTC pin, I2C communication cannot be used as the SCL input is disabled. In this case only serial communication via the SDA pin is available.

Serial communication across modulated AC supply and modulated power can take place parallel to I2C communication. The interface logic manages the data consistency (first come, first serve). If data access to the same register/memory is initiated through both interfaces the last data written will be valid.

Serial data communication is enabled for a limited time window after a DC voltage has been detected on the AC supply terminals. During this time window, serial data communication via the SDA pin is disabled..

To allow full read/write access to the register array (reg01h to regD0h) the ASCII string "Prog" is written to regFFh. To clear this mode write regFFh=00.

11.1 Locking data

The iW6401 provides register and OTP access locking; please refer to the Application Note “Locking data in iW6401” for more details.

11.2 OTP Checksum

In order to secure data consistency over the full lifetime of a light bulb a checksum algorithm is used to verify the data loaded from the OTP during the boot process. The checksum is triggered by writing to a dedicated register, this triggers the comparison of the stored checksum against the internal calculated value and if this is not equal the boot process will stop and the system state-machine will enter standby mode.

The correct checksum data is calculated inside the Dialog Programming Software; multiple checksums calculations are possible during the OTP boot sequence. Refer to the Application Note “Checksum and OTP data programming in iW6401” for more details..

11.3 Communication via I2C

11.3.1 I²C-bus timing

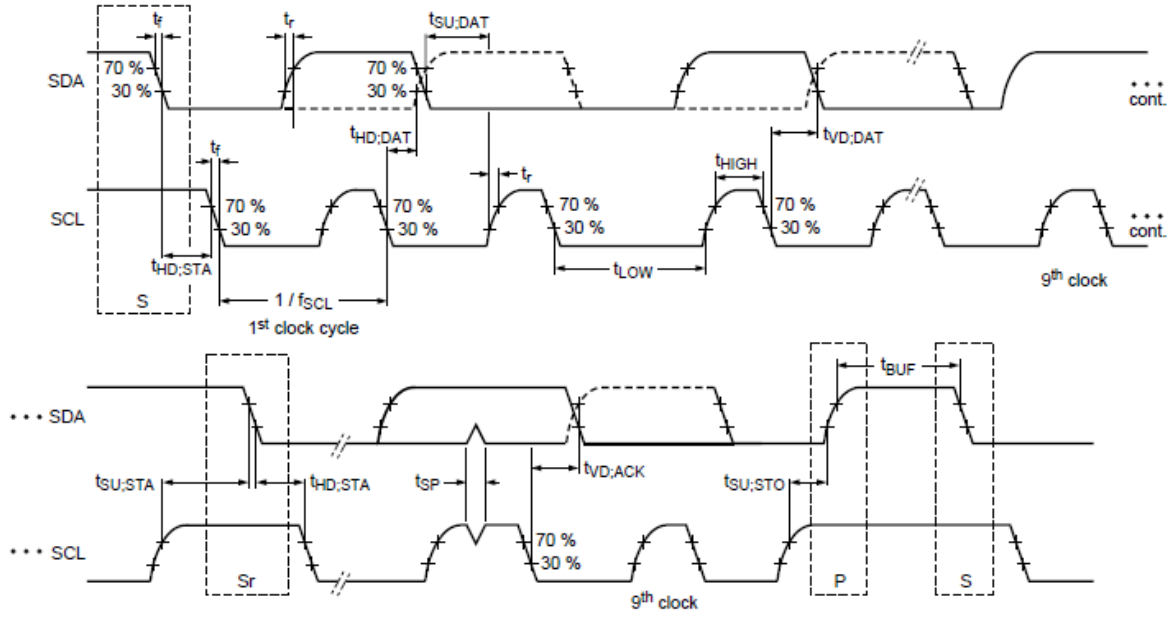


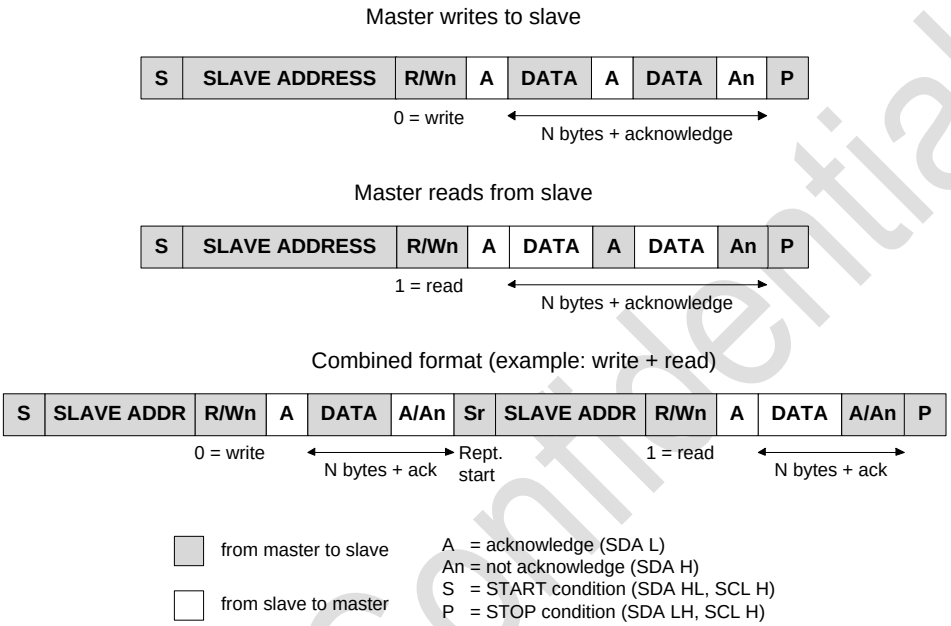
Figure 42: I²C-bus timing I²C-bus timing (normal mode)

11.3.2 I²C-bus protocol

The iW6401 operates as an I²C-bus slave device with default 7-bit slave address of 0x38.The two LSBs of the slave address are programmable with register COMM_I2C_ADDR, allowing up to four slave devices on the same I²C interface.

I²C-bus slave address

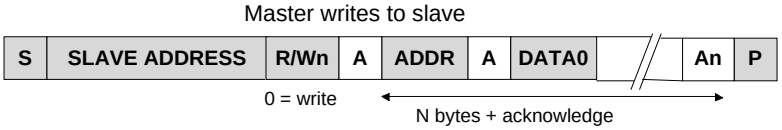
B7	B6	B5	B4	B3	B2	B1	B0
0	1	1	1	0	COMM_I2C_ADDR		R/W_N



11.3.3 I²C-bus Data Layer

Control of the chip via I2C is based on a register access protocol.. All data transfers start with an 8-bit address followed by the requested read or write, dependant on the register of 1 to 4 bytes. Initially after power-on-reset only the registers 0xE4 to 0xFF are available for read/write. Writing the correct ASCII string to register 0xFF enables one of the different memory maps available in the device. This is a protection mechanism against invalid write access.
After selection of one memory map the normal protocol as described before is used for data transfers.
Access to the OTP is via three dedicated registers, which allows full programming and verification.

11.3.3.1 I²C-bus register write



The 8-bit address indicates the register; followed by 1 to 4 data bytes. The I2C manager handles the correct number of bytes for each register. There is no auto-increment of the register address.

11.3.3.2 I²C-bus register read

Setting the read address

Master writes to slave

S	SLAVE ADDRESS	R/Wn	A	ADDR	P

0 = write

Reading the data

Master reads from slave

S	SLAVE ADDRESS	R/Wn	A	DATA	A	DATA	An	P

1 = read

N bytes + acknowledge

11.3.3.3 Dimming via I2C

The LED diming level is set by writing a 16-bit word to register 0xEE. The Dim-Level can be any value between 0x0000 and 0x03ff. This value is then scaled according to the calibration data in order to set the LED current.

11.3.3.4 Sleep mode

Sleep mode in the iW6401 is initiated by setting regEDh=0x04.
To wake the device from sleep mode, 4 pulses on the SDA pin are required.

11.4 Serial Data Communication

The serial interface is based on a Manchester encoded bit-stream which is received via the DATA pin or via a modulated DC voltage at the input terminals of the LED bulb. The DATA pin has an open-drain output, so requires an external pull-up resistor to 2.5V to 5.5V.

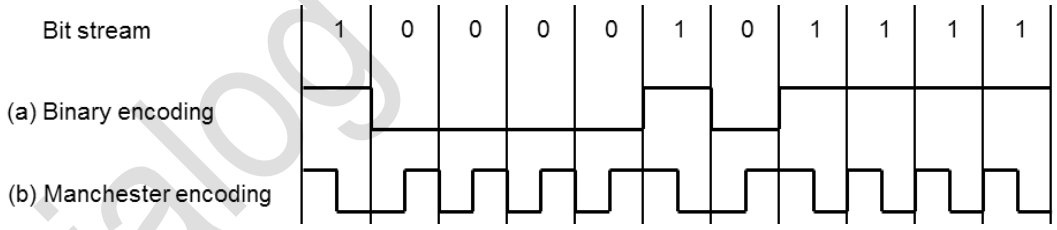


Figure 43: Manchester encoding of binary data

Input protocol format:
The incoming protocol on VIN or the DATA pin is Manchester encoded: a falling edge is interpreted as ‘1’, a rising edge as ‘0’. Data idles at a constant high level. Transmissions are in frames according to the following format:

Start sequence (’10’)	Address <9:0>	Write	Byte count <2:0>	0..8 * data<7:0>

Successive protocol bit widths are allowed to deviate +/- 10% from the start sequence; each valid data edge will be used to re-synchronize the timing; the edges which possibly occur between two separate data bits are not. If the start sequence duration shows the same variance as the other bits in the data frame, a deviation of +/- 5% in bit timing in general is allowed.

All receiving fields are transferred MSB first.

Output protocol format:
After receiving a valid input frame, the device transmits data. Data is Manchester encoded; with falling edge defined as a '1'. MSB is transferred first.

The following output frames are defined:

Data frame (for read access)

Start sequence ('10')	Data(*0*)<0:7>	…….	Start sequence ('10')	Data(*n*)<0:7>

Confirmation frame (for write access acknowledge)

Start sequence ('10')

Error frame (when invalid data has been detected)

Start sequence ('100')	Error Code<6:0>

- A frame with Manchester decoding errors in the header will not return any frame.
- A valid read frame reception –with the 'write' field set to '0'– results in a *data frame* being returned. If global read security is enabled, all read frames are regarded invalid.
- An invalid or incomplete read frame does not return any frame.
- A valid write frame reception –with the 'write' field set to '1'– result in a *confirmation frame* being returned, except when a previous read frame resulted in an error, in which case an *error frame* is returned. If global write security is enabled, all write frames are regarded invalid.
- An invalid write frame results in an *error frame* being returned.

12 Typical Application Diagrams

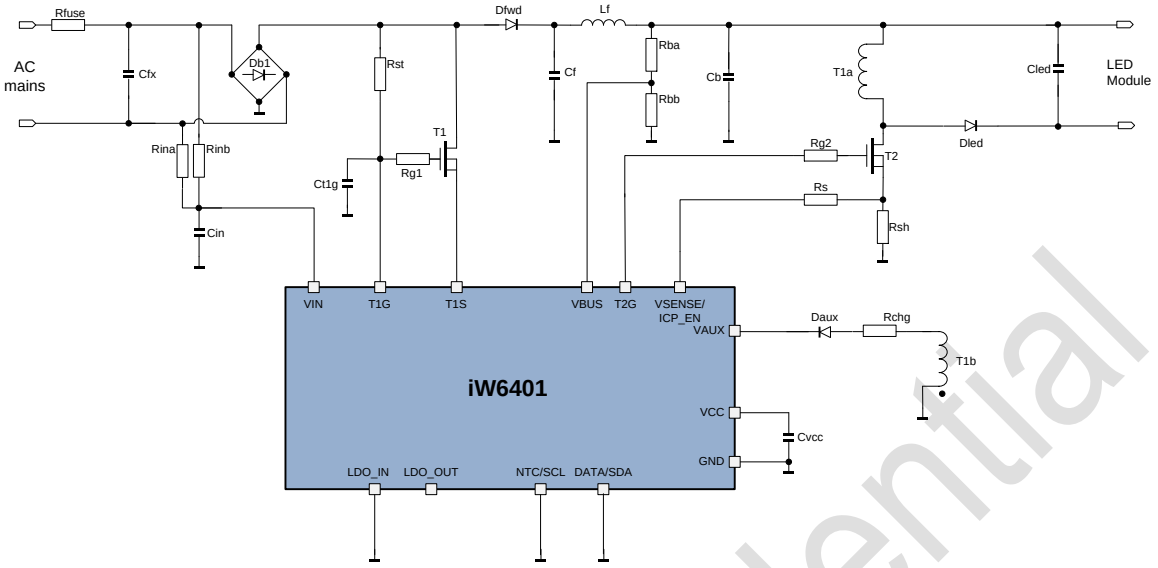


Figure 44: Application diagram for DLT dimming

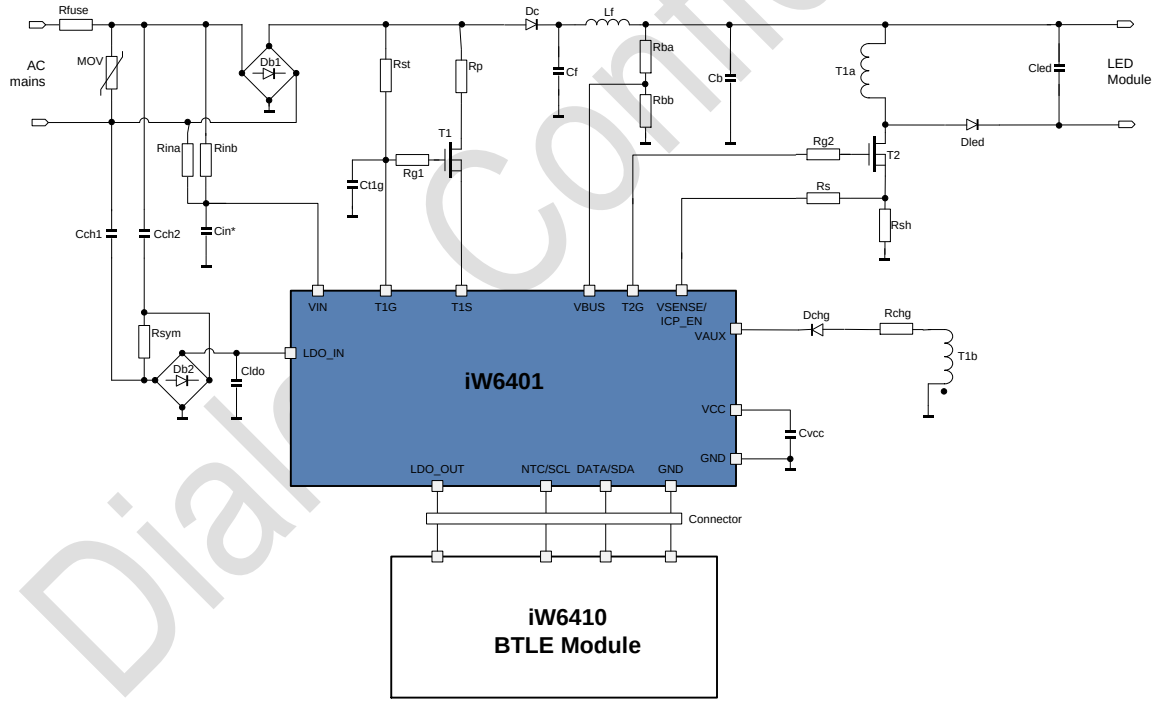


Figure 45: Application diagram with Bluetooth module and startup circuit

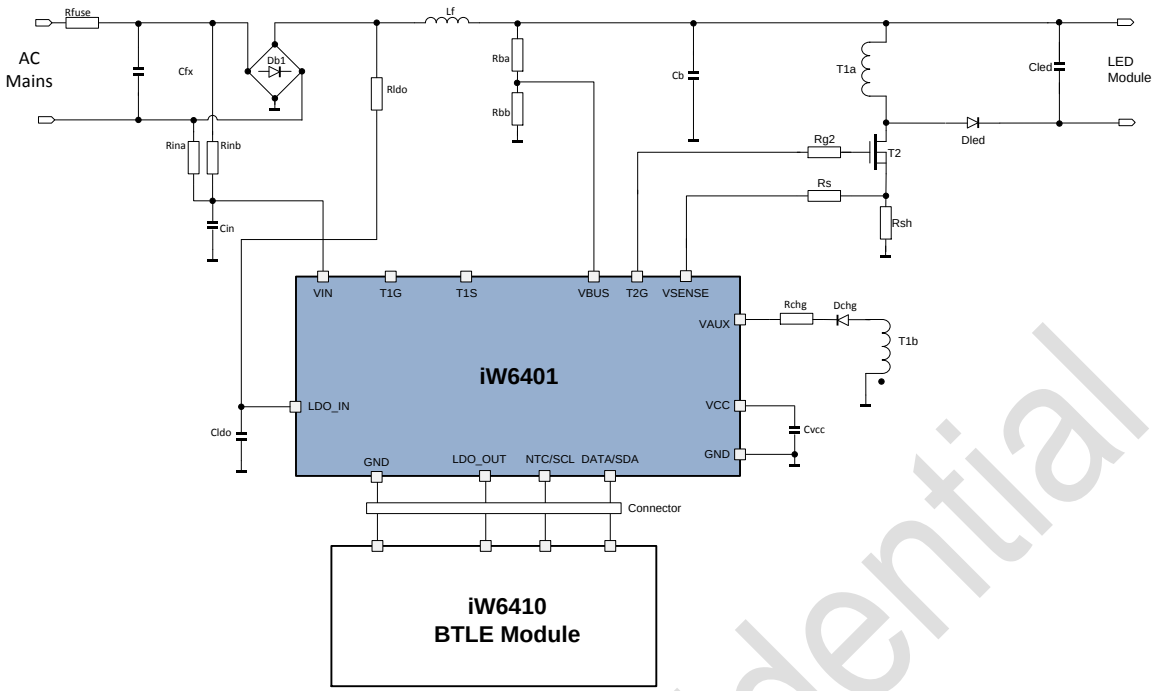


Figure 46: Application diagram with Bluetooth module and passicve startup

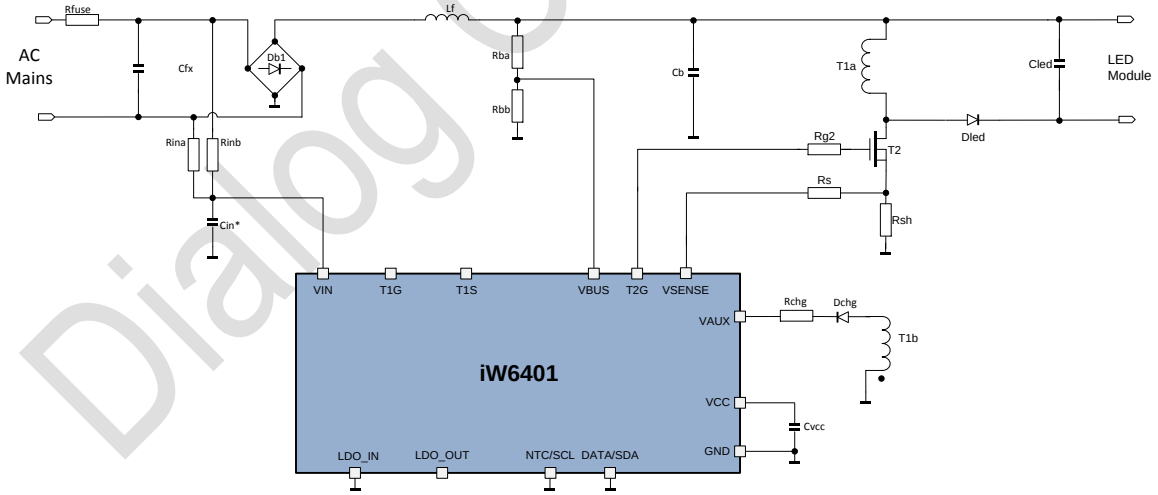


Figure 47: Application diagram with single flyback stage and passive startup

13 Package information

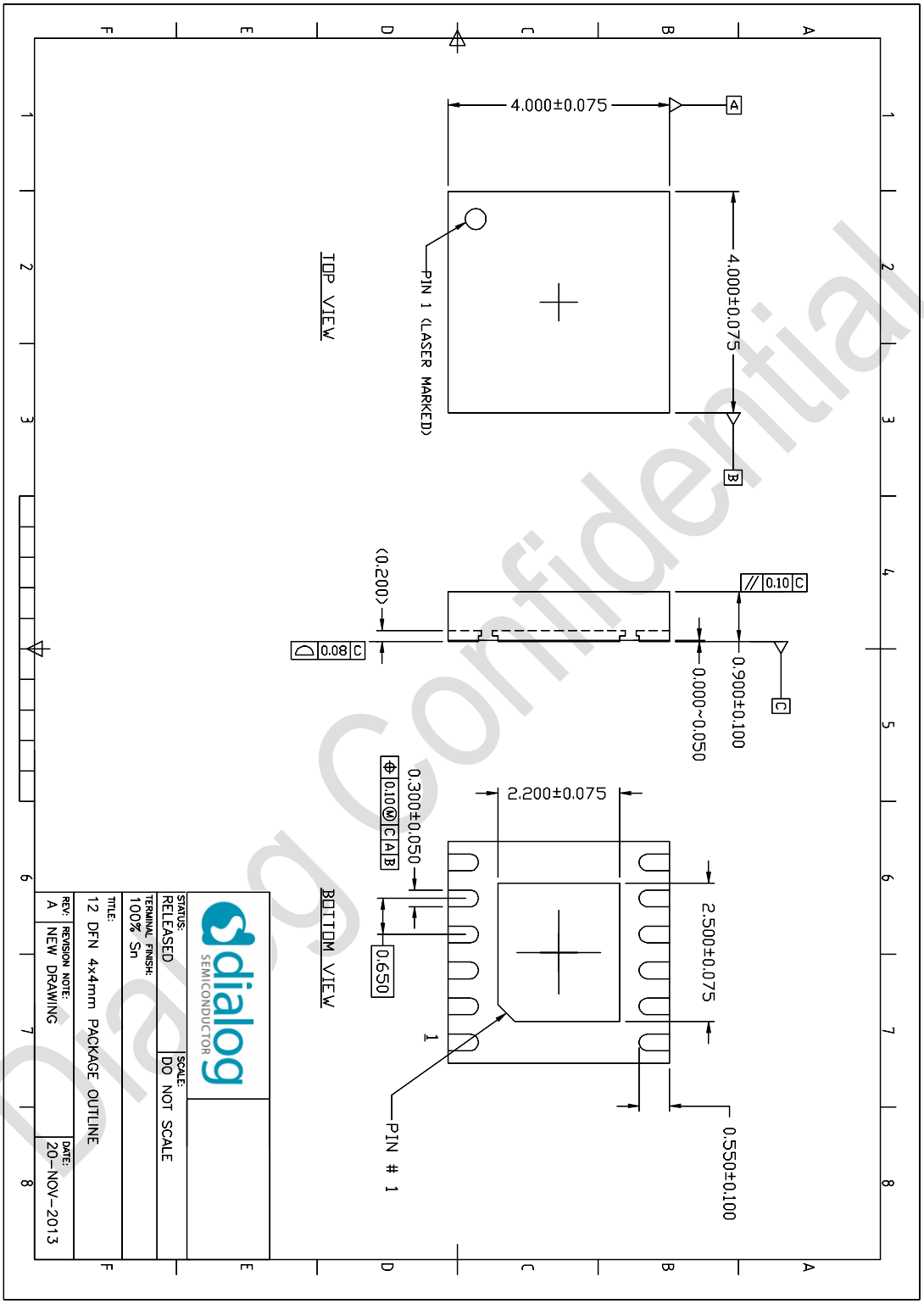


Figure 48: DFN12 package outline drawing

14 Ordering information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult the customer portal or your local sales representative.

Table 12: Ordering information

Part Number Note 1	Package Name	Package Description	Package Outline
iW6401-01A71	DFN12	Dual in-line flat no-lead package; 12 terminals	Figure 48
iW6401-01A72	DFN12	Dual in-line flat no-lead package; 12 terminals	Figure 48

Note 1 Legend: Part number iW6401-01A71 is for parts on tray
Part number iW6401-01A72 is for parts on tape and reel

15 Revision history

Revision	Date	Description
3.0	22 May 2015	First release.

Status definitions

Revision	Datasheet status	Product status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterisation data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via Customer Product Notifications.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

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