High Efficiency, Ultra-Low Quiescent Current and Ultra-Low Output Ripple Buck Regulator

General Description

DA9232 is a high efficiency, ultra-low quiescent current and ultra-low output ripple buck regulator in a compact I^2C configurable WLCSP package targeting battery powered applications needing low ripple and highly efficient power supplies.

The battery life of these devices is significantly improved due to the low quiescent current delivered by DA9232 during operation and shutdown.

The buck regulator extends high light load efficiency down to 10µA further extending battery life. Dynamic Voltage Control in the Buck regulator facilitates optimization across the system power modes enabling further improvement in System efficiency and battery life.

DA9232 provides multiple protection features and comes with the ability to monitor the events and indicators in the GPO pin.

Suitable for space constrained applications, the DA9232 comes in a 1.70 mm x 1.30 mm x 0.5 mm, 12-pin WLCSP package.

Key Features

- 60mA buck regulator
  - 750nA total input current (buck enabled, no load)
  - Up to 81% efficiency at 1.8V output, 10µA load currents
  - Input voltage 2.5V to 5.5V (Minimum 2.75V for start-up)
  - Output voltage 0.6V to 1.9V
  - Dynamic Voltage Control (DVC)
- I^2C interface for device configuration and control
- Protection features and System Monitors
- Small 1.7 mm x 1.3 mm x 0.5 mm, 12-pin WLCSP package

Applications

- Wearables – wrist wear, hearables
- Smart devices - thermostats and door locks
- Smoke detectors
- Portable medical devices
- Remote sensors
- High efficiency, low power applications

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1 Terms and Definitions

CDM	Charged Device Model
DC	Direct Current
DCM	Discontinuous Conduction Mode
FET	Field Effect Transistor
NMOS	N-channel Metal-Oxide-Semiconductor
OTP	One-Time Programmable (memory)
PMIC	Power Management IC
PMOS	P-channel Metal-Oxide-Semiconductor
R/W	Read/Write
SCL	Serial Clock SDA
T&R	Tape and Reel
UVLO	Under-Voltage Lock Out
WLCSP	Wafer-Level Chip-Scale Package

2 Block and Application Diagrams

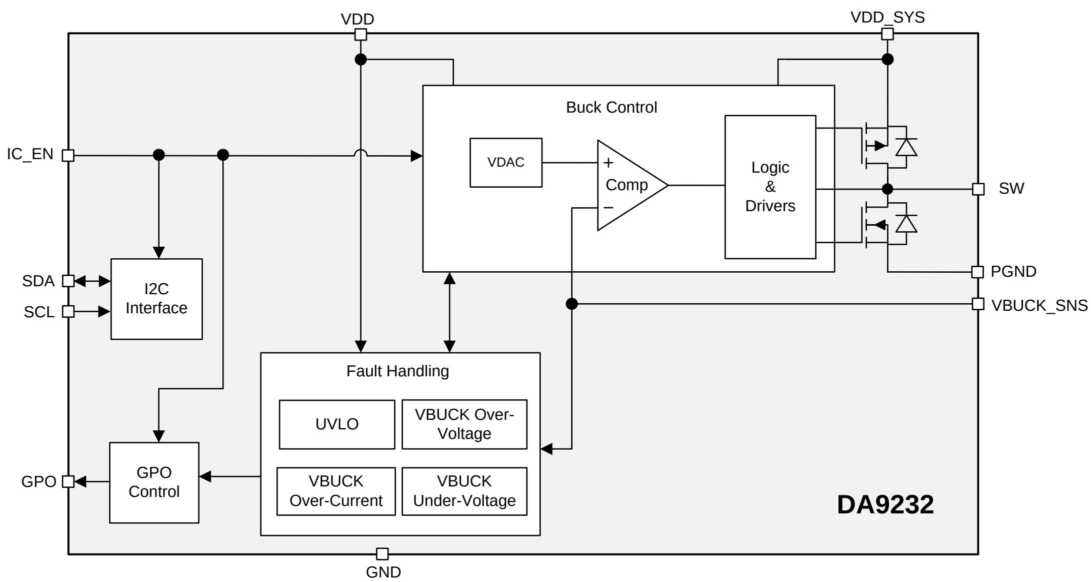


Figure 1: Block Diagram

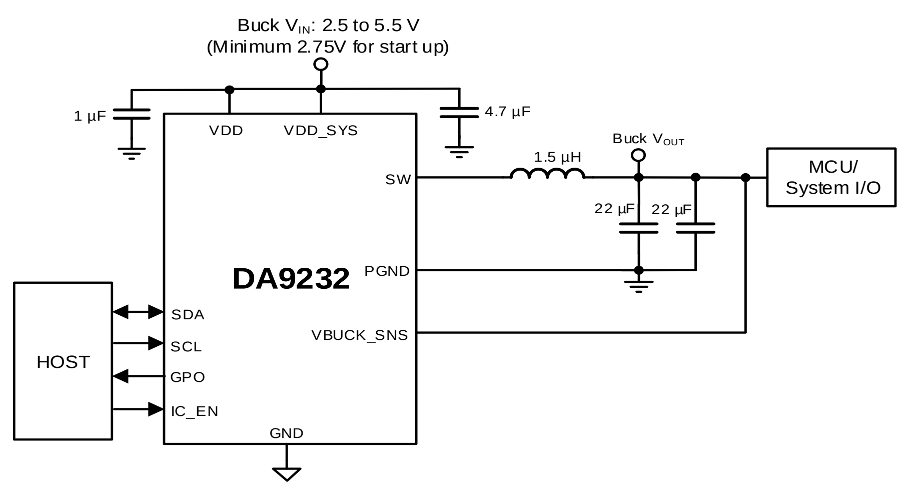


Figure 2: DA9232 Application Diagram

3 Pinout

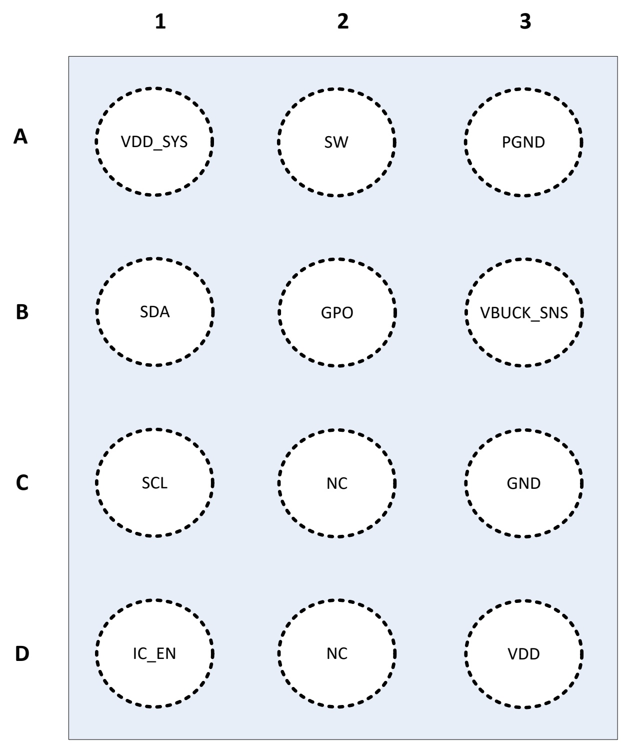


Figure 3: Pinout Diagram (Top View)

Table 1: Pin Description

Pin #	Pin Name	Type (See Table 2)	Drive (mA)	Reset State	Description
A1	VDD_SYS	AI			Buck V_{IN}
A2	SW	AIO			Buck switch node
A3	PGND	AIO			Buck ground
B1	SDA	DIO			I^2C serial data
B2	GPO	DO			General purpose output
B3	VBUCK_SNS	AI			Buck V_{OUT} /feedback voltage
C1	SCL	DI			I^2C serial clock
C2	NC				No connection
C3	GND	AI			Analog ground
D1	IC_EN	DI			Chip enable

Pin #	Pin Name	Type (See Table 2)	Drive (mA)	Reset State	Description
D2	NC				No connection
D3	VDD	AI			Analog V_{IN}

Table 2: Pin Type Definition

Pin Type	Description	Pin Type	Description
DI	Digital Input	AI	Analog Input
DO	Digital Output	AO	Analog Output
DIO	Digital Input / Output	AIO	Analog Input / Output
DIOD	Digital Input / Output open Drain	BP	Back drive Protection
PU	Fixed pull-up resistor	SPU	Switchable pull-up resistor
PD	Fixed pull-down resistor	SPD	Switchable pull-down resistor

4 Absolute Maximum Ratings

Table 3: Absolute Maximum Ratings

Symbol	Description	Conditions	Min	Max	Unit
T_{STG}	Storage temperature		-65	150	°C
T_J	Operating junction temperature		-40	125	°C
VDD	Analog V_{IN} pin	Tied to VDD_SYS	-0.3	6	V
VDD_SYS	Power V_{IN} pin	Tied to VDD	-0.3	6	V
I/O pins	Maximum voltage	I/O pin voltage ≤ VDD	-0.3	6	V

Stresses beyond those listed under Absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5 Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
VDD	Analog V_{IN}	Tied to VDD_SYS	2.5 Note 1		5.5	V
VDD_SYS	Power V_{IN}	Tied to VDD	2.5 Note 1		5.5	V
I_{OUT}	Load Current	Output current from SW pin, continuous DC current			60	mA

Note 1 Requires minimum 2.75V for start-up. Once started, input voltage can go down to 2.5V.

6 ESD Ratings

Parameter	Description	Conditions	Value	Unit
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 Note 2	± 2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 Note 3	± 500	

Note 2 JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

Note 3 JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7 Electrical Characteristics

VDD = VDD_SYS = 3.6 V, T_A= -40°C to 85°C. Typical values are at T_A = 25°C (unless otherwise noted).

Table 5: Input Current

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Electrical performance						
$I_{Q\_BUCK\_ON\_NO\_LD}$	Buck no load quiescent current	-40 °C < T_A < 85 °C Buck enabled and regulating, no load 2.5 V ≤ V_{VDD_SYS} ≤ 5.5 V V_{BUCK} = 1.8 V		0.75	3.5	µA

Table 6: Buck Output

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Electrical performance						
R_{ON_PMOS}	On resistance of PMOS pass device	V_{VDD_SYS} = 3.6 V I_{OUT} = 50 mA		600	800	mΩ
R_{ON_NMOS}	On resistance of NMOS pass device	V_{VDD_SYS} = 3.6 V I_{OUT} = 50 mA		300	450	mΩ
R_{SYS_DHCG}	MOSFET on-resistance for buck discharge	V_{VDD_SYS} = 3.6 V I_{OUT} = -10 mA into VOUT pin		33		Ω
t_{START}	Buck start-up time	V_{VDD_SYS} = 3.6 V V_{BUCK} = 1.8 V I_{OUT} = 0 A from BUCK_EN = 1 to switching start		3		ms
$I_{LIM\_SW\_PMOS}$	SW current limit PMOS	V_{VDD_SYS} = 3.6 V V_{BUCK} = 1.8 V		550		mA
f_{SW}	Switching frequency in continuous conduction mode				1.5	MHz
$I_{LIM\_PMOS\_SOFTSTART}$	PMOS switch current limit during soft-start	Current limit is reduced during soft-start		250		mA
$V_{OUT\_VBUCK\_SNS}$	Buck output voltage range	Programmable range, 50 mV steps	0.6		1.9	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{OUT\_VBUCK\_SNS\_HI}$	Buck output voltage range	HI programmable range, 50 mV steps $V_{OUT\_RANGE\_HI}$ = 1	1.3		1.9	V
$V_{OUT\_VBUCK\_SNS\_LO}$	Buck output voltage range	LO programmable range, 50 mV steps $V_{OUT\_RANGE\_HI}$ = 0	0.6		1.3	V
$V_{OUT\_VBUCK\_ACC\_HI}$	Buck output voltage accuracy (Note 1)	V_{VDD_SYS} = 2.5 - 5.5V I_{OUT} = 0 - 60 mA $V_{OUT\_RANGE\_HI}$ = 1 V_{BUCK} = 1.8 V	-1.5		1.5	%
$V_{OUT\_VBUCK\_ACC\_LO}$	Buck output voltage accuracy (Note 1)	V_{VDD_SYS} = 2.5 - 5.5 V I_{OUT} = 0 - 60 mA $V_{OUT\_RANGE\_HI}$ = 0 V_{BUCK} = 0.7 V	-2.5		2.5	%

Note 1: Includes all variations caused by Line and Load Regulations, Ripple and Temperature.

Table 7: GPO - Electrical performance

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PD}	GPO pull-down resistance	V_{VDD_SYS} = 3.6 V		12		Ω
V_{OH}	GPO Output high voltage	V_{PULLUP} = 1.8 V	1.4			V
V_{OL}	GPO Output low voltage	V_{PULLUP} = 1.8 V			0.4	V

Table 8: Analog Core - Electrical performance

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{TH_UVLO}	Under-voltage lockout threshold	Input voltage falling	2.4		2.5	V
$V_{TH\_UVLO\_RISE}$	Under-voltage lockout threshold rising.	Input voltage rising.			2.75	V
V_{HYS_UVLO}	Under-voltage lockout hysteresis	Input voltage rising		200		mV

Table 9: I2C interface

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Electrical performance						
f_{I2C_CLK}	I^2C bus specification standard and fast mode frequency support		100		400	kHz
$V_{IN\_HI\_THR}$	Input high threshold level for SDA and SCL		1.4			V
$V_{IN\_LO\_THR}$	Input low threshold level for SDA and SCL				0.4	V
$V_{OUT\_LO\_THR}$	Output low threshold level for SDA				0.4	V
I_{LKG_HILVL}	High-level leakage current for SDA and SCL.	$V_{PU} = V_{VDD}$ SDA and SCL			1	µA

8 Thermal Characteristics

Table 10: Thermal Characteristics

Parameter	Description	Conditions	Typ	Unit
R_{TH_JA}	Junction-to-ambient thermal resistance	JEDEC 6-layer pcb, no airflow	73.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	JEDEC 6-layer pcb, no airflow	6.66	°C/W
R_{TH_JB}	Junction-to-board thermal resistance	JEDEC 6-layer pcb, no airflow	34.8	°C/W

9 Typical Operating Characteristics

Test Circuit of Figure 2, Buck V_{IN} = VDD_SYS = VDD, T_A = 25°C, unless specified otherwise.

9.1 Buck No Load Quiescent Current vs Temperature, Device is Switching

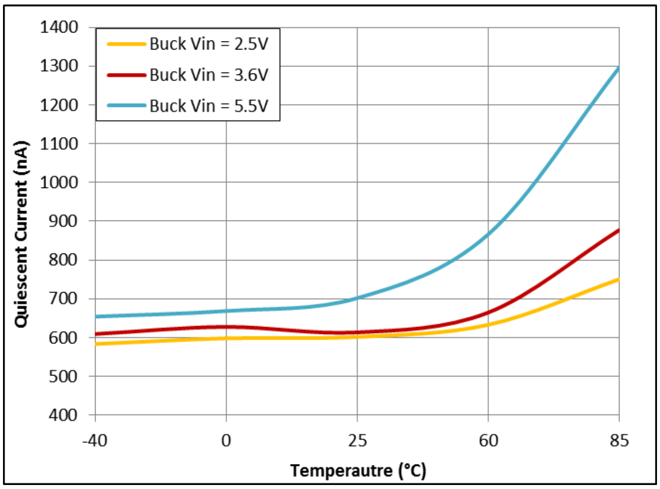


Figure 4: Buck V_{OUT} = 1.8 V

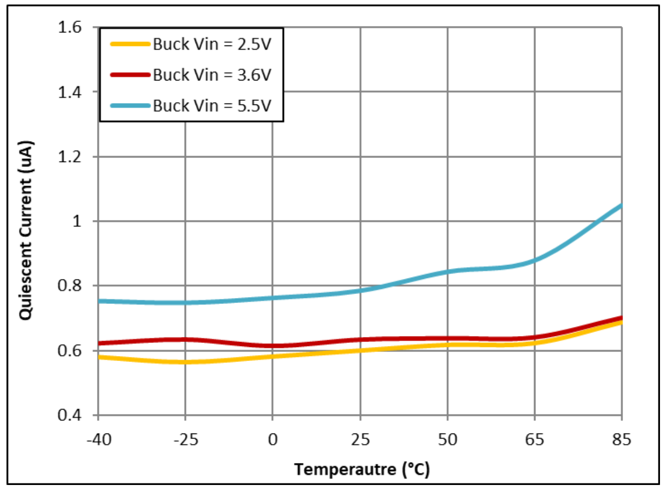


Figure 5: Buck V_{OUT} = 0.7 V

9.2 RDSon vs Temperature

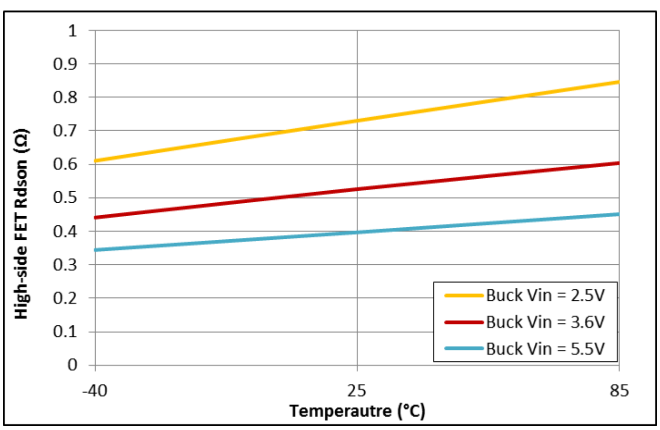


Figure 6: High-Side FET

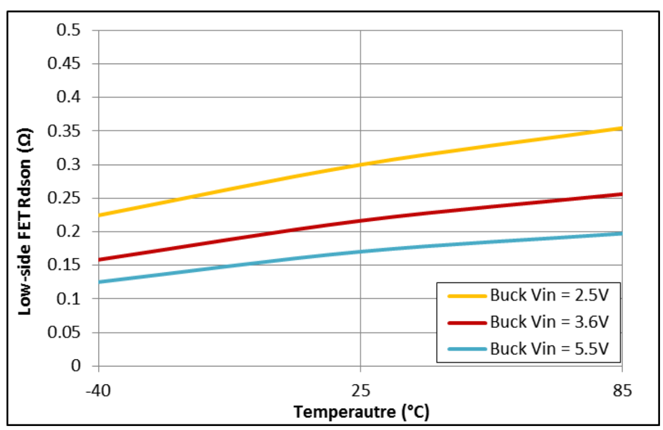


Figure 7: Low-Side FET

9.3 Efficiency vs Load Current

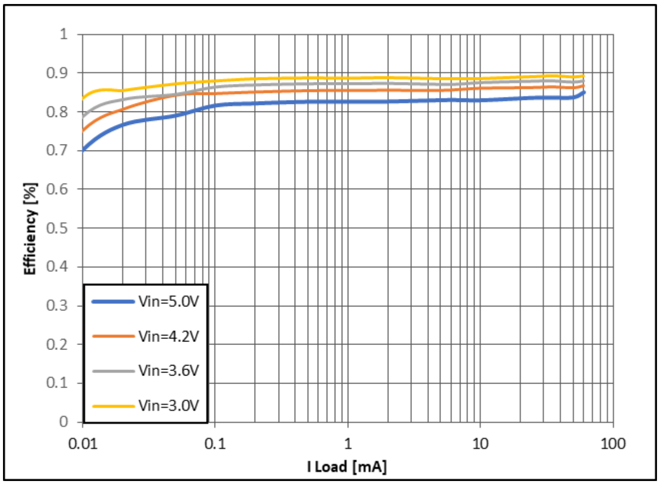


Figure 8: Buck V_{OUT} = 1.8 V

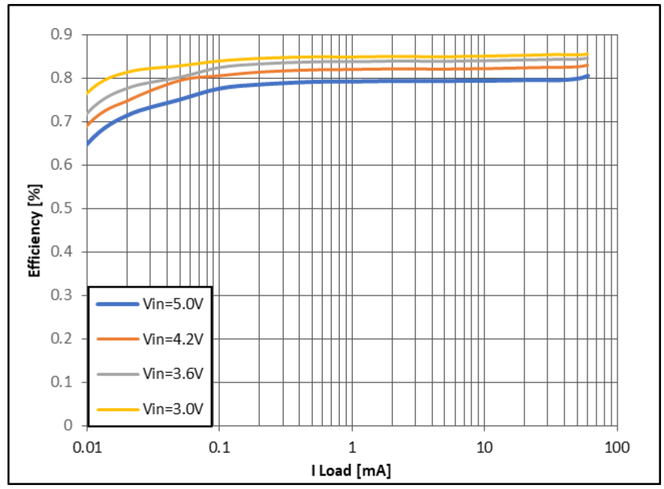


Figure 9: Buck V_{OUT} = 1.2 V

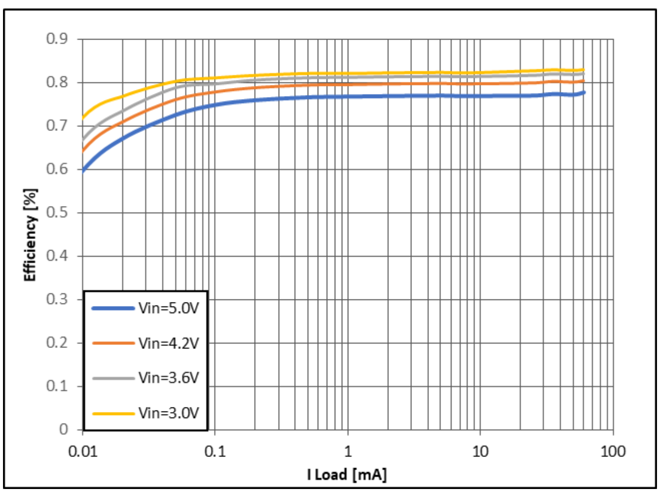


Figure 10: Buck V_{OUT} = 0.9V

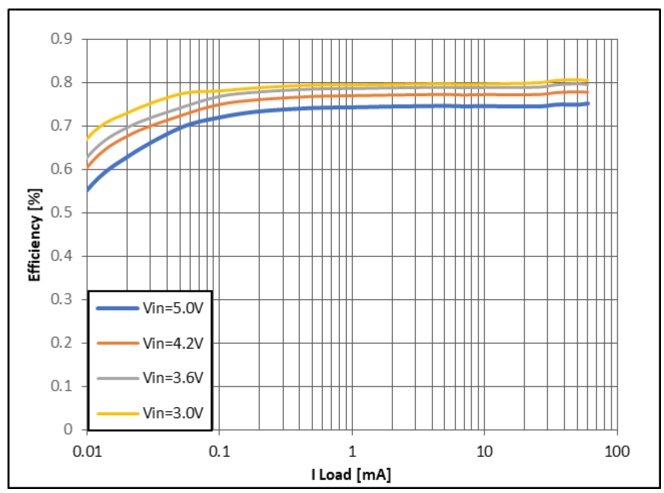


Figure 11: Buck V_{OUT} = 0.7 V

9.4 Switching Frequency vs Load Current

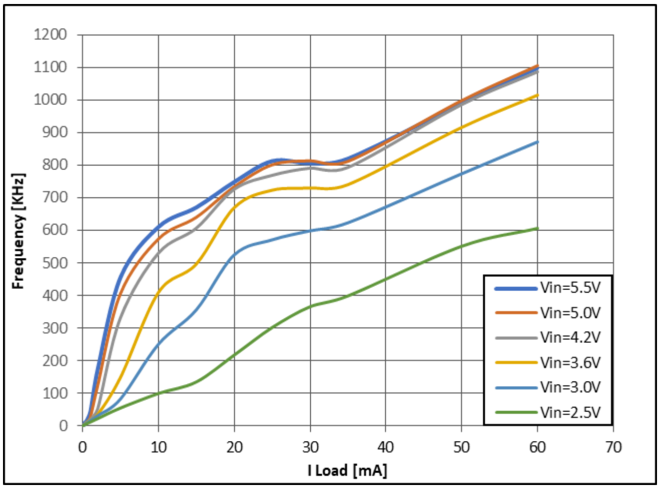


Figure 122: Buck V_{OUT} = 1.8 V

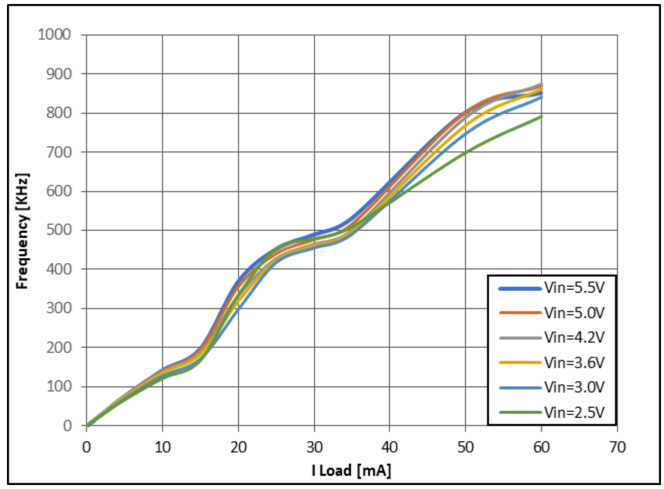


Figure 133: Buck V_{OUT} = 1.2 V

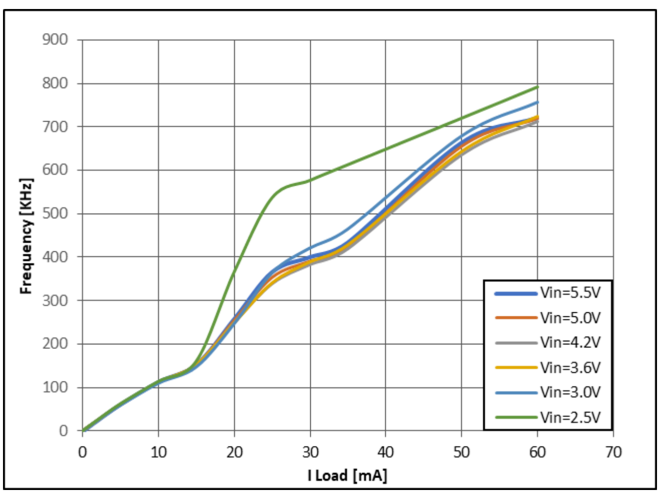


Figure 144: Buck V_{OUT} = 0.9 V

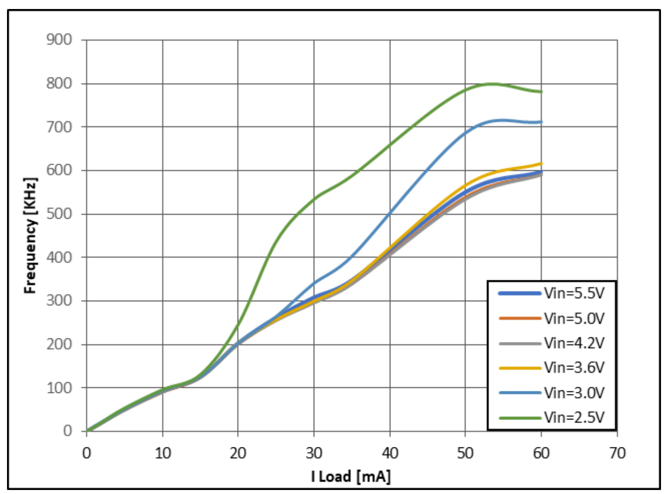


Figure 15: Buck V_{OUT} = 0.7 V

9.5 Buck V_{OUT} Ripple vs Load Current

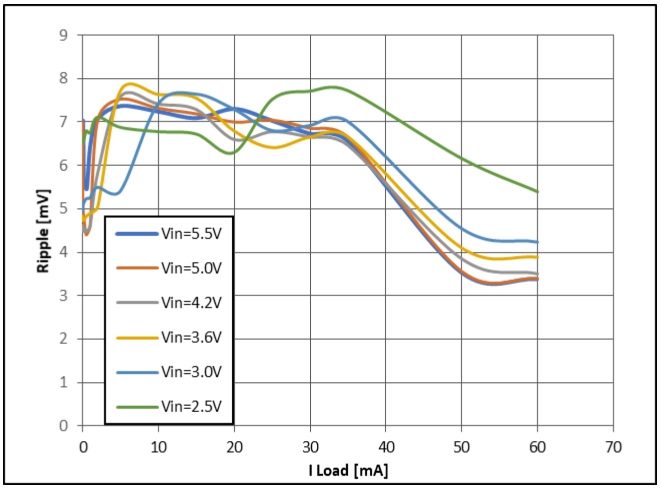


Figure 166: Buck V_{OUT} = 1.8 V

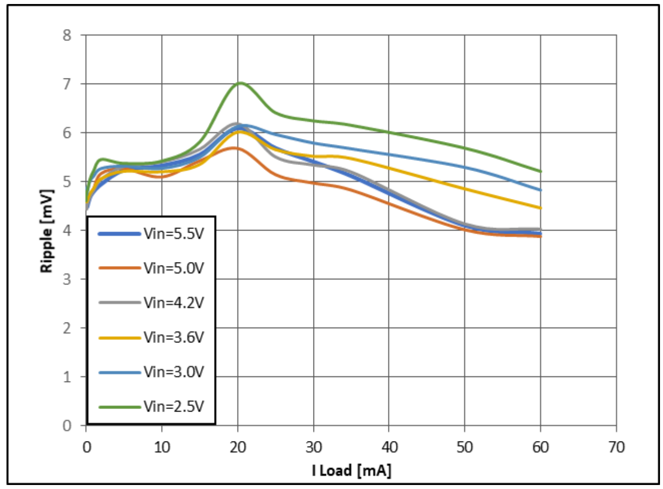


Figure 17: Buck V_{OUT} = 1.2 V

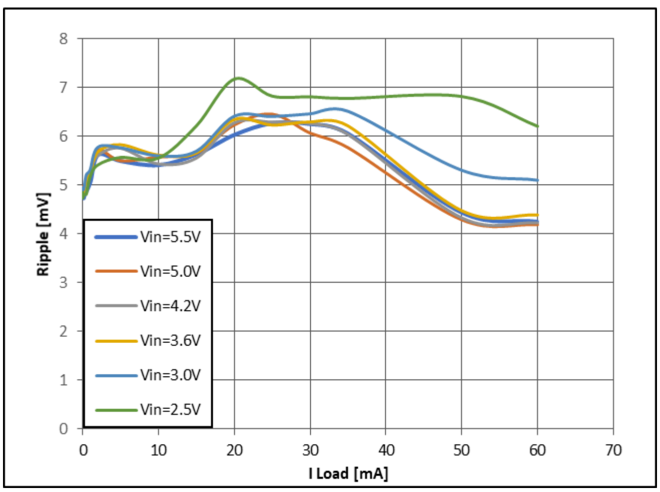


Figure 18: Buck V_{OUT} = 0.9 V

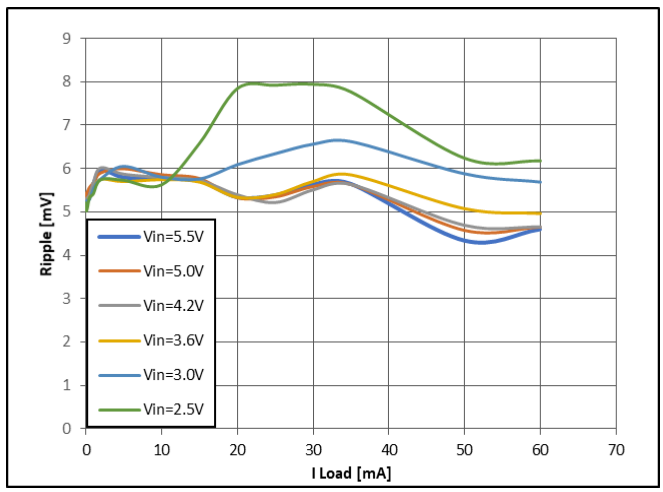


Figure19: Buck V_{OUT} = 0.7 V

9.6 Buck V_{OUT} vs Load Current

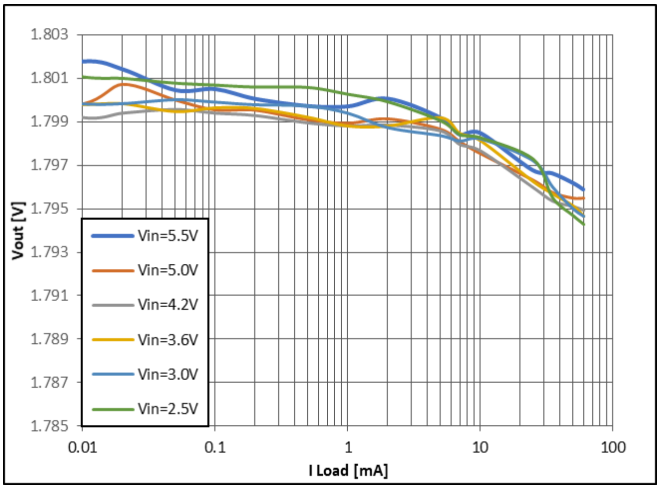


Figure 180: Buck V_{OUT} = 1.8 V

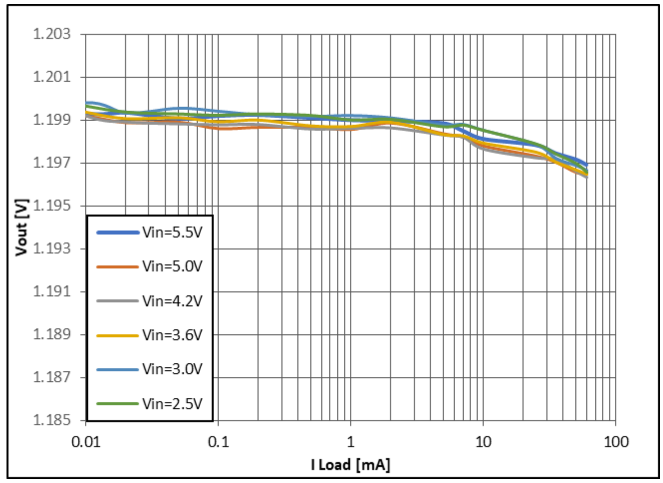


Figure 191: Buck V_{OUT} = 1.2 V

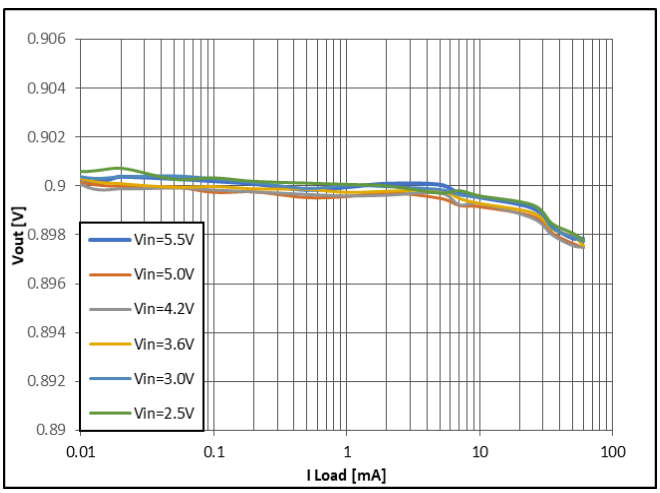


Figure 22: Buck V_{OUT} = 0.9 V

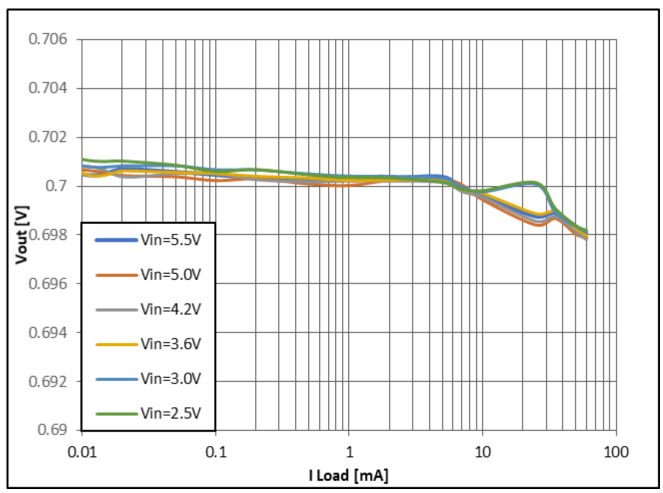


Figure 23: Buck V_{OUT} = 0.7 V

9.7 Typical Mode Operation

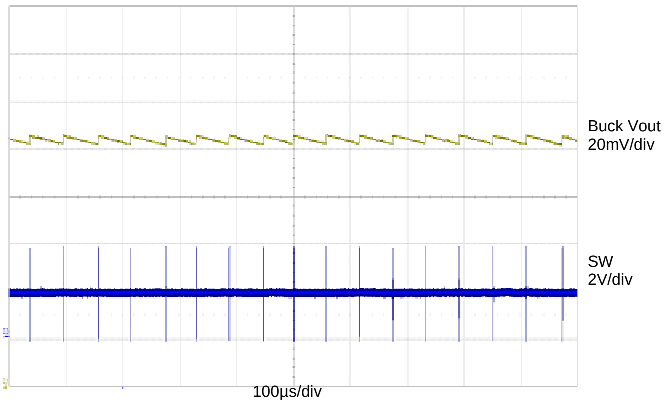


Figure 204: Buck V_{IN} = 3.6 V, Buck V_{OUT} = 1.8 V, Buck I_{LOAD} = 1 mA

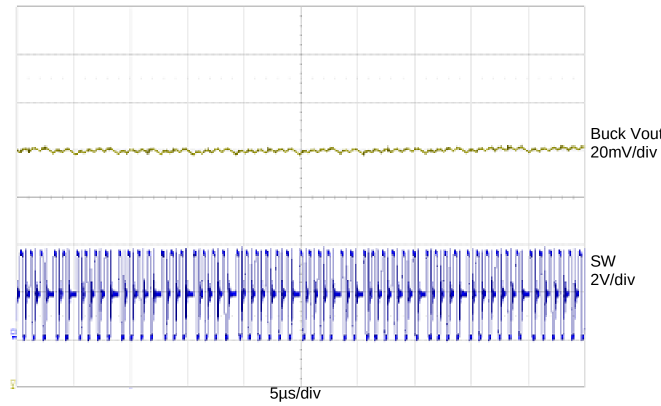


Figure 215: Buck V_{IN} = 3.6 V, Buck V_{OUT} = 1.8 V, Buck I_{LOAD} = 60 mA

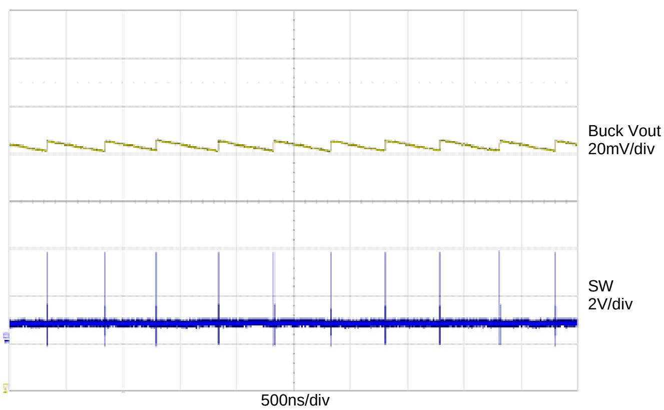


Figure 226: Buck VIN = 3.6 V, Buck VOUT = 0.7 V, Buck I_{LOAD} = 1 mA

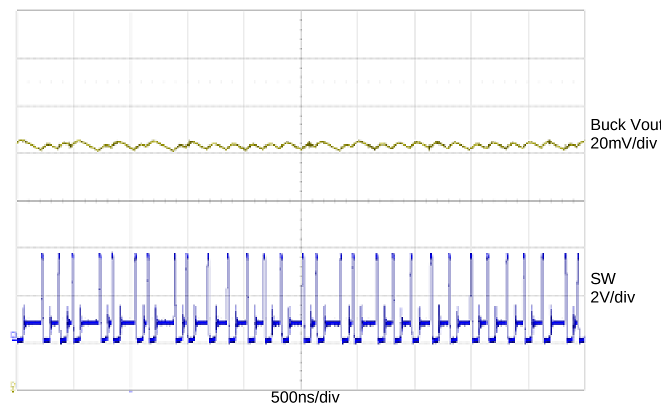


Figure 237: Buck V_{IN} = 3.6 V, Buck V_{OUT} = 0.7 V, Buck I_{LOAD} = 60 mA

9.8 Buck Load Transient Response

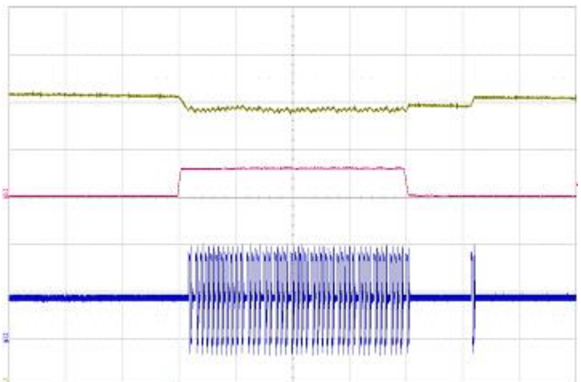


Figure 248: Buck I_{LOAD} = 0.5 mA to 60 mA to 0.5 mA (0.1A/µs); Buck V_{IN} = 3.6 V, Buck V_{OUT} = 1.8 V

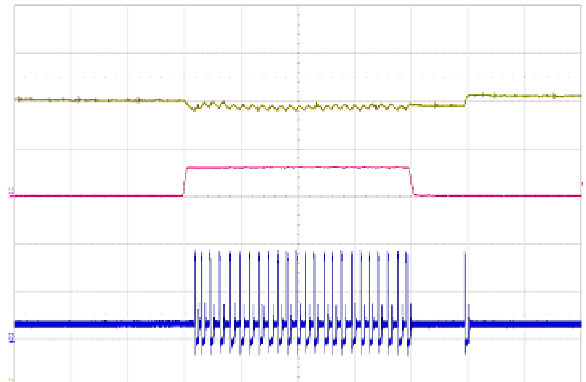


Figure 29: Buck I_{LOAD} = 0.5 mA to 60 mA to 0.5 mA (0.1A/µs); Buck V_{IN} = 3.6 V, Buck V_{OUT} = 0.7 V

9.9 Buck Dynamic Voltage Control

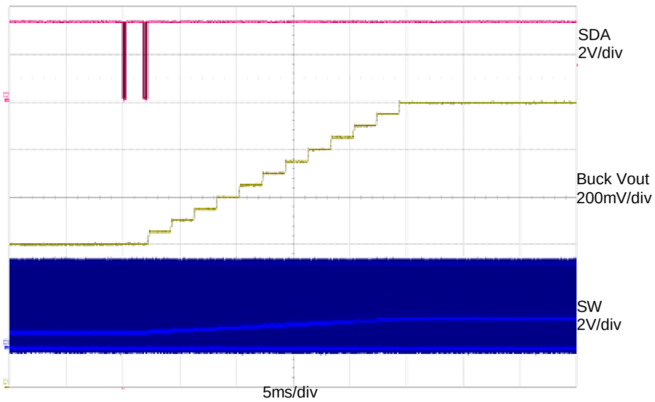


Figure 250: Buck V_{OUT} 0.6 V to 1.2 V; Buck V_{IN} = 3.6 V, Buck I_{LOAD} = 60 mA

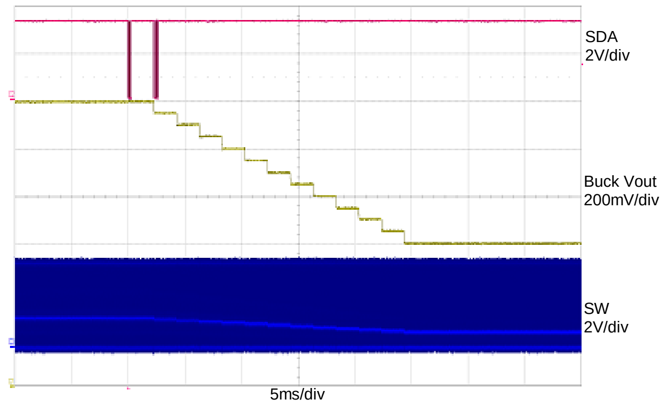


Figure 261: Buck V_{OUT} 1.2 V to 0.6 V; Buck V_{IN} = 3.6 V, Buck I_{LOAD} = 60 mA

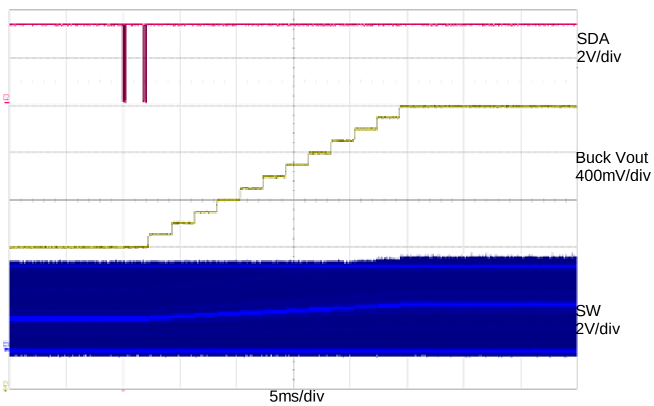


Figure 272: Buck V_{OUT} 1.3 V to 1.9 V; Buck V_{IN} = 3.6 V, Buck I_{LOAD} = 60 mA

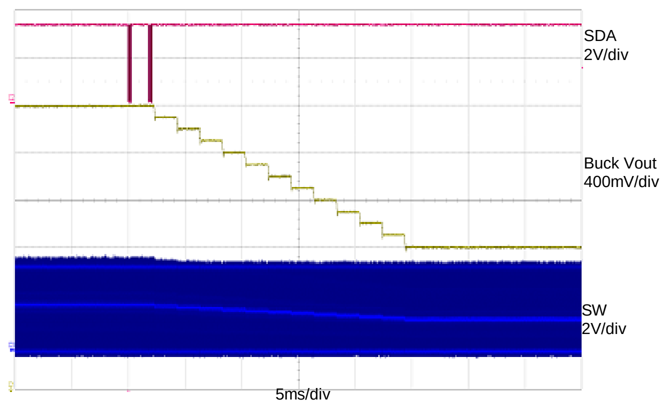


Figure 33: Buck V_{OUT} 1.9 V to 1.3 V; Buck V_{IN} = 3.6 V, Buck I_{LOAD} = 60 mA

9.10 Device Enable and Start up

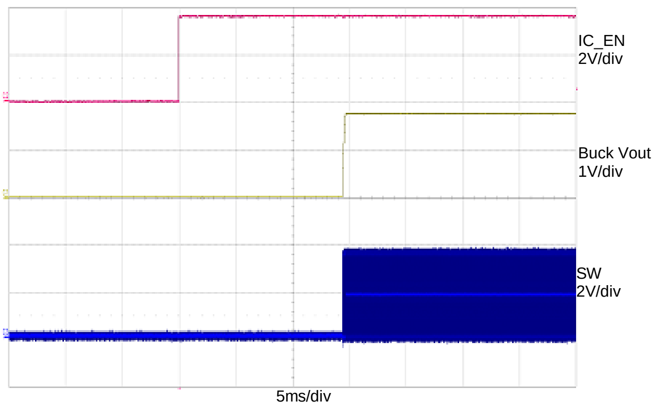


Figure 34: Device Enable: Buck V_{IN} = 3.6 V, Buck V_{OUT} 1.8 V, Buck I_{LOAD} = 60 mA

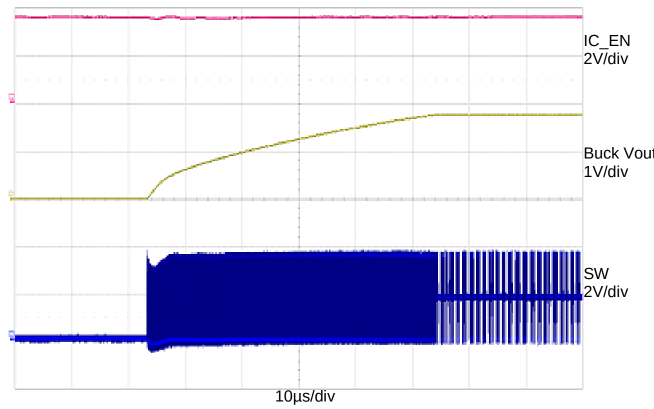


Figure 35: V_{OUT} ramp-up after Enabled (Zoom-in of Figure34)

10 Feature Descriptions

10.1 Chip Enable and Disable Through IC_EN

DA9232 features a dedicated IC_EN pin to enable and disable the chip. When IC_EN = high, the device is turned on. IC_EN voltage should not exceed VDD_SYS voltage on the device. When EN = low, the device is shut down completely, including I^2C communications.

10.2 VDD Under-Voltage Lockout

DA9232 features an under-voltage lockout (UVLO) on VDD. When VDD falls below UVLO falling threshold, buck is disabled, see Section 10.3.9 for fault behaviour and control, A VIN_UV_Event will be flagged if it is not masked. When VDD rises above the UVLO rising threshold, the device will be alive. VDD should be always tied to VDD_SYS on the PCB board so both VDD and VDD_SYS will share the same UVLO protection.

10.3 Buck Regulator

DA9232 includes a nano-ampere standby buck regulator with an adjustable output voltage, Dynamic Voltage Scaling capability and a maximum load current of 60 mA. It also has power saving mode operation and different protection features.

10.3.1 Buck Output Voltage Programmability

The DA9232 buck regulator can be set to two different ranges based on the value of VOUT_RANGE_HI. The value of BUCK_VOUT<4:0> is locked to a certain range based on the value of VOUT_RANGE_HI, and VOUT_RANGE_HI can only be changed while the buck is disabled. The buck can be set to the output voltages shown in Table 11. If a command is received outside of the allowable range (that is above 1.3 V for VOUT_RANGE_HI = 0 or below 1.3 V for VOUT_RANGE_HI = 1), digital will force the value of BUCK_VOUT<3:0> to 01110 (1.3 V).

Table 11: Buck Output Voltage Settings

VOUT_RANGE_HI	BUCK_VOUT<4:0>	Buck Output Voltage (V)
0	00000	0.60
0	00001	0.65
0	00010	0.70
0	00011	0.75
0	00100	0.80
0	00101	0.85
0	00110	0.90
0	00111	0.95
0	01000	1.00
0	01001	1.05

VOUT_RANGE_HI	BUCK_VOUT<4:0>	Buck Output Voltage (V)
0	01010	1.10
0	01011	1.15
0	01100	1.20
0	01101	1.25
0 or 1	01110	1.30
1	01111	1.35
1	10000	1.40
1	10001	1.45
1	10010	1.50
1	10011	1.55
1	10100	1.60
1	10101	1.65
1	10110	1.70
1	10111	1.75
1	11000	1.80
1	11001	1.85
1	11010	1.90
1	11011	1.90
1	11100	1.90
1	11101	1.90
1	11110	1.90
1	11111	1.90

10.3.2 Start-up Operation

DA9232 buck integrates a start-up circuit to minimize output voltage over-shoot and input voltage drop during start-up. When writing 1 to BUCK_EN (Bit 7 of Reg0x05), the buck is enabled and starts switching after a typical delay time of 3 ms. During start-up, the cycle-by-cycle current limit is reduced to limit inrush current.

10.3.3 Power Saving Mode Operation

DA9232 buck regulator features power saving mode that greatly reduces the quiescent current when device has very light load condition. Buck regulator operates in discontinuous mode with Pulse Frequency Modulation (PFM). The low-side FET will be turned off based on a zero-crossing comparator to prevent negative inductor current flowing through the FET which can result in additional conduction loss. If both FETs remain in the OFF state for a certain delay time after inductor current crosses zero, the device will enter power saving mode. In power saving mode, DA9232 shuts down most of the internal circuitry to save current consumption. The lighter the load, the longer the duration of power saving mode will be, to achieve the lowest quiescent current and improve light load efficiency.

10.3.4 Dynamic Voltage Control

DA9232 buck regulator has dynamic voltage control (DVC) feature which allows the buck output voltage to track the internal reference voltage when it changes at a rate of 50 mV/2 ms. Since the buck output voltage can only be changed within an allowable range while still keeping the buck enabled, DVC also follows the same behaviour. The DVC is done via I^2C, whereby the buck output voltage setting is stepped in 50 mV steps within either the low range or high range. Each voltage step lasts for 2 ms.

10.3.5 Cycle-by-cycle Over-Current Protection

For the Over-current Protection (OCP) in DA9232, the peak current through high-side FET is monitored cycle-by-cycle. When the sensed current exceeds the pre-set current limit, the high-side FET will be turned OFF immediately to limit the inductor current. The high-side FET will be turned on again after the constant-off time expires. If the OC condition persists for 64 µs, buck will be forced off and buck output will be pull-down until the fault clears, see Section 10.3.9 for fault behavior and control and Section 10.3.8 for output voltage discharge and control. An OC_BUCK_Event will be flagged if it is not masked.

10.3.6 Output Over-Voltage Protection

DA9232 features an output over-voltage protection (OVP) to protect the load from damage. When both IC_EN and BUCK_EN are high and the buck output voltage is 200 mV greater than the internal reference voltage, the high side FET is immediately OFF, see Section 10.3.9 for fault behavior and control. Then the internal buck output discharge FET will be turned on to discharge buck output capacitor, see Section 10.3.8 for output voltage discharge and control. An OV_BUCK_Event will be flagged if it is not masked. Buck will remain off and buck output will be pull-down until the fault is cleared.

10.3.7 Output Under-Voltage Protection

When buck output short happens, inductor current will increase until the peak reaches the cycle-by-cycle current limit. Then the high-side FET turns OFF and low-side FET turns on. Since buck output is shorted, inductor current slope is very small during low-side FET on time. The inductor current could gradually go higher and higher. To effectively prevent the inductor current running away at V_{OUT} short condition, buck V_{OUT} is also monitored. If over-current condition happens and buck V_{OUT} drops 400 mV below the reference voltage, the buck regulator will be shut off immediately and an UV_BUCK_Event will be flagged if it is not masked, see Section 10.3.9 for fault behavior and control.

10.3.8 Automatic Output voltage Discharge

To speed up the discharging of buck output capacitor and ensure a safer start-up next time, the buck regulator provides automatic output voltage discharge when IC_EN is pulled low or buck shutdown caused by any fault. Automatic output discharge when buck is forced OFF by fault needs to set register bit BUCK_PD_CFG1 = 0; automatic output discharge when buck is disabled by

BUCK_EN = 0 needs to set register bit BUCK_PD_CFG2 = 0. The output of the buck regulator is discharged through VBUCK_SNS pin and an internal buck output discharge FET with typical 33 Ω resistance.

10.3.9 Event Flag and Fault Control

DA9232 has the flexibility for customers to control the behavior of buck when there is a fault condition. There are five register bits (UVLO_FRC_DIS, OV_DIS_BUCK, OC_BUCK_EVENT, SC_DIS_BUCK) controlling whether the buck will be disabled when the corresponding fault condition happens. In addition, users can choose whether to mask or unmask the event flag when the fault condition happens.

When there is a VDD Under-voltage condition, buck will be forced OFF if UVLO_FRC_DIS = 1. Buck will remain alive if UVLO_FRC_DIS = 0. During the VDD Under-voltage condition, the event register bit VIN_UV_EVENT = 1 if the corresponding mask register bit M_VIN_UV is set to 0 otherwise VIN_UV_EVENT = 0.

When there is an over-voltage fault at buck output, buck will be forced OFF if OV_DIS_BUCK = 1. Buck will continue switching if OV_DIS_BUCK = 0. During the fault, OV_BUCK_EVENT is set to 1 if M_OV_BUCK_EVENT = 0 otherwise OV_BUCK_EVENT = 0.

When the over-current condition in buck persists for 64 µs and M_OC_BUCK_EVENT is set to 0, OC_BUCK_EVENT will be set to 1. If OC_DIS_BUCK = 1, BUCK is forced disabled. If OC_DIS_BUCK = 0, buck will continue switching during the over-current condition.

When there is a buck Output under-voltage condition and M_UV_BUCK_EVENT = 0, UV_BUCK_EVENT is set to 1. If both buck output under-voltage and over-current condition exist and SC_DIS_BUCK = 1, buck will be forced OFF. If SC_DIS_BUCK = 0, buck will continue switching without shutting down by the under-voltage protection.

DA9232 also has a fault recovery mechanism that can be customized through the 3-bits RCVRY_NUM. This value determines the fault recovery trial number for buck and is counted down by every fault that triggers buck OFF. When RCVRY_NUM reaches 0, recovery trial is ended and buck will remain OFF even if the buck enable signals are toggled HI. If RCVRY_NUM is set to 0x7, there will be no count down on the recovery trial number and recovery trail will not be ended. Before RCVRY_NUM reaches 0, buck will be recovered automatically if the fault condition disappears.

Event flags are not automatically cleared when the fault conditions disappear. They have to be cleared by changing the values in register EVENT through I^2C.

10.4 I²C Programming

10.4.1 Interface Description

DA9232 includes an I²C compatible interface based on the following signals:

- SCL: standard 400 kHz I²C bus serial clock generated by the Host processor
- SDA: standard 400 kHz I²C bus serial address/data input output

SDA and SCL are open drain I/O terminals. The standard frequency of the I²C bus is 400 kHz in fast mode or 100 kHz in slow mode.

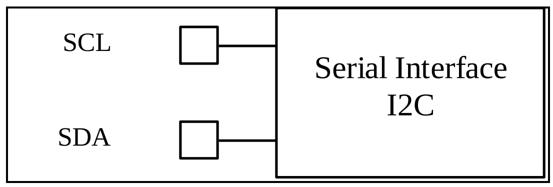


Figure 36: I²C Serial Interface Pins

The I²C bus is used to control most functions and change register values depending on the application requirements. In active battery, the I²C circuitry is powered from the battery. The interface maintains a proper operation as long as VDD_SYS is valid.

The device is compatible with the standard I²C protocol but only operates as a slave. The transfer protocol is the same whether operating in fast or slow mode.

10.4.2 Details of the I²C Protocol

The device supports 7-bit addressing only, the address is 0x2F. The 8-bit shifted address is 0x5E.
A timer runs during I²C transitions. If the timer expires while SDA is held low, all additional commands are ignored and the I²C state machine is reset. The timer is reset with a START condition and stopped with a STOP condition.
The I²C bus is monitored at all times for a valid SLAVE address, and an acknowledge bit is generated if the SLAVE address was true.

- A START condition is initiated by a high to low transition on the SDA line while the SCL is in the high state.
- A STOP condition is indicated by a low to high transition on the SDA line while the SCL is in the high state.
- An ACKNOWLEDGE is indicated by the receiver pulling the SDA line low during the following clock cycle.

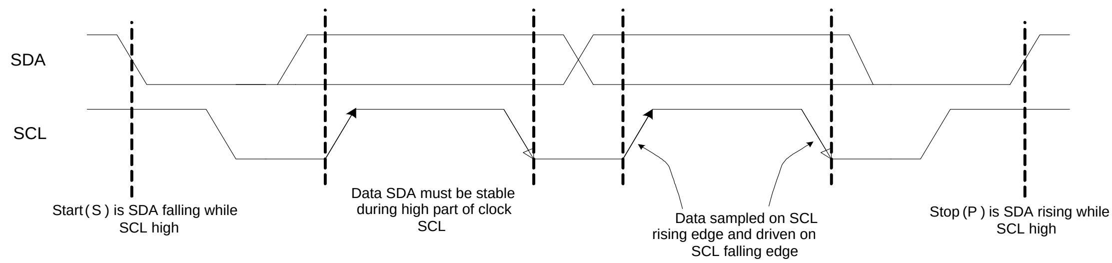


Figure 37: I²C Start and Stop Conditions

When the address is matching the following event sequence happens:

1. The device generates an ACKNOWLEDGE to indicate to the master that the communication link has been established
2. The master generates SCL clock cycles to transmit or receive data
3. After receiving data, an ACKNOWLEDGE is generated either by the device or the master (whichever is transmitting the data)
   A data sequence is 9-bit, consisting of 8-bit data and 1-bit ACKNOWLEDGE. It can be repeated as long as necessary.
4. The master generates a STOP condition to end the data transfer

The bus returns to IDLE-mode if during a message a new START or STOP condition occurs. Data is transmitted MSB first for both R/W operations.

10.5 GPO Pin Function Programming

DA9232 has a General-purpose output (GPO) pin which can be programmed to have multiple functions.

10.5.1 Power Good Indicator

When GPO pin is configured to the VDD power good indicator, it is an open drain output and can be configured to either active high or active low. When GPO status is Hi-Z, an external pull-up is required for GPO to be high.

Table 12: GPO as Power Good Indicator

GPO Configuration	$V_{IN} > V_{IN\_UVLO}$	GPO Status
Active High	No	0
	Yes	Hi-Z
Active Low	No	Hi-Z
	Yes	0

10.5.2 Event Indicator

GPO pin can also be configured as the event indicator in open drain output. Whenever there is an event or multiple events (VIN_UV_EVNT or OV_BUCK_EVENT or OC_BUCK_EVENT or UV_BUCK_EVENT) happen, GPO will be pulled down Low. This can be used as an interrupt to host CPU to inform events happened. When there is no event, GPO will remain in Hi-Z status and an external pull-up is required for GPO to be high.

10.5.3 Reset Pulse Generation

GPO pin can be configured to generate a reset pulse signal when buck starts. The reset signal can be used by host CPU or other device that are connected to buck output. When GPO is Low, it indicates a reset pulse period; when GPO is in Hi-Z status (An external pull-up is required for GPO to be high), it indicates a non-reset period.
There is also a timing control to negate the reset pulse signal. The GPO reset pulse width can be adjusted between 8 and 112 ms measured from written 1 to BUCK_EN register bit.

10.5.4 Always Pull-Down or Hi-Z

When GPO pin is not used, it can be configured to either always Hi-Z or pull-down to Low.

11 Register Overview

11.1 Register Map

11.1.1 Buck Control

Table 13: Event/Status/Mask and User Registers

User Registers									
Register	**Addr**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EVENT	0x0000	Reserved	VIN_UV_EVENT	Reserved	OC_BUCK_EVENT	OV_BUCK_EVENT	UV_BUCK_EVENT	Reserved	Reserved
STATUS	0x0002	Reserved	VIN_UV_STAT	Reserved	OC_BUCK_STAT	OV_BUCK_STAT	UV_BUCK_STAT	Reserved	BUCK_EN_STAT
MASK	0x0003	Reserved	M_VIN_UV	Reserved	M_OC_BUCK_EVENT	M_OV_BUCK_EVENT	M_UV_BUCK_EVENT	Reserved	Reserved
GPO	0x0004	GPO_RST_CTRL<3:0>				GPO_CTRL<3:0>			
BUCK	0x0005	BUCK_EN	VOUT_RANGE_HI	Reserved	BUCK_VOUT<4:0>				
BUCK_CFG	0x0006	Reserved	Reserved	BUCK_PD_CFG2	BUCK_PD_CFG1	Reserved	Reserved	SEL_BUCK_ILIM<1:0>	
FAULT_CTL	0x0008	SC_DIS_BUCK	OC_DIS_BUCK	OV_DIS_BUCK	TSD_FRC_DIS	UVLO_FRC_DIS	RCVRY_NUM<2:0>		
PIN_MONTOR	0x000A	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	GPO_OUT_MON

11.1.2 System Module

Table 14: System Reset Registers

User Registers									
Register	**Addr**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SYS_RST_EVENT	0x0001	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RESET_EVENT
SYS_SRST	0x0009	Reserved	Reserved	Reserved	Reserved	SRST<3:0>			
SYS_DEVICE_ID	0x0080	DEV_ID<7:0>							
SYS_VARIANT_ID	0x0081	MRC<3:0>				VRC<3:0>			
SYS_CONFIG_ID	0x0082	CONFIG_REV<7:0>							

11.2 Register Definitions

11.2.1 Buck Control

11.2.1.1 Event/Status/Mask Registers

Table 15: Register EVENT

Address	**Register Name**	**POR Value**	Event flag
0x0000	EVENT	0x00	

7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved	VIN_UV_EVENT	Reserved	OC_BUCK_EVENT	OV_BUCK_EVENT	UV_BUCK_EVENT	Reserved	Reserved

Field Name	Bits	Type	POR	Description
VIN_UV_EVENT	[6]	evnt	0x0	Under Voltage on VDD event flag. When Under Voltage (UVLO) condition is detected, this bit is set to 1. When I2C writes '1' to this bit, the event flag is cleared.
OC_BUCK_EVENT	[4]	evnt	0x0	Over Current on BUCK OUT event flag. When the buck Over Current condition is detected (when BUCK_EN==1 && M_OC_BUCK==0), this bit is set to 1. When I2C writes '1' to this bit, the event flag is cleared.
OV_BUCK_EVENT	[3]	evnt	0x0	Over Voltage on BUCK OUT event flag. When the buck Over Voltage condition is detected (when BUCK_EN==1 && M_OV_BUCK==0), this bit is set to 1. When I2C writes '1' to this bit, the event flag is cleared.
UV_BUCK_EVENT	[2]	evnt	0x0	Under voltage on BUCK OUT event flag. When the under voltage condition (i.e. short circuit) is detected on the buck (when BUCK_EN==1 && M_UV_BUCK==0), this bit is set to 1. When I2C writes '1' to this bit, this event flag is cleared.

Table 16: Register STATUS

Address	Register Name	POR Value	Status
0x0002	STATUS	0x00	

7	6	5	4	3	2	1	0
Reserved	VIN_UV_STAT	Reserved	OC_BUCK_STAT	OV_BUCK_STAT	UV_BUCK_STAT	Reserved	BUCK_EN_STAT

Field Name	Bits	Type	POR	Description
VIN_UV_STAT	[6]	virtual	0x0	Indicate present V_{IN} under-voltage status.
OC_BUCK_STAT	[4]	virtual	0x0	Indicate present BUCK VOUT over current status.
OV_BUCK_STAT	[3]	virtual	0x0	Indicate present BUCK VOUT over voltage status.

Field Name	Bits	Type	POR	Description
UV_BUCK_STAT	[2]	virtual	0x0	Indicate present BUCK VOUT under voltage status.
BUCK_EN_STAT	[0]	virtual	0x0	Indicate present Buck Enable status. 1:Buck enabled 0:Buck disabled

Table 17: Register MASK

Address	Register Name	POR Value	Mask
0x0003	MASK	0x7C	

7	6	5	4	3	2	1	0
Reserved	M_VIN_UV	Reserved	M_OC_BUCK_EVENT	M_OV_BUCK_EVENT	M_UV_BUCK_EVENT	Reserved	Reserved

Field Name	Bits	Type	POR	Description
M_VIN_UV	[6]	cfg OTP	0x1	Mask to set VIN_UV_EVNT. VIN_UV_STAT is updated regardless of this mask.
M_OC_BUCK_EVENT	[4]	cfg OTP	0x1	Masks to set OC_BUCK_EVENT. OC_BUCK_STAT is updated regardless of this mask.
M_OV_BUCK_EVENT	[3]	cfg OTP	0x1	Masks to set OV_BUCK_EVENT. OV_BUCK_STAT is updated regardless of this mask.
M_UV_BUCK_EVENT	[2]	cfg OTP	0x1	Masks to set UV_BUCK_EVENT. UV_BUCK_STAT is updated regardless of this mask.

11.2.1.2 User Registers

Table 18: Register GPO

Address	Register Name	POR Value	
0x0004	GPO	0x00	GPO control

7	6	5	4	3	2	1	0
GPO_RST_CTRL<3:0>				GPO_CTRL<3:0>			

Field Name	Bits	Type	POR	Description	
GPO_RST_CTRL	[7:4]	cfg OTP	0x0	Reset pulse signal nagate timing control	
				Value	**Description**
				0x0	8ms after BUCK_EN = 1, GPO reset pulse is negated.
				0x1	16ms after BUCK_EN = 1, GPO reset pulse is negated.
				0x2	32ms after BUCK_EN = 1, GPO reset pulse is negated.
				0x3	48ms after BUCK_EN = 1, GPO reset pulse is negated.
				0x4	64ms after BUCK_EN = 1, GPO reset pulse is negated.
				0x5	80ms after BUCK_EN = 1, GPO reset pulse is negated.
				0x6	96ms after BUCK_EN = 1, GPO reset pulse is negated.
				0x7	112ms after BUCK_EN = 1, GPO reset pulse is negated.
GPO_CTRL	[3:0]	cfg OTP	0x0	GPO Control	
				Value	**Description**

Field Name	Bits	Type	POR	Description	
				0x1	Reset Pulse generation output
				0x2	PowerGood indicator, Active Low
				0x3	PowerGood indicator, Active High
				0x4	Event indicator
				0x8	Force GPO output low
				0x9	Force GPO output hi-z

Table 19: Register BUCK

Address	Register Name	POR Value	Buck enable & vout control
0x0005	BUCK	0x58	

7	6	5	4	3	2	1	0
BUCK_EN	VOUT_RANGE_HI	Reserved	BUCK_VOUT<4:0>				

Field Name	Bits	Type	POR	Description	
BUCK_EN	[7]	cfg OTP	0x0	BUCK enable	
VOUT_RANGE_HI	[6]	cfg OTP	0x1	Range selection for buck. This can only be changed while BUCK_EN = 0	
				Value	**Description**
				0x0	0.60 V <= VBUCK <= 1.30 V
				0x1	1.30 V <= VBUCK <= 1.90 V
BUCK_VOUT	[4:0]	datablk OTP	0x18	Buck output voltage	

				Value	Description
				0x00	0.60 V
				0x01	0.65 V
				0x02	0.70 V
				0x03	0.75 V
				0x04	0.80 V
				0x05	0.85 V
				0x06	0.90 V
				0x07	0.95 V
				0x08	1.00 V
				0x09	1.05 V
				0x0A	1.10 V
				0x0B	1.15 V
				0x0C	1.20 V
				0x0D	1.25 V
				0x0E	1.30 V
				0x0F	1.35 V
				0x10	1.40 V
				0x11	1.45 V
				0x12	1.50 V

Field Name	Bits	Type	POR	Description	
				0x13	1.55 V
				0x14	1.60 V
				0x15	1.65 V
				0x16	1.70 V
				0x17	1.75 V
				0x18	1.80 V
				0x19	1.85 V
				0x1A	1.90 V
				0x1B	1.90 V
				0x1C	1.90 V
				0x1D	1.90 V
				0x1E	1.90 V
				0x1F	1.90 V

Table 20: Register BUCK_CFG

Address	Register Name	POR Value	Buck config
0x0006	BUCK_CFG	0x00	

7	6	5	4	3	2	1	0
Reserved	Reserved	BUCK_PD_CFG2	BUCK_PD_CFG1	Reserved	Reserved	SEL_BUCK_ILIM<1:0>	

<table>
<tr><th>Field Name</th><th>Bits</th><th>Type</th><th>POR</th><th>Description</th></tr>
<tr><td>BUCK_PD_CFG2</td><td>[5]</td><td>cfg OTP</td><td>0x0</td><td>0: If BUCK_EN = 0, BUCK_PD_EN = 1 1: If BUCK_EN = 0, BUCK_PD_EN = 0</td></tr>
<tr><td>BUCK_PD_CFG1</td><td>[4]</td><td>cfg OTP</td><td>0x0</td><td>0: When BUCK is forced off by faults, BUCK_PD_EN = 1 1: When BUCK is forced off by faults, BUCK_PD_EN = 0</td></tr>
<tr><td>SEL_BUCK_ILIM</td><td>[1:0]</td><td>cfg OTP</td><td>0x0</td><td>Buck peak current limit setting
<table>
<tr><th>Value</th><th>Description</th></tr>
<tr><td>0x0</td><td>Default current limit</td></tr>
<tr><td>0x1</td><td>Default +50mA</td></tr>
<tr><td>0x2</td><td>Default +100mA</td></tr>
<tr><td>0x3</td><td>Default +150mA</td></tr>
</table></td></tr>
</table>

Table 21: Register FAUL_CTL

Address	Register Name	POR Value	Fault & Recovery control
0x0008	FAULT_CTL	0x1F	

7	6	5	4	3	2	1	0
SC_DIS_BUCK	OC_DIS_BUCK	OV_DIS_BUCK	TSD_FRC_DIS	UVLO_FRC_DIS	RCVRY_NUM<2:0>		

Field Name	Bits	Type	POR	Description
SC_DIS_BUCK	[7]	cfg OTP	0x0	1: Force disable BUCK during SHORT CIRCUIT condition oc_buck=1 & uv_buck=1
OC_DIS_BUCK	[6]	cfg OTP	0x0	1: Force disable BUCK during oc_buck=1 for over 64 cycles
OV_DIS_BUCK	[5]	cfg OTP	0x0	1: Force disable BUCK during ov_buck=1
TSD_FRC_DIS	[4]	cfg OTP	0x1	1: Force disable BUCK during Over Temp

Field Name	Bits	Type	POR	Description
UVLO_FRC_DIS	[3]	cfg OTP	0x1	1: Force disable BUCK during UVLO
RCVRY_NUM	[2:0]	data OTP	0x7	BUCK recovery trial fault number. This is counted down by every fault forcing BUCK off. If RCVRY_NUM becomes 0, Recovery trial is ended. If RCVRY_NUM is set 0x7, this is not counted down and recovery trail is not ended.

Table 22: Register PIN_MONITOR

Address	Register Name	POR Value	PIN MONITOR
0x000A	PIN_MONTOR	0x00	

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	GPO_OUT_MON

Field Name	Bits	Type	POR	Description
GPO_OUT_MON	[0]	virtual	0x0	Indicate current GPO output

11.2.2 System Module

11.2.2.1 System Reset Registers

Table 23: Register SYS_RST_EVENT

Address	Register Name	POR Value	Reset Event flag
0x0001	SYS_RST_EVENT	0x01	

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RESET_EVENT

Field Name	Bits	Type	POR	Description
RESET_EVENT	[0]	evnt	0x1	RESET event flag. After Reset, this bit is set. When I2C write '1' to this bit, this event flag is cleared.

Table 24: Register SYS_SRST

Address	Register Name	POR Value	
0x0009	SYS_SRST	0x00	Soft Reset

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	SRST<3:0>			

Field Name	Bits	Type	POR	Description
SRST	[3:0]	cfg	0x0	Initiate Soft Reset by writing 0x5.

11.2.2.2 System ID Registers

Table 25: Register SYS_DEVICE_ID

Address	Register Name	POR Value	
0x0080	SYS_DEVICE_ID	0x00	DEVICE_ID

7	6	5	4	3	2	1	0
DEV_ID<7:0>							

Field Name	Bits	Type	POR	Description
DEV_ID	[7:0]	virtual	0x0	Device ID; hard-coded or metal-programmed

Table 26: Register SYS_VARIANT_ID

Address	Register Name	POR Value	VARIANT_ID
0x0081	SYS_VARIANT_ID	0x00	

7	6	5	4	3	2	1	0
MRC<3:0>				VRC<3:0>			

Field Name	Bits	Type	POR	Description
MRC	[7:4]	virtual	0x0	Mask Revision Code; mask design changes increment reset value.
VRC	[3:0]	trim OTP	0x0	Chip Variant Code; e.g. package variants.

Table 27: Register SYS_CONFIG_ID

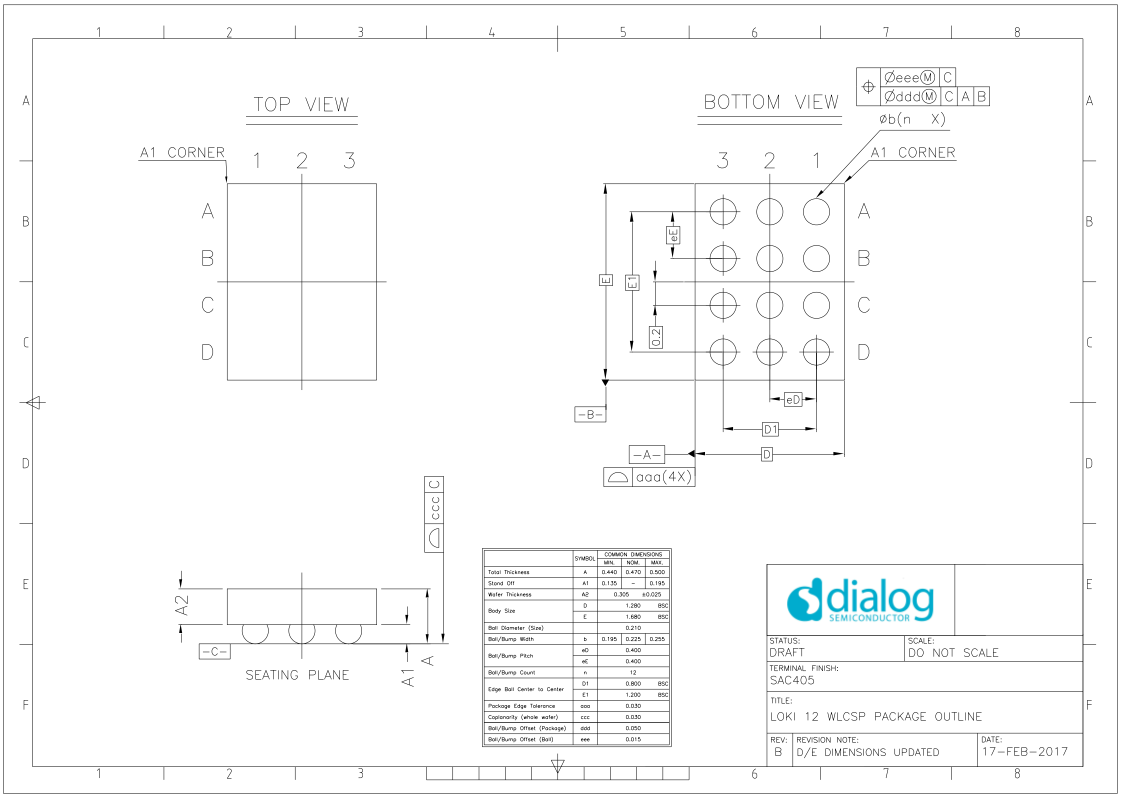
Address	Register Name	POR Value	CONFIG_ID
0x0082	SYS_CONFIG_ID	0x00	

7	6	5	4	3	2	1	0
CONFIG_REV<7:0>							

Field Name	Bits	Type	POR	Description
CONFIG_REV	[7:0]	trim OTP	0x0	OTP settings revision

12 Package Information

12.1 Package Outlines



	SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.
Total Thickness	A	0.440	0.470	0.500
Stand Off	A1	0.135	–	0.195
Wafer Thickness	A2	0.305 ±0.025		
Body Size	D	1.280 BSC		
	E	1.680 BSC		
Ball Diameter (Size)		0.210		
Ball/Bump Width	b	0.195	0.225	0.255
Ball/Bump Pitch	eD	0.400		
	eE	0.400		
Ball/Bump Count	n	12		
Edge Ball Center to Center	D1	0.800 BSC		
	E1	1.200 BSC		
Package Edge Tolerance	aaa	0.030		
Coplanarity (whole wafer)	ccc	0.030		
Ball/Bump Offset (Package)	ddd	0.050		
Ball/Bump Offset (Ball)	eee	0.015		

Figure 38: Package Outline Drawing

12.2 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a maximum temperature of 30 °C and a maximum relative humidity of 60% RH before the solder reflow process. The MSL classification is defined in Table 28.

The device package is qualified for MSL 1.

Table 28: MSL Classification

MSL level	Floor Lifetime
MSL 1	unlimited at 30 °C/85% RH

12.3 Soldering Information

Refer to the JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from http://www.jedec.org.

13 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability or other custom OTP parts, please consult Dialog Semiconductor's customer portal or your local sales representative.

Table 29: Ordering Information

Part number	Package	Size (mm)	Shipment Form	Pack Quantity
DA9232 -xxxx	WLCSP-12	1.3 x 1.7	T&R	4500

Table 30: OTP List

Order code	Description	Buck V_{OUT}
DA9232-81VZ2	OTP with buck voltage preconfigured	1.8 V
DA9232-82VZ2	OTP with buck voltage preconfigured	0.7 V

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via Customer Product Notifications.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

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