Flexible High-Power System PMIC with 1.8 A Switching USB Power Manager

General Description

The DA9053 is a quad buck 1 A per channel PMIC subsystem with supply domain flexibility to support a wide range of application processors, associated peripherals and user interface functions.

Combining a dual input switched-mode USB compatible charger, full power path management, four bucks, ten linear regulators and support for multiple sleep modes: the DA9053 offers an energy-optimized solution suitable for portable handheld, wireless, industrial and infotainment applications.

The high-efficiency Li-Ion/Polymer switching charger supports precise current/voltage charging as well as pre-charge and USB modes without processor interaction. During charging, the die temperature is thermally regulated enabling high-capacity batteries to be rapidly charged at currents up to 1.8 A with minimum thermal impact. USB suspend mode operation is supported and, for robustness, the power inputs are protected against over-voltage conditions.

The autonomous power-path controller seamlessly detects and manages energy flow between an AC adaptor, USB cable, and battery while maintaining USB power specification compliance. The internally-generated system power rail supports power scenarios such as instant-on with a fully discharged battery. A reverse-protected backup battery charger is also integrated into the powerpath function.

Controlled by a programmable digital power manager, the 14 user-programmable switched/linear regulators can be configured to meet the start-up sequence, voltage, and timing requirements for most applications. The power manager includes supply-rail qualification and system reset management. For optimal processor energy-per-task performance, Dynamic Voltage Scaling (DVS) is available on up to five supply domains. Dialog's patented SmartMirror™ dynamic biasing is implemented on all linear regulators.

An integrated 10-channel general purpose ADC includes support for a touch screen controller with pen down detect, programmable high and low thresholds, an integrated current source for resistive measurements, and system voltage monitoring with a programmable low-voltage warning. The ADC has 8-bit resolution in auto-mode and 10-bit resolution in manual conversion mode.

Key Features

- Switched DC/USB charger with power path management
- Four buck converters (three have DVS) 0.5 V to 2.5 V up to 2 A
- Ten programmable LDO's, High PSRR, 1 % accuracy
- Low-power backup charger, 1.1 V to 3.1 V, up to 6 mA
- 32 kHz real time clock (RTC) with alarm wake-up
- Ten channel general purpose ADC with touch screen interface
- High-voltage white LED driver boost, three strings
- Sixteen flexible GPIO pins for enhanced wakeup and peripheral control
- 2-wire and 4-wire control, 2-wire and 4-wire control interfaces
- System watchdog function
- -40 °C to +125 °C junction temperature operation
- 7x7x1 mm 0.5 mm pitch and 11x11x1 mm 0.8 mm pitch VFBGA package options
- AEC Q100 Grade 3 option

Typical Applications

- Mobile internet devices and tablet PCs
- IoT devices
- Personal navigation devices
- Consumer and in-vehicle infotainment devices

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1 Terms and Definitions

ADC	Analog to Digital Converter
BCD	Binary Coded Decimal
CC	Constant Current
CV	Constant Voltage
DCCC	Dynamic Charger Current Control
DVC	Dynamic Voltage Control
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
GND	Ground
GSM	Global System for Mobile Communication
IRQ	Interrupt Request
LDO	Low Dropout Voltage Regulator
LED	Light Emitting Diode
NTC	Negative Temperature Coefficient
OTP	One Time Programmable
OV	Overvoltage
PCB	Printed Circuit Board
PFM	Pulse Frequency Modulation
PMIC	Power Management Integrated Circuit
PSRR	Power Supply Rejection Ratio
PWM	Pulse Width Modulation
RTC	Real Time Clock
TDMA	Time Division Multiple Access
TRC	Trimming Release Code
USB	Universal Serial Bus

2 Block Diagram

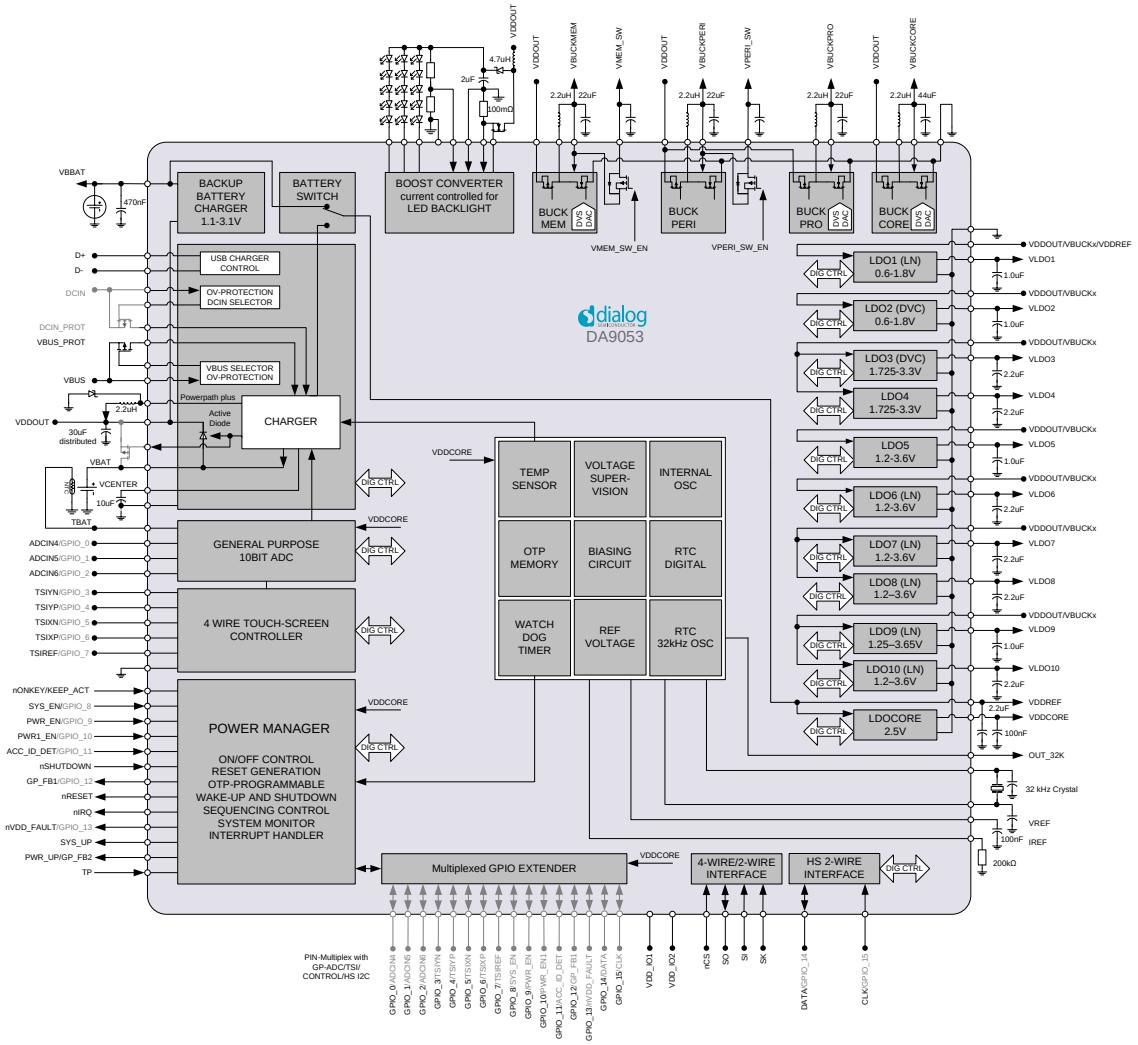

Figure 1: Block Diagram

3 Generated Supply Domains

Table 1: Regulator Overview

Regulator	Supplied Pins	Supplied Voltage (V)	Supplied Max Current (mA)	External Components	Notes
BUCKCORE	VBUCKCORE	0.5 to 2.075 ±3 % accuracy	2000	2.2 µH	DVC, 2 MHz, 25 mV steps,DVC ramp with controlled slew rate; pull-down resistor switch off
BUCKPRO	VBUCKPRO	0.5 to 2.075 ±3 % accuracy	1000	2.2 µH	DVC, 2 MHz, 25 mV steps, DVC ramp with controlled slew rate; pull-down resistor switch off, common supply with BUCKPERI
BUCKMEM	VBUCKMEM; VMEM_SW	0.95 to 2.525 ±3% accuracy	1000	2.2 µH	DVC, 2 MHz, 25 mV steps, DVC ramp with controlled slew rate; 2nd output with sequencer controllable switch, pull-down resistor switch off,
BUCKPERI	VBUCKPERI; VPERI_SW	0.95 to 2.525 ±3 % accuracy	1000	2.2 µH	2 MHz, 25 mV steps 2nd output with sequencer controllable switch, common supply with BUCKPRO
BOOST	Ext. FET	5 to 25, regulated via current feedback	78	4.7 µH	Current controlled boost converter for three strings of up to six serial white LEDs. Over voltage protection via a voltage feedback pin.
LDO1	VLDO1	0.6 to 1.8V ±3 % accuracy	40	1.0 µF	High PSSR, low noise LDO, 50 mV steps, pull-down resistor switch off
LDO2	VLDO2	0.6 to 1.8 ±3 % accuracy	100	1.0 µF	DVC, digital LDO, 25 mV steps, DVC ramp with controlled slew rate, pull-down resistor switch off
LDO3	VLDO3	1.725 to 3.3 ±3 % accuracy	200	2.2 µF	DVC, digital LDO, 25 mV steps, DVC with controlled slew rate, common supply with LDO4
LDO4	VLDO4	1.725 to 3.3 ±3 % accuracy	150	2.2 µF	Digital LDO, 25 mV steps, optional HW control from GPI1, common supply with LDO3

Regulator	Supplied Pins	Supplied Voltage (V)	Supplied Max Current (mA)	External Components	Notes
LDO5	VLDO5	1.2 to 3.6 ±3 % accuracy	100	1.0 µF	Digital LDO, 50 mV steps, pull-down resistor switch off, optional HW control from GPI2,
LDO6	VLDO6	1.2 to 3.6 ±3 % accuracy	150	2.2 µF	High PSRR, low noise, 50 mV steps
LDO7	VLDO7	1.2 to 3.6 ±3 % accuracy	200	2.2 µF	High PSRR, low noise, 50 mV steps, common supply with LDO8
LDO8	VLDO8	1.2 to 3.6V ±3 % accuracy	200	2.2 µF	High PSRR, low noise, 50 mV steps, common supply with LDO7
LDO9	VLDO9	1.25 to 3.6V ±1 % accuracy Note 1	100	1.0 µF	High PSRR, low noise, 50 mV steps, OTP trimmed, optional HW control from GPI12, common supply with LDO10
LDO10	VLDO10	1.2 to 3.6 ±3 % accuracy	250	2.2 µF	High PSRR, low noise, 50 mV steps, common supply with LDO9
BACKUP	VBBAT	1.1 to 3.1	6	470 nF	100 mV or 200 mV steps, configurable current limit between 100 and 6000 µA, reverse current protection
LDOCORE	Internal PMIC supply	2.5 ±2 % accuracy	4	100 nF	Not for external use

Note 1 At default voltage (1 % accuracy requires VLDO9 > 1.5 V).

4 Pad Description

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	NC	VREF	DCIN_PROT	DCIN_PROT	VBUS_PROT	VBUS_PROT	VCENTRE	VSW	VSW	VDDOUT	VDDOUT	VBAT	VBAT
B	XOUT	VBBAT	DCIN_SEL	DCIN	VBUS_SEL	VBUS	NC	NC	NC	GP_FB1_GPIO_12	AD_CONT	VMEM_SW	DMINUS
C	XIN	VDD_REF	NC	ADCIN6_GPIO_2	ADCIN5_GPIO_1	ADCIN4_GPIO_0	NC	NC	NC	PWR_EN_GPIO_9	nVDD_FAULT_GPIO_13	VBUCKMEM	DPLUS
D	VLDO1	VDDCORE	NC	NC	IREF	VSS_NOISY	VSS_NOISY	NC	NC	SYS_EN_GPIO_8	nSHUTDOWN	VPERI_SW	VDDBUCK_CORE
E	VDD_LDO2	VDD_LDO1	NC	NC	VSS_NOISY	VSS_NOISY	VSS_NOISY	VSS_NOISY	VSS_NOISY	nIRQ	NC	VBUCKPERI	VDDBUCK_CORE
F	VLDO5	VLDO2	NC	NC	VSS_NOISY	VSS_NOISY	VSS_NOISY	VSS_NOISY	VSS_NOISY	nRESET	NC	VBUCKCORE	SWBUCKCORE
G	VLDO6	VDD_LDO5	NC	NC	**VSS_QUIET**	**VSS_QUIET**	VSS_NOISY	VSS_NOISY	VSS_NOISY	NC	NC	NC	SWBUCKCORE
H	VLDO4	VDD_LDO6	NC	NC	**VSS_QUIET**	**VSS_QUIET**	VSS_NOISY	VSS_NOISY	VSS_NOISY	NC	NC	NC	SWBUCKPRO
J	VLDO3	VDD_LDO3_4	NC	NC	**VSS_QUIET**	**VSS_QUIET**	VSS_NOISY	VSS_NOISY	VSS_NOISY	PWR_UP_GP_FB2	NC	NC	VDDBUCK_PERI_PRO
K	VLDO7	VDD_LDO7_8	NC	VDD_IO2	TSIXN_GPIO_5	TSIYN_GPIO_3	TSIXP_GPIO_6	TSIYP_GPIO_4	TSIREF_GPIO_7	SI	NCS	OUT32K	VDDBUCK_PERI_PRO
L	VLDO8	PWR1_EN_GPIO_10	ACC_ID_DET_GPIO_11	VDD_IO1	TP	TBAT	LED3_IN	LED2_IN	NC	SO	SK	SYS_UP	SWBUCKPERI
M	VLDO9	CLK_GPIO_15	VDD_LDO9_10	NC	NC	NC	NC	NC	LED1_IN	SW_BOOST	nONKEY_KEEP_ACT	VBUCKPRO	SWBUCKMEM
N	DATA_GPIO_14	VLDO10	NC	NC	NC	NC	NC	NC	BOOST_SENSE_N	BOOST_SENSE_P	BOOST_PROT	NC	VDDBUCK_MEM

Figure 2: DA9053 Ballout (View From Top, Balls Through Package)

Table 2: Ballout Description

Pad	Pad Name	Type	Description
Power manager			
M11	nONKEY	DI	On/Off key with optional long press shutdown/hardware input for watchdog supervision
D10	SYS_EN	DI/DIO	Hardware enable of power domain SYSTEM/GPIO_8
C10	PWR_EN	DI/DIO	Hardware enable of power domain POWER/GPIO_9
L2	PWR1_EN	DI/DIO	Hardware enable of power domain POWER1/GPIO_10 with high-power output and blinking feature, input for power sequencer WAIT ID
L3	ACC_ID_DET	DI/DIO	ACC_ID_DET accessory detection circuitry/GPIO_11 with high-power output and blinking feature
D11	nSHUTDOWN	DI	Active low input from switch or error indication line from host to initiate shutdown
F10	nRESET	DO	Active low RESET towards host
B10	GP_FB1	DO/DIO	Status indication towards host for a valid Wakeup event (EXT_WAKEUP) or indicator for ongoing power mode transition (READY) /GPIO_12, enables HW control of LDO9
E10	nIRQ	DO	Active low IRQ line towards host
C11	nVDD_FAULT	DO/DIO	Active low indication for low supply voltage/GPIO_13
L12	SYS_UP	DO	Sequencer status indicator: All SYSTEM IDs powered up
J10	PWR_UP	DO/DO	Sequencer status indicator: All POWER IDs powered up (PWR_UP) or programmable level controlled from the power sequencer (GP_FB2)
L4	VDD_IO1	PS	First supply I/O voltage rail
K4	VDD_IO2	PS	Alternate supply I/O voltage rail
L5	TP	DIO	Test pin, enables power commander boot mode
4-Wire/2-Wire Interfaces			
L10	SO	DIO	4-wire data output, 2-wire data
K10	SI	DI	4-wire data input
L11	SK	DI	4-wire, 2-wire clock
K11	nCS	DI	4-wire chip select
N1	DATA	DIO	HS-2-wire data [GPIO_14] (enables reset if long press in parallel with GPI15) with high-power output and PWM LED control
M2	CLK	DI	HS-2-wire clock [GPIO_15] (enables reset if long press in parallel with GPI14)) with high-power output and PWM LED control

Pad	Pad Name	Type	Description
Voltage Regulators			
D1	VLDO1	AO	Output voltage from LDO1
E2	VDD_LDO1	PS	Supply voltage for LDO1
F2	VLDO2	AO	Output voltage from LDO2
E1	VDD_LDO2	PS	Supply voltage for LDO2
J1	VLDO3	AO	Output voltage from LDO3
H1	VLDO4	AO	Output voltage from LDO4
J2	VDD_LDO3_4	PS	Supply voltage for LDO3 and LDO4
F1	VLDO5	AO	Output voltage from LDO5
G2	VDD_LDO5	PS	Supply voltage for LDO5
G1	VLDO6	AO	Output voltage from LDO6
H2	VDD_LDO6	PS	Supply voltage for LDO6
K1	VLDO7	AO	Output voltage from LDO7
L1	VLDO8	AO	Output voltage from LDO8
K2	VDD_LDO7_8	PS	Supply voltage for LDO7 and LDO8
M1	VLDO9	AO	Output voltage from LDO9
N2	VLDO10	AO	Output voltage from LDO10
M3	VDD_LDO9_10	PS	Supply voltage for LDO9 and LDO10
D2	VDDCORE	AO	Supply for internal circuitry
C2	VDD_REF	AO	Switched supply from VBAT, VBUS or VBACKUP
DC/DC Buck Converters			
F12	VBUCKCORE	AI	Sense node for DVC DC/DC BUCKCORE
F-G13	SWBUCKCORE	AO	Switching node for BUCKCORE
M12	VBUCKPRO	AI	Sense node for DVC DC/DC BUCKPRO
H13	SWBUCKPRO	AO	Switching node for BUCKPRO
C12	VBUCKMEM	AI	Sense node for DVC DC/DC BUCKMEM and input for power switch (sequencer controlled)
B12	VMEM_SW	PS	Power switch output from BUCKMEM
M13	SWBUCKMEM	AO	Switching node for BUCKMEM
E12	VBUCKPERI	AI	Sense node for DC/DC BUCKPERI and input for power switch (sequencer controlled)
D12	VPERI_SW	PS	Power switch output from BUCKPERI
L13	SWBUCKPERI	AO	Switching node for BUCKPERI
D-E13	VDDBUCK_CORE	PS	Supply voltage for BUCKCORE
J-K13	VDDBUCK_PER_PRO	PS	Supply voltage for BUCKPERI and BUCKPRO To be connected to VDDOUT
N13	VDDBUCK_MEM	PS	Supply voltage for BUCKMEM To be connected to VDDOUT

Pad	Pad Name	Type	Description
Reference Voltage Generation			
A2	VREF	AIO	Reference voltage output, decouple with 100 nF
D5	IREF	AO	Connection for bias setting, configure with high precision 200 kΩ resistor
Internal Oscillator			
C1	XIN	AIO	32 kHz crystal connection Adjust with 10 pF
B1	XOUT	AIO	32 kHz crystal connection Adjust with 10 pF
K12	OUT_32K	DO	32 kHz oscillator buffer output
Charger			
B5	VBUS_SEL	AO	Control for external over voltage protection and input selection of VBUS To be connected to gate of PFET
A5-6	VBUS_PROT	PS	Overvoltage protected VBUS charger input
B6	VBUS	PS	USB or wall charger input
B3	DCIN_SEL	AO	Control for external over voltage protection and input selection of DCIN To be connected to gate of PFET
A3-4	DCIN_PROT	PS	Overvoltage protected DCIN charger input
B4	DCIN	PS	Wall charger input
A7	VCENTER	PS	Protected input for switching charger (decouple with 10 µF)
A8-9	VSW	PS	Switching node for charger buck
A10-11	VDDOUT	PS	System power supply output
B11	AD_CONT	AO	Active diode controller output To be connected to gate of PFET (leave unconnected, if not used)
A12-13	VBAT	PS	Connection to main battery
Boost Converter and LED Current Sinks			
M10	SW_BOOST	AO	Boost switching output To be connected to gate of NFET
N10	BOOST_SENSE_P	AI	High side sense connected to Boost Isat current protection resistor, stabilize with capacitor
N9	BOOST_SENSE_N	AI	Low side sense connected to Boost Isat current protection resistor
N11	BOOST_PROT	AI	Over voltage protection input Requires external resistor voltage divider
M9	LED1_IN	AI	Connection to LED string 1 Provides current controlled sink via logarithmic IDAC
L8	LED2_IN	AI	Connection to LED string 2 Provides current controlled sink via logarithmic IDAC
L7	LED3_IN	AI	Connection to LED string 3 Provides current controlled sink via logarithmic IDAC with PWM only LED control
USB Charger Control			
C13	D+	AIO	USB D+
B13	D-	AIO	USB D-

Pad	Pad Name	Type	Description
General Purpose ADC and Touch Screen Interface			
L6	TBAT	AIO	Connection to battery NTC resistor
C6	ADCIN4	AI/DIO	Connection to GP ADC auto channel 4 with threshold IRQ and resistor measurement option/GPIO_0
C5	ADCIN5	AI/DIO	Connection to GP ADC channel 5 with 1.2 V HW comparator IRQ/GPIO_1, enables HW control of LDO4
C4	ADCIN6	AI/DIO	Connection to GP ADC channel 6/GPIO_2 enables HW control of LDO5
K6	TSIYN	AIO/DIO	TSI interface connection to YN terminal of touch screen
K8	TSIYP	AIO/DIO	TSI interface connection to YP terminal of touch screen
K5	TSIXN	AIO/DIO	TSI interface connection to XN terminal of touch screen
K7	TSIXP	AIO/DIO	TSI interface connection to XP terminal of touch screen
K9	TSREF	PS	TSI interface reference voltage
Backup Battery Charger			
B2	VBBAT	AIO	Backup battery connection coin-cell or super-cap
VSS			
D6-D7, E5-F9, G7-J9	VSS_NOISY	VSS	VSS connection for noisy circuits (bucks) To be connected to main ground plane of PCB for optimum electrical and thermal performance
G5-J6	VSS_QUIET	VSS	VSS connection for quiet circuits (LDOs) To be connected to main ground plane of PCB for optimum electrical and thermal performance
A1, B7-C9, D8-D9, C3-K3, D4-J4, G10-H10, E11-J11, G12-J12, L9, M4-M8, N3-N8, N12	NC		Non-connected balls Floating in package, can be freely connected on PCB, recommended to be connected to ground plane for optimum noise and thermal performance

Table 3: Pin Type Definition

Pin Type	Description	Pin Type	Description
DI	Digital Input	AI	Analog Input
DO	Digital Output	AO	Analog Output
DIO	Digital Input/Output	AIO	Analog Input/Output
DIOD	Digital Input/Output Open Drain	BP	Backdrive Protection
PS	Power Supply	VSS	Power Supply

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

The maximum continuous charger voltage must be less than 5.5 V, the over-voltage protection (OVP) circuit will help protect against transients above this level minimizing effects on operation lifetime.

VDDOUT must not be driven from an external supply if the charger buck is used.

Table 4: Absolute Maximum Ratings

Parameter	Symbol	Conditions Note 1	Min	Max	Unit
Storage temperature			-40	+95	°C
Junction temperature	T_J		-40	+140 Note 2	°C
Supply voltage	V_{BAT}, V_{BUS_PROT}, D_{CIN_PROT}, V_{DDOUT}, V_{DD_REF}		-0.3	5.5	V
Supply voltage charger	V_{BUS}, D_{CIN}		-0.3	12	V
Supply voltage LDO and buck input pins (except listed below)			-0.3	V_{DDOUT} + 0.3 V, 5 V max	V
Supply voltage all pins (except listed above)			-0.3	V_{DDOUT} + 0.3 V, 5 V max	V
ESD susceptibility		Human body model		2	kV

Note 1 Stresses beyond those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2 See Section 5.11 for more details.

5.2 Recommended Operating Conditions

All voltages are referenced to V_{SS} unless otherwise stated. Currents flowing into DA9053 are deemed positive, currents flowing out are deemed negative. All parameters are valid over the recommended temperature range and power supply range unless otherwise noted.

NOTE
The power dissipation must be limited to avoid overheating of DA9053. The maximum power dissipation should not be reached with maximum ambient temperature.

Table 5: Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Max	Unit
Supply voltage	V_{BAT}		0	4.4	V
Supply voltage charger	V_{BUS}, D_{CIN}		0	5.5	V
Supply voltage IO	V_{DD_IO1}, V_{DD_IO2}		1.2	3.6 Note 1	V
Operating Junction Temperature	T_J		-40	+125	°C
Maximum power dissipation		7x7 package. Derating factor above Ta = 70 °C: 21 mW/ °C		1.14	W
Package thermal resistance Note 2		7x7 package.		48	°C/W
Maximum power dissipation		11 x 11 package Derating factor above Ta = 70 °C: 40 mW/ °C		2.2	W
Package thermal resistance Note 2		11x11 package		25	°C/W

Note 1 V_{DD_IO} must not exceed V_{DDOUT}.

Note 2 JEDEC 4 layer board, still air, influenced by PCB technology and layout. The numbers of supplies, that can be used at the same time at maximum dissipation power is limited by the thermal resistance of the package and the PCB layout.

5.3 Current Consumption

Table 6: Current Consumption

Operating mode	Conditions (Ta = 25 °C)	Min	Typ	Max	Unit
NO-POWER mode	Detection circuits running, oscillator off		15		µA
RESET mode	V_{DD_REF} > 2.2 V, bucks and LDOs off (except LDOCORE), RTC unit on		45 (Note 1)		µA
POWER-DOWN mode (Standby)	V_{DD_REF} > 2.8 V, supplies off (except LDOCORE), all blocks in powerdown mode, RTC unit on		45		µA
POWER-DOWN mode (Hibernate)	BUCKCORE, LDOCORE, LDO2, 4, 5 enabled, RTC and GPIO unit on		190 (Note 2)		µA
ACTIVE mode	All supplies, GPIO, RTC and GP-ADC on		460		µA

Note 1 V_{DD_REF} > 2.5 V if not supplied from backup battery.

Note 2 Enabled bucks are set to forced sleep mode, setting '00'.

5.4 Digital I/O Characteristics

Unless otherwise noted, the following is valid for T_J = -40 °C to +125 ºC, V_{DD_REF} = 2.8 V to 5.5 V.

Table 7: Digital I/O Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
GPI0 – GPI15, nONKEY, nSHUTDOWN SYS_EN, PWR_EN, PWR1_EN, CLK, DATA input high voltage	V_{IH}	VDDCORE mode VDD_IO2 mode	1.0 0.7*VDD_IO2		V_{DDOUT}	V
GPI0 – GPI15, nONKEY, nSHUTDOWN SYS_EN, PWR_EN, PWR1_EN' CLK, DATA input low voltage	V_{IL}	VDDCORE mode VDD_IO2 mode			0.4 0.3*V_{DD_IO2}	V
SK, nCS, SI input high voltage	V_{IH}	VDD_IO1 mode VDD_IO2 mode	0.7*V_{DD_IO1} 0.7*V_{DD_IO2}		V_{DDOUT}	V
SK, nCS, SI input low voltage	V_{IL}	VDD_IO1 mode VDD_IO2 mode			0.3*V_{DD_IO1} 0.3*V_{DD_IO2}	V
GPO0 – GPO15, nVDD_FAULT, SO nRESET, nIRQ SYS_UP, PWR_UP, GP_FB2, OUT_32K output high voltage	V_{OH} @ 1 mA	VDD_IO1 mode VDD_IO2 mode	0.8*V_{DD_IO1} 0.8*V_{DD_IO2}		V_{DDOUT}	V
GPO0 – GPO15, DATA, SO nRESET, nIRQ output high voltage	V_{OH}		0	OPEN DRAIN	V_{DDOUT}	V
GPO0 – GPO15, DATA, SO, nVDD_FAULT, nRESET (Note 1), nIRQ, SYS_UP, PWR_UP, GP_FB2, OUT_32K output low voltage	V_{OL} @ 1 mA				0.3	V

Note 1 For V_{SUPPLY} < 1.5 V the source current for min 0.8 * VDD is limited to 0.5 mA. It is good practice to allow a 10 % voltage margin when running at maximum temperatures to allow for worse case process variation.

5.5 GPIO Characteristics

Unless otherwise noted, the following is valid for T_J = -40 °C to +125 ºC, V_{DD_REF} = 2.8 V to 5.5 V.

Table 8: GPIO Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Sink current capability GPO 14, 15		VGPIO = 0.1 V		30 Note 1		mA
Sink current capability GPO 10,11		VGPIO = 0.5 V		15		mA
Source current capability GPO 10,11,14,15		VGPIO = $V_{DD\_IO1/2}$ - 0.5 V		-4 Note 2		mA
Sink current capability GPO 0…9, 12…13		VGPIO = 0.3 V		1		mA
Source current capability GPO 0…9, 12…13		VGPIO = $V_{DD\_IO1/2}$ - 0.5 V		-1 Note 2		mA
GPO pull-up resistor Note 3		$V_{DD\_IO1/2}$ = 1.5 V = 1.8 V = 3.3 V	100 70 25	180 120 40	300 170 60	kΩ
D+/D- input impedance			10		2	MΩ pF

Note 1 At low V_{DD_REF} values and high temperatures, the sink current capability will be reduced.

Note 2 For $V_{DD\_IO1/2}$ < 1.5 V the source current for min 0.8 * V_{DD} is limited to 0.8 mA.

Note 3 V(PAD) = 0 V.

5.6 Power on Reset

Table 9: Power on Reset Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Deep discharge lockout lower threshold	V_{POR_LOWER}		2.0		V
Deep discharge lockout upper threshold	V_{POR_UPPER}		2.5		V
Under voltage lower threshold	$V_{DD\_FAULT\_LOWER}$	2.8	2.8	3.15	V
Under voltage lower threshold accuracy	$V_{DD\_FAULT\_LOWER}$ accuracy		+/-2		%
Under voltage upper threshold	$V_{DD\_FAULT\_UPPER}$		$V_{DD\_FAULT\_LOWER}$ + 0.15		V
Charger buck under voltage	V_{DDOUT_MIN}	3.35	3.40	3.45	V

5.7 Watchdog

Table 10: Watchdog

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Minimum watchdog time	T_{WDMIN}		0.18	0.256	0.33	s
Maximum watchdog time	T_{WDMAX}		1.44	2.048	2.64	s

5.8 Power Manager and HS-2-Wire Control Bus

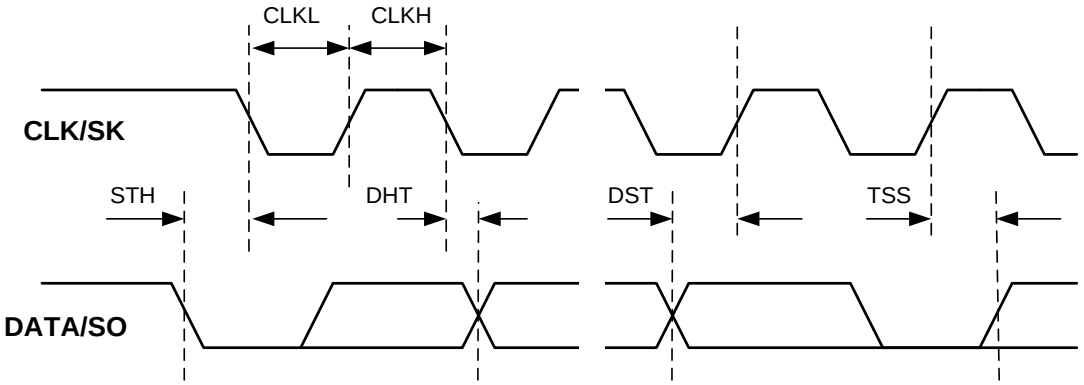

Figure 3: 2-Wire Control Bus Timing Diagram

Table 11: HS-2-Wire Timing

Parameter	Symbol	Min	Typ	Max	Unit
Bus free time STOP to START		1.3			µs
Bus line capacitive load				100	pF
Standard / Fast Mode					
CLK clock frequency		1		400	kHz
Bus free time STOP to START		1.3			µs
Start condition set-up time		0.6			µs
Start condition hold time	STH	0.6			µs
CLK low time	CLKL	1.3			µs
CLK high time	CLKH	0.6			µs
2-wire CLK and DATA rise/fall time				300	ns
Data set-up time	DST	100			ns
Data hold-time	DHT	0			ns
Stop condition set-up time	TSS	0.6			µs

Parameter	Symbol	Min	Typ	Max	Unit
High Speed Mode					
CLK clock frequency		1		1700	kHz
Start condition set-up time		160			ns
Start condition hold time	STH	160			ns
CLK low time	CLKL	160			ns
CLK high time	CLKH	60			ns
HS-2-wire CLK rise/fall time				40	ns
HS-2-wire DATA rise/fall time				80	ns
Data set-up time	DST	10			ns
Data hold-time	DHT	10			ns
Stop condition set-up time	TSS	16			ns

5.9 4-Wire Control Bus Timing

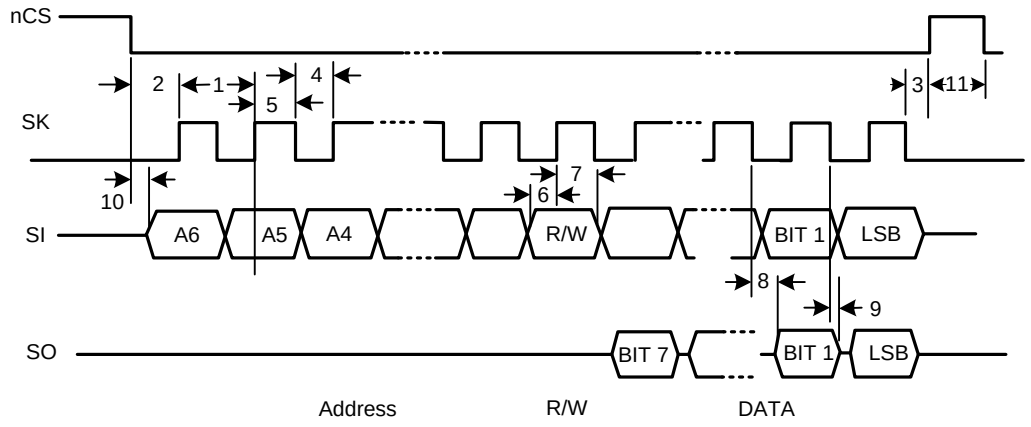

Figure 4: 4-Wire Control Bus Timing Diagram

NOTE
The above timing is valid for active low and high CS.

Table 12: 4-Wire Timing

Parameter	Symbol	Label in Figure 4	Min	Typ	Max	Unit
Cycle time	t_C	1	70			ns
Enable lead time	t_{CSS}	2, from CS active to first SK edge	20			ns
Enable lag time	t_{SCS}	3, from last SK edge to CS idle	20			ns
Clock low time	t_{CL}	4	0.4 * t_C			ns
Clock high time	t_{CH}	5	0.4 * t_C			ns

Parameter	Symbol	Label in Figure 4	Min	Typ	Max	Unit
Data in setup time	t_{SIS}	6	5			ns
Data in hold time	t_{SIH}	7	5			ns
Data out valid time	t_{SOV}	8			22	ns
Data out hold time	t_{SOH}	9	6			ns
Data access time	t_{H}	10			22	ns
CS inactive Time	t_{WCS}	11	20			ns

5.10 Oscillator

Table 13: Oscillator Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Internal oscillator frequency		Before trimming After trimming	1.4 1.9	2.0 2.0	2.6 2.1	MHz

5.11 Reference Voltage Generation and Temperature Supervision

Table 14: Reference Voltage Generation and Temperature Supervision

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reference voltage	VREF pin		-1.25 %	1.2	+1 %	V
VREF decoupling capacitor				100		nF
Reference current resistor	IREF pin		-1 %	200	+1 %	kΩ
Thermal shutdown	T_{OVER}		125	140	155	ºC
Charge current reduction	$T_{CHARGELOW}$		75	90	115	ºC
Charge suspend	$T_{CHARGESUSPEND}$		105	120	135	ºC
Hysteresis				10		ºC

5.12 LDO Voltage Regulators

5.12.1 LDO1

Table 15: LDO1 Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage	V_{DD}	(If supplied from buck)	2.0 (1.5)		V_{DDOUT} + 0.3 V, 5 V max	V
Output voltage	V_{LDO1}	$I_{OUT} = I_{MAX}$	0.6	Note 1	1.8	V
Output accuracy		$I_{OUT} = I_{MAX}$	-3	Note 2	+3	%
Stabilization	C_{OUT}	(including voltage and temperature coefficient @	-55 %	1.0	+35 %	µF

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
capacitor		configured VLDO1)				
ESR of capacitor		F > 1 MHz			0.1	Ω
Maximum output current	I_{MAX}	V_{DD} ≥ 1.8 V	40	Note 3		mA
Short circuit current	I_{SHORT}			80		mA
Dropout voltage	$V_{DROPOUT}$	V_{DD} > 2.15 V I_{OUT}= I_{MAX} (V_{DD} = 2.0 V I_{OUT} = 0.4 * I_{MAX} or V_{DD} = 1.5 V I_{OUT} = 0.25 * I_{MAX})		200 100	350 150	mV
Static line regulation	VS_{LINE}	V_{DD} = 3.0 V to 5.0 V I_{OUT} = I_{MAX}		5	20	mV
Static load regulation	VS_{LOAD}	I_{OUT} = 1 mA to I_{MAX}		5	20	mV
Line transient response	VTR_{LINE}	V_{DD} = 3.0 V to 3.6 V I_{OUT} = I_{MAX} t_r = t_f = 10 µs		5	20	mV
Load transient response	VTR_{LOAD}	V_{DD} = 3.6 V I_{OUT} = 1 mA to I_{MAX} t_r = t_f = 1 µs		15	50	mV
PSRR	PSRR	f = 10 Hz to 10 kHz V_{DD} = 3.6 V	50	60		dB
Output noise	N	f = 10 Hz to 100 kHz V_{DD} = 3.6 V I_{OUT} = 5 mA to I_{MAX}		80		µVrms
Quiescent current in ON mode	IQ_{ON}	Note 4		8 µA + 1.25 % of I_{OUT}		µA
Quiescent current in OFF mode	IQ_{OFF}				1	µA
Turn on time	T_{ON}	10 % to 90 %			300	µs
Turn off time	T_{OFF}	90 % to 10 %			10	ms
Pull down resistance in OFF mode	R_{OFF}	Can be switched off via LDO1_PD_DIS		100		Ω

Note 1 Programmable in 50 mV voltage steps, maximum output voltage is determined by V_{DD} - dropout voltage.

Note 2 Sourced from LDOCORE band gap.

Note 3 Max. current is 10 mA if supplied from V_{DD_REF}.

Note 4 Internal regulator current flowing to ground.

5.12.2 LDO2

Table 16: LDO2 Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage	V_{DD}	(if supplied from buck)	2.8 (1.5)		V_{DDOUT} + 0.3 V, 5 V Max	V
Output voltage	V_{LDO2}	$I_{OUT} = I_{MAX}$	0.6	Note 1	1.8	V
Output accuracy		$I_{OUT} = I_{MAX}$	-3		+3	%
Stabilization capacitor	C_{OUT}	(including voltage and temperature coefficient @ configured V_{LDO2})	-55%	1.0	+35 %	µF
ESR of capacitor		f > 1 MHz			0.1	Ω
Maximum output current	I_{MAX}	V_{DD} ≥ 1.8 V	100			mA
Short circuit current	I_{SHORT}			200		mA
Dropout voltage	$V_{DROPOUT}$	$I_{OUT} = I_{MAX}$ (for V_{DD} = 1.5 V $I_{OUT} = I_{MAX}/3$)		100	200	mV
Static line regulation	VS_{LINE}	V_{DD} = 3.0 V to 5.0 V $I_{OUT} = I_{MAX}$		5	20	mV
Static load regulation	VS_{LOAD}	I_{OUT} = 1 mA to I_{MAX}		5	20	mV
Line transient response	VTR_{LINE}	V_{DD} = 3.0 V to 3.6 V $I_{OUT} = I_{MAX}$ $t_r = t_f$ = 10 µs		5	20	mV
Load transient response	VTR_{LOAD}	V_{DD} = 3.6 V I_{OUT} =1 mA to I_{MAX} $t_r = t_f$ = 1 µs		15	50	mV
PSRR	PSRR	f = 10 Hz to 10 kHz V_{DD} = 3.6 V	40	60		dB
Quiescent current in ON mode	IQ_{ON}	Note 2		8 µA +0.6 % of I_{OUT}		µA
Quiescent current in OFF mode	IQ_{OFF}				1	µA
Turn on time	T_{ON}	10 % to 90 %			500	µs
Turn off time	T_{OFF}	90 % to 10 %			10	ms
Pull down resistance in OFF mode	R_{OFF}	Can be switched off via LDO2_PD_DIS		100		Ω

Note 1 Programmable in 25 mV voltage steps, maximum output voltage is determined by V_{DD} - dropout voltage.

Note 2 Internal regulator current flowing to ground.

5.12.3 LDO3

Table 17: LDO3 Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage	V_{DD}	(if supplied from buck)	2.8 (1.9)		V_{DDOUT} + 0.3 V, 5 V max	V
Output voltage	V_{LDO3}	$I_{OUT} = I_{MAX}$	1.725	Note 1	3.3	V
Output accuracy		$I_{OUT} = I_{MAX}$	-3		+3	%
Stabilization capacitor	C_{OUT}	(including voltage and temperature coefficient @ configured V_{LDO3})	-55 %	2.2	+35 %	µF
ESR of capacitor		f > 1 MHz			0.1	Ω
Maximum output current	I_{MAX}		200			mA
Short circuit current	I_{SHORT}			400		mA
Dropout voltage	$V_{DROPOUT}$	$I_{OUT} = I_{MAX}$ (for V_{DD} = 1.9 V $I_{OUT} = I_{MAX}$ *2/3)		100	150	mV
Static line regulation	VS_{LINE}	V_{DD} = 3.0 V to 5.0 V $I_{OUT} = I_{MAX}$		5	20	mV
Static load regulation	VS_{LOAD}	I_{OUT} = 1 mA to I_{MAX}		5	20	mV
Line transient response	VTR_{LINE}	V_{DD} = 3.0 V to 3.6 V $I_{OUT} = I_{MAX}$ $t_r = t_f$ = 10 µs		5	20	mV
Load transient response	VTR_{LOAD}	V_{DD} = 3.6 V I_{OUT} = 1 mA to I_{MAX} $t_r = t_f$ = 1 µs		20	50	mV
PSRR	PSRR	f = 10 Hz to 10 kHz V_{DD} = 3.6 V	40	60		dB
Quiescent current in ON mode	IQ_{ON}	Note 2		8 µA +0.3 % of I_{OUT}		µA
Quiescent current in OFF mode	IQ_{OFF}				1	µA
Turn on time	T_{ON}	10 % to 90 %			300	µs
Turn off time	T_{OFF}	90 % to 10 %			10	ms
Pull down resistance in OFF mode	R_{OFF}			100		Ω

Note 1 Programmable in 25 mV voltage steps, maximum output voltage is determined by V_{DD} - dropout voltage.

Note 2 Internal regulator current flowing to ground.

5.12.4 LDO4

Table 18: LDO4 Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage	V_{DD}	(if supplied from buck)	2.8 (1.9)		V_{DDOUT} + 0.3 V, 5 V max	V
Output voltage	V_{LDO4}	$I_{OUT} = I_{MAX}$	1.725	Note 1	3.3	V
Output accuracy		$I_{OUT} = I_{MAX}$	-3		+3	%
Stabilization capacitor	C_{OUT}	(including voltage and temperature coefficient @ configured VLDO4)	-55 %	2.2	+35 %	µF
ESR of capacitor		f > 1 MHz			0.1	Ω
Maximum output current	I_{MAX}		150			mA
Short circuit current	I_{SHORT}			300		mA
Dropout voltage	$V_{DROPOUT}$	$I_{OUT} = I_{MAX}$ (for V_{DD} = 1.9 V $I_{OUT} = I_{MAX}$* 2/3)		100	150	mV
Static line regulation	VS_{LINE}	V_{DD} = 3.0 V to 5.0 V $I_{OUT} = I_{MAX}$		5	20	mV
Static load regulation	VS_{LOAD}	I_{OUT} = 1 mA to I_{MAX}		5	20	mV
Line transient response	VTR_{LINE}	V_{DD} = 3.0 V to 3.6 V $I_{OUT} = I_{MAX}$ $t_r = t_f$ = 10 µs		5	20	mV
Load transient response	VTR_{LOAD}	V_{DD} = 3.6 V I_{OUT} = 1 mA to I_{MAX} $t_r = t_f$ = 1 µs		15	50	mV
PSRR	PSRR	f = 10 Hz to 10 kHz V_{DD} = 3.6 V	40	60		dB
Quiescent current in ON mode	IQ_{ON}	Note 2		8 µA +0.5 % of I_{OUT}		µA
Quiescent current in OFF mode	IQ_{OFF}				1	µA
Turn on time	T_{ON}	10 % to 90 %			300	µs
Turn off time	T_{OFF}	90 % to 10 %			10	ms
Pull down resistance in OFF mode	R_{OFF}			100		Ω

Note 1 Programmable in 25 mV voltage steps, maximum output voltage is determined by V_{DD} - dropout voltage.

Note 2 Internal regulator current flowing to ground.

5.12.5 LDO5

Table 19: LDO5 Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input voltage	V_{DD}	(if supplied from buck)	2.8 (1.5)		V_{DDOUT} + 0.3 V, 5 V max	V
Output voltage	V_{LDO5}	$I_{OUT} = I_{MAX}$	1.2	Note 1	3.6	V
Output accuracy		$I_{OUT} = I_{MAX}$	-3		+3	%
Stabilization capacitor	C_{OUT}	(including voltage and temperature coefficient @ configured V_{LDO5})	-55 %	1.0	+35 %	µF
ESR of capacitor		f > 1 MHz			0.1	Ω
Maximum output current	I_{MAX}	V_{DD} ≥ 1.8 V	100			mA
Short circuit current	I_{SHORT}			200		mA
Dropout voltage	$V_{DROPOUT}$	I_{OUT}= I_{MAX} (for V_{DD} = 1.5 V $I_{OUT} = I_{MAX}/3$)		100	200	mV
Static line regulation	VS_{LINE}	V_{DD} = 3.0 V to 5.0 V $I_{OUT} = I_{MAX}$		5	20	mV
Static load regulation	VS_{LOAD}	I_{OUT} = 1 mA to I_{MAX}		5	20	mV
Line transient response	VTR_{LINE}	V_{DD} = 3.0 V to 3.6 V $I_{OUT} = I_{MAX}$ $t_r = t_f$ = 10 µs		5	20	mV
Load transient response	VTR_{LOAD}	V_{DD} = 3.6 V I_{OUT} = 1 mA to I_{MAX} $t_r = t_f$ = 1 µs		15	50	mV
PSRR	PSRR	f =10 Hz to 10 kHz V_{DD}=3.6 V, $I_{OUT} = I_{MAX}/2$	40	60		dB
Quiescent current in ON mode	IQ_{ON}	Note 2		8 µA +0.7 % of I_{OUT}		µA
Quiescent current in OFF mode	IQ_{OFF}				1	µA
Turn on time	T_{ON}	10 % to 90 %			200	µs
Turn off time	T_{OFF}	90 % to 10 %			10	ms
Pull down resistance in OFF mode	R_{OFF}	Can be switched off via LDO5_PD_DIS		100		Ω

Note 1 Programmable in 50 mV voltage steps, maximum output voltage is determined by V_{DD} - dropout voltage.

Note 2 Internal regulator current flowing to ground.

5.12.6 LDO6

Table 20: LDO6 Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input voltage	V_{DD}	(if supplied from buck)	2.8 (1.5)		V_{DDOUT} + 0.3 V, 5 V max	V
Output voltage	V_{LDO6}	$I_{OUT} = I_{MAX}$	1.2	Note 1	3.6	V
Output accuracy		$I_{OUT} = I_{MAX}$	-3		+3	%
Stabilization capacitor	C_{OUT}	(including voltage and temperature coefficient @ configured V_{LDO6})	-55 %	2.2	+35 %	µF
ESR of capacitor		f > 1 MHz			0.1	Ω
Maximum output current	I_{MAX}	V_{DD} ≥ 1.8 V		150		mA
Short circuit current	I_{SHORT}			300		mA
Dropout voltage	$V_{DROPOUT}$	$I_{OUT} = I_{MAX}$ (for VDD = 1.5 V $I_{OUT} = I_{MAX}/3$		100	150	mV
Static line regulation	VS_{LINE}	V_{DD} = 3.0 V to 5.0 V $I_{OUT} = I_{MAX}$		5	20	mV
Static load regulation	VS_{LOAD}	I_{OUT} = 1 mA to I_{MAX}		5	20	mV
Line transient response	VTR_{LINE}	V_{DD} = 3.0 V to 3.6 V $I_{OUT} = I_{MAX}$ $t_r = t_f$ = 10 µs		5	20	mV
Load transient response	VTR_{LOAD}	V_{DD} = 3.6 V I_{OUT} =1 mA to I_{MAX} $t_r = t_f$ = 1 µs		15	50	mV
PSRR	PSRR	f = 10 Hz to 10 kHz V_{DD} = 3.6 V, $I_{OUT} = I_{MAX}/2$	60	70		dB
Output noise	N	f = 10 Hz to 100 kHz V_{DD} = 3.6 V I_{OUT} = 5 mA to I_{MAX}		80		µVrms
Quiescent current in ON mode	IQ_{ON}	Note 2		8 µA +0.5 % of I_{OUT}		µA
Quiescent current in OFF mode	IQ_{OFF}				1	µA
Turn on time	T_{ON}	10 % to 90 %			200	µs
Turn off time	T_{OFF}	90 % to 10 %			10	ms
Pull down resistance in OFF mode	R_{OFF}			100		Ω

Note 1 Programmable in 50 mV voltage steps, maximum output voltage is determined by V_{DD} - dropout voltage.

Note 2 Internal regulator current flowing to ground.

5.12.7 LDO7

Table 21: LDO7 Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage	V_{DD}	(if supplied from buck)	2.8 (1.5)		V_{DDOUT} + 0.3 V, 5 V max	V
Output voltage	V_{LDO7}	$I_{OUT} = I_{MAX}$	1.2	Note 1	3.6	V
Output accuracy		$I_{OUT} = I_{MAX}$	-3		+3	%
Stabilization capacitor	C_{OUT}	(including voltage and temperature coefficient @ configured V_{LDO7})	-55 %	2.2	+35 %	µF
ESR of capacitor		f > 1 MHz			0.1	Ω
Maximum output current	I_{MAX}	V_{DD} ≥ 1.8 V	200			mA
Short circuit current	I_{SHORT}			400		mA
Dropout voltage	$V_{DROPOUT}$	$I_{OUT} = I_{MAX}$ (for V_{DD} = 1.5 V $I_{OUT} = I_{MAX}/3$)		100	150	mV
Static line regulation	VS_{LINE}	V_{DD} = 3.0 V to 5.0 V $I_{OUT} = I_{MAX}$		5	20	mV
Static load regulation	VS_{LOAD}	I_{OUT} = 1 mA to I_{MAX}		5	20	mV
Line transient response	VTR_{LINE}	V_{DD} = 3.0 V to 3.6 V $I_{OUT} = I_{MAX}$ $t_r = t_f$ = 10 µs		5	20	mV
Load transient response	VTR_{LOAD}	V_{DD} = 3.6 V I_{OUT} = 1 mA to I_{MAX} $t_r = t_f$ = 1 µs		20	50	mV
PSRR	PSRR	f = 10 Hz to 10 kHz V_{DD} = 3.6 V, $I_{OUT} = I_{MAX}/2$	60	70		dB
Output noise	IQ_{ON}	f = 10 Hz to 100 kHz V_{DD} = 3.6 V I_{OUT} = 5 mA to I_{MAX}		80		µVrms
Quiescent current in ON mode	IQ_{OFF}	Note 2		8 µA +0.4 % of I_{OUT}		µA
Quiescent current in OFF mode	T_{ON}				1	µA
Turn on time	T_{OFF}	10 % to 90 %			600	µs
Turn off time	R_{OFF}	90 % to 10 %			10	ms

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Pull down resistance in OFF mode				100		Ω

Note 1 Programmable in 50 mV voltage steps, maximum output voltage is determined by V_{DD} - dropout voltage.

Note 2 Internal regulator current flowing to ground.

5.12.8 LDO8

Table 22: LDO8 Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage	V_{DD}	(if supplied from buck)	2.8 (1.5)		V_{DDOUT} + 0.3 V, 5 V max	V
Output voltage	V_{LDO8}	$I_{OUT} = I_{MAX}$	1.2	Note 1	3.6	V
Output accuracy		$I_{OUT} = I_{MAX}$	-3		+3	%
Stabilization capacitor	C_{OUT}	(including voltage and temperature coefficient @ configured V_{LDO8})	-55 %	2.2	+35 %	µF
ESR of capacitor		f > 1 MHz			0.1	Ω
Maximum output current	I_{MAX}	VDD ≥ 1.8 V	200			mA
Short circuit current	I_{SHORT}			400		mA
Dropout voltage	$V_{DROPOUT}$	$I_{OUT} = I_{MAX}$ (for V_{DD} = 1.5 V $I_{OUT} = I_{MAX}/3$)		100	150	mV
Static line regulation	VS_{LINE}	V_{DD} = 3.0 V to 5.0 V $I_{OUT} = I_{MAX}$		5	20	mV
Static load regulation	VS_{LOAD}	I_{OUT} = 1 mA to I_{MAX}		5	20	mV
Line transient response	VTR_{LINE}	V_{DD} = 3.0 V to 3.6 V $I_{OUT} = I_{MAX}$ $t_r = t_f$ = 10 µs		5	20	mV
Load transient response	VTR_{LOAD}	V_{DD} = 3.6 V I_{OUT} = 1 mA to I_{MAX} $t_r = t_f$ = 1 µs		20	50	mV
PSRR	PSRR	f = 10 Hz to 10 kHz V_{DD} = 3.6 V, $I_{OUT} = I_{MAX}/2$	60	70		dB
Output noise	N	f = 10 Hz to 100 kHz V_{DD} = 3.6 V I_{OUT} = 5 mA to I_{MAX}		80		µVrms
Quiescent current in ON mode	IQ_{ON}	Note 2		8 µA +0.4 % of I_{OUT}		µA
Quiescent current in	IQ_{OFF}				1	µA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OFF mode						
Turn on time	T_{ON}	10 % to 90 %			200	µs
Turn off time	T_{OFF}	90 % to 10 %			10	ms
Pull down resistance in OFF mode	R_{OFF}			100		Ω

Note 1 Programmable in 50 mV voltage steps, maximum output voltage is determined by V_{DD} - dropout voltage.

Note 2 Internal regulator current flowing to ground.

5.12.9 LDO9

Table 23: LDO9 Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage	V_{DD}	(if supplied from buck)	2.8 (1.5)		V_{DDOUT} + 0.3 V,5 V max	V
Output voltage	V_{LDO9}	$I_{OUT} = I_{MAX}$	1.25	Note 1	3.6	V
Output accuracy		$I_{OUT} = I_{MAX}$	-1		+1	%
Stabilization capacitor	C_{OUT}	(including voltage and temperature coefficient @ configured VLDO9)	-55 %	1.0	+35 %	µF
ESR of capacitor		f > 1 MHz			0.1	Ω
Maximum output current	I_{MAX}	V_{DD} ≥ 1.8 V	100			mA
Short circuit current	I_{SHORT}			200		mA
Dropout voltage	$V_{DROPOUT}$	$I_{OUT} = I_{MAX}$ (for VDD = 1.5 V $I_{OUT} = I_{MAX}/3$)		100	200	mV
Static line regulation	VS_{LINE}	V_{DD} = 3.0 V to 5.0 V $I_{OUT} = I_{MAX}$		5	20	mV
Static load regulation	VS_{LOAD}	I_{OUT} = 1 mA to I_{MAX}		5	20	mV
Line transient response	VTR_{LINE}	V_{DD} = 3.0 V to 3.6 V $I_{OUT} = I_{MAX}$ $t_r = t_f$ = 10 µs		5	20	mV
Load transient response	VTR_{LOAD}	V_{DD} = 3.6 V I_{OUT} = 1 mA to I_{MAX} $t_r = t_f$ = 1 µs		15	50	mV
PSRR	PSRR	f = 10 Hz to 10 kHz V_{DD} = 3.6 V, $I_{OUT} = I_{MAX}/2$	60	70		dB
Output noise	N	f = 10 Hz to 100 kHz V_{DD} = 3.6 V I_{OUT} = 5 mA to I_{MAX}		80		µVrms
Quiescent current in ON mode	IQ_{ON}	Note 1		8 µA +0.7 %		µA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
				of I_{OUT}		
Quiescent current in OFF mode	IQ_{OFF}				1	µA
Turn on time	T_{ON}	10 % to 90 %			200	µs
Turn off time	T_{OFF}	90 % to 10 %			10	ms
Pull down resistance in OFF mode	R_{OFF}			100		Ω

Note 1 Programmable in 50 mV voltage steps, max output voltage is determined by V_{DD} - dropout voltage.

Note 2 Internal regulator current flowing to ground.

5.12.10 LDO10

Table 24: LDO10 Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage	V_{DD}	(if supplied from buck)	2.8 (1.5)		V_{DDOUT} + 0.3 V, 5 V max	V
Output voltage	V_{LDO10}	$I_{OUT} = I_{MAX}$	1.2	Note 1	3.6	V
Output accuracy		$I_{OUT} = I_{MAX}$	-3		+3	%
Stabilization capacitor	C_{OUT}	(including voltage and temperature coefficient @ configured V_{LDO10})	-55 %	2.2	+35 %	µF
ESR of capacitor		f > 1 MHz			0.1	Ω
Maximum output current	I_{MAX}	V_{DD} ≥ 1.8 V	250			mA
Short circuit current	I_{SHORT}			500		mA
Dropout voltage	$V_{DROPOUT}$	$I_{OUT} = I_{MAX}$ (for V_{DD} < 1.8 V $I_{OUT} = I_{MAX}/3$)		100	150	mV
Static line regulation	VS_{LINE}	V_{DD} = 3.0 V to 5.0 V $I_{OUT} = I_{MAX}$		5	20	mV
Static load regulation	VS_{LOAD}	I_{OUT} = 1 mA to I_{MAX}		5	20	mV
Line transient response	VTR_{LINE}	V_{DD} = 3.0 V to 3.6 V $I_{OUT} = I_{MAX}$ $t_r = t_f$ = 10 µs		5	20	mV
Load transient response	VTR_{LOAD}	V_{DD} = 3.6 V I_{OUT} = 1 mA to I_{MAX} $t_r = t_f$ = 1 µs		30	50	mV
PSRR	PSRR	f = 10 Hz to 10 kHz V_{DD} = 3.6 V, $I_{OUT} = I_{MAX}/2$	60	70		dB
Output noise	N	f = 10 Hz to 100 kHz		80		µVrms

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
		V_{DD} = 3.6 V I_{OUT} = 5 mA to I_{MAX}				
Quiescent current in ON mode	IQ_{ON}	Note 2		8 µA +0.3 % of I_{OUT}		µA
Quiescent current in OFF mode	IQ_{OFF}				1	µA
Turn on time	T_{ON}	10 % to 90 %			300	µs
Turn off time	T_{OFF}	90 % to 10 %			10	ms
Pull down resistance in OFF mode	R_{OFF}			100		Ω

Note 1 Programmable in 50 mV voltage steps, max output voltage is determined by V_{DD} - dropout voltage.

Note 2 Internal regulator current flowing to ground.

5.12.11 LDOCORE

Table 25: LDOCORE Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output voltage	V_{DDCORE}	I_{OUT} =0 mA to I_{MAX} When supplied from V_{BBAT}	2.45 2.15	2.5 2.2	2.55 2.25	V
Decoupling capacitor	C_{IN}	On V_{DD_REF}	-35 %	2.2	+35 %	µF
Stabilization capacitor	C_{OUT}	Including voltage and temperature coefficient	-55 %	100	+35 %	nF
ESR resistance		f > 1 MHz			0.1	Ω
Dropout voltage	$V_{DROPOUT}$	Note 1		50	100	mV

Note 1 Setting $V_{DD\_FAULT\_LOWER}$ ≥ 2.65 V avoids LDOCORE dropout. See Section 5.6 for more details!

5.13 DC/DC Buck Converters

5.13.1 BUCKCORE

Table 26: BUCKCORE Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage	V_{DD}		2.8 Note 1		5.0 Note 1	V
Output capacitor	C_{OUT}		-30 %	40	+30 %	µF
Output capacitor ESR		f > 100 kHz all caps + track impedance		25	50	mΩ
Inductor value	L_{BUCK}		-30 %	2.2	+30 %	µH
Inductor resistance	L_{DCR}			100	150	mΩ
Output voltage	V_{BCORE}	I_{OUT} = I_{MAX}	0.725	Note 2	2.075	V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output voltage accuracy		incl. static line / load regulation	-3	Note 3	+3	%
Output voltage ripple		$I_{OUT} = I_{MAX}$		10		mV
Load regulation transient	VTR_{LOAD}	I_{OUT} = 0 mA / 500 mA, dI/dt = 50 mA/µs		15	30	mV
Line regulation transient	VTR_{LINE}	V_{DD} = 3.0 V.to 3.6 V I_{OUT} = 500 mA t_r=t_f=10 µs		3	8	mV
Output current	I_{MAX}		2000	Note 4		mA
Current limit (programmable)	I_{LIM}	BUCKCORE_ILIM= 00	-20 %	1600	20 %	mA
		BUCKCORE_ILIM= 01	-20 %	2000	20 %	mA
		BUCKCORE_ILIM= 10	-20 %	2400	20 %	mA
		BUCKCORE_ILIM= 11	-20 %	3000	20 %	mA
Quiescent current in OFF mode	IQ_{FF}				1	µA
Quiescent current in synchronous rectification mode	IQ_{ON}	open loop Note 5		4.0		mA
Switching frequency	f			2		MHz
Switching duty cycle	D		10		90	%
Turn on time	T_{ON}				2.2	ms
Output pull down resistor		@ V_{OUT} = 0.5 V, can be switched off via CORE_PD_DIS			200	Ω
Efficiency	η	I_{OUT}=30 mA to I_{MAX} V_{DD} < 4.2 V		85	90	%
On resistance pMOS	R_{pMOS}	incl. pin and routing		0.22	0.3	Ω
On resistance nMOS	R_{nMOS}	incl. pin and routing			0.2	Ω
PFM mode						
Output voltage	V_{BCORE}	I_{OUT} < 70 mA	0.5	Note 6	2.075	V
Typical mode switching current				100		mA
Output current	I_{OUT}		180			mA
Current limit	I_{LIM}		-20 %	400	+30 %	mA
Quiescent current in PFM mode	IQ_{PFM}	I_{OUT} = 0 mA		50	70	µA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Frequency of operation			0		5	MHz
Efficiency	η	I_{OUT} = 10 mA to 140 mA V_{DD} < 4.2 V		80		%
Mode transition time				16	18	µs

Note 1 Must be in the range of V_{DDOUT} +/- 0.3 V.

Note 2 Programmable in 25 mV increments with micro voltage ramp step size of 6.25 mV/µs while slewing.

Note 3 Minimum tolerance is +/-30 mV.

Note 4 BUCKCORE requires >1 V between V_{DD} and V_{BCORE}. This ratio depends on L_{DCR} and routing impedances.

Note 5 Quiescent current measurement in open loop synchronous mode. In closed loop configuration, switching losses at Iload = 0 will also increase IQ_{ON}.

Note 6 Max. V_{DD} – 1.0 V.

5.13.2 BUCKPRO

Table 27: BUCKPRO Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage	V_{DD}		2.8 Note 1		5.0 Note 1	V
Output capacitor	C_{OUT}		-30 %	20	+30 %	µF
Output capacitor ESR		f > 100 kHz all caps + track impedance		25	50	mΩ
Inductor value	L_{BUCK}		-30 %	2.2	+30 %	µH
Inductor resistance	L_{DCR}			100	150	mΩ
Output voltage	V_{BPRO}	I_{OUT} = $I_{MAX,}$	0.725	Note 2	2.075	V
Output voltage accuracy		incl. static line / load regulation	-3	Note 3	+3	%
Output voltage ripple		I_{OUT} = I_{MAX}		10		mV
Load regulation transient	VTR_{LOAD}	I_{OUT} = 0 mA / 500 mA, dI/dt = 50 mA/µs		15	30	mV
Line regulation transient	VTR_{LINE}	V_{DD} = 3.0 V.to.3.6V I_{OUT} = 500 mA t_r=t_f=10 µs		3	8	mV
Output current	I_{MAX}		1000	Note 4		mA
Current limit (programmable)	I_{LIM}	BUCKPRO_ILIM=00	-20 %		20 %	mA
		BUCKPRO_ILIM=01	-20 %		20 %	mA
		BUCKPRO_ILIM=10	-20 %		20 %	mA
		BUCKPRO_ILIM=11	-20 %		20 %	mA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Quiescent current in OFF mode	IQ_{FF}				1	µA
Quiescent current in synchronous rectification mode	IQ_{ON}			2.5		mA
Switching frequency	f			2		MHz
Switching duty cycle	D		10		90	%
Turn on time	T_{ON}	open loop Note 5			2.2	ms
Output pull down resistor		@ V_{OUT} = 0. 5V, can be switched off via PRO_PD_DIS			200	Ω
Efficiency	η	I_{OUT}=30 mA to I_{MAX} V_{DD} <4.2 V		85		%
On resistance pMOS	R_{pMOS}	incl. pin and routing		0.33	0.46	Ω
On resistance nMOS	R_{nMOS}	incl. pin and routing			0.3	Ω
PFM mode						
Output voltage	V_{BPRO}	I_{OUT} < 70 mA	0.5	Note 6	2.075	V
Typical mode switching current				50		mA
Output current	I_{OUT}		90			mA
Current limit	I_{LIM}		-20 %	200	+30 %	mA
Quiescent current in PFM mode	IQ_{PFM}	I_{OUT} = 0 mA		25	45	µA
Frequency of operation			0		5	MHz
Efficiency	η	I_{OUT} = 10 mA to 90 mA V_{DD} < 4.2 V		80		%
Mode transition time				16	18	µs

Note 1 Must be in the range of V_{DDOUT} +/- 0.3 V.

Note 2 Programmable in 25 mV increments with micro voltage ramp step size of 6.25 mV/µs while slewing.

Note 3 Minimum tolerance is +/-30 mV.

Note 4 BUCKPRO requires >1 V between V_{DD} and V_{BPRO}. This ratio depends on L_{DCR} and routing impedances.

Note 5 Quiescent current measurement in open loop synchronous mode. In closed loop configuration, switching losses at Iload = 0 will also increase IQ_{ON}.

Note 6 Max. V_{DD} – 1.0 V.

5.13.3 BUCKMEM

Table 28: BUCKMEM Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage	V_{DD}		2.8 Note 1		5.0 Note 1	V
Output capacitor	C_{OUT}		-30 %	20	+30 %	µF
Output capacitor ESR		f > 100 kHz all caps + track impedance		25	50	mΩ
Inductor value	L_{BUCK}		-30 %	2.2	+30 %	µH
Inductor resistance	L_{DCR}			100	150	mΩ
Output voltage	V_{BMEM}	$I_{OUT} = I_{MAX}$	0.95	Note 2	2.525	V
Output voltage accuracy		incl. static line / load regulation	-3	Note 3	+3	%
Output voltage ripple		$I_{OUT} = I_{MAX}$		10		mV
Load regulation transient	VTR_{LOAD}	I_{OUT} = 0 mA / 500 mA, dI/dt = 30 mA/µs		20	40	mV
Line regulation transient	VTR_{LINE}	V_{DD} = 3.0 V.to.3.6 V I_{OUT} = 500 mA t_r=t_f=10 µs		5	10	mV
Output current	I_{MAX}		1000	Note 4		mA
Current limit (programmable)	I_{LIM}	BUCKMEM_ILIM=00	-20 %	800	20 %	mA
		BUCKMEM_ILIM=01	-20 %	1000	20 %	mA
		BUCKMEM_ILIM=10	-20 %	1200	20 %	mA
		BUCKMEM_ILIM=11	-20 %	1500	20 %	mA
Quiescent current in OFF mode	IQ_{FF}				1	µA
Quiescent current in synchronous rectification mode	IQ_{ON}	open loop Note 5		2.5		mA
Switching frequency	f			2		MHz
Switching duty cycle	D		10		90	%
Turn on time	T_{ON}				2.2	ms
Output pull down resistor		@ V_{OUT} = 0.5 V, can be switched off via MEM_PD_DIS			200	Ω
Efficiency	η	I_{OUT}=30 mA to I_{MAX} V_{DD} <4.2 V		85		%
On resistance pMOS	R_{pMOS}	incl. pin and routing		0.33	0.46	Ω

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
On resistance nMOS	R_{nMOS}	incl. pin and routing			0.3	Ω
PFM mode						
Typical mode switching current				50		mA
Output current	I_{OUT}		90			mA
Current limit	I_{LIM}		-20 %	200	+30 %	mA
Quiescent current in PFM mode	IQ_{PFM}	I_{OUT} = 0		25	45	µA
Frequency of operation			0		5	MHz
Efficiency	η	I_{OUT} = 10 mA to 90 mA V_{DD} < 4.2 V	80			%
Mode transition time				16	18	µs
VMEM_SW switch RON		VBMEM=1.8 V Vdrop=200 mV			0.65	Ω
VMEM_SW switch Turn on time		VBMEM=1.8 V Cload=10 µF max		200	400	µs
VMEM_SW switch Rpull-down		VBMEM=1.8 V Vout=100 mV		200		Ω

Note 1 Must be in the range of V_{DDOUT} +/- 0.3 V.

Note 2 Programmable in 25 mV increments with micro voltage ramp step size of 6.25 mV/us while slewing.

Note 3 Minimum tolerance is +/-35 mV.

Note 4 BUCKMEM requires > 1 V between V_{DD} and V_{BMEM}. This ratio depends on L_{DCR} and routing impedances.

Note 5 Quiescent current measurement in open loop synchronous mode. In closed loop configuration, switching losses at Iload = 0 will also increase IQ_{ON}.

5.13.4 BUCKPERI

Table 29: BUCKPERI Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage	V_{DD}		2.8 Note 1		5.0 Note 1	V
Output capacitor	C_{OUT}		-30 %	20	+30 %	µF
Output capacitor ESR		f > 100 kHz all caps + track impedance		25	50	mΩ
Inductor value	L_{BUCK}		-30 %	2.2	+30 %	µH
Inductor resistance	L_{DCR}			100	150	mΩ
Output voltage	V_{BPERI}		0.95	Note 2	2.525	V
Output voltage accuracy		incl. static line / load	-3	Note 3	+3	%

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
		regulation				
Output voltage ripple		$I_{OUT} = I_{MAX}$		10		mV
Load regulation transient	VTR_{LOAD}	I_{OUT} = 0 mA / 500 mA, dI/dt = 50 mA/µs		20	40	mV
Line regulation transient	VTR_{LINE}	VDD = 3.0 V to 3.6 V I_{OUT} = 500 mA t_r=t_f=10 µs		5	10	mV
Output current	I_{MAX}		1000	Note 4		mA
Current limit (programmable)	ILIM	BUCKPERI_ILIM=00	-20 %	800	20 %	mA
		BUCKPERI_ILIM=01	-20 %	1000	20 %	mA
		BUCKPERI_ILIM=10	-20 %	1200	20 %	mA
		BUCKPERI_ILIM=11	-20 %	1500	20 %	mA
Quiescent current in OFF mode	IQ_{FF}				1	µA
Quiescent current in synchronous rectification mode	IQ_{ON}	open loop Note 5		2.5		mA
Switching frequency	f			2		MHz
Switching duty cycle	D		20		90	%
Turn on time	T_{ON}				2.2	ms
Output pull down resistor		@ V_{OUT} = 0.5 V			200	Ω
Efficiency	η	$I_{OUT} < I_{MAX}$ $V_{DD} < 4.2$ V		80	85	%
On resistance pMOS	R_{pMOS}	incl. pin and routing		0.33	0.46	Ω
On resistance nMOS	R_{nMOS}	incl. pin and routing			0.3	Ω
PFM mode						
Typical mode switching current				50		mA
Output current	I_{OUT}		90			mA
Current limit	I_{LIM}		-20 %	200	+30 %	mA
Quiescent current in PFM mode	IQ_{PFM}	I_{OUT} = 0		25	45	µA
Frequency of operation			0		5	MHz
Efficiency	η	I_{OUT} = 10 mA to 90 mA $V_{DD} < 4.2$ V		80		%
Mode transition time				16	18	µs
VPERI_SW switch		V_{BPERI} = 1.8 V			0.65	Ω

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
RON		Vdrop=200 mV				
VPERI_SW switch Turn on time		V_{BPERI} = 1.8 V Cload=10 µF max		200	400	µs
VPERI_SW switch Rpull-down		VBPERI = 1.8 V Vout=100 mV		200		Ω

Note 1 Must be in the range of V_{DDOUT} +/- 0.3 V.

Note 2 Programmable in 25 mV increments.

Note 3 Minimum tolerance is +/-35 mV.

Note 4 BUCKPERI requires >1 V between V_{DD} and V_{BPERI}. This ratio depends on L_{DCR} and routing impedances.

Note 5 Quiescent current measurement in open loop synchronous mode. In closed loop configuration, switching losses at Iload = 0 will also increase IQ_{ON}.

5.14 Battery Charger

5.14.1 Charger Supply Modes

Table 30: Charger Supply Mode Characteristics

Supply mode	Symbol	Conditions	Min	Typ	Max	Unit
VBUS (low-power USB, 100 mA)	VBUS	upstream port voltage with 500 mΩ impedance	4.4		5.5	V
	ISET_USB<3:0>	10 mA steps	80		120	mA
VBUS (high-power USB, 500 mA)	VBUS	upstream port voltage with 500 mΩ impedance	4.75		5.5	V
	ISET_USB<3:0>	50 mA steps	400		600	mA
VBUS (DCHG USB, 2000 mA)	VBUS	upstream port voltage with 200 mΩ impedance	4.5		5.5	V
	ISET_USB<3:0>	200 mA steps	600		1800	mA
DCIN (Wall Brick, 2000 mA)	VDCIN	As VBUS, Higher currents can require higher voltages	4.4		5.5	V
	ISET_DCIN<3:0>	10 mA, 50 mA and 200 mA steps	80		1800	mA

5.14.2 Charger Buck

Table 31: Charger Buck Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage	V_{CENTER}		4.4		5.6	V
Output capacitor	C_{OUT}		30			µF
ESR of output capacitor		f > 100 kHz			20	mΩ
Inductor value	L_{BUCK}		-30 %	2.2 to 4.7	+30 %	µH
Inductor resistance	L_{DCR}	f = 1 MHz			100	mΩ
Output voltage	V_{DDOUT}	I_{OUT}= 1000 mA included static load regulation	3.6	V_{BAT} + 250 mV		V
Ripple voltage		I_{OUT} = 1000 mA L_{BUCK} = 4.7 µH		10		mV
Static load regulation	VS_{LOAD}	I_{OUT} = 1 mA to 1000 mA		55	80	mV
Load regulation transient	VTR_{LOAD}	I_{OUT}: 0 mA / 1000 mA, dI/dt = 20 mA/µs		45	65	mV
Line regulation transient	VTR_{LINE}	VBUS_PROT=4.4 V to 5.6 V I_{OUT}=1000 mA $t_r = t_f$ = 10 µs		10		mV
Output current	I_{MAX}		1890			mA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Current limitation	I_{LIM}	2-wire programmable 10 mA, 50 mA and 200 mA steps	70		1800	mA
Quiescent current in OFF mode					1	µA
Quiescent current in synchronous rectification mode				5		mA
F_BUCK frequency of operation				2		MHz
Switching duty cycle			10		100	%
Ton turn on time					2.2	ms
Efficiency		I_{OUT} = 1000 mA VBUS_PROT = 5 V	85	90		%
R_PMOS PMOS on resistance		including pin and routing	0.08	0.15	0.2	Ω
R_NMOS NMOS on resistance		including pin and routing	0.15	0.25	0.3	Ω
R_VBUS_PROT internal switch on resistance		including pin and routing, VBUS_PROT= 4.8 V	0.05	0.1	0.2	Ω
SLEEP mode – PFM mode						
Sleep mode output current	$I_{OUTSLEEP}$		100			mA
Current limitation			75	278	300	mA
IQ_ SLEEP – No load supply current in SLEEP mode		I_{OUT} = 0 mA		80	100	µA
F_BUCK Frequency of operation			0		5	MHz
Efficiency		I_{OUT} = 10 mA to 100 mA		90		%
Efficiency		I_{OUT} = 1 mA to 50 mA V_{DD} =4.8 V		80		%
Mode transition time				16	18	µs

5.14.3 Voltage Levels on VBAT

Table 32: Voltage Levels on VBAT

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
BAT_FAULT				2.8		V
Battery voltage range	V_{BAT}		2.8		4.425	V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
ICHG_BAT		V_{BAT} < BAT_FAULT	20	40	60	mA

5.14.4 Charging Modes

Table 33: Charging Modes

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
CC mode output current		6 bits ICHG_BAT (30 mA steps)	0	300	1890	mA
CC absolute accuracy		ICHG_BAT < 100 mA	-10		+10	mA
CC absolute accuracy		ICHG_BAT > 100 mA	-10		+10	%
CV mode output voltage		VCHG_BAT (25 mV steps)	3.65	4.2	4.425	V
CV output voltage accuracy		VCHG_BAT	-25		25	mV

5.14.5 Charger Detection Circuit

Table 34: Charger Detection Circuit

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Charger detect threshold	VCH_DET	VCHG_BAT < 4.2 V	4.25	4.35	4.4	V
		VCHG_BAT > 4.2 V	4.45	4.55	4.6	V
Charger current limit reduction threshold		VCH_THR (configurable)	3.8	4.4	4.8	V
Charger insertion debounce time				10		ms
VBUS, DCIN excess voltage threshold			5.4	5.6	5.8	V

5.14.6 VBUS Charge Control

Table 35: VBUS Charge Control

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data source voltage	V_{DAT_SRC}	@I_{DAT_SRC}	0.5		0.7	V
Data source current	I_{DAT_SRC}		0		200	µA
Data detect voltage	V_{DAT_REF}	@I_{DAT_SINK}	0.25		0.4	V
Data sink current	I_{DAT_SINK}		50		150	µA
D+ source on time	$T_{DP\_SRC\_ON}$		100			ms
D+ source off to high current	T_{DPSRC_HICRNT}		40			ms
VBUS load in low-power suspend mode	$I_{VBUS\_SUSPEND}$	0 V ≤ VBUS ≤ 5.25 V T_{AVG} = <1 s, no spikes higher than 100 mA			500	µA

5.14.7 Charge Timer

Table 36: Charge Timer

Parameter	Register	Conditions	Min	Step	Max	Step
Total charging timer setting	TCTR	30 min total. Charge time is defined as the total charge time from when the charger was enabled (both for LINEAR and PRE-CHARGE mode charging). If the timer expires, the CHG_TO flag is set in the EVENT register, an IRQ issued and the charging is disabled. Setting the TCTR to 0x00 disables the timer.	0	30	450	min
Read back of current timer value	CHG_TIME	This register can be used to read back the current value of the charge time counter, counting down from the value loaded by the TCTR	0	2	510	min

5.14.8 DCCC and Active-Diode

Table 37: DCCC and Active Diode

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Active diode R_{on}		V_{BAT} = 3.6 V, I = 500 mA Including pin and routing		0.14		Ω
Circuit activation voltage		V_{BAT} - V_{DDOUT}	10	20	40	mV
Maximum diode current	ID_{max}			2.2		A

5.14.9 Backup Battery Charger

Table 38: Backup Battery Charger

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Backup battery charging current	BCHARGER_ISET	V_{IN} = 3.6 V, V_{BBAT} = 2.5 V	100	Note 1	6000	µA
Charger termination voltage	BCHARGER_VSET	V_{IN} = 3.6 V	1.1		3.1	V
Backup battery short circuit current		V_{BBAT} = 0 V		9		mA
Stabilizationcapacitor	C_{OUT}		55 %	470	+35 %	nF
ESR of capacitor		f > 1 MHz			0.1	Ω
Dropout voltage	$V_{DROPOUT}$	I_{OUT} = 5 mA		150	200	mV
Quiescent current	IQ	I_{OUT} > 50 µA		5.25 + 1.75 % of I_{OUT}		µA
		I_{OUT} < 50 µA		5.25 + 1.5 % of I_{OUT}		µA

Note 1 Programmable in 100 µA increments from 100 µA to 1000 µA and 1 mA increments from 1 mA to 6 mA.

5.14.10 Boost Converter

Table 39: Boost Converter

- Parameters measured using external components shown in Conditions.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output voltage	V_{BOOST}	2.8 V < V_{IN} < 4.5 V 0.03 mA < I_{LOAD} <50 mA	4.6		25	V
Efficiency		1 MHz, V_{BOOST} = 20 V I_{LOAD} = 50 mA;		80		%
Output voltage ripple		I_{LOAD} = 26 mA C_{OUT} = 2 µF (@ max V_{OUT})		200		mV_{p-p}
Operating quiescent Current		I_{LOAD} = 0 mA; automatically changed to discontinuous mode		250	350	µA
Shutdown quiescent current		Leakage of ext. transistor and feedback resistors excluded			1	µA
Switching frequency		Programmable	-10 %	1 or 2	+10 %	MHz
Programmable output current (reg. 0x24/0x25)		LEDx_IN	0.05		26	mA
Inductor			-20 %	4.7	+20 %	µH
Inductor current limitation		Tolerance w/o ext. resistor	-20 %	1100 Note 1	+20 %	mA
Decoupling capacitor	C_{boost}	Ceramic capacitor recommended; figure with 25 V voltage bias, may correspond to 10 µF nom. value without bias	1	2		µF
ESR C_{boost}		f > 100 kHz		100		mΩ
Current monitoring resistor Rsense		External connection from sense resistor to BOOST_SENSEP input		0.1		Ω
Output voltage overshoot				1	2.5	V
Over-voltage threshold		Voltage at BOOST_PROT pin		1.38		V

Note 1 For reduced backlight power requirements a lower current limitation of 710 mA can be selected via control BOOST_ILIM.

5.14.11 WLED Driver

Table 40: WLED Driver

Parameter	Conditions	Min	Typ	Max	Unit
Absolute output current accuracy (LED1_IN1 / LED2_IN / LED3_IN)	Full scale tolerance Linearity 1 mA to 26 mA Linearity 0.1 mA to 1 mA	-20 -10 -20		+20 +10 +20	%
Relative output current accuracy (IOUT1 - IOUT2) / (IOUT1 + IOUT2)	I_{out}1/2/3 = 5 mA to. 26 mA I_{out}1/2/3 = < 5 mA	-3.25 -4.5		+3.25 +4.5	%
Current sink VDSAT	@ I_{OUT} = 26 mA		0.6		V
LED current sink VDMAX	Max. voltage drop at current source			5.5	V
Ramp step rate	TSTEP-UP		1		ms
IDAC step size	LEDx_CURRENT = 0 to 255		0.212		dB

5.15 ADC

Table 41: ADC

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
ADC reference voltage		V_{DDCORE} / TSIREF	1.8 Note 1	2.5	2.6	V
Off current					1	µA
ADC operating current		During conversion		100		µA
ADC resolution				10		bit
ADC integral non linearity				± 2		LSB
ADC differential non linearity				± 0.8		LSB
ADC absolute accuracy			12		15	mV
ADC conversion clock				1.0		MHz
Auto-zero time				5		µs
Conversion time				29		µs
Total ADC conversion Time				34		µs
Internal MUX-resistance	R_{INT}			5		kΩ
Maximum source impedance	R_{SOURCE} Note 2			100		kΩ
Internal sampling capacitor.				10		pF

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Acquisition time			10	12	14	µs
Input capacitance	C_{INT}	Total input capacitance		10.5		pF
VDDOUT voltage range Channel 0		V_{DDOUT} - V_{DDCORE} Gain of 1.25 ADC = [(V_{DDOUT}-2.5 V)*0.5] *1023	2.5		4.5	V
ICH current measurement using an internal current mirror device. Channel 1, used for dynamic safety timer and EOC detection		Equivalent to 3.9 mA/bit	0		1000	mA
TBAT voltage range Channel 2		Voltage across a NTC resistor in the battery pack, 50 µA biasing	0		VDDCORE	V
VBAT voltage range Channel 3		V_{BAT} - V_{DDCORE} Gain of 1.25 ADC = [(V_{BAT} - 2.5 V)*0.5] * 1023	2.5		4.5	V
ADCIN4 – 6 voltage range Channel 4 – 6		ADC = [V_{IN}/2.5 V] * 1023	0		2.5	V
VBBAT voltage range Channel 9		Gain of 0.5 ADC = [(V_{BBAT}/2.5 V)*0.5] * 1023	0		5.0	V
ADCIN4 current source Channel 4		If enabled		15		µA
ADCIN5 comparator threshold Channel 5		Disabled during ADCIN5 conversion		1.2		V
RON, TSI X-Y switches				5		Ω
MUX cross talk isolation				60		dB

Note 1 TSIREF voltage range.

Note 2 R_{SOURCE} is the impedance of the external source the ADC is sampling.

6 Accessory Identity Detection (ACC_ID_DET)

This block detects the status of the ACC_ID_DET pin. It is capable of detecting three different states:

- Floating (USB peripheral device connected)
- Shorted to ground (USB host device connected)
- Connected to ground via resistor (accessory asserted)

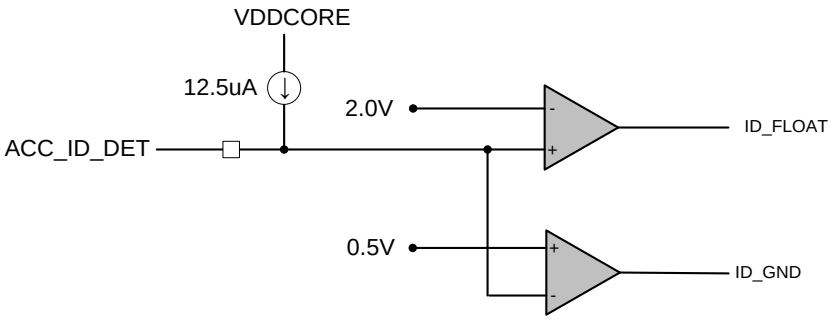

Figure 5: ID Detection Circuitry

The sensing can be turned on/off ID_FLOAT and ID_GND asserts an interrupt at both (rising and falling) edges. The sensing can be debounced. If a mini-USB or an accessory is connected to the ACC_ID_DET pin in POWER-DOWN mode a wake-up will be initiated (only at falling edge of ID_FLOAT).

If the accessory coding requires the detection of an impedance less than 40 kΩ an external resistor has to be placed between VDDCORE and ACC_ID_DET.

6.1 Accessory Detection States

Table 42: Accessory Detection States

External Resistance to GND	ACC_ID_DET State	ID_Float	ID_GND
R > 160 k Ω	Floating open pin. USB B-Device connected (peripheral)	High	Low
40 kΩ < R < 160 kΩ	High via resistor to ground. Accessory connected	Low	Low
R < 40 kΩ	Low < 10 Ω to ground. USB A-Device connected (host)	Low	High

Real Time Clock and 32 kHz Oscillator

The RTC block keeps track of the RTC clock counter and alarm function. The RTC block will operate from the LDOCORE power supply.

6.2 32 kHz Oscillator

The clock oscillator cell is used to drive the real time clock (RTC) counter. It works with an external piezoelectric oscillator crystal at 32.768 kHz.

In order to achieve typically the desired crystal frequency an external capacitor (10 pF to 20 pF, depending on the parasitic capacitance of the board) is connected to ground from each of the crystal pins. The start-up time of the oscillator is typically 0.5 s over the voltage range. When the crystal is not mounted the XTAL pins should be grounded. The 32 kHz clock signal is made available at the OUT_32K pin and the buffer can be disabled from the sequencer during POWER-DOWN mode.

The timekeeping error from the frequency variance of crystal oscillators (typ. +/-20 ppm) can be trimmed individually by +/- 242 ppm with a resolution of 1.9 ppm (1/(32768 x 16)). The timekeeping correction will be applied only towards the on-chip RTC block. To avoid potential clock jitter issues, the 32 kHz clock signal at the OUT_32K pin provides the original frequency of the crystal.

NOTE
The oscillator inputs will be able to withstand a leakage current, corresponding to at least a 10 MΩ connected between the pin and any signal level between V_{DDOUT} and GND.

6.3 RTC Counter and Alarm

The RTC counter will count the number of 32 kHz clock periods, providing a seconds, minutes, hours, day, month and year output. Year 0 corresponds to 2000, the maximum is 63 years. The value of the RTC calendar shall be read-/write-able via the power manager communication. The calendar is reset to zero when VDDCORE is lost.

There is an alarm register containing minutes, hours, day, month, and year. When the RTC counter register value corresponds to the value set in the alarm an IRQ event will be triggered (and a wake-up if DA9053 is in POWER-DOWN mode). The trigger will also set a bit in an event register to notify that an alarm has occurred. The alarm can alternatively be asserted from a periodic tick signal that, depending on control TICK_Type, is either asserted every second or minute. In the case where the host has enabled both alarms it can be determined from the status of ALARM_Type whether the IRQ/wake-up was caused by the timer or the tick.

The power manager registers ALARM_ON and TICK_ON enable/disable the alarm/tick. The power manager register bit MONITOR will be set to 0 each time the RTC is powered up. Software shall set this bit to ‘1’ when setting the time and date, which will allow software to detect a subsequent loss of the clock.

NOTE
Values written into the RTC calendar and alarm registers have to be valid regarding the allowed value range (see register description, for example maximum 60 for seconds or minutes).

The RTC seconds registers define a 32-bit seconds counter (approx. 136 years), that can only be reset via the nPOR and starts counting seconds after nPOR is released. Using the RTC input clock the output ports GPO10 and GPO11 can be toggled with a configurable periodic pulse. In this mode GPO10 or GPO11 offer blinking LED drivers that are able to run in POWER-DOWN mode.

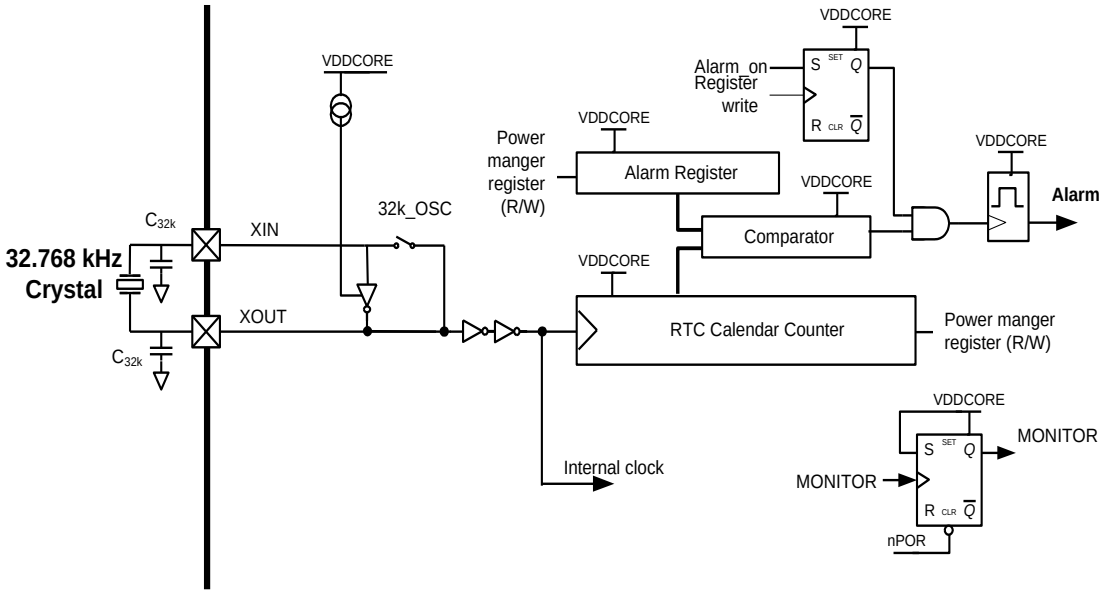

Figure 6: Schematic of the RTC Oscillator and Counter Functionality

6.4 Oscillator

Table 43: LPI Interface Signals

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DDCORE}		2.0	2.5	2.55	V
Oscillator crystal frequency	f_{OSC}			32.768		kHz
Crystal series resistance	R_{OSC}				100	kΩ
Output frequency	f_{OUT}			32.768		kHz
Start-up time for cell over the voltage range	T_{START}			0.5	2.0	s
Current consumption power down mode				1	5	µA
Current consumption active mode				3	5	µA
Input duty cycle	D_{XTAL1}	BYPASS mode	40	50	60	%
OUT_32K clock jitter		Cycle to cycle		20	30	ns

7 ID Code/Scratch Pad

DA9053 offers 10 general purpose registers, which can be configured from OTP cells. The OTP cells can be programmed during test/production with an individual code and so can provide a device specific serial number as required for music and media applications supporting Digital Rights Management (DRM). The general purpose registers are loaded from OTP when DA9053 starts-up from RESET-mode and can be 'read only' protected during fusing. If writing is enabled the registers can be used by the application to store up to 10 bytes of data that a host processor can use (for example after powering up from low-power modes).

7.1 Programming the ID Code/Scratch Pad

The ID code/scratch pad OTP cells can be programmed only once and cannot be erased. Programming can only take place when all of the following conditions are satisfied:

- DA9053 is in power commander mode.
- DA9053 has reached the active mode operational state.
- There is no charger attached.
- The supply voltage for the programming VPP has been provided at the VBUS node.
- The range modifiers have been set to select the correct addresses (OTP_GP = 1).
- The write access enable bit GP_WRITE_DIS has been set to program the intended GP register mode (after being programmed once to 'read only' registers R133 - R142 can only be written for fusing). The content received from a read can no longer be modified just by writing in to the registers.
- The lock bit in the OTP is in the correct state (OTP_GP_LOCK = 0).

NOTE
Connecting TP to VDDCORE enables the power commander mode.

The data intended to be programmed into the OTP must be first loaded into the related GP_ID registers using the HS 2-WIRE interface. The contents of the GP_ID registers are then transferred into the OTP cells by setting OTP_TRANSFER = OTP_RP = 1. Once started the transfer cannot be stopped. During an ongoing programming transfer the device will not react to any external events that otherwise would make it transition to other states. Upon completion of a transfer the OTP_TRANSFER bit will be reset automatically. So the end of the transfer can be determined by polling this bit.

If the lock bit OTP_GP_LOCK is set any further programming of the ID code/scratch pad is suppressed. If the write access control bit GP_WRITE_DIS is set, then the GP_ID registers become 'read-only' (reading content will be always a 100 % mirror of the related OTP cells).

In a production environment it is mandatory to check the success of the programming of the GP_ID registers by reading back the OTP contents. DA9053 defaults to performing a margin mode read which allows the reliability of the stored information to be assessed.

To initiate a read transfer from the OTP cells into the related GP_ID registers, firstly set OTP_GP = 1 to access the correct addresses, and then OTP_RP = 0 and OTP_TRANSFER = 1 to start the read operation. Read transfers are unaffected by the state of the lock or write enable bits.

8 Typical Characteristics

8.1 Buck Regulator Performance

The following performance was measured while using 2.2 µH inductors:

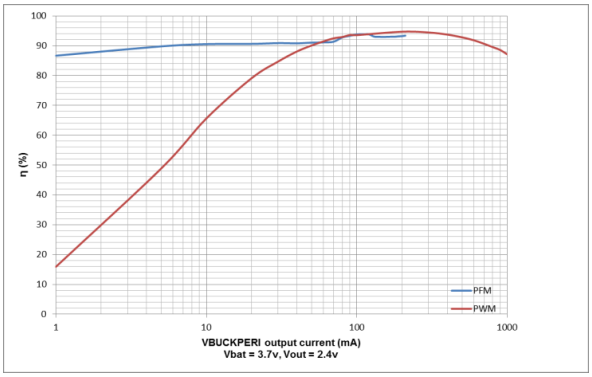

Figure 7: BUCKPERI Efficiency Curves

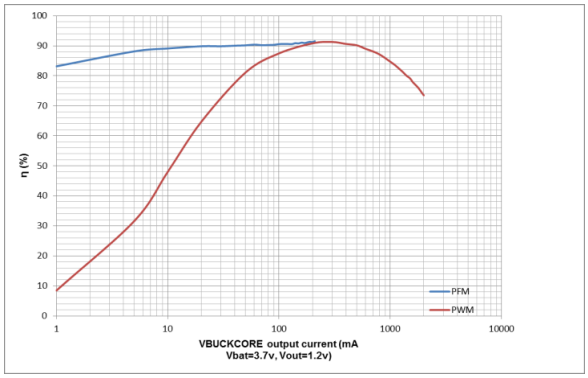

Figure 8: BUCKCORE Efficiency Curves

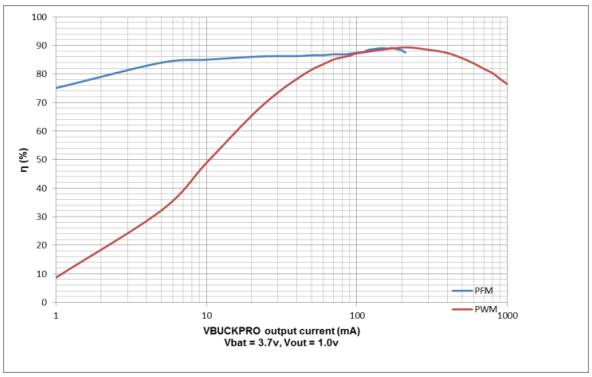

Figure 9: BUCKPRO Efficiency Curves

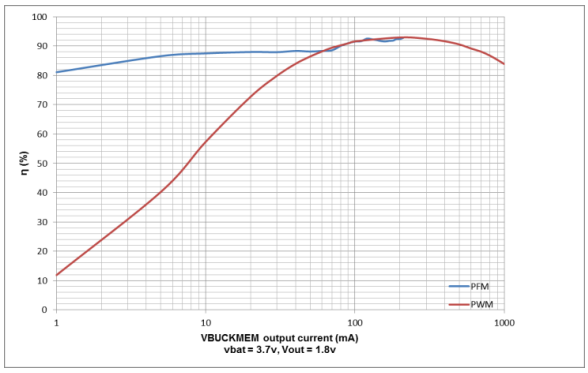

Figure 10: BUCKMEM Efficiency Curves

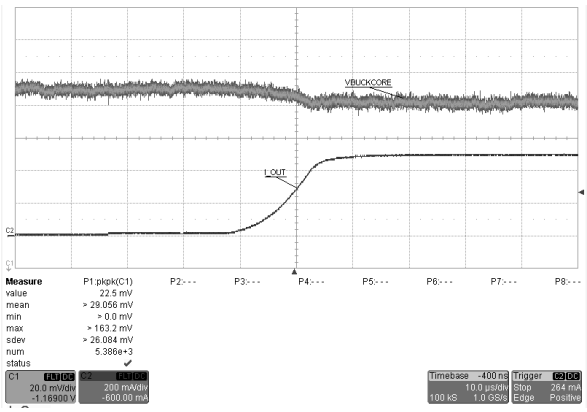

Figure 11: BUCKPRO Load Regulation Transient

Vout = 1.2 V, ILoad = 500 mA.

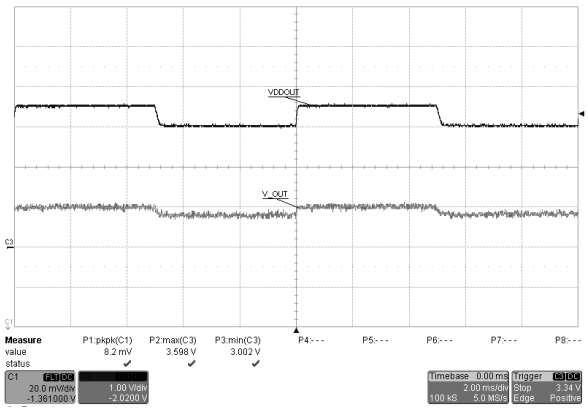

Figure 12: BUCKPRO Line Regulation Transient

Vbuck = 1.35 V, ILoad = 500 mA, Vsupply = 3 V

8.2 Linear Regulator Performance

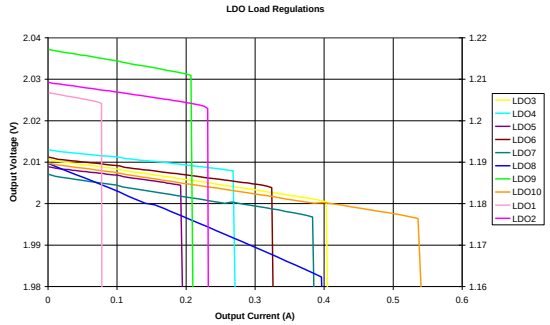

Figure 13: Typical LDO Load Regulation

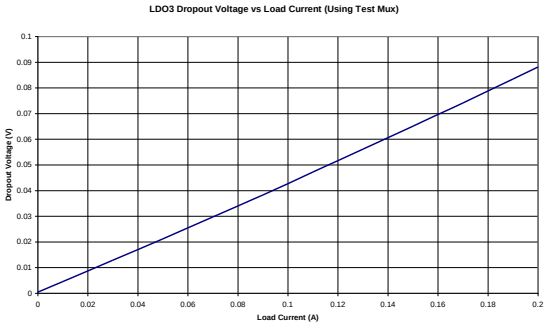

Figure 14: Typical LDO Drop-Out Voltage

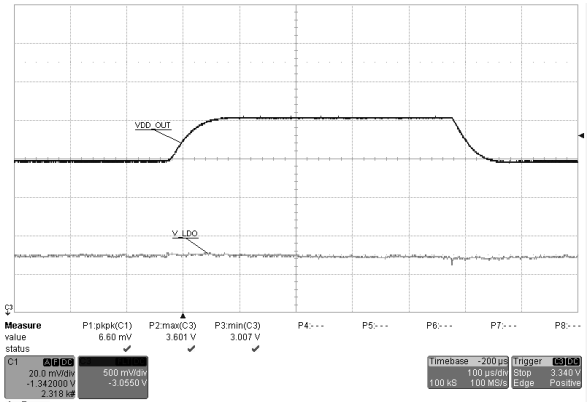

Figure 15: Typical LDO Line Transient

Transition of 3.6 V to 4.2 V at VBAT

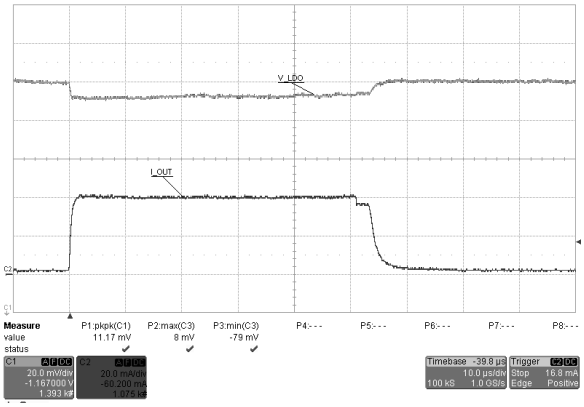

Figure 16: LDO Load Transient

(1 mA to Imax of 40 mA) VLDO = 1.2 V

8.3 Typical LDO Voltage vs Temperature

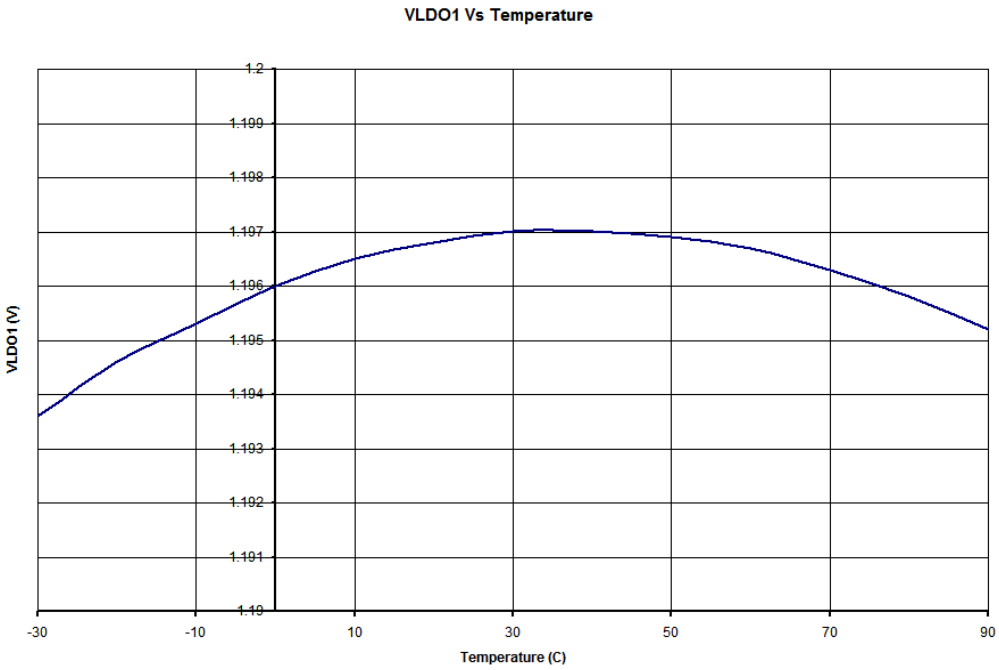

Figure 17: Typical LDO Voltage vs Temperature

8.4 ADC Performance

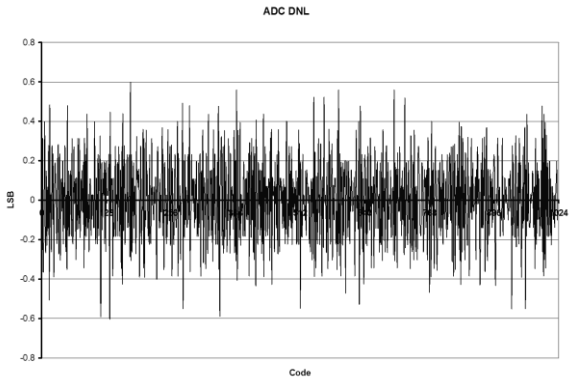

Figure 18: ADC DNL Performance

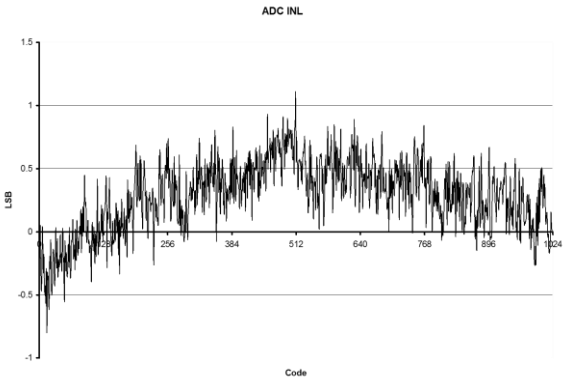

Figure 19: ADC INL Performance

8.5 Power Path Performance

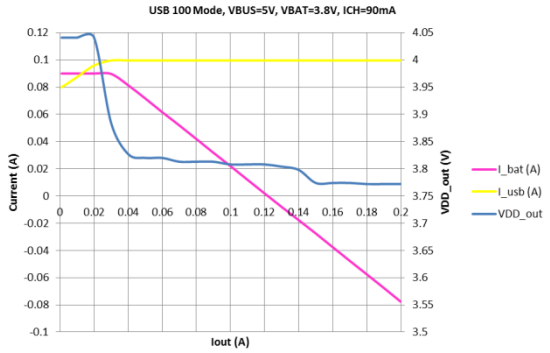

Figure 20: Power Path Behaviour USB 100 Mode

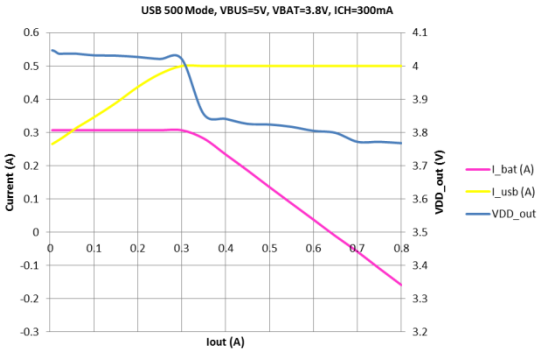

Figure 21: Power Path Behaviour USB 500 Mode

Figure 20 and Figure 21 and show increasing load current supplied from VBUS, powerpath loop reduces ICH until active diode turns on which then allows current from battery to supply system load current via VDD_OUT.

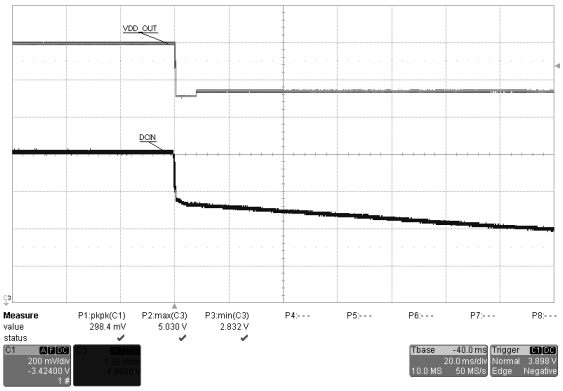

Figure 22: Transitioning Supply from VCHG (via DCIN) to VBAT

Top trace = VDDOUT, Bottom Trace = DCIN

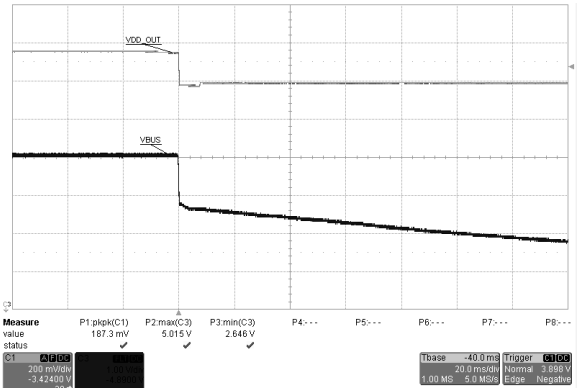

Figure 23: Transitioning Supply from USB 5 V (via VBUS) to VBAT

Top Trace = VDDOUT, Bottom Trace = VBUS

8.6 Boost and LED Current Control Performance

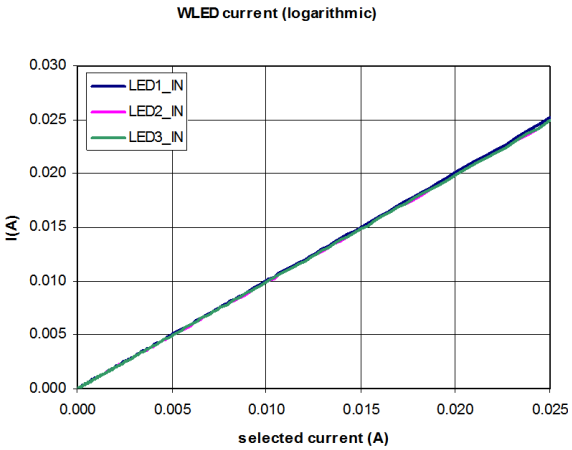

Figure 24: WLED Current Performance

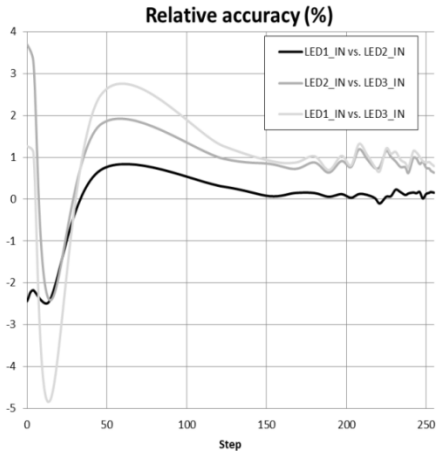

Figure 25: WLED Relative Accuracy

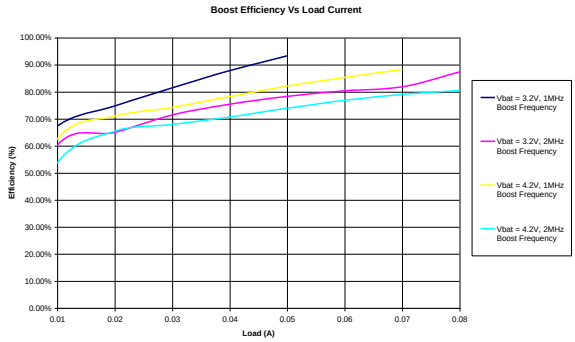

Figure 26: Boost Converter Efficiency Curves

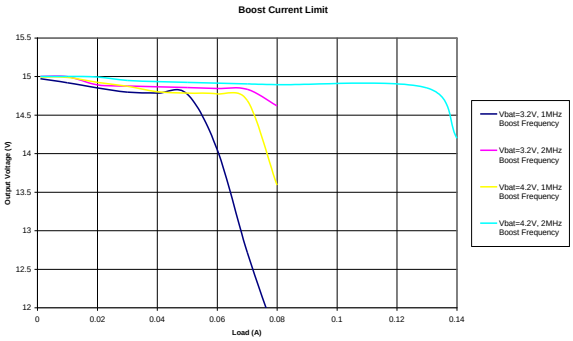

Figure 27: Boost Regulation Voltages

9 Functional Description

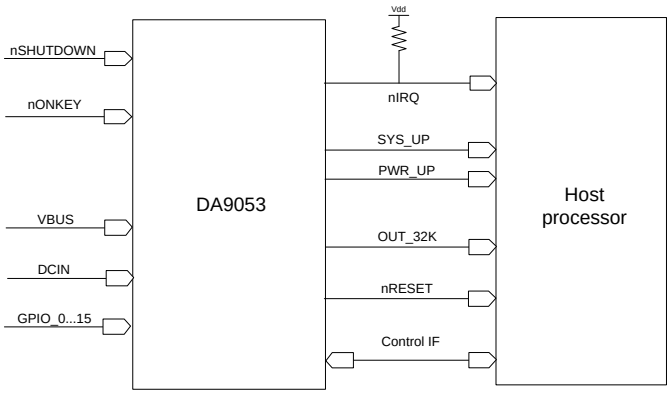

Figure 28: Control Ports and Interface

9.1 Power Manager IO Ports

The power manager input ports are supplied either from the internal rail VDDCORE or VDD_IO2. The output ports are supplied from VDD_IO1 or VDD_IO2. All output ports are push-pull type except nRESET, nIRQ and nVDD_FAULT.

9.2 On/Off and HW-Watchdog Port (nONKEY/KEEP_ACT)

The nONKEY signal is an edge triggered high to low wake-up interrupt/event intended to switch-on the DA9053 supplied application. nONKEY is always enabled during POWER-DOWN mode, so that the application can be switched-on with a disabled GPIO extender. The wake-up event can be disabled via the interrupt mask. This pin can be alternatively asserted to the watchdog unit, so that every assertion of the pin (rising edge sensitive) sets its bit similar to a write via the power manager bus. The host has to release KEEP_ACT in advance to the next assertion during continuous watchdog supervision (if enabled). The minimum assertion and de-assertion cycle time is 150 µs.

9.3 Hardware Reset (nSHUTDOWN, nONKEY, GPIO14 & GPIO15)

A user-initiated hard reset at the DA9053 nSHUTDOWN is an active low input initiated typically by a push button switch or an asserted error detection line from a host processor. The sequencer then powers down all domains in reverse order down to step 0 and all supplies of DA9053 except LDOCORE are switched off.

DA9053 includes a second hardware reset that follows the nONKEY after being asserted for a period of 5 s ±30 %. The same can be achieved by a parallel connection of GPI14 AND GPI15 to ground for 5 s ±30 %.

If the WATCHDOG has been disabled, this feature provides the ability to emergency turn-off the application in the event of a software lock-up without the need for a dedicated RESET hardware switch or removing the battery.

After a minimum time-out of 500 ms DA9053 will start to power up again. It will wait for a valid wake-up event (for example key press) or will start the power sequencer automatically if autoboot is enabled. By asserting EXT_WAKEUP it can request the host processor to control the subsequent start-up. Alternatively the power up sequence can be performed autonomously by the PMIC following OTP pre-configurations. A detection of a hard reset forces the assertion of nRESET to low when the sequencer returns from POWER-DOWN mode to RESET mode. This type of reset is typically used

only for severe and unrecoverable hardware or software problems, because it completely resets the processor and can result in data loss.

9.4 Reset Output (nRESET)

The nRESET signal is an active-low output signal from DA9053 to the host processor, which tells the host to enter the hardware-reset state. nRESET is always asserted at the beginning of a DA9053 cold start from NO-POWER mode to when the DA9053 returns to RESET mode. nRESET can also be asserted as a soft reset after the sequencer finishes powering down without progressing to RESET mode.

The reset timer trigger signal can be configured to be EXT_WAKEUP, SYS_UP or PWR1_UP. After being asserted nRESET remains low until the reset timer is started from the selected trigger signal and expires. The expiry time can be configured from 1 ms to 1024 ms.

9.5 Accessory and ID Detect (ACC_ID_DET)

In ACTIVE and POWER-DOWN modes the detector can track the condition of the USB ID line and differentiates between the following three conditions:

ACC_ID_DET:

- Floating (USB peripheral device connected)
- Shorted to ground (USB host device connected)
- Connected to ground via resistor (accessory asserted)

If the ACC_ID_DET pin stops floating (falling edge) during POWER-DOWN mode a wake up is triggered.

9.6 System Enable (SYS_EN)

SYS_EN is an input signal from the host processor to DA9053 which initiates enabling the system power supplies. The control SYS_EN will be initialized from OTP if the related port is configured as GPI or GPO. The register bit SYS_EN can be read and changed via the control interfaces. DA9053 will not accept any power mode transition commands until the sequencer has stopped processing IDs. De-asserting SYS_EN informs the DA9053 that the host processor is going into a standby/hibernate mode. When the port is changing from active to passive state there is no IRQ or wake-up event trigger. With the exception of supplies that are configured in ACTIVE mode with a voltage preset before powering down all regulators and buck converters in power domain POWER1, POWER and SYSTEM will be sequentially disabled in reverse order.

9.7 Power Enable (PWR_EN)

PWR_EN is an input signal from the host processor to DA9053 or is configured via OTP or host commands. Initialisation, IRQ assertion and register bit PWR_EN control is similar to SYS_EN. To ensure the correct sequencing SYS_EN has to be active before asserting PWR_EN. When de-asserting SYS_EN the sequencer will sequentially power down POWER1, POWER and SYSTEM domains respectively.

9.8 Power1 Enable (PWR1_EN)

PWR1_EN is an input signal from a host to DA9053 and is configured via OTP or host commands. Initialisation, IRQ assertion and register bit PWR1_EN control is similar to SYS_EN. The domain POWER1 is a sub power domain for general purpose.

9.9 General Purpose Feedback Signal 1 (GP_FB1: EXT_WAKEUP/READY)

The feedback GP_FB1 supports two different modes. If configured as EXT_WAKEUP it is an active high output signal to the host processor that indicates a valid wake-up event during POWER-DOWN mode. External signals that are causing wake-up events are debounced before DA9053 assert the EXT_WAKEUP signal. EXT_WAKEUP is released when entering the ACTIVE mode. If configured as READY signal it indicates ongoing DVC or power sequencer activities. The signal is active low and is asserted from DA9053 as long as the power sequencer processes IDs or DVC voltage transitions are ongoing.

9.10 Power Domain Status (SYS_UP, PWR_UP/GP_FB2)

The power domain status indicators are active high and assigned after the sequencer has processed all IDs of a power domain (all assigned supplies are up). When domains are disabled during power mode transitions the status indicator is released before the DA9053 sequencer processes the last step of a domain.

PWR_UP is one mode of the general purpose indicator GP_FB2 that can also be used as a configurable feedback signal that is level/time controlled from the power sequencer.

9.11 Supply Rail Fault (nVDD_FAULT)

nVDD_FAULT is an active low output signal to the host processor to indicate a VDDOUT low status. The assertion of nVDD_FAULT indicates that the main battery and the supply input voltage is low and therefore informs the host processor that the power will shut down very soon. After that the processor may operate for a limited time from the backup battery, which can provide power to the processor for a few cycles. In the event of nVDD_FAULT assertion the processor may be programmed to enter an emergency mode, for example external memory data refresh is no longer performed.

9.12 Interrupt Request (nIRQ)

The nIRQ is an active low output signal which indicates that an interrupt causing event has occurred and that the event and status information is available in the related registers. Such information can be temperature and voltage of the PMIC, fault conditions, charging status, status changes at GPI ports, and others. The event registers hold information about the events that have occurred. Events are triggered by a status change at the monitored signals. When an event bit is set the nIRQ signal is asserted (unless this interrupt is masked by a bit in the IRQ mask register). The nIRQ will not be released until the event registers have been cleared.

9.13 Real Time Clock Output (OUT_32K)

The OUT_32K is an output signal that generates a buffered signal of the DA9053 32 kHz oscillator. The 32 kHz oscillator will always run on the DA9053 following the initial start-up from NO-POWER mode until the device has reached NO-POWER mode again. The signal output buffer can be disabled during POWER-DOWN mode.

9.14 IO Supply Voltage (VDD_IO1 and VDD_IO2)

VDD_IO1 and VDD_IO2 are two independent IO supply rail inputs of DA9053 that can be individually assigned to the power manager interface, power manager IOs and GPIOs. The rail assignment determines the IO voltage levels and logical thresholds. The selection of the supply rail for GPIOs is also partially used for their alternate functions. GPOs configured in open drain mode have to use the VDD_IO1 rail if an internal pull-up resistor is required.

10 Control Interfaces

The DA9053 is completely software controlled from the host by registers. DA9053 offers two independent serial control interfaces to access these registers. The communication via the main power manager interface is selectable to be either a 2-wire or a 4-wire connection (I^2C or SPI compliant). The alternative interface is fixed towards a 2-wire bus. Data is shifted in to or out from DA9053 under the control of the host processor that also provides the serial clock.

10.1 Power Manager Interface (4-Wire and 2-Wire Control Bus)

This is the dedicated power control interface from the primary host processor. In 4-wire mode the interface uses a chip-select line (nCS/nSS), a clock line (SK), data input (SI) and data output line (SO).

10.2 4-Wire Communication

In 4-wire mode the DA9053 register map is split into two pages with each page containing up to 128 registers. The register at address zero on each page is used as a page control register. The default active page after reset includes registers R1 to R127. Writing to the page control register changes the active page for all subsequent read/write operations. After modifying the active page it is recommended to read back the page control register to ensure that future data exchange is accessing the intended registers.

The 4-wire interface features a half-duplex operation (data can be transmitted and received with in a single 16-bit frame) at enhanced clock speed (up to 14 MHz). It operates at the provided host clock frequencies.

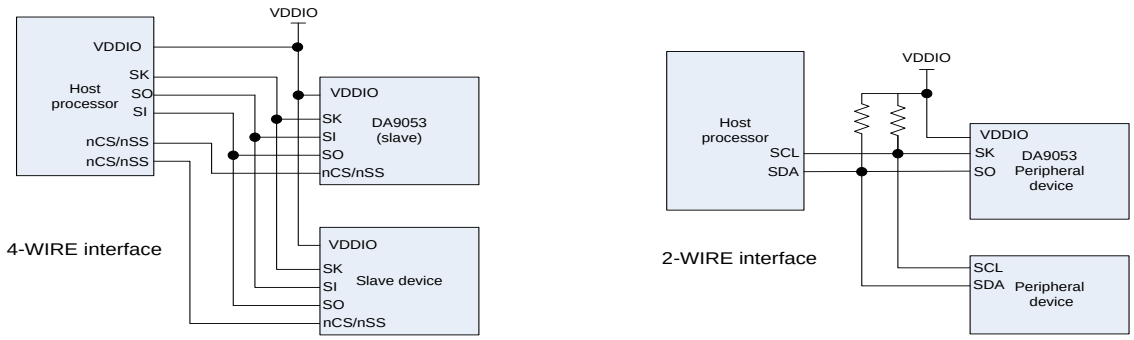

Figure 29: Schematic of a 4-Wire and 2-Wire Power Manager Bus

A transmission begins when initiated by the host. Reading and writing is accomplished by the use of an 8-bit command, which is sent by the host prior to the exchanged 8-bit data. The byte from the host begins shifting in on the SI pin under the control of the serial clock SK provided from the host. The first seven bits specify the register address (0 to 127, decimal) which will be written or read by the host. The register address is automatically decoded after receiving the seventh address bit. The command word ends with an R/W bit, which specifies the direction of the following data exchange. During register writing the host continues sending out data during the following eight SK clocks. For reading the host stops transmitting and the 8-bit register is clocked out of DA9053 during the consecutive eight SK clocks of the frame. Address and data are transmitted with MSB first. nCS resets the interface when inactive and it has to be released between successive cycles.

The SO output from DA9053 is normally in high impedance state and active only during the second half of read cycles. A pull-up or pull-down resistor may be needed at the SO line if a floating logic signal can cause unintended current consumption inside other circuits.

Table 44: 4-Wire Clock Configurations

CPOL Clock Polarity	CPHA Clock Phase	Output Data is Updated at SK Edge	Input Data is Registered at SK Edge
0 (idle low)	0	falling	rising
0 (idle low)	1	rising	falling
1 (idle high)	0	rising	falling
1 (idle high)	1	falling	rising

The DA9053 4-wire interface offers two further configuration bits. Clock polarity (CPOL) and clock phase (CPHA) define when the interface will latch the serial data bits. CPOL determines whether SK idles high (CPOL = 1) or low (CPOL = 0). CPHA determines on which SK edge data is shifted in and out. With CPOL = 0 and CPHA = 0 setting DA9053 latches data on the SK rising edge. If the CPHA is set to 1 the data is latched on the SK falling edge. CPOL and CPHA states allow four different combinations of clock polarity and phase; each setting is incompatible with the other three. The host and DA9053 must be set to the same CPOL and CPHA states to communicate with each other.

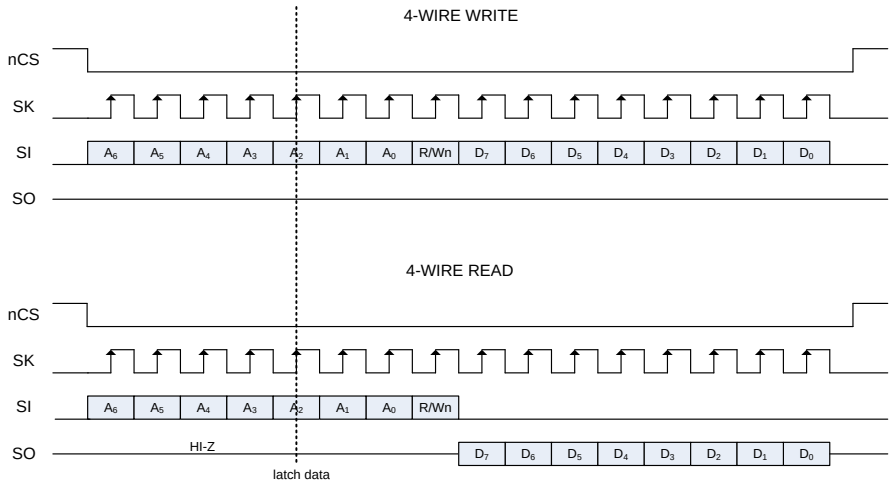

Figure 30: 4-Wire Host Write and Read Timing (nCS_POL = '0', CPOL = '0', CPHA = '0'')

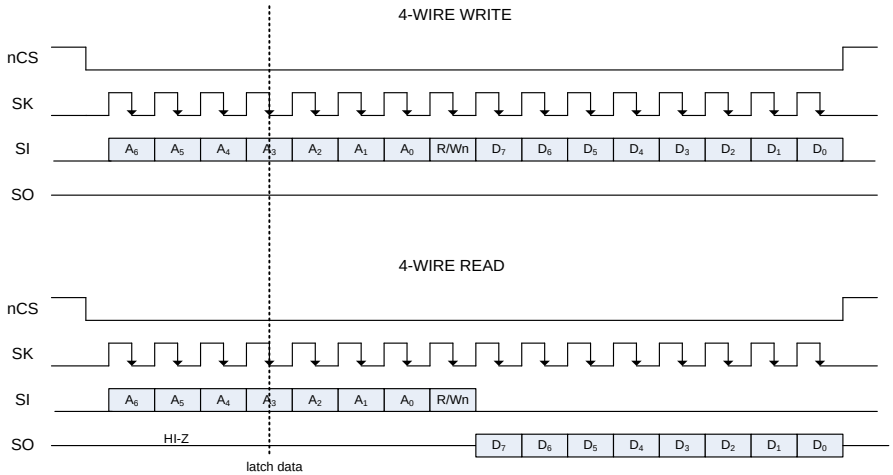

Figure 31: 4-Wire Host Write and Read Timing (nCS_POL = '0', CPOL = '0', CPHA = '1'')

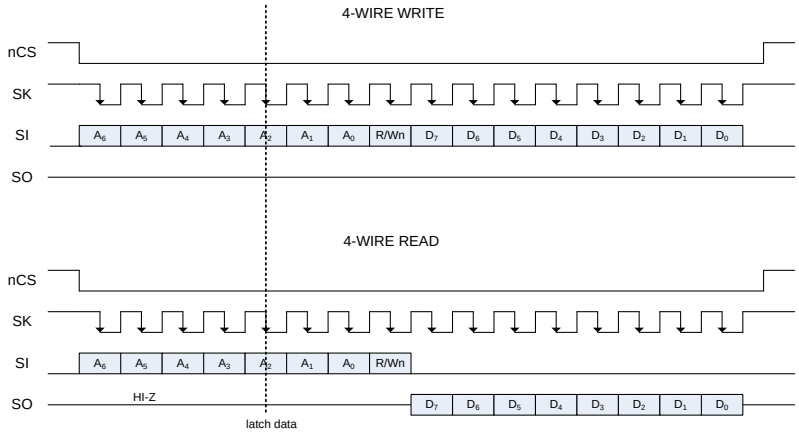

Figure 32: 4-Wire Host Write and Read Timing (nCS_POL = '0', CPOL = '1', CPHA = '0'')

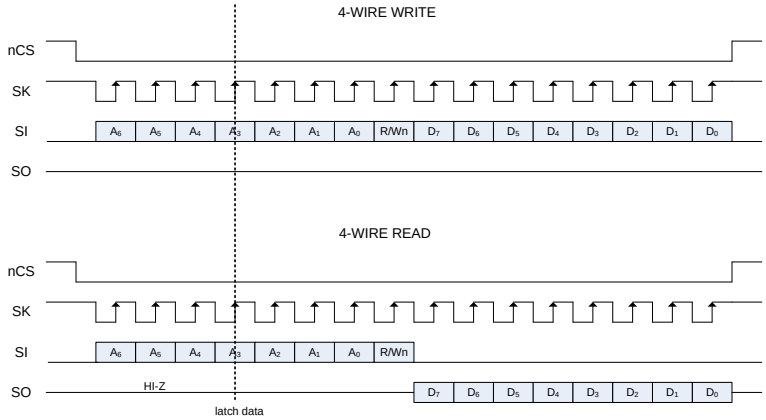

Figure 33: 4-Wire Host Write and Read Timing (nCS_POL = '0', CPOL = '1', CPHA = '1'')

Table 4: 4-Wire Interface Summary

Parameter		
Signal lines	nCS	Chip select
	SI Serial input data	Master out Slave in
	SO Serial output data	Master in Slave out
	SK	Transmission clock
Interface	Push-pull with tristate	
Supply voltage	Selected from VDD_IO1/VDD_IO2	1.6 V to 3.3 V
Data rate	Effective read/write data	Up to 7 Mbps
Transmission	Half-duplex	MSB first
	16-bit cycles	7-bit address, 1-bit read/write, 8-bit data
Configuration	CPOL	Clock polarity
	CPHA	Clock phase
	nCS_POL	nCS is active low/high

NOTE
Reading the same register at high clock rates directly after writing it does not guarantee a correct value. It is recommended to keep a delay of one frame until re-accessing a register that has just been written (for example by writing/reading another register address in between).

10.3 2-Wire Communication

The power manager interface can be configured for a 2-wire serial data exchange. It has a configurable SLAVE write address (default: 0x90) and a configurable SLAVE read address (default: 0x91).

SK provides the 2-wire clock and SO carries all the power manager bidirectional 2-wire data. The 2-wire interface is open-drain supporting multiple devices on a single line. The bus lines have to be pulled HIGH by external pull-up resistors (2 kΩ to 20 kΩ range). The attached devices only drive the bus lines LOW by connecting them to ground. As a result two devices cannot conflict, if they drive the bus simultaneously. In standard/fast mode the highest frequency of the bus is 400 kHz. The exact frequency can be determined by the application and does not have any relation to the DA9053 internal clock signals. DA9053 will follow the host clock speed within the described limitations and does not initiate any clock arbitration or slow down.

In high speed mode the maximum frequency of the bus may be increased towards 1.7 MHz. This mode is supported if the SK line is driven with a push-pull stage from the host and if the host enables an external 3 mA pull-up at the SO pin to decrease the rise time of the data. In this mode the SO line on DA9053 is able to sink up to 12 mA. In all other respects the high speed mode behaves as the standard/fast mode.

Communication on the 2-wire bus always takes place between two devices, one acting as the master and the other as the slave. The DA9053 will only operate as a slave. As opposed to the 4-wire mode the 2-wire interface has direct (linear) access to the whole DA9053 register space (except R0 and R128). This is achieved by using the MSB of the 2-wire 8-bit register address as a selector of the register page (this does not modify the page control register R0/R128 that is accessible only in 4-wire mode).

10.3.1 Details of the 2-Wire Control Bus Protocol

All data is transmitted across the 2-wire bus in groups of 8 bits. To send a bit the SO line is driven towards the independent state while the SK is LOW (a low on SO indicates a zero bit). Once the SO has settled the SK line is brought HIGH and then LOW. This pulse on SK clocks the SO bit into the receiver's shift register.

A two byte serial protocol is used containing one byte for address and one byte data. Data and address transfer is MSB transmitted first for both read and write operations. All transmission begins with the START condition from the master during the bus is in IDLE state (the bus is free). It is initiated by a high to low transition on the SO line while the SK is in the high state (a STOP condition is indicated by a low to high transition on the SO line while the SK is in the high state).

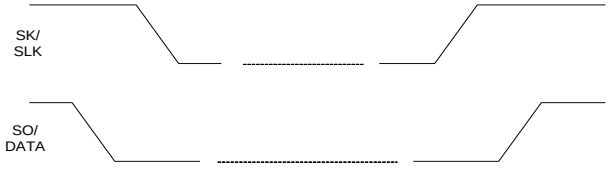

Figure 34: Timing of 2-Wire START and STOP Condition

The 2-wire bus will be monitored by DA9053 for a valid SLAVE address whenever the interface is enabled. It responds immediately when it receives its own slave address. This acknowledge is done by pulling the SO line low during the following clock cycle (white blocks marked with an 'A' in Figure 12 to Figure 16).

The protocol for a register write from master to slave consists of a start condition, a slave address with read/write bit and the 8-bit register address followed by 8 bits of data terminated by a STOP condition (all bytes responded by DA9053 with Acknowledge):

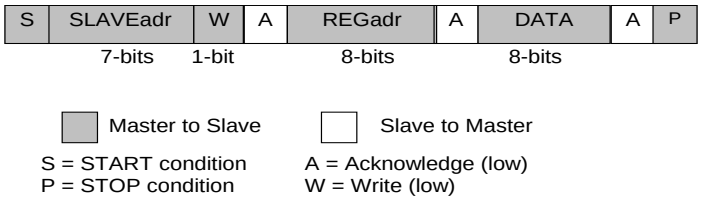

Figure 35: 2-Wire Byte Write (SO/DATA Line)

When the host reads data from a register it first has to write access DA9053 with the target register address and then read access DA9053 with a Repeated START or alternatively a second START condition. After receiving the data the host sends Not acknowledge and terminates the transmission with a STOP condition:

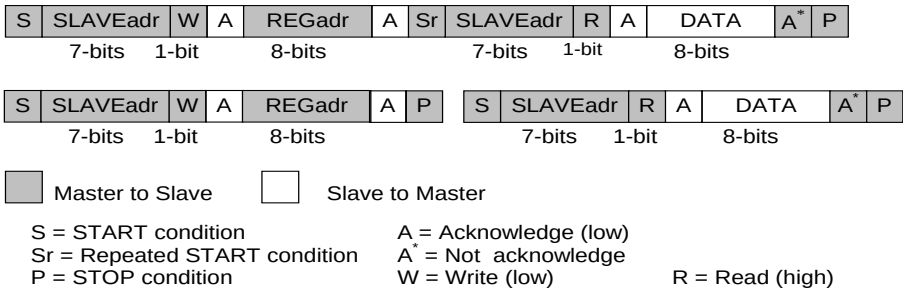

Figure 36: Examples of 2-Wire Byte Read (SO/DATA line)

Consecutive (page) read out mode is initiated from the master by sending an Acknowledge instead of Not acknowledge after receipt of the data word. The 2-wire control block then increments the address pointer to the next 2-wire address and sends the data to the master. This enables an unlimited read of data bytes until the master sends a Not acknowledge directly after the receipt of data, followed by a subsequent STOP condition. If a non-existent 2-wire address is read out then the DA9053 will return code zero:

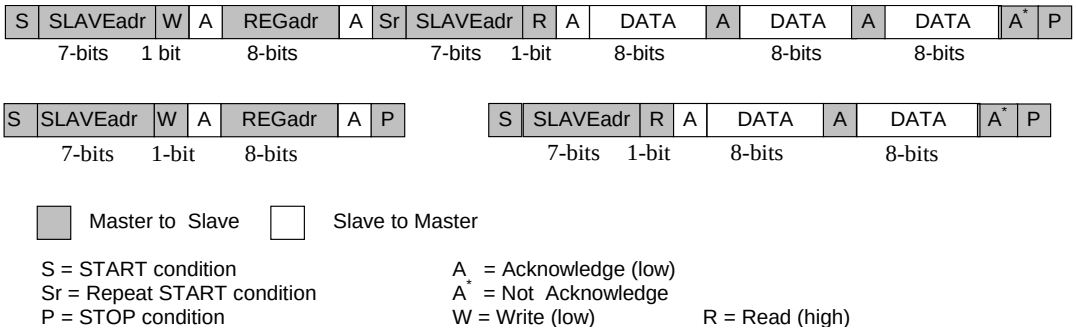

Figure 37: Examples of 2-Wire Page Read (SO/DATA line)

NOTE
The slave address after the Repeated START condition must be the same as the previous slave address.

Consecutive (page) write mode is supported if the master sends several data bytes following a slave register address. The 2-wire control block then increments the address pointer to the next 2-wire address, stores the received data and sends an Acknowledge until the master sends the STOP condition.

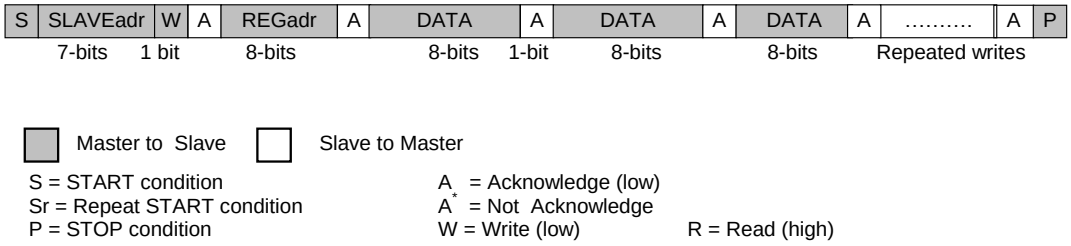

Figure 38: 2-Wire Page Write (SO/DATA line)

An alternate write mode receiving alternated register address and data can be configured to support host repeated write operations that access several but non-consecutive registers. Data will be stored at the previously received register address:

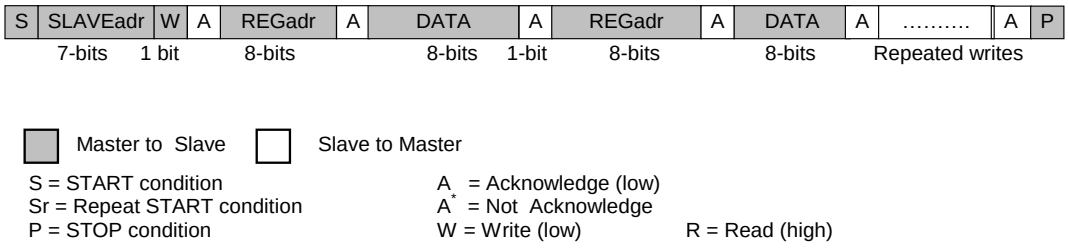

Figure 39: 2-Wire Repeated Write (SO/DATA line)

If a new START or STOP condition occurs within a message, the bus will return to IDLE-mode.

10.4 Alternative High Speed 2-Wire Interface

The high speed 2-wire (HS-2-wire) interface is the alternative serial control bus, which consists of a DATA (data line) and a CLK (clock line). It can be used as an independent control interface for data transactions between DA9053 and a second host processor. The DA9053 high speed 2-wire interface has a configurable 8-bit SLAVE write address (default: 0x92) and a configurable SLAVE read address (default: 0x93).

The interface is enabled if DATA was selected via configuration GPIO14_PIN. The bus lines have to be pulled HIGH by external pull-up resistors (2 kΩ to 20 kΩ range). GPIO15_Type defines the supply rail of the interface (used for input logic levels and the internal pull-up resistors). The controls GPIO15_PIN and GPIO15_ MODE are disabled when the interface is enabled via GPIO14_PIN. Whenever the interface receives a READ or WRITE command that includes a matching slave address it is able to trigger the assertion of a nIRQ including an optional wake-up event (enabled via GPIO14_ MODE).

NOTE
If the nIRQ assertion from interface access is enabled (E_GPI4) it may by masked as long as the HS-2-wire is in use (this nIRQ cannot be cleared via the HS-2_wire interface because every interface access will trigger a re-assertion).

Beside the interface base address and the optional wake-up, the characteristics of the HS-2-wire interface are identical to the power manager 2-wire interface (see 10.3.1 Details of the 2-Wire Control Bus Protocol).

11 Operating Modes

11.1 ACTIVE Mode

DA9053 enters ACTIVE mode after the host processor has performed at least one initial 'alive' watchdog write (or alternatively an initial assertion of the KEEP_ACT pin) within the target time window (this watchdog condition can be disabled).

A running application is typically in ACTIVE mode. In this mode the PMIC core functions (for example LDOCORE, BCD counter, internal oscillator) as well as a supplies for features like battery charger and GP-ADC are enabled. In ACTIVE mode the host processor can take over the control of the automatic battery charging block if necessary and is able to respond to any faults that have been detected. Status information can be read from the host processor via the power manager bus and the DA9053 can flag interrupt requests to the host via a dedicated interrupt port (nIRQ). Temperature and voltages inside and outside the DA9053 can be monitored and any fault conditions flagged to the host processor.

11.2 POWER-DOWN Mode

DA9053 is in POWER-DOWN mode whenever the power domain SYSTEM is disabled (even partially). This can be achieved when progressing from RESET mode or by returning from ACTIVE mode. A return from ACTIVE mode is initiated by low-power mode instructions from the host or happens as an interim state during an application shutdown to RESET mode.

During POWER-DOWN mode the LDOCORE, the band-gap, the nONKEY and the BCD counter are active. In addition GPIO-ports, the GP-ADC, battery charger and the control interfaces keep on running if not disabled. Also dedicated power supplies can be enabled in POWER-DOWN mode if power down voltages have been pre-configured during ACTIVE mode. The internal oscillator (2 MHz) will only run on demand (for example for a running GP-ADC or bucks that are enabled and are not forced to PFM mode). The application supervision by WATCHDOG timer is discontinued in POWER-DOWN mode. The digital control logic of disabled features of DA9053 (regulators, bucks, chargers, boosts, GP-ADC, and others) will be disconnected from the clock tree via clock gating, so that the device offers an optimized dissipation power in POWER-DOWN mode.

Following the next Wake-up event all supplies are re-configured with their default voltage values from OTP and the sequencer timers are set to their default OTP values. If the POWER-DOWN mode was caused by releasing SYS_EN the sequencer pointer is located at position 0 this allows default enabling/disabling of supplies (beside LDOCORE).

11.3 RESET Mode

DA9053 is in RESET mode whenever a complete application reset is required. The RESET mode happens after cold start when progressing from NO-POWER mode or can be forced by the user via a pressed reset switch that is connected to port nSHUTDOWN, a long press of nONKEY (if its RESET feature was enabled) or a long parallel assertion of GPIO14 and GPIO15 (if this RESET feature was enabled), from the host processor by asserting port nSHUTDOWN or via an error detection from DA9053.

DA9053 error conditions that force a RESET mode:

- A watchdog write from the host outside of the watchdog time window (if watchdog was enabled)
- An under-voltage detected at VDDOUT ($V_{DDOUT} < V_{DD\_FAULT\_LOWER}$)
- An internal die over-temperature detected
- An over voltage or over current at the boost

In order to allow the host to determine the reason for the RESET a FAULTLOG register records the cause.

When returning from POWER-DOWN mode the RESET mode will be achieved after powering down domain SYSTEM completely and continue towards a state with absolute minimum current consumption, with the only active circuits being LDOCORE, the BCD counter, the band gap and the VDD_REF, VBUS, DCIN, ACC_ID_DET and VDDOUT comparators. Beside supplies (controlled by the power sequencer) and the backup battery charger, other blocks on DA9053 (for example the backlight boost) are automatically disabled to avoid draining the battery. During DA9053 RESET mode the host processor can be held in a RESET state via port nRESET that is always asserted to low when DA9053 progresses from RESET mode (for example after cold start from NO-POWER mode) and can be asserted (depending on configuration of sequencer step 0) when the sequencer has finished powering down domain SYSTEM (even partially) .

Some RESET conditions like the SHUTDOWN via register bit, WATCHDOG error, or over-temperature, will automatically expire. Other conditions like asserting the port nSHUTDOWN need to be released to enable a progression from RESET to POWER-DOWN mode. If the RESET was initiated by the user a 500 ms time out will be inserted before trying to power up again. When the RESET condition has disappeared DA9053 requires either a connected good main battery (V_{DDOUT} > $V_{DD\_FAULT\_UPPER}$) or a detected supply (VBUS/DCIN > VCH_THR) that is able to provide enough power to VDDOUT (V_{DDOUT} > V_{DDOUT_MIN}) to start up to POWER-DOWN mode.

11.4 NO-POWER Mode

DA9053 will enter the NO-POWER mode when the internal supply rail V_{DD_REF} drops below V_{POR_LOWER} (for example during continued discharge of main and backup battery). As long as V_{DD_REF} is now lower than V_{POR_UPPER} the core supply LDOCORE, the 32K oscillator and the BCD counter are switched off, an internal power-on-reset (nPOR) is asserted and only the VDD_REF comparator is active and checks for a condition that allows DA9053 to turn on again. When DA9053 detects either a good main battery or a connected supply charger which raises V_{DD_REF} > V_{POR_UPPER} it will reset the BCD counter and progress to RESET mode.

11.5 Power Commander Mode

This is a special mode for evaluation and configuration. In power commander mode DA9053 is configured to load the control register default values from the HS 2-wire interface instead of from the OTP cells so that unprogrammed DA9053 samples will power up and allow a PC running power commander software to load all the configuration registers.

Power commander mode is enabled by connecting TP to VDDCORE.

In RESET mode DA9053 will do an initial OTP read to setup the trim values. However, if the OTP values loaded into these registers are not as required they can be updated during the subsequent power commander programming sequences.

NOTE
In power commander mode GPI14/15 will be configured for HS-2-wire interface operation (with VDDCORE as the supply) and GPO13 will be configured as an output for nVDD_FAULT. Any register writes or OTP loads which can change this configuration are ignored until DA9053 has exited from power commander mode.

After the initial OTP read has completed DA9053 informs the system that it is waiting for a programming sequence by driving nVDD_FAULT low. The software running on the PC monitors nVDD_FAULT and responds by downloading the values into the configuration registers within DA9053. nVDD_FAULT is automatically released after the release register is loaded.

There are two programming sequences performed in power commander mode. The first takes place between RESET and POWER-DOWN mode and the second takes place between POWER-DOWN and SYSTEM mode. Two release registers are used support these two programming sequences:

- A write to register R106 will end the first programming sequence
- A write to register R61 will end the second programming sequence

During these programming sequences any registers can be written to in any order, but the sequence will terminate after the appropriate release register has been written to.

NOTE
To correctly configure DA9053 registers, R10 to R105 should be programmed during the first sequence and FAULT LOG register (R9) bit VDD_FAULT has to be cleared by writing a '1'. Registers R14 and R43 to R61 should be programmed during the second sequence.

The host can determine whether DA9053 is in the first or second programming sequence by reading the FAULT LOG register. If a read of the FAULT LOG register bit VDD_FAULT returns a zero, then the DA9053 is in the second programming sequence otherwise it is in the first.

After the first programming sequence has been completed DA9053 will be in POWER-DOWN mode. Progression from this mode is determined by the values programmed for SYS_EN and AUTO_BOOT. If DA9053 has been directed to progress from POWER-DOWN mode then it will drive pin nVDD_FAULT low for a second time to request that the SW performs the second programming sequence.

Once the second programming sequence has completed the progress of the power-up sequence will be controlled by the values loaded during the programming sequence.

The programmed configuration can be identified by reading the fuse register CONFIG_ID.

NOTE
During power commander mode the fault detection status bit VDD_FAULT and the level at the related pin nVDD-FAULT do not match and does not indicate a low voltage level at VDDOUT. An enabled shutdown from the 5 s assertion of GPIO14/15 will be ignored during power commander mode.

11.6 Start-Up from NO-POWER Mode

11.6.1 Power-On-Reset (nPOR)

To guarantee the correct start-up of DA9053 an internal power-on-reset nPOR (active low) is generated for the initial connection of either a supply or a good battery following a phase of not being supplied with sufficient power. To allow DA9053 to start up, even if the main battery is completely discharged, an internal VDD_REF rail is used to supply the charger blocks, comparators and the control logic. If no charger is present VDD_REF is switched to either the main battery or the backup battery, whichever provides the higher voltage level. If the backup battery was connected to the application before main power, DA9053 remains off and draws no current. This allows the application to wait for its initial activation without discharging the backup battery.

While $V_{DDCORE} < V_{POR\_UPPER}$ the internal nPOR is asserted and DA9053 will not switch on (NO-POWER mode). When V_{DDCORE} rises above V_{POR_UPPER} the nPOR is negated, LDOCORE is switched on, the BCD counter and FAULT_LOG register are reset and DA9053 progresses to RESET mode.

When an external charger is detected (rising edge on DCIN_DET or VBUS_DET) having no, or only a deep discharged, main battery connected to DA9053 the internal charger, oscillator and band-gap are enabled and the whole OTP trim block is read and stored to the register bank. If the supply voltage is below the charger detection threshold (VCH_THR) after a debouncing period of Tdelay (10 ms, to allow for de-bouncing of the input signal and the band-gap reference to settle) the device returns to RESET mode.

If the external charger is still present and the CHG_ATT comparator flags a minimum of 100 mV head room from charger input VCENTER to VDDOUT DA9053 starts up the charger buck to supply VDDOUT at the default current limit (loaded from OTP) and starts supplying power to VDDOUT, which enables an application start-up also with a flat battery. When V_{DDOUT} rises above V_{DDOUT_MIN} DA9053 enters the POWER-DOWN mode. If this does not happen within 128 ms it will return to RESET mode.

From POWER-DOWN mode DA9053 will continue with powering up supplies if the power domain SYSTEM was asserted via input port (or set via OTP settings) and AUTO_BOOT was enabled (or a valid Wake-event has happened). The simplified flow diagram,(Figure 40), shows the start-up events and an example of a typical initial sequence. If DA9053 causes a RESET from an under voltage detected within 10 s after releasing nRESET (the start-up initiating supply is not strong enough to supply the application) DA9053 will assert VDD_START inside the FAULTLOG register and temporally disable AUTO_BOOT for the consecutive start-up (enabling only the battery charger and start waiting for a valid wake-up event). Only events generated from user inputs (GPIs or nONKEY) trigger a wake-up during this emergency charging, however a flashing LED connected to GPIO 11 or 11 can be automatically enabled via control BLINK_FRQ. AUTO_BOOT is set back to its default value when the battery voltage V_{BAT} > VCHG_BAT- VCHG_DROP.

A similar start-up to POWER-DOWN mode will be performed when a pre-charged battery was inserted ($V_{DDOUT}>V_{DD\_FAULT\_UPPER}$) following a state where DA9053 has not been provided with any supply voltage as shown inFigure 40.

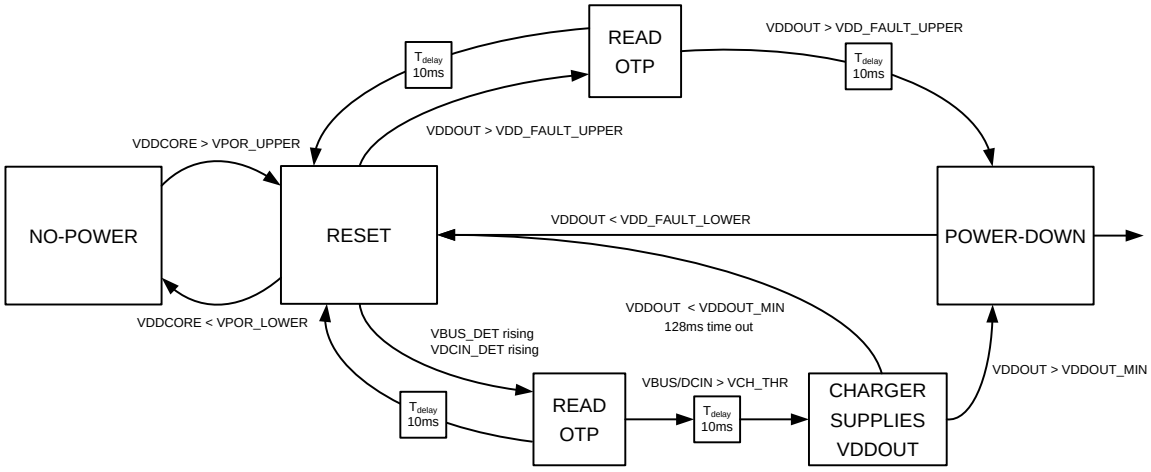

Figure 40: Start-Up from NO-POWER to POWER-DOWN Mode

11.7 Application Wake-Up

A valid wake-up event (for example nONKEY, SYS_EN, RTC-Alarm or a trigger from GPIOs) initiates an application power up from POWER-DOWN mode. The wake-up from GPIOs (or selected alternative features, that use a shared GPI event) has to be enabled via GPIx_MODE and can be masked in addition with the related nIRQ mask. After a wake-up condition is detected the OTP trim block for all supplies and the sequencer timer is read (R14 and R43-R61). The values (re-)configure the supplies and the sequencer timer. If the POWER-DOWN mode was reached by progressing from RESET mode the power sequencer can also be started without waiting for a wake-up event if AUTO_BOOT was asserted.

DA9053 will assert the EXT_WAKEUP signal toward the host processor and if the power domains are not pre-enabled by OTP the host processor has to control the further application start-up (for example via the power domain enable lines). Alternatively DA9053 continues stand-alone powering up the OTP enabled domains via the power domain sequencer. By that a start-up from RESET mode powers up the application automatically only if SYS_EN is asserted from the host processor or was default set from OTP.

Continuation into ACTIVE mode requires an assertion of PWR_EN (from the host via port PWR_EN, register write or enabled from OTP). After starting the WATCHDOG timer the host processor has the configured time window to assert the WATCHDOG timer via the power manager bus (if Watchdog is enabled). If this does not happen the state-machine will terminate the ACTIVE mode at the end of the time window and return to the RESET mode.

11.8 System Monitor (Watchdog)

After powering up domain POWER, DA9053 can initiate an initial watchdog monitor function (if this feature is enabled via control TWDSCALE). If the WATCHDOG is enabled the host processor has to write logic ‘1’ within a configured time (TWDMAX) to bit WATCHDOG in DA9053 register R17 to indicate that it is ‘alive’ after PWR_UP was asserted. If the host does not write ‘1’ to the WATCHDOG bit within the TWDMAX time DA9053 will assert TWD_ERROR in the FAULT_LOG register and power down to RESET mode.

After this first write to the WATCHDOG bit the host must write again to the WATCHDOG bit within a configured time window or DA9053 will assert TWD_ERROR in the FAULT_LOG register and power down to RESET mode. The WATCHDOG error condition is cleared when entering the RESET mode. The time window has a minimum time TWDMIN fixed at 256 ms and a maximum time TWDMAX of nominally 2.048 s. The TWDMAX value can be extended by multiplying the nominal TWDMAX by the

register bits TWDSCALE. TWDSCALE is used to extend the TWDMAX time by x1, x2, x4, x8, x16, x32 or x64.

Changing the maximum value of the time window (TWDMAX) or the state of KEEPACT_EN bit requires TWDSCALE to be zero (WATCHDOG is disabled) for a minimum of 100 µs. This requires the host to first switch off the WATCHDOG for at least 150 µs before configuring it with a new timing window scale value (TWDSCALE).

The WATCHDOG bit can also be asserted from the host via hardware by asserting KEEP_ACT. This mode is selected via control KEEPACT_EN, which disables the control of the WATCHDOG bit via the host control interface. The (in time) assertion of nONKEY will then also enable DA9053 to transfer into ACTIVE mode.

Once in the ACTIVE state DA9053 will continue to monitor the system unless it is disabled via setting TWDSCALE to zero. If the WATCHDOG register bit is set to a '1' within the time window the watchdog monitor resets the timer, sets the WATCHDOG bit back to zero (bit is always read as zero) and waits for the next watchdog signal.

11.9 Wake-Up Events

Table 45: Wake-Up Events

Signal / Condition	Wake-up	User event	System event	IRQ
Charger attach: E_DCIN_DET	X		X	X
Charger attach: E_VBUS_DET	X		X	X
Charger removal: E_DCIN_REM	X		X	X
Charger removal: E_VBUS_REM	X		X	X
VDDOUT low pre-warning: E_VDD_LOW	X		X	X
RTC alarm: E_ALARM	X		X	X
Sequencing finished: E_SEQ_RDY			X	X
Voltage comparator: E_COMP_1V2	X		X	X
Pressed On-key: E_nONKEY	X	X		X
Accessory and USB ID detect (ID_FLOAT falling edge)	X		X	X
Accessory and USB ID detect (ID_FLOAT rising edge)			X	X
End of battery charging: E_CHG_END	X		X	X
Battery temperature: E_TBAT			X	X
Manual ADC result ready: E_ADC_EOM			X	X
Pen down detection from TSI: E_PEN_DOWN	X	X		X
Measurement ready from TSI: E_TSI_READY			X	X
GPIOs: E_GPIx	X	X		X
ADC 4, 5, 6 threshold: via GPI0, 1, 2	X		X	X
SYS_EN, PWR_EN, PWR1_EN (passive to active transition): via GPIO8, 9, 10	X		X	X
HS-2-wire interface: via GPIO14	X		X	X

Power Supply Sequencer

The start-up of DA9053 supplies is performed with a sequencer that contains a programmable step timer, a variable ID array of time slot pointers and four predefined pointers (SYSTEM_END, POWER_END, MAX_COUNT and PART_DOWN). The sequencer is able to control up to 22 IDs (4 buck converter, 2 rail switches VPERI_SW_EN / VMEM_SW_EN, 10 LDOs, 4 feedback pin level controls, a Wait ID (GPI10) and a POWER-DOWN register), which can be grouped in three power domains. The power domains have configurable size and their borders are described by the location pointers SYSTEM_END, POWER_END and MAX_COUNT.

The lowest level power domain SYSTEM starts at step 1 and ends at the step that is described by the location pointer SYSTEM_END. The second level domain POWER starts at the successive step and ends at POWER_END. The third level domain POWER1 starts at the consecutive step and ends at MAX_COUNT. The values of pointer SYSTEM_END, POWER_END and MAX_COUNT are predefined in OTP registers. and should be configured to be SYSTEM_END < POWER_END < MAX_COUNT.

The domain SYSTEM by can be understood as a basic set of supplies that are mandatory to keep the application at least inside a standby/hibernate mode. If enabled via control OTPREAD_EN all supplies of DA9053 and the sequencer timer (registers R14 and R43-R61) are configured with the default value from OTP before powering up the domain SYSTEM. This will cause a reconfiguration of all supplies that have been powered down with a preset voltage level. The second level domain POWER includes supplies that are required in addition to get the application 'alive' and set DA9053 in to ACTIVE mode. POWER1 can be understood as a sub domain of POWER that can be used for additional hardware/software initiated control of supply blocks during ACTIVE mode (for example for a sub-application like WLAN or GSM baseband). Supplies in domain POWER and POWER1 can be voltage preconfigured and after that sequentially changed during powering down, but will not be reset to their default values from OTP unless there is a power-up from domain SYSTEM.

NOTE
Running applications should be configured to ACTIVE mode (domain POWER is up) and pointer POWER_END has to be at least one time slot higher than SYSTEM_END.

All buck converter and 10 LDOs of DA9053 have received a unique sequencer ID. The power-up sequence is then defined by an OTP register bank that contains a series of supplies (and other features), which are pointing towards a sequencer time slot. Several supplies can point in to the same time slot and by that will be enabled by the sequencer in parallel. Time slots that have no IDs pointing towards it are dummy steps that do nothing but insert a configurable time delay (marked as 'D' in Figure 42). Supplies that are not pointing towards a sequencer time slot (with a step number greater than zero and less than MAX_COUNT) will not be enabled by the power sequencer and have to be controlled individually by the host (via the power manager bus).

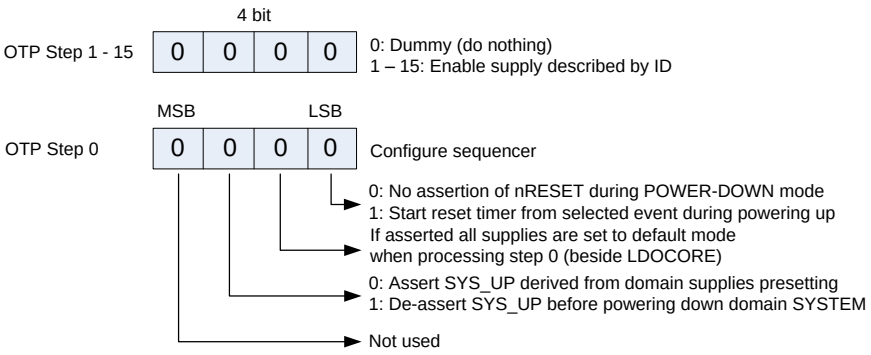

Figure 41: Content of OTP Power Sequencer Register Cell

During powering up the sequencer will start at step 0 where the sequencer behaviour is configured. If DEF_SUPPLY is asserted this includes an optional enabling of supplies (depending on the OTP default settings of the supplies). If SYS_EN was asserted via port or OTP, the sequencer will assert the READY signal (if selected for the feedback pin) and continue with step 1 (this enables all supplies (features) from the OTP register bank that are pointing towards step 1) The sequencer will progress until it has reached the position of pointer SYSTEM_END. Once all supplies of the first power domain SYSTEM are enabled, DA9053 will assert the output signal SYS_UP, release the READY signal and assert the E_SEQ_RDY interrupt.

NOTE
It is recommended that supplies having an asserted enable bit in the OTP are not controlled via IDs of the power sequencer if DEF_SUPPLY is asserted (IDs of these supplies should point into time slot 0).

Table 46: Power Sequencer Controlled Actions

Action	Sequencer Time Slot
Step 0: Configure power sequencer	ID_0
LDO1_EN	LDO1_STEP
LDO2_EN	LDO2_STEP
LDO3_EN	LDO3_STEP
LDO4_EN	LDO4_STEP
LDO5_EN	LDO5_STEP
LDO6_EN	LDO6_STEP
LDO7_EN	LDO7_STEP
LDO8_EN	LDO8_STEP
LDO9_EN	LDO9_STEP
LDO10_EN	LDO10_STEP
PD_DIS	PD_DIS_STEP
VPERI_SW_EN	VPERI_SW_STEP
VMEM_SW_EN	VMEM_SW_STEP
BCORE_EN	BUCKCORE_STEP
BPRO_EN	BUCKPRO_STEP
BMEM_EN	BUCKMEM_STEP
BPERI_EN	BUCKPERI_STEP
Assert/Release GP_FB2	GP_RISE1_STEP
Assert/Release GP_FB2	GP_RISE2_STEP
Release/Assert GP_FB2	GP_FALL1_STEP
Release/Assert GP_FB2	GP_FALL2_STEP
Wait for active state at GPI 10	WAIT_STEP

NOTE
IDs not controlled by the sequencer (or enabled via DEF_SUPPLY in step 0) should point into step 0.

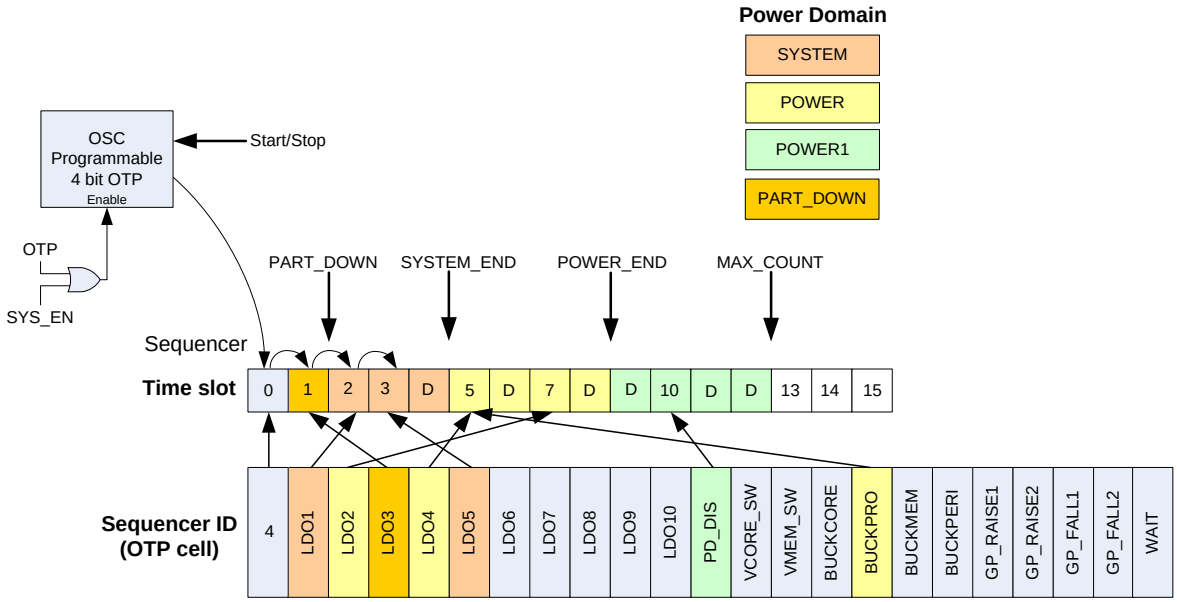

Figure 42: Allocation of Supplies (IDs) to the Sequencer Time Slots

To continue, the sequencer checks for PWR_EN to be asserted (via PWR_EN port, register write or OTP). When this is available the feedback signal READY will be asserted and supplies of domain POWER will be enabled sequentially. The sequencer stops at step POWER_END, releases the READY signal, asserts PWR_UP, assert the E_SEQ_RDY interrupt, enables the initial WATCHDOG timer and waits for an 'alive' feedback from the host processor which starts the ACTIVE mode of DA9053 and releases an asserted EXT_WAKEUP signal.

A third power domain POWER1 can be enabled from PWR1_EN (asserted via PWR1_EN port, register write or OTP). It will enable all consecutive supplies until step MAX_COUNT has been reached, assert PWR1_UP and assert the E_SEQ_RDY interrupt. The READY signal will be asserted as long as IDs are processed (if enabled). The domain POWER1 offers no dedicated status indicator, but the end of its power-up sequence can be selected to start the RESET timer.

The delay between the steps of a sequence is controlled via a 4-bit OTP programmable timer unit SEQ_TIME with a default delay of 1285 µs per step (min. 32 µs and max. 816 ms). The delay time between individual supplies can be extended by leaving consecutive steps with no IDs pointing to it (Dummy supply), which provides an independent delay configured via control SEQ_DUMMY. The delay timers are configured with their default values from OTP (R43) every time before powering up inside domain SYSTEM.

NOTE
During entering and leaving a power domain a 32 µs delay will always be inserted.

When DA9053 is powering down the sequencer will disable the supplies in reverse order and timing. Supplies that are configured with a preset value (LDOx_CONF or BUCKxxx_CONF bit is set) will not be disabled but configured with its preset voltage when the related time slot/ID is processed. If a domain contains at least one supply with an assigned preset, the power domain status indicator (PWR1_UP, PWR_UP and SYS_UP) will not be released. Otherwise the indicator will be released before the first supply of a power domain will be disabled (a de-assertion of SYS_UP can be forced via step 0 configuration). If powering down was initiated from releasing PWR_EN1 the sequencer will stop to modify supplies when the domain pointer POWER_END was reached. If PWR_EN was disabled the domain POWER1 will be powered down followed by POWER until the sequencer reaches pointer SYSTEM_END. If SYS_EN was disabled the sequencer will process all IDs lower than the actual pointer position down to step 0. If the low-power mode was initiated by asserting the control register DEEP_SLEEP the sequencer will first power down POWER1 and POWER continue

with SYSTEM and stop when pointer PART_DOWN has been reached (PART_DOWN has to point into domain SYSTEM). If SYS_EN was disabled the sequencer will process all IDs lower than the actual pointer position down to step 0 (ignoring the PART_DOWN pointer). The sequencer asserts the E_SEQ_RDY interrupt whenever reaching the target pointer position. During processing step 0 all supplies (beside LDOCORE) can be set to their OTP default state (if bit DEF_SUPPLY of step 0 is asserted), but the voltage levels are unchanged. Because of adding rush currents on the battery it is not recommended to default enable more than a single supply at step 0. Asserting control register bit SHUTDOWN will first power down to step 0 and then forces DA9053 to RESET mode. DA9053 features, for example, the 32K output buffer or an Auto ADC measurement can be disabled temporarily in POWER-DOWN mode via register PD_DIS. The timing for processing PD_DIS can be defined by the placement of PD_DIS inside the sequence. The temporally disable will be discontinued Features asserted in PD_DIS are enabled when PD_DIS is processed during a the next power-up sequence. If the READY signal is enabled, it will be asserted during processing the IDs for powering down.

NOTE
Any reconfiguration of supplies from the host in ACTIVE mode will not affect the domain status indicators (SYS_UP, and PWR_UP) and by that has to be performed carefully. The sequencer will later only check for supplies with an assigned preset configuration bit; others will keep their actual voltage level unchanged during power mode transitions. Powering up from domain SYS_EN will configure all supplies and the sequencer timer with the default values from OTP (R14 and R43-R61). During sequencing (indicated from DA9053 via signal READY or the E_SEQ_RDY interrupt) the host is not allowed to send additional power mode transition requests (via power manger interface or power domain enable lines).

A conditional mode transition can be achieved using ID WAIT_STEP. If pointing into the sequence the progress of an initiated mode transition can be synchronized, for example with the state of a host, that is indicated via a signal connected to GPI10. Via GPIO10_ MODE a security time-out of 500 ms can be selected, that will trigger a power down to RESET mode (including the assertion of WAIT_SHUT inside register FAULT_LOG) if E_GPI10 was not asserted until then.

NOTE
In the case of a shutdown sequence towards RESET mode (or power-down from fault condition) any waiting from ID WAIT_STEP will be skipped.

When powering up from NO_POWER mode ID WAIT_STEP can alternatively be used as a configurable delay to allow the 32K oscillator to stabilize before the TTL signal is provided at the 32K output pin (see register WAIT_CONT).

The configuration at sequencer step 0 (nRES_MODE) enables the assertion of nRESET at the end of a power down sequence and starting the reset timer during the consecutive powering up. This is also true for partial POWER-DOWN mode, when the sequencer powers down to pointer position PART_DOWN. The reset timer will start to run from the selected event RESET_EVENT and release the nRESET port after the reset timer has expired (see also description for powering up from NO-POWER/RESET mode).

NOTE
By connecting TP to VDDCORE DA9053 can be configured to load control register default values from the HS 2-wire interface instead of from the OTP cells. During start-up the power sequencer will then assert pin nVDD_FAULT (set to zero) and wait until an external device has loaded default values into the control registers R10 to R106 after RESET MODE (if VDD_FAULT is asserted), R14 and R43 to R61 when leaving POWER-DOWN mode (if VDD_FAULT is not asserted), via HS 2-wire interface. The host has to clear the FAULT_LOG register after loading R10 to R106. When the last register has been loaded nVDD_FAULT will be released and the start-up sequence is continued. During this mode the settings of GPI14 and 15 will be ignored (pins are assigned as 2-wire interface supplied from VDDCORE).

System Monitor (Watchdog)

After powering up domain POWER DA9053 can initiate an initial Watchdog monitor function (if this feature is enabled via control TWDSCALE). If the Watchdog function is enabled the host processor has to write logic '1' within a configured TWDMAX time to bit WATCHDOG in DA9053 register R17 to indicate that it is 'alive' after PWR_UP was asserted. If the host does not write '1' to the WATCHDOG bit within the TWDMAX time DA9053 will assert TWD_ERROR in the FAULT_LOG register and power down to RESET mode.

After this first write to the WATCHDOG bit the host must write again to the WATCHDOG bit within a configured time window or DA9053 will assert TWD_ERROR in the FAULT_LOG register and power down to RESET mode. The WATCHDOG error condition is cleared when entering the RESET mode. The time window has a minimum time TWDMIN fixed at 256 ms and a maximum time TWDMAX of nominally 2.048 s. The TWDMAX value can be extended by multiplying the nominal TWDMAX by the register bits TWDSCALE. TWDSCALE is used to extend the TWDMAX time by x1, x2, x4, x8, x16, x32 or x64.

Changing the maximum value of the time window or the state of the KEEPACT_EN bit requires TWDSCALE to be zero (WATCHDOG is disabled) for a minimum of 100 µs. This requires the host to first switch off the WATCHDOG for at least 150 µs before configuring it with a new timing window scale value (TWDSCALE).

The WATCHDOG bit can also be asserted from the host via hardware by asserting KEEP_ACT. This mode is selected via control KEEPACT_EN, which disables the control of the WATCHDOG bit via the host control interface. The in time assertion of nONKEY will then also enable DA9053 to transfer into ACTIVE mode.

Once in the ACTIVE state DA9053 will continue to monitor the system unless it is disabled via setting TWDSCALE to zero. If the WATCHDOG register bit is set to a '1' within the time window the Watchdog monitor resets the timer, sets the WATCHDOG bit back to zero (bit is always read as zero) and waits for the next Watchdog signal.

12 Register Page Control

Table 47: Register Page 0

Register Address	Bit	Type	Label	Description
R00 PAGE_CON_P0	6:0	R		Reserved
	7	RW	REG_PAGE	0: Selects Register R1 to R127 1: Selects Register R129 to R255

12.1 Power Manager Control and Monitoring

The STATUS register reports the current value of the various signals at the time that it is read out.

NOTE
All the status bits have the same polarity as their corresponding signals.

Register bits in blue are loaded from OTP.

Register Address	Bit	Type	Label	Description
R01 STATUS_A	0	R	nONKEY	Current nONKEY state
	1	R	ID_FLOAT	Current ID_FLOAT detector value
	2	R	ID_GND	Current ID_GND detector value
	3	R	DCIN_DET	0: DCIN voltage not detected (@ DCIN pin) 1: DCIN voltage detected
	4	R	VBUS_DET	0: VBUS voltage not detected (@ VBUS pin) 1: VBUS voltage detected
	5	R	DCIN_SEL	0: No valid charger at DCIN (over voltage) 1: DCIN charger selected
	6	R	VBUS_SEL	0: No valid charger at VBUS (over voltage) or DCIN charger received priority 1: VBUS charger selected
	7	R	VDAT_DET	0: USB host/hub detected (100 mA) 1: Dedicated or host/hub charger detected

Register Address	Bit	Type	Label	Description
R02 STATUS_B	0	R	CHG_ATT	0: No charger attached (drop from VCENTER to VDDOUT < 100 mV) 1: Charger attached (drop from VCENTER to VDDOUT > 100 mV)
	1	R	CHG_PRE	Charging mode when CHG_END is not asserted 0: Charger is in fast CC/CV mode 1: Charger is in pre-charge mode
	2	R	CHG_LIM	0: Charging as configured

Register Address	Bit	Type	Label	Description
				1: Charge current in constant current mode reduced to less than ICHG_THD
	3	R	CHG_END	0: Battery charging 1: Battery charging completed cleared automatically when starting charging/re-charging
	4	R	CHG_TO	0: Battery charging timer OK or disabled 1: Battery charging timeout caused charging finished cleared automatically when starting charging/re-charging and when loading TCTR
	5	R	GP_FB2	Status of GP_FP2 pin: configured from power sequencer
	6	R	SEQUENCING	0: Sequencer is idle 1: Sequencer is processing IDs
	7	R	COMP_DET	0: Comparator at ADCIN5 (1.2 V) not asserted 1: Comparator asserted

Register Address	Bit	Type	Label	Description
R03 STATUS_C	0	R	GPI0	GPI0 level or ADCIN4 threshold indicator (‘1’ when overriding high limit)
	1	R	GPI1	GPI1 level or ADCIN5 threshold indicator (‘1’ when overriding high limit)
	2	R	GPI2	GPI2 level or ADCIN6 threshold indicator (‘1’ when overriding high limit)
	3	R	GPI3	GPI3 level
	4	R	GPI4	GPI4 level
	5	R	GPI5	GPI5 level
	6	R	GPI6	GPI6 level
	7	R	GPI7	GPI7 level

Register Address	Bit	Type	Label	Description
R04 STATUS_D	0	R	GPI8	GPI8/SYS_EN level
	1	R	GPI9	GPI9/PWR_EN level
	2	R	GPI10	GPI10/PWR1_EN level
	3	R	GPI11	GPI11 level
	4	R	GPI12	GPI12/EXT_WAKEUP/READY level
	5	R	GPI13	GPI13 level

	6	R	GPI14	GPI14 level
	7	R	GPI15	GPI15 level

The EVENT registers hold information about events that have occurred in DA9053. Events are triggered by a change in the status registers that contains the status of monitored signals. When an EVENT bit is set in the event register the nIRQ signal shall be asserted (unless the nIRQ is to be masked by a bit in the IRQ mask register).

The nIRQ is also masked during the power-up sequence and will not be released until the event registers have been cleared. The IRQ triggering event register will be cleared from the host by writing a byte containing a '1' at the bit to be reset (bits written containing a zero will leave the related event register bits unchanged).

The event registers may be read in page/repeated mode. New events that occur during clearing will be delayed before they are passed to the event register, ensuring that the host controller does not miss them.

Register Address	Bit	Type	Label	Description
R05 EVENT_A Note 1	0	R	E_DCIN_DET	DCIN detection caused event
	1	R	E_VBUS_DET	VBUS 4.4 V detection caused event
	2	R	E_DCIN_REM	DCIN removal caused event
	3	R	E_VBUS_REM	VBUS removal caused event
	4	R	E_VDD_LOW	VDDOUT less than VDDOUT_MON threshold caused event
	5	R	E_ALARM	RTC alarm caused event
	6	R	E_SEQ_RDY	Sequencer reached stop position caused event
	7	R	E_COMP_1V2	1.2 V comparator caused event

Note 1 Cleared by writing from host with bit assigned to '1' (bits containing zero during writing do not change event register bits).

Register Address	Bit	Type	Label	Description
R06 EVENT_B Note 1	0	R	E_nONKEY	nONKEY caused event
	1	R	E_ID_FLOAT	Accessory detection change caused event (rising and falling edge of ID_FLOAT, only falling edge during POWER-DOWN mode)
	2	R	E_ID_GND	Accessory detection change caused event (rising and falling edge of ID_GND)
	3	R	E_CHG_END	Battery charging complete caused event
	4	R	E_TBAT	Battery over/ under temp caused event
	5	R	E_ADC_EOM	ADC manual conversion result ready caused event
	6	R	E_PEN_DOWN	Pen down detection caused event
	7	R	E_TSI_READY	TSI sequence (XP, XYP, XYZP) finished caused event

Note 1 Cleared by writing from host with bit assigned to '1' (bits containing zero during writing do not change event register bits).

Register Address	Bit	Type	Label	Description
R07 EVENT_C Note 1	0	R	E_GPI0	GPI event according to active state setting/ ADCIN4 high / low threshold exceeded caused event
	1	R	E_GPI1	GPI event according to active state setting/ ADCIN5 high / low threshold exceeded caused event
	2	R	E_GPI2	GPI event according to active state setting/ ADCIN6 high / low threshold exceeded caused event
	3	R	E_GPI3	GPI event according to active state setting
	4	R	E_GPI4	GPI event according to active state setting
	5	R	E_GPI5	GPI event according to active state setting
	6	R	E_GPI6	GPI event according to active state setting
	7	R	E_GPI7	GPI event according to active state setting

Note 1 Cleared by writing from host with bit assigned to '1' (bits containing zero during writing do not change event register bits).

Register Address	Bit	Type	Label	Description
R08 EVENT_D Note 1	0	R	E_GPI8	GPI event according to active state setting/SYS_EN assertion caused event
	1	R	E_GPI9	GPI event according to active state setting/PWR_EN assertion caused event
	2	R	E_GPI10	GPI event according to active state setting/PWR1_EN assertion caused event
	3	R	E_GPI11	GPI event according to active state setting
	4	R	E_GPI12	GPI event according to active state setting
	5	R	E_GPI13	GPI event according to active state setting
	6	R	E_GPI14	GPI event according to active state setting/Event caused from host addressing HS-2-wire interface
	7	R	E_GPI15	GPI event according to active state setting

Note 1 Cleared by writing from host with bit assigned to '1' (bits containing zero during writing do not change event register bits).

The nIRQ line will be released only when all events have been cleared from the host processor by writing a '1' to each asserted event bit (to prohibit missing events it is recommended to clear event bits individually).

Register Address	Bit	Type	Label	Description
R09 FAULT_LOG Note 1 Note 2	0	R	TWD_ERROR	Watchdog time violated
	1	R	VDD_FAULT	Power down by VDDOUT under voltage detect
	2	R	VDD_START	Power down by VDDOUT under voltage detect within 10 s from releasing nRESET
	3	R	TEMP_OVER	Junction over temperature detected
	4	R		Reserved
	5	R	KEY_SHUT	Power down by a long press of the nONKEY or GPI14 and GPI15 in parallel
	6	R	nSD_SHUT	Power down by assertion of port nSHUTDOWN
	7	R	WAIT_SHUT	Power down by time out of ID WAIT_STEP

Note 1 Cleared by writing from host with bit assigned to '1' (bits containing zero during writing do not change event register bits).

Note 2 The FAULT_LOG register has to be cleared from the host after reading by writing '11111111'.

Register Address	Bit	Type	Label	Description
R10 IRQ_MASK_A	0	R/W	M_DCIN_VLD	Mask DCIN detection caused nIRQ
	1	R/W	M_VBUS_VLD	Mask VBUS 4.4 V detection caused nIRQ
	2	R/W	M_DCIN_REM	Mask DCIN removal caused nIRQ
	3	R/W	M_VBUS_REM	Mask VBUS removal caused nIRQ
	4	R/W	M_VDD_LOW	Mask VDDOUT low caused nIRQ
	5	R/W	M_ALARM	Mask RTC alarm caused nIRQ
	6	R/W	M_SEQ_RDY	Mask Sequencer reached stop position caused nIRQ
	7	R/W	M_COMP_1V2	Mask 1.2 V comparator caused nIRQ

Register Address	Bit	Type	Label	Description
R11 IRQ_MASK_B	0	R/W	M_nONKEY	Mask nONKEY caused nIRQ
	1	R/W	M_ID_FLOAT	Mask ID_FLOAT accessory detection change caused nIRQ
	2	R/W	M_ID_GND	Mask ID_GND accessory detection change caused nIRQ
	3	R/W	M_CHG_END	Mask battery charging complete caused nIRQ

	4	R/W	M_TBAT	Mask Battery over / under temp caused nIRQ
	5	R/W	M_ADC_EOM	Mask ADC manual conversion result ready caused nIRQ
	6	R/W	M_PEN_DOWN	Mask Pen down detection caused nIRQ
	7	R/W	M_TSI_READY	Mask TSI sequence (XP, XYP, XYZP) finished caused nIRQ

Register Address	Bit	Type	Label	Description
R12 IRQ_MASK_C	0	R/W	M_GPI0	Mask GPI caused/ ADCIN4 high / low threshold exceeded caused nIRQ
	1	R/W	M_GPI1	Mask GPI caused/ ADCIN5 high / low threshold exceeded caused nIRQ, should be asserted for LDO H/W control
	2	R/W	M_GPI2	Mask GPI caused/ ADCIN6 high / low threshold exceeded caused nIRQ, should be asserted for LDO H/W control
	3	R/W	M_GPI3	Mask GPI caused nIRQ
	4	R/W	M_GPI4	Mask GPI caused nIRQ
	5	R/W	M_GPI5	Mask GPI caused nIRQ
	6	R/W	M_GPI6	Mask GPI caused nIRQ
	7	R/W	M_GPI7	Mask GPI caused nIRQ

Register Address	Bit	Type	Label	Description
R13 IRQ_MASK_D	0	R/W	M_GPI8	Mask GPI/SYS_EN caused nIRQ
	1	R/W	M_GPI9	Mask GPI/PWR_EN caused nIRQ
	2	R/W	M_GPI10	Mask GPI/PWR1_EN caused nIRQ
	3	R/W	M_GPI11	Mask GPI caused nIRQ
	4	R/W	M_GPI12	Mask GPI caused nIRQ, should be asserted for LDO H/W control
	5	R/W	M_GPI13	Mask GPI caused nIRQ
	6	R/W	M_GPI14	Mask GPI/HS-2-wire caused nIRQ
	7	R/W	M_GPI15	Mask GPI caused nIRQ

Register Address	Bit	Type	Label	Description
R14 CONTROL_A	0	R/W	SYS_EN Note 1	Target status of power domain SYSTEM: state of GPI8 (OTP default ignored) or configuration from OTP/PM interface (depended on setting at

				GPIO_8_PIN)
	1	R/W	PWR_EN Note 2	Target status of power domain POWER: state of GPI9 (OTP default ignored) or configuration from OTP/PM interface (depended on setting at GPIO_9_PIN)
	2	R/W	PWR1_EN Note 3	Target status of power domain POWER1: state of GPI10 (OTP default ignored) or configuration from OTP/PM interface (depended on setting at GPIO_10_PIN)
	3	R/W	PM_IF_V	0: Power manager IF (4-wire/2-wire) supplied from VDD_IO1 1: Power manager IF (4-wire/2-wire) supplied from VDD_IO2
	4	R/W	PM_I_V	nONKEY, nSHUTDOWN, SYS_EN, PWR_EN, PWR1_EN are supplied from: 0: VDDCORE 1: VDD_IO2
	5	R/W	PM_O_V	SYS_UP, PWR_UP, GP_FB2, OUT_32K, nRESET, nIRQ are supplied from: 0: VDD_IO1 1: VDD_IO2
	6	R/W	PM_O_Type	nRESET, nIRQ output are: 0: Push-pull 1: Open drain
	7	R/W	GPI_V	GPIs (not configured as PM control inputs) are supplied from: 0: VDDCORE 1: VDD_IO2

Note 1 SYS_EN hardware control can be configured as high or low active via GPIO_8_Type.

Note 2 PWR_EN hardware control can be configured as high or low active via GPIO_9_Type.

Note 3 PWR1_EN hardware control can be configured as high or low active via GPIO_10_Type.

Register Address	Bit	Type	Label	Description
R15 CONTROL_B	0	R/W	RESERVED	
	1	R/W	ACT_DIODE	Battery provides power 0: through internal active diode path (mandatory, if no external FET connected!) 1: through internal active diode and external power FET
	2	R/W	AUTO_BOOT	0: Start-up of power sequencer after progressing from RESET mode requires a valid wake-up event 1: PMIC automatically starts power sequencer after progressing from RESET mode
	3	R/W	OTPREAD_EN	0: Partial OTP read after POWER-DOWN mode disabled 1: Power supplies are configured with OTP values when leaving POWER-DOWN mode

Register Address	Bit	Type	Label	Description
	4	R/W	BBAT_EN	0: Disables supply from backup battery 1: Automatic switch of VDD_REF to backup battery enabled
	5	R/W	WRITE_MODE	2-wire multiple write mode (setting used for both 2-wire interfaces) 0: Page Write mode 1: Repeated Write mode
	6	R/W	DEEP_SLEEP	If set to '1' DA9053 goes to deep sleep mode (sequencer stops at pointer PART_DOWN). The bit is cleared back to '0' automatically before powering up from POWER-DOWN mode
	7	R/W	SHUTDOWN	If set to '1' the sequencer powers down to RESET mode The bit is cleared back to '0' automatically before leaving the RESET mode

Register Address	Bit	Type	Label	Description
R16 CONTROL_C	0	R/W	PM_FB1_PIN	0: Feedback pin indicates EXT_WAKEUP events (active high) 1: Feedback pin is used as READY indicator, signalling ongoing power mode transitions (power sequencer and DVC) (active low)
	1	R/W	PM_FB2_PIN	0: Feedback pin indicates the status of domain POWER1 (active high PWR1_UP) 1: Feedback pin is used as a configurable GP_FB indicator, that is asserted from the power sequencer
	4:2	R/W	DEBOUNCING	GPI, nONKEY and nSHUTDOWN debounce time 000: no debounce time 001: 10.24 ms 010: 20.48 ms 011: 40.96 ms 100: 102.40 ms 101: 1024 ms 110: 2048 ms 111: 5120 ms
	6:5	R/W	BLINK_FRQ	GPO10/GPO11 flashing frequency 00: no blinking 01: every second 10: every two second 11: every two seconds enabled during PRE-CHARGE mode and emergency charging
	7	R/W	BLINK_DUR	GPO10/GPO11 flashing on-time 0:10 ms 1:40 ms

Register Address	Bit	Type	Label	Description
R17 CONTROL_D	2:0	R/W	TWDSCALE	000: Watchdog disabled 001: 1x scaling applied to TWDMAX period 010: 2x 011: 4x 100: 8x 101: 16x 110: 32x 111: 64x
	3	R/W	KEEPACT_EN	0: nONKEY is enabled 1: nONKEY is disabled, pin asserted to KEEPACT (HW-assertion of bit WATCHDOG)
	4	R/W	nONKEY_SD	0: Disables shutdown via nONKEY 1: Enables shutdown via nONKEY
	5	R/W	GPI14_15_SD	0: Disables shutdown via parallel assertion of GPI14 and GPI15 1: Enables shutdown via GPI14 & GPI15
	6	R/W	ACC_DET_EN	Enables ACC_DET circuitry when set to '1'
	7	R/W	WATCHDOG	If set to '1' watchdog timer is reset. The bit is cleared back to '0' automatically.

Register Address	Bit	Type	Label	Description
R18 PD_DIS	0	R/W	GPIO_PD	0: GPIO extender enabled during POWER-DOWN 1: Auto-Disable of features configured as GPIO pins during POWER-DOWN mode and force the detection of a pending Active state on GPIs by re-enabling the pin through a passive state of the related GPI status register
	1	R/W	GP-ADC_PD	0: ADC/TSI measurements continue during POWER-DOWN as configured 1: Auto-Disable auto measurements on A4, A5, A6, A7(TSI) and manual measurement on all channels during POWER-DOWN mode; if no auto measurements for charging and on A0 are required switch off the ADC completely
	2	R/W	PM-IF_PD	0: Power manager interface not disabled during POWER-DOWN 1: Auto-Disable of Power manager interface during POWER-DOWN mode
	3	R/W	HS-2-wire_PD	0: HS-2-wire not disabled during POWER-DOWN 1: Auto-Disable of HS-2-wire interface during POWER-DOWN mode
	4	R/W	CHG_PD	0: Enables battery charging during POWER-DOWN 1: Auto-Disable battery charging during POWER-DOWN mode
	5	R/W	CHG_BBAT_PD	0: Enables Backup battery charger during POWER-

Register Address	Bit	Type	Label	Description
				DOWN mode 1: Auto-Disable Backup battery charger during POWER-DOWN
	6	R/W	OUT_32K_PD	0: Enables OUT_32K during POWER-DOWN 1: Auto-Disable OUT_32K output buffer during POWER-DOWN mode and auto-enable during power-up from NO-POWER mode when executing this ID
	7	R/W	PM-CONT_PD	0: SYS_EN, PWR_EN, PWR1_EN enabled during POWER-DOWN 1: Auto-Disable of SYS_EN, PWR_EN and PWR_EN during POWER-DOWN mode and force the detection of a pending Active state by re-enabling the pin through a passive state of the related GPI status register

Register Address	Bit	Type	Label	Description
R19 INTERFACE	0	R	IF_Type	0: Power manager IF is 4-wire 1: Power manager IF is 2-wire
	1	R	CPOL	4-wire IF clock polarity 0: SK is low during idle 1: SK is high during idle
	2	R	CPHA	4-wire IF clock phase (see Table : 4-wire clock configurations)
	3	R	R/W_POL	4-wire: Read/Write bit polarity 0: Host indicates reading access via R/W bit = ‘0’ 1: Host indicates reading access via R/W bit = ‘1’
	4	R	nCS_POL	4-wire chip select polarity 0: nCS is low active 1: nCS is high active
	7:5	R	IF_BASE_ADDR (Note 1)	3 MSB of 2-wire control interfaces base address XXX10000 10010000 = 0x90 write address of PM 2-wire interface 10010001 = 0x91 read address of PM 2-wire interface 10010010 = 0x92 write address of HS-2-wire interface 10010011 = 0x93 read address of HS-2-wire interface

Note 1 The base address can be written/modified for unmarked samples having the control OTP_CONF_LOCK not been asserted/fused.

Register Address	Bit	Type	Label	Description
R20 RESET	5:0	R/W	RESET_TIMER	000000: RESET disabled 000001: 1.024 ms 000010: 2.048 ms 000011: 3.072 ms

Register Address	Bit	Type	Label	Description
				000100: 4.096 ms 000101: 5.120 ms …. 011110: 30.720 ms 011111: 31.744 ms 100000: 32.768 ms 100001: 65.536 ms 100010: 98.304 ms ….. 111101: 983.040 ms 111110: 1015.808 ms 111111: 1048.576 ms
	7:6	R/W	RESET_EVENT	RESET timer started by 00: EXT_WAKEUP 01: SYS_UP 10: PWR_UP 11: PWR1_UP (internal signal)

13 GPIO Extender

The DA9053 includes a GPIO extender that offer up to 16 V_{DDOUT}-tolerant (5.5 V max) general purpose input/output pins; each controlled by registers from the host.

NOTE
The input voltage has to be lower than the VDDIO level selected for the port.

The GPIO ports are pin-shared with ports from GP-ADC, TSI-interface, HS-2-wire interface and signals from the power manager and can be individually assigned. Configuration settings and events from several GPIx ports are shared with alternate features. For example, if ADCIN5 was selected, overriding the configured thresholds will trigger a GPI1 event that generates a maskable GPI1 interrupt. The GPI active High/Low setting from GPIOx_Type register and the selection of supply rail (and pull-up resistor) is also valid for the alternate port features selected via GPIOx_PIN (for example SYS_EN, PWR_EN and PWR1_EN). The same is true for GPIOx_MODE to enable triggering a Wake-up event (ADCIN4, ADCIN5, SYS_EN, PWR_EN, PWR1_EN, HS-2-wire interface) for the alternate features.

In ACTIVE and POWER-DOWN mode the GPIO Extender can continuously monitor the level of ports that are selected as general purpose inputs. GPIs are supplied from the internal rail VDDCORE or VDD_IO2 and can be configured to trigger events in active high or active low mode. The input signals can be debounced or directly change the state of the assigned status register GPIx to high or low. Whenever the status has changed to its configured active state (edge sensitive) the assigned event register is set and the nIRQ signal is asserted (unless this nIRQ is masked inside the nIRQMASK register). GPI 0, 3 to 11 and 13 to 15 will generate a system wake-up if debouncing is enabled. In debouncing off mode GPI 12 enables/disables LDO9, the minimum enable time is 100 µs. The same feature is available at GPI 1 for LDO4_EN and GPI 2 for LDO5_EN. Events on GPI10 can be used to control the progress of the power sequencer. Processing ID WAIT_STEP will cause the sequencer to wait until GPI 10 changes into active state.

If defined as an output the GPO can be configured as open-drain or push-pull. The supply rail can be individually selected from either VDD_IO1 or VDD_IO2. When selecting VDD_IO1 in open-drain mode, there is an internal pull-up resistor against this rail, otherwise an external pull-up resistor towards the target voltage level is required. The output state will be assigned as configured by the GPIO register bit GPIOx_MODE.

GPO 10 and 11 are high-power GPO ports, where the maximum sink current is rated to be 15 mA and the maximum source current will be 4 mA. This enables driving LEDs with optional RTC timer controlled flashing.

GPO 14 and 15 are high-power GPO ports able to sink up to 30 mA and include an optional PWM control. The PWM control can also be made to dim the brightness between its current value and a new value at a rate of 32 ms per step. In conjunction with the LED3 drive, which offers a similar PWM mode, this creates a common anode tri-color LED brightness control.

Register Address	Bit	Type	Label	Description
R21 GPIO_0-1	1:0	R/W	GPIO0_PIN	PIN assigned to 00: ADCIN4 01: GPI 10: GPO (Open drain) 11: GPO (Push-pull)
	2	R/W	GPIO0_Type	0: GPI: active low GPO: supplied from VDD_IO1/internal pull-up in

				open-drain mode 1: GPI: active high GPO: supplied from VDD_IO2/external pull-up in open-drain mode
	3	R/W	GPIO0_ MODE	0: GPI/ADCIN4: debouncing off GPO: Sets output to low level 1: GPI/ADCIN4: debouncing on and generate wake-up GPO: Sets output to high level
	5:4	R/W	GPIO1_PIN	PIN assigned to 00: ADCIN5/1.2 V comparator 01: GPI (LDO4 HW control) 10: GPO (Open drain) 11: GPO (Push-pull)
	6	R/W	GPIO1_Type	0: GPI: active low GPO: supplied from VDD_IO1/internal pull-up in open-drain mode 1: GPI: active high GPO: supplied from VDD_IO2/external pull-up in open-drain mode
	7	R/W	GPIO1_ MODE	0: GPI/ADCIN5:/ debouncing off, Set LDO4_EN when GPI transfers to active state (reset when GPI gets to passive state) 1.2 V comparator: (debouncing off), Set LDO4_EN when GPI transfers to active state (reset when GPI gets to passive state) GPO: Sets output to low level 1: GPI: debouncing on, no LDO4_EN control ADCIN5/1.2 V comparator: debouncing on and generate wake up GPO: Sets output to high level

If GPIO1 pin = 01 and GPIO1 mode = 00 then bit 1 of register R12 should also be set to avoid small nIRQ pulse generation.

Register Address	Bit	Type	Label	Description
R22 GPIO_2-3	1:0	R/W	GPIO2_PIN	PIN assigned to 00: ADCIN6 01: GPI (LDO5 HW control) 10: GPO (Open drain) 11: GPO (Push-pull)
	2	R/W	GPIO2_Type	0: GPI: active low GPO: supplied from VDD_IO1/internal pull-up in open-drain mode 1: GPI: active high GPO: supplied from VDD_IO2/external pull-up in open-drain mode
	3	R/W	GPIO2_MODE	0: GPI/ADCIN6: (debouncing off), Set LDO5_EN when GPI transfers to active state (reset when GPI gets to passive state) GPO: Sets output to low level

				1: GPI: debouncing on, no LDO5_EN control ADCIN6: debouncing on and generate wake up GPO: Sets output to high level
	5:4	R/W	GPIO3_PIN	PIN assigned to 00: TSIYN 01: GPI 10: GPO (Open drain) 11: GPO (Push-pull)
	6	R/W	GPIO3_Type	0: GPI: active low GPO: supplied from VDD_IO1/internal pull-up in open-drain mode 1: GPI: active high GPO: supplied from VDD_IO2/external pull-up in open-drain mode
	7	R/W	GPIO3_ MODE	0: GPI: debouncing off GPO: Sets output to low level 1: GPI: debouncing on and generate wake-up GPO: Sets output to high level

If GPIO2 pin = 01 and GPIO2 mode = 0 then bit 2 of register R12 should also be set to avoid small nIRQ pulse generation.

Register Address	Bit	Type	Label	Description
R23 GPIO_4-5	1:0	R/W	GPIO4_PIN	PIN assigned to 00: TSIYP 01: GPI 10: GPO (Open drain) 11: GPO (Push-pull)
	2	R/W	GPIO4_Type	0: GPI: active low GPO: supplied from VDD_IO1/internal pull-up in open-drain mode 1: GPI: active high GPO: supplied from VDD_IO2/external pull-up in open-drain mode
	3	R/W	GPIO4_ MODE	0: GPI: debouncing off GPO: Sets output to low level 1: GPI: debouncing on and generate wake-up GPO: Sets output to high level
	5:4	R/W	GPIO5_PIN	PIN assigned to 00: TSIXN 01: GPI 10: GPO (Open drain) 11: GPO (Push-pull)
	6	R/W	GPIO5_Type	0: GPI: active low GPO: supplied from VDD_IO1/internal pull-up in open-drain mode 1: GPI: active high GPO: supplied from VDD_IO2/external pull-up in open-drain mode

	7	R/W	GPIO5_ MODE	0: GPI: debouncing off GPO: Sets output to low level 1: GPI: debouncing on and generate wake-up GPO: Sets output to high level

Register Address	Bit	Type	Label	Description
R24 GPIO_6-7	1:0	R/W	GPIO6_PIN	PIN assigned to 00: TSIXP 01: GPI 10: GPO (Open drain) 11: GPO (Push-pull)
	2	R/W	GPIO6_Type	0: GPI: active low GPO: supplied from VDD_IO1/internal pull-up in open-drain mode 1: GPI: active high GPO: supplied from VDD_IO2/external pull-up in open-drain mode
	3	R/W	GPIO6_ MODE	0: GPI: debouncing off GPO: Sets output to low level 1: GPI: debouncing on and generate wake-up GPO: Sets output to high level
	5:4	R/W	GPIO7_PIN	PIN assigned to 00: TSIREF 01: GPI 10: GPO (Open drain) 11: GPO (Push-pull)
	6	R/W	GPIO7_Type	0: GPI: active low GPO: supplied from VDD_IO1/internal pull-up in open-drain mode 1: GPI: active high GPO: supplied from VDD_IO2/external pull-up in open-drain mode
	7	R/W	GPIO7_ MODE	0: GPI: debouncing off GPO: Sets output to low level 1: GPI: debouncing on and generate wake-up GPO: Sets output to high level

Register Address	Bit	Type	Label	Description
R25 GPIO_8-9	1:0	R/W	GPIO8_PIN	PIN and status register bit assigned to 00: SYS_EN 01: GPI 10: GPO (Open drain) 11: GPO (Push-pull)
	2	R/W	GPIO8_Type	0: GPI/SYS_EN: active low GPO: supplied from VDD_IO1/internal pull-up in open-drain mode 1: GPI/SYS_EN: active high

				GPO: supplied from VDD_IO2/external pull-up in open-drain mode
	3	R/W	GPIO8_ MODE	0: GPI only (not SYS_EN): debouncing off GPO: Sets output to low level 1: GPI/SYS_EN: debouncing on and generate wake-up GPO: Sets output to high level
	5:4	R/W	GPIO9_PIN	PIN and status register bit assigned to 00: PWR_EN 01: GPI 10: GPO (Open drain) 11: GPO (Push-pull)
	6	R/W	GPIO9_Type	0: GPI/PWR_EN: active low GPO: supplied from VDD_IO1/internal pull-up in open-drain mode 1: GPI/PWR_EN: active high GPO: supplied from VDD_IO2/external pull-up in open-drain mode
	7	R/W	GPIO9_ MODE	0: GPI/PWR_EN: debouncing off GPO: Sets output to low level 1: GPI/PWR_EN debouncing on and generate wake-up GPO: Sets output to high level

Register Address	Bit	Type	Label	Description
R26 GPIO_10-11	1:0	R/W	GPIO10_PIN	PIN and status register bit assigned to 00: PWR1_EN 01: GPI 10: GPO (Open drain) 11: GPO (Push-pull)

	2	R/W	GPIO10_Type	0: GPI/PWR1_EN: active low GPO: supplied from VDD_IO1/internal pull-up in open-drain mode 1: GPI/PWR1_EN: active high GPO: blinking from RTC counter, supplied from VDD_IO2/ external pull-up in open-drain mode
	3	R/W	GPIO10_ MODE	0: GPI/PWR1_EN: debouncing off GPO: Sets output to low level 1: GPI/PWR1_EN: debouncing on and generate wake-up, time out from processing ID WAIT_STEP after 500ms GPO: Sets output to high level
	5:4	R/W	GPIO11_PIN	PIN assigned to 00: ACC_ID_DET 01: GPI 10: GPO (Open drain) 11: GPO (Push-pull)
	6	R/W	GPIO11_Type	0: GPI: active low GPO: supplied from VDD_IO1/internal pull-up in open-drain mode 1: GPI: active high GPO: blinking from RTC counter, supplied from VDD_IO2/external pull-up in open-drain mode
	7	R/W	GPIO11_ MODE	0: GPI: : debouncing off / ACC_ID_DET: debouncing off GPO: Sets output to low level 1: GPI: : debouncing on and generate wake-up /ACC_ID_DET: debouncing on and generate wake-up (for ACC_ID_DET only at ID_FLOAT falling edge) GPO: Sets output to high level

Register Address	Bit	Type	Label	Description
R27 GPIO_12-13	1:0	R/W	GPIO12_PIN	PIN and status register bit assigned to 00: GP_FB1 (EXT_WAKEUP/READY) 01: GPI (LDO9 HW control) 10: GPO (Open drain) 11: GPO (Push-pull)
	2	R/W	GPIO12_Type	0: GPI: active low GPO/GP_FB1: supplied from VDD_IO1/internal pull-up for open-drain 1: GPI: active high GPO/GP_FB1: supplied from VDD_IO2/external pull-up in open-drain mode
	3	R/W	GPIO12_MODE	0: GPI: debouncing off, Set LDO9_EN when GPI transfers to active state (reset when GPI gets to passive state) GPO: Sets output to low level 1: GPI: debouncing on, no LDO9_EN control GPO: Sets output to high level
	5:4	R/W	GPIO13_PIN	PIN assigned to 00: nVDD_FAULT 01: GPI 10: GPO (Open drain) 11: GPO (Push-pull)
	6	R/W	GPIO13_Type	0: GPI: active low GPO/nVDD_FAULT: supplied from VDD_IO1/internal pull-up for open-drain 1: GPI: active high GPO/nVDD_FAULT: supplied from VDD_IO2/external pull-up in open-drain mode
	7	R/W	GPIO13_MODE	0: GPI: debouncing off GPO: Sets output to low level 1: GPI: debouncing on and generate wake-up GPO: Sets output to high level

If GPIO12 pin = 01 and GPIO12 mode = 0 then bit 4 of register R13 should also be set to avoid small nIRQ pulse generation.

Register Address	Bit	Type	Label	Description
R28 GPIO_14-15	1:0	R/W	GPIO14_PIN	PIN assigned to 00: DATA (assigns GPIO15_PIN to CLK) 01: GPI 10: GPO (Open drain, PWM control) 11: GPO (Push-pull)
	2	R/W	GPIO14_Type	0: GPI: active low GPO: supplied from VDD_IO1/internal pull-up in open-drain mode 1: GPI: active high GPO: supplied from VDD_IO2/external pull-up in open-drain mode
	3	R/W	GPIO14_ MODE	0: GPI: debouncing off, no wake-up HS-2-wire: no wake-up GPO: Sets output to low level 1: GPI:debouncing on and generate wake-up HS-2-wire: generate wake-up when interface was accessed GPO: Sets output to high level
	5:4	R/W	GPIO15_PIN	PIN assigned to 00: CLK (see GPIO14_PIN) 01: GPI 10: GPO (Open drain, PWM control) 11: GPO (Push-pull)
	6	R/W	GPIO15_Type	0: GPI: active low GPO: supplied from VDD_IO1/internal pull-up in open-drain mode DATA/CLK supplied from VDD_IO1 (Note 1) 1: GPI: active high GPO: supplied from VDD_IO2/external pull-up in open-drain mode DATA/CLK supplied from VDD_IO2
	7	R/W	GPIO15_ MODE	0: GPI: debouncing off GPO: Sets output to low level 1: GPI: debouncing on and generate wake-up GPO: Sets output to high level

Note 1 In power commander mode the HS-2-wire IF is always supplied from VDDCORE.

14 Power Supply Sequencer

The start-up of DA9053 supplies is performed with a sequencer. The sequencer is able to control up to 22 IDs (4 buck converter, 2 rail switches, 10 LDOs, 4 feedback pin level controls, a Wait ID and a POWER-DOWN register), which can be grouped in 3 power domains. The power sequences for each domain have configurable size.

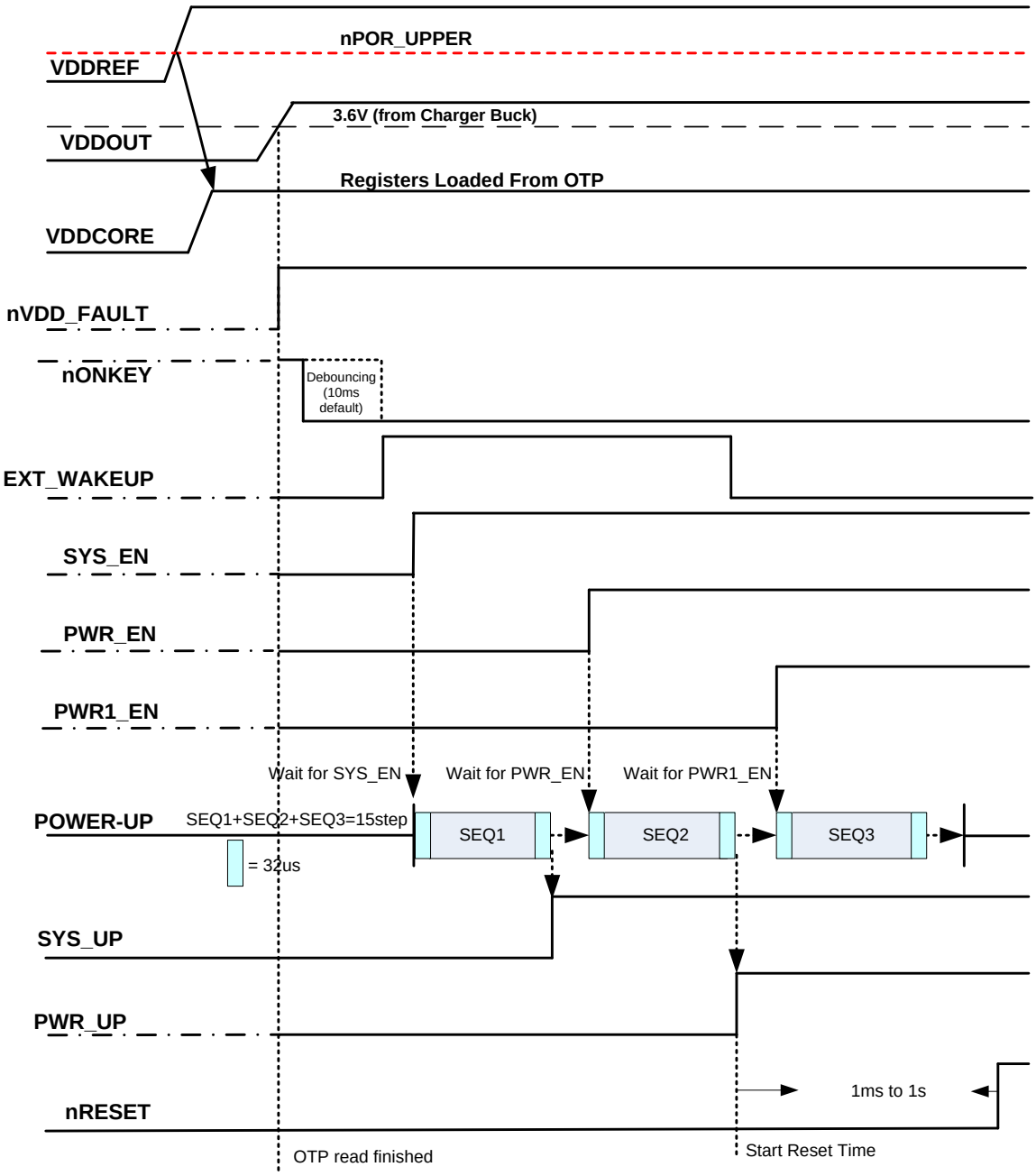

Figure 43: Typical Power-Up Timing

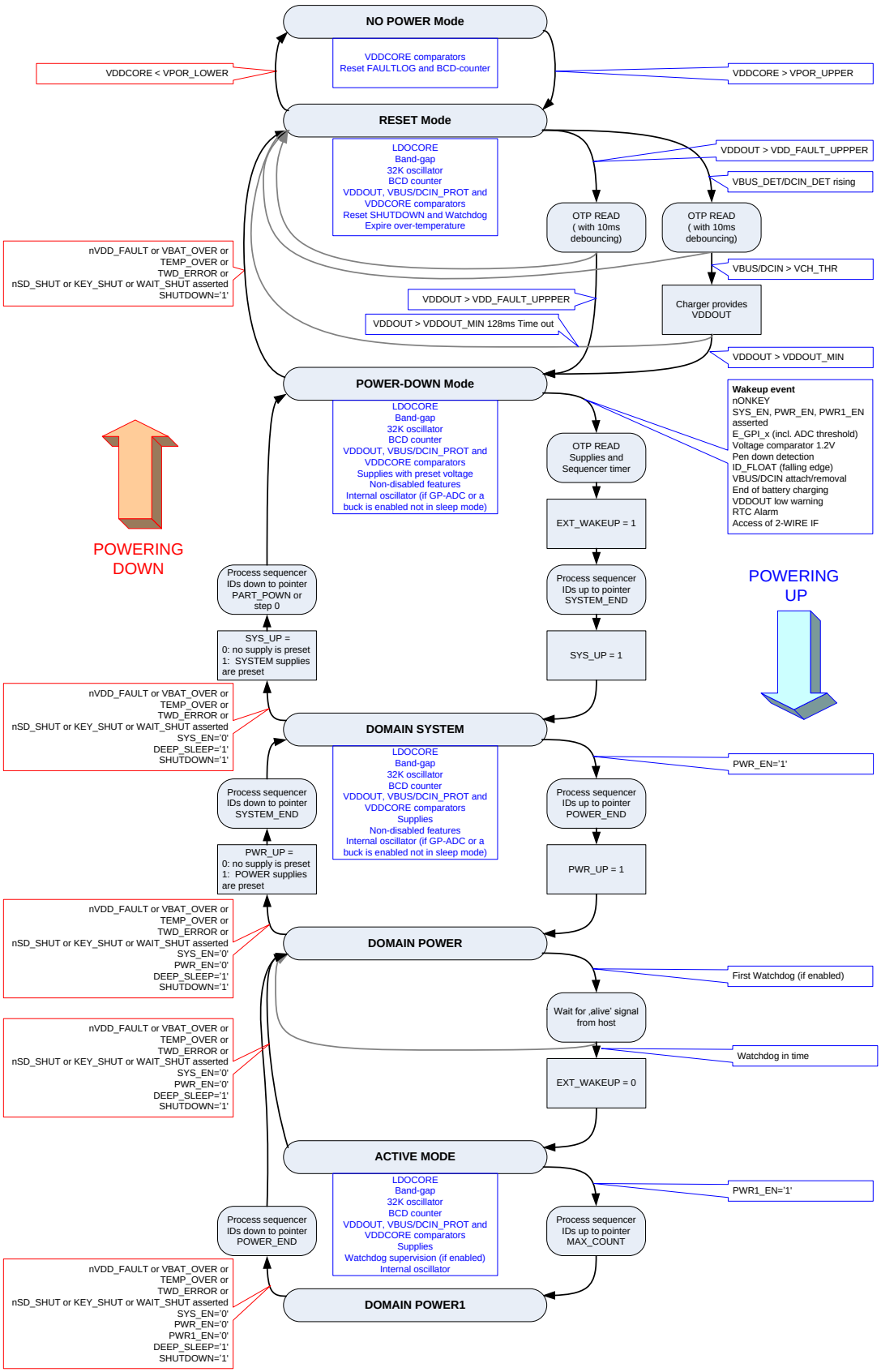

Figure 44: Power Mode Transitions

Table 48: Power Sequencer Control Registers

Register Address	Bit	Type	Label	Description
R29 ID_0_1	0	R/W	nRES_MODE	0: No assertion of nRESET during POWER-DOWN mode 1: Assert nRESET when entering POWER-DOWN mode (release after leaving POWER-DOWN mode)
	1	R/W	DEF_SUPPLY	When asserted all supplies (beside LDOCORE) are enabled/disabled from OTP default mode
	2	R/W	SYS_PRE	0: Set SYS_UP as configured from supplies presettings 1: Always de-assert SYS_UP before powering down domain SYSTEM
	3	R/W	WAIT_ID_ALWAYS PD_MODE	0: Only perform the WAIT_ID step on first use of the sequencer 1: Perform the WAIT_ID step all uses of the sequencer
	7:4	R/W	LDO1_STEP	Power sequencer time **slot 9**

Register Address	Bit	Type	Label	Description
R30 ID_2_3	3:0	R/W	LDO2_STEP	Power sequencer time slot 4
	7:4	R/W	LDO3_STEP	Power sequencer time slot 8

Register Address	Bit	Type	Label	Description
R31 ID_4_5	3:0	R/W	LDO4_STEP	Power sequencer time slot 2
	7:4	R/W	LDO5_STEP	Power sequencer time slot 3

Register Address	Bit	Type	Label	Description
R32 ID_6_7	3:0	R/W	LDO6_STEP	Not controlled by power sequencer
	7:4	R/W	LDO7_STEP	Not controlled by power sequencer

Register Address	Bit	Type	Label	Description
R33 ID_8_9	3:0	R/W	LDO8_STEP	Not controlled by power sequencer
	7:4	R/W	LDO9_STEP	Not controlled by power sequencer

Register Address	Bit	Type	Label	Description
R34 ID_10_11	3:0	R/W	LDO10_STEP	Not controlled by power sequencer
	7:4	R/W	PD_DIS_STEP	Power sequencer time **slot 5**

Register Address	Bit	Type	Label	Description
R35 ID_12_13	3:0	R/W	VPERI_SW_STEP	Not controlled by power sequencer
	7:4	R/W	VMEM_SW_STEP	Not controlled by power sequencer

Register Address	Bit	Type	Label	Description
R36 ID_14_15	3:0	R/W	BUCKCORE_STEP	Power sequencer time **slot 1**
	7:4	R/W	BUCKPRO_STEP	Power sequencer time **slot 7**

Register a Address	Bit	Type	Label	Description
R37 ID_16_17	3:0	R/W	BUCKMEM_STEP	Not controlled by power sequencer
	7:4	R/W	BUCKPERI_STEP	Not controlled by power sequencer

Register Address	Bit	Type	Label	Description
R38 ID_18_19	3:0	R/W	GP_RISE1_STEP	Not controlled by power sequencer
	7:4	R/W	GP_RISE2_STEP	Not controlled by power sequencer

Register Address	Bit	Type	Label	Description
R39 ID_20_21	3:0	R/W	GP_FALL1_STEP	Not controlled by power sequencer
	7:4	R/W	GP_FALL2_STEP	Not controlled by power sequencer

Register Address	Bit	Type	Label	Description
R40 SEQ_STATUS	3:0	R/W	WAIT_STEP	Not controlled by power sequencer
	7:4	R/W	SEQ_POINTER	Actual pointer position (time slot) of power sequencer

Register Address	Bit	Type	Label	Description
R41 SEQ_A	3:0	R/W	SYSTEM_END	OTP pointer to last supply of domain SYSTEM
	7:4	R/W	POWER_END	OTP pointer to last supply of domain POWER

Register Address	Bit	Type	Label	Description
R42 SEQ_B	3:0	R/W	MAX_COUNT	OTP pointer to last supply of domain POWER1
	7:4	R/W	PART_DOWN	OTP pointer for partial POWER-DOWN mode

Register Address	Bit	Type	Label	Description
R43 SEQ_TIMER	3:0	R/W	SEQ_TIME	0000: 32 µs 0001: 64 µs 0010: 96 µs 0011: 128 µs 0100: 160 µs 0101: 192 µs 0110: 224 µs 0111: 256 µs 1000: 288 µs 1001: 384 µs 1010: 448 µs 1011: 512 µs 1100: 1.024 ms 1101: 2.048 ms 1110: 4.096 ms 1111: 8.192 ms
	7:4	R/W	SEQ_DUMMY	0000: 32 µs 0001: 64 µs 0010: 96 µs 0011: 128 µs 0100: 160 µs 0101: 192 µs 0110: 224 µs 0111: 256 µs 1000: 288 µs 1001: 384 µs 1010: 448 µs 1011: 512 µs 1100: 1.024 ms 1101: 2.048 ms 1110: 4.096 ms 1111: 8.192 ms

15 Voltage Regulators

Three types of low dropout regulators are integrated on the DA9053, each optimized for performance depending on the most critical parameter of the circuitry supplied. For high performance analog supplies (for example audio) the regulators have been designed to offer high PSRR and low noise, for the digital supplies PSRR is relaxed saving quiescent current and for the PMIC core/RTC supplies quiescent current has been optimised as the most important performance parameters. The regulators employ Dialog Semiconductor's SmartMirror™ dynamic biasing, removing the need for a low-power operating mode and associated software or hardware overhead.

SmartMirror™ technology guarantees a high phase margin within the regulator control loop and has been designed to offer stable performance with small output capacitances over a wide range of output currents. The circuit technique offers significantly higher gain bandwidth performance than conventional designs, enabling higher power supply rejection performance at higher frequencies. PSRR is also maintained across the full operating current range however quiescent current consumption is scaled to demand giving improved efficiency when current demand is low.

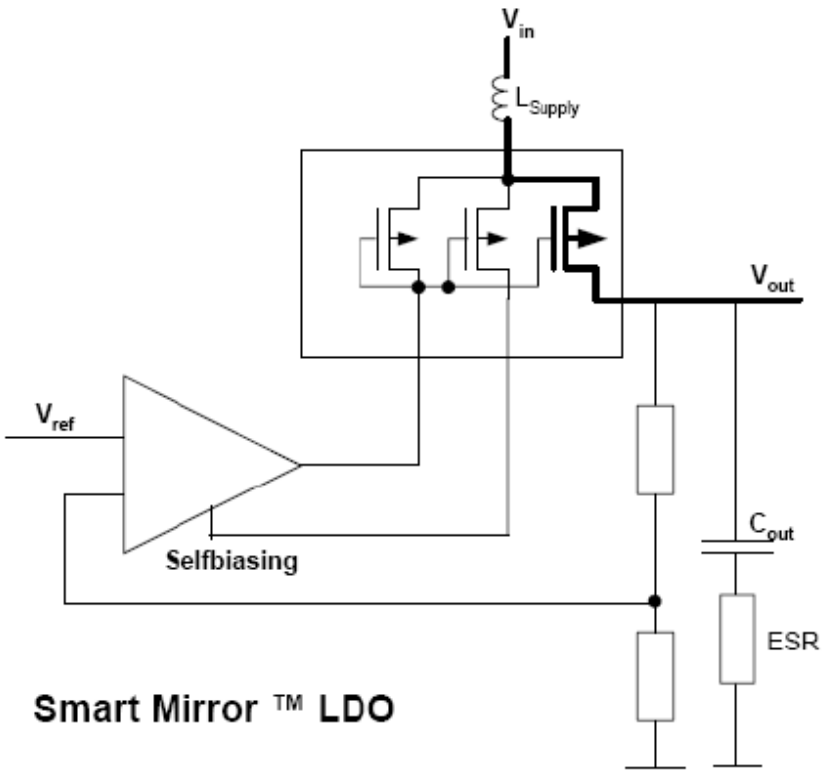

Figure 45: Smart Mirror™ Voltage Regulator

The regulator output voltages are fully programmable via the control interface allowing optimisation of the complete system for maximum performance and power efficiency. For security reasons the re-programming of output voltages from the control interfaces can be disabled. The default output voltage is loaded from after start-up from OTP. A power saving mode is not required for the LDOs due to the use of dynamic biasing in the LDO internal circuitry, so when operating at low current demands the quiescent current taken by the regulator is automatically minimised. LD01 to LDO10

can optionally be supplied from a buck output (VDD < 2.8 V). In this mode some specification parameters will change.

LDO2 and LDO3 include dynamic DVC control to enable power savings on peripheral domains:

- The output voltage is programmable over the power manager bus in 25 mV steps.
- The output voltage ramp step size is 6.25 mV/µs while slewing. If the feedback signal is configured to be READY this line is asserted while slewing.

NOTE
Powering down to RESET mode will automatically disable all regulators beside LDO1.

LDO4, 5 and 9 include an optional hardware enable/disable via GPIO1, 2 and 12 by selecting the GPI feature with ‘debouncing off’.

LDO1 to LDO10 can be controlled inside the power manager sequence. If enabled at sequencer step 0 (DEF_SUPPLY) supplies can be default enabled via OTP whenever the sequencer passes step 0 (OTP settings are used). To limit the battery rush current it is recommended to enable not more than a single supply (including bucks) at step 0. When powering down (for example to POWER-DOWN mode) sequencer controlled supplies can be pre-configured with a new target voltage (LDOx_CONF bit is set). If LDOx_CONF was asserted in parallel with LDOx_EN also the supply enable is deferred until the sequencer is processing the related ID. The previous output voltage and enable state will be kept unchanged until the sequencer processes the related time slot/ID during powering down (ignoring any assertions of VLDOx_GO while LDOx_CONF is high). Before wake-up from POWER-DOWN mode (processing time slots from domain SYSTEM) the sequencer will configure all regulators with their default voltage values from OTP and by that also reset the LDOx_CONF bits. The regulators can also be enabled/disabled/configured via the power manager and HS-2-wire interface when the DA9053 is in the ACTIVE state. Voltage transitions on LDOs including DVC will always be ramped.

Disabling regulators LDO1, 2, and 5 can switch off their pull down resistor which is required for usage in parallel to an alternate supply.

15.1 Core Regulator LDOCORE

The LDOCORE will be used for running the DA9053 internal Real Time Clock module, internal state machine, GPIO pins with comparators, bias, reference, GPADC, OTP and power manager registers. It is supplied by the battery switch either from an external supply, VBAT or the backup battery (coin cell or super cap). If no backup battery exists or the backup battery charger is configured to a level below 2.0 V the automatic VREF switch to the backup battery can be disabled.

15.2 DC/DC Buck Converters

DA9053 includes four DC/DC buck converters,

NOTE
Powering down to RESET mode will automatically disable all buck converters.

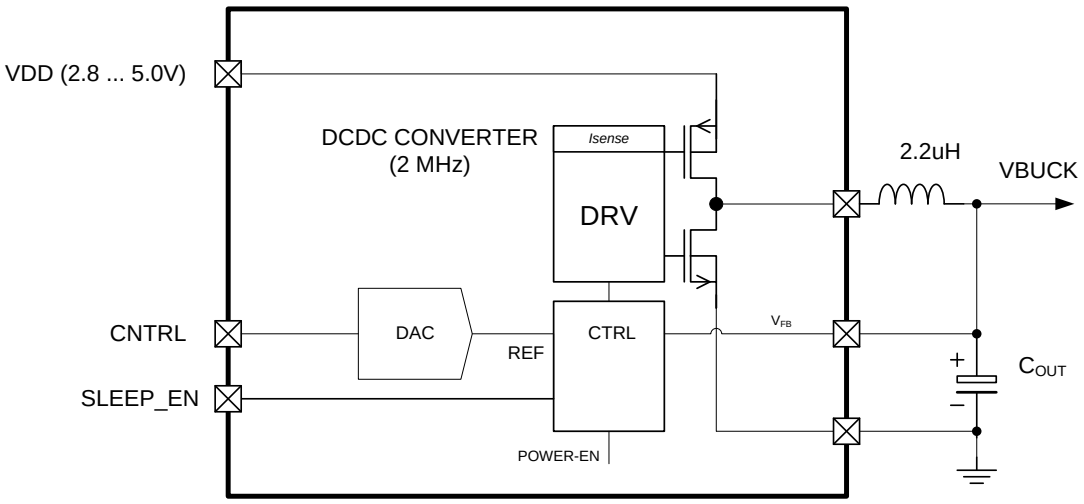

Figure 46: DCDC Buck Converter

15.3 Converters BUCKCORE, BUCKPRO and BUCKMEM with DVC

These converters are high efficiency synchronous step down regulators operating at a high frequency (2 MHz) supplying individual output voltages with +/- 3 % accuracy. Default output voltage is loaded from OTP and can be set in 25 mV steps.

The DVC controller allows the following features:

- The buck converter output voltage to be programmable over the power manager bus in 25 mV steps.
- The output voltage ramp step size is 6.25 mV/µs while slewing. If the feedback signal is configured to be READY this line is asserted while slewing.
- Output voltages below 0.725 V will only be supported in Pulse Frequency Modulation (PFM) mode. During a voltage reduction below 0.725 V the slew rate control ends at 0.725 V and the buck mode is automatically changed to sleep mode (with reduced maximum current capability). The timing of voltage transitions between 0.5 V and 0.725 V depends on the load.

The supply current during PWM (synchronous rectification) operation is in the order of 4 mA for BUCKCORE and 2.5 mA for BUCKPRO, BUCKMEM and BUCKPERI (quiescent current and charge/discharge current) and drops to < 1 µA in shutdown.

The buck converter can be forced to operate in either Synchronous mode or Sleep mode. Additionally the buck converter has an automatic mode where it will switch between Synchronous and Sleep mode depending on the load current. In Sleep mode the buck converter works in PFM mode. An internal zero crossing comparator is used to time the turn-off of the NFET, thereby removing the need for an external Schottky diode.

The converters BUCKPERI and BUCKMEM provide additional power path switches that can be controlled from the sequencer. This enables a partial power down of IO and power rails for optimized application quiescent currents during standby/hibernate modes.

The embedded soft start (approximately 200 µs) enables a usage as power manager controlled hot swap power switches with a maximum capacitive load up to 10 µF (for example for SD-cards). If a switch is open, the associated pin will be discharged to VSS by a pull down resistor.

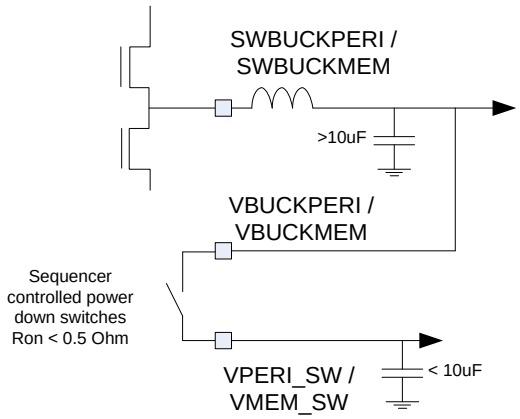

Figure 47: BUCKPERI / BUCKMEM Output Switches

Table 49 shows the relationship between the programmed buck current limit and the saturation current limit of the coil. It must be ensured that the minimum I_{SAT} is above the maximum current limit including spread.

Table 49: Buck Current Limit and Coil Saturation Current Limit

Min. I_{SAT} (mA)	Frequency (MHz)	Buck Current Limit (mA)
3600	2	3000
2900	2	2400
1800	2	1500
1680	2	1400
1450	2	1200
1080	2	900
840	2	700

16 Power Supplies

Table 50: Power Supply Control Registers

Register Address	Bit	Type	Label	Description
R44 BUCK_A	1:0	R/W	BCORE_MODE	00: BUCKCORE always operates in Sleep mode 01: BUCKCORE operates in Automatic mode 10: BUCKCORE always operates in Synchronous mode 11: BUCKCORE in Automatic forcing to Synchronous mode
	3:2	R/W	BCORE_ILIM	00: BUCKCORE current limit 1600 mA 01: BUCKCORE current limit 2000 mA 10: BUCKCORE current limit 2400 mA 11: BUCKCORE current limit 3000 mA
	5:4	R/W	BPRO_MODE	00: BUCKPRO always operates in Sleep mode 01: BUCKPRO operates in Automatic mode 10: BUCKPRO always operates in Synchronous mode 11: BUCKPRO in Automatic forcing to Synchronous mode
	7:6	R/W	BPRO_ILIM	00: BUCKPRO current limit 800 mA 01: BUCKPRO current limit 1000 mA 10: BUCKPRO current limit 1200 mA 11: BUCKPRO current limit 1500 mA

Register Address	Bit	Type	Label	Description
R45 BUCK_B	1:0	R/W	BMEM_ MODE	00: BUCKMEM always operates in Sleep mode 01: BUCKMEM operates in Automatic mode 10: BUCKMEM always operates in Synchronous mode 11: BUCKMEM in Automatic forcing to Synchronous mode
	3:2	R/W	BMEM_ILIM	00: BUCKMEM current limit 800 mA 01: BUCKMEM current limit 1000 mA 10: BUCKMEM current limit 1200 mA 11: BUCKMEM current limit 1500 mA
	5:4	R/W	BPERI_ MODE	00: BUCKPERI always operates in Sleep mode 01: BUCKPERI operates in Automatic mode 10: BUCKPERI always operates in Synchronous mode 11: BUCKPERI in Automatic forcing to Synchronous mode
	7:6	R/W	BPERI_ILIM	00: BUCKPERI current limit 800 mA 01: BUCKPERI current limit 1000 mA 10: BUCKPERI current limit 1200 mA 11: BUCKPERI current limit 1500 mA

Register Address	Bit	Type	Label	Description
R46 BUCKCORE	5:0	R/W	VBCORE	000000: 0.500 V 000001: 0.525 V 000010: 0.550 V 000011: 0.575 V 000100: 0.600 V 000101: 0.625 V … 011011: 1.175 V 011100: 1.200 V 011101: 1.225 V 011110: 1.250 V 011111: 1.275 V 100000: 1.300 V 100001: 1.325 V 100010: 1.350 V 100011: 1.375 V 100100: 1.400 V 100101: 1.425 V 100110: 1.450 V 100111: 1.475 V 101000: 1.500 V 101001: 1.525 V 101010: 1.550 V 101011: 1.575 V 101100: 1.600 V 101101: 1.625 V 101110: 1.650 V 101111: 1.675 V 110000: 1.700 V 110001: 1.725 V 110010: 1.750 V 110011: 1.775 V 110100: 1.800 V 110101: 1.825 V 110110: 1.850 V 110111: 1.875 V 111000: 1.900 V 111001: 1.925 V 111010: 1.950 V 111011: 1.975 V 111100: 2.000 V 111101: 2.025 V 111110: 2.050 V 111111: 2.075 V
	6	R/W	BCORE_EN	0: BUCKCORE disabled

				1: BUCKCORE enabled
	7	R/W	BCORE_CONF	0: Voltage ramped after assertion of VB_CORE_GO 1: Supply voltage preset

Register Address	Bit	Type	Label	Description
R47 BUCKPRO	5:0	R/W	VBPRO	000000: 0.500 V 000001: 0.525 V 000010: 0.550 V 000011: 0.575 V 000100: 0.600 V 000101: 0.625 V … 011011: 1.175 V 011100: 1.200 V 011101: 1.225 V 011110: 1.250 V 011111: 1.275 V 100000: 1.300 V 100001: 1.325 V 100010: 1.350 V 100011: 1.375 V 100100: 1.400 V 100101: 1.425 V 100110: 1.450 V 100111: 1.475 V 101000: 1.500 V 101001: 1.525 V 101010: 1.550 V 101011: 1.575 V 101100: 1.600 V 101101: 1.625 V 101110: 1.650 V 101111: 1.675 V 110000: 1.700 V 110001: 1.725 V 110010: 1.750 V 110011: 1.775 V 110100: 1.800 V 110101: 1.825 V 110110: 1.850 V 110111: 1.875 V 111000: 1.900 V 111001: 1.925 V 111010: 1.950 V 111011: 1.975 V 111100: 2.000 V

				111101: 2.025 V 111110: 2.050 V 111111: 2.075 V
	6	R/W	BPRO_EN	0: BUCKPRO disabled 1: BUCK PRO enabled
	7	R/W	BPRO_CONF	0: Voltage ramped after assertion of VB_PRO_GO 1: Supply voltage preset

Register Address	Bit	Type	Label	Description
R48 BUCKMEM	5:0	R/W	VBMEM	000000: 0.950 V 000001: 0.975 V 000010: 1.000 V 000011: 1.025 V 000100: 1.050 V … 010110: 1.500 V 010111: 1.525 V 011000: 1.550 V 011001: 1.575 V 011010: 1.600 V 011011: 1.625 V 011100: 1.650 V 011101: 1.675 V 011110: 1.700 V 011111: 1.725 V 100000: 1.750 V 100001: 1.775 V 100010: 1.800 V 100011: 1.825 V 100100: 1.850 V 100101: 1.875 V 100110: 1.900 V 100111: 1.925 V 101000: 1.950 V 101001: 1.975 V 101010: 2.000 V 101011: 2.025 V 101100: 2.050 V 101101: 2.075 V 101110: 2.100 V 101111: 2.125 V 110000: 2.150 V 110001: 2.175 V 110010: 2.200 V 110011: 2.225 V 110100: 2.250 V

				110101: 2.275 V 110110: 2.300 V 110111: 2.325 V 111000: 2.350 V 111001: 2.375 V 111010: 2.400 V 111011: 2.425 V 111100: 2.450 V 111101: 2.475 V 111110: 2.500 V 111111: 2.525 V
	6	R/W	BMEM_EN	0: BUCKMEM disabled 1: BUCKMEM enabled
	7	R/W	BMEM_CONF	0: Voltage ramped after assertion of VB_MEM_GO 1: Supply voltage preset

Register Address	Bit	Type	Label	Description
R49 BUCKPERI	5:0	R/W	VBPERI	000000: 0.950 V 000001: 0.975 V 000010: 1.000 V 000011: 1.025 V 000100: 1.050 V … 010110: 1.500 V 010111: 1.525 V 011000: 1.550 V 011001: 1.575 V 011010: 1.600 V 011011: 1.625 V 011100: 1.650 V 011101: 1.675 V 011110: 1.700 V 011111: 1.725 V 100000: 1.750 V 100001: 1.775 V 100010: 1.800 V 100011: 1.825 V 100100: 1.850 V 100101: 1.875 V 100110: 1.900 V 100111: 1.925 V 101000: 1.950 V 101001: 1.975 V 101010: 2.000 V 101011: 2.025 V 101100: 2.050 V

				101101: 2.075 V 101110: 2.100 V 101111: 2.125 V 110000: 2.150 V 110001: 2.175 V 110010: 2.200 V 110011: 2.225 V 110100: 2.250 V 110101: 2.275 V 110110: 2.300 V 110111: 2.325 V 111000: 2.350 V 111001: 2.375 V 111010: 2.400 V 111011: 2.425 V 111100: 2.450 V 111101: 2.475 V 111110: 2.500 V 111111: 2.525 V
	6	R/W	BPERI_EN	0: BUCKPERI disabled 1: BUCKPERI enabled
	7	R/W	BPERI_CONF	0: Supply voltage immediate change 1: Supply voltage preset (activated during power down sequence instead of disable)

Register Address	Bit	Type	Label	Description
R50 LDO1	4:0	R/W	VLDO1	00000: 0.600 V 00001: 0.650 V 00010: 0.700 V 00011: 0.750 V 00100: 0.800 V 00101: 0.850 V 00110: 0.900 V 00111: 0.950 V 01000: 1.000 V 01001: 1.050 V 01010: 1.100 V 01011: 1.150 V 01100: 1.200 V 01101: 1.250 V 01110: 1.300 V 01111: 1.350 V 10000: 1.400 V 10001: 1.450 V 10010: 1.500 V 10011: 1.550 V

				10100: 1.600 V 10101: 1.650 V 10110: 1.700 V 10111: 1.750 V 11000: 1.800 V >11000: 1.800 V
	5	R		Reserved
	6	R/W	LDO1_EN	0: LDO1 disabled 1: LDO1 enabled
	7	R/W	LDO1_CONF	0: Supply voltage immediate change 1: Supply voltage preset (activated during power down sequence instead of disable)

Register Address	Bit	Type	Label	Description
R51 LDO2	5:0	R/W	VLDO2	000000: 0.600 V 000001: 0.625 V 000010: 0.650 V 000011: 0.675 V 000100: 0.700 V 000101: 0.725 V 000110: 0.750 V 000111: 0.775 V 001000: 0.800 V 001001: 0.825 V 001010: 0.850 V 001011: 0.875 V 001100: 0.900 V 001101: 0.925 V 001110: 0.950 V 001111: 0.975 V 010000: 1.000 V 010001: 1.025 V 010010: 1.050 V 010011: 1.075 V 010100: 1.100 V 010101: 1.125 V 010110: 1.150 V 010111: 1.175 V 011000: 1.200 V 011001: 1.225 V 011010: 1.250 V 011011: 1.275 V 011100: 1.300 V 011101: 1.325 V 011110: 1.350 V 011111: 1.375 V

Register Address	Bit	Type	Label	Description
				100000: 1.400 V 100001: 1.425 V 100010: 1.450 V 100011: 1.475 V 100100: 1.500 V 100101: 1.525 V 100110: 1.550 V 100111: 1.575 V 101000: 1.600 V 101001: 1.625 V 101010: 1.650 V 101011: 1.675 V 101100: 1.700 V 101101: 1.725 V 101110: 1.750 V 101111: 1.775 V 110000: 1.800 V >110000: 1.800 V
	6	R/W	LDO2_EN	0: LDO2 disabled 1: LDO2 enabled
	7	R/W	LDO2_CONF	0: Voltage ramped after assertion of VLDO2_GO 1: Supply voltage preset (ramping activated during power down)

Register Address	Bit	Type	Label	Description
R52 LDO3	5:0	R/W	VLDO3	000000: 1.725 V 000001: 1.750 V 000010: 1.775 V 000011: 1.800 V 000100: 1.825 V … 010110: 2.275 V 010111: 2.300 V 011000: 2.325 V 011001: 2.350 V 011010: 2.375 V 011011: 2.400 V 011100: 2.425 V 011101: 2.450 V 011110: 2.475 V 011111: 2.500 V 100000: 2.525 V 100001: 2.550 V 100010: 2.575 V

Register Address	Bit	Type	Label	Description
				100011: 2.600 V 100100: 2.625 V 100101: 2.650 V 100110: 2.675 V 100111: 2.700 V 101000: 2.725 V 101001: 2.750 V 101010: 2.775 V 101011: 2.800 V 101100: 2.825 V 101101: 2.850 V 101110: 2.875 V 101111: 2.900 V 110000: 2.925 V 110001: 2.950 V 110010: 2.975 V 110011: 3.000 V 110100: 3.025 V 110101: 3.050 V 110110: 3.075 V 110111: 3.100 V 111000: 3.125 V 111001: 3.150 V 111010: 3.175 V 111011: 3.200 V 111100: 3.225 V 111101: 3.250 V 111110: 3.275 V 111111: 3.300 V
	6	R/W	LDO3_EN	0: LDO3 disabled 1: LDO3 enabled
	7	R/W	LDO3_CONF	0: Voltage ramped after assertion of VLDO3_GO 1: Supply voltage preset

Register Address	Bit	Type	Label	Description
R53 LDO4	5:0	R/W	VLDO4	000000: 1.725 V 000001: 1.750 V 000010: 1.775 V 000011: 1.800 V 000100: 1.825 V … 010110: 2.275 V 010111: 2.300 V 011000: 2.325 V

Register Address	Bit	Type	Label	Description
				011001: 2.350 V 011010: 2.375 V 011011: 2.400 V 011100: 2.425 V 011101: 2.450 V 011110: 2.475 V 011111: 2.500 V 100000: 2.525 V 100001: 2.550 V 100010: 2.575 V 100011: 2.600 V 100100: 2.625 V 100101: 2.650 V 100110: 2.675 V 100111: 2.700 V 101000: 2.725 V 101001: 2.750 V 101010: 2.775 V 101011: 2.800 V 101100: 2.825 V 101101: 2.850 V 101110: 2.875 V 101111: 2.900 V 110000: 2.925 V 110001: 2.950 V 110010: 2.975 V 110011: 3.000 V 110100: 3.025 V 110101: 3.050 V 110110: 3.075 V 110111: 3.100 V 111000: 3.125 V 111001: 3.150 V 111010: 3.175 V 111011: 3.200 V 111100: 3.225 V 111101: 3.250 V 111110: 3.275 V 111111: 3.300 V
	6	R/W	LDO4_EN	0: LDO4 disabled 1: LDO4 enabled
	7	R/W	LDO4_CONF	0: Supply voltage immediate change 1: Supply voltage preset (activated during power down sequence instead of disable)

Register Address	Bit	Type	Label	Description
R54 LDO5	5:0	R/W	VLDO5	000000: 1.20 V 000001: 1.25 V 000010: 1.30 V 000011: 1.35 V 000100: 1.40 V 000101: 1.45 V 000110: 1.50 V 000111: 1.55 V 001000: 1.60 V 001001: 1.65 V 001010: 1.70 V 001011: 1.75 V 001100: 1.80 V 001101: 1.85 V 001110: 1.90 V 001111: 1.95 V 010000: 2.00 V 010001: 2.05 V 010010: 2.10 V 010011: 2.15 V 010100: 2.20 V 010101: 2.25 V 010110: 2.30 V 010111: 2.35 V 011000: 2.40 V 011001: 2.45 V 011010: 2.50 V 011011: 2.55 V 011100: 2.60 V 011101: 2.65 V 011110: 2.70 V 011111: 2.75 V 100000: 2.80 V 100001: 2.85 V 100010: 2.90 V 100011: 2.95 V 100100: 3.00 V 100101: 3.05 V 100110: 3.10 V 100111: 3.15 V 101000: 3.20 V 101001: 3.25 V 101010: 3.30 V 101011: 3.35 V 101100: 3.40 V 101101: 3.45 V 101110: 3.50 V

				101111: 3.55 V 110000: 3.60 V >110000: 3.60 V
	6	R/W	LDO5_EN	0: LDO5 disabled 1: LDO5 enabled
	7	R/W	LDO5_CONF	0: Supply voltage immediate change 1: Supply voltage preset (activated during power down sequence instead of disable)

Register Address	Bit	Type	Label	Description
R55 LDO6	5:0	R/W	VLDO6	000000: 1.20 V 000001: 1.25 V 000010: 1.30 V 000011: 1.35 V 000100: 1.40 V 000101: 1.45 V 000110: 1.50 V 000111: 1.55 V 001000: 1.60 V 001001: 1.65 V 001010: 1.70 V 001011: 1.75 V 001100: 1.80 V 001101: 1.85 V 001110: 1.90 V 001111: 1.95 V 010000: 2.00 V 010001: 2.05 V 010010: 2.10 V 010011: 2.15 V 010100: 2.20 V 010101: 2.25 V 010110: 2.30 V 010111: 2.35 V 011000: 2.40 V 011001: 2.45 V 011010: 2.50 V 011011: 2.55 V 011100: 2.60 V 011101: 2.65 V 011110: 2.70 V 011111: 2.75 V 100000: 2.80 V 100001: 2.85 V 100010: 2.90 V 100011: 2.95 V

Register Address	Bit	Type	Label	Description
				100100: 3.00 V 100101: 3.05 V 100110: 3.10 V 100111: 3.15 V 101000: 3.20 V 101001: 3.25 V 101010: 3.30 V 101011: 3.35 V 101100: 3.40 V 101101: 3.45 V 101110: 3.50 V 101111: 3.55 V 110000: 3.60 V >110000: 3.60 V
	6	R/W	LDO6_EN	0: LDO6 disabled 1: LDO6 enabled
	7	R/W	LDO6_CONF	0: Supply voltage immediate change 1: Supply voltage preset (activated during power down sequence instead of disable)

Register Address	Bit	Type	Label	Description
R56 LDO7	5:0	R/W	VLDO7	000000: 1.20 V 000001: 1.25 V 000010: 1.30 V 000011: 1.35 V 000100: 1.40 V 000101: 1.45 V 000110: 1.50 V 000111: 1.55 V 001000: 1.60 V 001001: 1.65 V 001010: 1.70 V 001011: 1.75 V 001100: 1.80 V 001101: 1.85 V 001110: 1.90 V 001111: 1.95 V 010000: 2.00 V 010001: 2.05 V 010010: 2.10 V 010011: 2.15 V 010100: 2.20 V 010101: 2.25 V 010110: 2.30 V

Register Address	Bit	Type	Label	Description
				010111: 2.35 V 011000: 2.40 V 011001: 2.45 V 011010: 2.50 V 011011: 2.55 V 011100: 2.60 V 011101: 2.65 V 011110: 2.70 V 011111: 2.75 V 100000: 2.80 V 100001: 2.85 V 100010: 2.90 V 100011: 2.95 V 100100: 3.00 V 100101: 3.05 V 100110: 3.10 V 100111: 3.15 V 101000: 3.20 V 101001: 3.25 V 101010: 3.30 V 101011: 3.35 V 101100: 3.40 V 101101: 3.45 V 101110: 3.50 V 101111: 3.55 V 110000: 3.60 V >110000: 3.60 V
	6	R/W	LDO7_EN	0: LDO7 disabled 1: LDO7 enabled
	7	R/W	LDO7_CONF	0: Supply voltage immediate change 1: Supply voltage preset (activated during power down sequence instead of disable)

Register Address	Bit	Type	Label	Description
R57 LDO8	5:0	R/W	VLDO8	000000: 1.20 V 000001: 1.25 V 000010: 1.30 V 000011: 1.35 V 000100: 1.40 V 000101: 1.45 V 000110: 1.50 V 000111: 1.55 V 001000: 1.60 V 001001: 1.65 V

Register Address	Bit	Type	Label	Description
				001010: 1.70 V 001011: 1.75 V 001100: 1.80 V 001101: 1.85 V 001110: 1.90 V 001111: 1.95 V 010000: 2.00 V 010001: 2.05 V 010010: 2.10 V 010011: 2.15 V 010100: 2.20 V 010101: 2.25 V 010110: 2.30 V 010111: 2.35 V 011000: 2.40 V 011001: 2.45 V 011010: 2.50 V 011011: 2.55 V 011100: 2.60 V 011101: 2.65 V 011110: 2.70 V 011111: 2.75 V 100000: 2.80 V 100001: 2.85 V 100010: 2.90 V 100011: 2.95 V 100100: 3.00 V 100101: 3.05 V 100110: 3.10 V 100111: 3.15 V 101000: 3.20 V 101001: 3.25 V 101010: 3.30 V 101011: 3.35 V 101100: 3.40 V 101101: 3.45 V 101110: 3.50 V 101111: 3.55 V 110000: 3.60 V >110000: 3.60 V
	6	R/W	LDO8_EN	0: LDO8 disabled 1: LDO8 enabled
	7	R/W	LDO8_CONF	0: Supply voltage immediate change 1: Supply voltage preset (activated during power down sequence instead of disable)

Register Address	Bit	Type	Label	Description
R58 LDO9	5:0	R/W	VLDO9	000000: 1.25 V 000001: 1.30 V 000010: 1.35 V 000011: 1.40 V 000100: 1.45 V 000101: 1.50 V 000110: 1.55 V 000111: 1.60 V 001000: 1.66 V 001001: 1.70 V 001010: 1.75 V 001011: 1.80 V 001100: 1.85 V 001101: 1.90 V 001110: 1.95 V 001111: 2.00 V 010000: 2.05 V 010001: 2.10 V 010010: 2.15 V 010011: 2.20 V 010100: 2.25 V 010101: 2.30 V 010110: 2.35 V 010111: 2.40 V 011000: 2.45 V 011001: 2.50 V 011010: 2.55 V 011011: 2.60 V 011100: 2.65 V 011101: 2.70 V 011110: 2.75 V 011111: 2.80 V 100000: 2.85 V 100001: 2.90 V 100010: 2.95 V 100011: 3.00 V 100100: 3.05 V 100101: 3.10 V 100110: 3.15 V 100111: 3.20 V 101000: 3.25 V 101001: 3.30 V 101010: 3.35 V 101011: 3.40 V 101100: 3.45 V 101101: 3.50 V 101110: 3.55 V

				101111: 3.60 V 110000: 3.65 V >110000: 3.65 V
	6	R/W	LDO9_EN	0: LDO9 disabled 1: LDO9 enabled
	7	R/W	LDO9_CONF	0: Supply voltage immediate change 1: Supply voltage preset (activated during power down sequence instead of disable)

Register Address	Bit	Type	Label	Description
R59 LDO10	5:0	R/W	VLDO10	000000: 1.20 V 000001: 1.25 V 000010: 1.30 V 000011: 1.35 V 000100: 1.40 V 000101: 1.45 V 000110: 1.50 V 000111: 1.55 V 001000: 1.60 V 001001: 1.65 V 001010: 1.70 V 001011: 1.75 V 001100: 1.80 V 001101: 1.85 V 001110: 1.90 V 001111: 1.95 V 010000: 2.00 V 010001: 2.05 V 010010: 2.10 V 010011: 2.15 V 010100: 2.20 V 010101: 2.25 V 010110: 2.30 V 010111: 2.35 V 011000: 2.40 V 011001: 2.45 V 011010: 2.50 V 011011: 2.55 V 011100: 2.60 V 011101: 2.65 V 011110: 2.70 V 011111: 2.75 V 100000: 2.80 V 100001: 2.85 V 100010: 2.90 V 100011: 2.95 V

Register Address	Bit	Type	Label	Description
				100100: 3.00 V 100101: 3.05 V 100110: 3.10 V 100111: 3.15 V 101000: 3.20 V 101001: 3.25 V 101010: 3.30 V 101011: 3.35 V 101100: 3.40 V 101101: 3.45 V 101110: 3.50 V 101111: 3.55 V 110000: 3.60 V >110000: 3.60 V
	6	R/W	LDO10_EN	0: LDO10 disabled 1: LDO10 enabled
	7	R/W	LDO10_CONF	0: Supply voltage immediate change 1: Supply voltage preset (activated during power down sequence instead of disable)

Register Address	Bit	Type	Label	Description
R60 SUPPLY	0	R/W	VB_CORE_GO	0: Hold VBUCKCORE at current setting. 1: Ramp BUCKCORE to configured voltage. While the voltage is ramping, write access is blocked to BUCKPRO register. VBUCKCORE_GO is cleared when the target voltage is reached. While ramping, the buck is forced into PWM
	1	R/W	VB_PRO_GO	0: Hold VBUCKPRO at current setting. 1: Ramp BUCKPRO to configured voltage. While the voltage is ramping, write access is blocked to BUCKPRO register. VBUCKPRO_GO is cleared when the target voltage is reached. While ramping, the buck is forced into PWM
	2	R/W	VB_MEM_GO	0: Hold VBUCKMEM at current setting. 1: Ramp BUCKMEM to configured voltage. While the voltage is ramping, write access is blocked to BUCKMEM register. VBUCKMEM_GO is cleared when the target voltage is reached. While ramping, the buck is forced into PWM
	3	R/W	VLDO2_GO	0: Hold LDO2 at current setting. 1: Ramp LDO2 to configured voltage. While the voltage is ramping, write access is blocked to LDO2 register. VLDO2_GO is cleared when the target voltage is reached (ignored if LDO2_CONF was asserted)
	4	R/W	VLDO3_GO	0: Hold VLDO3 at current setting. 1: Ramp VLDO3 to configured voltage. While the

Register Address	Bit	Type	Label	Description
				voltage is ramping, write access is blocked to LDO3 register. VLDO3_GO is cleared when the target voltage is reached (ignored if LDO3_CONF was asserted)
	5	R/W	VPERI_SW_EN	0: Disconnects VPERI_SW pin from buck 1: VPERI_SW closed (controllable from sequencer)
	6	R/W	VMEM_SW_EN	0: Disconnects VMEM_SW pin from buck 1: VMEM_SW closed (controllable from sequencer)
	7	R/W	V_LOCK	0: Allows writing new values into buck and LDO voltage registers 1: Disables voltage re-programming from the host (enable/disable, DVC ramping, power sequencing including deferred update still possible)

Register Address	Bit	Type	Label	Description
R61 PULLDOWN	0	R/W	CORE_PD_DIS	0: Enable pull down resistor 1: No pull down resistor in disabled mode
	1	R/W	PRO_PD_DIS	0: Enable pull down resistor 1: No pull down resistor in disabled mode
	2	R/W	MEM_PD_DIS	0: Enable pull down resistor 1: No pull down resistor in disabled mode
	3	R/W	LDO1_PD_DIS	0: Enable pull down resistor 1: No pull down resistor in disabled mode
	4	R/W	LDO2_PD_DIS	0: Enable pull down resistor 1: No pull down resistor in disabled mode
	5	R/W	LDO5_PD_DIS	0: Enable pull down resistor 1: No pull down resistor in disabled mode
	7:6	R/W		Reserved

17 Programmable Battery Charger

The system power and charger control block contains the following functions:

- Automatic selection of the system power source (VDDOUT) from either the wall charger DCIN, VBUS or VBAT with preference given to DCIN. An Active Diode function allows seamless switching of the power source. The optional external Active Diode controller provides an extended current power path from the battery. The 3-way power path switch supports the automatic power selection from up to two connected external chargers (wall charger/USB charger).
- Battery disconnection switch to allow instant-On system start-up with discharged main battery.
- Independent VBAT tracking mode buck regulator supplying system power out of VBUS with an efficiency > 85 % @ 1000 mA load current.
- Individual programmable current limits for the USB and DCIN supply input.
- Automatic USB Battery Charging Specification Rev.1.0 compliant charger type detection, USB Suspend mode support.
- An autonomous battery charger with pre-configurable current limits and programmable EOC voltages (3.65 V to 4.425 V), current monitoring (always active when the charger is on) and OTP programmable EOC currents.
- Protection against continuous top charging extends battery life (configurable re-charge hysteresis).
- Integrated control over battery pre-charge (including battery pack wake-up), Constant-Current and Constant-Voltage charging phases with die temperature thermal feedback (automatic adjustment to maximum charge rate without overheating).
- Dynamic Charger Current Control (DCCC), providing system power and charging the battery without exceeding the supply current limits.
- Battery temperature qualified charging (using GP-ADC) with default settings loaded from OTP.
- Battery charging termination by current (using GP-ADC) with default setting loaded from OTP.
- Charge current thermal regulation by IC temperature (using GP-ADC).
- Programmable charge termination by timer for safety.

17.1 High Efficiency Charger DC-DC Buck Converter

In order to minimize the total system power loss at high input currents, DA9053's main system power V_{DDOUT} is supplied out of a high efficient DCDC converter, which is able to track V_{BAT}+250 mV (with minimum V_{DDOUT} = 3.75 V).

When powering up V_{DDOUT} the DC-DC converter provides a soft-start circuitry and the current limit is implemented to meet the USB 2.0 specification for currents spikes where charge peaks are always less than an equivalent bypass capacitive load of 10 µF. An integrated over voltage protection and supply selection controls the behaviour of these power paths.

The buck converter operates at a high frequency (2 MHz). This switching frequency is chosen to be high enough to allow the use of a small 2.2 µH or 4.7 µH inductor. To guarantee high efficiency at high load currents the serial resistance of the coil is limited to 100 mΩ (at 1000 mA). Under light load conditions the buck converter can be forced by the host to a low current PFM mode.

17.2 Charger Supply Detection/VBUS Monitoring

DA9053 provides a dual mode charger input VBUS, which can be supplied either from a USB host/hub, a USB type host/hub charger or a dedicated wall charger. To protect DA9053 against destruction from invalid supplies an over voltage protection circuitry will disconnect every charger that supplies more than 5.6 V.

At the VBUS input a connected USB 2.0 compliant host/hub will supply 5 V and is able to provide maximum 100 mA whenever it is operational. A dedicated wall charger or USB host/hub charger has to be differentiated from a USB host/hub because it usually provides charging currents greater 100 mA. DA9053 has therefore a built-in circuitry to detect the attached charger type at VBUS. For a dedicated charger DA9053 has to detect a short between D+ and D- (with a maximum resistance of 200 Ω). From then on the USB charger specification allows the connected charger to charge the device with a current up to 1500 mA. If alternatively the voltage on D- was detected to be less than V_{DAT_REF} (0.25 V to 0.4 V) DA9053 will keep the current limit at 100 mA.

In addition to the combined charger input VBUS DA9053 provides a second charger input DCIN that allows a wall charger to be connected in parallel. This supply will receive priority as soon as it is detected. VCENTER will then be connected to DCIN.

NOTE
The configured default maximum current values have to allow the application being powered completely from the external supply (in the case of a deep discharged battery) but at the same time have to secure that all potential chargers are able to provide the automatically selected maximum average current.

17.3 VBUS Over-Voltage Protection and USB Suspend

DA9053 includes an over-voltage protection circuit that disconnects VBUS or DCIN from the VBUS_PROT and DCIN_PROT inputs via the external P-FETs whenever the VBUS or DCIN voltage is above the threshold. If both inputs are connected to valid supplies DCIN will receive priority and VBUS will be disconnected via the P-FET.

This circuit also supports a USB Suspend mode where the VBUS_PROT path is switched off (disabling the USB charger path) and the VDD_OUT main supply is switched to the battery. Additionally, DA9053 supports a BUS powered low-power mode. In this mode the charger buck is forced to a PFM mode (Sleep mode) to ensure the system is backed up with minimum power dissipation when being supplied from an external supply.

Monitoring of the VBUS and DCIN voltage is always provided, allowing the host processor to detect a removal of the VBUS also in suspend mode. The removal of supplies will issue interrupt requests and trigger a wake-up in POWER-DOWN mode if is still present after a debounce time of 10 ms.

17.4 Battery Pre-Charge Mode

Battery pre-charge mode is started and controlled automatically by DA9053. This is needed to ensure that a completely empty battery can be charged without the intervention of the host processor. In the event of a heavily discharged battery the battery is disconnected from the V_{DDOUT} supply so that the system may be started. The charger then powers the V_{DDOUT} rail from one of the supply paths as described above, allowing the LDOs and buck converter to be switched on.

Pre-charge mode is started when a charger has been detected and V_{DDOUT} is greater than V_{BAT} + 200 mV (or > 3.6 V). The pre-charge mode also handles the re-enable of a battery pack which has had an internal safety switch activated (from deep discharge). The safety switch will be reset by applying a current through the diode in the safety switch, charging the battery cell up to about 2.8 V where the switch will be closed again. DA9053 can optionally drive a flashing LED at GPIO 10 or 11 that will indicate the invisible battery charging until the application is able to power up.

17.5 Fast Linear-Charge Mode

Battery LINEAR-CHARGE mode is initiated automatically once the battery voltage has exceeded the BAT_FAULT threshold for a minimum of 40 ms (to allow a battery safety switch to close)

The linear charge mode has two phases of operation:

1. Constant current (CC) mode.
2. Constant voltage (CV) mode.

If the battery voltage (V_{BAT}) is less than the target voltage, the charging starts in CC mode.

Temperature supervision of the battery by the GP-ADC channel 2 is started and charging is only allowed if the battery temperature is in the correct range. If a TBAT fault condition is detected while charging the battery, charging will be suspend until the battery temperature is back in the correct range, except in the case that the charging end point has been reached.

The CC mode has 64 possible current settings ranging from 30 mA to 1890 mA, controllable by the host processor via the power manager bus. When the battery voltage approaches the target regulation voltage level the charger control loop changes over to CV mode. Note that the CC and CV mode actually operate in parallel, with the CC loop limiting the charging current and the CV loop limiting the charging voltage.

The charging current will be measured automatically by the GP-ADC, generating an average current reading over 10 s period that will be used to determine the charging end point detection. This allows for flexibility in determining when to automatically stop charging for different sizes and types of battery.

17.6 Thermal Charge Current Control

During charging the temperature of DA9053 (Tjunc) is continuously supervised by the GP-ADC against overheating. A thermal supervision circuit reduces the charge current via a current/temperature control whenever the die temperature attempts to rise above a preset value of TCHARGELOW (90 °C). It completely suspends charging when TCHARGESUSPEND (120 °C) has been reached. This protects DA9053 from excessive temperature but allows the application to push the limits of the power handling capability of a given circuit board without risk of damage. Another benefit of the thermal limit is that the charge current can be set according to typical, not worst-case, ambient temperatures for a given application with the assurance that the charger will automatically reduce the current in worst-case conditions.

Whenever the package temperature (Tjunc, see chapter GP-ADC) crosses a threshold from the table below the thermal control will raise the (internal) temperature class and reduce the battery charge current limit towards the related value. It will increase the charge current limit only if the temperature drops below the threshold of the actual class 1. This prohibits a continuous change of the charging current around a temperature threshold.

The thermal charge current control can be disabled but this will increase the risk for a complete thermal shutdown from the internal temperature supervision inside high-power applications.

Table 51: Thermal Charge Current Control

Tjunc (° C)	Class	Charge Current Limit (mA)	ICHG_BAT (Register Value)
<90	0	1890	111111
>90	1	1650	110111
>95	2	1350	101101
>100	3	1050	100011
>105	4	750	011001

>110	5	450	001111
>115	6	Charging suspended	000000

17.7 Dynamic Charging Current Control (DCCC) and Active-Diode

If the combination of the system load plus the battery charging current (pre-charge or fast linear charging) exceeds the charger buck output current (which is limited by the current limitation of the buck) into the VDDOUT node, then the output voltage on VDDOUT will start to drop down to VBAT (which automatically reduces the charging current). When the VDDOUT voltage drops to 3.6 V, and the charger buck is still in current limit, the charging current to the battery will be reduced until it reaches zero or the buck runs below its current limit. Once the VDDOUT is above >3.75 V or the buck runs below its current limit, the charging will be increased until it reaches the programmed setting.

The battery charging control includes an Active-Diode circuit that will automatically provide current to the system if the VDDOUT voltage falls below the VBAT voltage. If large currents or very low resistance in series with the battery output is required the path can be extended by an external power FET using the external Active-Diode controller.

Example of DCCC & Active Diode operation in USB high power mode

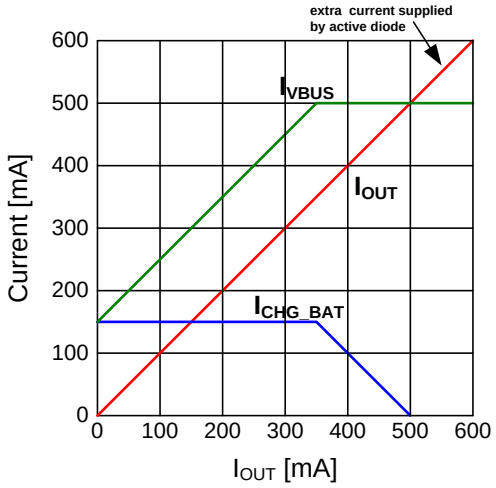

Figure 48: DCCC and Active Diode Operation

17.8 Programmable Charge Termination by Time

The battery charger block will provide a safety timer controlling the maximum time allowed for battery charging. The charge timer is programmable through the power manager bus. The total charge time is defined as the time from when the battery charging was enabled (both for FAST and PRE-CHARGE mode charging). During FAST charge mode the time is dynamically extended whenever the current into the battery is automatically reduced from DCCC or thermal regulation towards less than for example, 50% of the configured maximum charge current. This change in charge time is inversely proportional to the change in charge current. The dynamic safety timer is limited to eight times the programmed clock period and can alternatively be configured towards a fixed timer. If the timer expires (reaches zero) an interrupt request is issued and charging is disabled.

17.9 Backup Battery Charger / Battery Switch

The backup battery charger provides a constant charge current with a programmable top off charging voltage for charging of Lithium-Manganese coin cell batteries and super capacitors. Charging current

is programmable from 100 µA to 1000 µA (in steps of 100 µA) and from 1 mA to 6 mA (in steps of 1 mA). Termination voltage is programmable in 100 mV steps from 1.1 V to 3.1 V. Charging is suspended whenever the termination voltage has been reached and the charging current drops below 50 µA. Charging is re-enabled whenever the backup battery voltage drops 0.2 V below the target termination voltage. It switches off automatically during NO-POWER mode (nPOR asserted).

The function of the battery switch is to provide power to VDD_REF (LDOCORE) from the appropriate battery or supply, depending on conditions as described below.

- If only the backup battery is applied, the switch will automatically connect VDD_REF to this battery. If the power path provides a voltage from the main battery or an external supply that is higher than VBBAT the switch will automatically connect to VDDOUT. During NO-POWER mode VDD_REF will always be disconnected from the backup battery to prohibit a discharge in advance to the initial start-up of the application. If the target voltage of the backup battery is configured lower than VDDCORE the automatic connection of VBBAT to VDD_REF is disabled.
- As the main battery is discharged the system will be warned via the VDDOUT Voltage Supervision with an interrupt. If no action is taken to restore the charge on the main battery and discharging is continued the battery switch will disconnect the input of the LDOCORE (VDD_REF) from the main battery and connect to the backup battery when VDDOUT < VBBAT - 0.2 V. If the application includes no backup battery or the backup battery voltage is configured to be less than LDOCORE (intended to provide only a low voltage RTC supply to the host) the automatic switch to the backup battery can be disabled. Having a typical 3 V backup battery the main battery voltage at which is switched over from main to backup battery is 2.8 V. There is a hysteresis in this switch operation so VDD_REF will not be reconnected to main battery until the main battery voltage is greater than VBBAT (3.0 V) typically.
- The backup battery charger includes a reverse current protection against VDD_REF and can also be used as an ultra-low quiescent ‘always on’ supply for low voltage/power rails (on during RESET mode).

17.10 Battery Charger

Table 52: Charging Control Registers

Register Address	Bit	Type	Label	Description
R62 CHG_BUCK	3:0	R/W	ISET_BUCK	0000: 80 mA 0001: 90 mA 0010: 100 mA 0011: 110 mA 0100: 120 mA 0101: 400 mA 0110: 450 mA 0111: 500 mA 1000: 550 mA 1001: 600 mA 1010: 800 mA 1011: 1000 mA 1100: 1200 mA 1101: 1400 mA 1110: 1600 mA 1111: 1800 mA
	4	R/W	CHG_BUCK_EN	This bit is controlled by the charger state machine. If reset by the host only a charger removal and re-attach starts automatic charger control again. If set to 1 the

				automatic charger control is started immediately.
	5	R/W	CHG_BUCK_LP	When set to 1 the charger buck is forced to the PFM (sleep) mode and charging will be suspended. Automatically cleared when starting charging/re-charging
	6	R/W	CHG_USB_ILIM	0: No automatic USB charger type detection (always use ISET_USB) 1: Automatic USB supply current limit enabled (D+,D- sensing, start with ISET_BUCK)
	7	R/W	CHG_TEMP	0: Thermal charging control disabled 1: Thermal charging control enabled

Register Address	Bit	Type	Label	Description
R63 WAIT_CONT	3:0	R/W	DELAY_TIME	0000: 0 µs 0001: 540 µs 0010: 1.0 ms 0011: 2.0 ms 0100: 4.1 ms 0101: 8.2 ms 0110: 16.4 ms 0111: 32.8 ms 1000: 65.5 ms 1001: 131 ms 1010: 262 ms 1011: 524 ms 1100: 1.0 s 1101: 2.1 s 1110: 4.2 s 1111: Reserved
	4	R/W	EN_32KOUT	0: 32K clock buffer off 1: 32K clock buffer on
	5	R/W	WAIT_MODE	0: Wait for GPIO10 to be active 1: Delay timer mode (start timer and wait for expire)
	6	R/W	RTC_CLOCK	0: No gating of RTC calendar clock 1: Clock to RTC counter is gated until WAIT is asserted
	7	R/W	WAIT_DIR	0: Wait during power-up sequence 1: Wait during power-up and power-down sequence

Register Address	Bit	Type	Label	Description
R64 ISET	3:0	R/W	ISET_USB	0000: 80 mA 0001: 90 mA 0010: 100 mA 0011: 110 mA

				0100: 120 mA 0101: 400 mA 0110: 450 mA 0111: 500 mA 1000: 550 mA 1001: 600 mA 1010: 800 mA 1011: 1000 mA 1100: 1200 mA 1101: 1400 mA 1110: 1600 mA 1111: 1800 mA
	7:4	R/W	ISET_DCIN	0000: 80 mA 0001: 90 mA 0010: 100 mA 0011: 110 mA 0100: 120 mA 0101: 400 mA 0110: 450 mA 0111: 500 mA 1000: 550 mA 1001: 600 mA 1010: 800 mA 1011: 1000 mA 1100: 1200 mA 1101: 1400 mA 1110: 1600 mA 1111: 1800 mA

Register Address	Bit	Type	Label	Description
R65 BAT_CHG	5:0	R/W	ICHG_BAT Note 1	Battery charger current limit (CC) 000000: 0 mA (charging suspended) 000001: 30 mA 000010: 60 mA 000011: 90 mA 000100: 120 mA 000101: 150 mA 000110: 180 mA 000111: 210 mA 001000: 240 mA 001001: 270 mA 001010: 300 mA 001011: 330 mA ... 110111: 1650 mA 111000: 1680 mA 111001: 1710 mA

				111010: 1740 mA 111011: 1770 mA 111100: 1800 mA 111101: 1830 mA 111110: 1860 mA 111111: 1890 mA
	7:6	R/W	ICHG_PRE	Battery pre-charge current limit 00: 0 mA (charging suspended) 01: 20 mA 10: 40 mA 11: 60 mA

Note 1 3-bit trimming are used to adjust the absolute value via OTP.

Register Address	Bit	Type	Label	Description
R66 CHG_CONT	2:0	R/W	VCH_THR	Charger buck reduces the actual current limit if external supply voltage drops below: 000: 3.8 V 001: 4.0 V 010: 4.1 V 011: 4.2 V 100: 4.3 V 101: 4.4 V 110: 4.5 V 111: 4.8 V
	7:3	R/W	VCHG_BAT	Battery charger voltage limit (CV) 00000: 3.650 V 00001: 3.675 V 00010: 3.700 V 00011: 3.725 V 00100: 3.750 V 00101: 3.775 V 00110: 3.800 V 00111: 3.825 V 01000: 3.850 V 01001: 3.875 V 01010: 3.900 V 01011: 3.925 V 01100: 3.950 V 01101: 3.975 V 01110: 4.000 V 01111: 4.025 V 10000: 4.050 V 10001: 4.075 V 10010: 4.100 V (Li-Polymer) 10011: 4.125 V 10100: 4.150 V

				10101: 4.175 V 10110: 4.200 V (Li-Ion) 10111: 4.225 V 11000: 4.250 V 11001: 4.275 V 11010: 4.300 V 11011: 4.3250 V 11100: 4.350 V 11101: 4.375 V 11110: 4.400 V 11111: 4.425 V

Register Address	Bit	Type	Label	Description
R67 INPUT_CONT	3:0	R/W	TCTR Note 1	0000: Charge time out disabled 0001: 30 mins remaining 0010: 60 mins remaining 0011: 90 mins remaining … 1010: 300 mins remaining ... 1111: 450 mins remaining
	4	R/W	VBUS_SUSP	When set to 1, the USB charger path is set into suspend mode, where the power path from VBUS_PROT to VCENTER is switched off. Automatically cleared when USB supply is removed
	5	R/W	DCIN_SUSP	When set to 1, the DCIN charger path is set into disconnect mode, where the power path from DCIN_PROT to VCENTER is switched off. Automatically cleared when DCIN supply is removed
	6	R/W	VCHG_DROP	Charger re-enabled if VBAT drops below VCHG_BAT minus 0: 100 mV 1: 200 mV
	7	R/W	TCTR_MODE	0: Total charge time is extended during periods with reduced charge current 1: Total charge time is fixed

Note 1 Changing the value of TCTR sets the timer to the new value. The timer is paused whenever the ICHG_BAT=0mA. The current timer value can be read from the CHG_TIME register. The timer counts down from the loaded value.

Register Address	Bit	Type	Label	Description
R68 CHG_TIME	7:0	R	CHG_TIME	Remaining minutes until charging time out 00000000: Charging ended 00000001: 2 mins remaining 00000010: 4 mins remaining

				... 11111111: 510 mins remaining

17.11 Backup Battery Charger

Table 53: Backup Battery Charging Control Registers

Register Address	Bit	Type	Label	Description
R69 BBAT_CONT	3:0	R/W	BCHARGER_VSET	0000: disabled 0001: 1.1 V 0010: 1.2 V 0011: 1.4 V 0100: 1.6 V 0101: 1.8 V 0110: 2.0 V 0111: 2.2 V 1000: 2.4 V 1001: 2.5 V 1010: 2.6 V 1011: 2.7 V 1100: 2.8 V 1101: 2.9 V 1110: 3.0 V 1111: 3.1 V
	7:4	R/W	BCHARGER_ISET	0000: disabled 0001: 100 µA 0010: 200 µA 0011: 300 µA 0100: 400 µA 0101: 500 µA 0110: 600 µA 0111: 700 µA 1000: 800 µA 1001: 900 µA 1010: 1 mA 1011: 2 mA 1100: 3 mA 1101: 4 mA 1110: 5 mA 1111: 6 mA

17.12 White LED Driver and Boost Converter

DA9053 will provide the capability for supplying the power for at least 5 white LEDs in series. Using the components described in this datasheet to drive three independent strings of 5 LEDs the inductive boost converter will provide around 24 V at a forward current of max.78mA. (To handle strings of greater than 5 LEDs higher voltages are also possible also by using lower voltages to driving fewer than 5 LEDs more than 50 mA will be possible by choosing different external components, please contact your Dialog representative for specific cases). The regulation scheme will ensure that the correct voltage is generated for the series connected LEDs. This is achieved by controlling the output voltage of the boost converter such that the lowest voltage at the control loop enabled pins LED1_IN / LED2_IN / LED3_IN exceeds a threshold voltage of approx. 0.7 V at the programmed current. The over voltage protection will protect the block from a disconnected load, limiting the output voltage of the Boost converter. The over voltage protection threshold is defined by an external voltage divider compared with a reference voltage of 1.41 V. Whenever over voltage is detected or the current through the inductor gets larger than the maximum configured limit, the boost switches off.

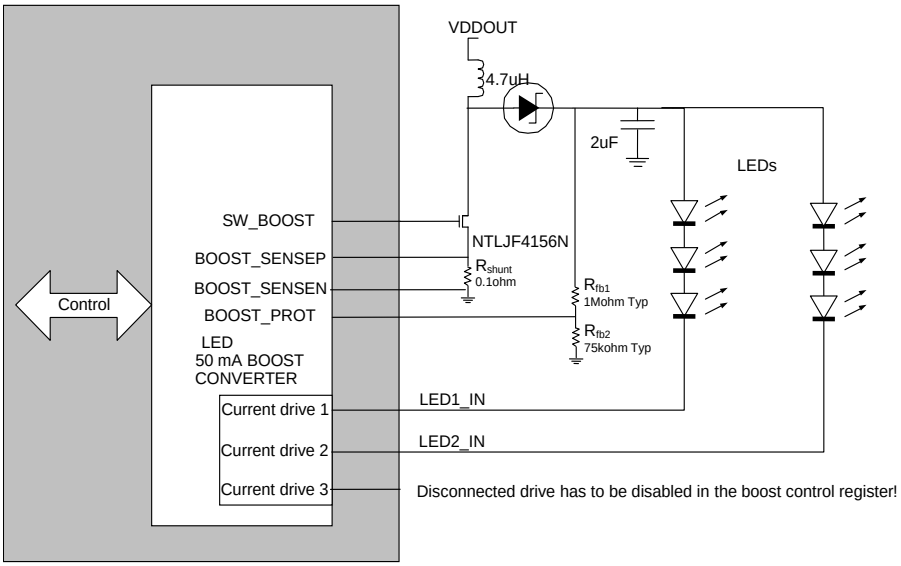

Figure 49: Example of White LED Backlight Application

Each white LED output driver will have a programmable logarithmic IDAC with 256 steps to set the output current. The dynamic range is 50 µA to 26 mA resulting towards a step multiplication of the “255th root of 520”. All three drivers will have individual controls to enable a LED current ramping with 1ms per step. The relative matching of identical configured IDACs is designed to be within the range of +/-3.25% at full current.

NOTE
All LEDx_IN ports that are connected (via LED) to a voltage rail potentially >5.5 V have to be enabled at a current level that protects the port against high voltages. If a current drive input is not connected to the boost, its regulation has to be disabled in the control register allowing an enabled boost to stop increasing at the intended voltage level. Disabling the current sink without disabling it for the boost control will potentially damage the current drive. It is mandatory to prohibit voltages higher than 5.5 V at the current sink inputs. A balanced configuration is recommended with a similar type and number of LEDs and a similar current for the connected LED strings. Always enable all connected current sinks BEFORE enabling the boost.

The current sinks offer a PWM control. The generated PWM signal is of duty cycle from 16 to 100%, with a repetition frequency of 21 kHz and 95 steps (using 2 MHz clock for each step). A PWM ratio greater than 95 results in the output switch being permanently closed. During the duty cycle the current sinks use the individual configured current setting. The low level current of the PWM

controlled LED strings is common. The PWM control can also be made to dim between its actual value and a new value at a rate of 40ms per step. When set to zero the PWM ratio will change immediately.

NOTE
It is strongly recommended that PWM controlled LED strings, which are enabled for the boost control loop are configured balanced with identical PWM duty cycle and high level current settings. If boost driven strings contain more than 4 LEDs small current deltas or a current ramping are highly recommended because an immediate switch to very low currents can already generate critical input voltages at the current sinks.

LED3 includes a PWM-only mode (no current control) which automatically disables the LED3 input towards the boost control with a duty cycle from 0 to 100%. In conjunction with the GPIO 14 and 15 this offers a common anode tricolour LEDs brightness control. This mode is intended to drive a single LED from supply voltages below 5.5 V and requires an appropriate serial resistor.

NOTE
The efficiency of the boost converter is dominated by the external losses. To achieve a good efficiency, the coil, diode and transistor losses should be minimized. 2 MHz mode will achieve lowest current ripple but especially for low output currents 1 MHz will provide better efficiency.

17.13 Boost and LED Driver

Table 54: Boost and LED Driver Control Registers

Register Address	Bit	Type	Label	Description
R70 BOOST	0	R/W	BOOST_EN	0: Boost converter disabled 1: Boost converter enabled
	1	R/W	LED1_IN_EN	0: LED1 input is disabled for boost voltage control (mandatory, if not connected to boost) 1: LED1 is included for lowest input voltage
	2	R/W	LED2_IN_EN	0: LED2 input is disabled for boost voltage control (mandatory, if not connected to boost) 1: LED2 is included or lowest input voltage
	3	R/W	LED3_IN_EN	0: LED3 input is disabled for boost voltage control (mandatory, if not connected to boost) 1: LED3 is included for lowest input voltage
	4	R/W	BOOST_ILIM	0: 710 mA Boost current limitation 1: 1000 mA Boost current limitation
	5	R/W	BOOST_FRQ	0: 1 MHz Boost switching frequency 1: 2 MHz Boost switching frequency
	6	R/W	M_B_FAULT	Mask boost failure caused nIRQ
	7	R	E_B_FAULT	If set boost the over voltage or over current limitation triggered an error event

Register Address	Bit	Type	Label	Description
R71 LED_CONT	0	R/W	LED1_EN	0: LED1 current sink disabled, LED1_IN_EN is automatically set to zero 1: LED1 current sink enabled
	1	R/W	LED1_RAMP	0: No LED1 current ramping 1: New target LED1 current will be adjusted by ramping (1 step/1ms)
	2	R/W	LED2_EN	0: LED2 current sink disabled, LED2_IN_EN is automatically set to zero 1: LED2 current sink enabled
	3	R/W	LED2_RAMP	0: No LED2 current ramping 1: New target LED2 current will be adjusted by ramping (1 step/1ms)
	4	R/W	LED3_EN	0: LED3 current sink disabled, LED3_IN_EN is automatically set to zero 1: LED3 current sink enabled
	5	R/W	LED3_RAMP	0: No LED3 current ramping 1: New target LED3 current will be adjusted by ramping (1 step/1ms)
	6	R/W	LED3_ICONT	0: LED3 is PWM-only controlled (GPIO14/15 mode), LEDMIN_CURRENT and LED3_CURRENT are not used, LED3_EN and LED3_IN_EN are automatically set to zero 1: LED3 is current controlled (LED1/2 mode)
	7	R/W	SEL_LED_MODE	0: Reserved 1: The boost is in current driving mode

Register Address	Bit	Type	Label	Description
R72 LEDMIN_123	7:0	R/W	LEDMIN_CURRENT	LED1/2/3 current value during PWM idle time: 00000000: 50.0 µA 00000001: 51.2 µA (+0.213 dB) 00000010: 52.5 µA (+0.213 dB) ... 11111111: 26000 µA

Register Address	Bit	Type	Label	Description
R73 LED1_CONF	7:0	R/W	LED1_CURRENT	LED1 current value: 00000000: 50.0 µA 00000001: 51.2 µA (+0.213 dB) 00000010: 52.5 µA (+0.213 dB) ... 11111111: 26000 µA

Register Address	Bit	Type	Label	Description
R74 LED2_CONF	7:0	R/W	LED2_CURRENT	LED2 current value: 00000000: 50.0 µA 00000001: 51.2 µA (+0.213 dB) 00000010: 52.5 µA (+0.213 dB) ... 11111111: 26000 µA

Register Address	Bit	Type	Label	Description
R75 LED3_CONF	7:0	R/W	LED3_CURRENT	LED3 current value: 00000000: 50.0 µA 00000001: 51.2 µA (+0.212 dB) 0000010: 52.5 µA (+0.212 dB) ... 11111111: 26000 µA

Register Address	Bit	Type	Label	Description
R76 LED1_CONT	6:0	R/W	LED1_PWM	LED1 intensity control in periods of 2 MHz clock (period 21 kHz = 95 cycles) 0000000: off 0000001: 1 % (not used) .... 0001111: 15 % (not used) 0010000: 16 % .... 1011111: 100 % >1011111: 100 % LED1_CURRENT is used during the duty cycle. During idle times the alternate current is taken from LEDMIN_CURRENT.
	7	R/W	LED1_DIM	0: LED1 PWM ratio changes instantly 1: LED1 ramps between changes in PWM ratio with 40 ms per step

Register Address	Bit	Type	Label	Description
R77 LED2_CONT	6:0	R/W	LED2_PWM	LED2 intensity control in periods of 2 MHz clock (period 21 kHz = 95 cycles) 0000000: off 0000001: 1 % (not used) .... 0001111: 15 % (not used) 0010000: 16 %

				.... 1011111: 100 % >1011111: 100 % LED2_CURRENT is used during the duty cycle. During idle times the alternate current is taken from LEDMIN_CURRENT.
	7	R/W	LED2_DIM	0: LED2 PWM ratio changes instantly 1: LED2 ramps between changes in PWM ratio with 40 ms per step

Register Address	Bit	Type	Label	Description
R78 LED3_CONT	6:0	R/W	LED3_PWM	LED3 intensity control in periods of 2 MHz clock (period 21 kHz = 95 cycles) 0000000: off 0000001: 1 % (not used if current controlled) .... 0001111: 15 % (not used if current controlled) 0010000: 16 % .... 1011111: 100 % >1011111: 100 % LED3_CURRENT is used during the duty cycle. During idle times the alternate current is taken from LEDMIN_CURRENT (LED1/2 mode). If LED3_ICONT is not asserted the current control with be disabled and the output will be just switched on and off (GPIO14/15 mode).
	7	R/W	LED3_DIM	0: LED3 PWM ratio changes instantly 1: LED3 ramps between changes in PWM ratio with 40ms per step

Register Address	Bit	Type	Label	Description
R79 LED4_CONT	6:0	R/W	LED4_PWM	GPIO14 LED on-time (low level at GPIO 14, period 21 kHz = 95 cycles of 0.5 µs) 0000000: off 0000001: 1 % 0000010: 2 % (1 µs bursts) 0000011: 3 % 0000100: 4 % 0000101: 5 % 0000110: 6 % 0000111: 7 % 0001000: 8 % 0001001: 9 % 0001010: 10 %

				0001011: 11 % 0001100: 12 % 0001101: 13 % 0001110: 14 % 0001111: 15 % 0010000: 16 % .... 1011111: 100 % >1011111: 100 %
	7	R/W	LED4_DIM	0: LED4 PWM ratio changes instantly 1: LED4 ramps between changes in PWM ratio with 40 ms per step

Register Address	Bit	Type	Label	Description
R80 LED5_CONT	6:0	R/W	LED5_PWM	GPIO15 LED on-time (low level at GPIO 15, period 21 kHz = 95 cycles of 0.5 µs)) 0000000: off 0000001: 1 % 0000010: 2 % (1 µs bursts) 0000011: 3 % 0000100: 4 % 0000101: 5 % 0000110: 6 % 0000111: 7 % 0001000: 8 % 0001001: 9 % 0001010: 10 % 0001011: 11 % 0001100: 12 % 0001101: 13 % 0001110: 14 % 0001111: 15 % 0010000: 16 % .... 1011111: 100 % >1011111: 100 %
	7	R/W	LED5_DIM	0: LED5 PWM ratio changes instantly 1: LED5 ramps between changes in PWM ratio with 40 ms per step

18 Monitoring ADC and Touch Screen Interface

18.1 ADC Overview

The DA9053 provides an Analog to Digital Converter (ADC) with 10-bits resolution and track and hold circuitry combined with an analog input multiplexer. The analog input multiplexer will allow conversion of up to 10 different inputs. The track and hold circuit ensures stable input voltages at the input of the ADC during the conversion.

The ADC is used to measure the following inputs:

- Channel 0: VDDOUT – measurement of the system voltage
- Channel 1: ICH – internal battery charger current measurement
- Channel 2: TBAT – output from the battery NTC
- Channel 3: VBAT – measurement of the battery voltage
- Channel 4: ADC_IN4 – high impedance input (0 V to 2.5 V)
- Channel 5: ADC_IN5 – high impedance input (0 V to 2.5 V)
- Channel 6: ADC_IN6 – high impedance input (input divider, 0 V to 2.5 V)
- Channel 7: XY– TSI interface to measure the X and Y voltage of the touch screen resistive potentiometers
- Channel 8: internal Tjunc.-sense (internal temp. sensor)
- Channel 9: VBBAT – measurement of the backup battery voltage

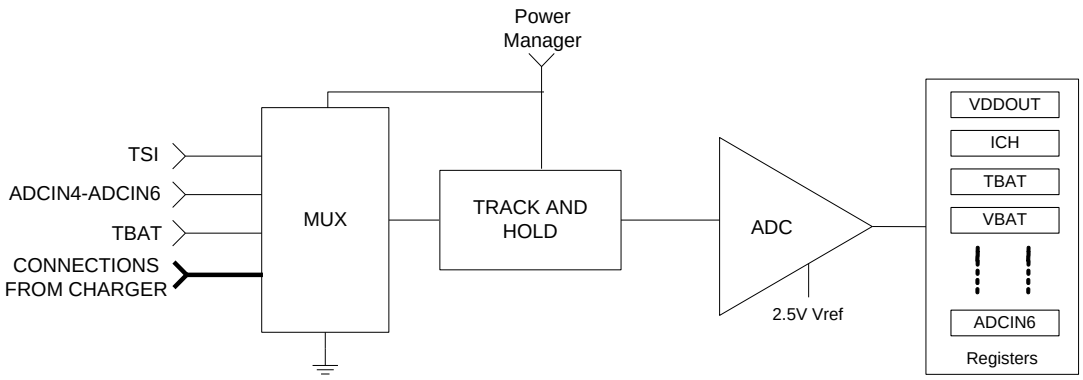

Figure 50: ADC Block Diagram

18.2 Input MUX

The MUX selects from and isolates the 10 inputs and presents the channel to be measured to the ADC input. When selected, an input amplifier on the VDDOUT (and VBAT) channel subtracts the VDDCORE reference voltage and scales the signal to the correct value for the ADC.

18.3 ADC

The ADC uses a sample and hold successive approximation switched capacitor architecture. It is supplied from internal core supply rail VDDCORE (2.5 V). It can be used either in high speed mode with measurements sequences repeated every 1ms or in economy mode with sequences performed every 10ms.

18.4 Manual Conversion Mode

For manual measurements the ADC powers up, one conversion is done on the specified channel and the 10-bit result is stored. After the conversion is completed, the ADC powers down again and an IRQ event flag is set (end of manual conversion). The generation of this IRQ can be masked by the IRQ mask.Note: the IRQ must be cleared before subsequent manual measurements can be made.

18.5 Automatic Measurements Scheduler

The automatic measurement scheduler allows monitoring of the system voltage VDDOUT, the charging current ICH, the battery temperature TBAT and the touch screen interface XY. Additionally, the auxiliary channels ADCIN4-6 are able to be automatically monitored with upper and low thresholds set by power manager registers to give a nIRQ event if a measurement is outside these levels. All measurements are handled by the scheduler system detailed below.

The scheduler performs a sequence of 10 slots continually repeated according to the configured mode. If the TSI is enabled the first half slot performs either an automatic or a manual conversion. The second half slot performs TSI actions and measurements. If the TSI measurement is disabled there is no split of the slot and only the first conversion is performed. A slot requires 100µs. The pattern of measurements over the 10 slots depends upon the charging mode. Automatic measurements of VDDOUT, ICH and TBAT are made during charging. These cease when not charging. When automatic measurements are disabled, the manual measurements are made immediately and unused automatic measurements will handle manual conversion requests.

The action of each automatic measurement follows. Beside the TSI automatic measurements only store the 8MSB's of the ADC measurement.

Example sequence of AUTO-ADC measurements

Slot No	0		1		2		3		4		5		6		7		8		9		
	A0	X	M	Y	M	Z	A4	P	M	X	M	Y	A5	P	M	X	M	Y	A6	P	TSI, no charging, TSI_DELAY<=1, TSI_SKIP=0
	A0	X	A1	Y	M	Z	A4	P	A2	-	M	-	A5	X	A6	Y	M	P	A8	-	TSI, with charging TSI_DELAY<=1, TSI_SKIP=2 slots
	A0		M		M		A4		M		M		A5		M		M		A6		No TSI, no charging
	A0		A1		M		A4		A2		M		A5		A6		M		A8		No TSI, with charging

Each Slot allows 1 automatic or manual measurement and 1 TSI measurement to be made
A0 - Automatic measurement of VDDOUT (mux channel 0)
A1 - Automatic measurement of ICH (mux channel 1)
A2 - Automatic measurement of TBAT (mux channel 2)
A4 - Automatic measurement of ADCIN4 (mux channel 4)
A5 - Automatic measurement of ADCIN5 (mux channel 5)
A6 - Automatic measurement of ADCIN6 (mux channel 6)
A8 - Automatic measurement of Tjunc with gain 3 (mux channel 8)
TSI - Automatic X&Y(&Z) measurement followed by a pen detection (mux channel 7)
M indicates time slots when a Manual measurement can be made

Figure 51: Example Sequence of AUTO-ADC Measurements

18.6 A0: VDDOUT Low Voltage nIRQ Measurement Mode

VDDOUT is measured and compared with a threshold. If the reading is below this level for a number of three consecutive readings an error event is generated. If nIRQ was asserted the automatic measurement of channel VDDOUT is paused until the host has cleared the associated event flag (the event causing value is kept inside the result register). If no action is taken to restore the VDDOUT voltage (discharging the battery is continued) the host may consider to switch off optional

'Always on' blocks (backup battery charger or supplies, that are not disabled when powering down to RESET mode) to save energy later on. The multiple reading provides a debouncing of the VDDOUT voltage before issuing a nIRQ. The assertion of nIRQ can be masked by IRQ mask.

18.7 A1: ICH (and ICH_BAT Average) Measurement Mode

When the battery is being charged in FAST CHARGE mode the ICH current is measured automatically every 1 ms or 10 ms and an average value is determined by adding the result to an 18-bit accumulator and latching the top eight bits every 1024 samples (during high speed mode nine measurements are ignored before performing an update). This provides an average charging current value every 10.24 s. When the ICH_BAT falls below the value set (and the other requirements for charging end detect are met), an IRQ will be flagged. The IRQ can be masked.

18.8 A2: TBAT and Battery Temperature Warning nIRQ Measurement Mode

When the battery is being charged, the TBAT voltage is measured automatically. During this measurement, a 50 µA current is sourced to the battery temperature sense resistor from the TBAT pin. During production testing, the TBAT high and low thresholds are programmed into the OTP memory, with adjustments made to correct for the accuracy of the 50 µA current source and the high and low temperature resistance of the NTC resistor etc. The measurement result is used to protect the battery pack from damage during charging at too high temperatures. Temperature is flagged by three threshold levels held in the threshold registers (loaded from OTP at start-up). If three consecutive readings of TBAT are outside the configured range, then charging is disabled, an event flag is set and an interrupt is generated. The processor can then either service the IRQ and turn off charging or do nothing. If nothing is done, the FAST CHARGE block will start charging again as soon as the temperature readings are inside the programmed range. The generation of this IRQ can be masked.

18.9 A4, A5, A6: Automatic Measurement and High/Low Threshold Warning nIRQ Mode

The automatic measurement result of channel ADC_IN4 is stored. If a reading of A4 outside the programmed range then an event flag is set. If nIRQ was asserted the automatic measurement of channel ADC_IN4 is paused until the host has cleared the associated event flag (the event causing value is kept inside the result register). If debouncing is selected the event will only be asserted if two consecutive measurements override the same threshold. The assertion of nIRQ can be masked by IRQ mask. The same functionality is available at ADC_IN5 and ADC_IN6. In addition it is possible to use ADCIN_4 with a 15 µA current source that allows automatic measurement of a resistor value. During automatic measurements the enabled current source is dynamically switched-off at the end of the conversion and switched-on one slot prior to the next ADCIN_4 measurement (to enable minimum current consumption, but external capacitance to settle); otherwise its status is static.

18.10 A8: Automatic Measurement of Internal Temperature

Selection of channel 8 (Tjunc) will be used to measure the output of the internal temperature sensor generated out of a PTAT current from the BGR. The channel 8 measures the output of the temperature sensor with a gain of 3. An offset register can be used for a one point calibration of the temperature sensor.

18.11 A3, A9: Manual Measurement VBAT and VBBAT

Channel 3 can be used to manually measure the main battery voltage and channel 9 can be used to measure the voltage of the backup battery.

18.12 Fixed Threshold Non-ADC Warning nIRQ Mode

A comparator with a threshold of VDD_REF (1.2 V) is connected to the input of channel 5. The comparator is asserted whenever the input voltage is excessing or dropping below 1.2 V for at least 10ms (debouncing) when being enabled via COMP1V2_EN. A status-flag COMP_DET is indicating the actual state and a mask able interrupt request E_COMP_1V2 is generated at falling and rising edge state transitions. The comparator has to be disabled via COMP1V2_EN when auto measurements with high resolution are executed on ADCIN5.

18.13 A7: XY Touch Screen Interface

The TSI operates as a sub-system within the scheduler, using the slots to step through tasks such as; pen down detection, matrix switching and settling, and X (one-dimensional resistor network) or XY measurements including pen pressure (Z).

18.13.1 Features

- Compatible with 4-wire resistive touch screens and supports pen pressure measurement
- Unidirectional resistor network measurements (XP mode)
- X+, X-, Y+, Y- inputs can be alternatively used for multiplexed manual measurements on GP-ADC channel 7
- Pen detection, pen controlled automatic measurements and nIRQ generation with application wake-up
- Supports configurable low-power schemes
- Includes TSI pre-charging (to compensate external noise reduction capacitors) and TSI settling to let mechanical vibration of TSI layer sheet stabilize prior to measurement

Maximum X&Y sample rate: 3 kHz (pen pressure: 1 kHz)

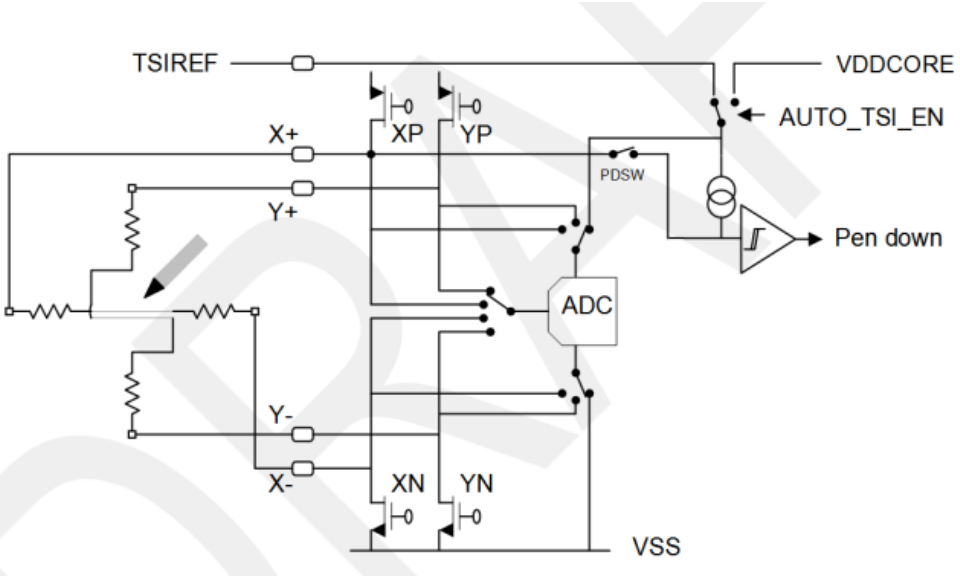

Figure 52: TSI Switch Matrix

18.14 Pen Down Detect

Whenever the screen is touched outside of autonomous TSI sequences (AUTO_TSI_EN is released) the pen detection will issue an interrupt and will trigger a wake up from POWER-DOWN mode. An autonomous start of configured TSI sequences (XYZ or X mode) can be armed in parallel to

PEN_DET_EN (requires a valid supply voltage at TSIREF); otherwise the host has to start the TSI measurements by asserting AUTO_TSI_EN. For a single sequence of X&Y&Z&P (or X&P) the host has to disable AUTO_TSI_EN when receiving the E_TSI_READY interrupt request.

For pen detection the YN switch is closed, grounding the Y plate. The XP signal is internally connected by switch PDSW to a current source. When the screen is touched, the formed conducting path steers the current to ground and a low voltage triggers an interrupt request. When pen detect is blocked the PDSW is opened to isolate the current from the resistor matrix and ADC. As long as only the pen detection is running the current source is supplied from VDDCORE (2.5 V). Otherwise the supply will be switched to TSIREF which should be connected to LDO9 or a similar high precision regulator.

18.15 TSI Scheduler

The TSI measurement circuitry is supplied from TSIREF. When measuring the X position the X- switch is closed (grounding the X plane), the X+ switch is closed (charging the X plane) and later the Y+ signal is connected to the ADC input for measurement. When measuring the Y position the Y- switch is closed (grounding the Y plane), the Y+ switch is closed (charging the Y plane) and later the X+ signal is connected to the ADC input.

The TSI function operates every half-slot of the scheduler, performing automatic X, Y, Z (and pen detect) measurements of the touch screen resistive potentiometer. The resulting XYP or XYZP (XP) measurements are then available from the distributed TSI_X & TSI_Y (and (TSI_Z) registers. Whenever a XYP or XYZP (or alternatively XP) data block is ready an interrupt is generated to inform the host about new data to be read. The registers latch the results for all three/four values to ensure an autonomic data read, given that a new measurement may become available whilst reading the multiple registers.

Filtering of LCD noise is handled by external capacitors connected from each TSI pin to ground. A low pass filter is formed with the touch screen resistance that forces a longer settling time prior to ADC sampling. The time between switching and measurement conversion is handled by control bits.

To reduce power consumption the data block measurement can be made intermittently. The gap between actual measurements specifies a delay in multiples of slot time. A value of zero indicates the XYP, XYZP (or XP) block measurements are continually repeated. Otherwise the specified number of slots is skipped in advance to the next XYP, XYZP (or XP) measurement.

In summary a settling delay precedes an X measurement, followed by a settling delay preceding a Y measurement, which is performed identical to the Z and pen detection measurements. A number of slots are missed between a pair of XYP, XYZP (or XP) block measurements. Figure 53shows an example sequence explaining TSI_DELAY (2 slots) and TSI_SKIP (2 slots) in XP mode.

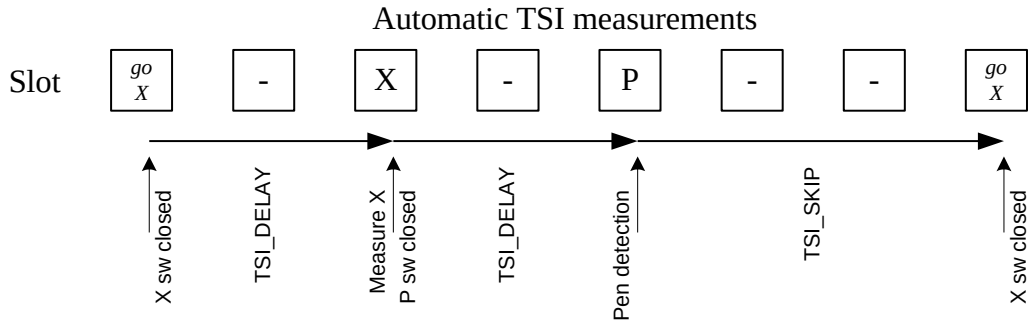

Figure 53: Example Sequence in XP Mode

18.16 Pen Pressure

When measuring Z the X- switch is closed (grounding the X plane), the Y+ switch is closed (charging the Y plane) and the X+ signal is later then connected to the ADC input for measuring the value.

The pen pressure can then be estimated from the touch resistance Pressure which has to be calculated by the host from the measured X, Y and Z values and the known resistance values of the TSI X- and Y-plates (Rx and Ry).

Manual measurements can be executed by asserting TSI_MAN. If asserted in combination with AUTO_TSI_EN = 1 it forces the immediate single TSI measurement selected within TSI_MODE (not waiting for an activate pen detection). If AUTO_TSI_EN = 0 all TSI input channels can be used as further general purpose inputs routed via TSI_MUX to ADC channel 7. In combination with the assertion of TSI_SEL_0 to TSI_SEL_3 this interface mode supports a wide range of host controlled voltage/impedance measurements with ADC channel 7.

Table 55: Registers Summary

Name (bits)	Description
AUTO_TSI_EN	Touch screen block enable. Regular measurements of X-Y and pen detection are scheduled.
PEN_DET_EN	Enables pen detection mode.
TSI_MODE	0: XYZP mode (X&Y&Z plus two X&Y measurement, each followed by a pen detection) 1: XP mode (X measurements followed by a pen detection)
E_PEN_DOWN	Pen touch detected. Set when pen touch down, else reset. Flags nIRQ and wake up with current value shown in status registers.
E_TSI_READY	Interrupt request. Cleared by reading event register.
M_TSI_READY	Interrupt request mask. Set to 1 to disable interrupt.
M_PEN_DOWN	Interrupt request mask. Set to 1 to disable interrupt.
TSI_XM, TSI_YM, TSI_XL,TSI_YL, TSI_ZL, PEN_DOWN TSI_Z	Touch screen X, Y and Z readings: R107: TSI_X bits 9:2 R107+1: TSI_Y bits 9:2 R107+2: TSI_X bits 1:0, TSI_Y bits 1:0, TSI_Z bits 1:0, PEN_DOWN R107+3: TSI_Z bits 9:2 (used to calculate the pen pressure) To ensure a synchronous data read, the assertion of the TSI_READY event latches the latest X&Y (and Z) measurements. The values at addresses R107, R107+1 & R107+2 (& R107+3 in XYZP mode) can then be safely read until the event was cleared by the host, even if another TSI measurement has occurred in the elapsed time between reads. The addresses are sequential, allowing a 3 or 4 word page mode 2-wire read.
TSI_DELAY	Delay between closing X and Y switches and ADC conversion: 0=0 slot: Switches closed only for ADC conversion. This allows 6 µs for settling. 1=1 slot, 2=2 slots, 3=4 slots Switches are set at the end of ADC conversion, reading occurs in next slot and the pattern repeats. Delay of 1 slot enables continuous X, Y, Z (and P) readings.
TSI_SKIP	Delay between two measurements (X&Y or X&Y&Z) where no TC measurements are made (between X values for XP mode). During this period the switches are open and no current is flowing through the screen so reducing average current consumption. 0 = Continuous operation. 1 = 2 slot, 2 = 5 slot, 3 = 10 slot, 4 = 30 slot, 5 = 80 slot, 6 = 130 slot, 7 = 330

	slot.
TSI_MAN	When set with AUTO_TSI_EN released, the following registers override the normal operation.
TSI_SEL_0 TSI_SEL_1 TSI_SEL_2 TSI_SEL_3	Direct setting of XY switches: 0 = Open X+, 1 = Close X+ 0 = Open X-, 1 = Close X- 0 = Open Y+, 1 = Close Y+ 0 = Open Y-, 1 = Close Y-
TSI_MUX	Direct setting of MUX selecting which XY pin is routed to GPADC_IN7 input. Depending on the MUX settings the result will be available either in the TSI_X or TSI_Y registers named in brackets: 00 = X+ (TSI_XM, TSI_XL) 01 = Y+ (TSI_YM, TSI_YL) 10 = X- (TSI_XM, TSI_XL) 11 = Y- (TSI_YM, TSI_YL)
ADCREF	ADC reference connection. 0 = TSIREF/VSS 1 = X+/X-, Y+/Y- or Y+/X- depending on the channel being measured (X/Y/Z)

18.17 GP-ADC

Table 56: GP-ADC Control Registers

Register Address	Bit	Type	Label	Description
R81 ADC_MAN	3:0	R/W	MUX_SEL	0000: VDDOUT pin (channel 0) selected 0001: ICH (channel 1) selected 0010: TBAT pin (channel 2) selected 0011: VBAT pin (channel 3) selected 0100: ADCIN4 selected 0101: ADCIN5 selected 0110: ADCIN6 selected 0111: TSI (channel 7) selected) 1000: internal T-Sense using gain 1 (channel 8) selected 1001: VBBAT-voltage
	4	R/W	MAN_CONV	Perform manual conversion. Bit is reset to 0 when conversion is complete.
	7:5	R		

Register Address	Bit	Type	Label	Description
R82 ADC_CONT	0	R/W	AUTO_VDD_EN	0: VDDOUT auto measurements disabled 1: VDDOUT auto measurements enabled
	1	R/W	AUTO_AD4_EN	0: ADCIN4 auto measurements disabled 1: ADCIN4 auto measurements enabled

	2	R/W	AUTO_AD5_EN	0: ADCIN5 auto measurements disabled 1: ADCIN5 auto measurements enabled
	3	R/W	AUTO_AD6_EN	0: ADCIN6 auto measurements disabled 1: ADCIN6 auto measurements enabled
	4	R/W	AD4_ISRC_EN	0: Disable ADCIN4 15 µA current source 1: Enable ADCIN4 15 µA current source
	5	R/W	TBAT_ISRC_EN	0: TBAT 50 µA current source enabled one slot before measurement (disabled after measurement) 1: Enable TBAT 50 µA current source permanently
	6	R/W	ADC_MODE	0: Measurement sequence interval 10 ms (economy mode) 1: Measurement sequence interval 1 ms (recommended for TSI mode)
	7	R/W	COMP1V2_EN	0: Disable 1.2 V comparator at ADCIN5 1: Enable 1.2 V comparator

Register Address	Bit	Type	Label	Description
R83 ADC_RES_L	1:0	R	ADC_RES_LSB	10-bit manual conversion result (2 LSBs)

Register Address	Bit	Type	Label	Description
R84 ADC_RES_H	7:0	R	ADC_RES_MSB	10-bit manual conversion result (8 MSBs)

Register Address	Bit	Type	Label	Description
R85 VDD_RES	7:0	R	VDDOUT_RES	0x00 – 0xFF: Auto VDDOUT conversion result (ADCIN0) 00000000 corresponds to 2.5 V 11111111 corresponds to 4.5 V

Register Address	Bit	Type	Label	Description
R86 VDD_MON	7:0	R/W	VDDOUT_MON	VDDOUT_MON threshold setting (8-bit). 00000000 corresponds to 2.5 V 11111111 corresponds to 4.5 V

Register Address	Bit	Type	Label	Description
R87 ICHG_AV	7:0	R	ICHG_AV	Charger current average conversion result, 8 MSBs from an internal 18-bit accumulator, updated every 10.24 s:

				00000000 corresponds to 0 mA, 11111111 corresponds to 1000 mA

Register Address	Bit	Type	Label	Description
R88 ICHG_THD	7:0	R/W	ICHG_THD	Reduced Battery charging current detection threshold (compared with ICHG_AV) 00000000 corresponds to 0 mA, 11111111 corresponds to 1000 mA

Register Address	Bit	Type	Label	Description
R89 ICHG_END	7:0	R/W	ICHG_END	Battery charging end point current detection threshold (compared with ICHG_AV) 00000000 corresponds to 0 mA, 11111111 corresponds to 1000 mA

Register Address	Bit	Type	Label	Description
R90 TBAT_RES	7:0	R	TBAT_RES	00000000 – 11111111: Auto ADC TBAT conversion result (ADCIN1)

Register Address	Bit	Type	Label	Description
R91 TBAT_HIGHP	7:0	R/W	TBAT_HIGHP	00000000 – 11111111: TBAT high temperature threshold

Register Address	Bit	Type	Label	Description
R92 TBAT_HIGHN	7:0	R/W	TBAT_HIGHN	00000000 – 11111111: TBAT high temperature resume charging threshold (typically 45 °C)

Register Address	Bit	Type	Label	Description
R93 TBAT_LOW	7:0	R/W	TBAT_LOW	00000000 – 11111111: TBAT low temperature threshold (typically 0 °C)

Register Address	Bit	Type	Label	Description
R94 T_OFFSET	7:0	R/W	T_OFFSET	10000000 – 01111111: signed two's complement calibration offset for junction temperature

				measurement

Register Address	Bit	Type	Label	Description
R95 ADCIN4_RES	7:0	R	ADCIN4_RES	00000000 – 11111111: Auto ADC ADCIN4 conversion result

Register Address	Bit	Type	Label	Description
R96 AUTO4_HIGH	7:0	R/W	AUTO4_HIGH	00000000 – 11111111: ADCIN4 high level threshold

Register Address	Bit	Type	Label	Description
R97 AUTO4_LOW	7:0	R/W	AUTO4_LOW	00000000 – 11111111: ADCIN4 low level threshold

Register Address	Bit	Type	Label	Description
R98 ADCIN5_RES	7:0	R	ADCIN5_RES	00000000 – 11111111: Auto ADC ADCIN5 conversion result

Register Address	Bit	Type	Label	Description
R99 AUTO5_HIGH	7:0	R/W	AUTO5_HIGH	00000000 – 11111111: ADCIN5 high level threshold

Register Address	Bit	Type	Label	Description
R100 AUTO5_LOW	7:0	R/W	AUTO5_LOW	00000000 – 11111111: ADCIN5 low level threshold

Register Address	Bit	Type	Label	Description
R101 ADCIN6_RES	7:0	R	ADCIN6_RES	00000000 – 11111111: Auto ADC ADCIN6 conversion result

Register Address	Bit	Type	Label	Description
R102 AUTO6_HIGH	7:0	R/W	AUTO6_HIGH	00000000 – 11111111: ADCIN6 high level threshold

Register Address	Bit	Type	Label	Description
R103 AUTO6_LOW	7:0	R/W	AUTO6_LOW	00000000 – 11111111: ADCIN6 low level threshold

Register Address	Bit	Type	Label	Description
R104 TJUNC_RES	7:0	R	TJUNC_RES	00000000 – 11111111: Auto TJUNC conversion result (ADCIN8)

19 TSI Control

Table 57: TSI Control Registers

Register Address	Bit	Type	Label	Description
R105 TSI_CONT_A	0	R/W	AUTO_TSI_EN	0: Auto TSI sequence disabled 1: Auto TSI sequence measurements enabled (triggered from pen detection or manual measurement)
	1	R/W	PEN_DET_EN	0: Pen detection (repeating sequences measurement) disabled 1: Pen detect circuit (repeating sequences measurement) enabled
	2	R/W	TSI_MODE	Configures TSI to automatically measure sequence either XP or XYZP (XYP) values 0: XYZP mode: X&Y&Z plus two X&Y measurement, each followed by a pen detection 1: XP mode: X measurements each followed by a pen detection. If PEN_DETECT_EN is asserted the sequences will be repeated until PEN_DOWN is released otherwise only one sequence is measured
	5:3	R/W	TSI_SKIP	Delay between two measurements of X&Y&P or X&Y&Z&P (or X&P) where no measurements are made. During this period the XY switches are open and no current is flowing through the screen so reducing average current consumption. 000: continuous operation (<=3 kHz X&Y) 001: 2 slots (<=1.875 kHz X&Y) 010: 5 slots (<=1.200 kHz X&Y) 011: 10 slots (<=750 Hz X&Y) 100: 30 slots (<=300 Hz X&Y) 101: 80 slots (<=120 Hz X&Y) 110: 130 slots (<=75 Hz X&Y) 111: 330 slots (<=30 Hz X&Y)
	7:6		TSI_DELAY	Delay between closing XY switches and ADC measurement to allow external decoupling capacitors to settle (extends the measurement interval in addition to TSI_SKIP). 00: 0 slot (Switches closed inside ADC conversion slot => 6 µs for settling) 01: 1 slots (Switches closed at end of previous slot => 56 µs for settling) 10: 2 slots (> 156 µs for settling) 11: 4 slots (> 256 µs for settling) Switches are set at the end of previous TSI conversion, reading occurs in the slot following the specified number of delay slots and the pattern repeats. Delay of <= 1 slot provides continuous readings.

Register Address	Bit	Type	Label	Description
R106 TSI_CONT_B	0	R/W	TSI_SEL_0	0: X+ switch open 1: X+ switch closed
	1	R/W	TSI_SEL_1	0: X- switch open 1: X- switch closed
	2	R/W	TSI_SEL_2	0: Y+ switch open 1: Y+ switch closed
	3	R/W	TSI_SEL_3	0: Y- switch open 1: Y- switch closed
	5:4	R/W	TSI_MUX	Direct setting of MUX selecting which XY pin is routed to ADC_IN7 input. 00: X+ (results will be stored in TSI_XM) 01: Y+ (results will be stored in TSI_YM) 10: X- (results will be stored in TSI_XM) 11: Y- (results will be stored in TSI_YM)
	6	R/W	TSI_MAN	When set, starts manual operation of the TSI measurements: If AUTO_TSI_EN is zero an individual measurement configured by TSI_SEL_x and TSI_MUX will be performed. If AUTO_TSI_EN was asserted the content from TSI_SEL_x and TSI_MUX will be ignored and a single measurement sequence configured in TSI_MODE will be executed. This bit clears automatically at the end of the selected measurement.
	7	R/W	ADCREF	ADC reference connection for TSI measurements. 0: TSIREF/VSS 1: X+/X-, Y+/Y- or Y+/X- (for X, Y or Z measurements)

Register Address	Bit	Type	Label	Description
R107 TSI_X_MSB	7:0	R	TSI_XM	TSI X measurement result- 8 MSBs To ensure a synchronous data read, the act of reading TSI_X_MSB, latches the latest X & Y measurements. The values can then be safely read, even if another TSI measurement has occurred in the elapsed time between reads. The addresses are sequential, allowing a page mode read.

Register Address	Bit	Type	Label	Description
R108 TSI_Y_MSB	7:0	R	TSI_YM	TSI Y measurement result- 8 MSBs

Register Address	Bit	Type	Label	Description
R109 TSI_LSB	1:0	R	TSI_XL	TSI X measurement result- 2 LSBs
	3:2	R	TSI_YL	TSI Y measurement result- 2 LSBs
	5:4	R	TSI_ZL	TSI Z measurement result- 2 LSBs
	6	R	PEN_DOWN	PEN_DOWN state: 0: Pen touch not detected 1: Pen touch detected
	7	R		Reserved

Register Address	Bit	Type	Label	Description
R110 TSI_Z_MSB	7:0	R	TSI_ZM	TSI Z measurement result- 8 MSBs

20 RTC Calendar and Alarm

Table 58: RTC Calendar and Alarm Control Registers

Register Address	Bit	Type	Label	Description
R111 COUNT_S	5:0	R/W	COUNT_SEC	0x00 – 0x3B: RTC seconds read-out. A read of this register latches the current RTC calendar count into the registers R111 to R116 (cohererent for approx 0.5 s).
	6	R/W	MONITOR	Read-out '0' indicates that the power was lost. Read-out of '1' indicates that the clock is OK Set to '1' when setting time to arm RTC monitor function.
	7	R		Reserved

Register Address	Bit	Type	Label	Description
R112 COUNT_MI	5:0	R/W	COUNT_MIN	0x00 – 0x3B: RTC minutes read-out
	7:6	R		Reserved

Register Address	Bit	Type	Label	Description
R113 COUNT_H	4:0	R/W	COUNT_HOUR	0x00 – 0x17: RTC hours read-out
	7:5	R		Reserved

Register Address	Bit	Type	Label	Description
R114 COUNT_D	4:0	R/W	COUNT_DAY	0x01 – 0x1F: RTC days read-out
	7:5	R		Reserved

Register Address	Bit	Type	Label	Description
R115 COUNT_MO	3:0	R/W	COUNT_MONTH	0x01 – 0x0C: RTC months read-out
	7:4	R		Reserved

Register Address	Bit	Type	Label	Description
R116	5:0	R/W	COUNT_YEAR	0x00 – 0x3F: RTC years read-out (0 corresponds to year 2000). A write to this register latches the registers

COUNT_Y				R111 to R116 into the current RTC calendar count
	7:6	R		Reserved

Register Address	Bit	Type	Label	Description
R117 ALARM_MI	5:0	R/W	ALARM_MIN	0x00 – 0x3B: Alarm minutes setting
	6	R/W	ALARM_Type	Alarm event caused by: 0: TICK 1: Timer alarm
	7	R/W	TICK_Type	Tick alarm interval is: 0: one second 1: one minute

Register Address	Bit	Type	Label	Description
R118 ALARM_H	4:0	R/W	ALARM_HOUR	0x00 – 0x17: Alarm hours setting
	7:5	R		Reserved

Register Address	Bit	Type	Label	Description
R119 ALARM_D	4:0	R/W	ALARM_DAY	0x01 – 0x1F: Alarm days setting
	7:5	R		Reserved

Register Address	Bit	Type	Label	Description
R120 ALARM_MO	3:0	R/W	ALARM_MONTH	0x01 – 0x0C: Alarm months setting
	7:4	R		Reserved

Register Address	Bit	Type	Label	Description
R121 ALARM_Y	5:0	R/W	ALARM_YEAR	0x00 – 0x3F: Alarm years setting (0 corresponds to year 2000). A write to this register latches the registers R117 to R121
	6	R/W	ALARM_ON	0: Alarm function is disabled 1: Alarm enabled
	7	R/W	TICK_ON	0: Tick function is disabled 1: Periodic tick alarm enabled

Register Address	Bit	Type	Label	Description
R122 SECOND_A	7:0	R	SECONDS_A	RTC seconds counter A (LSBs). A read of this register latches the current 32-bit counter into the registers R122 to R125 (cohererent for approx 0.5 s).

Register Address	Bit	Type	Label	Description
R123 SECOND_B	7:0	R	SECONDS_B	RTC seconds counter B

Register Address	Bit	Type	Label	Description
R124 SECOND_C	7:0	R	SECONDS_C	RTC seconds counter C

Register Address	Bit	Type	Label	Description
R125 SECOND_D	7:0	R	SECONDS_D	RTC seconds counter D (MSBs)

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Table 59: Customer OTP Registers

Register Address	Bit	Type	Label	Description
R128 PAGE_CON_P1	6:0	R		Reserved
	7	RW	REG_PAGE	0: Selects Register R1 to R127 1: Selects Register R129 to R255

Register Address	Bit	Type	Label	Description
R129 CHIP_ID	3:0	R	TRC	Read back of OTP Trimming release code (TRC) – starts with a code 0
	7:4	R	MRC	Read back of mask revision code (MRC) – code 0 for AA release

Register Address	Bit	Type	Label	Description
R130 CONFIG_ID	2:0	R	CONF_ID	ID for customer variant of start-up voltages and sequencer configuration, written during production of variant
	7:3	R	CUSTOMER_ID	ID for customer, written during production of variant

22 Customer OTP

Register Address	Bit	Type	Label	Description
R131 OTP_CONT	0	R/W	OTP_TRANSFER	0: No transfer in progress 1: Writing '1' to this bit initiates the fusing of selected OTP cells with the content from corresponding registers 1: Reading '1' indicates the transfer is still ongoing
	1	R/W	OTP_RP	0: Transfer is Read 1: Transfer is Programming
	2	R/W	OTP_GP	0: No action 1: Transfer includes configuration registers R132 to 0 (plus GP_WRITE_DIS and OTP_GP_LOCK)
	3	R/W	OTP_CONF	0: No action 1: Transfer includes configuration 0 to 0 (plus OTP_CONF_LOCK)
	4	R		Reserved
	5	R	OTP_GP_LOCK	0: OTP not locked after programming 1: OTP will be locked during programming (no further fusing possible) Note: Write access for fusing only, control state is loaded from OTP defaults after POR
	6	R/W	OTP_CONF_LOCK	0: OTP registers 0 to 0 not locked after programming (only for unmarked evaluation samples) 1: OTP registers 0 to 0 will be locked during programming (set for all marked parts, no further fusing possible) Note: Write access for fusing only, control state is loaded from OTP defaults after POR
	7	R/W	GP_WRITE_DIS	0: Enables write access to GP_ID registers 1: GP_ID registers are 'read only' Note: Write access for fusing only, control state is loaded from OTP defaults after POR

Register Address	Bit	Type	Label	Description
R132 OSC_TRIM	7:0	R/W	TRIM_32K	Bits for correction of the 32 kHz oscillator frequency: 10000000: -244.1ppm … 11111111: -1.9ppm 00000000: off 00000001: 1.9ppm (1/(32768*16)) … 01111111: 242.2ppm

NOTE
Write access disabled to GP_ID if GP_WRITE_DIS fused with '1'.

Register Address	Bit	Type	Label	Description
R133 GP_ID_0	7:0	R/W	GP_0	Data from fuse array (OTP)

Register Address	Bit	Type	Label	Description
R134 GP_ID_1	7:0	R/W	GP_1	Data from fuse array (OTP)

Register Address	Bit	Type	Label	Description
R135 GP_ID_2	7:0	R/W	GP_2	Data from fuse array (OTP)

Register Address	Bit	Type	Label	Description
R136 GP_ID_3	7:0	R/W	GP_3	Data from fuse array (OTP)

Register Address	Bit	Type	Label	Description
R137 GP_ID_4	7:0	R/W	GP_4	Data from fuse array (OTP)

Register Address	Bit	Type	Label	Description
R138 GP_ID_5	7:0	R/W	GP_5	Data from fuse array (OTP)

Register Address	Bit	Type	Label	Description
R139 GP_ID_6	7:0	R/ R/W	GP_6	Data from fuse array (OTP)

Register Address	Bit	Type	Label	Description
R140 GP_ID_7	7:0	R/W	GP_7	Data from fuse array (OTP)

Register Address	Bit	Type	Label	Description
R141 GP_ID_8	7:0	R/W	GP_8	Data from fuse array (OTP)

Register Address	Bit	Type	Label	Description
R142 GP_ID_9	7:0	R/W	GP_9	Data from fuse array (OTP)

23 Register MAP

23.1 Overview

Most register bits (exceptions are for example, FAULT_LOG or CHG_TIME), that are not loaded from OTP are reset to defaults (zero in most cases) when powering up from RESET mode. Register bits shown in BLUE are loaded from OTP.

R	FUNCTION	7	6	5	4	3	2	1	0
PAGE 0									
System control and event registers (SYSMON)									
R0	PAGE_CON	REG_PAGE	Reserved						
R1	STATUS_A	VDAT_DET	VBUS_SEL	DCIN_SEL	VBUS_DET	DCIN_DET	ID_GND	ID_FLOAT	nONKEY
R2	STATUS_B	COMP_DET	SEQUENCING	GP_FB2	CHG_TO	CHG_END	CHG_LIM	CHG_PRE	CHG_ATT
R3	STATUS_C	GPI7	GPI6	GPI5	GPI4	GPI3	GPI2	GPI1	GPI0
R4	STATUS_D	GPI15	GPI14	GPI13	GPI12	GPI11	GPI10	GPI9	GPI8
R5	EVENT_A	M_COMP_1V2	M_SEQ_RDY	E_ALARM	E_VDD_LOW	E_VBUS_REM	E_DCIN_REM	E_VBUS_DET	E_DCIN_DET
R6	EVENT_B	E_TSI_READY	E_PEN_DOWN	E_ADC_EOM	E_TBAT	E_CHG_END	E_ID_GND	E_ID_FLOAT	E_nONKEY
R7	EVENT_C	E_GPI7	E_GPI6	E_GPI5	E_GPI4	E_GPI3	E_GPI2	E_GPI1	E_GPI0
R8	EVENT_D	E_GPI15	E_GPI14	E_GPI13	E_GPI12	E_GPI11	E_GPI10	E_GPI9	E_GPI8
R9	FAULT_LOG	WAIT_SHUT	nSD_SHUT	KEY_SHUT	Reserved	TEMP_OVER	VDD_START	VDD_FAULT	TWD_ERROR
R10	IRQ_MASK_A	M_COMP_1V2	M_SEQ_RDY	M_ALARM	M_VDD_LOW	M_VBUS_REM	M_DCIN_REM	M_VBUS_VLD	M_DCIN_VLD
R11	IRQ_MASK_B	M_TSI_READY	M_PEN_DOWN	M_ADC_EOM	M_TBAT	M_CHG_END	M_ID_GND	M_ID_FLOAT	M_nONKEY
R12	IRQ_MASK_C	M_GPI7	M_GPI6	M_GPI5	M_GPI4	M_GPI3	M_GPI2	M_GPI1	M_GPI0
R13	IRQ_MASK_D	M_GPI15	M_GPI14	M_GPI13	M_GPI12	M_GPI11	M_GPI10	M_GPI9	M_GPI8
R14	CONTROL_A	GPI_V	PM_O_Type	PM_O_V	PM_I_V	PM_IF_V	PWR1_EN	PWR_EN	SYS_EN
R15	CONTROL_B	SHUTDOWN	DEEP_SLEEP	WRITE_MODE	BBAT_EN	OTPREAD_EN	AUTO_BOOT	ACT_DIODE	BUCK_MERGE
R16	CONTROL_C	BLINK_DUR	BLINK_FRQ		DEBOUNCING			PM_FB2_PIN	PM_FB1_PIN
R17	CONTROL_D	WATCHDOG	ACC_DET_EN	GPI14_15_SD	nONKEY_SD	KEEPACT_EN	TWDSCALE		
R18	PD_DIS	PM-CONT_PD	OUT_32K_PD	CHG_BBAT_PD	CHG_PD	HS-2-wire_PD	PM-IF_PD	GP-ADC_PD	GPIO_PD
R19	INTERFACE	IF_BASE_ADDR			nCS_POL	R/W_POL	CPHA	CPOL	IF_Type
R20	RESET	RESET_EVENT		RESET_TIMER					
GPIO control registers (GPIO)									
R21	GPIO_0-1	GPIO1_ MODE	GPIO1_Type	GPIO1_PIN		GPIO0_ MODE	GPIO0_Type	GPIO0_PIN	
R22	GPIO_2-3	GPIO3_ MODE	GPIO3_Type	GPIO3_PIN		GPIO2_MODE	GPIO2_Type	GPIO2_PIN	
R23	GPIO_4-5	GPIO5_ MODE	GPIO5_Type	GPIO5_PIN		GPIO4_ MODE	GPIO4_Type	GPIO4_PIN	
R24	GPIO_6-7	GPIO7_ MODE	GPIO7_Type	GPIO7_PIN		GPIO6_ MODE	GPIO6_Type	GPIO6_PIN	
R25	GPIO_8-9	GPIO9_ MODE	GPIO9_Type	GPIO9_PIN		GPIO8_ MODE	GPIO8_Type	GPIO8_PIN	
R26	GPIO_10-11	GPIO11_ MODE	GPIO11_Type	GPIO11_PIN		GPIO10_ MODE	GPIO10_Type	GPIO10_PIN	
R27	GPIO_12-13	GPIO13_ MODE	GPIO13_Type	GPIO13_PIN		GPIO12_ MODE	GPIO12_Type	GPIO12_PIN	
R28	GPIO_14-15	GPIO15_ MODE	GPIO15_Type	GPIO15_PIN		GPIO14_ MODE	GPIO14_Type	GPIO14_PIN	
Power sequencer control registers (SEQ)									
R29	ID_0_1	LDO1_STEP				WAIT_ID_ALWAYS	SYS_PRE	DEF_SUPPLY	nRES_MODE
R30	ID_2_3	LDO3_STEP				LDO2_STEP			
R31	ID_4_5	LDO5_STEP				LDO4_STEP			
R32	ID_6_7	LDO7_STEP				LDO6_STEP			
R34	ID_10_	LDO9_STEP				LDO8_STEP			
R34	ID_10_11	PD_DIS_STEP				LDO10_STEP			
R35	ID_12_13	VMEM_SW_STEP				VPERI_SW_STEP			
R36	ID_14_15	BUCKPRO_STEP				BUCKCORE_STEP			
R37	ID_16_17	BUCKPERI_STEP				BUCKMEM_STEP			

R38	ID_18_19	GP_RISE2_STEP				GP_RISE1_STEP			
R39	ID_20_21	GP_FALL2_STEP				GP_FALL1_STEP			
R40	SEQ_STATUS	SEQ_POINTER				WAIT_STEP			
R41	SEQ_A	POWER_END				SYSTEM_END			
R42	SEQ_B	PART_DOWN				MAX_COUNT			
R43	SEQ_TIMER	SEQ_DUMMY				SEQ_TIME			
Power supply control registers (REG)									
R44	BUCK_A	BPRO_ILIM		BPRO_MODE		BCORE_ILIM		BCORE_MODE	
R45	BUCK_B	BPERI_ILIM		BPERI_ MODE		BMEM_ILIM		BMEM_ MODE	
R46	BUCKCORE	BCORE_CONF	BCORE_EN	VBCORE					
R47	BUCKPRO	BPRO_CONF	BPRO_EN	VBPRO					
R48	BUCKMEM	BMEM_CONF	BMEM_EN	VBMEM					
R49	BUCKPERI	BPERI_CONF	BPERI_EN		VBPERI				
R50	LDO1	LDO1_CONF	LDO1_EN	VLDO1					
R51	LDO2	LDO2_CONF	LDO2_EN	VLDO2					
R52	LDO3	LDO3_CONF	LDO3_EN	VLDO3					
R53	LDO4	LDO4_CONF	LDO4_EN	VLDO4					
R54	LDO5	LDO5_CONF	LDO5_EN	VLDO5					
R55	LDO6	LDO6_CONF	LDO6_EN	VLDO6					
R56	LDO7	LDO7_CONF	LDO7_EN	VLDO7					
R57	LDO8	LDO8_CONF	LDO8_EN	VLDO8					
R58	LDO9	LDO9_CONF	LDO9_EN	VLDO9					
R59	LDO10	LDO10_CONF	LDO10_EN	VLDO10					
R60	SUPPLY	V_LOCK	VMEM_SW_EN	VPERI_SW_EN	VLDO3_GO	VLDO2_GO	VB_MEM_GO	VB_PRO_GO	VB_CORE_GO
R61	PULLDOWN	Reserved	Reserved	LDO5_PD_DIS	LDO2_PD_DIS	LDO1_PD_DIS	MEM_PD_DIS	PRO_PD_DIS	CORE_PD_DIS
Charging control registers (CHARGE)									
R62	CHG_BUCK	CHG_TEMP	CHG_USB_ILIM	CHG_BUCK_LP	CHG_BUCK_EN	ISET_BUCK			
R63	WAIT_CONT	WAIT_DIR	RTC_CLOCK	WAIT_MODE	EN_32KOUT	DELAY_TIME			
R64	ISET	ISET_DCIN				ISET_USB			
R65	BAT_CHG	ICHG_PRE		ICHG_BAT					
R66	CHG_CONT	VCHG_BAT					VCH_THR		
R67	INPUT_CONT	TCTR_MODE	VCHG_DROP	DCIN_SUSP	VBUS_SUSP	TCTR			
R68	CHG_TIME	CHG_TIME							
Backup battery charging control registers (BBAT)									
R69	BBAT_CONT	BCHARGER_ISET				BCHARGER_VSET			
Boost and LED driver control registers (LED)									
R70	BOOST	E_B_FAULT	M_B_FAULT	BOOST_FRQ	BOOST_ILIM	LED3_IN_EN	LED2_IN_EN	LED1_IN_EN	BOOST_EN
R71	LED_CONT	SEL_LED_MODE	LED3_ICONT	LED3_RAMP	LED3_EN	LED2_RAMP	LED2_EN	LED1_RAMP	LED1_EN
R72	LEDMIN	LEDMIN_CURRENT							
R73	LED1_CONF	LED1_CURRENT							
R74	LED2_CONF	LED2_CURRENT							
R75	LED3_CONF	LED3_CURRENT							
R76	LED1_CONT	LED1_DIM	LED1_PWM						
R77	LED2_CONT	LED2_DIM	LED2_PWM						
R78	LED3_CONT	LED3_DIM	LED3_PWM						

R79	LED4_CONT	LED4_DIM	LED4_PWM						
R80	LED5_CONT	LED5_DIM	LED5_PWM						
GP-ADC control registers (GPADC)									
R81	ADC_MAN	Reserved			MAN_CONV	MUX_SEL			
R82	ADC_CONT	COMP1V2_EN	ADC_MODE	TBAT_ISRC_EN	AD4_ISRC_EN	AUTO_AD6_EN	AUTO_AD5_EN	AUTO_AD4_EN	AUTO_VDD_EN
R83	ADC_RES_L	Reserved						ADC_RES_LSB	
R84	ADC_RES_H	ADC_RES_MSB							
R85	VDD_RES	VDDOUT_RES							
R86	VDD_MON	VDDOUT_MON							
R87	ICHG_AV	ICHG_AV							
R88	ICHG_THD	ICHG_THD							
R89	ICHG_END	ICHG_END							
R90	TBAT_RES	TBAT_RES							
R91	TBAT_HIGHP	TBAT_HIGHP							
R92	TBAT_HIGHN	TBAT_HIGHN							
R93	TBAT_LOW	TBAT_LOW							
R94	T_OFFSET	T_OFFSET							
R95	ADCIN4_RES	ADCIN4_RES							
R96	AUTO4_HIGH	AUTO4_HIGH							
R97	AUTO4_LOW	AUTO4_LOW							
R98	ADCIN5_RES	ADCIN5_RES							
R99	AUTO5_HIGH	AUTO5_HIGH							
R100	AUTO5_LOW	AUTO5_LOW							
R101	ADCIN6_RES	ADCIN6_RES							
R102	AUTO6_HIGH	AUTO6_HIGH							
R103	AUTO6_LOW	AUTO6_LOW							
R104	TJUNC_RES	TJUNC_RES							
TSI control registers (TSI)									
R105	TSI_CONT_A	TSI_DELAY		TSI_SKIP			TSI_MODE	PEN_DET_EN	AUTO_TSI_EN
R106	TSI_CONT_B	ADCREF	TSI_MAN	TSI_MUX		TSI_SEL_3	TSI_SEL_2	TSI_SEL_1	TSI_SEL_0
R107	TSI_X_MSB	TSI_XM							
R108	TSI_Y_MSB	TSI_YM							
R109	TSI_LSB	Reserved	PEN_DOWN	TSI_ZL		TSI_YL		TSI_XL	
R110	TSI_Z_MSB	TSI_ZM							
RTC calendar and alarm (RTC)									
R111	COUNT_S	Reserved	MONITOR	COUNT_SEC					
R112	COUNT_MI	Reserved		COUNT_MIN					
R113	COUNT_H	Reserved			COUNT_HOUR				
R114	COUNT_D	Reserved			COUNT_DAY				
R115	COUNT_MO	Reserved				COUNT_MONTH			
R116	COUNT_Y	Reserved	Reserved	COUNT_YEAR					
R117	ALARM_MI	TICK_Type	ALARM_Type	ALARM_MIN					
R118	ALARM_H	Reserved			ALARM_HOUR				
R119	ALARM_D	Reserved			ALARM_DAY				
R120	ALARM_MO	Reserved				ALARM_MONTH			

R121	ALARM_Y	TICK_ON	ALARM_ON	ALARM_YEAR					
R122	SECOND_A	SECONDS_A							
R123	SECOND_B	SECONDS_B							
R124	SECOND_C	SECONDS_C							
R125	SECOND_D	SECONDS_D							
PAGE 1									
Customer OTP (MEM)									
R128	PAGE_CON	REG_PAGE	Reserved						
R129	CHIP_ID	MRC				TRC			
R130	CONFIG_ID	CUSTOMER_ID					CONF_ID		
R131	OTP_CONT	GP_WRITE_DIS	OTP_CONF_LOCK	OTP_GP_LOCK	Reserved	OTP_CONF	OTP_GP	OTP_RP	OTP_TRANSFER
R132	OSC_TRIM	TRIM_32K							
R133	GP_ID_0	GP_0							
R134	GP_ID_1	GP_1							
R135	GP_ID_2	GP_2							
R136	GP_ID_3	GP_3							
R137	GP_ID_4	GP_4							
R138	GP_ID_5	GP_5							
R139	GP_ID_6	GP_6							
R140	GP_ID_7	GP_7							
R141	GP_ID_8	GP_8							
R142	GP_ID_9	GP_9							

24 External Component Selection

24.1 Capacitor Selection

Ceramic capacitors are used as bypass capacitors at all VDD and output rails.

When selecting a capacitor, especially for types with high capacitance at smallest physical dimension, the DC bias characteristic has to be taken into account.

On the VDDOUT main supply rail a minimum distributed capacitance of 80 µF with the following split is recommended:

- 2x 10 µF close to VDDOUT pin
- 22 µF close to VDDBUCK_PERI_PRO buck supply pin
- 22 µF close to VDDBUCK_CORE buck supply pin
- 10 µF close to VDDBUCK_MEM buck supply pin
- 4.7 µF close to boost converter input (coil)
- 2 x 1 µF close to VDD_LDOx pins

Table 60: Recommended Capacitor Types

Application	Value	Size	Temp. Char.	Tolerance	Rated Voltage	Type
VLDO1, VLDO2, VLDO5, VLDO9 output bypass	4x 1 µF	0402	X5R +/- 15 %	+/-10 %	10 V	Murata GRM155R61A105KE15D
VLDO3, VLDO4, VLDO6, VLDO7, VLDO8, VLDO10 output bypass	6x 2.2 µF	0402	X5R +/- 15 %	+/-20 %	6.3 V	Murata GRM155R60J225ME15D
VDDCORE output bypass, VREF	1x 100 nF	0402	X7R +/- 15 %	+/-10 %	16 V	Murata GRM155R71C104KA88D
VBUCKPRO, VBUCKPERI, VBUCKMEM output bypass	3x 22 µF	0805	X5R +/- 15 %	+/-20 %	6.3 V	Murata GRM21BR60J226ME39L
VBUCKCORE	2x 22 µF	0805	X5R +/- 15 %	+/-20 %	6.3 V	Murata GRM21BR60J226ME39L
VMEM_SW, VCORE_SW output bypass	2x 100 nF	0402	X7R +/- 15 %	+/-10 %	16 V	Murata GRM155R71C104KA88D
VBOOST output bypass	1x 2.2 µF	1206	X7R +/- 15 %	+/-10 %	25 V	Murata GRM31MR71E225KA93L
VBUS, DCIN bypass	2x 2.2 µF	0603	X5R +/- 15 %	+/-10 %	16 V	Murata GRM188R61C225KE15
VBUS_PROT, DCIN_PROT bypass	2x 4.7 µF	0603	X5R +/- 15 %	+/-10 %	6.3 V	Murata GRM188R71J475KE19D

Application	Value	Size	Temp. Char.	Tolerance	Rated Voltage	Type
VCENTER bypass	1x 10 µF	0805	X7R +/- 15%	+/-10 %	6.3 V	Murata GRM21BR70J106KE76L
VDDOUT bypass	3x 10 µF	0805	X7R +/- 15%	+/-10 %	6.3 V	Murata GRM21BR70J106KE76L
	2x 1 µF	0402	X5R +/- 15%	+/-10 %	10 V	Murata GRM155R61A105KE15D
VBAT bypass	1x 10 µF	0805	X7R +/- 15%	+/-10 %	6.3 V	Murata GRM21BR70J106KE76L
VDD_REF bypass	1x 2.2 µF	1206	X7R +/- 15%	+/-10 %	25 V	Murata GRM31MR71E225KA93L
XIN, XOUT bypass to VSS	2x 12 pF	0402	U2J	+/-5 %	50 V	Murata GRM1557U1H120JZ01D
VBBAT	1 x 470 nF	0402	X5R +/- 10%	+/-10 %	10 V	Murata GRM155R61A474KE15D

24.2 Inductor Selection

Inductors should be selected based upon the following parameters:

- Rated max. current: Usually a coil provides two current limits, one specifies the maximum current at which the inductance derating due to saturation effects is limited to be within a specified tolerance (typical 20% or 30%) of the peak current. The second limit is defined by the maximum power dissipation and is applied to the effective current.
- DC resistance: Critical to converter efficiency and should therefore be minimized.
- Inductance: Given by converter electrical characteristics; designed for 2.2 µH for all DA9053 buck converters,

Table 61: Recommended Inductor Types

Application	Value	Size (mm)	Isat (A) (Note 1)	Irms (A) (Note 2)	Tol (%)	DCR (Ω)	Type
BUCKCORE	1 x 2.2 µH	3.7x3.9x1.8	2.55	1.9	+/-20	0.048	TOKO DE3518C 1127AS-2R7M
	1 x 2.2 µH	4x4x1.2	2.5	1.75	+/-30	0.1	Coilcraft LPS4012-222NL
	1 x 2.2 µH	5x5x1.5	2.7	2	+/-20	0.09	Coilcraft LPS5015-222ML
BUCKPERI, BUCKMEM, BUCKPRO	3 x 2.2 µH	2.5x2x1.2	1.8	1.3	+/-20	0.155	TDK VLS252012T-2R2M1R3
	3 x 2.2 µH	2.5x2x1.2	1.7	1.3	+/-20	0.096	TOKO DFE252012 1239AS-H-2R2N
BOOST	1x 4.7 µH	3x3x1.2	1	1.4	+/-20	0.13	TDK VLS3012T-4R7M1R0
CHARGER BUCK	1 x 2.2 µH	4x4x1.2	2.5	1.75	+/-30	0.1	Coilcraft LPS4012-222NL

	1 x 2.2 µH	4x4x1.7	2	2.9	+/-20	0.07	Coilcraft LPS4018-222ML

Note 1 Value obtained when the nominal value of the inductance has fallen by 30 % under the value at zero current.

Note 2 Value obtained when the temperature has risen by 40 °C. This parameter is important for the maximum DC current.

24.3 Resistors

Table 62: Recommended Resistor Types

Application	Value	Size	Tolerance	P max	Type
BOOST current sense	100 mΩ	0402	+/-2 %	125 mW	Panasonic ERJ2BSGR10x
IREF bias current reference	200 kΩ	0402	+/-1 %	100 mW	Panasonic ERJ2RKF2003x

24.4 External Pass Transistors and Schottky Diodes

Table 63: Recommended Schottky Diode and Transistor Types

Application	Package	Type
BOOST FET + SCHOTTKY	WDFN6 2x2x0.8 mm	ON Semiconductor NTLJF4156N
SCHOTTKY	SOD323	BAT760
VBUS overvoltage protection FET	SOT-23	CSD25301W1015, PMV65XP
DCIN overvoltage protection FET	SOT-23	CSD25301W1015, PMV65XP
VBUS/DCIN dual overvoltage protection FET	PowerPAK1212-8 3.3x3.3x1 mm	Vishay Siliconix Si7911DN
System load switch (active diode) FET	SOT-23 3x2.6x1 mm	Vishay Siliconix Si2333DS

24.5 Backup Battery

The backup battery charger supports Lithium coin cells as well as Supercaps/Goldcaps. However if the internal RTC clock is used, the battery's nominal voltage should be above 3 V to allow reasonable backup times though the backup battery charger allows charge voltages from 1.1 V to 3.1 V (for example, for external RTC clock modules).

Table 64: Example Backup Battery Types

Type	Size	Manufacturer
Lithium Battery (rechargeable) ML414, 1.0 mAh, 3.1 V	4.8 (dia.) x 1.4 mm	Sanyo, Panasonic
Electric Double Layer Capacitor (Gold Capacitor) EECEN0F204xx, 0.2 F, 3.3 V	6.8 (dia.) x 1.8 mm	Panasonic
Electric Double Layer Capacitor (Gold Capacitor) EECEP0E333A, 0.033 F, 2.6 V	3.8 (dia.) x 1.5 mm	Panasonic

24.6 Battery Pack Temperature Sensor (NTC)

In order to achieve reasonable accuracy over the relevant temperature range (for example, 0 °C to 50 °C for charging) by using the internal 50 µA current source, the recommended NTC should have a nominal resistance of 10 kΩ (25) and its resistance should not exceed 50 kΩ within this range.

Table 65: Example Battery Pack Temperature Sensor

Type	Size	Manufacturer
NCP15XH103J03RC	0402	Murata

24.7 Crystal

The Real Time Clock module requires an external 32.768 kHz crystal. For crystal selection the effective load capacitance has to be taken into account. It includes both external capacitors on pins XIN and XOUT in series combination and the PCB and DA9053 stray capacitances.

For example, if two times 12pF external capacitors are used, which gives a series combination of 6pF, and the stray capacitance is 3pF, and then the crystal type specified for a load capacitance of 9pF should be chosen. Different stray capacitances may require different external capacitors and/or a different crystal type. Furthermore the series resistance of the crystal must not exceed 100 kΩ.

Table 66: Recommended Crystal Type

Type	Size	Manufacturer
CC7V-T1A 32.768 kHz 9.0 pF +/-30 ppm	3.2x1.5x0.9 mm	Micro Crystal

25 Layout Guidelines

25.1 General Recommendations

Appropriate trace width and amount of vias should be used for all power supply paths.

Too high trace resistances can prevent the system from proper operation, for example efficiency and current ratings of switch mode converters and charger might be degraded. Furthermore the PCB might be exposed to thermal hot spots, which can lead to critical overheating due to the positive temperature coefficient of copper.

Special care must be taken to the DA9053 pad connections. The traces of the outer row should be connected with the same width as the pads and should become wider as soon as possible. For supply pins in the second row connection in an inner layer is recommended (depending on the maximum current two or more vias might be required).

A common ground plane should be used, which allows proper electrical and thermal performance. Noise sensitive references like the VREF capacitor and IREF resistor should be referred to a silent ground which is connected at a star point underneath or close to the DA9053 main ground connection.

Generally all power tracks with discontinuous and / or high currents should be kept as short as possible.

Noise sensitive analogue signals like feedback lines or crystal connections should be kept away from traces carrying pulsed analogue or digital signals. This can be achieved by separation (distance) or shielding with quiet signals or ground traces.

See Dialog Semiconductor Applications note AN-PM-010_PCB_Layout_Guidlines.pdf for further layout guidance.

25.2 System Supply and Charger

- Trace resistance of the VBUSPROT (or DCIN_PROT) bypass capacitor to VCENTER has to be minimized to allow proper operation of the charge and system current control.
- In case an external pMOS transistor is used to bypass the internal active diode, its connection trace resistance has to be kept to a minimum.
- The placement of the distributed capacitors at VDDOUT must ensure that all VDD inputs, especially to the buck converters and LDOs, are connected to a bypass capacitor close to the pads. It is recommended to place at least two 1 µF capacitors close to the LDO supply pads and at least one 10 µF close to the buck VDD rail. Using a local power plane underneath the chip for VDDOUT might be considered.
- Adequate heat sink areas should be used for at least one terminal of the external overvoltage protection and / or active diode FETs.

25.3 LDOs and Switched Mode Supplies

- Transient current loops area of the switched mode converters should be minimized.
- The common references (VREF capacitor, IREF resistor) should be placed close to DA9053, cross coupling to any noisy digital or analog trace must be avoided.
- Output capacitors of the LDOs should be placed close to the output pins. Small capacitors (for example 100 nF) are also required close to the input pins of the supplied devices.
- Care must be taken that no current is carried on feedback lines (buck output voltages VBUCKxx and boost current sense inputs (BOOST_SENSE_P/N).

25.4 Crystal Oscillator

The crystal and its load capacitors should be placed as close as possible to the IC with short and symmetric traces.

The traces must be isolated from noisy signals, especially from clocked digital ones. Ideally the lines are buried between two ground layers, surrounded by additional ground traces.

25.5 Thermal Connection, Land Pad and Stencil Design

The DA9053 provides a centre ground plane, which is soldered directly to the PCB's centre ground pad. This PCB ground pad must be connected with as many vias and as direct as possible to the PCB's main ground plane in order to achieve good thermal performance.

Solder mask openings for the ground pad must be split by following a certain pattern like stripes or round shapes or squares, as a solid square would apply too much solder paste and the signal pads might not be connected properly.

As DA9053 also provides different sizes of the signal pads, some adaptation of the mask openings might be required as well (generally small pads a bit larger, large pads a bit smaller than the pad itself). Vias inside or next to the pads should be filled. An appropriately fine solder paste is required.

26 Definitions

26.1 Power Dissipation and Thermal Design

When designing with the DA9053 consideration must be given to power dissipation as the level of integration of the device can result in high power dissipation when all functions are operating with high battery voltages. Exceeding the package power dissipation will result in the internal thermal sensor shutting down the device until it has cooled sufficiently.

The package includes thermal management paddle to enable improved heat spreading on the PCB.

Linear regulators operating with a high current and high differential voltage between input and output will dissipate the following power

$$P_{diss} = (V_{in} - V_{out})*I_{out}$$

For example:

A regulator supplying 150 mA @ 2.8 V from a fully charged lithium battery (VDD = 4.1 V)

Pdiss = (4.1 V - 2.8 V)*0.15 A = 195 mW

For switching regulators:

Pout = Pin*efficiency

Therefore:

Pdiss = Pin - Pout

$$P_{diss} = \frac{P_{out}}{\text{Efficiency}} - P_{out}$$

$$P_{diss} = P_{out} * \left(\frac{1}{\text{Efficiency}} - 1\right)$$

$$P_{diss} = I_{out} * V_{out} * \left(\frac{1}{\text{Efficiency}} - 1\right)$$

Example – an 85 % efficient buck converter supplying 1.2 V@ 400 mA

$$P_{diss} = 1.2V * 0.4A * \left(\frac{1}{0.85} - 1\right) = 85mW$$

As the DA9053 is a multiple regulator configuration each supply must be considered and summed to give the total device dissipation (current drawn from the reference and control circuitry can be considered negligible in these calculations).

27 Regulator Parameters

27.1 Dropout Voltage

In the DA9053 a regulator's dropout voltage is defined as the minimum voltage differential between the input and output voltages whilst regulation still takes place. Within the regulator, voltage control takes place across a PMOS pass transistor and when entering the dropout condition the transistor is fully turned on and therefore cannot provide any further voltage control. When the transistor is fully turned on the output voltage tracks the input voltage and regulation ceases. As the DA9053 is a CMOS device and uses a PMOS pass transistor, the dropout voltage is directly related to the ON resistance of the device. In the device the pass transistors are sized to provide the optimum balance between required performance and silicon area. By employing a 0.25 µm process Dialog are able to achieve very small pass transistor sizes for superior performance.

Vdropout=Vin – Vout = Rdson * Iout

When defining dropout voltage it is specified in relation to a minimum acceptable change in output voltage. For example all Dialog regulators have dropout voltage defined as the point at which the output voltage drops 10 mV below the output voltage at the minimum guaranteed operating voltage. The worst case conditions for dropout are high temperature (highest ON resistance for internal device) and maximum current load.

27.2 Power Supply Rejection

Power supply rejection (PSRR) is especially important in the supplies to the RF and audio parts of the telephone. In a TDMA system such as GSM, the 217 Hz transmit burst from the power amplifier results in significant current pulses being drawn from the battery. These can peak at up to 2 A before reaching a steady state of 1.4 A (see below). Due to the battery having a finite internal resistance (typically 0.5 Ω) these current peaks induce ripple on the battery voltage of up to 500 mV. As the supplies to the audio and RF are derived from this supply it is essential that this ripple is removed otherwise it would show as a 217 Hz tone in the audio and could also affect the transmit signal. Power supply rejection should always be specified under worst case conditions when the battery is at its minimum operating voltage, when there is minimum headroom available due to dropout.

27.3 Line Regulation

Static line regulation is a measurement that indicates a change in the regulator output voltage ΔVreg (regulator operating with a constant load current) in response to a change in the input voltage ΔVin. Transient line regulation is a measurement of the peak change ΔVreg in regulated voltage seen when the line input voltage changes.

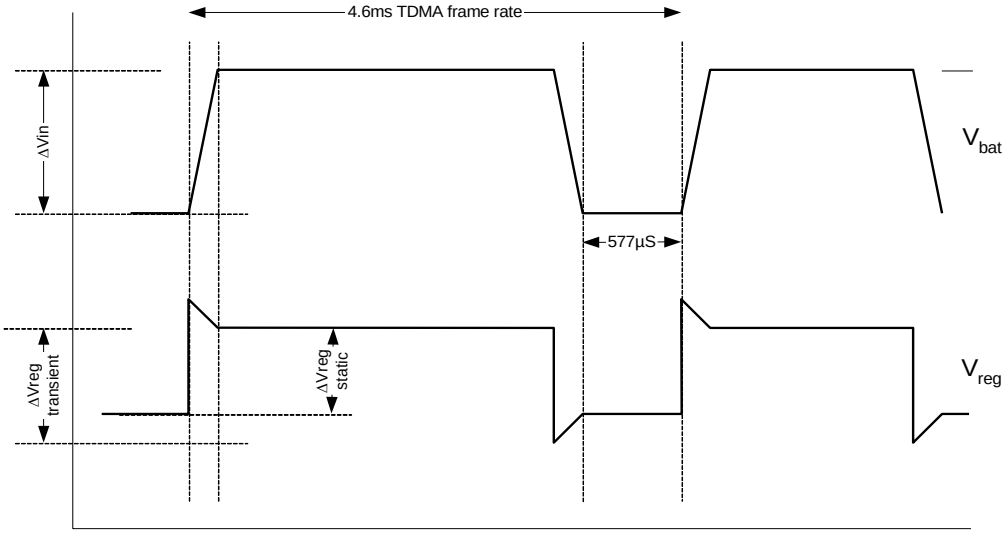


Figure 54: Transient and Static Line Regulation

27.4 Load Regulation

Static load regulation is a measurement that indicates a change in the regulator output voltage ΔVreg in response to a change in the regulator loading Δload whilst the regulator input voltage remains constant. Transient load regulation is a measurement of the peak change in regulated voltage ΔVreg seen when the regulator load changes.

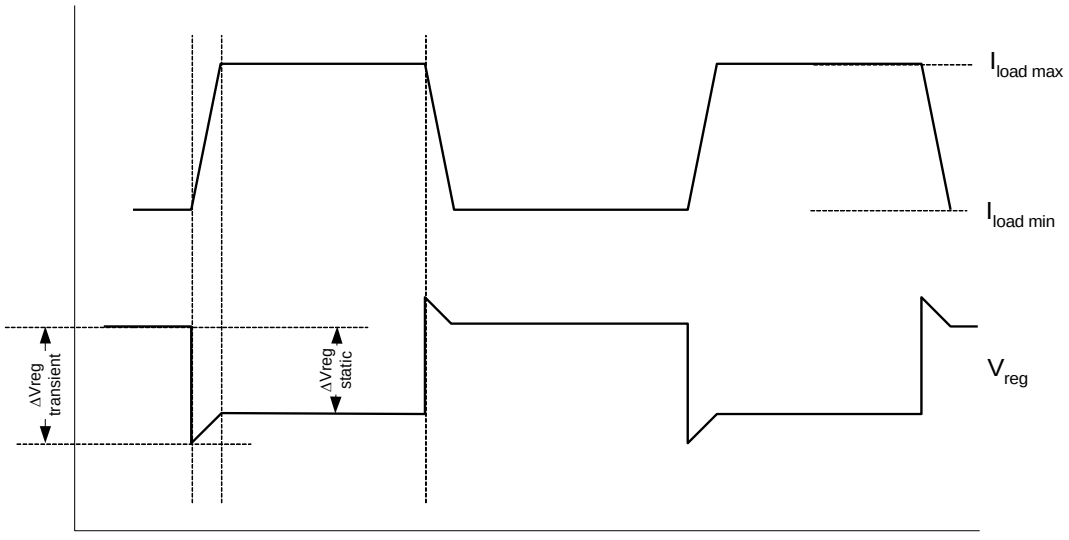
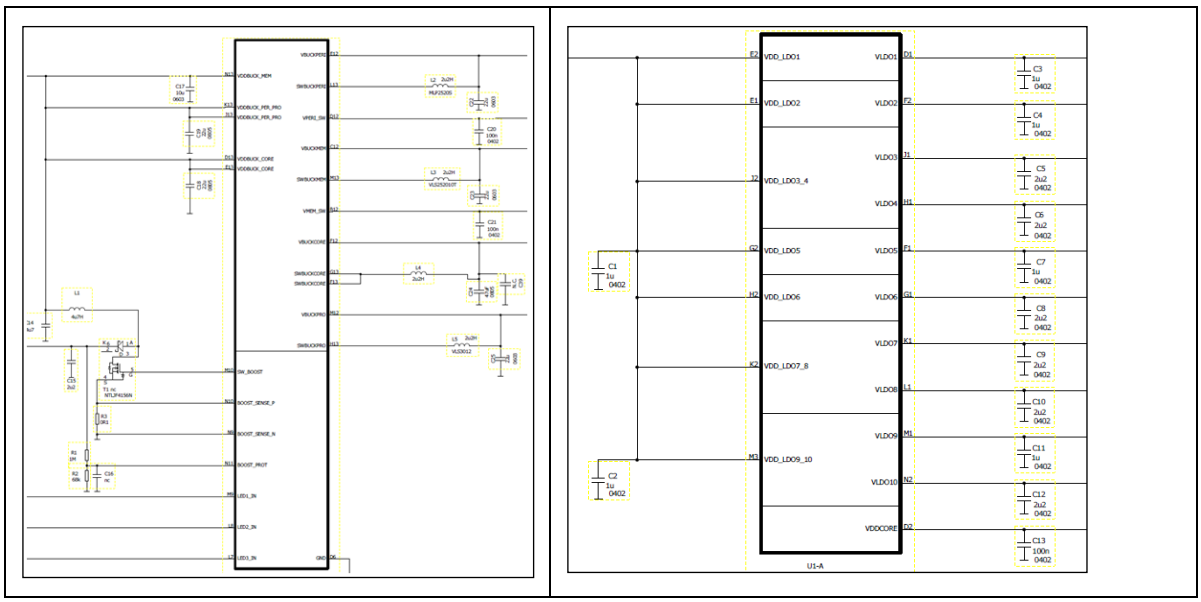


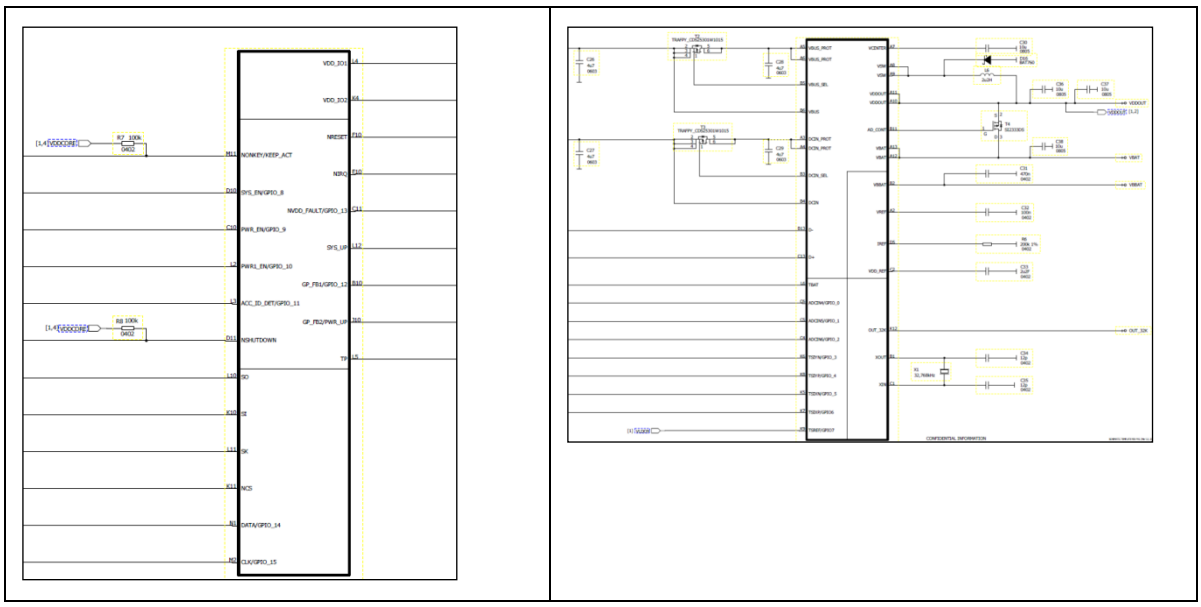
Figure 55: Transient and Static Load Regulation

28 Dialog Semiconductor 7x7 DA9053 Reference Board Bill of Materials

Qty	Reference	Part Name	Value	Package	Manufacturer	Order Number
4	C13 ,C20,C21,C32	CAPCY_0402_NEW	100n	0402	Murata	GRM155R71C104KA88D
2	C34 ,C35	CAPCY_0402_NEW	12p	0402	Murata	GRM155C1H120JZ01D
6	C1,C2,C3,C4,C7,C11	CAPCY_0402_NEW	1u	0402	Murata	GRM155R61A105KE15
7	C5,C6,C8,C9,C10,C12	CAPCY_0402_NEW	2u2	0402	Murata	GRM155R60J225ME15
1	C31	CAPCY_0402_NEW	470n	0402	Murata	GRM155R61A474KE15D
3	C22,C23,C25	CAPCY_0603_NEW	22u	0603	Murata	GRM188R60J226ME69
1	C17	CAPCY_0603_NEW	10u	0603	Murata	GRM188R60J106M
5	C14 ,C26-C29	CAPCY_0603_NEW	4u7	0603	Murata	GRM188R60J475KE19
2	C18,C19	CAPCY_0805_NEW	22u	0805	Murata	GRM21BR60J226ME39L
4	C30,C36,C37,C38	CAPCY_0805_NEW	10u	0805	Murata	GRM21BR61C106KE15
1	C24	CAPCY_0805_NEW	47U	0805	Murata	GRM21BC80E476ME15L
1	C39	CAPCY_0805_NEW	N.C.	0805	Murata	GRM21BC80G226ME39L
1	C15	CAPCY_1206_NEW	2u2	1206	Murata	GRM31CR71H225KA88
1	L1	INDY-INDUCTOR_2-4MM	4u7H	NR4018T4R7M	Taiyo Yuden	NR4018T4R7M
1	L2	INDUCTOR_VLS3012	2u2H	NR3015T2R2M	Taiyo Yuden	NR3015T2R2M
1	L3	INDUCTOR_VLS3012	2u2H	NR3015T2R2M	Taiyo Yuden	NR3015T2R2M
1	L4	INDY-INDUCTOR_2-4MM	2u2H	NR4018T2R2M	Taiyo Yuden	NR4018T2R2M
1	L5	INDUCTOR_VLS3012	2u2H	NR3015T2R2M	Taiyo Yuden	NR3015T2R2M
1	L6	INDY-INDUCTOR_2-4MM	2u2H	NR4018T2R2M	Taiyo Yuden	NR4018T2R2M
1	R1	RESY_0402_NEW	1M			
1	R2	RESY_0402_NEW	68k			
1	R3	RESY_0402_NEW	0R1			
2	VAR1,VAR2	RESY_0402	N.C.	0402	AVR-M1005C080M	
1	R6	RESY_0402_NEW	200k 1%			
2	R7,R8	RESY_0402_NEW	100k			
1	T1	TRAFNY_NTLJF4156N	FDFMA3N109	MLP6	Fairchild	Farnell order No.1324787
1	T2,T3	TRAFPY_CDS25301W1015	CSD25301W1015	WLCSP1x1.5	TI	CSD25301W1015
1	T4	TRAFPY_SI2333DS_SOT23	SI2333CDS	SOT-23	Fairchild	FDV302P
1	X1	XTAY_CC7V-T1A	32,768kHz	3,2 x 1,5mm	Micro crystal	CC7VA-T1A
1	U1	PMCY_KANGAROOPLUS	DA9053	169 ball BGA 0.5mm pitch		Supplied by Dialog.
2	J1,J2	15x2 Header	Header	RS		
1	C16	CAPCY_0402_NEW	N.C.			
1	D16	DIOSCY_BAT760_SOD323	BAT760	SOD323	NXP	

28.1 Dialog Reference Board Component Identification for Bill of Materials





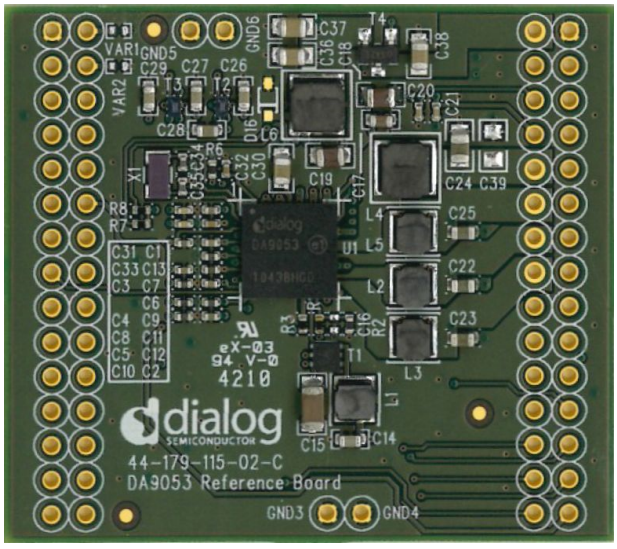
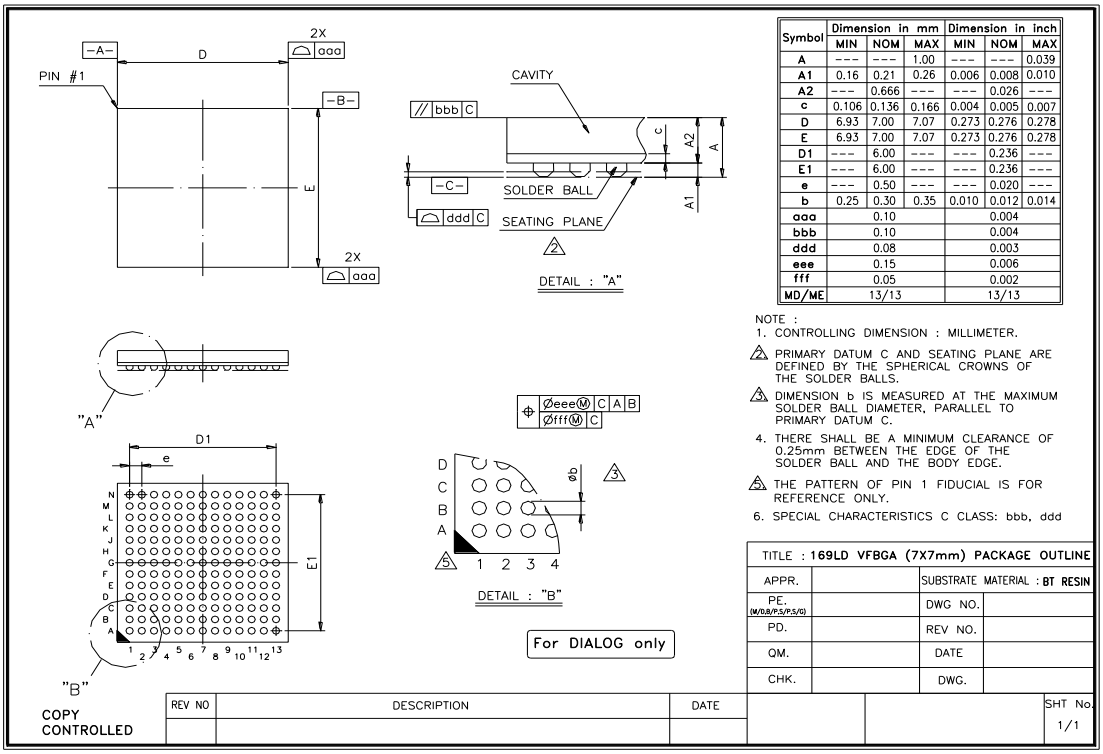


Figure 56: Dialog DA9053 Reference Board

29 Package Information

29.1 Package Outlines



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.00	---	---	0.039
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	---	0.666	---	---	0.026	---
c	0.106	0.136	0.166	0.004	0.005	0.007
D	6.93	7.00	7.07	0.273	0.276	0.278
E	6.93	7.00	7.07	0.273	0.276	0.278
D1	---	6.00	---	---	0.236	---
E1	---	6.00	---	---	0.236	---
e	---	0.50	---	---	0.020	---
b	0.25	0.30	0.35	0.010	0.012	0.014
aaa		0.10			0.004	
bbb		0.10			0.004	
ddd		0.08			0.003	
eee		0.15			0.006	
fff		0.05			0.002	
MD/ME		13/13			13/13	

Figure 57: 169LD-VFBGA (7 x 7 mm) Package Outline Drawing

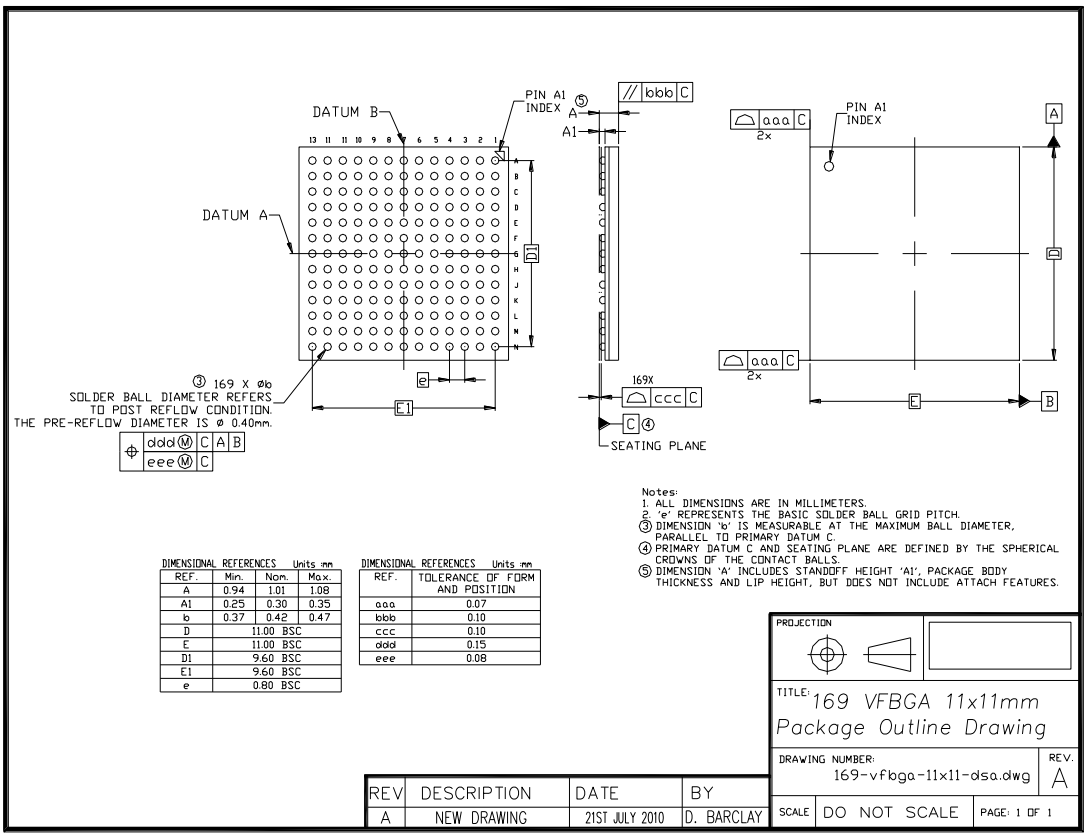


Figure 58: 169-VFBGA (11 x 11 mm) Package Drawing

30 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult Dialog Semiconductor's customer portal or your local sales representative.

Table 67: Ordering Information

Part Number	Package	Shipment Form	Pack Quantity
DA9053-xxC51	7 x 7 169 bump BGA Pb-free/green	Tray	260
DA9053-xxC52	7 x 7 169 bump BGA Pb-free/green	T&R	3,000
DA9053-xxHA1	11 x 11 169 bump BGA Pb-free/green	Tray	168
DA9053-xxHA2	11 x 11 169 bump BGA Pb-free/green	T&R	2000
AEC Q100 Grade 3			
DA9053-xxHA1-A	11 x 11 169 bump BGA Pb-free/green	Tray	168
DA9053-xxHA2-A	11 x 11 169 bump BGA Pb-free/green	T&R	2000

30.1 Variants Ordering Information

DA9053 supports delivery of customised variants indicated by xx in the part number above, please contact your local Dialog Semiconductor office or representative to discuss requirements.

Revision History

Revision	Date	Description
1.0	01-Jun-2010>	Initial version.
2.0	17-Oct-2013-	Minor updates
2.1	30-Aug-2016-	Updated to latest template and cosmetic changes

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.dialog-semiconductor.com.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

Disclaimer

RoHS Compliance

Dialog Semiconductor's suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

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