16-Channel White LED Controller for LCD Backlight

1 Description

The AS3824 is a 16 channel high precision LED controller for use in LCD-backlight panels. Dynamic power feedback controls the external power supply to guarantee best efficiency. One high accurate global 10 bit DAC can be used to set the LED current as well as each channel has its own additional 8 bit DAC to boost the dynamic range of LED Backlight systems.

Each channel is equipped with an independent PWM generator which can also be synchronized to an external synchronization signal (VSYNC).

A fast mode supports minimum PWM duty cycle operation which helps to further reduce the energy consumption of modern LED Backlight systems.

The PWM generator clock can be generated internally (DPLL) or an external clock source can be connected to the HSYNC input.

Built-in safety features include thermal shutdown as well as open and short LED detection. The device is programmable via serial interface (SPI).

2 Features

- Supports all LED backlight topologies
  - » No limit of VLED or ILED, device is not exposed to high voltage/high current
- Optimum power savings through local dimming
  - » 16 fully flexible 12 bit PWM generators (period, high time, delay, reverse)
- One global highly accurate 10 bit DAC which sets the LED current (±0.5% accuracy)
- High dynamic range boost function
  - » 16 independent 8 bit DACs can be used to boost/ decrease LED current within certain frames
- Global dimming mode option
  - » AS3824E/E1 are pre-programmed as external PWM mode (DPWM mode), V_{SYNC} pin is used as PWM input. AS3824A/A1 are pre-programmed as SPI mode
- VSYNC and HSYNC inputs, as well as integrated digital PLL for synchronization with TV frame
- Lowest BOM
  - » Due to 2 pin concept of the output channel: no HV protection, no cascade FETs
- Feedback function is compatible to every DC-DC architecture and configurable via SPI
- Short/OPEN LED detection, temperature shutdown, register lock/unlock, SPI transfer checksum

3 Applications

- HD TVs
- UHD TVs
- LCD Monitors

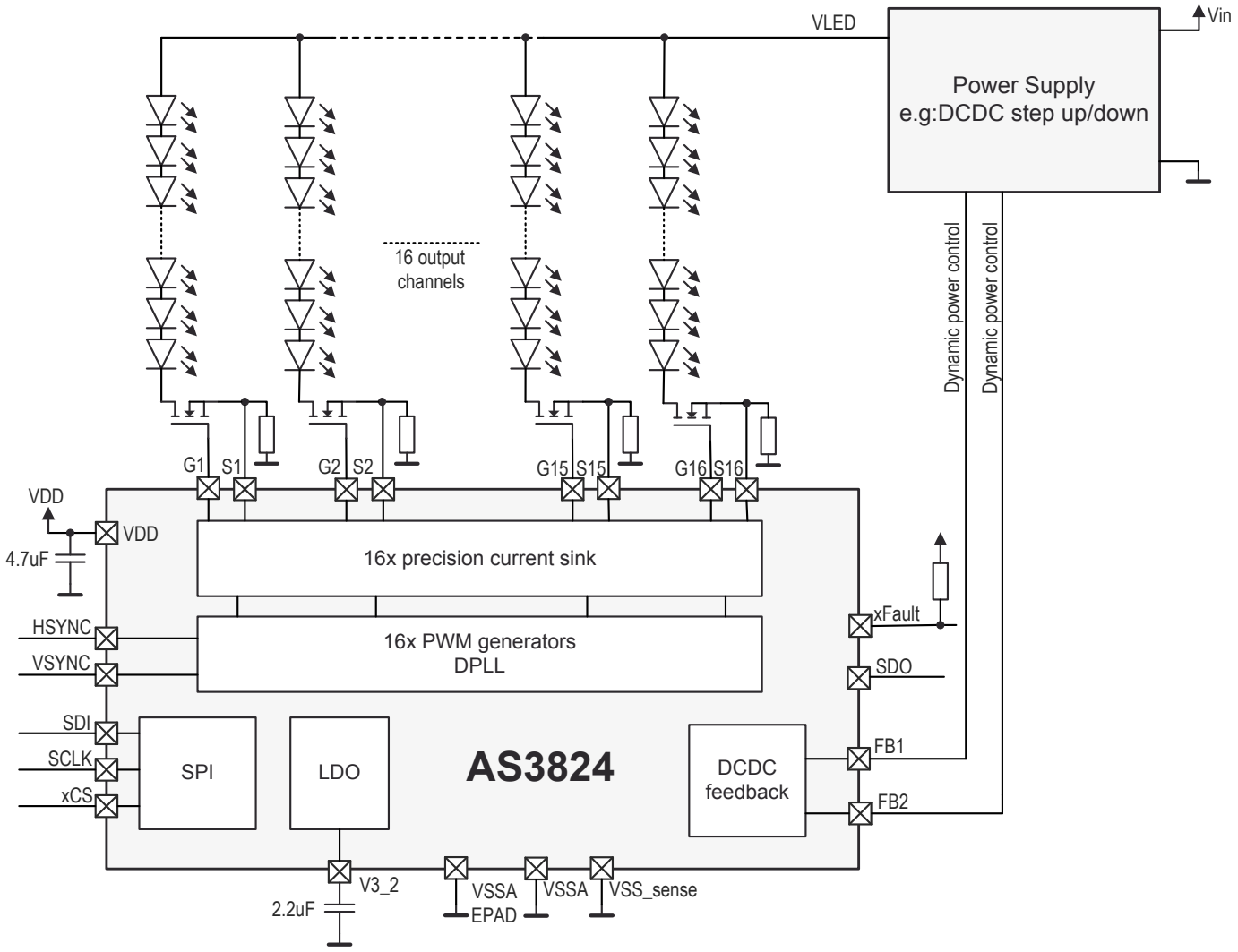


Figure 3.1 : AS3824 Typical Application

4 Pinout Description

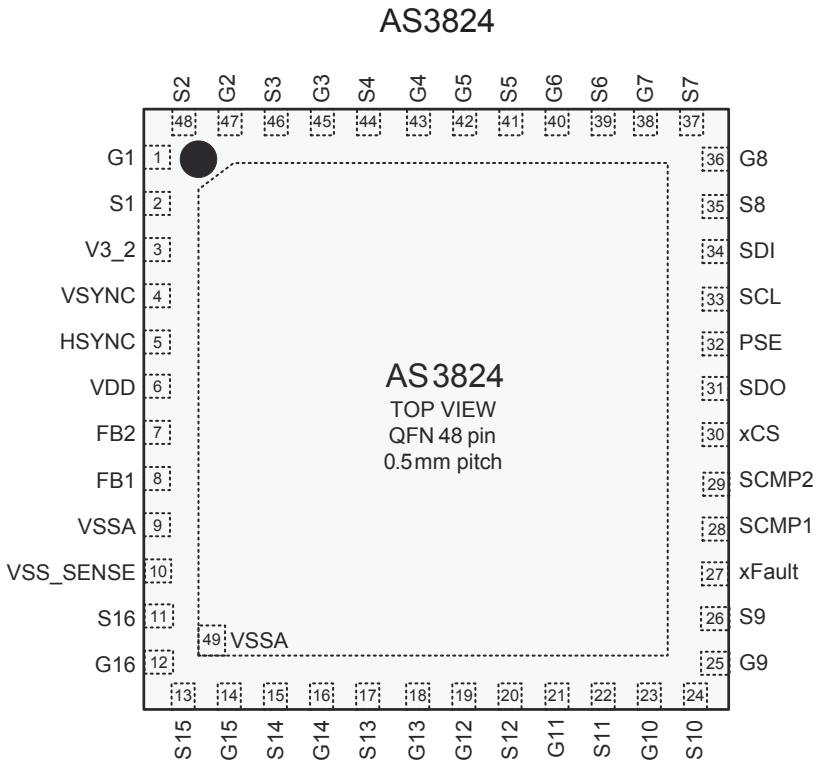


Figure 4.1 : Pin Diagram of AS3824 (Top View)

Pin Number	Pin Name	Type	Pin Description	If Not Used
1	G1	A_I/O	Connect to gate of external transistor	Connect to S1
2	S1	A_I/O	Connect to source of external transistor	Connect to G1
3	V3_2	P	Digital supply output. Connect 2.2uF capacitor to GND	
4	VSYNC	DI_PD	Vertical sync frequency. PWM generator reset	Leave open
5	HSYNC	DI_PD	Clock input for PWM generators	Leave open
6	VDD	P	Supply Voltage input Connect 4.7uF bypass capacitor to GND	
7	FB2	A_I/O	Power supply feedback output 2	Leave open
8	FB1	A_I/O	Power supply feedback output 1	Leave open
9	VSSA	P	GND	
10	VSS_ SENSE	P	GND	
11	S16	A_I/O	Connect to source of external transistor	Connect to G16

4 Pinout Description (cont'd)

Pin Number	Pin Name	Type	Pin Description	If Not Used
12	G16	A_I/O	Connect to gate of external transistor	Connect to S16
13	S15	A_I/O	Connect to source of external transistor	Connect to G15
14	G15	A_I/O	Connect to gate of external transistor	Connect to S15
15	S14	A_I/O	Connect to source of external transistor	Connect to G14
16	G14	A I/O	Connect to gate of external transistor	Connect to S14
17	S13	A I/O	Connect to source of external transistor	Connect to G13
18	G13	A I/O	Connect to gate of external transistor	Connect to S13
19	G12	A I/O	Connect to gate of external transistor	Connect to S12
20	S12	A I/O	Connect to source of external transistor	Connect to G12
21	G11	A I/O	Connect to gate of external transistor	Connect to S11
22	S11	A I/O	Connect to source of external transistor	Connect to G11
23	G10	A I/O	Connect to gate of external transistor	Connect to S10
24	S10	A I/O	Connect to source of external transistor	Connect to G10
25	G9	A I/O	Connect to gate of external transistor	Connect to S9
26	S9	A I/O	Connect to source of external transistor	Connect to G9
27	xFAULT	DO_OD	Open drain fault output, connect pull-up to V3_2	Leave open
28	SCMP1	AI	Input of short comparator 1	Connect to VSS
29	SCMP2	AI	Input of short comparators 2	Connect to VSS
30	xCS	DI_PU	SPI interface chip select	Leave open
31	SDO	DO	SPI interface data output. Tristate output	Leave open
32	PSE	DI	Phase Shift enable	Connect to VSS
33	SCL	DI_PD	SPI interface clock	Leave open
34	SDI	DI_PD	SPI interface data input	Leave open
35	S8	A I/O	Connect to source of external transistor	Connect to G8
36	G8	A I/O	Connect to gate of external transistor	Connect to S8
37	S7	A I/O	Connect to source of external transistor	Connect to G7
38	G7	A I/O	Connect to gate of external transistor	Connect to S7
39	S6	A I/O	Connect to source of external transistor	Connect to G6
40	G6	A I/O	Connect to gate of external transistor	Connect to S6

4 Pinout Description (cont'd)

Pin Number	Pin Name	Type	Pin Description	If Not Used
41	S5	A I/O	Connect to source of external transistor	Connect to G5
42	G5	A I/O	Connect to gate of external transistor	Connect to S5
43	G4	A I/O	Connect to gate of external transistor	Connect to S4
44	S4	A I/O	Connect to source of external transistor	Connect to G4
45	G3	A I/O	Connect to gate of external transistor	Connect to S3
46	S3	A I/O	Connect to source of external transistor	Connect to G3
47	G2	A I/O	Connect to gate of external transistor	Connect to S2
48	S2	A I/O	Connect to source of external transistor	Connect to G2
EP	VSSA	P	Exposed PAD. Connect to VSSP	

Note 1. If an output channel "X" is not used, connect unused pins Gx and Sx together.

A_I/O: Analog pin
P: Power pin
DO: Digital Output
DO_OD: Digital Output Open Drain
DI: Digital Input
DI_PU: Digital Input with Pull Up resistor
DI_PD: Digital Input with Pull Down resistor

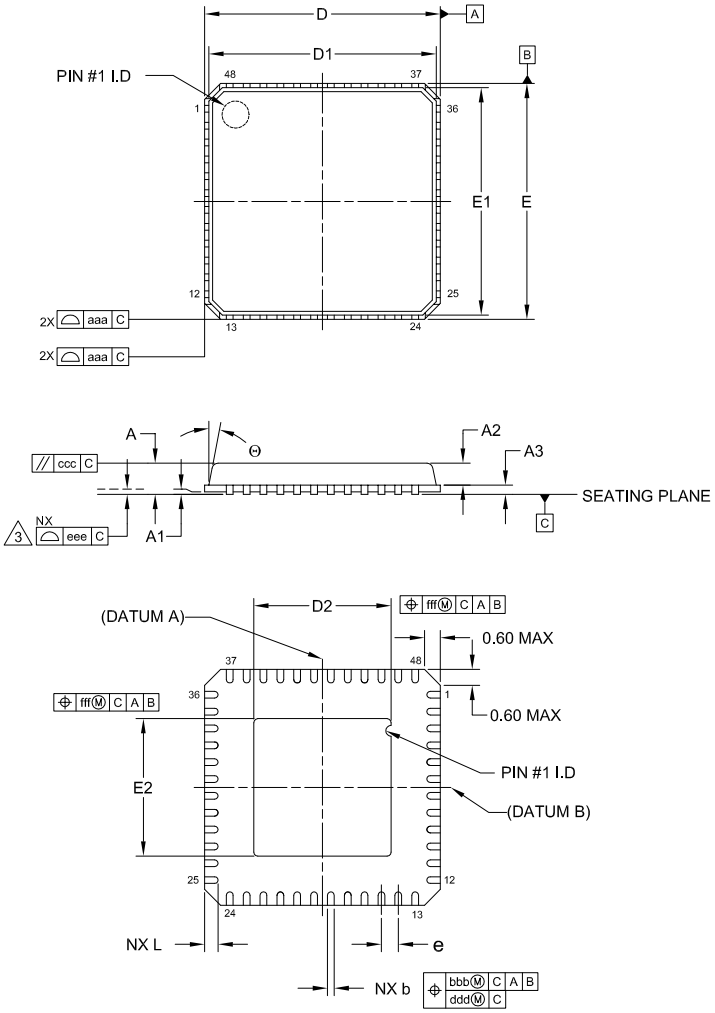
5 Absolute Maximum Ratings

Absolute maximum ratings are the parameter values or ranges which can cause permanent damage if exceeded. For maximum safe operating conditions, refer to the Electrical Characteristics section.

Parameter	Symbol	Conditions	Min	Max	Unit
Electrical Parameters					
Supply Voltage to Ground	V_{DDMAX} / V_{GND}	Applicable for pin VDD	-0.3	7	V
Maximum Voltage Analog pins	V_{ANAMAX}	Applicable for pins: FB1, FB2, G1-G16, S1-S16, VSYNC, HSYNC	-0.3	7	V
Maximum Voltage Digital pins	V_{DIGMAX}	Applicable for pins: V3_2, SDI, SDO, SCL, xCS, SCMP1, SCMP2, xFAULT, PSE	-0.3	5	V
Input Current (latch-up immunity)	I_{SCR}	JEDEC JESD78D Nov 2011	±100		mA
Electrostatic Discharge					
Electrostatic Discharge HBM	ESD_{HBM}	JS-001-2012	±2000		V
Electrostatic Discharge CDM	ESD_{CDM}	JEDEC JESD22-C101F Oct 2013	±500		V
Electrostatic Discharge MM	ESD_{MM}	JESD22-A115C	±200		V
Temperature Ranges and Storage Conditions					
Junction to Ambient Thermal Resistance	R_{THJA}	R_{THJA} typical 35°C/W			°C/W
Operating Junction Temperature	T_J		-20	115	°C
Storage Temperature Range	T_{STRG}		-55	150	°C
Package Body Temperature	T_{BODY}	IPC/JEDEC J-STD-020 The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices.” The lead finish for Pb-free leaded packages is “Matte Tin” (100% Sn)		260	°C
Relative Humidity (non-condensing)	RH_{NC}		5	85	%
Moisture Sensitivity Level	MSL	Maximum floor life time of 168h	3		

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6 Physical Dimensions



REF.	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0	0.02	0.05
A2	-	0.65	1.00
A3		0.20 REF	
L	0.35	0.40	0.45
Θ	0°	-	14°
b	0.18	0.25	0.30
D		7.00 BSC	
E		7.00 BSC	
e		0.50 BSC	
D2	4.00	4.10	4.20
E2	4.00	4.10	4.20
D1	-	6.75 BSC	-
E1	-	6.75 BSC	-
aaa	-	0.15	-
bbb	-	0.10	-
ccc	-	0.10	-
ddd	-	0.05	-
eee	-	0.08	-
fff	-	0.10	-
N		48	

NOTE:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES)
3. COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.
4. RADIUS ON TERMINAL IS OPTIONAL.
5. N IS THE TOTAL NUMBER OF TERMINALS.

Figure 6.1 : QFN-48 package outline drawing

7 Ordering Information

Part Number	Ordering Code	Package	Description
AS3824A1	AS3824A1-ZQFT	48-Pin QFN	Tape & Reel[1]
AS3824E1	AS3824E1-ZQFT	48-Pin QFN	Tape & Reel[1]

Note 1. Tape & Reel packing quantity is 4,000/reel. Minimum packing quantity is 4,000.

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