DATASHEET

AT25SF128A

128 Mbit Serial NOR Flash Memory with Dual and Quad I/O Support

Features

- Single voltage operation with range of 2.7 V to 3.6 V
- Serial Peripheral Interface (SPI) compatible support
  - Supports SPI modes 0 and 3
  - Supports dual and quad output read
  - 133 MHz maximum operating frequency
- Read Operations
  - 70 MHz normal read
  - 120 MHz fast read
  - 133 MHz Quad Output fast read
  - Dual I/O data transfer rate up to 240 Mbps
  - Quad I/O data transfer rate up to 480 Mbps
  - Quad Output data transfer rate up to 532 Mbps
  - Continuous read with 8/16/32/64-byte wrap
- Flexible, optimized erase architecture for code and data storage applications
  - Sector erase 4 kbytes
  - Block erase 32 kbytes, and 64 kbytes
  - Full chip erase
  - Erase suspend and resume
- Flexible programming
  - Byte/Page program (1 to 256 Bytes)
  - Program suspend and resume
- Fast program and erase times
  - 0.6 ms typical page (256 byte) program time
  - 70 ms typical 4-kbyte block erase time
  - 150 ms typical 32-kbyte block erase time
  - 250 ms typical 64-kbyte block erase time
  - Full chip erase: 60 s typical
- Hardware and software Write Protection
  - Hardware-controlled locking of protected sector via $\overline{WP}$ pin
  - Three 256-byte OTP-capable security registers
  - Write protect all or part of memory via software with top/bottom block selection
- Serial Flash Discoverable Parameter (SFDP) register
- Low power dissipation
  - 13 µA standby current
  - 2 µA deep power down current
- Endurance 100K program/erase cycles
- Data Retention: 20 years
- Temperature Range:
  - Industrial (-40 ^{o}C to 85 ^{o}C)
- Industry standard green (Pb/Halide-free/RoHS compliant) package options
  - 8-lead 0.208” Wide SOIC (8S4)
  - 8-pad (5 x 6 x 0.6 mm) UDFN (8MA1)
  - 24-ball (5 x 5 array) TFBGA (24CC)

Adesto™

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1. Product Overview

The Adesto® AT25SF128A is a 128 Mb Serial Peripheral Interface (SPI) Flash memory device designed for use in a wide variety of high-volume consumer based applications in which program code is shadowed from Flash memory into embedded or external RAM for execution. The flexible erase architecture of the AT25SF128A is ideal for data storage as well, eliminating the need for additional data storage devices.

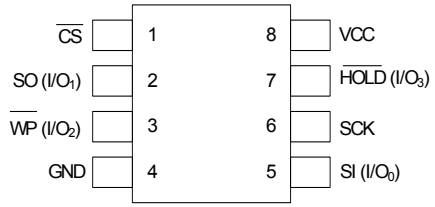
The SPI clock frequencies support up to 133 MHz enabling data transfers up to 532 Mbits/s for Quad Output operations.

The AT25SF128A array is organized into 65,536 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time using the Page Program instructions. Pages can be erased in 4 kbytes, 32 kbytes, or 64 kbytes blocks, or the entire chip.

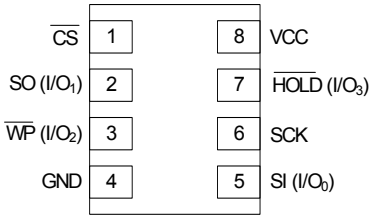
The devices operate on a single 2.7 V to 3.6 V power supply with current consumption as low as 2 µA for Deep Power Down. All devices offered in space-saving packages. The device supports JEDEC standard manufacturer and device identification with three 256-byte secure OTP registers.

2. Package Pinouts

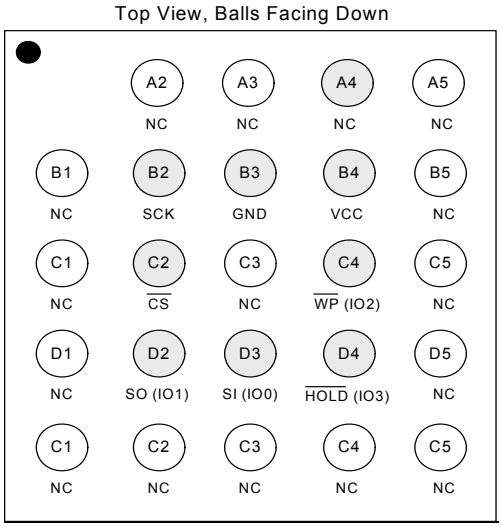
Figure 2-1 show the package pinouts for the following devices.



8-lead 8S1 SOIC Package (208-mil)



8-pad UDFN Package



24-ball TFBGA Package

Figure 2-1. Adesto AT25SF128A Flash Memory Package Types

3. Pin Descriptions

During all operations, VCC must be held stable and within the specified valid range: VCC (min) to VCC (max).

All of the input and output signals must be held high or low (according to voltages of VIH, VOH, VIL or VOL, see Section 9.6, DC Electrical Characteristics). These pins are described below.

3.1 Pin Summary

Table 3-1. AT25SF128A Pin Names

Pin Name	I/O	Description
$\overline{CS}$	I	Chip select.
SO (IO_1)	I/O	Serial Output for single bit data Instructions. IO_1 for dual or quad Instructions.
$\overline{WP}$ (IO_2)	I/O	Write Protect in single bit or dual data Instructions. IO_2 in quad mode. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for quad Instructions.
GND		Ground.
SI (IO_0)	I/O	Serial input for single bit data Instructions. IO_0 for dual or quad Instructions.
SCLK	I	Serial clock.
$\overline{HOLD}$ (IO_3)	I/O	Hold (pause) serial transfer in single bit or dual data Instructions. IO_3 in Quad-I/O mode. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad Instructions.
VCC		Core and I/O power supply.

3.2 Chip Select ($\overline{CS}$)

The chip select signal indicates when a instruction for the device is in process and the other signals are relevant for the memory device. When the $\overline{CS}$ signal is at the logic high state, the device is not selected and all input signals are ignored and all output signals are high impedance. Unless an internal *Program*, *Erase* or *Write Status Registers* embedded operation is in progress, the device remains in the Standby Power mode. Driving the $\overline{CS}$ input to logic low state enables the device, placing it in the *Active Power* mode. After Power Up, a falling edge on $\overline{CS}$ is required prior to the start of any instruction.

3.3 Serial Clock (SCLK)

This input signal provides the synchronization reference for the SPI interface. Instructions, addresses, or data input are latched on the rising edge of the SCLK signal. Data output changes after the falling edge of SCLK.

3.4 Serial Input (SI or I/O_0)

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and data to be programmed. Values are latched on the rising edge of serial SCK clock signal.

SI becomes I/O_0 an input and output during Dual and Quad Instructions for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial SCK clock signal) as well as shifting out data (on the falling edge of SCK).

3.5 Serial Data Output (SO or I/O_1)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of the serial SCK clock signal.

The SO pin becomes an I/O pin (I/O_1) during Dual and Quad Instructions for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial SCK clock signal) as well as shifting out data (on the falling edge of SCK).

3.6 Write Protect ($\overline{WP}$ or I/O_2)

When $\overline{WP}$ is driven low, while the Status Register Protect bits (SRP1 and SRP0) of the Status Registers are set to 0 and 1 respectively, it is not possible to write to the Status Registers. This prevents any alteration of the Status Registers. As a consequence, all the data bytes in the memory area that are protected by the Block Protect, TB, SEC, and CMP bits in the status registers, are also hardware protected against data modification while $\overline{WP}$ remains low. The $\overline{WP}$ function is not available when the Quad mode is enabled (QE bit in Status Register 2 = 1).

The $\overline{WP}$ function is replaced by I/O_2 for input and output during Quad mode for receiving addresses, and data to be programmed (values are latched on rising edge of the SCK signal) as well as shifting out data (on the falling edge of SCK). $\overline{WP}$ has an internal pull-up resistance; when unconnected; $\overline{WP}$ is at VIH and may be left unconnected in the host system if not used for Quad mode.

3.7 Hold ($\overline{HOLD}$ or I/O_3)

The $\overline{HOLD}$ function is only available when QE = O. If QE = 1, The $\overline{HOLD}$ function is disabled and the pin acts as dedicated data I/O pin.

The $\overline{HOLD}$ signal goes low to stop any serial communications with the device, but doesn't stop the operation of write status register, programming, or erasing in progress.

3.8 VCC Power Supply

VCC is the supply voltage. It is the single voltage used for all device functions including read, program, and erase.

3.9 GND Ground

GND is the ground reference for the VCC supply voltage.

4. Block/Sector Addresses

Table 4-1. Block/Sector Addresses of AT25SF128A

Memory Density	Block (64k byte)	Block (32k byte)	Sector No.	Sector Size (kbytes)	Address Range
128Mbit	Block 0	Half block 0	Sector 0	4	000000h - 000FFFh
			:	:	:
			Sector 7	4	007000h - 007FFFh
		Half block 1	Sector 8	4	008000h - 008FFFh
			:		:
			Sector 15	4	00F000h - 00FFFFh
	Block 1	Half block 2	Sector 16	4	010000h - 010FFFh
			:	:	:
			Sector 23	4	017000h - 017FFFh
		Half block 3	Sector 24	4	018000h - 018FFFh
			:	:	:
			Sector 31	4	01F000h - 01FFFFh
	:	:	:	:	:
	Block 254	Half block 508	Sector 4064	4	FE0000h - FE0FFFh
			:	:	:
			Sector 4071	4	FE7000h - FE7FFFh
		Half block 509	Sector 4072	4	FE8000h - FE8FFFh
			:	:	:
			Sector 4079	4	FEF000h - FEFFFFh
	Block 255	Half block 510	Sector 4080	4	FF0000h - FF0FFFh
			:	:	:
			Sector 4087	4	FF7000h - FF7FFFh
		Half block 511	Sector 4088	4	FF8000h - FF8FFFh
			:	:	:
			Sector 4095	4	FFF000h - FFFFFFh

5. SPI Operation

5.1 Standard SPI Instructions

The AT25SF128A features a 4-pin serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select ($\overline{CS}$), Serial Data Input (SI) and Serial Data Output (SO). SPI bus modes 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

5.2 Dual SPI Instructions

The AT25SF128A supports Dual SPI operation when using the *Dual Output Fast Read* (3Bh), *Dual I/O Fast Read* (BBH) and *Read Manufacture ID/Device ID Dual I/O* (92h) instructions. These instructions allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI instruction the SI and SO pins become bidirectional I/O pins: I/O_0 and I/O_1 respectively.

5.3 Quad SPI Instructions

The AT25SF128A supports Quad SPI operation when using the *Quad Output Fast Read* (6Bh), *Quad I/O Fast Read* (EBH), *Quad I/O Word Fast Read* (E7h), *Read Manufacture ID/Device ID Quad I/O* (94h) and *Quad Page Program* (32h) instructions. These instructions allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI instruction the SI and SO pins become bidirectional I/O pins: I/O_0 and I/O_1, and /WP and $\overline{HOLD}$ pins become I/O_2 and I/O_3. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register to be set.

6. Operating Features

6.1 Supply Voltage

6.1.1 Operating Supply Voltage

Prior to selecting the memory and issuing instructions to it, a valid and stable VCC voltage within the specified VCC (min) / VCC (max) range must be applied. In order to secure a stable DC supply voltage, it is recommended to decouple the VCC line with capacitors (usually 10 nF to 100 nF in parallel) placed close to the VCC/GND package pins. This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W).

6.1.2 Power-up Conditions

When the power supply is turned on, VCC rises continuously from GND to VCC. During this time, the Chip Select ($\overline{CS}$) line is not allowed to float but should follow the VCC voltage, it is therefore recommended to connect the $\overline{CS}$ line to VCC via a pull-up resistor.

In addition, the $\overline{CS}$ input is both edge sensitive and level sensitive. After power-up, the device does not become selected until a falling edge is first detected on $\overline{CS}$. This ensures that $\overline{CS}$ must have been High, prior to going Low to start the first operation.

6.1.3 Device Reset

In order to prevent inadvertent Write operations during power-up (continuous rise of VCC), a power on reset (POR) circuit is included. At Power-up, the device does not respond to any instruction until VCC has reached the power on reset threshold voltage (this threshold is lower than the minimum VCC operating voltage defined by the DC operating ranges).

When VCC has passed the POR threshold, the device is reset.

6.1.4 Power-down

At Power-down (continuous decrease in VCC), as soon as VCC drops from the normal operating voltage to below the power on reset threshold voltage, the device stops responding to any instruction sent to it. During Power-down, the device must be deselected (Chip Select ($\overline{CS}$) should be allowed to follow the voltage applied on VCC) and in Standby Power mode (that is there should be no internal Write cycle in progress).

6.2 Active Power and Standby Power Modes

When Chip Select ($\overline{CS}$) is low, the device is selected and in the Active Power mode and consuming current (ICC).

When Chip Select ($\overline{CS}$) is high, the device is deselected. If a Write cycle is not currently in progress, the device enters the Standby Power mode, and the current consumption drops to ICC1.

6.3 Hold Condition

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without resetting the clocking sequence. During the Hold condition, the Serial Data Output (SO) is high impedance, and Serial Data Input (SI) and Serial Clock (SCLK) are don't care.

To enter the Hold condition, the device must be selected, with Chip Select ($\overline{CS}$) low. Normally, the device remains selected for the duration of the Hold condition. Deselecting the device while it is in the Hold condition, has the effect of resetting the state of the device, and this mechanism can be used if it is required to reset any processes that had been in progress.

The Hold condition starts when the Hold ($\overline{HOLD}$) signal is driven Low at the same time as Serial Clock (SCLK) already being Low (as shown in Figure 6-1).

The Hold condition ends when the Hold ($\overline{HOLD}$) signal is driven High at the same time as Serial Clock (C) already being Low. Figure 6-1 also shows what happens if the rising and falling edges are not timed to coincide with Serial Clock (SCLK) being Low.

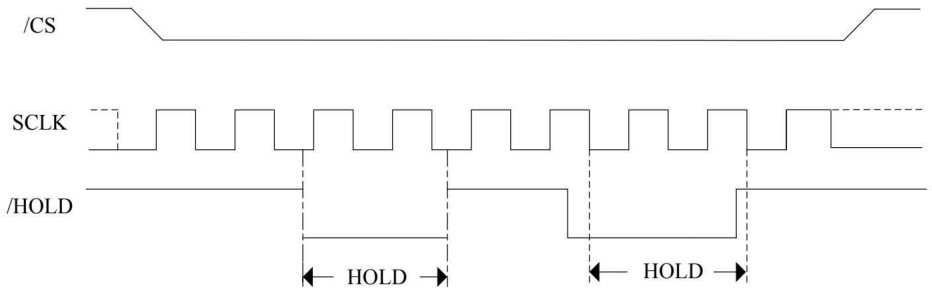


Figure 6-1. Hold Condition Activation

6.4 Status Register

6.4.1 Status Register Table

The following diagram shows the layout of the Status Register bits.

Table 6-1. Status Register Byte 3

S23	S22	S21	S20	S19	S18	S17	S16
Reserved	DRV1	DRV0	Reserved	Reserved	Reserved	Reserved	Reserved

Table 6-2. Status Register Byte 2

S15	S14	S13	S12	S11	S10	S9	S8
SUS1	CMP	LB3	LB2	LB1	SUS2	QE	SRP1

Table 6-3. Status Register Byte 1

S7	S6	S5	S4	S3	S2	S1	S0
SRP0	BP4	BP3	BP2	BP1	BP0	WEL	WIP

6.4.2 Status and Control Bits

6.4.2.1 WIP bit

The Write in Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

6.4.2.2 WEL bit

The Write Enable Latch bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase instruction is accepted.

6.4.2.3 BP4, BP3, BP2, BP1, BP0 bits

The Block Protect (BP4, BP3, BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions. These bits are written with the Write Status Register instruction.

- When the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are set to 1, the relevant memory becomes protected against Page Program, Sector Erase and Block Erase instructions.
- The Block Protect (BP4, BP3, BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set.
- The Chip Erase (CE) instruction is executed if the Block Protect (BP2, BP1, BP0) bits are 0 and CMP = 0 or the Block Protect (BP2, BP1, BP0) bits are 1 and CMP = 1.

6.4.2.4 SRP1, SRP0 bits

The Status Register Protect (SRP1 and SRP0) bits are non-volatile Read/Write bits in the status register. The SRP bits control the method of write protection: software protection, hardware protection, or power supply lock-down.

6.4.2.5 QE bit

The Quad Enable (QE) bit is a non-volatile Read/Write bit in the Status Register that allows Quad operation. When the QE bit is set to 0 (Default) the $\overline{WP}$ pin and $\overline{HOLD}$ pin are enable. When the QE pin is set to 1, the Quad I/O_2

and I/O_3 pins are enabled. (The QE bit should never be set to 1 during standard SPI or Dual SPI operation if the $\overline{WP}$ or $\overline{HOLD}$ pins directly to the power supply or ground).

6.4.2.6 LB3/LB2/LB1 bit

The LB bits are non-volatile One Time Program (OTP) bits in Status Register (S13 - S11) that provide the write protect control and status to the Security Registers. The default state of LBx is 0, the security registers are unlocked. The LBx bits can be set to 1 individually using the Write Register instruction. The LBx bits are One Time Programmable. Once they are set to 1, the Security Registers become read-only permanently.

6.4.2.7 CMP bit

The CMP bit is a non-volatile Read/Write bit in the Status Register (S14). It is used in conjunction the SEC and BP0 bits to provide more flexibility for the array protection. Please see the Status registers Memory Protection table for details. The default setting is CMP = 0.

6.4.2.8 SUS1/SUS2 bit

The SUS1 and SUS2 bits are read only bits in the status register2 (S15 and S10) that are set to 1 after executing an Erase/Program Suspend (75h) instruction (The Erase Suspend sets SUS1 to 1, and the Program Suspend sets SUS2 to 1). The SUS1 and SUS2 bits are cleared to 0 by Erase/Program Resume (7Ah) instruction as well as a power-down, power-up cycle.

6.4.2.9 DRV1/DRV0

The DRV1 and DRV0 bits are used to determine the output driver strength for the Read instruction.

Table 6-4. DRV1 / DRV0 Bit Encoding

DRV1, DRV0	Driver Strength
00	100%(default)
01	75%
10	50%
11	25%

6.4.3 Status Register Protect Table

The Status Register Protect (SRP1 and SRP0) bit are non-volatile Read/Write bits in the Status Register. The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable protection.

Table 6-5. Status Register Protect Table

SRP1	SRP0	$\overline{WP}$	Status Register	Description
0	0	X	Software Protected	The Status Register can be written to after a Write Enable instruction, WEL = 1 (Factory Default).
0	1	0	Hardware Protected	$\overline{WP}$ = 0, the Status Register locked and cannot be written.

Table 6-5. Status Register Protect Table *(continued)*

SRP1	SRP0	$\overline{WP}$	Status Register	Description
0	1	1	Hardware Unprotected	$\overline{WP}$ = 1, the Status Register is unlocked and can be written to after a Write Enable instruction, WEL = 1.
1	0	X	Power Supply Lock-Down(1)	Status Register is protected and cannot be written to again until the next Power-Down, Power-Up cycle.
1	1	X		Not allowed.

Notes:

1. When SRP1, SRP0 = (1, 0), a Power-Down, Power-Up cycle will change SRP1, SRP0 to (0, 0) state.

6.4.4 Write Protect Features

1. Software Protection: The Block Protect (BP4, BP3, BP2, BP1, BP0) bits define the section of the memory array that can be read but not change.
2. Hardware Protection: $\overline{WP}$ going low to protected the writable bits of Status Register.
3. Deep Power-Down: In Deep Power-Down mode, all instructions are ignored except the *Release from Deep Power-Down Mode* instruction.
4. Write Enable: The Write Enable instruction is set the Write Enable Latch (WEL) bit. The WEL bit is reset under any of the following conditions:
   - Power -up
   - Write Disable
   - Write Status Register
   - Page Program
   - Sector Erase/Block Erase/Chip Erase
   - Software Reset

6.4.5 Status Register Memory Protection

6.4.5.1 Protect Table

Table 6-6. AT25SF128A Status Register Memory Protection (CMP = 0)

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	252 to 255	FC0000h - FFFFFFh	256 kB	Upper 1/64
0	0	0	1	0	248 to 255	F80000h - FFFFFFh	512 kB	Upper 1/32
0	0	0	1	1	240 to 255	F00000h - FFFFFFh	1 MB	Upper 1/16
0	0	1	0	0	224 to 255	E00000h - FFFFFFh	2 MB	Upper 1/8
0	0	1	0	1	192 to 255	C00000h - FFFFFFh	4 MB	Upper 1/4
0	0	1	1	0	128 to 255	800000h - FFFFFFh	8 MB	Upper 1/2
0	1	0	0	1	0 to 3	000000h - 03FFFFh	256 kB	Upper 1/64
0	1	0	1	0	0 to 7	000000h - 07FFFFh	512 kB	Upper 1/32
0	1	0	1	1	0 to 15	000000h - 0FFFFFh	1 MB	Upper 1/16
0	1	1	0	0	0 to 31	000000h - 1FFFFFh	2 MB	Upper 1/8
0	1	1	0	1	0 to 63	000000h - 3FFFFFh	4 MB	Upper 1/4
0	1	1	1	0	0 to 127	000000h - 7FFFFFh	8 MB	Upper 1/2
X	X	1	1	1	0 to 255	000000h - FFFFFFh	16 MB	ALL
1	0	0	0	1	255	FFF000h - FFFFFFh	4 kB	Top Block
1	0	0	1	0	255	FFE000h - FFFFFFh	8 kB	Top Block
1	0	0	1	1	255	FFC000h - FFFFFFh	16 kB	Top Block
1	0	1	0	X	255	FF8000h - FFFFFFh	32 kB	Top Block
1	0	1	1	0	255	FF8000h - FFFFFFh	32 kB	Top Block
1	1	0	0	1	0	000000h - 000FFFh	4 kB	Bottom Block
1	1	0	1	0	0	000000h - 001FFFh	8 kB	Bottom Block
1	1	0	1	1	0	000000h - 003FFFh	16 kB	Bottom Block
1	1	1	0	X	0	000000h - 007FFFh	32 kB	Bottom Block
1	1	1	1	0	0	000000h - 007FFFh	32 kB	Bottom Block

Table 6-7. AT25SF128A Status Register Memory Protection (CMP = 1)

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	X	0	0	0	0 to 255	000000h - FFFFFFh	ALL	ALL
0	0	0	0	1	0 to 251	000000h - FBFFFFh	16128 kB	Lower 63/64
0	0	0	1	0	0 to 247	000000h - F7FFFFh	15872 kB	Lower 31/32
0	0	0	1	1	0 to 239	000000h - EFFFFFh	15 kbytes	Lower 15/16
0	0	1	0	0	0 to 223	000000h - DFFFFFh	14 MB	Lower 7/8
0	0	1	0	1	0 to 191	000000h - BFFFFFh	12 MB	Lower 3/4
0	0	1	1	0	0 to 127	000000h - 7FFFFFh	8 MB	Lower 1/2
0	1	0	0	1	4 to 255	040000h - FFFFFFh	16,128 kB	Upper 63/64
0	1	0	1	0	8 to 255	080000h - FFFFFFh	15,872 kB	Upper 31/32
0	1	0	1	1	16 to 255	100000h - FFFFFFh	15 kB	Upper 15/16
0	1	1	0	0	32 to 255	200000h - FFFFFFh	14 MB	Upper 7/8
0	1	1	0	1	64 to 255	400000h - FFFFFFh	12 MB	Upper 3/4
0	1	1	1	0	128 to 255	800000h - FFFFFFh	8 MB	Upper 1/2
X	X	1	1	1	NONE	NONE	NONE	NONE
1	0	0	0	1	0 to 255	000000h - FFEFFFh	16380 kB	L-4095/4096
1	0	0	1	0	0 to 255	000000h - FFDFFFh	16376 kB	L-2047/2048
1	0	0	1	1	0 to 255	000000h - FFBFFFh	16368 kB	L-1023/1024
1	0	1	0	X	0 to 255	000000h - FF7FFFh	16352 kB	L-511/512
1	0	1	1	0	0 to 255	000000h - FF7FFFh	16352 kB	L-511/512
1	1	0	0	1	0 to 255	001000h - FFFFFFh	16380 kB	U-4095/4096
1	1	0	1	0	0 to 255	002000h - FFFFFFh	16376 kB	U-2047/2048
1	1	0	1	1	0 to 255	004000h - FFFFFFh	16368 kB	U-1023/1024
1	1	1	0	X	0 to 255	008000h - FFFFFFh	16352 kB	U-511/512
1	1	1	1	0	0 to 255	008000h - FFFFFFh	16352 kB	U-511/512

7. Device Identification

Three legacy Instructions are supported to access device identification that can indicate the manufacturer, device type, and capacity (density). The returned data bytes provide the information as shown in the below table.

Table 7-1. AT25SF128A ID Definition

Operating Code	M7-M0	ID15-ID8	ID7-ID0
9Fh	1Fh	89h	01h
90h/92h/94h	1Fh		17h
ABh			17h

8. Instruction Descriptions

All instructions, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after $\overline{CS}$ is driven low. Then, the one byte instruction code must be shifted in to the device, most significant bit first on SI, each bit being latched on the rising edges of SCLK.

See Table 8-1, every instruction sequence starts with a one-byte instruction code. Depending on the instruction, this might be followed by address bytes, data bytes, both, or none. The $\overline{CS}$ pin must be driven high after the last bit of the instruction sequence has been shifted in.

For the *Read*, *Fast Read*, *Read Status Register*, *Release from Deep Power Down*, and *Read Device ID* instructions, the shifted-in instruction sequence is followed by a data out sequence. The $\overline{CS}$ pin can be driven high after any bit of the data-out sequence is being shifted out.

For the instruction of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down instruction, $\overline{CS}$ must be driven high exactly at a byte boundary, otherwise the instruction is rejected, and is not executed. That is $\overline{CS}$ must driven high when the number of clock pulses after $\overline{CS}$ being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

Table 8-1. Instruction Set

Instruction Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	N-Bytes
Write Enable	06h						
Write Disable	04h						
Read Status Register-1	05h	(S7 - S0)					continuous
Read Status Register-2	35h	(S15 - S8)					continuous
Read Status Register-3	15h	(S23 - S16)					continuous
Write Enable for Volatile Status Register	50h						
Write Status Register-1	01h	(S7 - S0)					

Table 8-1. Instruction Set *(continued)*

Instruction Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	N-Bytes
Write Status Register-2	31h	(S15 - S8)					
Write Status Register-3	11h	(S23 - S16)					
Read Data	03h	A23 - A16	A15 - A8	A7 - A0	(D7 - D0)	Next byte	continuous
Fast Read	0Bh	A23 - A16	A15 - A8	A7 - A0	dummy	(D7 - D0)	continuous
Dual Output Fast Read	3Bh	A23 - A16	A15 - A8	A7 - A0	dummy	(D7 - D0)(1)	continuous
Dual I/O Fast Read	BBh	A23 - A8(2)	A7 - A0 M7 - M0(2)	(D7 - D0)(1)	Next byte	Next byte	continuous
Quad Output Fast Read	6Bh	A23 - A16	A15 - A8	A7 - A0	dummy	(D7 - D0)(3)	continuous
Quad I/O Fast Read	EBh	A23 - A0 M7 - M0(4)	dummy(5)	(D7 - D0)(3)	Next byte	Next byte	continuous
Quad I/O Word Fast Read(7)	E7h	A23 - A0 M7 - M0 (4)	dummy(6)	(D7 - D0)(3)	Next byte	Next byte	continuous
Page Program	02h	A23 - A16	A15 - A8	A7 - A0	(D7 - D0)	Next byte	continuous
Quad Page Program	32h	A23 - A16	A15 - A8	A7 - A0	(D7 - D0)(3)	Next byte	continuous
Fast Page Program	F2h	A23 - A16	A15 - A8	A7 - A0	(D7 - D0)	Next byte	continuous
Sector Erase	20h	A23 - A16	A15 - A8	A7 - A0			
Block Erase(32K)	52h	A23 - A16	A15 - A8	A7 - A0			
Block Erase (64K)	D8h	A23 - A16	A15 - A8	A7 - A0			
Chip Erase	C7/60h						
Enable Reset	66h						
Reset	99h						
Set Burst with Wrap	77h	dummy(6) W7 - W0					
Program/Erase Suspend	75h						
Program/Erase Resume	7Ah						
Deep Power-Down	B9h						

Table 8-1. Instruction Set *(continued)*

Instruction Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	N-Bytes
Release From Deep Power-Down, And Read Device ID	ABh	dummy	dummy	dummy	(ID7 - ID0)		continuous
Release From Deep Power-Down	ABh						
Manufacturer/ Device ID	90h	dummy	dummy	00H	(MID7 - MID0)	(ID7 - ID0)	continuous
Manufacturer/ Device ID by Dual I/O	92h	A23 - A8	A7 - A0, dummy	(MID7 - MID0), (DID7 -DID0)			continuous
Manufacturer/ Device ID by Quad I/O	94h	A23 - A0, dummy	dummy[10] (MID7 - MID0) (DID7 - DID0)				continuous
JEDEC ID	9Fh	MID7 - MID0	ID15 - ID8	ID7-ID0			continuous
Read Serial Flash Discoverable Parameter	5Ah	A23 - A16	A15 - A8	A7-A0	Dummy	D7 - D0	continuous
Erase Security Registers[8]	44h	A23 - A16	A15 - A8	A7-A0			
Program Security Registers[8]	42h	A23 - A16	A15 - A8	A7-A0	(D7 - D0)	(D7 - D0)	continuous
Read Security Registers[8]	48h	A23 - A16	A15 - A8	A7-A0	dummy	(D7 - D0)	continuous

Notes:

1. Dual Output data

   IO_0 = (D6, D4, D2, D0)

   IO_1 = (D7, D5, D3, D1)
2. Dual Input Address

   IO_0 = A22, A20, A18, A16, A14, A12, A10, A8, A6, A4, A2, A0, M6, M4, M2, M0

   IO_1 = A23, A21, A19, A17, A15, A13, A11, A9, A7, A5, A3, A1, M7, M5, M3,M1
3. Quad Output Data

   IO_0 = (D4, D0,…..)

   IO_1 = (D5, D1,…..)

   IO_2 = (D6, D2,…..)

   IO_3 = (D7, D3,…..)
4. Quad Input Address

IO_0 = A20, A16, A12, A8, A4, A0, M4, M0

IO_1 = A21, A17, A13, A9, A5, A1, M5, M1

IO_2 = A22, A18, A14, A10, A6, A2, M6, M2

IO_3 = A23, A19, A15, A11, A7, A3, M7, M3

5. Fast Read Quad I/O Data

   IO_0 = (x, x, x, x, D4, D0,…)

   IO_1 = (x, x, x, x, D5, D1,…)

   IO_2 = (x, x, x, x, D6, D2,…)

   IO_3 = (x, x, x, x, D7, D3,…)

6. Fast Word Read Quad I/O Data

   IO_0 = (x, x, D4, D0,…)

   IO_1 = (x, x , D5, D1,…)

   IO_2 = (x, x, D6, D2,…)

   IO_3 = (x, x, D7, D3,…)

7. Fast Word Read Quad I/O Data:the lowest address bit must be 0.
8. Security Registers Address:

   Security Register 1: A23 - A16 = 00h, A15 - A8 = 00010000b, A7 - A0 = Byte Address;

   Security Register 2: A23 - A16 = 00h, A15 - A8 = 00100000b, A7 - A0 = Byte Address;

   Security Register 3: A23 - A16 = 00h, A15 - A8 = 00110000b, A7 - A0 = Byte Address;

9. Dummy bits and Wraps Bits

   IO_0 = (x, x, x, x, x, x, w4, x)

   IO_1 = (x, x, x, x, x, x, w5, x)

   IO_2 = (x, x, x, x, x, x, w6, x)

   IO_3 = (x, x, x, x, x, x, x, x)

10. Address, continuous Read Mode bits, Dummy bits, Manufacture ID and Device ID

    IO_0 = (A20, A16, A12, A8, A4, A0, M4, M0, x, x, x, x, MID4, MID0, DID4, DID0)

    IO_1 = (A21, A17, A13, A9, A5, A1, M5, M1, x, x, x, x, MID5, MID1, DID5, DID1)

    IO_2 = (A22, A18, A14, A10, A6, A2, M6, M2, x, x, x, x, MID6, MID2, DID6, DID2)

    IO_3 = (A23, A19, A15, A11, A7, A3, M7, M3, x, x, x, x, MID7, MID3, DID7, DID3)

8.1 Configuration and Status Instructions

8.1.1 Write Enable (06h)

The Write Enable instruction is for setting the Write Enable Latch (WEL) bit. The WEL bit must be set prior to every *Page Program*, *Sector Erase*, *Block Erase*, *Chip Erase*, *Write Status Register*, and *Erase/Program Security Registers* instruction.

The Write Enable instruction sequence: $\overline{CS}$ goes low sending the Write Enable instruction $\overline{CS}$ goes high.

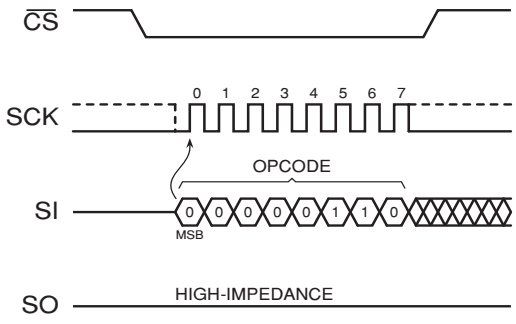


Figure 8-1. Write Enable Sequence Diagram

8.1.2 Write Disable (04h)

The Write Disable instruction is for resetting the Write Enable Latch bit. The Write Disable instruction sequence: $\overline{CS}$ goes low -> sending the Write Disable instruction -> $\overline{CS}$ goes high. The WEL bit is reset by following condition: Power-up and upon completion of the *Write Status Register*, *Page Program*, *Sector Erase*, *Block Erase*, *Chip Erase*, *Erase/Program Security Registers,* and *Reset* instructions.

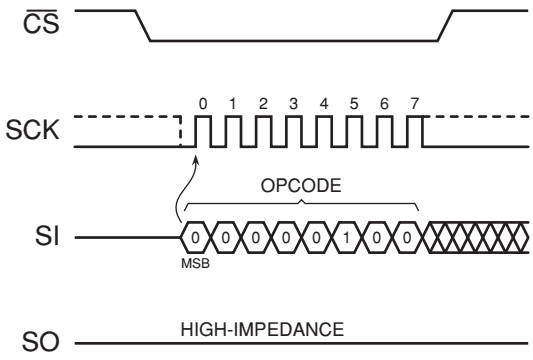


Figure 8-2. Write Disable Sequence Diagram

8.1.3 Read Status Register (05h or 35h or 15h)

The Read Status Register (RDSR) instruction is for reading the Status Register. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write in Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously. For instruction code 05h, the SO outputs Status Register bits S7 - S0. For instruction code 35h, the SO outputs Status Register bits S15 - S8. For instruction code 15h, the SO outputs Status Register bits S23 - 16.

Figure 8-3 shows a Read Status Register operation for Status Register 1 (05h). The Read Status Register 2 and 3 operations would be the same, but with a different opcode in the first eight clocks.

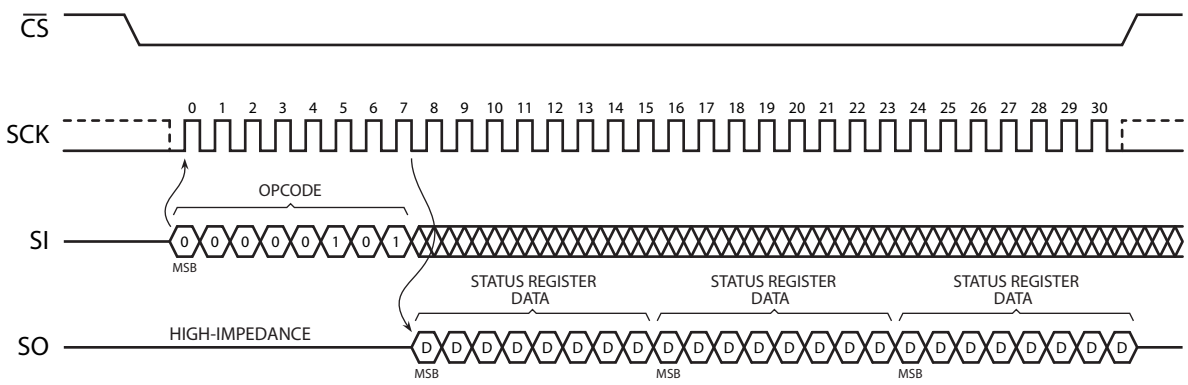


Figure 8-3. Read Status Register Sequence Diagram

8.1.4 Write Status Register (01h or 31h or 11h)

The Write Status Register instruction allows new values to be written to the Status Register. Before it can be accepted, a Write Enable instruction must previously have been executed. After the Write Enable instruction has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register instruction has no effect on S23, S20, S19, S18, S17, S16, S15, S1 and S0 of the Status Register. $\overline{CS}$ must be driven high after the eighth bit of the data byte has been latched in. If not, the Write Status Register instruction is not executed. As soon as $\overline{CS}$ is driven high, the self-timed Write Status Register cycle (whose duration is t_W) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write in Progress (WIP) bit. This bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the WEL bit is reset.

The Write Status Register instruction allows the user to change the values of the Block Protect (BP4, BP3, BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only. The Write Status Register instruction also allows the user to set or reset the Status Register Protect (SRP1 and SRP0) bits in accordance with the Write Protect ($\overline{WP}$) signal. The Status Register Protect (SRP1 and SRP0) bits and Write Protect ($\overline{WP}$) signal allow the device to be put in the Hardware Protected Mode. The Write Status Register instruction is not executed once the Hardware Protected Mode is entered.

Figure 8-3 shows a Write Status Register operation for Status Register 1 (01h). The Write Status Register 2 and 3 operations would be the same, but with a different opcode in the first eight clocks.

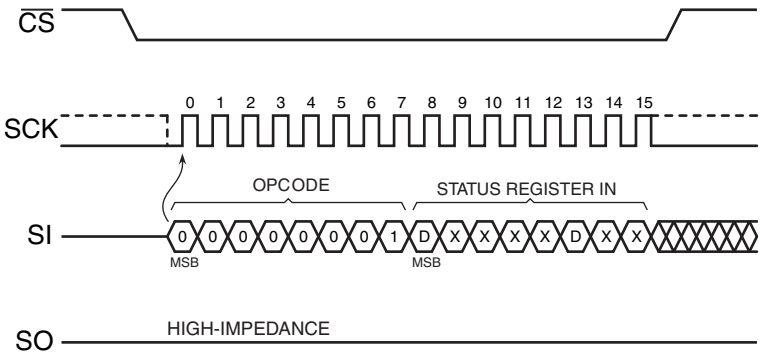


Figure 8-4. Write Status Register Sequence Diagram

8.1.5 Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Write Enable for Volatile Status Register instruction does not set the Write Enable Latch bit, it is only valid for the Write Status Registers instruction to change the volatile Status Register bit values.

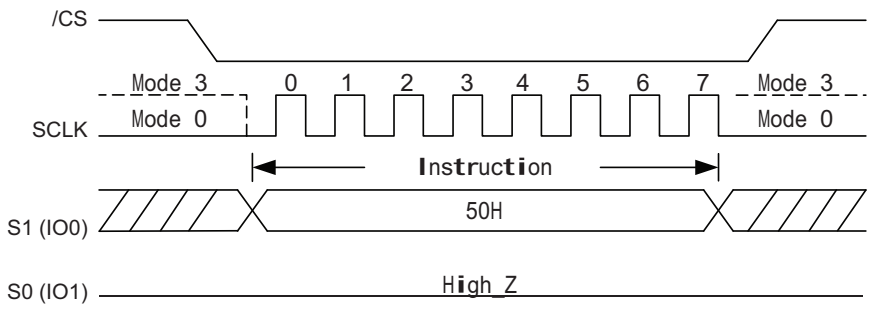


Figure 8-5. Write Enable for Volatile Status Register

8.2 Read Instructions

8.2.1 Read Data (03h)

The Read Data instruction is followed by a 3-byte address (A23 - A0), each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency f_{C2}, during the falling edge of SCLK. The address automatically increments to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single command as long as the clock continues. The command is completed by driving $\overline{CS}$ high. The whole memory can be read with a single Read Data Bytes (READ) instruction. Any *Read Data* instruction attempting to execute while an *Erase*, *Program* or *Write* cycle is in progress, is rejected without having any effects on the cycle that is in progress.

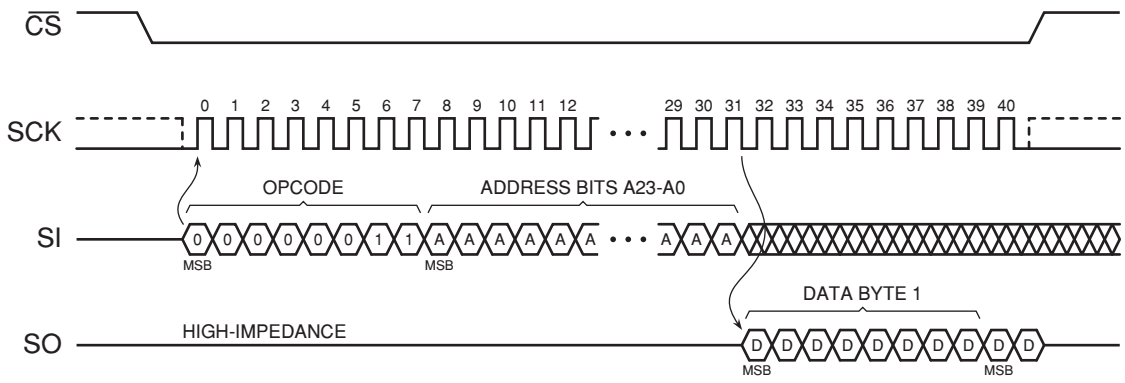


Figure 8-6. Read Data Bytes Sequence Diagram

8.2.2 Fast Read (0Bh)

The Read Data at Higher Speed (Fast Read) instruction is for quickly reading data out. It is followed by a 3-byte address (A23 - A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency of f_{C4} during the falling edge of SCLK. The first byte addressed can be at any location. The address automatically increments to the next higher address after each byte of data is shifted out.

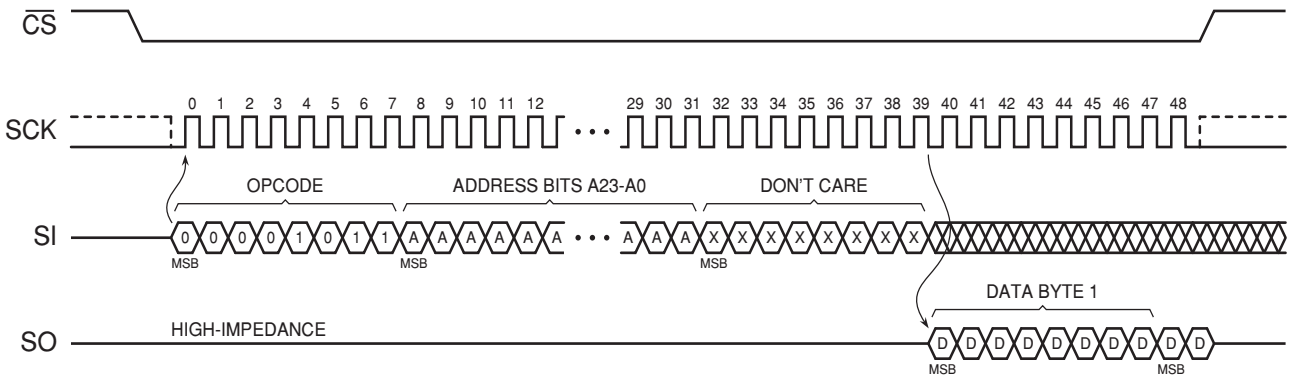


Figure 8-7. Fast Read Sequence Diagram

8.2.3 Dual Output Fast Read (3Bh)

The Dual Output Fast Read instruction is followed by 3-byte address (A23 - A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The first byte addressed can be at any location. The address automatically increments to the next higher address after each byte of data is shifted out.

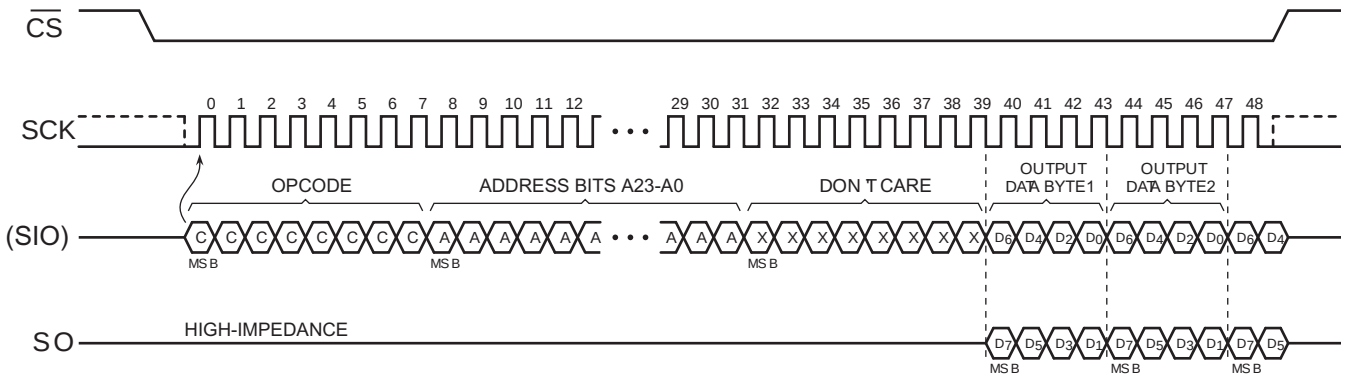


Figure 8-8. Dual Output Fast Read Sequence Diagram

8.2.4 Quad Output Fast Read (6Bh)

The Quad Output Fast Read instruction is followed by 3-byte address (A23 - A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO_3, IO_2, IO_1 and IO_0. The first byte addressed can be at any location. The address automatically increments to the next higher address after each byte of data is shifted out.

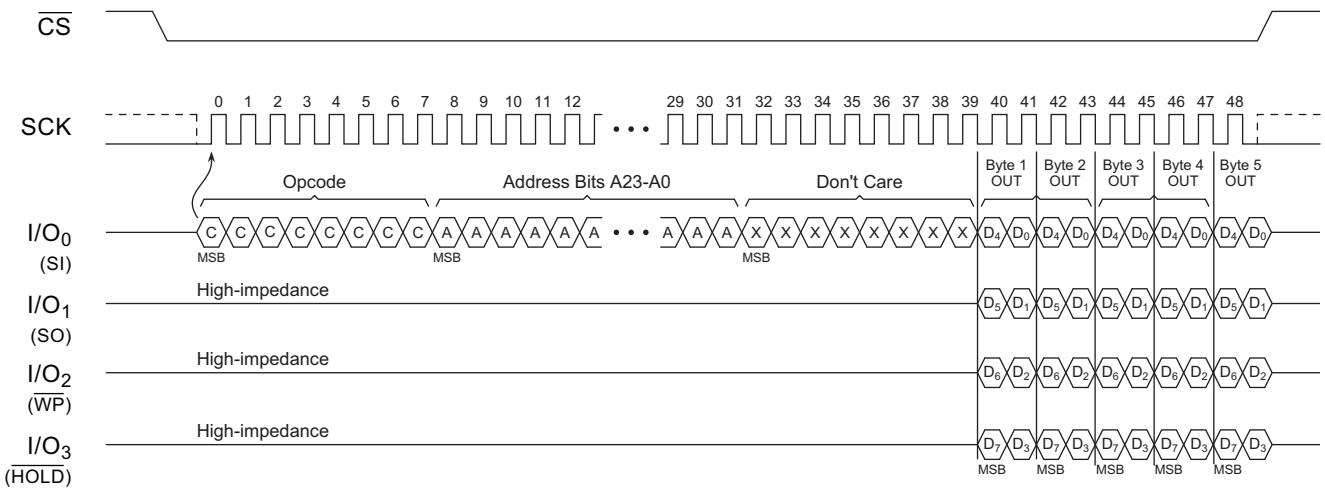


Figure 8-9. Quad Output Fast Read Sequence Diagram

8.2.5 Dual I/O Fast Read (BBh)

The Dual I/O Fast Read instruction is similar to the Dual Output Fast Read instruction but with the capability to input the 3-byte address (A23 - 0) and a Continuous Read Mode byte 2-bits per clock by SI and SO, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out two bits per clock cycle on the SI and SO pins. The first byte addressed can be at any location. The address automatically increments to the next higher address after each byte of data is shifted out.

Dual I/O Fast Read with Continuous Read Mode

The Dual I/O Fast Read instruction can further reduce instruction overhead through setting the Continuous Read Mode bits (M7 - 4) after the inputs 3-byte address A23 - A0).

If the Continuous Read Mode bits (M5:M4) do not equal (1,0), the next instruction requires the first BBh instruction code, thus returning to normal operation. A Continuous Read Mode Reset instruction can be used to reset (M5:M4) before issuing normal instruction. The instruction sequence is shown in the following Figure 8-10.

If the Continuous Read Mode bits (M5:M4) = (1, 0), then the next Dual I/O fast Read instruction (after $\overline{CS}$ is raised and then lowered) does not require the BBh instruction code. The instruction sequence is shown in the following Figure 8-11.

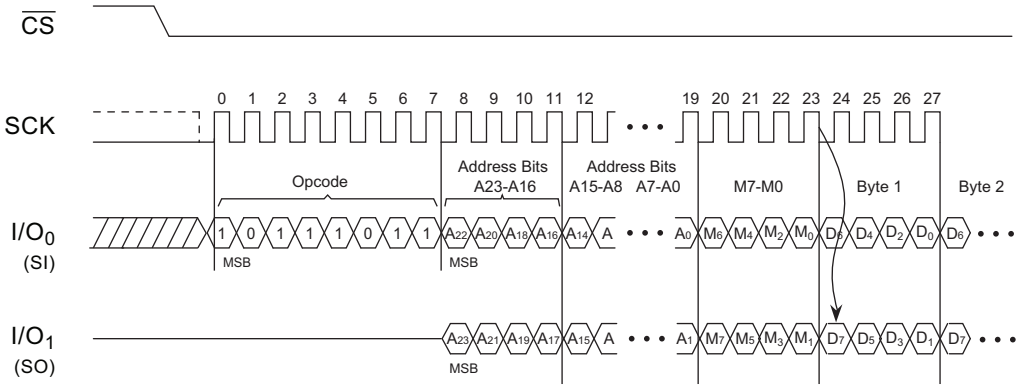


Figure 8-10. Dual I/O Fast Read Sequence Diagram (Initial command or previous (M5:4) ≠ (1,0))

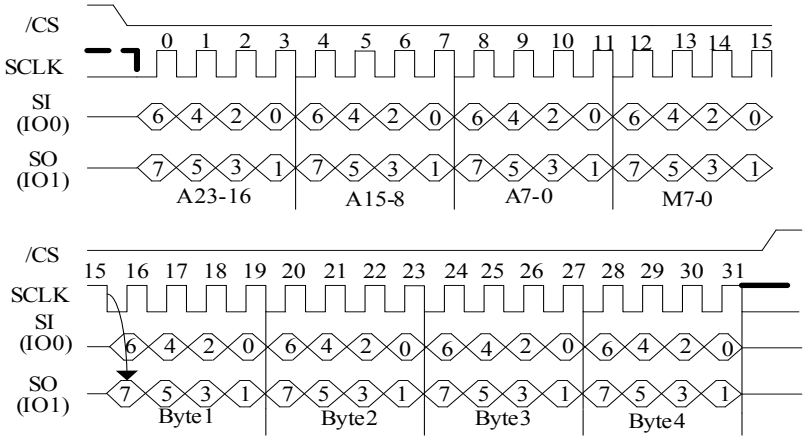


Figure 8-11. Dual I/O Fast Read Sequence Diagram (Previous command set (M5:4) = (1,0))

8.2.6 Quad I/O Fast Read (EBh)

The Quad I/O Fast Read instruction is similar to the Dual I/O Fast Read instruction but with the capability to input the 3-byte address (A23-0) and a Continuous Read Mode byte and 4-dummy clocks, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO_0, IO_1, IO_2, IO_3. The first byte addressed can be at any location. The address automatically increments to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register must be set to enable for the Quad I/O Fast read instruction.

Quad I/O Fast Read with Continuous Read Mode

The Quad I/O Fast Read instruction can further reduce instruction overhead through setting the Continuous Read Mode bits (M7-0) after the input Address bits (A23-0).

If the Continuous Read Mode bits M5-4 do not equal to (1,0), the next instruction requires the first EBh instruction code, thus returning to normal operation. A Continuous Read Mode Reset command can also be used to reset (M5-4) before issuing normal command. The instruction sequence is shown in the followed Figure 8-12.

If the Continuous Read Mode bits (M5-4) = (1,0), then the next Fast Read Quad I/O instruction (after $\overline{CS}$ is raised and then lowered) does not require the EBh instruction code. The instruction sequence is shown in the followed Figure 8-13.

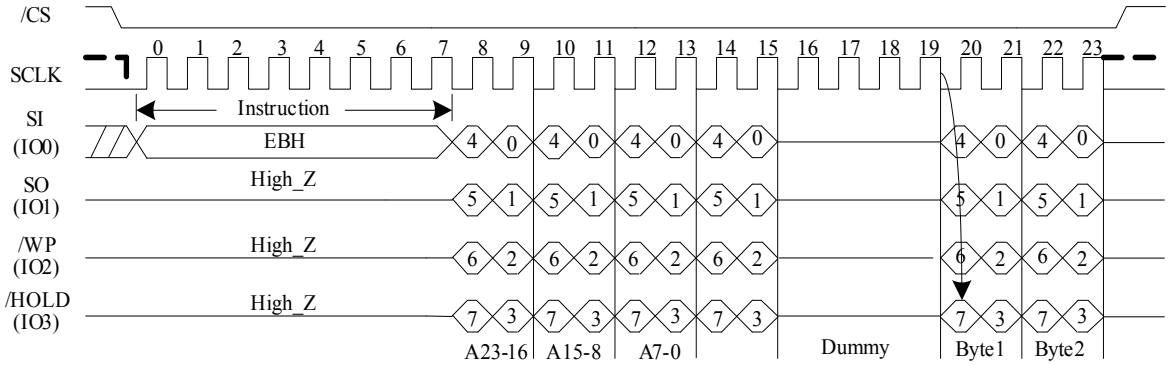


Figure 8-12. Quad I/O Fast Read Sequence Diagram (Initial command or previous (M5-4) ≠ (1,0))

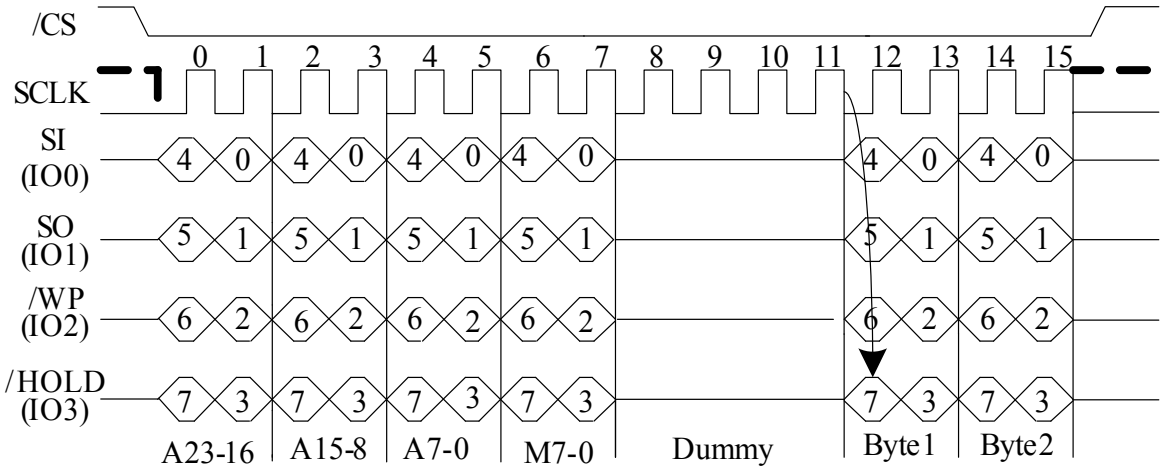


Figure 8-13. Quad I/O Fast Read Sequence Diagram (Previous command set (M5-4) = (1,0))

Quad I/O Fast Read with 8/16/32/64-Byte Wrap Around

The Quad I/O Fast Read instruction can also be used to access a specific portion within a page by issuing a Set Burst with Wrap (77h) instruction prior to EBh. The Set Burst with Wrap (77h) instruction can either enable or disable the Wrap Around feature for the following EBh instructions.

When Wrap Around is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output wraps around to the beginning boundary automatically until $\overline{CS}$ is pulled high to terminate the instruction.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read instructions.

The Set Burst with Wrap instruction allows three Wrap Bits, W6-4 to be set. The W4 bit is used to enable or disable the Wrap Around operation while W6-5 are used to specify the length of the wrap around section within a page.

8.2.7 Quad I/O Word Fast Read (E7h)

The Quad I/O Word Fast Read instruction is similar to the Quad Fast Read instruction except that the lowest address bit (A0) must equal to 0 and 2 dummy clocks. The address automatically increments to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Word Fast Read instruction.

Quad I/O Word Fast Read with Continuous Read Mode

The Quad I/O Word Fast Read instruction can further reduce instruction overhead through setting the Continuous Read Mode bits (M7-0) after the input 3-byte Address bits (A23-0).

If the Continuous Read Mode bits M5-4 do not equal to (1,0), the next instruction requires the first E7h instruction code, thus returning to normal operation. A Continuous Read Mode Reset command can also be used to reset (M5-4) before issuing normal command. The instruction sequence is shown in the followed Figure 8-14.

If the Continuous Read Mode bits (M5-4) = (1, 0), then the next Quad I/O Fast Read instruction (after $\overline{CS}$ is raised and then lowered) does not require the E7h instruction code, the instruction sequence is shown in the followed Figure 8-15.

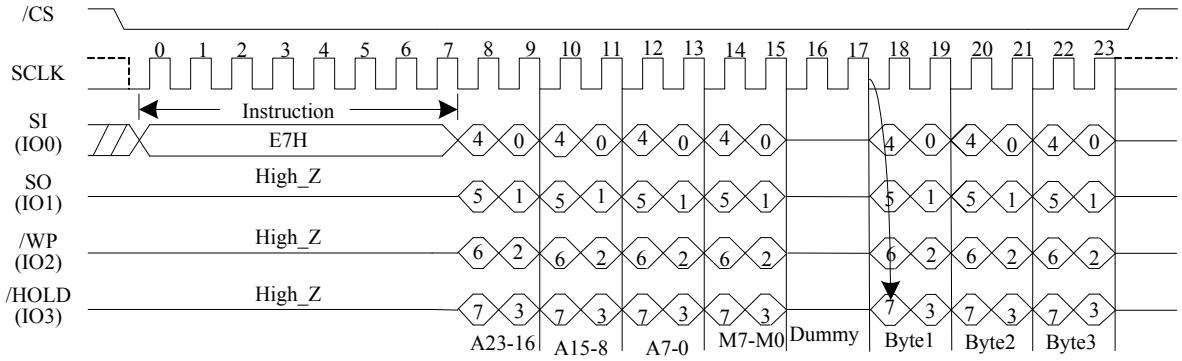


Figure 8-14. Quad I/O Word Fast Read Sequence Diagram (Initial command or previous (M5-4) ≠ (1,0))

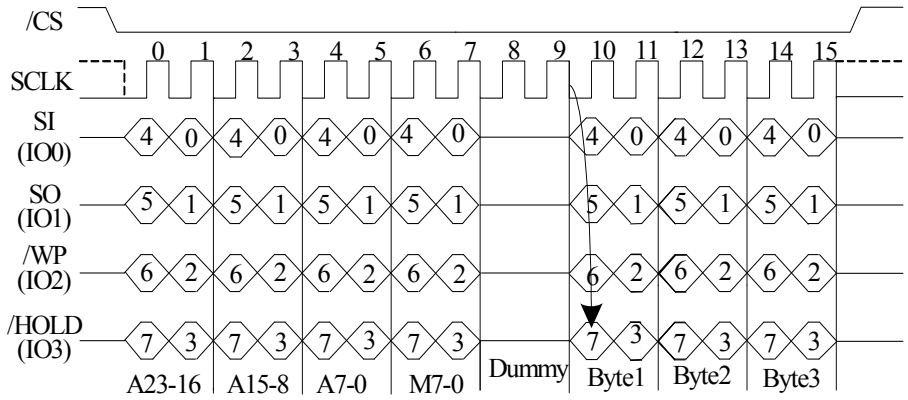


Figure 8-15. Quad I/O Word Fast Read Sequence Diagram (Previous command set (M5-4) = (1,0))

Quad I/O Word Fast Read with 8/16/32/64-Byte Wrap Around in Standard SPI Mode

The Quad I/O Fast Read instruction can also be used to access a specific portion within a page by issuing a Set Burst with Wrap (77h) instruction prior to E7h. The Set Burst with Wrap (77h) instruction can either enable or disable the Wrap Around feature for the following E7h instructions. When Wrap Around is enabled, the data being

accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until $\overline{CS}$ is pulled high to terminate the instruction.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read instructions. The Set Burst with Wrap instruction allows three Wrap Bits, W6-4 to be set. The W4 bit is used to enable or disable the Wrap Around operation while W6-5 are used to specify the length of the wrap around section within a page.

8.2.8 Set Burst with Wrap (77h)

The Set Burst with Wrap instruction is used in conjunction with Quad I/O Fast Read and Quad I/O Word Fast Read instruction to access a fixed length of 8/16/32/64-byte section within a 256-byte page in standard SPI mode. The Set Burst with Wrap instruction sequence is as follows: $\overline{CS}$ goes low -> Send Set Burst with Wrap instruction -> Send 24 Dummy bits -> Send 8 Wrap bits -> $\overline{CS}$ goes high.

If W6-4 is set by a Set Burst with Wrap instruction, all the following Fast Read Quad I/O and Word Read Quad I/O instructions will use the W6-4 setting to access the 8/16/32/64-byte section within any page. To exit the Wrap Around function and return to normal read operation, another Set Burst with Wrap instruction should be issued to set W4 = 1. The default value of W4 upon power on is 1.

Table 8-2. Set Burst with Wrap

W6, W5	W4 = 0		W4 = 1 (Default)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0 0	Yes	8-byte	No	N/A
0 1	Yes	16-byte	No	N/A
1 0	Yes	32-byte	No	N/A
1 1	Yes	64-byte	No	N/A

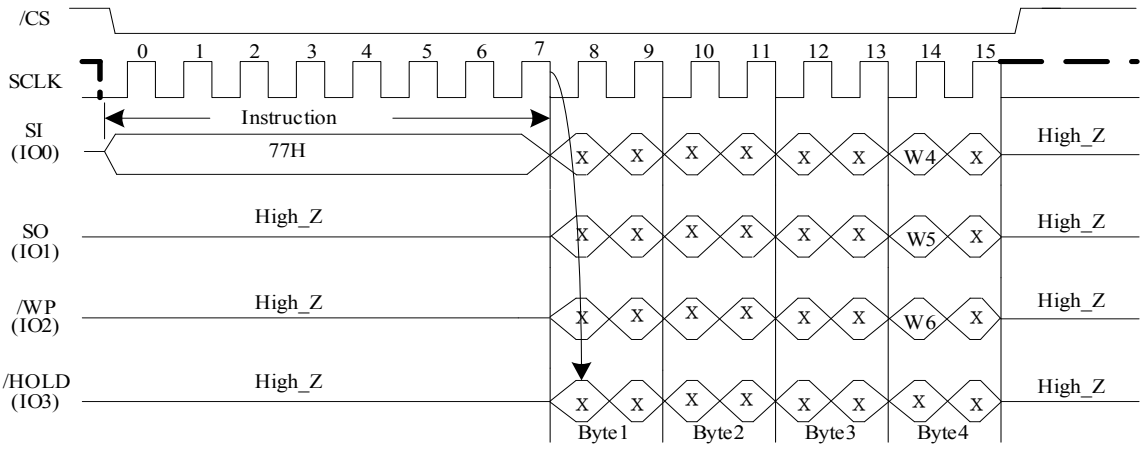


Figure 8-16. Set Burst with Wrap Sequence Diagram

8.3 ID and Security Instructions

8.3.1 Read Manufacture ID/ Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-Down/Device ID instruction that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The instruction is initiated by driving the $\overline{CS}$ pin low and shifting the instruction code 90h followed by a 24-bit address (A23-A0) of 000000h. If the 24-bit address is initially set to 000001h, the Device ID will be read first.

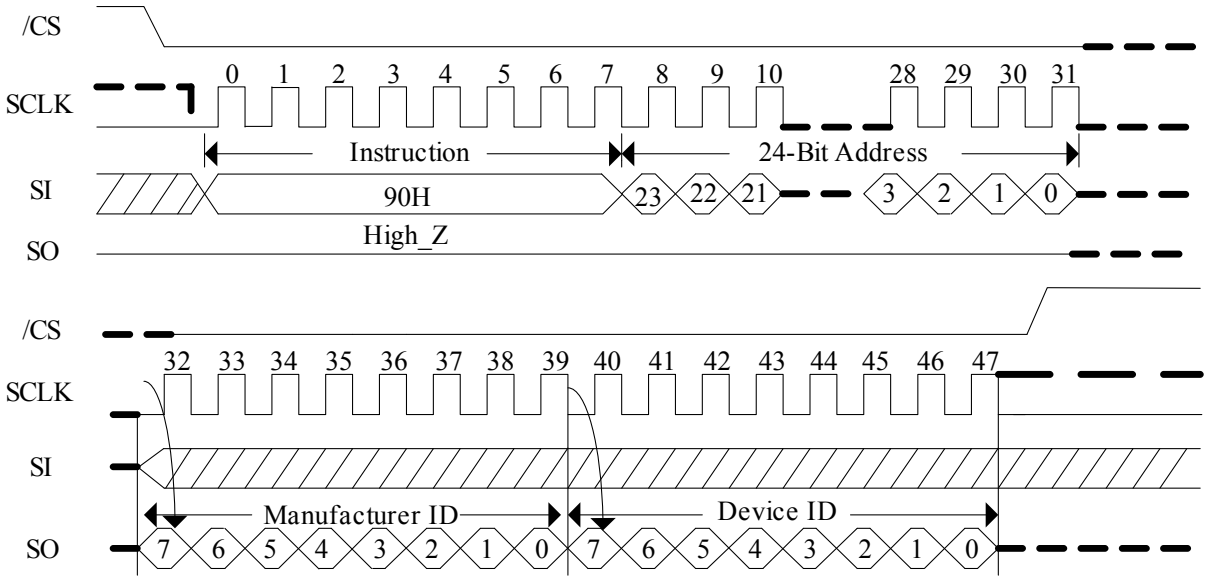


Figure 8-17. Read Manufacture ID/ Device ID Sequence Diagram

8.3.2 Dual I/O Read Manufacture ID/ Device ID (92h)

The Dual I/O Read Manufacturer/Device ID instruction is an alternative to the Release from Power-Down/Device ID instruction that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by Dual I/O.

The instruction is initiated by driving the $\overline{CS}$ pin low and shifting the instruction code 92h followed by a 24-bit address (A23 - A0) of 000000h. If the 24-bit address is initially set to 000001h, the Device ID is read first.

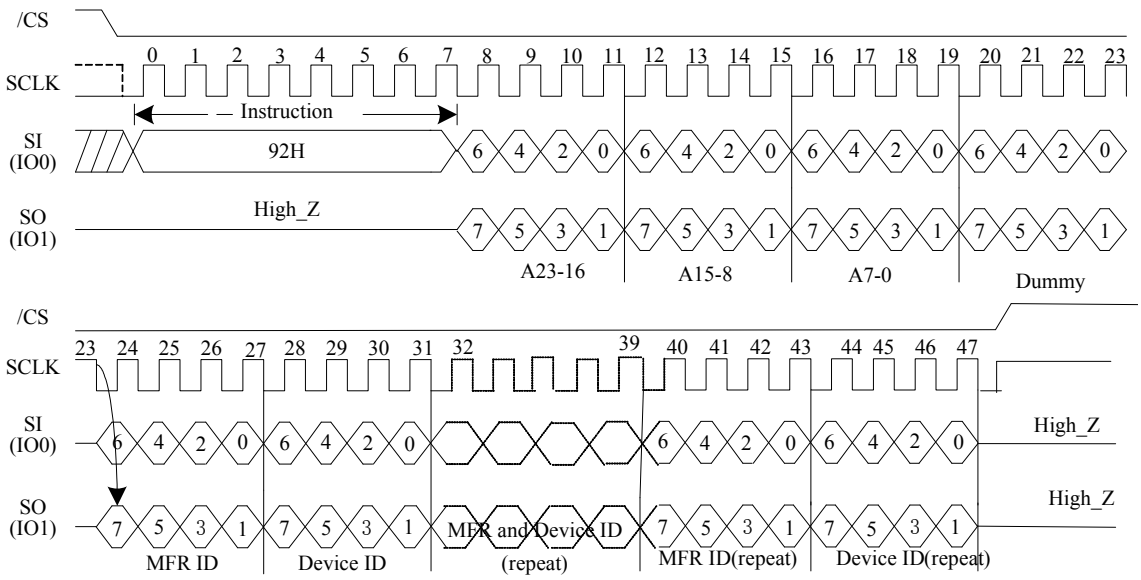


Figure 8-18. Dual I/O Read Manufacture ID/ Device ID Sequence Diagram

8.3.3 Quad I/O Read Manufacture ID/ Device ID (94h)

The Quad I/O Read Manufacturer/Device ID instruction is an alternative to the Release from Power-Down/Device ID instruction that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by quad I/O.

The instruction is initiated by driving the $\overline{CS}$ pin low and shifting the instruction code 94h followed by a 24-bit address (A23 - A0) of 000000h and four dummy clocks. If the 24-bit address is initially set to 000001h, the Device ID is read out first.

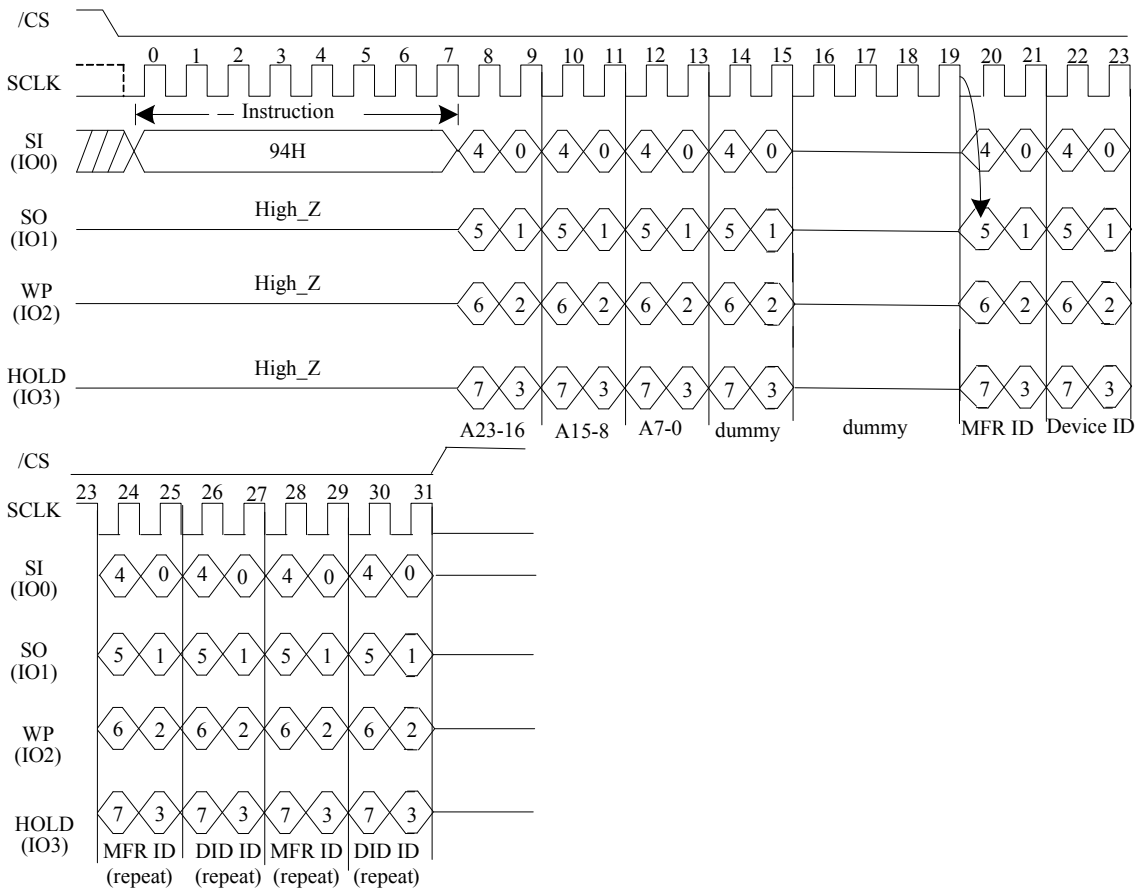


Figure 8-19. Quad I/O Read Manufacture ID / Device ID Sequence Diagram

8.3.4 Read JEDEC ID (9Fh)

The JEDEC ID instruction allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. JEDEC ID instruction while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The JEDEC ID instruction should not be issued while the device is in Deep Power-Down Mode.

The device is first selected by driving $\overline{CS}$ to low. Then, the 8-bit instruction code for the instruction is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output, each bit being shifted out during the falling edge of Serial Clock. The JEDEC ID instruction is terminated by driving $\overline{CS}$ to high at any time during data output. When $\overline{CS}$ is driven high, the device is put in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute instructions.

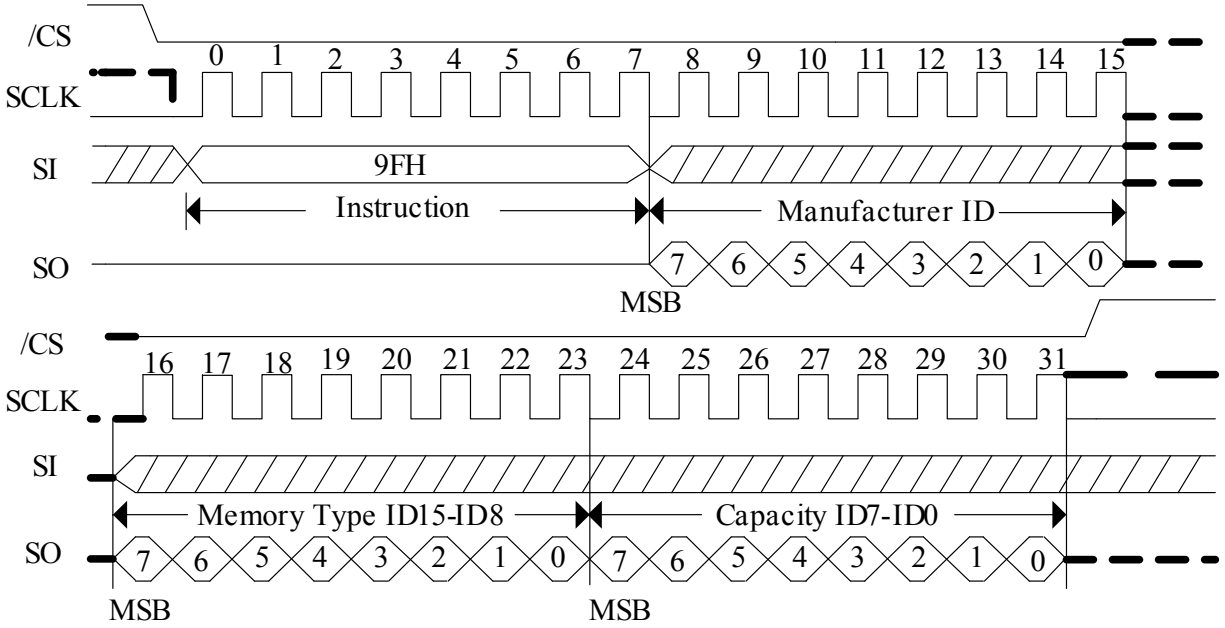


Figure 8-20. JEDEC ID Sequence Diagram

8.3.5 Read Unique ID Number (4Bh)

The Read Unique ID Number instruction accesses a factory-set read-only 64-bit number that is unique to each AT25SF128A device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the $\overline{CS}$ pin low and shifting the instruction code 4Bh followed by a four bytes of dummy clocks. After which, the 64-bit ID is shifted out on the falling edge of SCLK as shown in Figure 8-21.

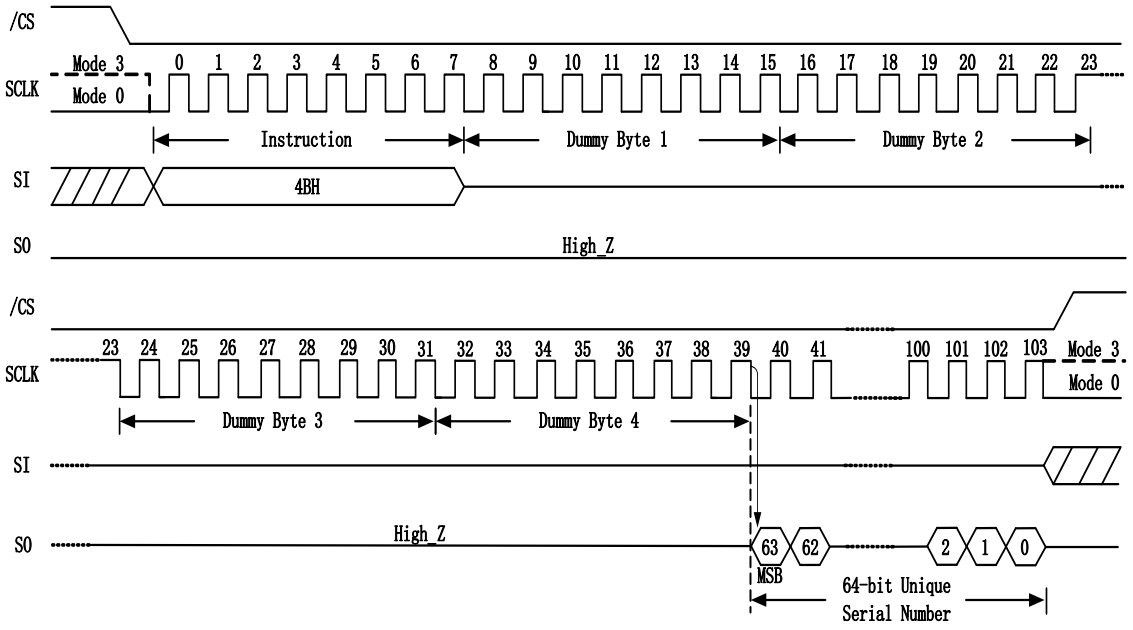


Figure 8-21. Read Unique ID Sequence Diagram

8.3.6 Deep Power-Down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Deep Power-down instruction. The lower power consumption makes the Deep Power-down (DPD) instruction especially useful for battery powered applications (see ICC1 and ICC2). The instruction is initiated by driving the $\overline{CS}$ pin low and shifting the instruction code B9h as shown in Figure 8-22.

The $\overline{CS}$ pin must be driven high after the eighth bit has been latched. If this is not done the Deep Power down instruction is not executed. After $\overline{CS}$ is driven high, the power-down state is entered within the time duration of t_{DP}. While in the power-down state only the Release from Deep Power-down / Device ID instruction, which restores the device to normal operation, will be recognized. All other Instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction also makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of ICC1.

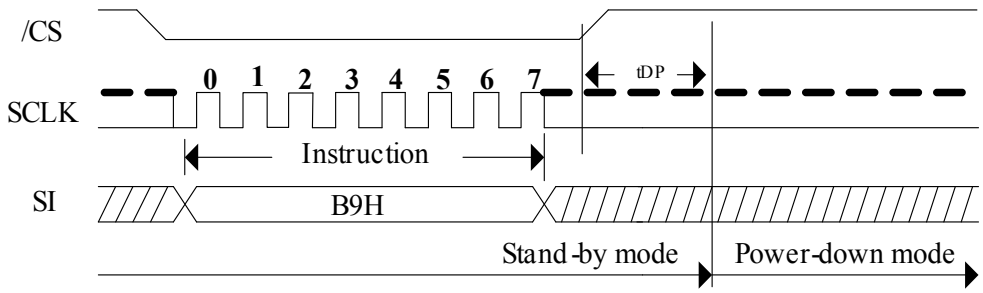


Figure 8-22. Deep Power-Down Sequence Diagram

8.3.7 Release from Deep Power-Down/Read Device ID (ABh)

The Release from Power-Down or Device ID instruction is a multi-purpose instruction. It can be used to release the device from the Power-Down state or obtain the devices electronic identification (ID) number.

To release the device from the Power-Down state, the instruction is issued by driving the $\overline{CS}$ pin low, shifting the instruction code ABh and driving $\overline{CS}$ high Release from Power-Down will take the time duration of t_{RES1} (See Section 9.8, AC Electrical Characteristics) before the device resumes normal operation and other instruction are accepted. The $\overline{CS}$ pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the Power-Down state, the instruction is initiated by driving the $\overline{CS}$ pin low and shifting the instruction code ABh followed by 3-dummy byte. The Device ID bits are then shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure 8-23. The Device ID value for the AT25SF128A is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving $\overline{CS}$ high.

When used to release the device from the Power-Down state and obtain the Device ID, the instruction is the same as previously described, and shown in Figure 8-23, except that after $\overline{CS}$ is driven high it must remain high for a time duration of t_{RES2} (See Section 9.8, AC Electrical Characteristics). After this time duration the device resumes normal operation and other instructions are accepted. If the Release from Power-Down/Device ID instruction is issued while an Erase, Program or Write cycle is in process (when WIP equal 1) the instruction is ignored and does not effect the current cycle.

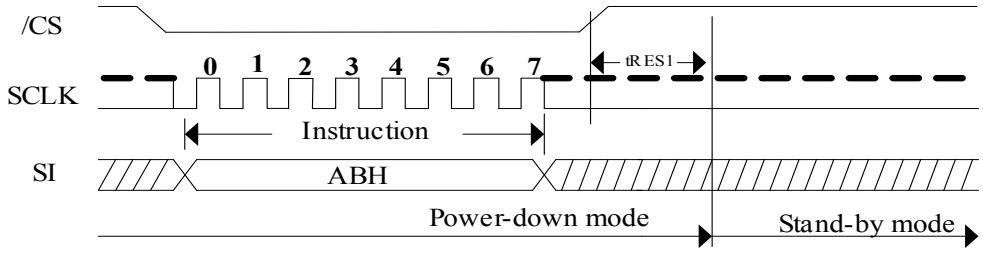


Figure 8-23. Release Power-Down Sequence Diagram

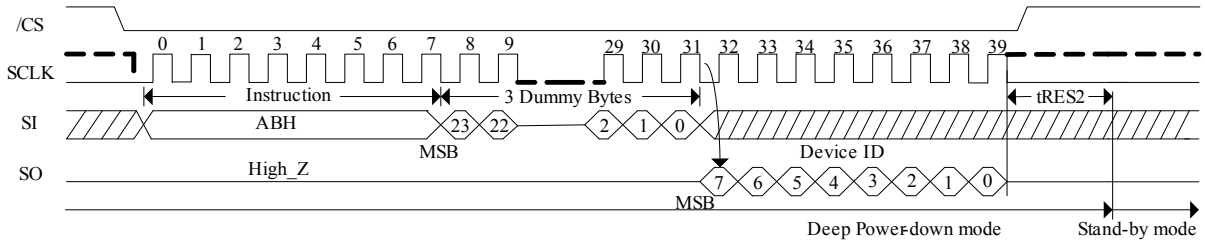


Figure 8-24. Release Power-Down/Read Device ID Sequence Diagram

8.3.8 Read Security Registers (48h)

The Read Security Registers instruction is similar to Fast Read instruction. The instruction is followed by a 3-byte address (A23 - A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency f_C, during the falling edge of SCLK. The first byte addressed can be at any location. The address automatically increments to the next higher address after each byte of data is shifted out. Once the A7 - A0 address reaches the last byte of the register (Byte FFh), it resets to 000h, the instruction is completed by driving $\overline{CS}$ high.

Table 8-3. Read Security Registers

Address	A23-A16	A15-A12	A11-A8	A7-A0
Security Registers 1	00h	0001	0000	Byte Address
Security Registers 2	00h	0010	0000	Byte Address
Security Registers 3	00h	0011	0000	Byte Address

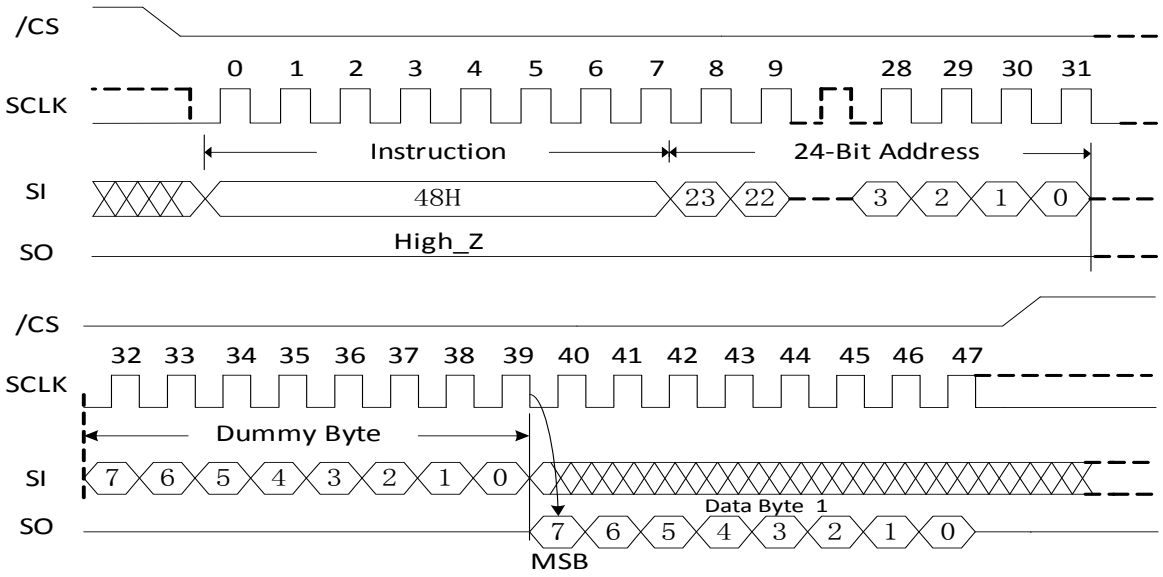


Figure 8-25. Read Security Registers Instruction Sequence Diagram

8.3.9 Erase Security Registers (44h)

The AT25SF128A provides three 256-byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Registers instruction is similar to Sector/Block Erase instruction. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit.

The Erase Security Registers instruction sequence: $\overline{CS}$ goes low -> sending Erase Security Registers instruction -> $\overline{CS}$ goes high. $\overline{CS}$ must be driven high after the eighth bit of the instruction code has been latched in otherwise the Erase Security Registers instruction is not executed. As soon as $\overline{CS}$ is driven high, the self-timed Erase Security Registers cycle (whose duration is t_{SE}) is initiated. While the Erase Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. The Security Registers Lock Bit (LB) in the Status Register can be used to OTP protect the security registers. Once the LB bit is set to 1, the Security Registers are permanently locked; the Erase Security Registers instruction is ignored.

Table 8-4. Erase Security Registers

Address	A23 - A16	A15 - A12	A11 - A8	A7 - A0
Security Registers 1	00h	0001	0000	Byte Address
Security Registers 2	00h	0010	0000	Byte Address
Security Registers 3	00h	0011	0000	Byte Address

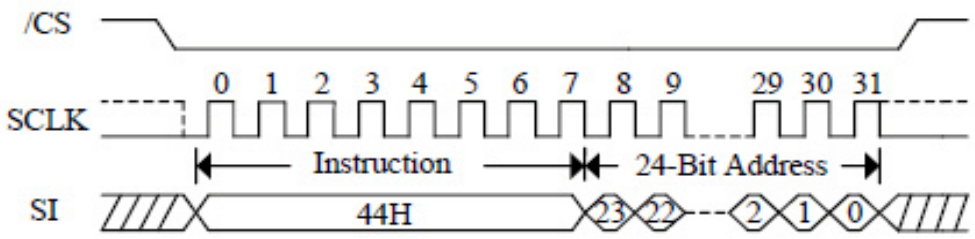


Figure 8-26. Erase Security Registers Instruction Sequence Diagram

8.3.10 Program Security Registers (42h)

The Program Security Registers instruction is similar to the Page Program instruction. It allows from 1 to 256 bytes Security Registers data to be programmed. A Write Enable instruction must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Program Security Registers instruction.

The Program Security Registers instruction is entered by driving $\overline{CS}$ low, followed by the instruction code (42h), a 3-byte address and at least one data byte on the SI pin. As soon as $\overline{CS}$ is driven high, the self-timed Program Security Registers cycle (whose duration is t_{PP}) is initiated. While the Program Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the WEL bit is reset.

If the Security Registers Lock Bit (LB3/LB2/LB1) bits are set to 1, the Security Registers are permanently locked. The Program Security Registers instruction is ignored.

Table 8-5. Program Security Registers

Address	A23 - A16	A15 - A12	A11 - A8	A7 - A0
Security Registers 1	00h	0001	0000	Byte Address
Security Registers 2	00h	0010	0000	Byte Address
Security Registers 3	00h	0011	0000	Byte Address

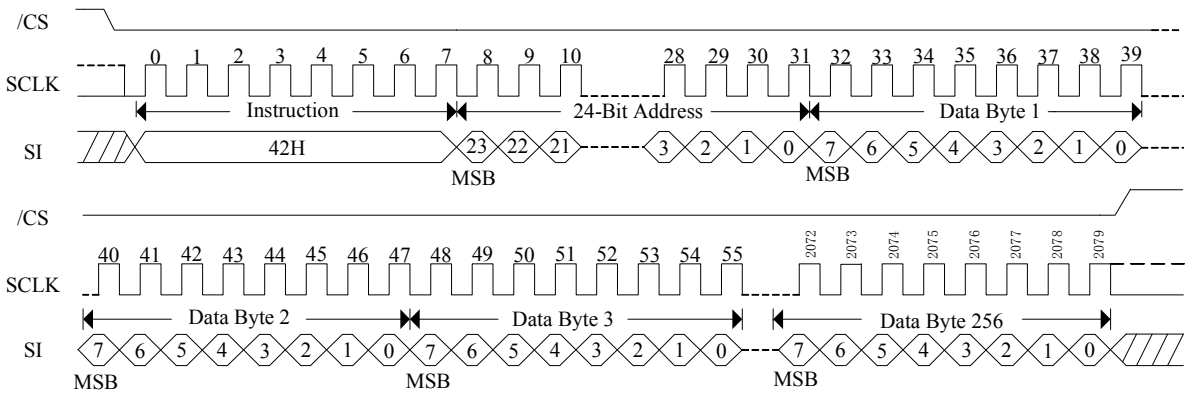


Figure 8-27. Program Security Registers Instruction Sequence Diagram

8.3.11 Enable Reset (66h) and Reset Device (99h)

Because of the small package and the limitation on the number of pins, the AT25SF128A provides a software Reset instruction instead of a dedicated RESET pin. Once the software Reset instruction is accepted, any on-going internal operations are terminated and the device returns to its default power-on state and loses all of the current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL) status, Program/Erase Suspend status, Continuous Read Mode bit setting (M7-M0) and Wrap Bit setting (W6-W4).

To avoid accidental reset, both Enable Reset (66h) and Reset (99h) instructions must be issued in sequence. Any other commands other than Reset (99h) after the Enable Reset (66h) command will disable the Reset Enable state. A new sequence of Enable Reset (66h) and Reset (99h) is needed to reset the device. Once the Reset command is accepted by the device, the device takes approximately 30 µs to reset. During this period, no commands are accepted.

The Enable Reset (66h) and Reset (99h) instruction sequence is shown in Figure 8-28.

Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset command sequence.

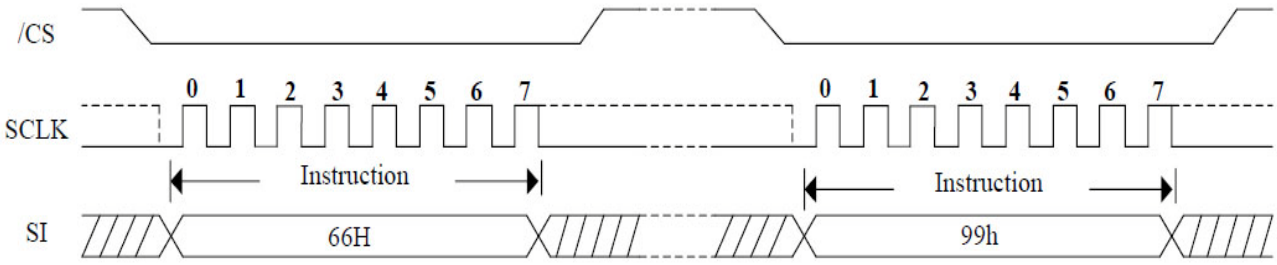


Figure 8-28. Enable Reset (66h) and Reset (99h) Command Sequence

8.4 Program and Erase Instructions

8.4.1 Page Program (02h)

The Page Program instruction is for programming the memory. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit before sending the Page Program instruction.

The Page Program instruction is entered by driving $\overline{CS}$ Low, followed by the instruction code, 3-byte address and at least one data byte on SI. If the 8 least significant address bits (A7 - A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7 - A0) are all zero). $\overline{CS}$ must be driven low for the entire duration of the sequence. The Page Program instruction sequence: $\overline{CS}$ goes low -> sending Page Program instruction -> 3-byte address on SI -> at least 1 byte of data on SI -> $\overline{CS}$ goes high.

If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. $\overline{CS}$ must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program instruction is not executed.

As soon as $\overline{CS}$ is driven high, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP)

bit. The Write in Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program instruction applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits is not executed.

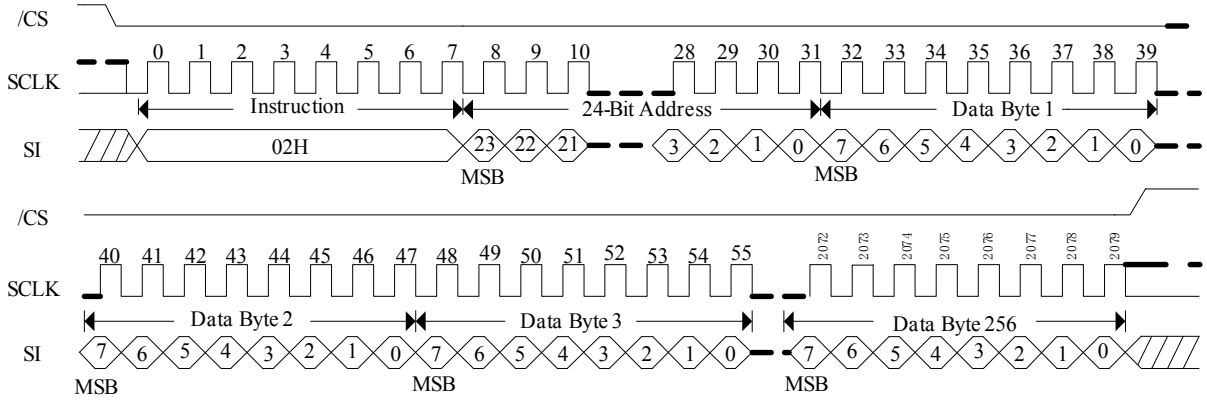


Figure 8-29. Page Program Sequence Diagram

8.4.2 Quad Page Program (32h)

The Quad Page Program instruction is for programming the memory using for pins: IO_0, IO_1, IO_2 and IO_3. To use Quad Page Program the Quad Enable (QE) bit in the Status register must be set (QE = 1). A Write Enable instruction must previously have been executed to set the Write Enable Latch bit before sending the Page Program instruction. The Quad Page Program instruction is entered by driving $\overline{CS}$ low, followed by the command code (32h), three address bytes and at least one data byte on IO pins.

The instruction sequence is shown in Figure 8-30. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. $\overline{CS}$ must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Quad Page Program instruction is not executed.

As soon as $\overline{CS}$ is driven high, the self-timed Quad Page Program cycle (whose duration is t_{PP}) is initiated. While the Quad Page Program cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Quad Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset.A Quad Page Program instruction applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits is not executed.

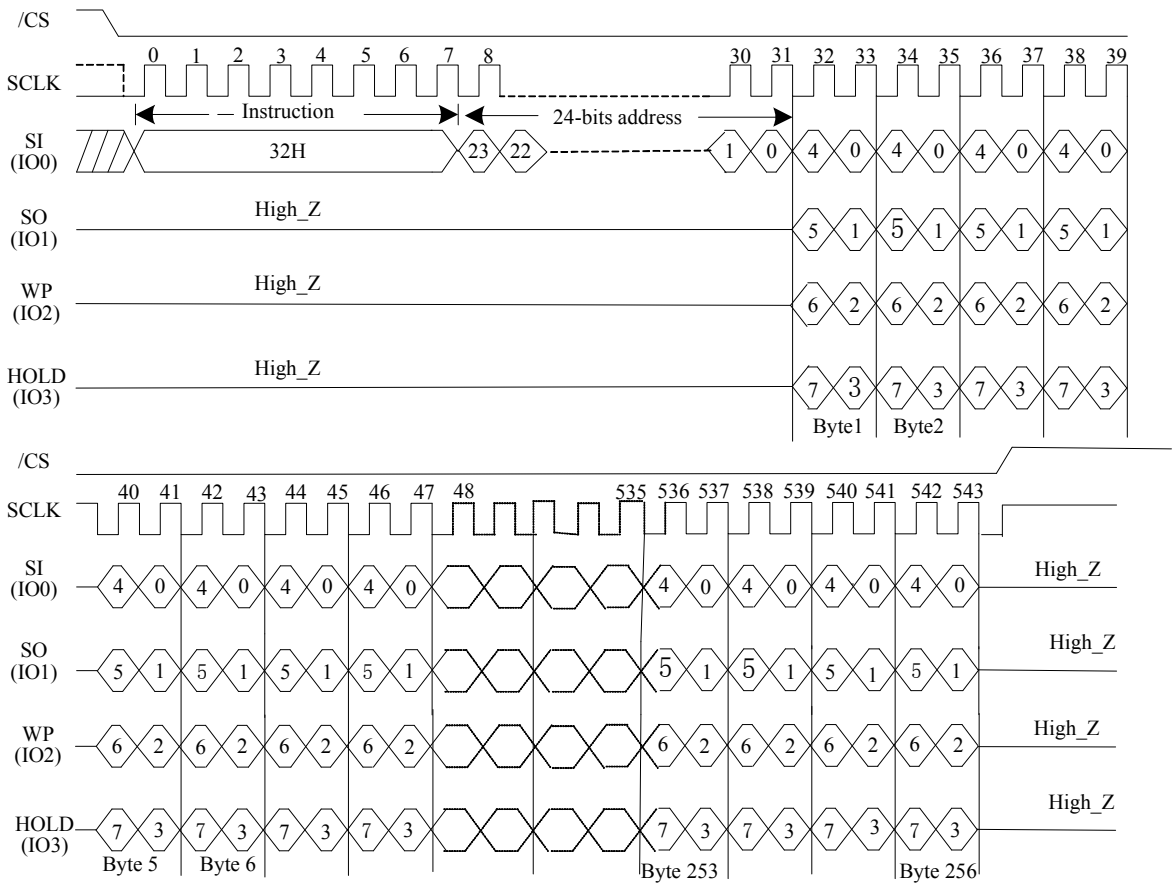


Figure 8-30. Quad Page Program Sequence Diagram

8.4.3 Fast Page Program (F2h)

The Fast Page Program instruction is used to program the memory. A Write Enable instruction must previously have been executed to set the WEL bit before sending the Page Program instruction.

The Fast Page Program instruction is entered by driving $\overline{CS}$ Low, followed by the instruction code, 3-byte address and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). $\overline{CS}$ must be driven low for the entire duration of the sequence.

The Fast Page Program instruction sequence: $\overline{CS}$ goes low -> sending Page Program instruction -> 3-byte address on SI -> at least 1 byte data on SI -> $\overline{CS}$ goes high.

The command sequence is shown in Figure 8-31. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. $\overline{CS}$ must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Fast Page Program instruction is not executed.

As soon as $\overline{CS}$ is driven high, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write-in-Progress (WIP)

bit. The WIP bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the WEL bit is reset.

A Fast Page Program instruction applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits is not executed.

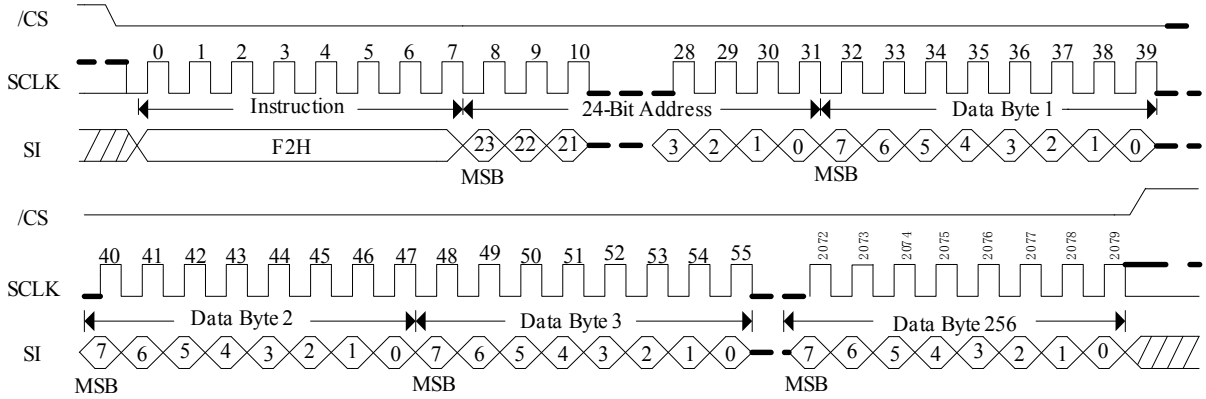


Figure 8-31. Fast Page Program Sequence Diagram

8.4.4 Sector Erase (20h)

The Sector Erase instruction is for erasing the all data of the chosen sector. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit. The Sector Erase instruction is entered by driving $\overline{CS}$ low, followed by the instruction code, and 3-address byte on SI. Any address inside the sector is a valid address for the Sector Erase instruction. $\overline{CS}$ must be driven low for the entire duration of the sequence.

The Sector Erase instruction sequence: $\overline{CS}$ goes low -> sending Sector Erase instruction -> 3-byte address on SI -> $\overline{CS}$ goes high. $\overline{CS}$ must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Sector Erase instruction is not executed. As soon as $\overline{CS}$ is driven high, the self-timed Sector Erase cycle (whose duration is t_{SE}) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write-in-Progress (WIP) bit. The WIP bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Sector Erase instruction applied to a sector which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits is not executed.

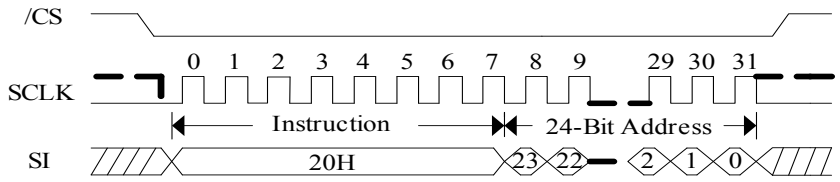


Figure 8-32. Sector Erase Sequence Diagram

8.4.5 32 kbytes Block Erase (52h)

The 32 kbytes Block Erase instruction is for erasing all data of a chosen block. A Write Enable instruction must have been previously executed to set the WEL bit. The 32 kB Block Erase instruction is entered by driving $\overline{CS}$ low, followed by the instruction code, and 3-byte address on SI. Any address inside the block is a valid address for the 32 kbytes Block Erase instruction. $\overline{CS}$ must be driven low for the entire duration of the sequence.

The 32 kbytes Block Erase instruction sequence: $\overline{CS}$ goes low -> sending 32 kB Block Erase instruction -> 3-byte address on SI -> $\overline{CS}$ goes high. $\overline{CS}$ must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 32 kB Block Erase instruction is not executed.

As soon as $\overline{CS}$ is driven high, the self-timed Block Erase cycle (whose duration is t_{BE}) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write-in-Progress (WIP) bit. The WIP bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 32 kB Block Erase instruction applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits is not executed.

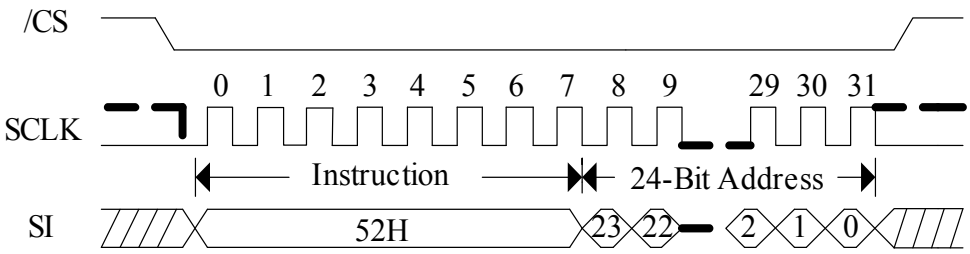


Figure 8-33. 32 kbytes Block Erase Sequence Diagram

8.4.6 64 kbytes Block Erase (D8h)

The 64 kbytes Block Erase instruction is for erasing the all data of the chosen block. A Write Enable instruction must previously have been executed to set the WEL bit. The 64 kbytes Block Erase instruction is entered by driving $\overline{CS}$ low, followed by the instruction code, and 3-byte address on SI. Any address inside the block is a valid address for the 64 kbytes Block Erase instruction. $\overline{CS}$ must be driven low for the entire duration of the sequence.

The 64 kbytes Block Erase instruction sequence: $\overline{CS}$ goes low sending 64 kbytes Block Erase instruction 3-byte address on SI $\overline{CS}$ goes high. $\overline{CS}$ must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 64 kbytes Block Erase instruction is not executed. As soon as $\overline{CS}$ is driven high, the self-timed Block Erase cycle (whose duration is t_{BE}) is initiated.

While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write-in-Progress (WIP) bit. The WIP bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the WEL bit is reset. A 64 kbytes Block Erase instruction applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits is not executed.

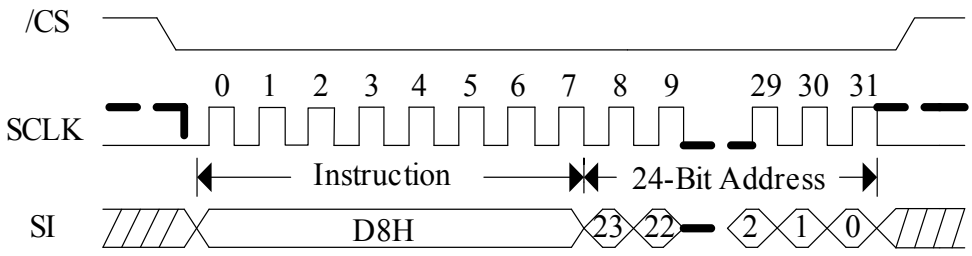


Figure 8-34. 64 kbytes Block Erase Sequence Diagram

8.4.7 Chip Erase (60/C7h)

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device accepts the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the $\overline{CS}$ pin low and shifting the instruction code C7h or 60h. The Chip Erase instruction sequence is shown in Figure 8-35.

The $\overline{CS}$ pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction is not executed. After $\overline{CS}$ is driven high, the self-timed Chip Erase instruction commences for a time duration of t_{CE}. While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the WIP bit.

The WIP bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other Instructions again. After the Chip Erase cycle has finished the WEL bit in the Status Register is cleared to 0. The Chip Erase instruction is executed only if all Block Protect (BP2, BP1, and BP0) bits are 0. The Chip Erase instruction is ignored if one or more sectors are protected.

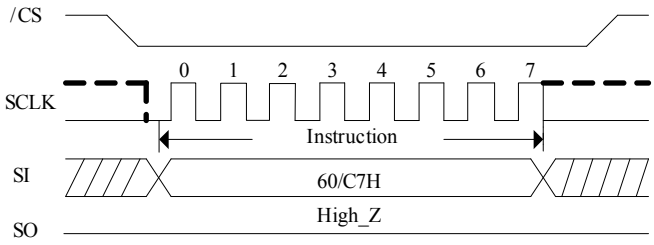


Figure 8-35. Chip Erase Sequence Diagram

8.4.8 Erase / Program Suspend (75h)

The Erase/Program Suspend instruction allows the system to interrupt a Sector or Block Erase operation, then read from or program data to any other sector. The Erase/Program Suspend instruction also allows the system to interrupt a Page Program operation and then read from any other page or erase any other sector or block. The Erase/Program Suspend instruction sequence is shown in Figure 8-36.

The Write Status Registers instruction (01h) and Erase instructions (20h, D8h, C7h, 60h, 44h) are not allowed during Erase Suspend. Erase Suspend is valid only during the Sector or Block erase operation. If written during the Chip Erase operation, the Erase Suspend instruction is ignored. The Write Status Registers instruction (01h), and Program instructions (02h, 42h) are not allowed during Program Suspend. Program Suspend is valid only during the Page Program operation.

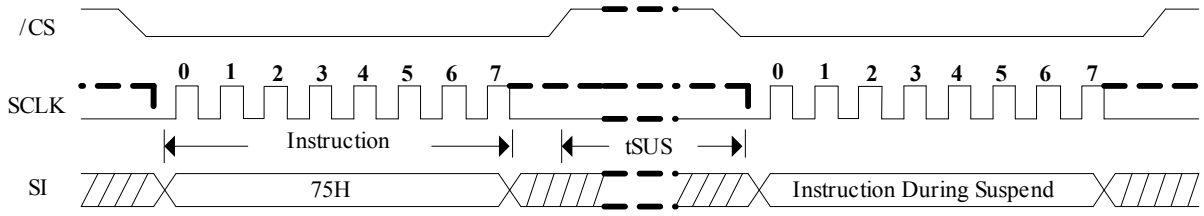


Figure 8-36. Erase/Program Suspend Command Sequence

8.4.9 Erase / Program Resume (7Ah)

The Erase/Program Resume instruction 7Ah must be written to resume the Sector or Block Erase operation or the Page Program operation after an Erase/Program Suspend. The Resume instruction 7Ah is accepted by the device only if the SUS bit in the Status Register equals to 1 and the WIP bit equals to 0.

After the Resume instruction is issued the SUS bit is cleared from 1 to 0 immediately, the WIP bit is set from 0 to 1 within 200 ns and the Sector or Block completes the erase operation or the page completes the program operation. If the SUS bit equals to 0 or the WIP bit equals to 1, the Resume instruction 7Ah is ignored by the device. The Erase/Program Resume instruction sequence is shown in Figure 8-37.

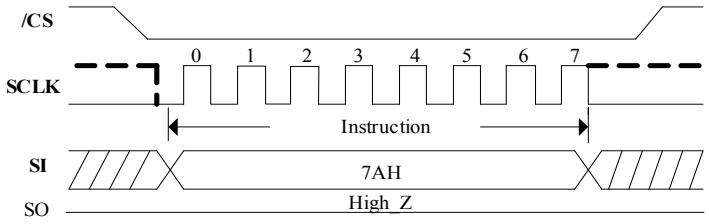


Figure 8-37. Erase/Program Resume Command Sequence

8.4.10 Read Serial Flash Discoverable Parameter (5Ah)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial Flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. For more detail on the SFDP parameters, please contact Adesto.

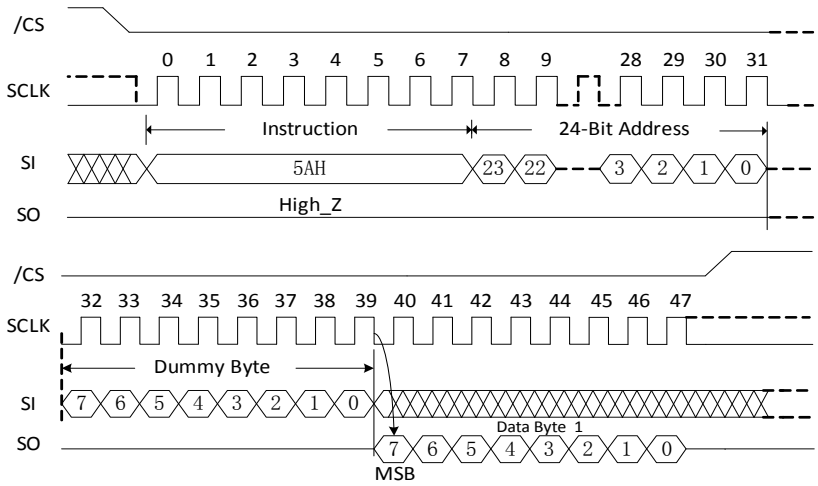


Figure 8-38. Read Serial Flash Discoverable Parameter Command Sequence Diagram

9. Electrical Characteristics

9.1 Absolute Maximum Ratings

Table 9-1. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Range	Units
Supply Voltage	VCC		-0.5 to 4	V
Voltage Applied to Any Pin	VIO	Relative to Ground	-0.5 to 4	V
Transient Voltage on any Pin	VIOT	<20nS Transient Relative to Ground	-2.0 to VCC + 2.0	V
Storage Temperature	TSTG		-65 to +150	ºC
Electrostatic Discharge Voltage	VESD	Human Body Model(1)	-2000 to +2000	V

Notes:
1. JEDEC Std JESD22-A114 (C1 = 100 pF, R1 = 1500Ω, R2 = 500Ω)

9.2 Operating Ranges

Table 9-2. Operating Range

PARAMETERS	SYMBOL	CONDITIONS	MIN	MAX	UNIT
Supply Voltage	VCC		2.7	3.6	V
Operating Temperature	TA	Industrial	-40	+85	ºC

9.3 Data Retention and Endurance

Table 9-3. Data Retention and Endurance

Parameter	Condition	Min	Max	Units
Erase/Program Cycles	4 kbytes sector, 32/64 kbytes block, or full chip	100,000		Cycles
Data Retention	Full temperature range	20		Years

9.4 Latch Up Characteristics

Table 9-4. Latch-up Characteristics

Parameter	Min	Max
Input Voltage Respect To GND on I/O Pins	-1.0 V	VCC + 1.0 V
VCC Current	-100 mA	100 mA

9.5 Power-up Timing

Table 9-5. Power-up Timing

Symbol	Parameter	Min	Max	Unit
t_{VSL}	VCC (min) To $\overline{CS}$ low	300		us

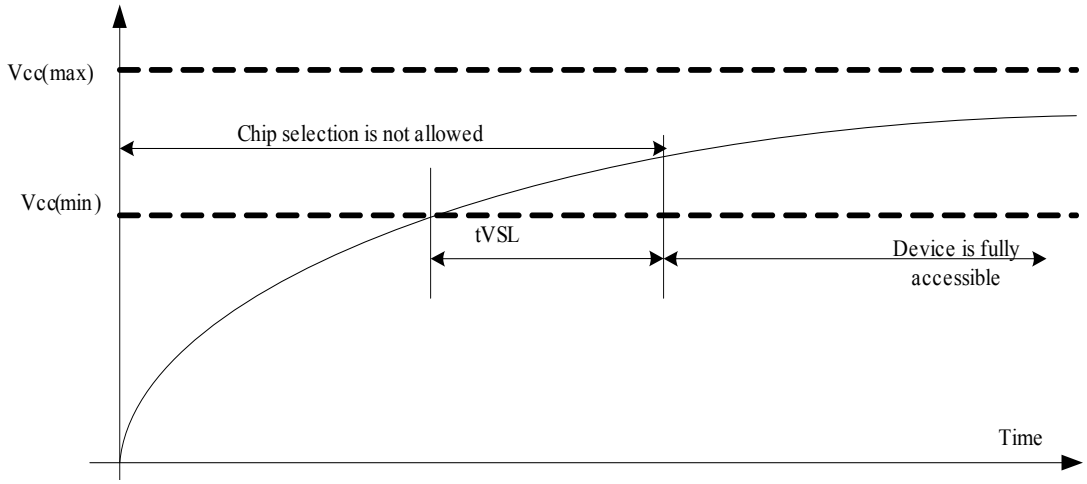


Figure 9-1. Power-up Timing and Voltage Levels

9.6 DC Electrical Characteristics

Table 9-6. DC Electrical Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
I_{LI}	Input Leakage Current				±2	µA
I_{LO}	Output Leakage Current				±2	µA
ICC_1	Standby Current	$\overline{CS}$ = VCC, VIN = VCC or GND		13	25	µA
ICC_2	Deep Power-Down Current	$\overline{CS}$ = VCC, VIN = VCC or GND		2	5	µA
ICC_3	Operating Current: (Read)	SCLK = 0.1VCC/0.9VCC, at 120 MHz, Q = Open (*1,*,2*4 I/O)		12	18	mA
		SCLK = 0.1VCC/0.9VCC, at 80MHz,Q = Open (*1,*,2*4 I/O)		10	16	mA
ICC_4	Operating Current (Page Program)	$\overline{CS}$ = VCC		15	20	mA
ICC_5	Operating Current (WRSR)	$\overline{CS}$ = VCC			5	mA
ICC_6	Operating Current (Sector Erase)	$\overline{CS}$ = VCC		9	20	mA
ICC_7	Operating Current (Block Erase)	$\overline{CS}$ = VCC		9	20	mA
ICC_8	Operating Current (Chip Erase)	$\overline{CS}$ = VCC		9	20	mA
V_{IL}	Input Low Voltage		-0.5		0.2 VCC	V
V_{IH}	Input High Voltage		0.8 VCC		VCC+0.4	V
V_{OL}	Output Low Voltage	IOL = 100 µA			0.4	V
V_{OH}	Output High Voltage	IOH = -100 µA	VCC-0.2			V

9.7 AC Measurement Conditions

Table 9-7. AC Measurement Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
C_L	Load Capacitance			30	pF	
t_R, t_F	Input Rise and Fall time			5	ns	
V_{IN}	Input Pause Voltage	0.2 VCC to 0.8 VCC			V	
IN	Input Timing Reference Voltage	0.5 VCC			V	
OUT	Output Timing Reference Voltage	0.5 VCC			V	

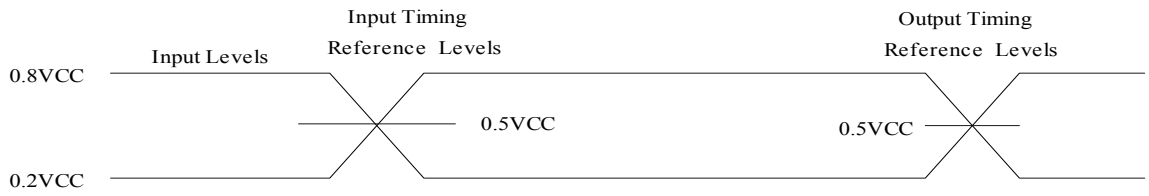


Figure 9-2. AC Measurement I/O Waveform

9.8 AC Electrical Characteristics

Table 9-8. AC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units
Fc_1	Clock frequency for Quad Output Fast Read (6Bh) on 3.0 V - 3.6 V power supply.	DC		133	MHz
Fc_2	Clock frequency for Read Data (03h) on 2.7 V - 3.6 V power supply.	DC		70	MHz
Fc_3	Clock frequency except for Quad Output Fast Read (6Bh) or Read Data (03h) on 3.0 V - 3.6 V power supply.	DC		120	MHz
Fc_4	Clock frequency except for Read Data (03h) on 2.7 V - 3.6 V power supply.	DC		108	MHz
t_{CLH}	Serial Clock High Time	3.75			ns
t_{CLL}	Serial Clock Low Time	3.75			ns
t_{CLCH}	Serial Clock Rise Time (Slew Rate)	0.1(1)			V/ns
t_{CHCL}	Serial Clock Fall Time (Slew Rate)	0.1(1)			V/ns
t_{SLCH}	$\overline{CS}$ Active Setup Time	5			ns
t_{CHSH}	$\overline{CS}$ Active Hold Time	5			ns
t_{SHCH}	$\overline{CS}$ Not Active Setup Time	5			ns

Table 9-8. AC Electrical Characteristics *(continued)*

Symbol	Parameter	Min	Typ	Max	Units
t_{CHSL}	$\overline{CS}$ Not Active Hold Time	5			ns
t_{SHSL}	$\overline{CS}$ High Time (read/write)	20			ns
t_{SHQZ}	Output Disable Time			6	ns
t_{CLQX}	Output Hold Time	0			ns
t_{DVCH}	Data In Setup Time	2			ns
t_{CHDX}	Data In Hold Time	2			ns
t_{HLCH}	$\overline{HOLD}$ Low Setup Time (relative to Clock)	5			ns
t_{HHCH}	$\overline{HOLD}$ High Setup Time (relative to Clock)	5			ns
t_{CHHL}	$\overline{HOLD}$ High Hold Time (relative to Clock)	5			ns
t_{CHHH}	$\overline{HOLD}$ Low Hold Time (relative to Clock)	5			ns
t_{HLQZ}	$\overline{HOLD}$ Low To High-Z Output			6	ns
t_{HHQX}	$\overline{HOLD}$ Low To Low-Z Output			6	ns
t_{CLQV}	Clock Low To Output Valid			7	ns
t_{WHSL}	Write Protect Setup Time Before $\overline{CS}$ Low	20			ns
t_{SHWL}	Write Protect Hold Time After $\overline{CS}$ High	100			ns
t_{DP}	$\overline{CS}$ High To Deep Power-Down Mode			20	µs
t_{RES1}	$\overline{CS}$ High To Standby Mode Without Electronic Signature Read			20	µs
t_{RES2}	$\overline{CS}$ High To Standby Mode With Electronic Signature Read			20	µs
t_{SUS}	$\overline{CS}$ High To Next Instruction After Suspend			20	µs
t_{RST_R}	$\overline{CS}$ High To Next Instruction After Reset (from read)			20	
t_{RST_P}	$\overline{CS}$ High To Next Instruction After Reset (from program)			20	
t_{RST_E}	$\overline{CS}$ High To Next Instruction After Reset (from erase)			12	
t_W	Write Status Register Cycle Time		5	30[2]	ms
t_{BP1}	Byte Program Time (First Byte)		30	50	µs
t_{BP2}	Additional Byte Program Time (After First Byte)		2.5	12	µs
t_{PP}	Page Programming Time		0.6	2.4	ms
t_{SE}	Sector Erase Time		70	300	ms
t_{BE}	Block Erase Time (32K Bytes/64K Bytes)		0.15/ 0.25	1.6/2.0	sec
t_{CE}	Chip Erase Time		60	120	sec

Notes:

1. Tested with clock frequency lower than 50 MHz.

2. For multiple bytes after first byte within a page, $t_{BPn} = t_{BP1} + t_{BP2} * N$, where N is the number of bytes programmed.

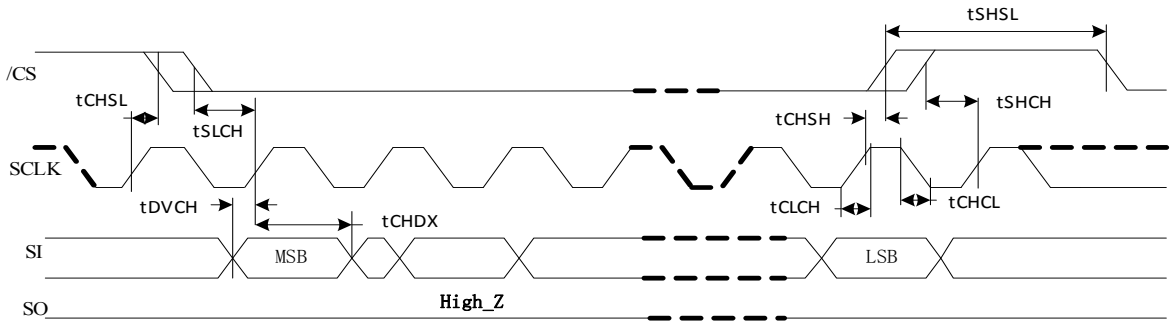


Figure 9-3. Serial Input Timing

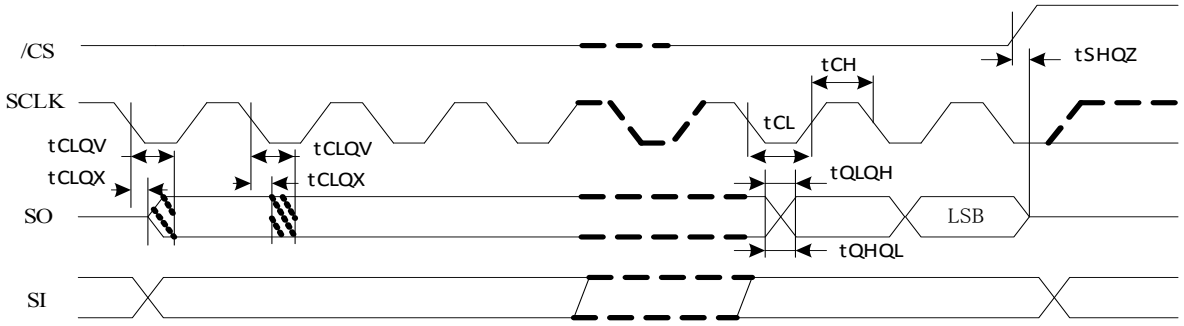


Figure 9-4. Output Timing

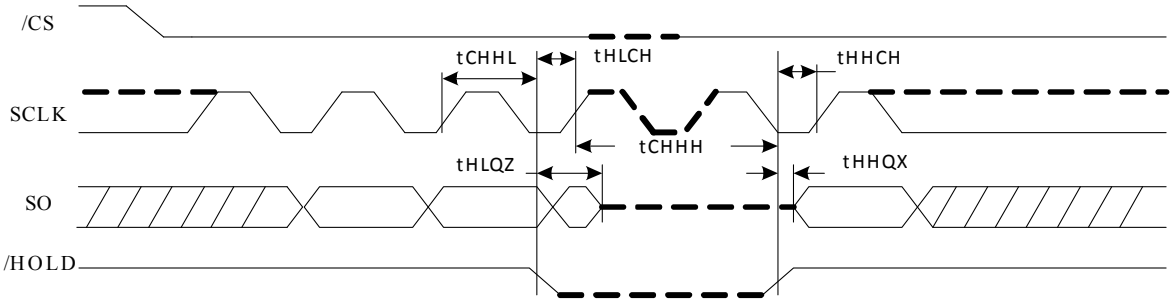


Figure 9-5. $\overline{\text{HOLD}}$ Timing

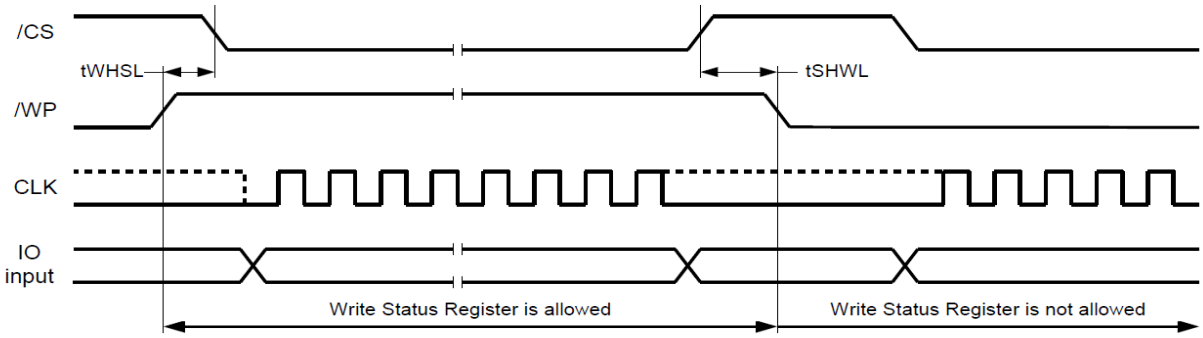
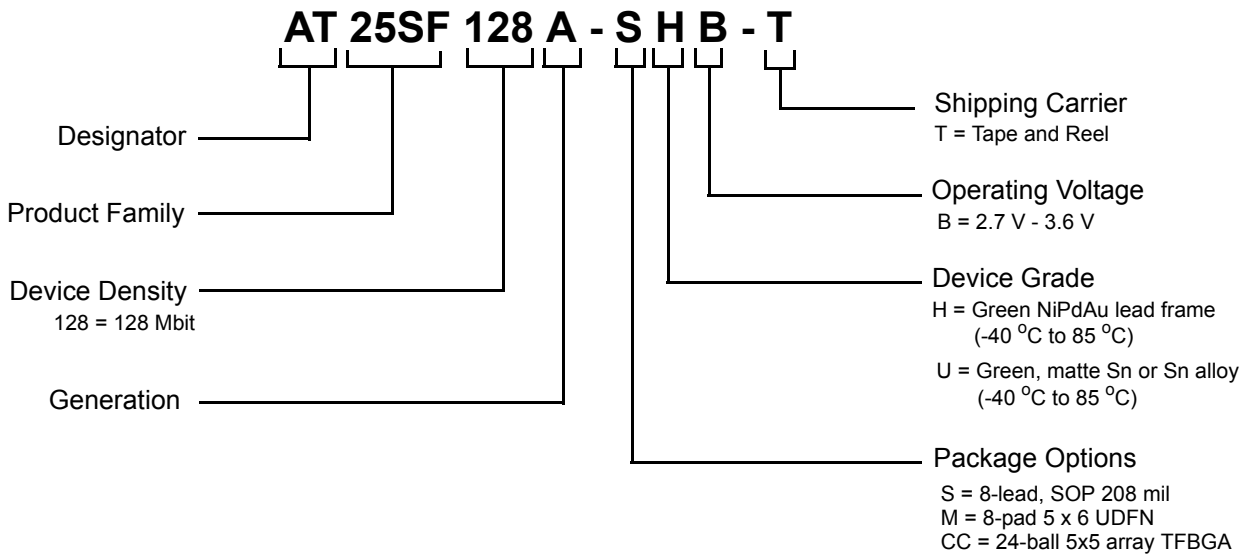


Figure 9-6. $\overline{\text{WP}}$ Timing

10. Ordering Information



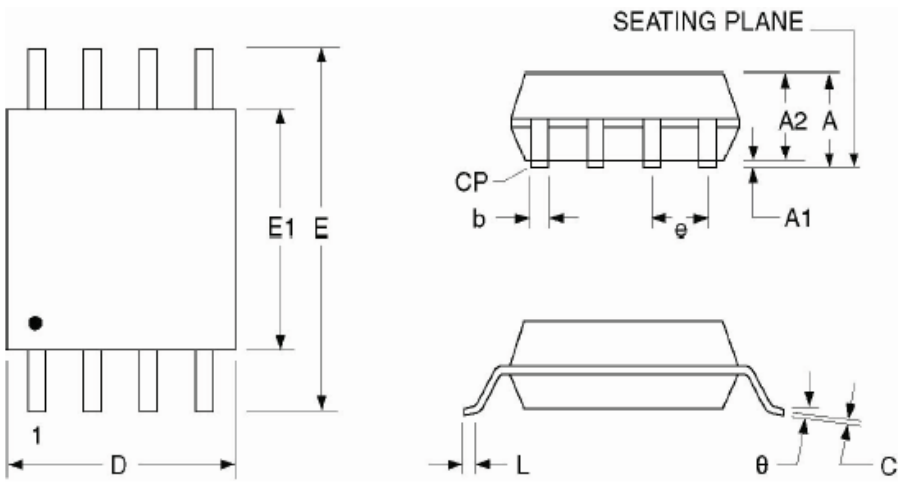
Ordering Code	Package Type	Lead Finish	Operating Voltage	Maximum Frequency	Operating Range
AT25SF128A-SHB-T	8S4	NiPdAu	2.7 - 3.6 V	133 MHz (1)	-40 °C to 85 °C
AT25SF128A-MHB-T	8MA1 (2)				
AT25SF128A-CCUB-T	24CC(2)	Sn or Sn Alloy			

1. Only for Quad Output Fast Read (6Bh) command with 3.0 V - 3.6 V power supply.
2. Contact Adesto for more information.

Package Type	
8S4	8-lead, 0.208" Wide, Plastic Gull Wing Small Outline Package (EIAJ SOIC)
8MA1	8-pad (5 x 6 x 0.6 mm body), Thermally Enhanced Plastic Ultra-Thin Dual Flat No-lead (UDFN)
24CC	24-ball, thin profile, fine pitch, 6 x 6 x 1.2 mm, 5 x 5 ball array TFBGA Package

11. Package Information

11.1 8S4 — 8-Pin SOP 208-mil

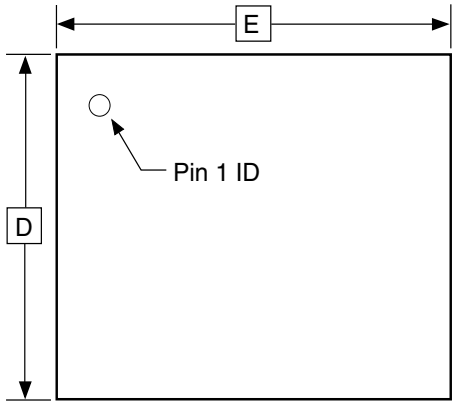


SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.75	1.95	2.16	0.069	0.077	0.085
A1	0.05	0.15	0.25	0.002	0.006	0.010
A2	1.70	1.80	1.91	0.067	0.071	0.075
B	0.35	0.42	0.48	0.014	0.017	0.019
C	0.19	0.20	0.25	0.007	0.008	0.010
D	5.18	5.28	5.38	0.204	0.208	0.212
E	7.70	7.90	8.10	0.303	0.311	0.319
E1	5.18	5.28	5.38	0.204	0.208	0.212
e	1.27 BSC			0.050 BSC		
L	0.50	0.65	0.80	0.020	0.026	0.031
Θ	0°	-	8°	0°	-	8°
Y	-	-	0.10	-	-	0.004

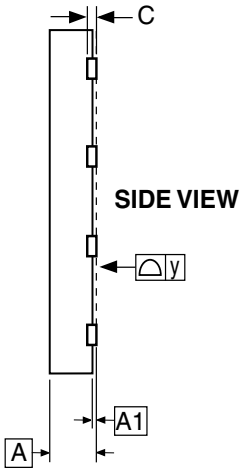
5/5/16

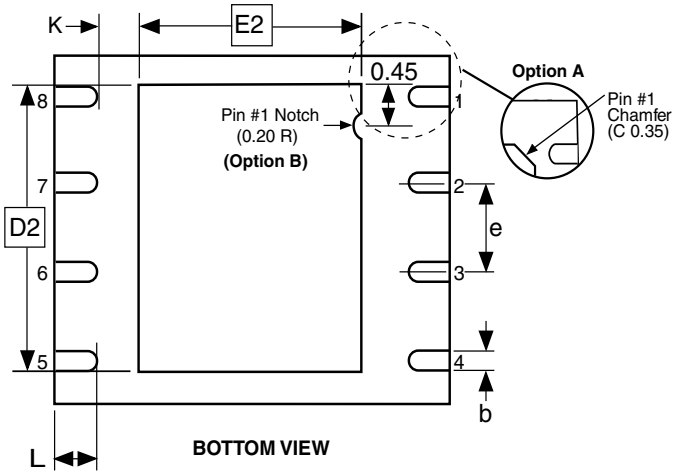
Package Drawing Contact: contact@adestotech.com	TITLE 8S3, 8-lead, 0.208" Body, Plastic Small Outline Package (EIAJ)	GPC STN	DRAWING NO. 8S3	REV. A

11.2 8MA1 — 8-Pad UDFN



TOP VIEW





BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

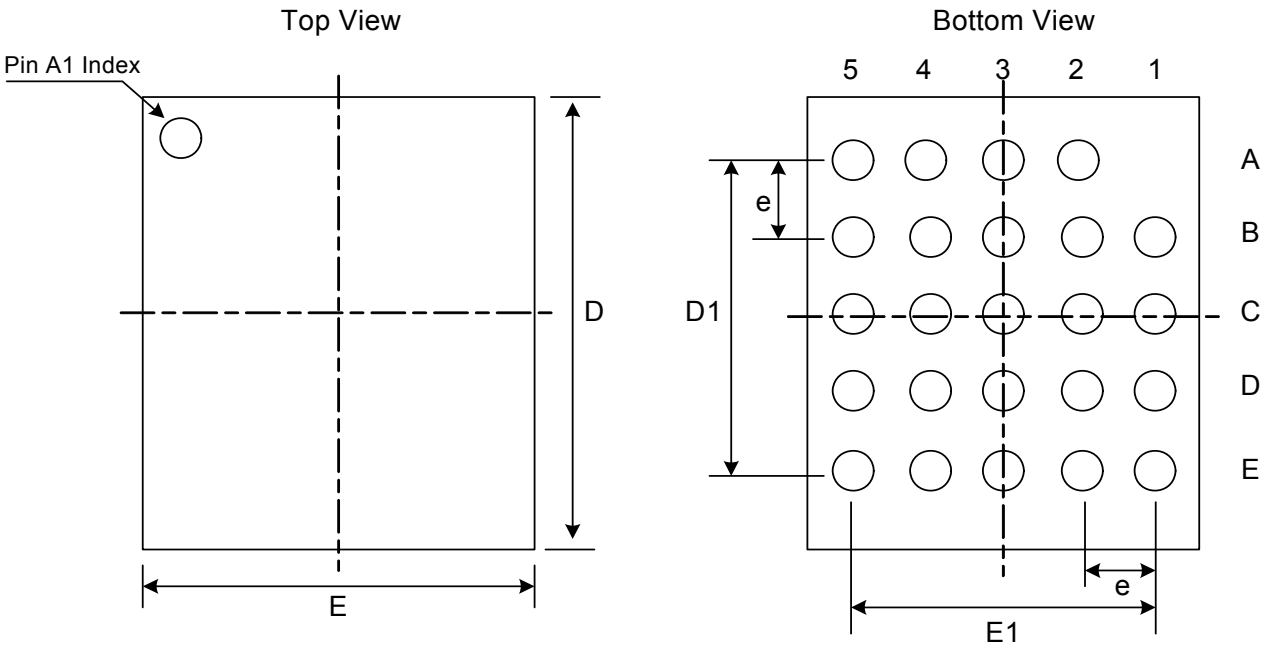
SYMBOL	MIN	NOM	MAX	NOTE
A	0.45	0.55	0.60	
A1	0.00	0.02	0.05	
b	0.35	0.40	0.48	
C		0.152 REF		
D	4.90	5.00	5.10	
D2	3.80	4.00	4.20	
E	5.90	6.00	6.10	
E2	3.20	3.40	3.60	
e		1.27		
L	0.50	0.60	0.75	
y	0.00	–	0.08	
K	0.20	–	–	

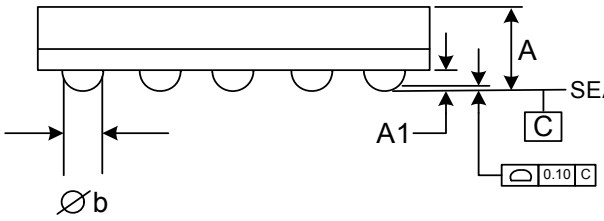
Notes: 1. This package conforms to JEDEC reference MO-229, Saw Singulation.
2. The terminal #1 ID is a Laser-marked Feature.

4/15/08

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: contact@adestotech.com	**8MA1,** 8-pad (5 x 6 x 0.6 mm Body), Thermally Enhanced Plastic Ultra Thin Dual Flat No Lead Package (UDFN)	YFG	8MA1	D

11.3 24CC — 24-Ball TFBGA





Symbol	Dimensions		
	Min	Nom	Max
A	-	-	1.20
A1	0.26	0.31	0.36
b	0.35	0.40	0.45
D	7.90	8.00	8.10
D1	4.00 BSC		
E	5.90	6.00	6.10
E1	4.00 BSC		
e	1.00 BSC		

Controlling Dimension: mm
Reference Document: JEDEC MO-207

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: contact@adestotech.com	24-ball, thin profile, fine pitch, 6 x 6 x 1.2 mm, 5 x 5 ball array TFBGA Package		24B	A

12. Revision History

Table 12-1. Document Revision History

Revision	Date	Change Description
A	10/2018	Initial release.
B	11/2018	Added 133 MHz maximum frequency for Quad Output Fast Read operation. Added read throughput value of 532 Mbps for Quad Output Fast Read on page 1. Removed High Performance Mode references throughout document. Updated Data Retention and Endurance Table 9-3. Updated first four rows of Table 9-8, AC Electrical Characteristics to include the Quad Output Fast Read instruction timing.
C	02/2019	Added 24CC TFBGA package drawing. Added 24CC TFBGA pinout drawing. Updated package types on page 1. Changed designation from ADVANCED to PRELIMINARY. Updated Ordering Codes section.
D	03/2019	Updated ICC4, ICC6, ICC7, and ICC8 values in Table 9-6, DC Electrical Characteristics
E	07/2019	Removed SFDP tables and updated Section 8.4.10, Read SFDP (5Ah). Updated text in Section 8.4.10, Read SFDP. Updated document to new Adesto template. Updated Section 3.7, HOLD. Updated definition of SRP[1:0] bits in Section 6.4.2.4. Reformatted tables in Section 6.4.1, Status registers. Updated Table 6-2, Status register protections.
F	02/2020	Minor grammatical edits. Changed chip erase time (t_{CE}) from 30 to 60 sec. Updated document status from Preliminary to Complete.

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