



SILEGO

SLG5NV1430V

Ultra-small 7.8 mΩ 4 A Load Switch with Discharge

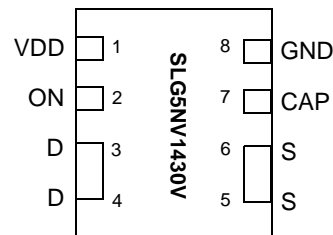
General Description

The SLG5NV1430V is a 7.8 mΩ 4 A single-channel load switch that is able to switch 1 to 5 V power rails. The product is packaged in an ultra-small 1.5 x 2.0 mm package.

Features

- 1.5 x 2.0 mm FC-TDFN 8L package (2 fused pins for drain and 2 fused pins for source)
- Logic level ON pin capable of supporting 0.85 V CMOS Logic
- User selectable ramp rate with external capacitor
- 7.8 mΩ RDS_{ON} while supporting 4 A
- Discharges load when off
- Two Over Current Protection Modes
 - Short Circuit Current Limit
 - Active Current Limit
- Over Temperature Protection
- Pb-Free / Halogen-Free / RoHS compliant
- Operating Temperature: -20 °C to 70°C
- Operating Voltage: 2.5 V to 5.5 V

Pin Configuration

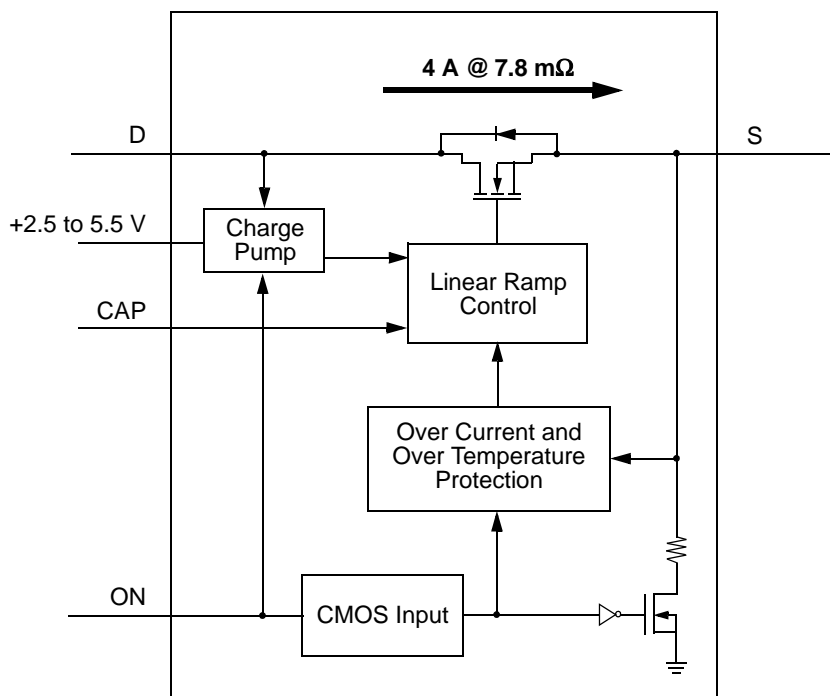


8-pin FC-TDFN
(Top View)

Applications

- Notebook Power Rail Switching
- Tablet Power Rail Switching
- Smartphone Power Rail Switching

Block Diagram





Pin Description

| Pin # | Pin Name | Type | Pin Description |
|-------|----------|--------|--|
| 1 | VDD | PWR | VDD power for load switch control (2.5 V to 5.5 V) |
| 2 | ON | Input | Turns MOSFET ON (4 M Ω pull down resistor) CMOS input with VIL < 0.3 V, VIH > 0.85 V |
| 3 | D | MOSFET | Drain of Power MOSFET (fused with pin 4) |
| 4 | D | MOSFET | Drain of Power MOSFET (fused with pin 3) |
| 5 | S | MOSFET | Source of Power MOSFET (fused with pin 6) |
| 6 | S | MOSFET | Source of Power MOSFET (fused with pin 5) |
| 7 | CAP | Input | Capacitor for controlling power rail ramp rate |
| 8 | GND | GND | Ground |

Ordering Information

| Part Number | Type | Production Flow |
|---------------|----------------------------|-----------------------------|
| SLG5NV1430V | FC-TDFN 8L | Commercial, -20 °C to 70 °C |
| SLG5NV1430VTR | FC-TDFN 8L (Tape and Reel) | Commercial, -20 °C to 70 °C |



Absolute Maximum Ratings

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|-------------------|-----------------------------------|--|------|------|------|------|
| V_{DD} | Power Supply | | -- | -- | 7 | V |
| T_S | Storage Temperature | | -65 | -- | 150 | °C |
| ESD_{HBM} | ESD Protection | Human Body Model | 2000 | -- | -- | V |
| W_{DIS} | Package Power Dissipation | | -- | -- | 1 | W |
| MOSFET IDS_{PK} | Peak Current from Drain to Source | For no more than 1 ms with 1% duty cycle | -- | -- | 6 | A |

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

$T_A = -20$ to 70 °C (unless otherwise stated)

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|------------------|--------------------------------------|---|---------------------------|------|----------|------|
| V_{DD} | Power Supply Voltage | -20 to 70°C | 2.5 | -- | 5.5 | V |
| I_{DD} | Power Supply Current (PIN 1) | when OFF | -- | -- | 1 | μA |
| | | when ON, No load | -- | 70 | 100 | μA |
| $R_{DS_{ON}}$ | Static Drain to Source ON Resistance | T_A 25°C @ 100 mA | -- | 7.8 | 8.5 | mΩ |
| | | T_A 70°C @ 100 mA | -- | 8.5 | 9.6 | mΩ |
| IDS | Operating Current | $V_D = 1.0$ V to 5.5 V | -- | -- | 4 | A |
| V_D | Drain Voltage | | 1.0 | -- | V_{DD} | V |
| T_{ON_Delay} | ON pin Delay Time | 50% ON to Ramp Begin | 0 | 300 | 500 | μs |
| T_{Total_ON} | Total Turn On Time | 50% ON to 90% V_S | Configurable ¹ | | | ms |
| | | Example: CAP (PIN 7) = 4 nF, $V_{DD} = V_D = 5$ V, Source_Cap = 10 μF, $IDS = 100$ mA | -- | 1.96 | -- | ms |
| $T_{SLEWRATE}$ | Slew Rate | 10% V_S to 90% V_S | Configurable ¹ | | | V/ms |
| | | Example: CAP (PIN 7) = 4 nF, $V_{DD} = V_D = 5$ V, Source_Cap = 10 μF, $IDS = 100$ mA | -- | 3.0 | -- | V/ms |
| CAP_{SOURCE} | Source Cap | Source to GND | -- | -- | 500 | μF |
| R_{DIS} | Discharge Resistance | | 100 | 150 | 300 | Ω |
| ON_V_{IH} | High Input Voltage on ON pin | | 0.85 | -- | V_{DD} | V |
| ON_V_{IL} | Low Input Voltage on ON pin | | -0.3 | 0 | 0.3 | V |
| I_{LIMIT} | Active Current Limit | MOSFET will automatically limit current when $V_S > 250$ mV | -- | 6.0 | -- | A |
| | Short Circuit Current Limit | MOSFET will automatically limit current when $V_S < 250$ mV | -- | 0.5 | -- | A |
| $THERM_{ON}$ | Thermal shutoff turn-on temperature | | -- | 125 | -- | °C |
| $THERM_{OFF}$ | Thermal shutoff turn-off temperature | | -- | 100 | -- | °C |
| $THERM_{TIME}$ | Thermal shutoff time | | -- | -- | 1 | ms |
| T_{OFF_Delay} | OFF Delay Time | 50% ON to V_S Fall, $V_{DD} = V_D = 5$ V | -- | -- | 15 | μs |
| T_{FALL} | V_S Fall Time | 90% V_S to 10% V_S , $V_{DD} = V_D = 5$ V | -- | TBD | -- | μs |

Notes:

1. Refer to table for configuration details.



SLG5NV1430V Turn ON

The normal power on sequence is first VDD, with VD only being applied after VDD is > 1 V, and then ON after VD is at least 90% of final value. The normal power off sequence is the power on sequence in reverse.

If VDD and VD are turned on at the same time then it is possible that a voltage glitch will appear on VS before VDD achieves 1V which is the V_T of the main MOSFET. The size of the glitch is dependent on source and drain capacitance loading and the ramp rate of VDD & VD.

SLG5NV1430V Turn ON

The VS ramp follows a linear path, not an RC limitation provided the ramp is slow enough to not be current limited by load capacitance.

SLG5NV1430V Current Limiting

The SLG5NV1430V has two forms of current limiting.

Standard Current Limiting Mode

Current is measured by mirroring the current through the main MOSFET. The mirrored current is then sent through a resistor creating a voltage $V(i)$ proportional to the MOSFET current. The $V(i)$ is then compared with a Band Gap voltage $V(BG)$. If $V(i)$ exceeds the Band Gap voltage then the voltage $V(g)$ on the gate of the main MOSFET is reduced. The $V(g)$ continues to drop until $V(i) < V(BG)$. This response is a closed loop response and is therefore very fast and current limits in less than a few micro-seconds. There is no difference between peak or constant current limit.

Temperature Cutoff

However, as the $V(g)$ drops the $R_{ds}(ON)$ of the main MOSFET will increase, thus limiting the current, but also increasing the power dissipation of the IC. The IC is very small and cannot dissipate much power. Therefore, if a current limit condition is sustained the IC will heat up. If the temperature exceeds approximately 120°C, then $V(g)$ will be brought low completely shutting off the main MOSFET. As the die cools the MOSFET will be turned back on at 100°C.

If the current limiting condition has not been mitigated then the die will again heat up to 120°C and the process will repeat.

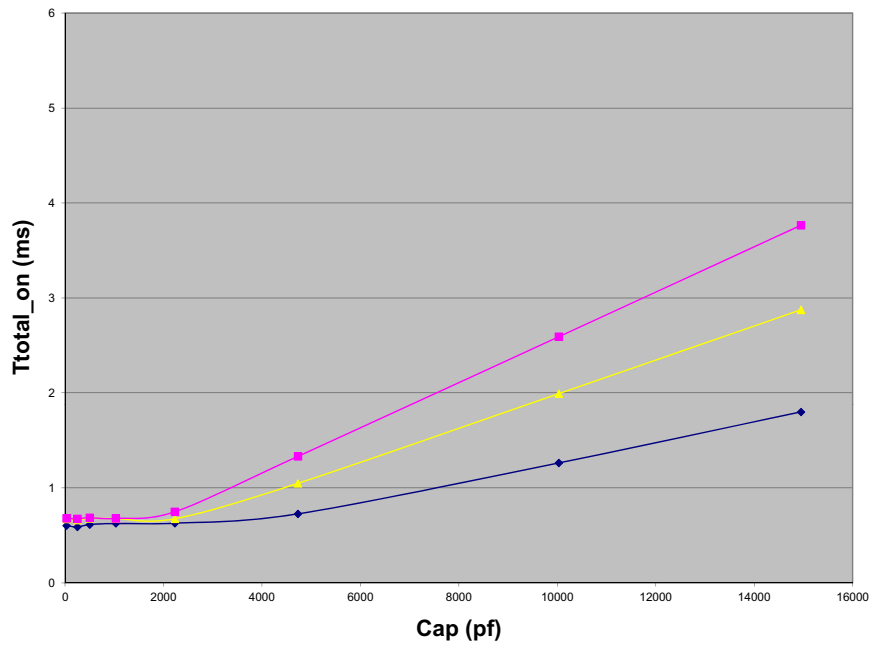
Short Circuit Current Limiting Mode

When $V(S) < 250$ mV, which is the case if there is a solder bridge during the manufacturing process or a hard short on the power rail, then the current is limited to approximately 500 mA. This current limit is accomplished in the same manner as the Standard Current Limiting Mode with the exception that the current mirror is 15x greater. Because the current mirror is so much larger, a 15x smaller main MOSFET current is required to generate the same $V(i)$. If $V(S)$ rises above approximately 250 mV, then this mode is automatically switched out.



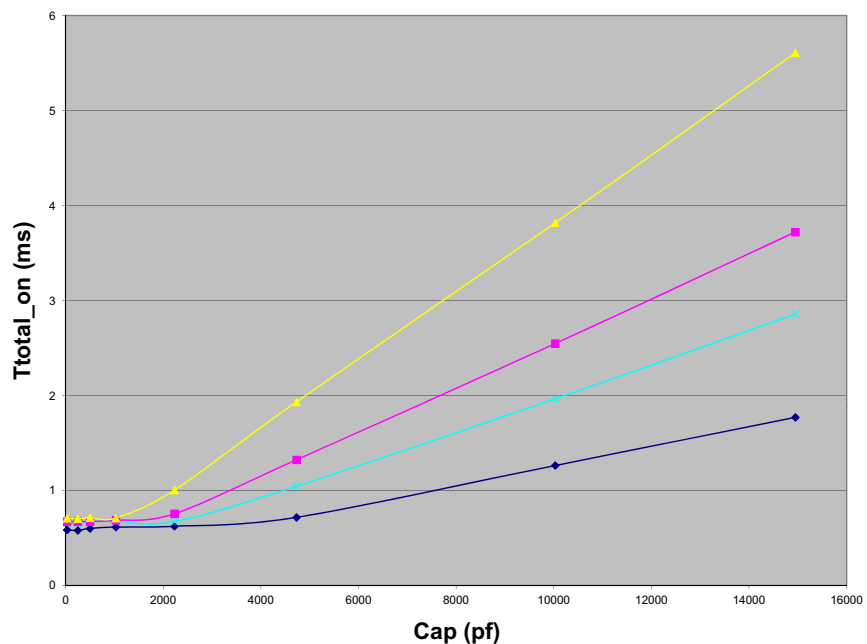
$T_{\text{Total_ON}}$ vs. CAP @ $V_{\text{DD}} = 3.3 \text{ V}$

SLG5NV1430V $T_{\text{Total_ON}}$: ON (50%) - V_{S} (90%)
 $V_{\text{DD}} = 3.3 \text{ V}$, $T_{\text{A}} = 25^\circ\text{C}$, $C_{\text{L}} = 10 \mu\text{F}$, $I_{\text{DS}} = 100 \text{ mA}$



$T_{\text{Total_ON}}$ vs. CAP @ $V_{\text{DD}} = 5.0 \text{ V}$

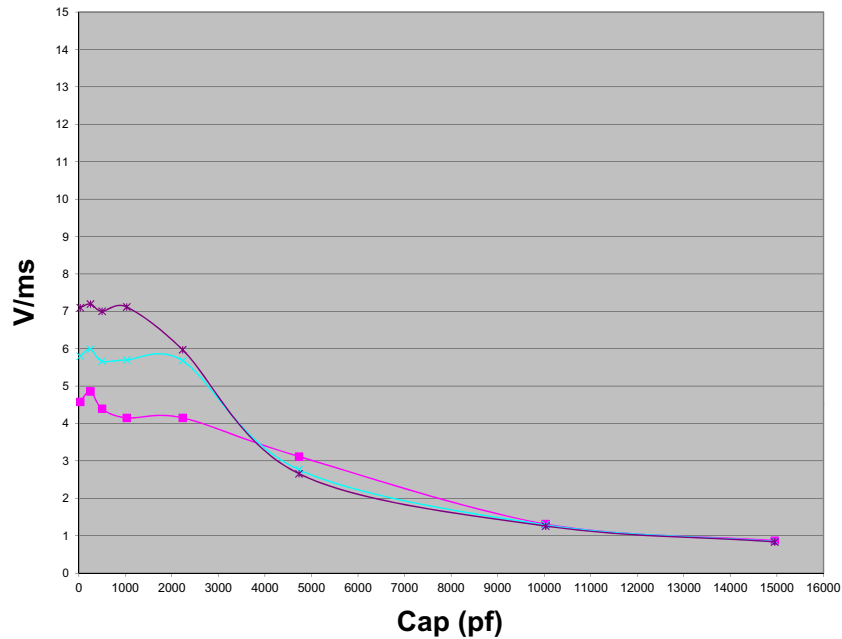
SLG5NV1430V $T_{\text{Total_ON}}$: ON (50%) - V_{S} (90%)
 $V_{\text{DD}} = 5.0 \text{ V}$, $T_{\text{A}} = 25^\circ\text{C}$, $C_{\text{L}} = 10 \mu\text{F}$, $I_{\text{DS}} = 100 \text{ mA}$





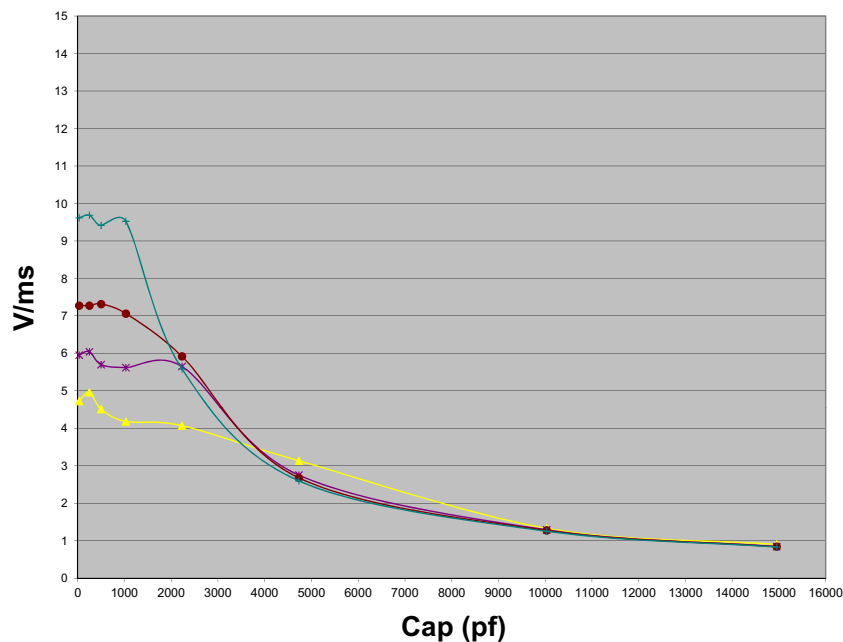
T_{SLEW} vs. CAP @ $V_{DD} = 3.3\text{ V}$

SLG5NV1430V T_{SLEW} : $V_S(10\%) - V_S(90\%)$
 $V_{DD} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, $C_L = 10\text{ }\mu\text{F}$, $I_{DS} = 100\text{ mA}$



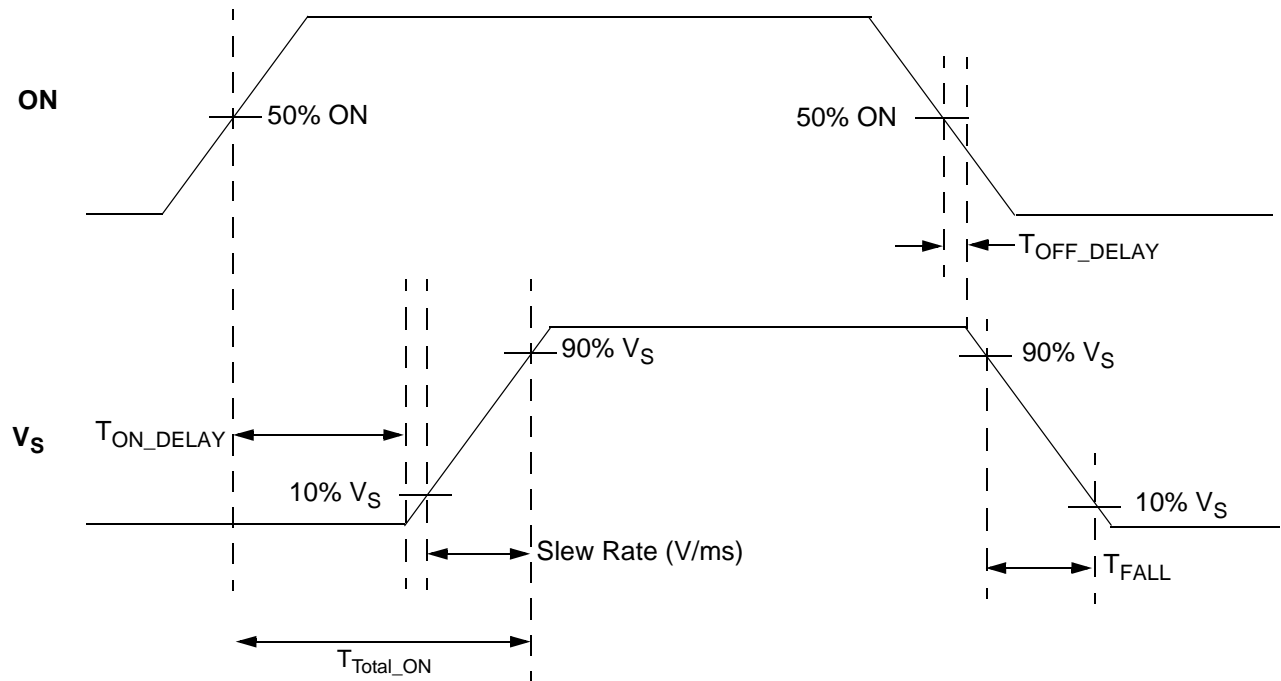
T_{SLEW} vs. CAP @ $V_{DD} = 5.0\text{ V}$

SLG5NV1430V T_{SLEW} : $V_S(10\%) - V_S(90\%)$
 $V_{DD} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$, $C_L = 10\text{ }\mu\text{F}$, $I_{DS} = 100\text{ mA}$



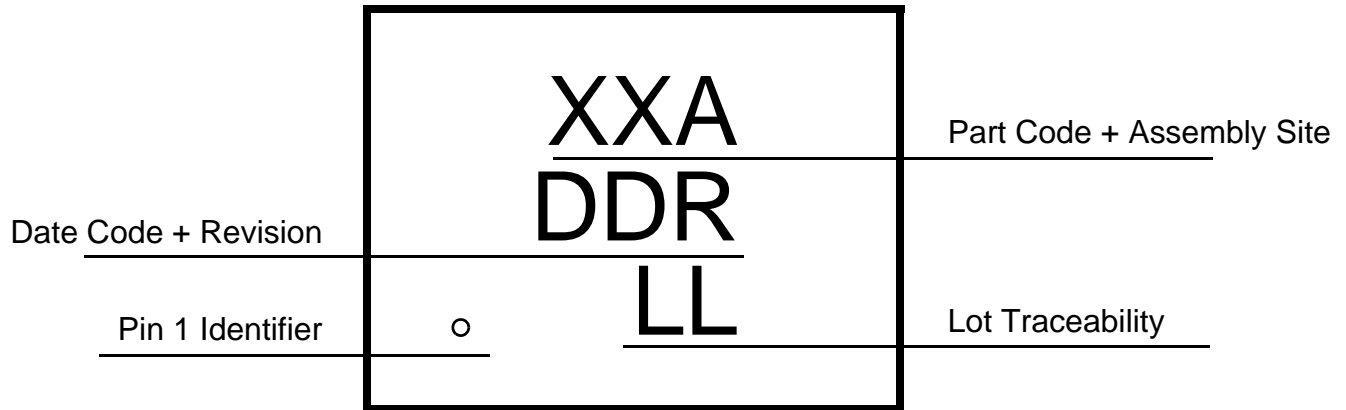


T_{Total_ON} , T_{ON_Delay} and Slew Rate Measurement





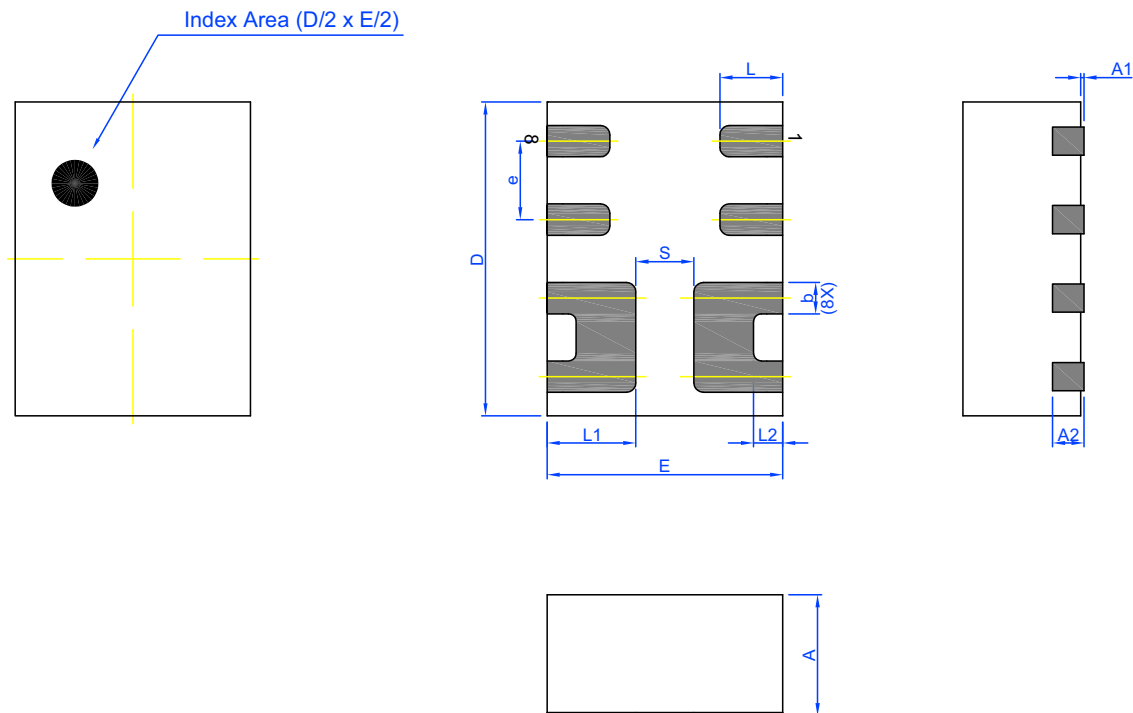
Package Top Marking System Definition





Package Drawing and Dimensions

8 Lead TDFN Package 1.5 x 2.0 mm (Fused Lead)
JEDEC MO-252, Variation W2015D



Unit: mm

| Symbol | Min | Nom. | Max | Symbol | Min | Nom. | Max |
|--------|-------|------|-------|--------|----------|-------|-------|
| A | 0.70 | 0.75 | 0.80 | L | 0.35 | 0.40 | 0.45 |
| A1 | 0.005 | - | 0.060 | L1 | 0.515 | 0.565 | 0.615 |
| A2 | 0.15 | 0.20 | 0.25 | L2 | 0.135 | 0.185 | 0.235 |
| b | 0.15 | 0.20 | 0.25 | e | 0.50 BSC | | |
| D | 1.95 | 2.00 | 2.05 | S | 0.37 REF | | |
| E | 1.45 | 1.50 | 1.55 | | | | |

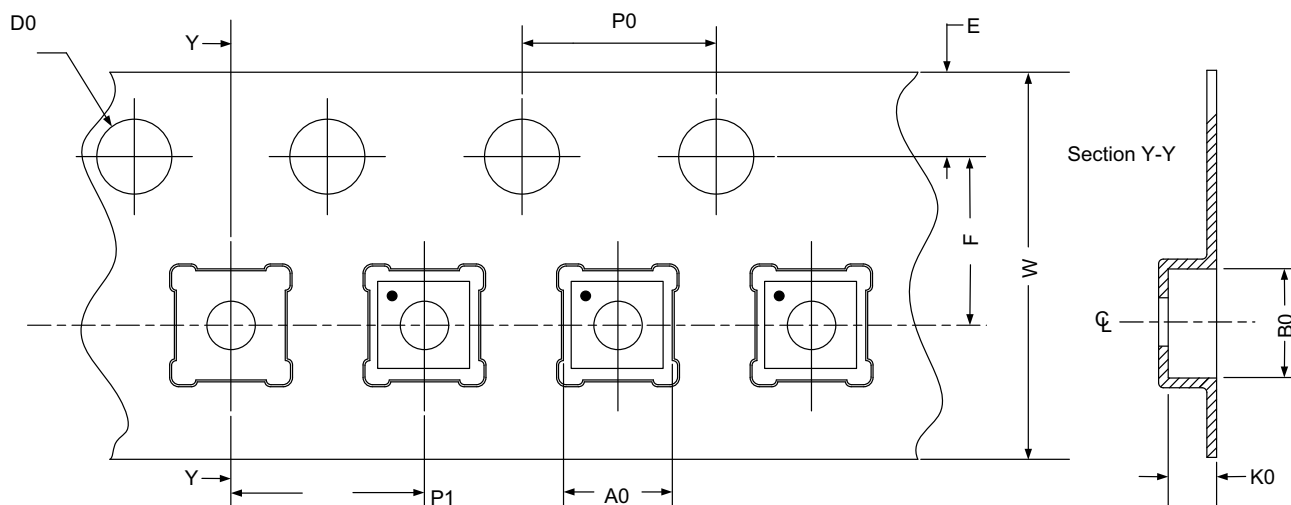


Tape and Reel Specifications

| Package Type | # of Pins | Nominal Package Size [mm] | Max Units | | Reel & Hub Size [mm] | Leader (min) | | Trailer (min) | | Tape Width [mm] | Part Pitch [mm] |
|------------------|-----------|---------------------------|-----------|---------|----------------------|--------------|-------------|---------------|-------------|-----------------|-----------------|
| | | | per Reel | per Box | | Pockets | Length [mm] | Pockets | Length [mm] | | |
| TDFN 8L FC Green | 8 | 1.5 x 2.0 x 0.75 | 3000 | 3000 | 178 / 60 | 100 | 400 | 100 | 400 | 8 | 4 |

Carrier Tape Drawing and Dimensions

| Package Type | Pocket BTM Length | Pocket BTM Width | Pocket Depth | Index Hole Pitch | Pocket Pitch | Index Hole Diameter | Index Hole to Tape Edge | Index Hole to Pocket Center | Tape Width |
|------------------|-------------------|------------------|--------------|------------------|--------------|---------------------|-------------------------|-----------------------------|------------|
| | A0 | B0 | K0 | P0 | P1 | D0 | E | F | W |
| TDFN 8L FC Green | 1.68 | 2.18 | 0.9 | 4 | 4 | 1.5 | 1.75 | 3.5 | 8 |



Refer to EIA-481 specification

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.25 mm³ (nominal). More information can be found at www.jedec.org.

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