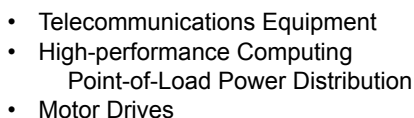




Pin Configuration

Designed to operate over a -40°C to 85°C range, the SLG59H1019V is available in a low thermal resistance, RoHS-compliant, 1.6 x 3.0 mm STQFN package.

- Wide Operating Input Voltage: 4.5 V to 25.2 V
- Maximum Continuous Switch Current: 5 A
- Automatic nFET SOA Protection
- High-performance MOSFET Switch
 - Low $R_{DS(ON)}$: 13 m Ω at $V_{IN} = 25.2$ V
 - Low $\Delta R_{DS(ON)} / \Delta V_{IN}$: <0.05 m Ω /V
 - Low $\Delta R_{DS(ON)} / \Delta T$: <0.06 m Ω /°C
- Capacitor-adjustable Inrush Current Control
- Two stage Current Limit Protection:
 - Resistor-adjustable Active Current Limit
 - Internal Short-circuit Current limit
- Open Drain FAULT Signaling
- MOSFET Current Analog Output Monitor: 10 μ A/A
- Fast 0.75 k Ω Output Discharge
- Pb-Free / Halogen-Free / RoHS Compliant Packaging



The block diagram illustrates the internal architecture of the LTC3890, including the Charge Pump, Linear Ramp Control, State Machine (CL/SC Detection and Over Temperature Protection), CMOS Input, Discharge, and the 3.1 V VIN UVLO. External components and connections are shown, such as VIN, VOUT, IOUT, and FAULT, along with various capacitors (C1, C2, C3, C4, C5, CSLEW, CLOAD, CIOUT) and resistors (RSET, RPU, RIOU, 1 MΩ). The diagram also indicates the connection of the 3 V FS - Connect to System ADC and the FAULT signal to the System GPI.



Pin Description

Pin #	Pin Name	Type	Pin Description
1	ON	Input	A low-to-high transition on this pin initiates the operation of the SLG59H1019V's state machine. ON is an asserted HIGH, level-sensitive CMOS input with $V_{IL} < 0.3 \text{ V}$ and $V_{IH} > 0.9 \text{ V}$. Even though the ON pin circuit has a 1 M Ω internal pull-down resistor internally grounded, connect this pin to a general-purpose output (GPO) of a microcontroller, an application processor, or a system controller.
2	GND	GND	Pin 2 is a low-current GND terminal for the SLG59H1019V. Connect directly to Pin 3
3	GND	GND	Pin 3 is the main ground connection for the SLG59H1019V's internal charge pump, its gate drive and current-limit circuits as well as its internal state machine. Therefore, use a short, stout connection from Pin 3 to the system's analog or power plane.
4-8	VIN	MOSFET	VIN supplies the power for the operation of the SLG59H1019V, its internal control circuitry, and the drain terminal of the nFET power switch. With 5 pins fused together at VIN, connect a 47 μF (or larger) low-ESR capacitor from this pin to ground. Capacitors used at VIN should be rated at 50 V or higher.
9-13	VOUT	MOSFET	Source terminal of n-channel MOSFET (5 pins fused for VOUT). Connect a 47 μF (or larger) low-ESR capacitor from this pin to ground. Capacitors used at VOUT should be rated at 50 V or higher.
14	NC	Null	No Connect – Do not make any connection to this pin.
15	$\overline{\text{FAULT}}$	Output	An open drain output, $\overline{\text{FAULT}}$ is asserted within $T_{\text{FAULT_LOW}}$ when a current-limit or an over-temperature condition is detected. $\overline{\text{FAULT}}$ is deasserted within $T_{\text{FAULT_HIGH}}$ when the fault condition is removed. Connect an 100 k Ω external resistor from the $\overline{\text{FAULT}}$ pin to local system logic supply.
16	CAP	Output	A low-ESR, stable dielectric, ceramic surface-mount capacitor connected from CAP pin to GND sets the V_{OUT} slew rate and overall turn-on time of the SLG59H1019V. For best performance, the range for C_{SLEW} values are $10 \text{ nF} \leq C_{\text{SLEW}} \leq 20 \text{ nF}$ – please see typical characteristics for additional information. Capacitors used at the CAP pin should be rated at 10 V or higher. See equation for selecting capacitor and start-up slewing.
17	IOUT	Output	IOUT is the SLG59H1019V's power MOSFET load current monitor output. As an analog output current, this signal when applied to a ground-reference resistor generates a voltage proportional to the current through the n-channel MOSFET. The I_{OUT} transfer characteristic is typically 10 $\mu\text{A/A}$ with a voltage compliance range of $0.5 \text{ V} \leq V_{\text{IOUT}} \leq 4 \text{ V}$. Optimal I_{OUT} linearity is exhibited for $0.5 \text{ A} \leq I_{\text{DS}} \leq 5 \text{ A}$. In addition, it is recommended to bypass the IOUT pin to GND with a 0.18 nF capacitor.
18	RSET	Input	A 1%-tolerance, metal-film resistor between 18 k Ω and 91 k Ω sets the SLG59H1019V's active current limit. A 91 k Ω resistor sets the SLG59H1019V's active current limit to 1 A and a 18 k Ω resistor sets the active current limit to 5 A.

Ordering Information

Part Number	Type	Production Flow
SLG59H1019V	STQFN 18L FC	Industrial, -40 °C to 85 °C
SLG59H1019VTR	STQFN 18L FC (Tape and Reel)	Industrial, -40 °C to 85 °C



Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IN} to GND	Power Switch Input Voltage to GND	Continuous	-0.3	--	30	V
		Maximum pulsed V_{IN} , pulse width < 0.1s	--	--	32	V
V_{OUT} to GND	Power Switch Output Voltage to GND		-0.3	--	V_{IN}	V
ON, CAP, RSET, IOUT, and FAULT to GND	ON, CAP, RSET, IOUT, and FAULT Pin Voltages to GND		-0.3	--	7	V
T_S	Storage Temperature		-65	--	150	°C
ESD _{HBM}	ESD Protection	Human Body Model	2000	--	--	V
ESD _{CDM}	ESD Protection	Charged Device Model	500	--	--	V
MSL	Moisture Sensitivity Level		1			
θ_{JA}	Thermal Resistance	1.6 x 3.0 mm 18L STQFN; Determined with the device mounted onto a 1 in ² , 1 oz. copper pad of FR-4 material	--	40	--	°C/W
$T_{J,MAX}$	Maximum Junction Temperature		--	150	--	°C
MOSFET $I_{DS,CONT}$	Continuous Current from VIN to VOUT	$T_J < 150^\circ\text{C}$	--	--	5	A
MOSFET $I_{DS,PEAK}$	Peak Current from VIN to VOUT	Maximum pulsed switch current, pulse width < 1 ms, 1% duty cycle	--	--	6	A

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

4.5 V ≤ V_{IN} ≤ 25.2 V; C_{IN} = 47 μF, T_A = -40°C to 85°C, unless otherwise noted. Typical values are at T_A = 25°C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating Input Voltage		4.5	--	25.2	V
$V_{IN(UVLO)}$	V_{IN} Undervoltage Lockout Threshold	$V_{IN} \downarrow$	2.4	--	3.8	V
I_Q	Quiescent Supply Current	ON = HIGH; $I_{DS} = 0$ A	--	0.5	0.6	mA
I_{SHDN}	OFF Mode Supply Current	ON = LOW; $I_{DS} = 0$ A	--	1	3	μA
$R_{DS,ON}$	ON Resistance	$T_A = 25^\circ\text{C}$; $I_{DS} = 0.1$ A	--	13	14	mΩ
		$T_A = 85^\circ\text{C}$; $I_{DS} = 0.1$ A	--	17.2	19.2	mΩ
MOSFET I_{DS}	Current from VIN to VOUT	Continuous	--	--	5	A
I_{LIMIT}	Active Current Limit, I_{ACL}	$V_{OUT} > 0.5$ V; $R_{SET} = 30.1$ kΩ	2.7	3.19	3.4	A
	Short-circuit Current Limit, I_{SCL}	$V_{OUT} < 0.5$ V	--	0.5	-	A
T_{ACL}	Active Current Limit Response Time	$R_{SET} = 51.6$ kΩ	--	120	--	μs
R_{DSCHRG}	Output Discharge Resistance		650	750	900	Ω



Electrical Characteristics (continued)

4.5 V ≤ V_{IN} ≤ 25.2 V; C_{IN} = 47 μF, T_A = -40°C to 85°C, unless otherwise noted. Typical values are at T_A = 25°C

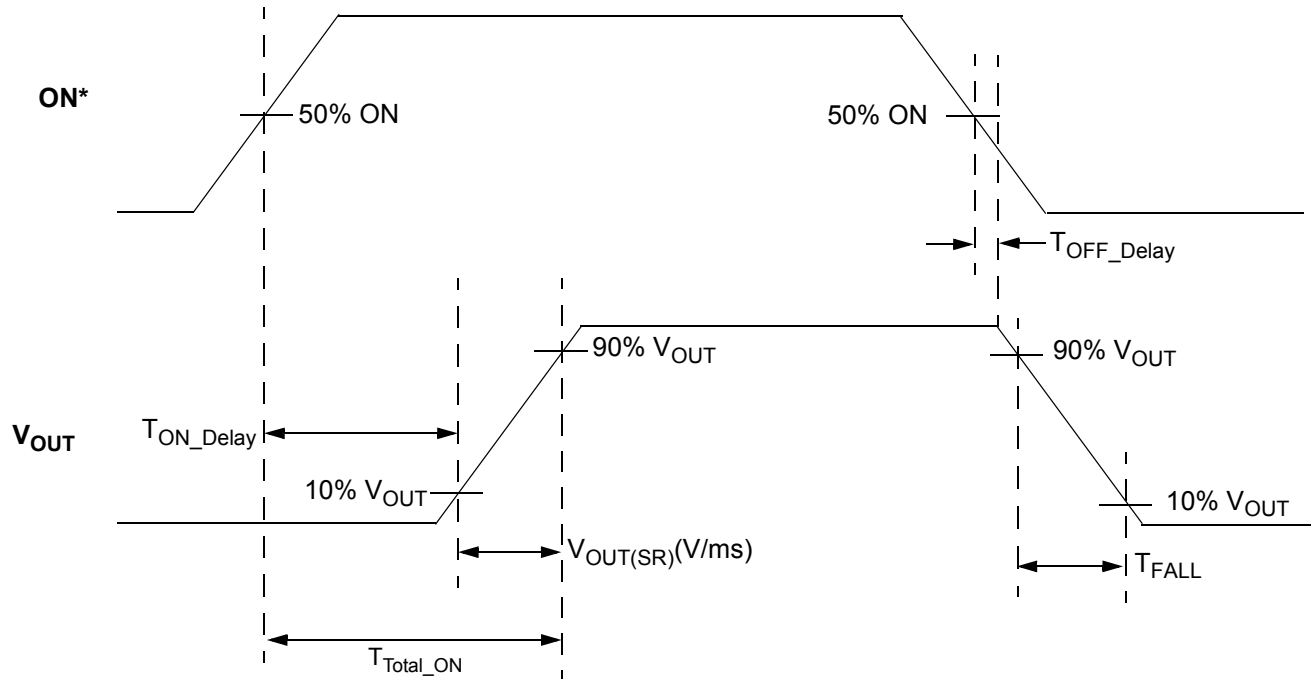
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
I _{OUT}	MOSFET Current Analog Monitor Output	I _{DS} = 1 A	9.3	10	11.1	μA
		I _{DS} = 3 A	29	30.3	32	μA
T _{IOUT}	I _{OUT} Response Time to Change in Main MOSFET Current	C _{IOUT} = 180 pF; Step load 0 to 2.4 A; 0% to 90% I _{OUT}	--	45	--	μs
C _{LOAD}	Output Load Capacitance	C _{LOAD} connected from V _{OUT} to GND	47	--	--	μF
T _{ON_Delay}	ON Delay Time	50% ON to 10% V _{OUT} ↑; V _{IN} = 4.5 V; C _{SLEW} = 10 nF; R _{LOAD} = 100 Ω, C _{LOAD} = 10 μF	300	400	600	μs
		50% ON to 10% V _{OUT} ↑; V _{IN} = 25.2 V; C _{SLEW} = 10 nF; R _{LOAD} = 100 Ω, C _{LOAD} = 10 μF	0.9	1.0	1.2	ms
T _{Total_ON}	Total Turn-on Time	50% ON to 90% V _{OUT} ↑	Set by External C _{SLEW} ¹			ms
		50% ON to 90% V _{OUT} ↑; V _{IN} = 4.5 V; C _{SLEW} = 10 nF; R _{LOAD} = 100 Ω, C _{LOAD} = 10 μF	1.8	1.9	2.1	ms
		50% ON to 90% V _{OUT} ↑; V _{IN} = 25.2 V; C _{SLEW} = 10 nF; R _{LOAD} = 100 Ω, C _{LOAD} = 10 μF	8.9	9.0	9.2	ms
V _{OUT(SR)}	V _{OUT} Slew rate	50% ON to 90% V _{OUT} ↑	Set by External C _{SLEW} ¹			V/ms
		10% to 90% V _{OUT} ↑; V _{IN} = 4.5 to 25.2 V; C _{SLEW} = 10 nF; R _{LOAD} = 100 Ω, C _{LOAD} = 10 μF	3	3.2	3.5	V/ms
T _{OFF_Delay}	OFF Delay Time	50% ON to V _{OUT} ↓; R _{LOAD} = 100 Ω, No C _{LOAD}	--	15	--	μs
T _{FALL}	V _{OUT} Fall Time	90% V _{OUT} to 10% V _{OUT} ↓; ON = HIGH-to-LOW; V _{IN} = 4.5 V to 25.2 V; R _{LOAD} = 100 Ω, No C _{LOAD}	10	12	18	μs
T _{FAULT_LOW}	FAULT Assertion Time	Abnormal Step Load Current event to FAULT ↓; I _{ACL} = 1 A; V _{IN} = 25.2 V; R _{SET} = 91 kΩ; switch in 20 Ω load	--	80	--	μs
T _{FAULT_HIGH}	FAULT De-assertion Time	Delay to FAULT ↑ after fault condition is removed; I _{ACL} = 1 A; V _{IN} = 25.2 V; R _{SET} = 91 kΩ; switch out 20 Ω load	--	180	--	μs
FAULT _{VOL}	FAULT Output Low Voltage	I _{FAULT} = 1 mA	--	0.2	--	V
ON_V _{IH}	ON Pin Input High Voltage	Internal 1 MΩ ±20% from ON Pin to GND	0.9	--	5	V
ON_V _{IL}	ON Pin Input Low Voltage		-0.3	0	0.3	V
I _{ON(Leakage)}	ON Pin Leakage Current	0.9 V ≤ ON ≤ 5 V or ON = GND	--	--	2	μA
THERM _{ON}	Thermal Protection Shutdown Threshold		--	145	--	°C
THERM _{OFF}	Thermal Protection Restart Threshold		--	120	--	°C

Notes:

1. Refer to typical Timing Parameter vs. C_{SLEW} performance charts for additional information when available.



T_{Total_ON} , T_{ON_Delay} and Slew Rate Measurement Timing Details

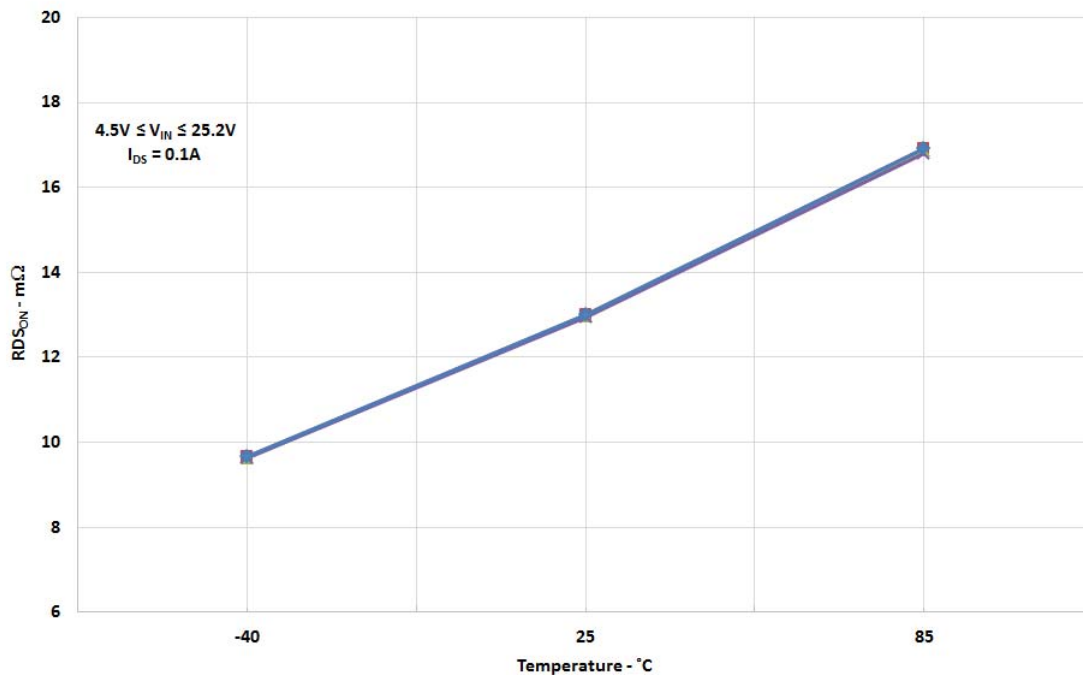


* Rise and Fall times of the ON signal are 100 ns

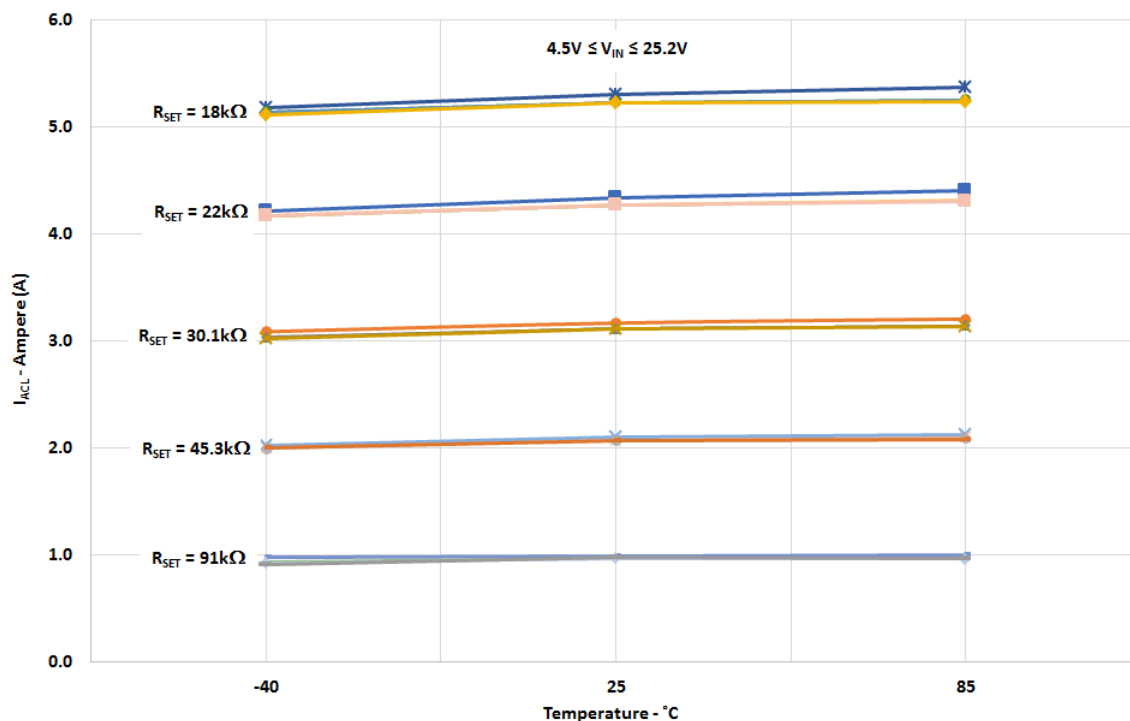


Typical Performance Characteristics

$R_{DS(on)}$ vs. Temperature and V_{IN}

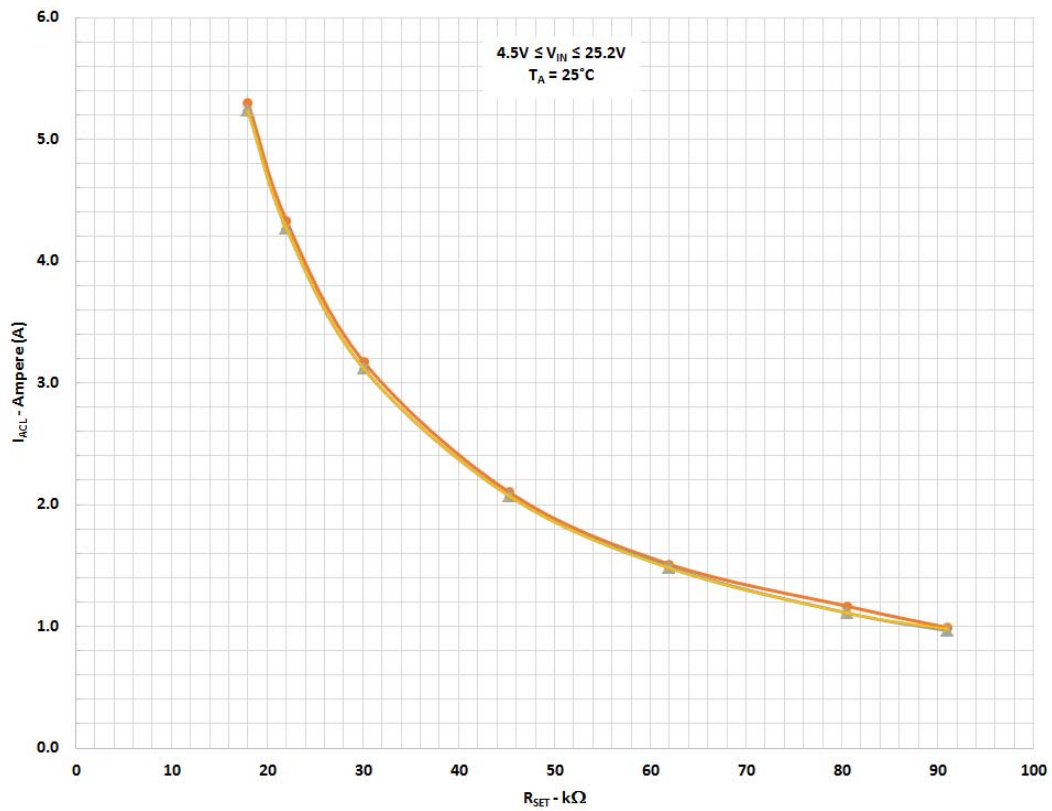


I_{ACL} vs. Temperature and R_{SET}

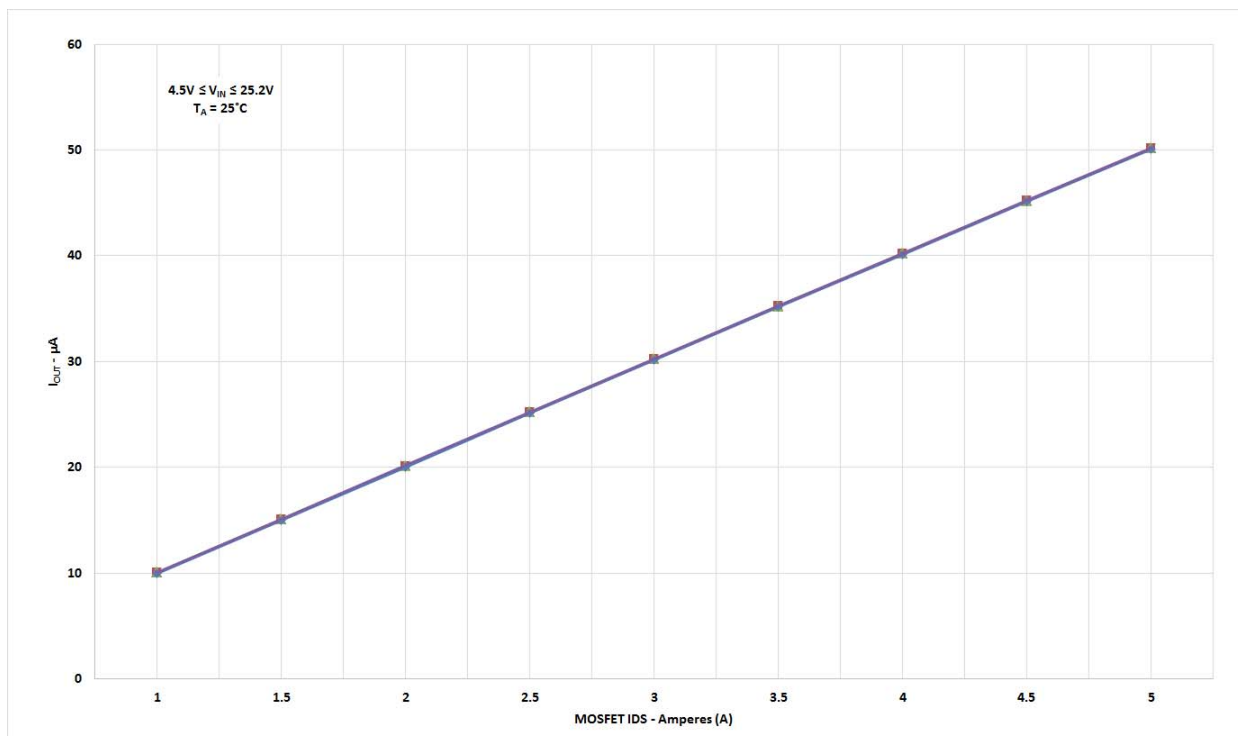




I_{ACL} vs. R_{SET} and Temperature

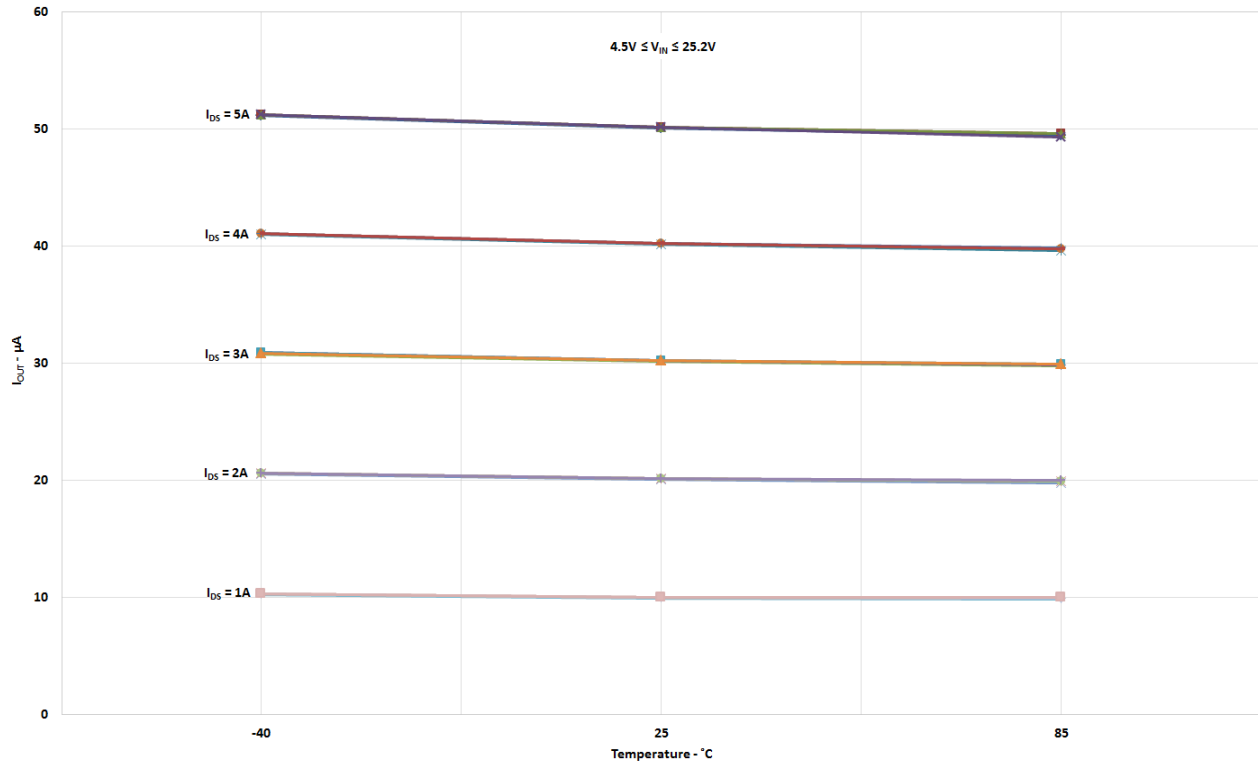


I_{OUT} vs. MOSFET I_{DS} and V_{IN}

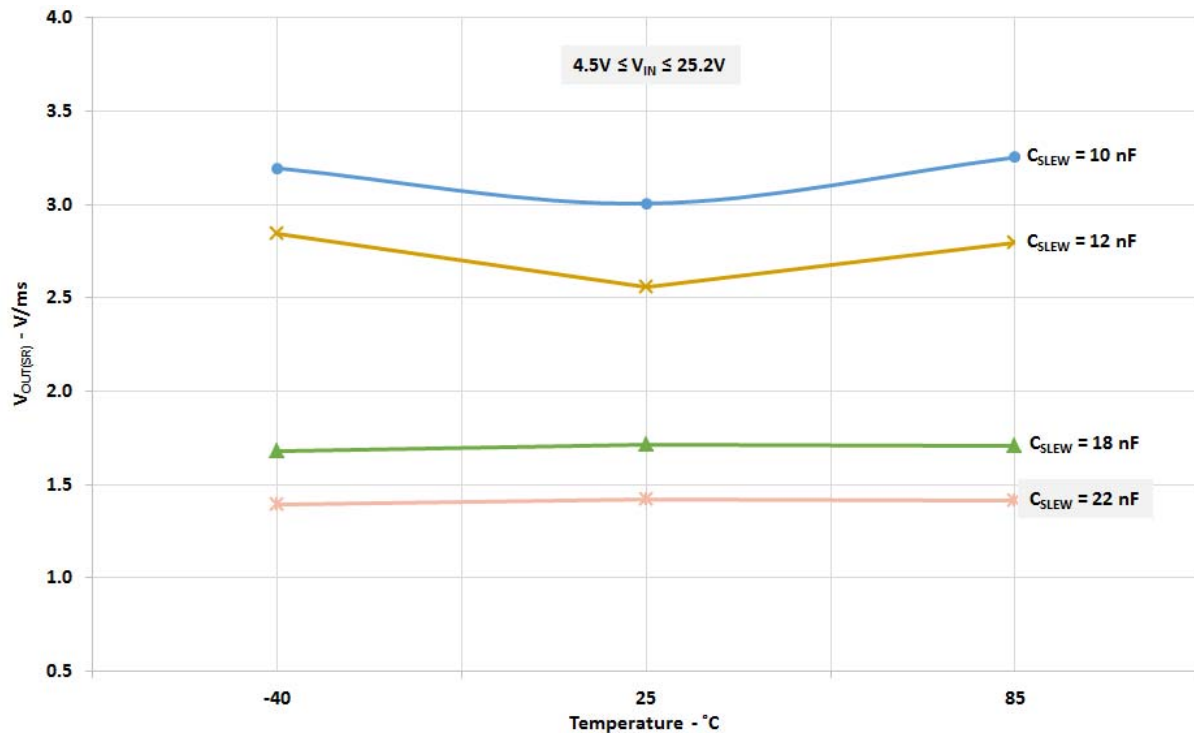




I_{OUT} vs. Temperature and MOSFET I_{DS}

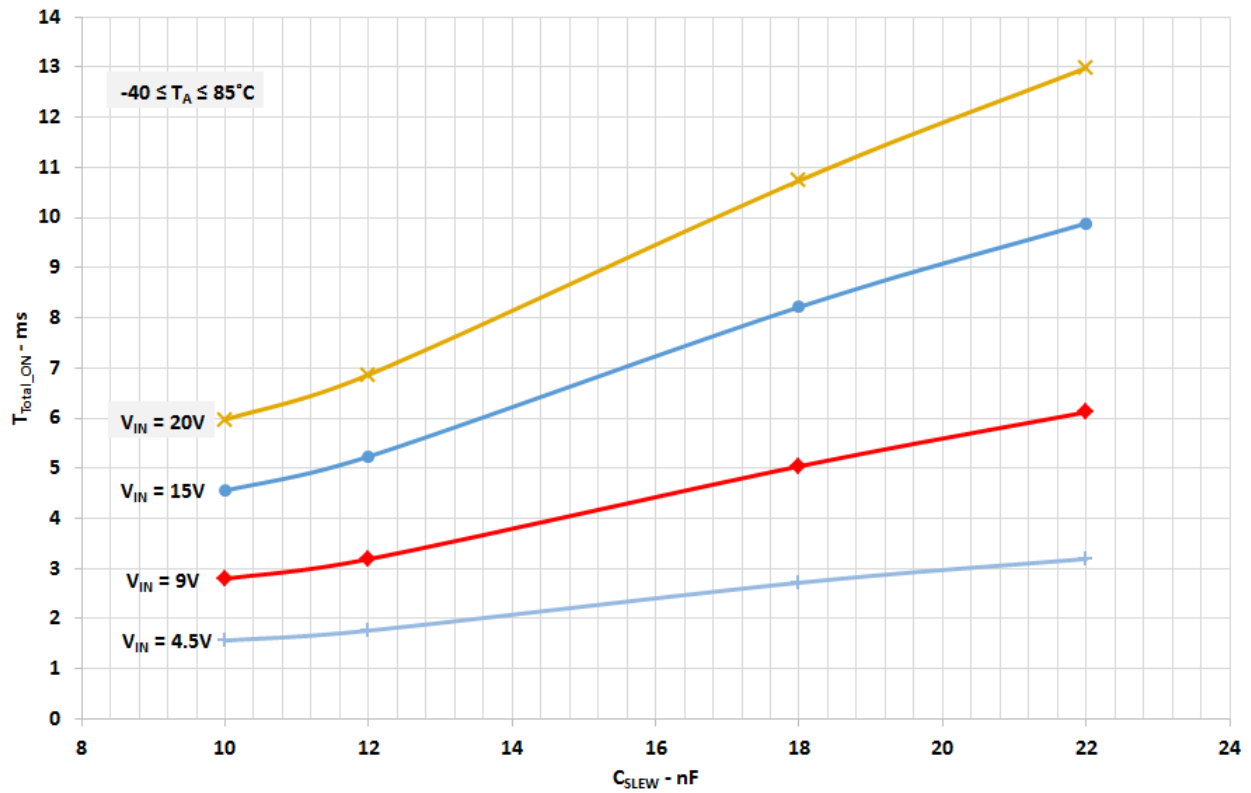


V_{OUT} Slew Rate vs. Temperature, V_{IN} , and C_{SLEW}



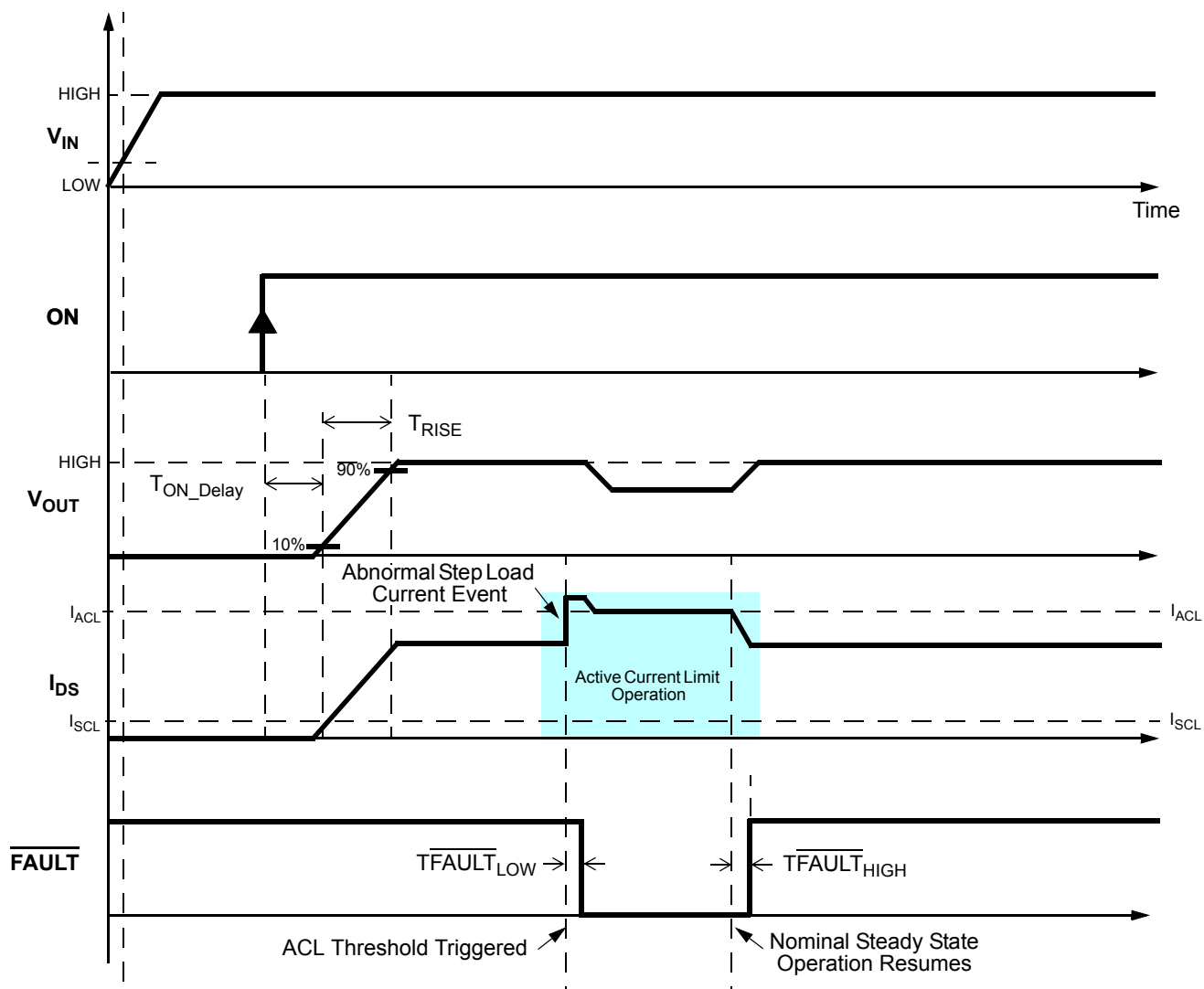


$T_{\text{Total_ON}}$ vs. C_{SLEW} , V_{IN} , and Temperature



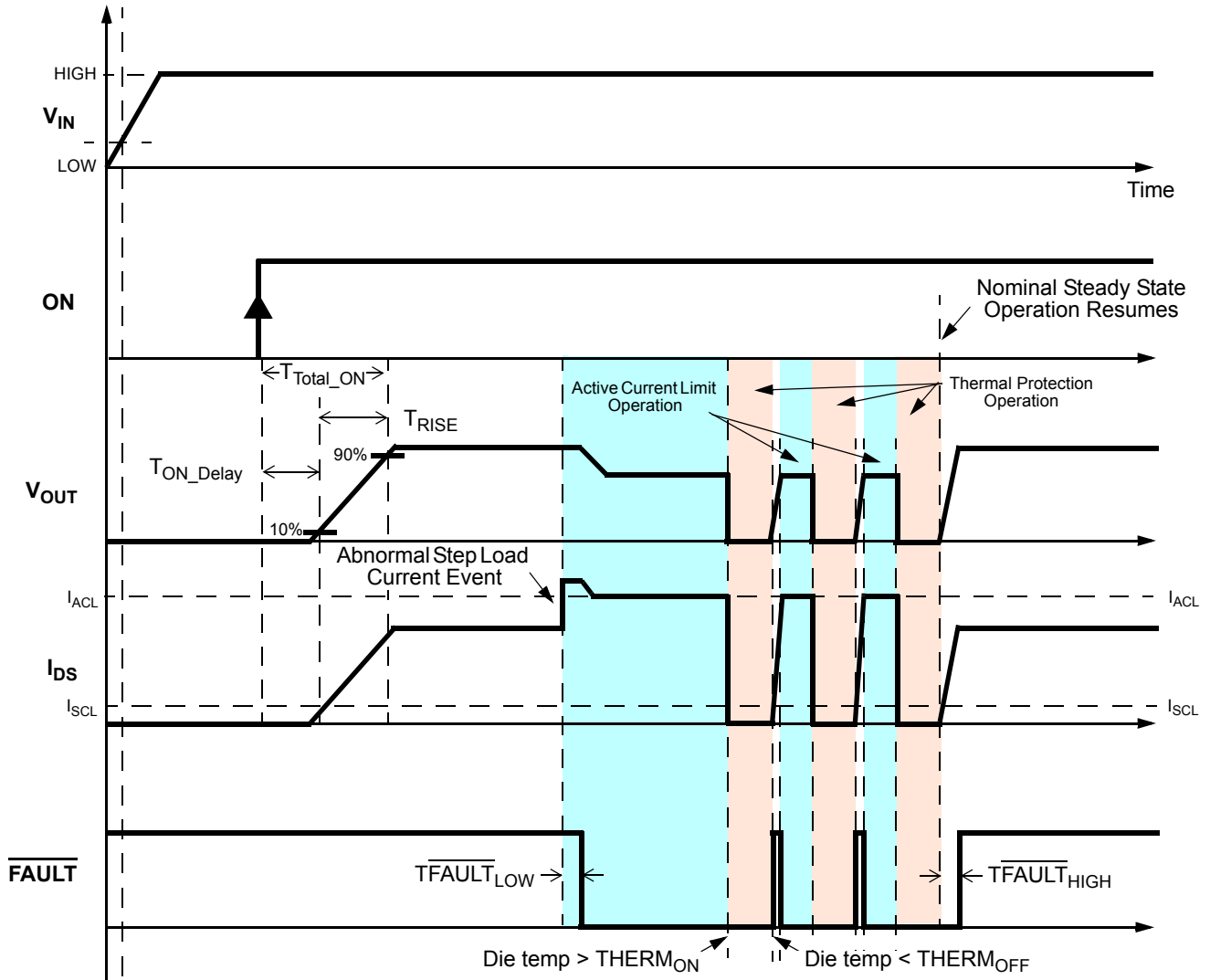


Timing Diagram - Basic Operation including Active Current Limit Protection



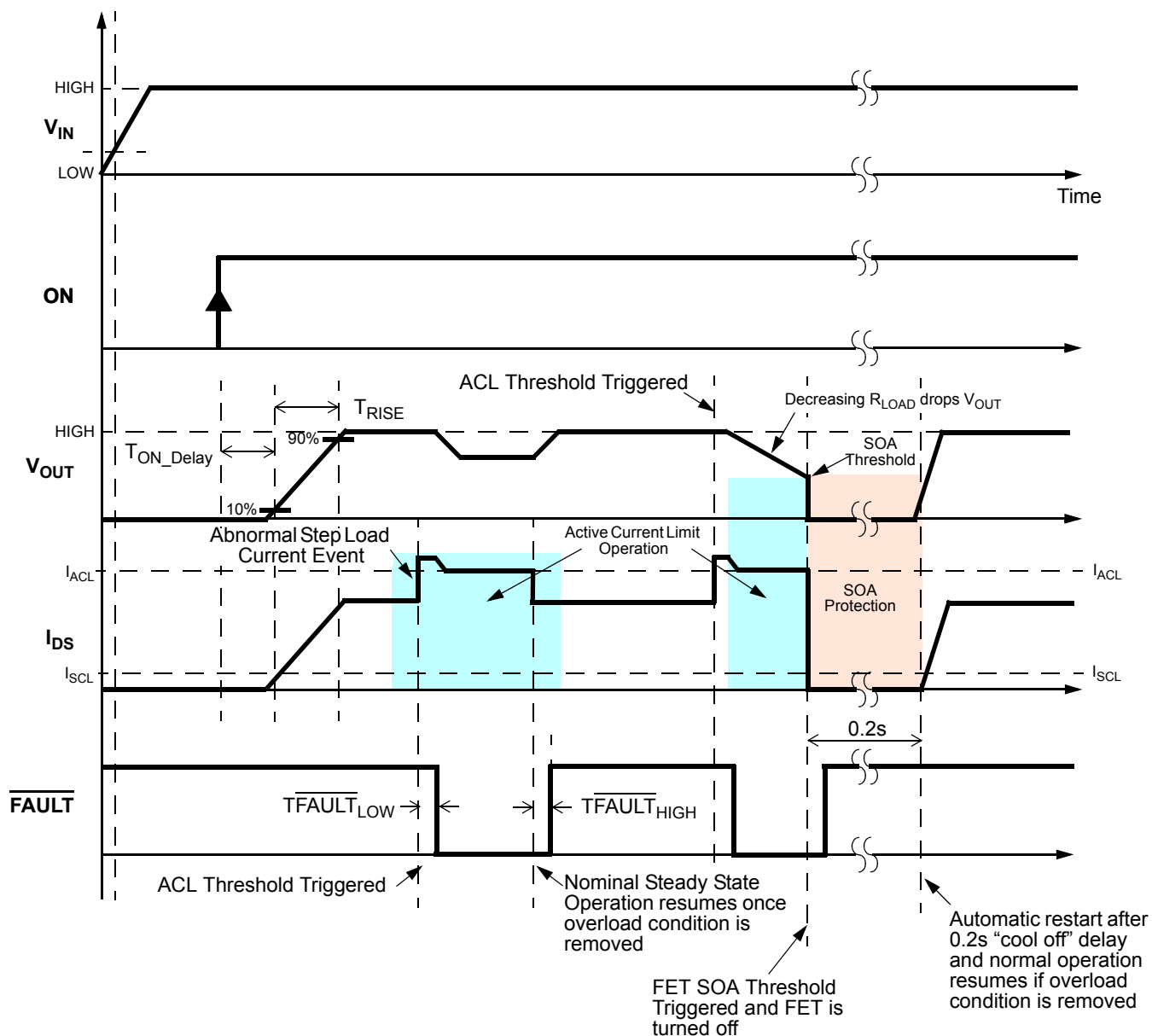


Timing Diagram - Active Current Limit & Thermal Protection Operation





Timing Diagram - Basic Operation including Active Current + Internal FET SOA Protection





SLG59H1019V Application Diagram

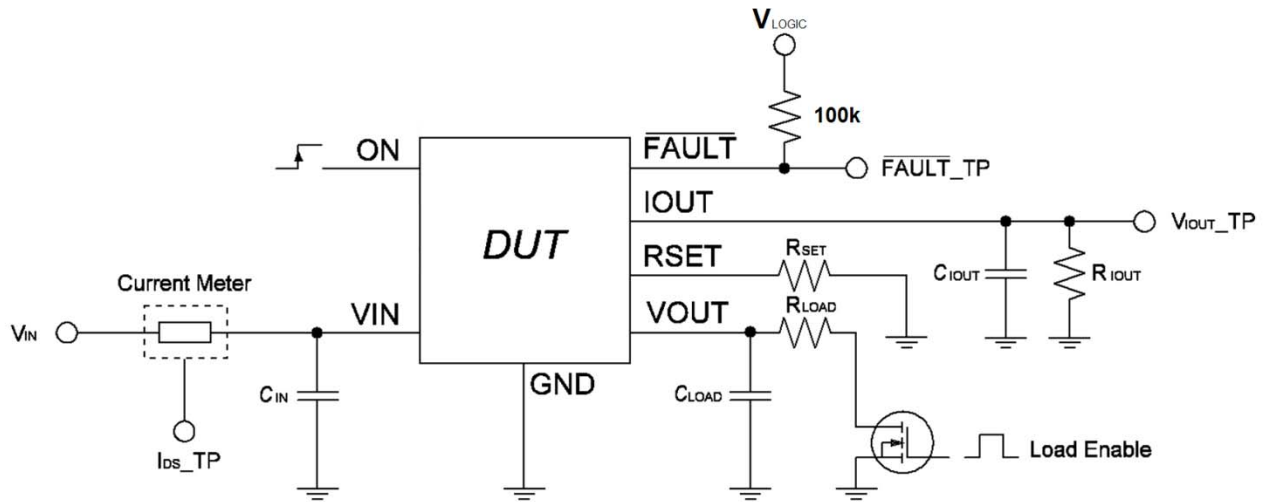


Figure 1. Test setup Application Diagram

Typical Turn-on Waveforms

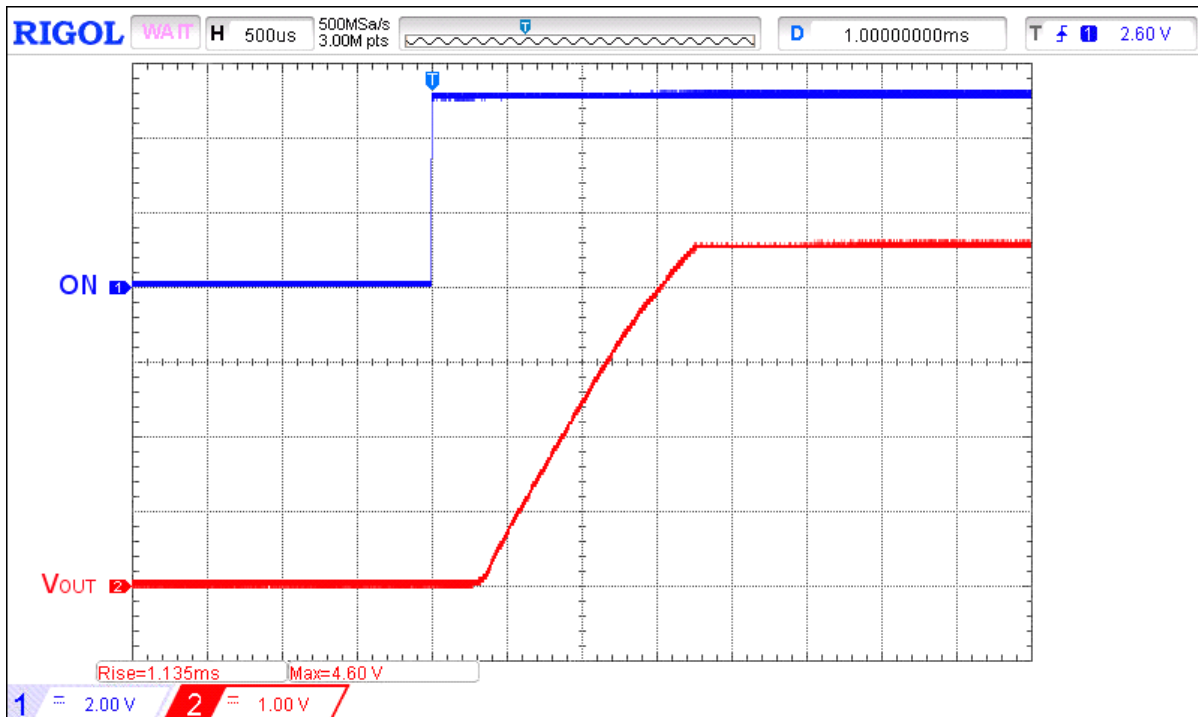


Figure 2. Typical Turn ON operation waveform for $V_{IN} = 4.5\text{ V}$, $C_{SLEW} = 10\text{ nF}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{LOAD} = 100\text{ }\Omega$

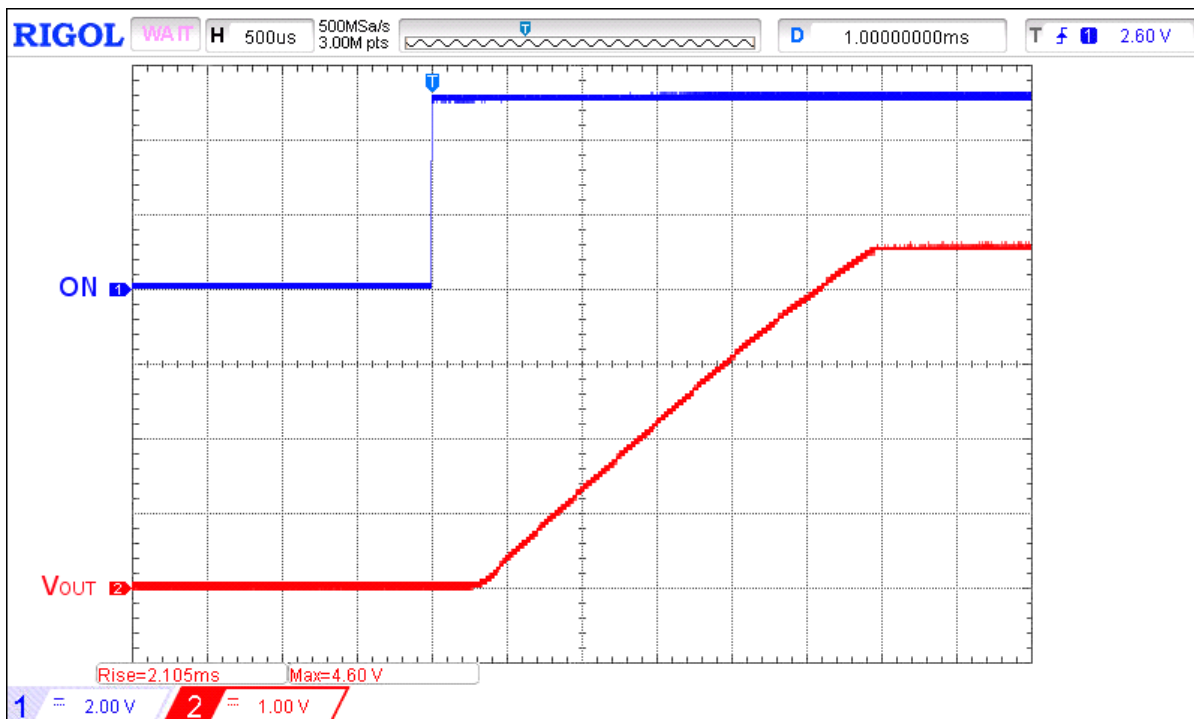


Figure 3. Typical Turn ON operation waveform for $V_{IN} = 4.5\text{ V}$, $C_{SLEW} = 18\text{ nF}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{LOAD} = 100\text{ }\Omega$

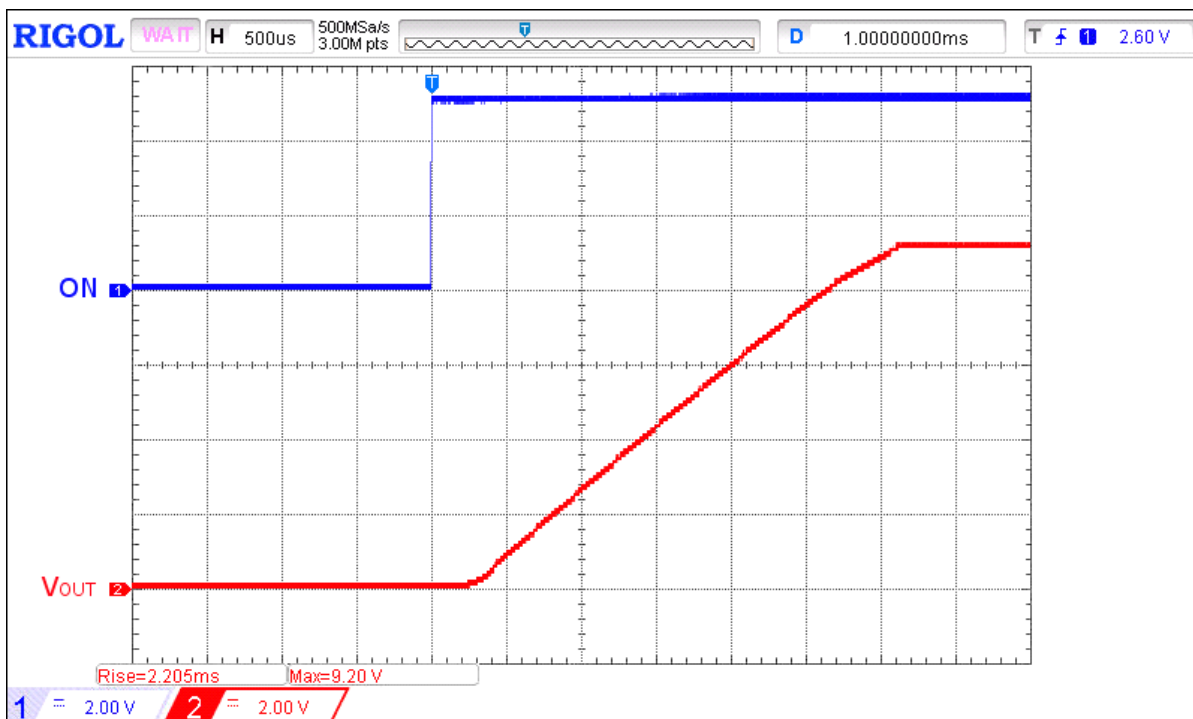


Figure 4. Typical Turn ON operation waveform for $V_{IN} = 9\text{ V}$, $C_{SLEW} = 10\text{ nF}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{LOAD} = 100\text{ }\Omega$

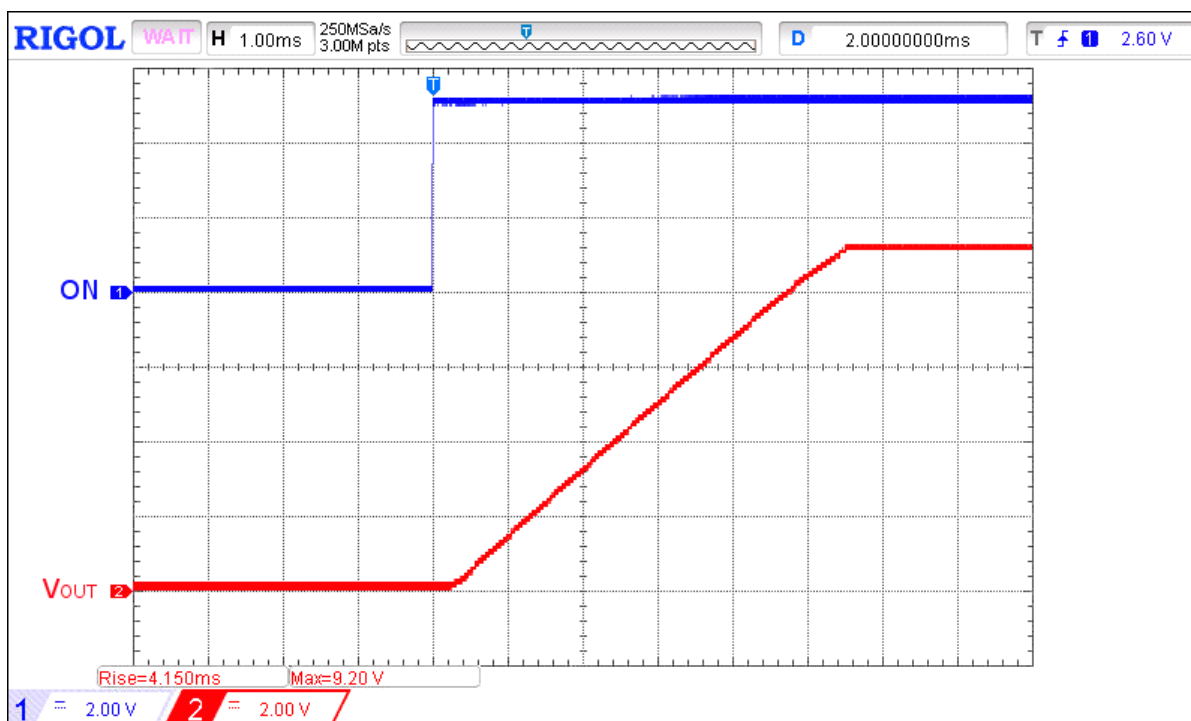


Figure 5. Typical Turn ON operation waveform for $V_{IN} = 9\text{ V}$, $C_{SLEW} = 18\text{ nF}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{LOAD} = 100\text{ }\Omega$

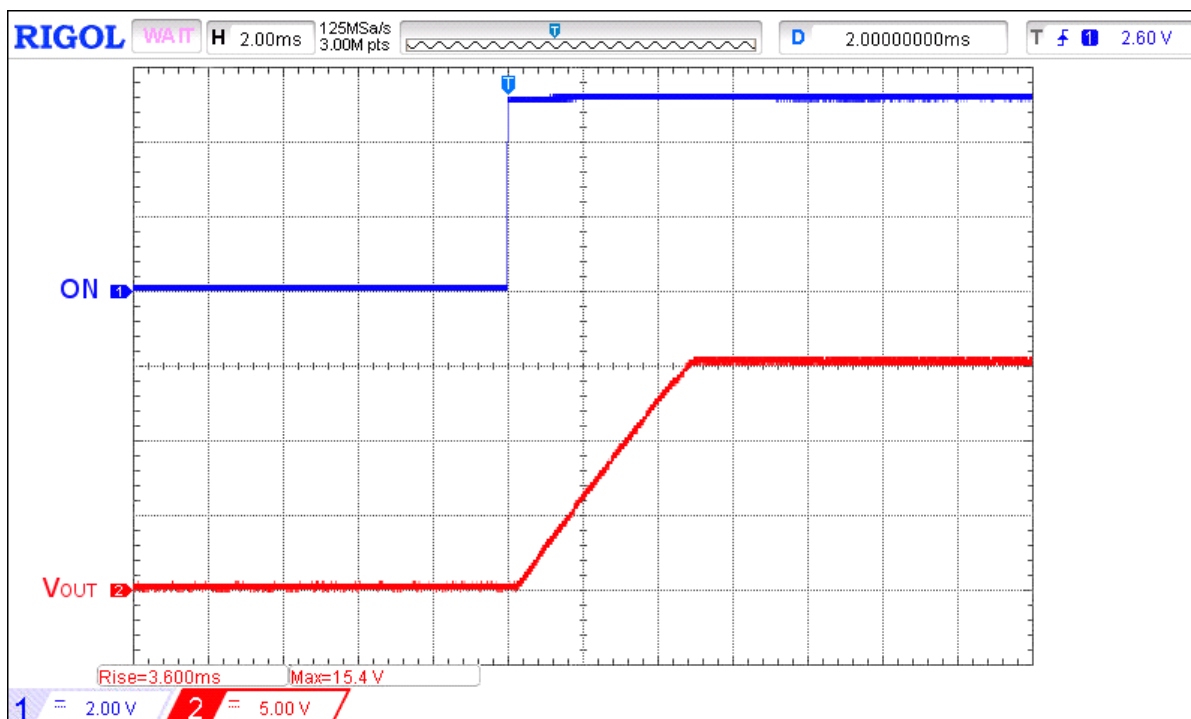


Figure 6. Typical Turn ON operation waveform for $V_{IN} = 15\text{ V}$, $C_{SLEW} = 10\text{ nF}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{LOAD} = 100\text{ }\Omega$

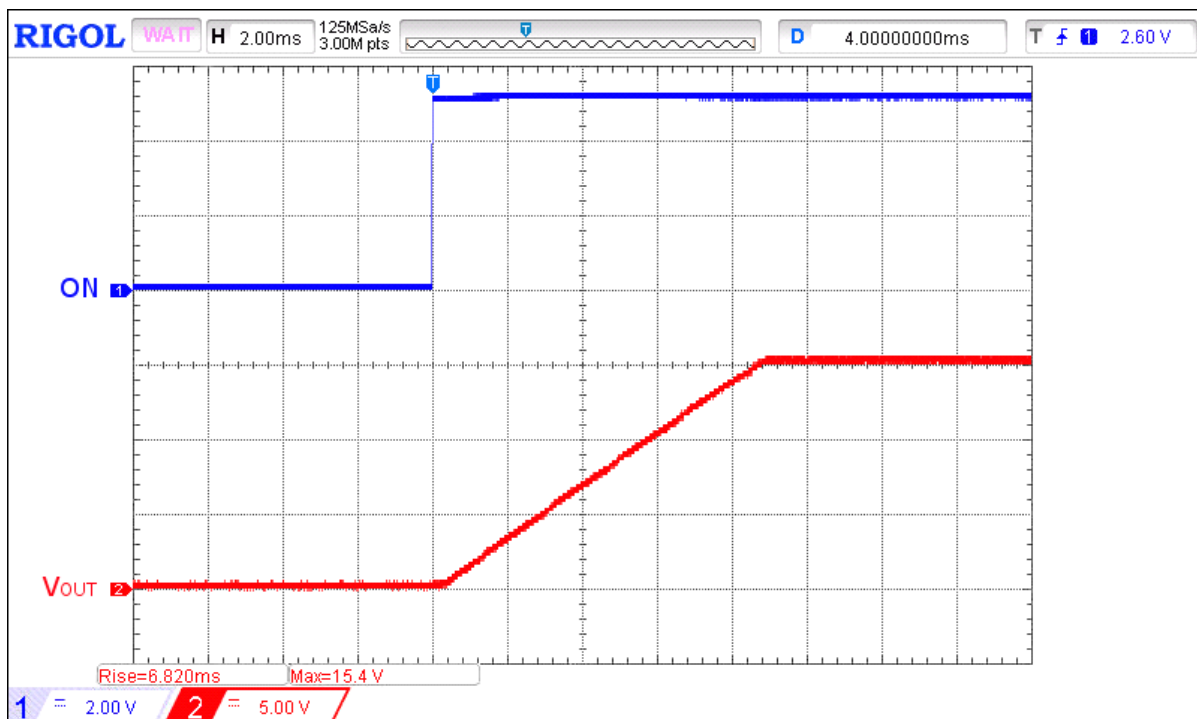


Figure 7. Typical Turn ON operation waveform for $V_{IN} = 15\text{ V}$, $C_{SLEW} = 18\text{ nF}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{LOAD} = 100\text{ }\Omega$

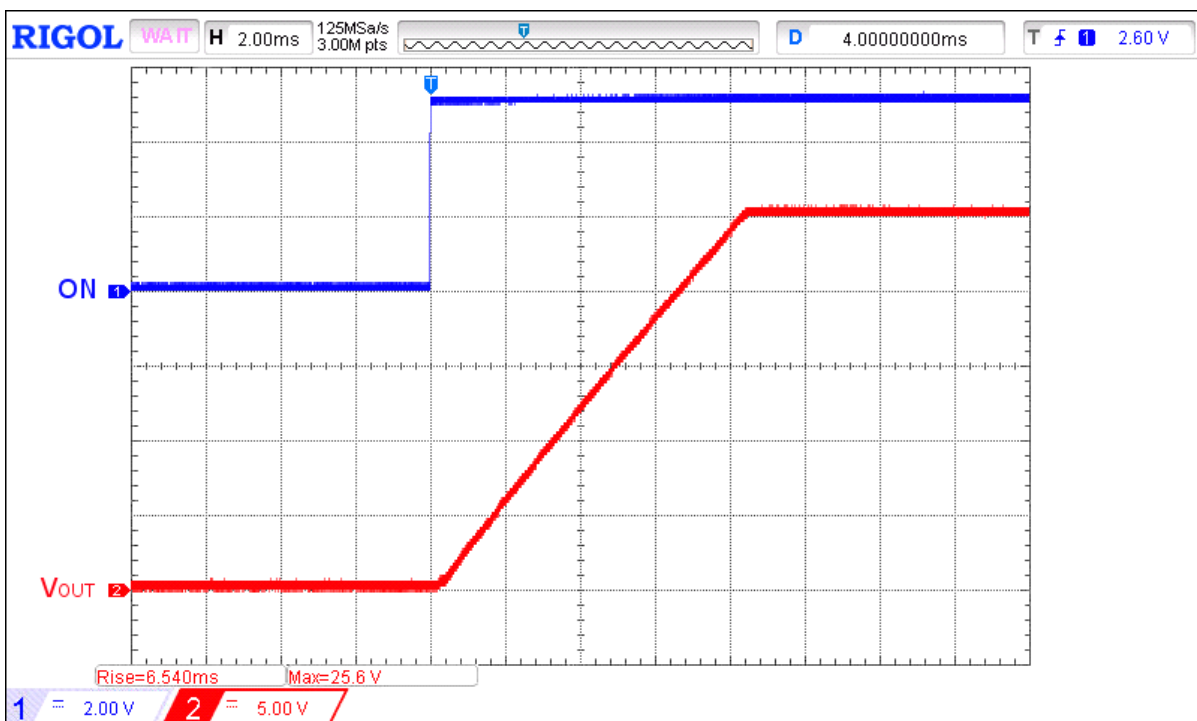


Figure 8. Typical Turn ON operation waveform for $V_{IN} = 25.2\text{ V}$, $C_{SLEW} = 10\text{ nF}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{LOAD} = 100\text{ }\Omega$

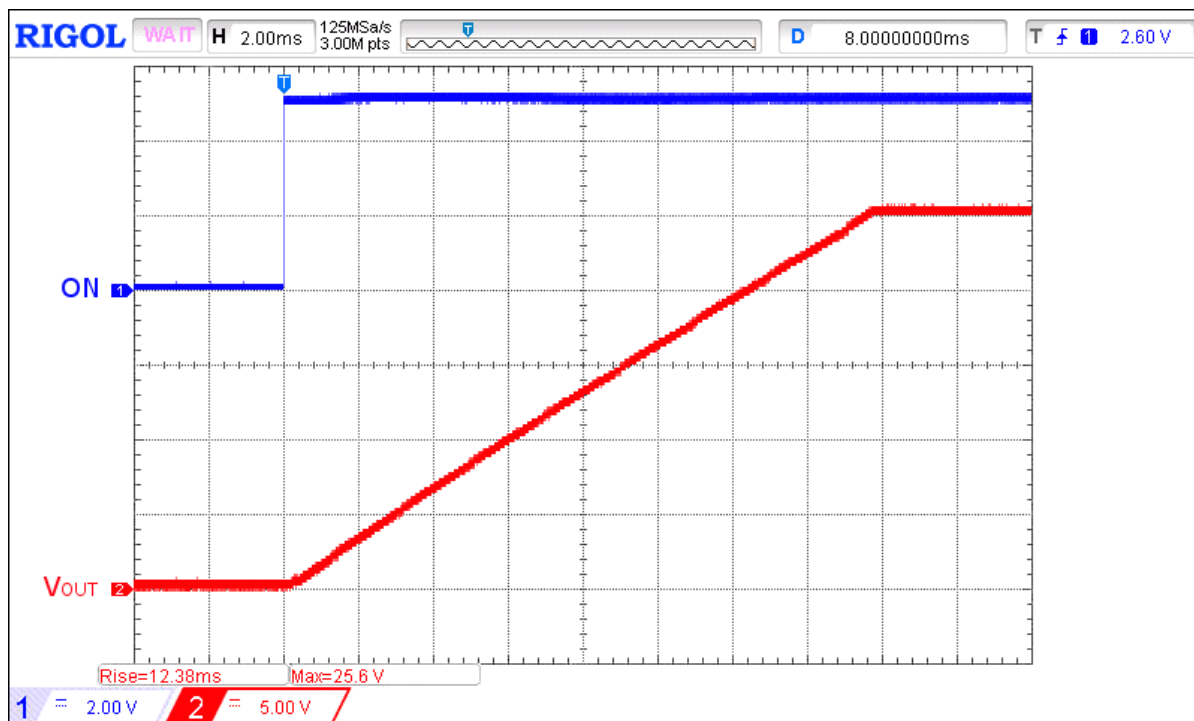


Figure 9. Typical Turn ON operation waveform for $V_{IN} = 25.2\text{ V}$, $C_{SLEW} = 18\text{ nF}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{LOAD} = 100\text{ }\Omega$

Typical Turn-off Waveforms

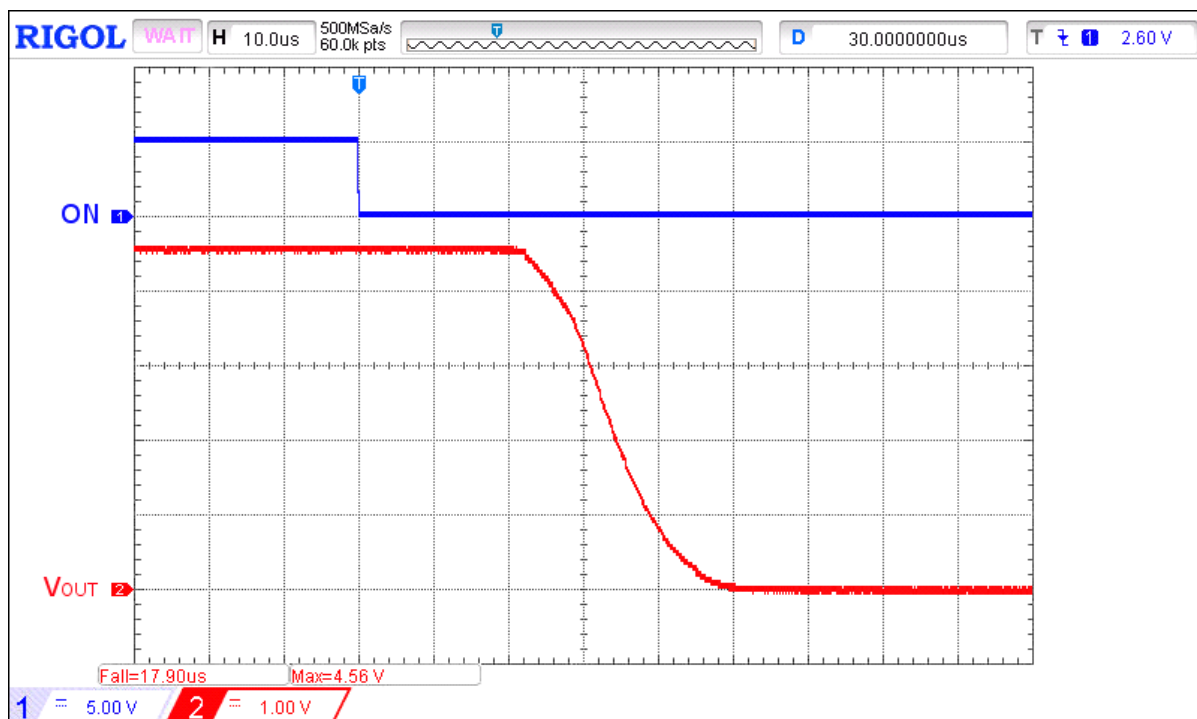


Figure 10. Typical Turn OFF operation waveform for $V_{IN} = 4.5\text{ V}$, $C_{SLEW} = 10\text{ nF}$, no C_{LOAD} , $R_{LOAD} = 100\text{ }\Omega$

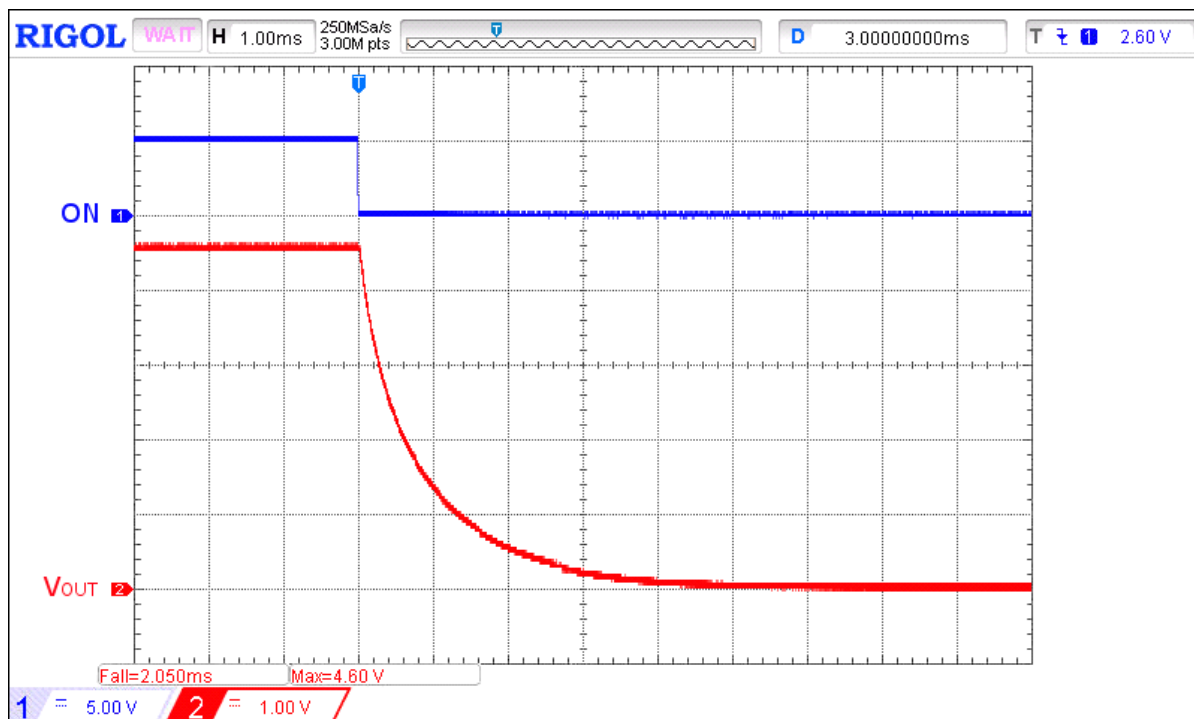


Figure 11. Typical Turn OFF operation waveform for $V_{IN} = 4.5\text{ V}$, $C_{SLEW} = 10\text{ nF}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{LOAD} = 100\text{ }\Omega$

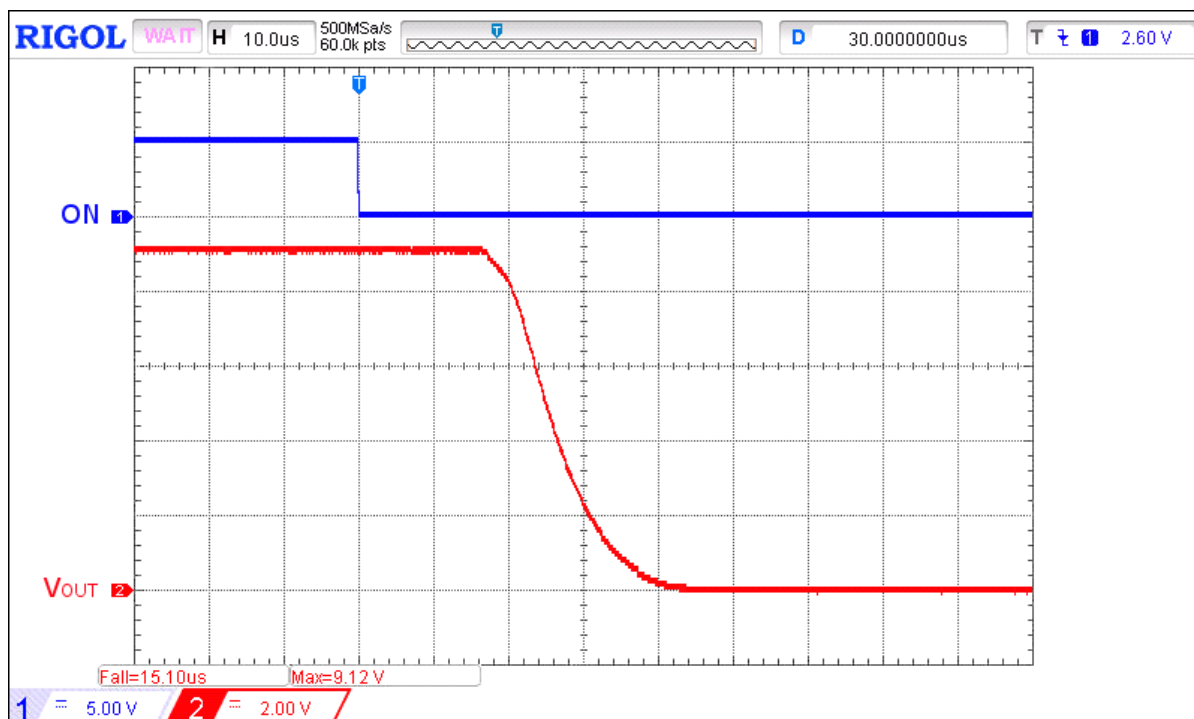


Figure 12. Typical Turn OFF operation waveform for $V_{IN} = 9\text{ V}$, $C_{SLEW} = 10\text{ nF}$, no C_{LOAD} , $R_{LOAD} = 100\text{ }\Omega$

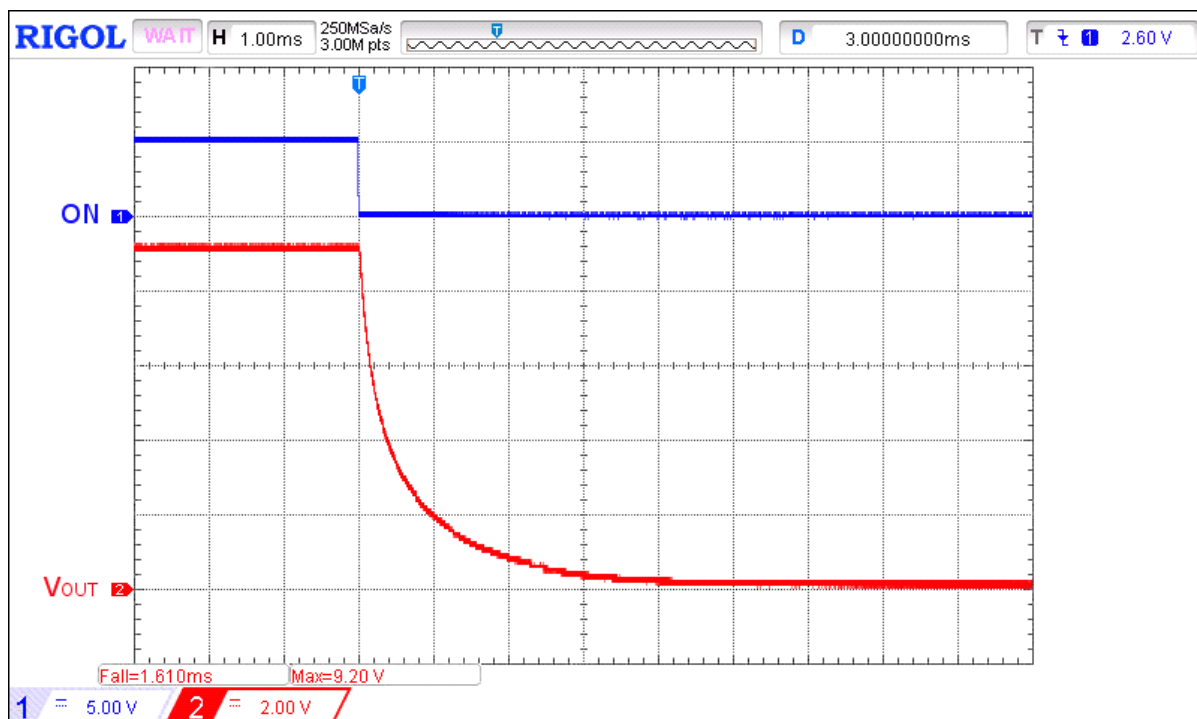


Figure 13. Typical Turn OFF operation waveform for $V_{IN} = 9\text{ V}$, $C_{SLEW} = 10\text{ nF}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{LOAD} = 100\text{ }\Omega$

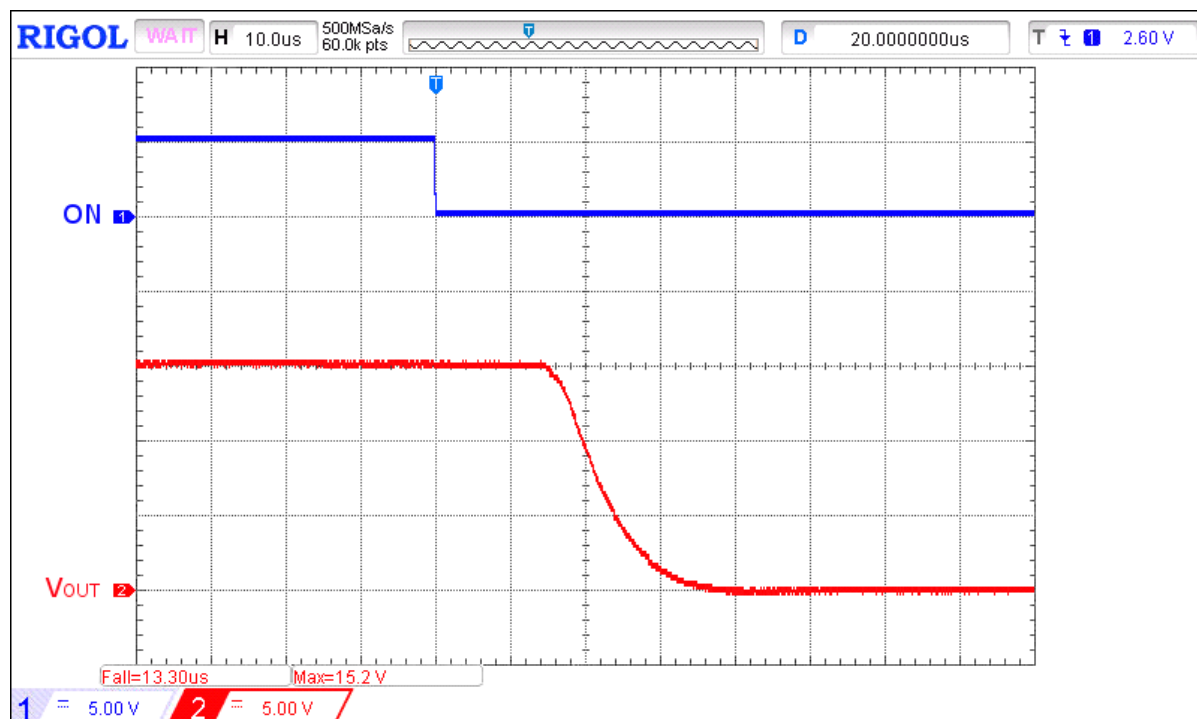


Figure 14. Typical Turn OFF operation waveform for $V_{IN} = 15\text{ V}$, $C_{SLEW} = 10\text{ nF}$, no C_{LOAD} , $R_{LOAD} = 100\text{ }\Omega$

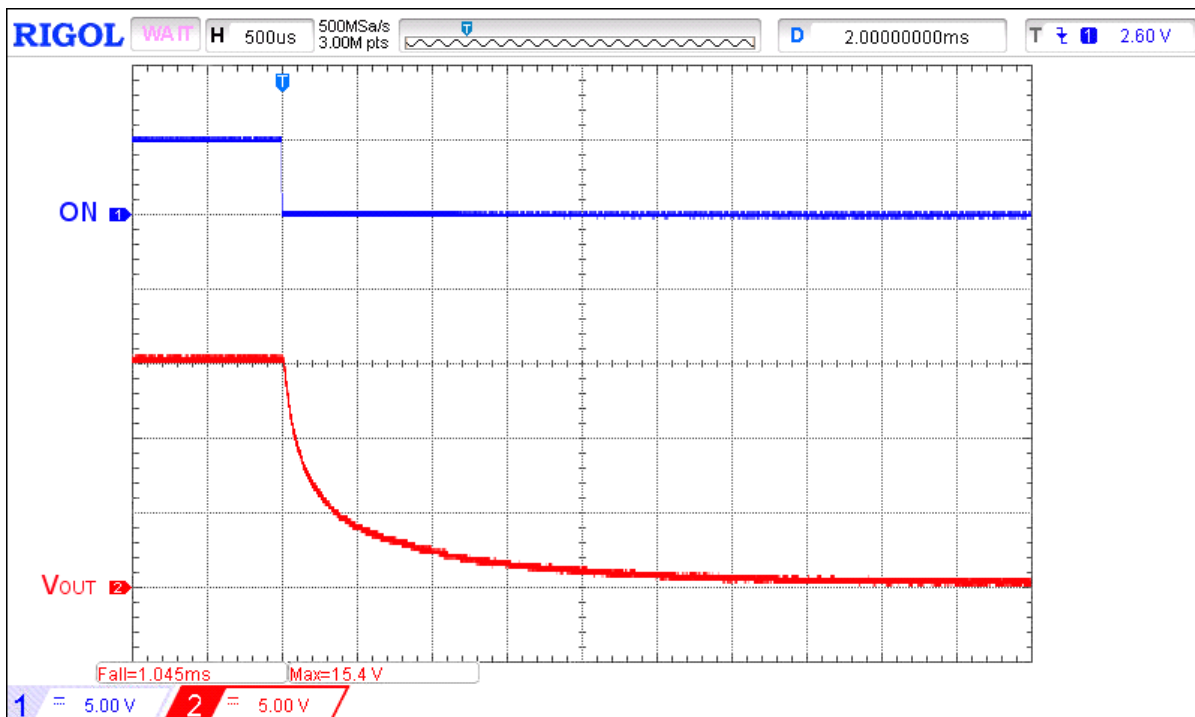


Figure 15. Typical Turn OFF operation waveform for $V_{IN} = 15\text{ V}$, $C_{SLEW} = 10\text{ nF}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{LOAD} = 100\text{ }\Omega$

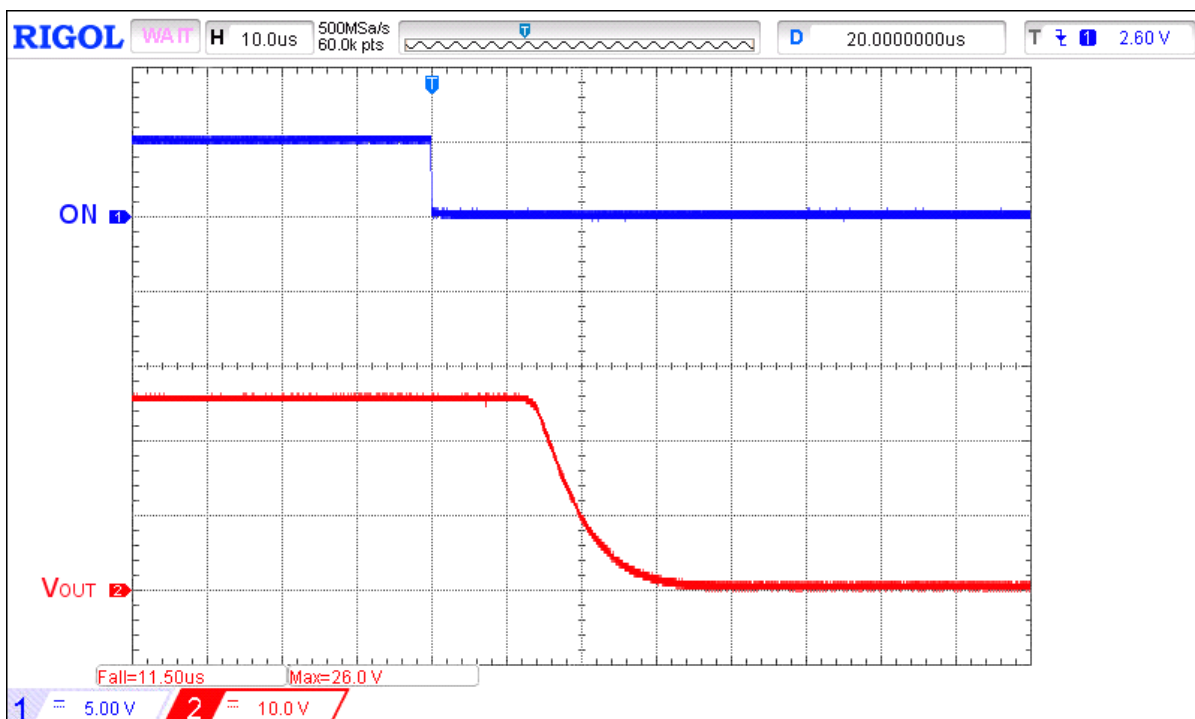


Figure 16. Typical Turn OFF operation waveform for $V_{IN} = 25.2\text{ V}$, $C_{SLEW} = 10\text{ nF}$, no C_{LOAD} , $R_{LOAD} = 100\text{ }\Omega$

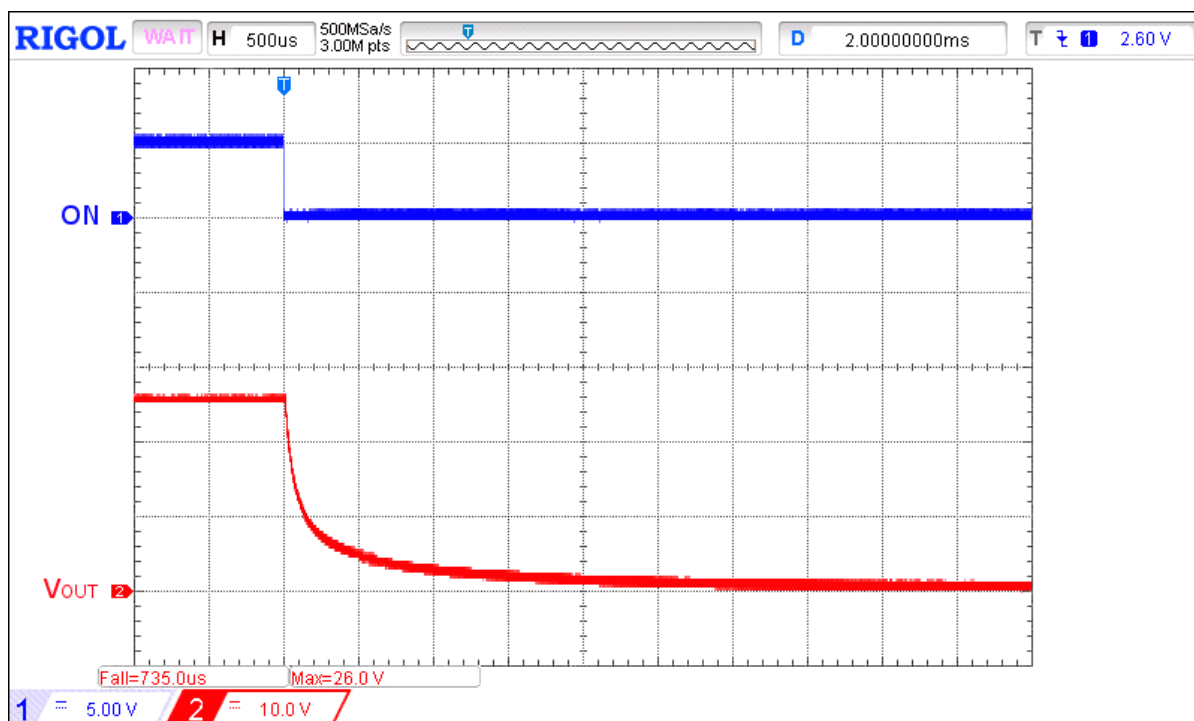


Figure 17. Typical Turn OFF operation waveform for $V_{IN} = 25.2 \text{ V}$, $C_{SLEW} = 10 \text{ nF}$, $C_{LOAD} = 10 \text{ } \mu\text{F}$, $R_{LOAD} = 100 \text{ } \Omega$

Typical ACL Operation Waveforms

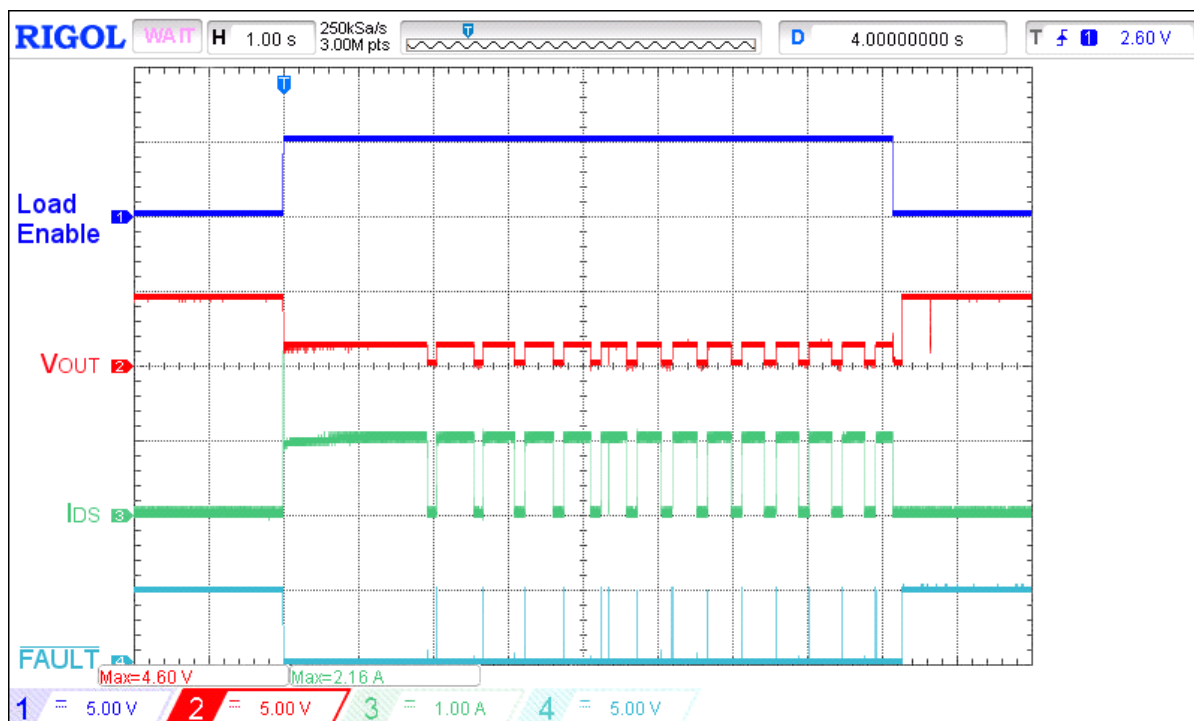


Figure 18. Typical ACL operation waveform for $V_{IN} = 4.5 \text{ V}$, $C_{LOAD} = 10 \text{ } \mu\text{F}$, $I_{ACL} = 1 \text{ A}$, $R_{SET} = 91 \text{ k}\Omega$

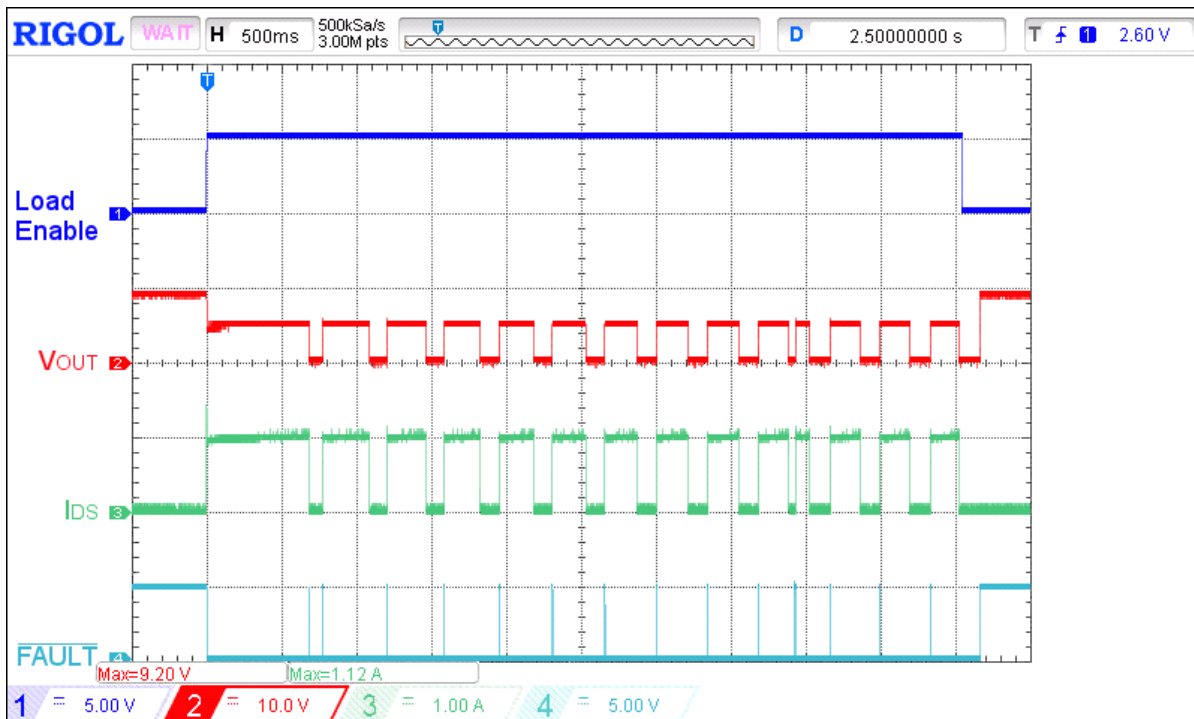


Figure 19. Typical ACL operation waveform for $V_{IN} = 9\text{ V}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $I_{ACL} = 1\text{ A}$, $R_{SET} = 91\text{ k}\Omega$

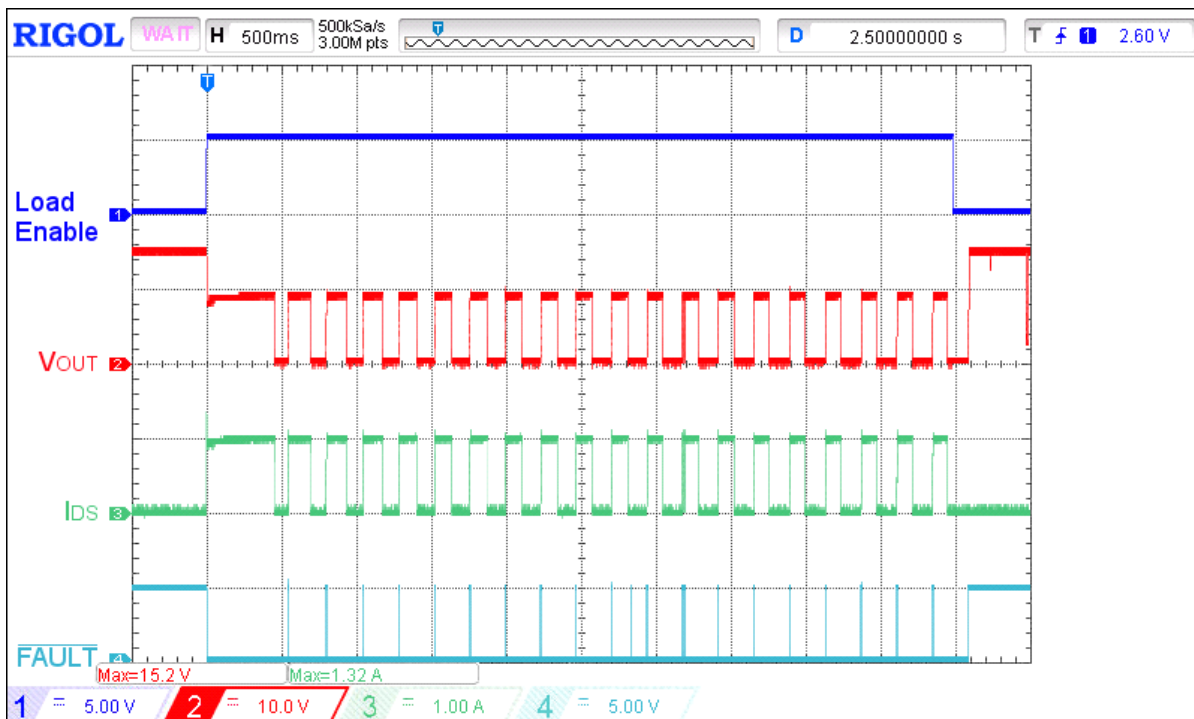


Figure 20. Typical ACL operation waveform for $V_{IN} = 15\text{ V}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $I_{ACL} = 1\text{ A}$, $R_{SET} = 91\text{ k}\Omega$

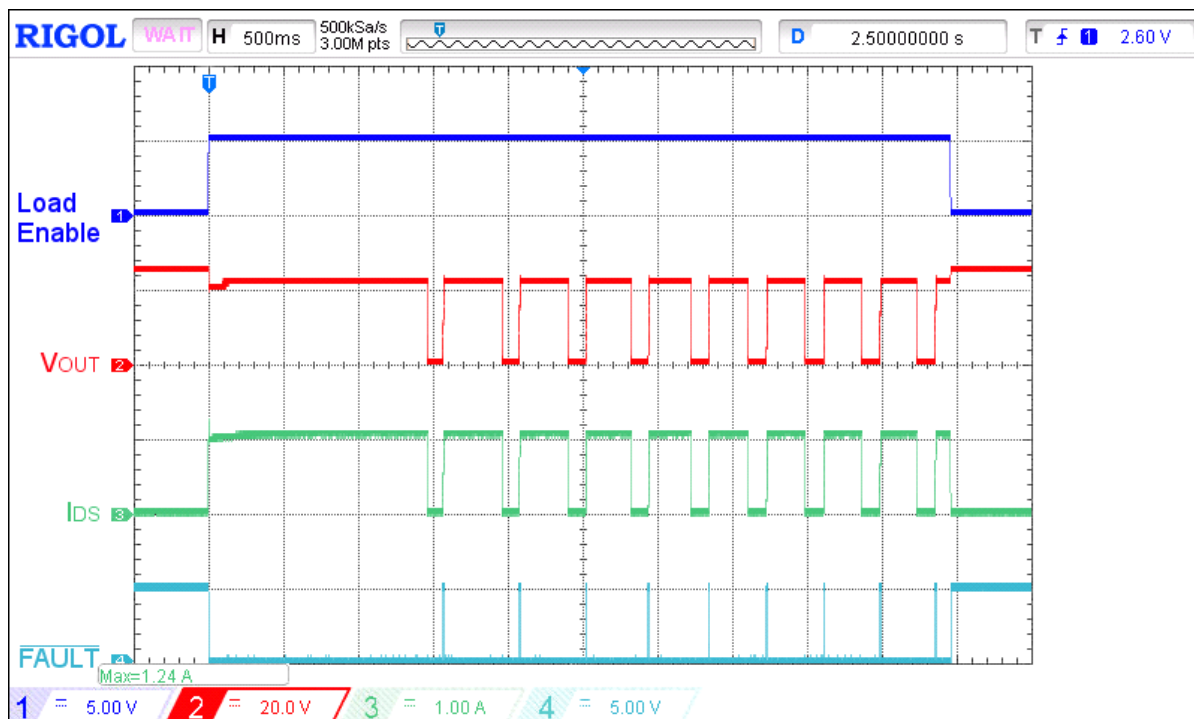


Figure 21. Typical ACL operation waveform for $V_{IN} = 25.2\text{ V}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $I_{ACL} = 1\text{ A}$, $R_{SET} = 91\text{ k}\Omega$

Typical FAULT Operation Waveforms

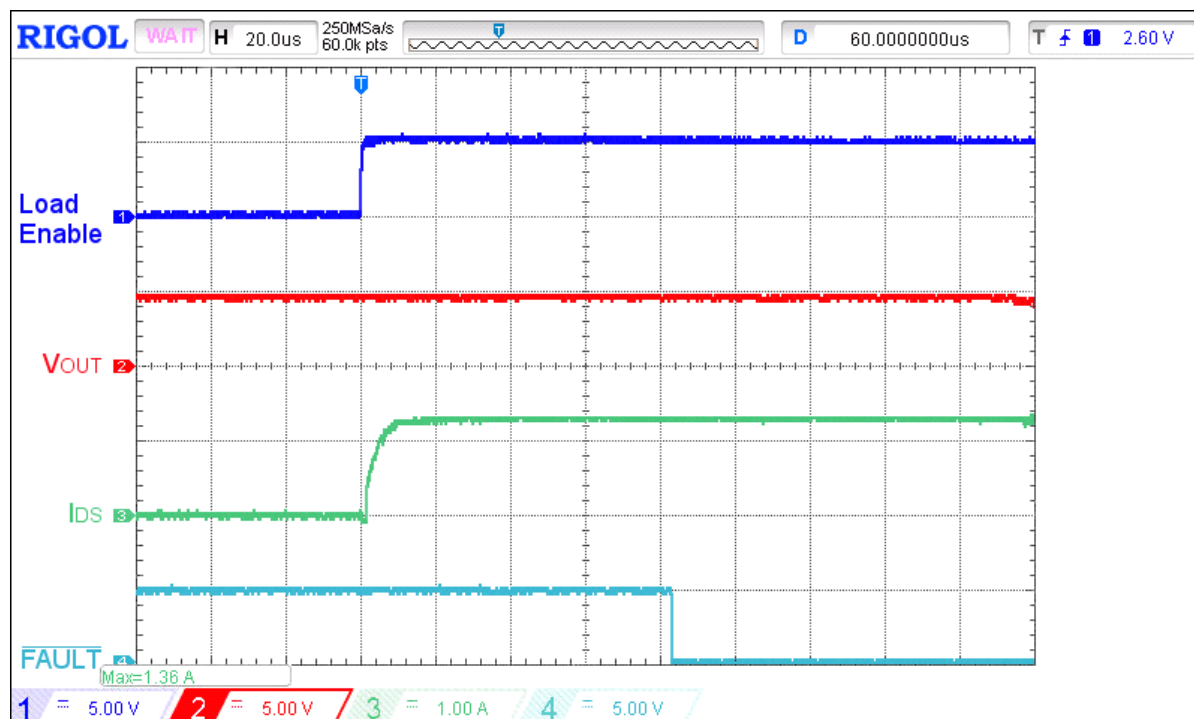


Figure 22. Typical FAULT assertion waveform for $V_{IN} = 4.5\text{ V}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $I_{ACL} = 1\text{ A}$, $R_{SET} = 91\text{ k}\Omega$, switch on $3.3\text{ }\Omega$ load

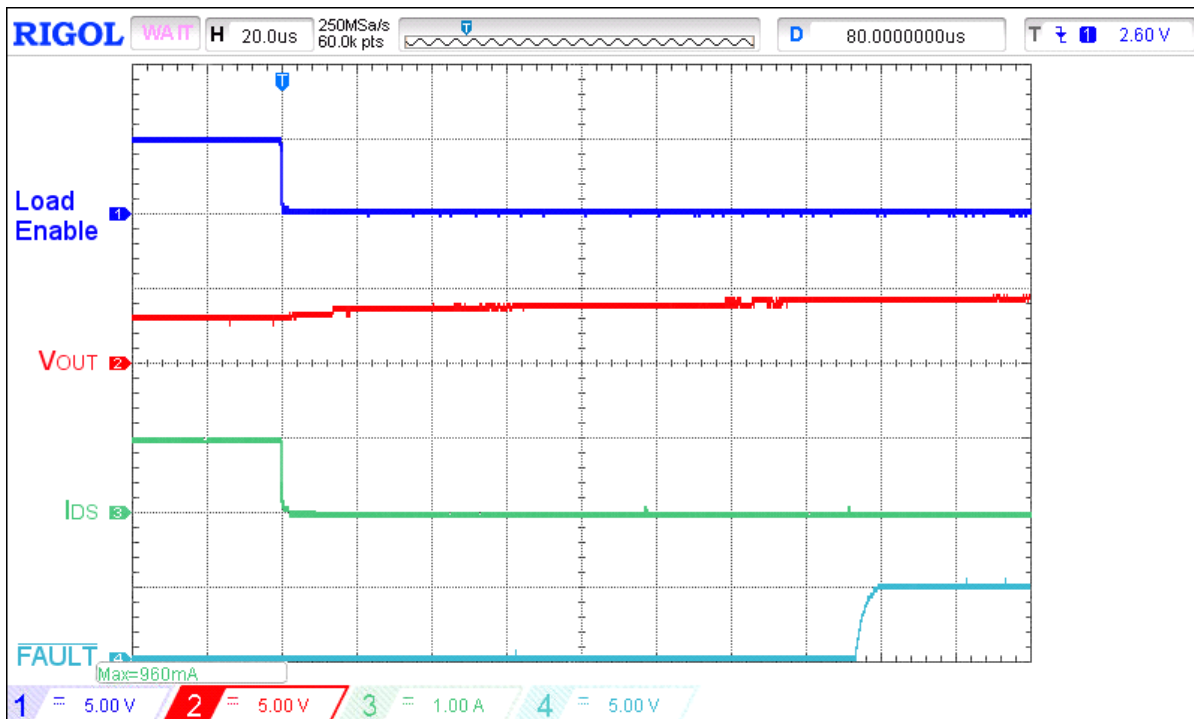


Figure 23. Typical $\overline{\text{FAULT}}$ de-assertion waveform for $V_{\text{IN}} = 4.5 \text{ V}$, $C_{\text{LOAD}} = 10 \mu\text{F}$, $I_{\text{ACL}} = 1 \text{ A}$, $R_{\text{SET}} = 91 \text{ k}\Omega$, switch out 3.3Ω load

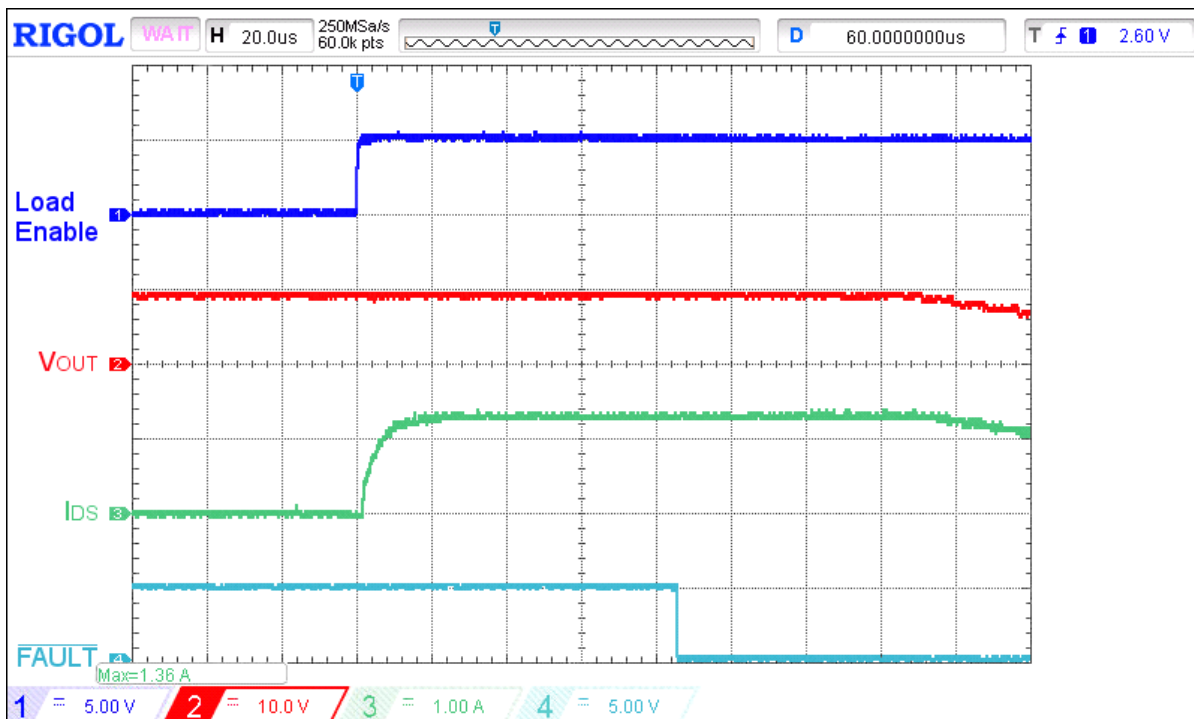


Figure 24. Typical $\overline{\text{FAULT}}$ assertion waveform for $V_{\text{IN}} = 9 \text{ V}$, $C_{\text{LOAD}} = 10 \mu\text{F}$, $I_{\text{ACL}} = 1 \text{ A}$, $R_{\text{SET}} = 91 \text{ k}\Omega$, switch on 6.6Ω load

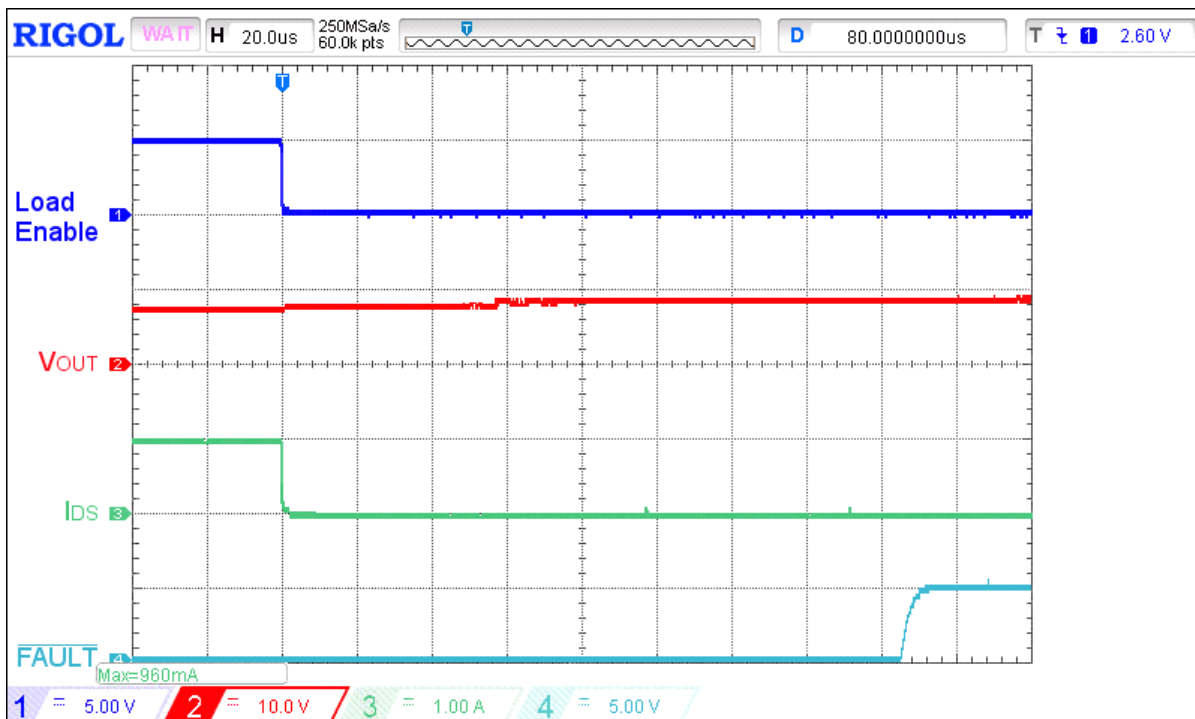


Figure 25. Typical FAULT de-assertion waveform for $V_{IN} = 9\text{ V}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $I_{ACL} = 1\text{ A}$, $R_{SET} = 91\text{ k}\Omega$, switch out $6.6\text{ }\Omega$ load

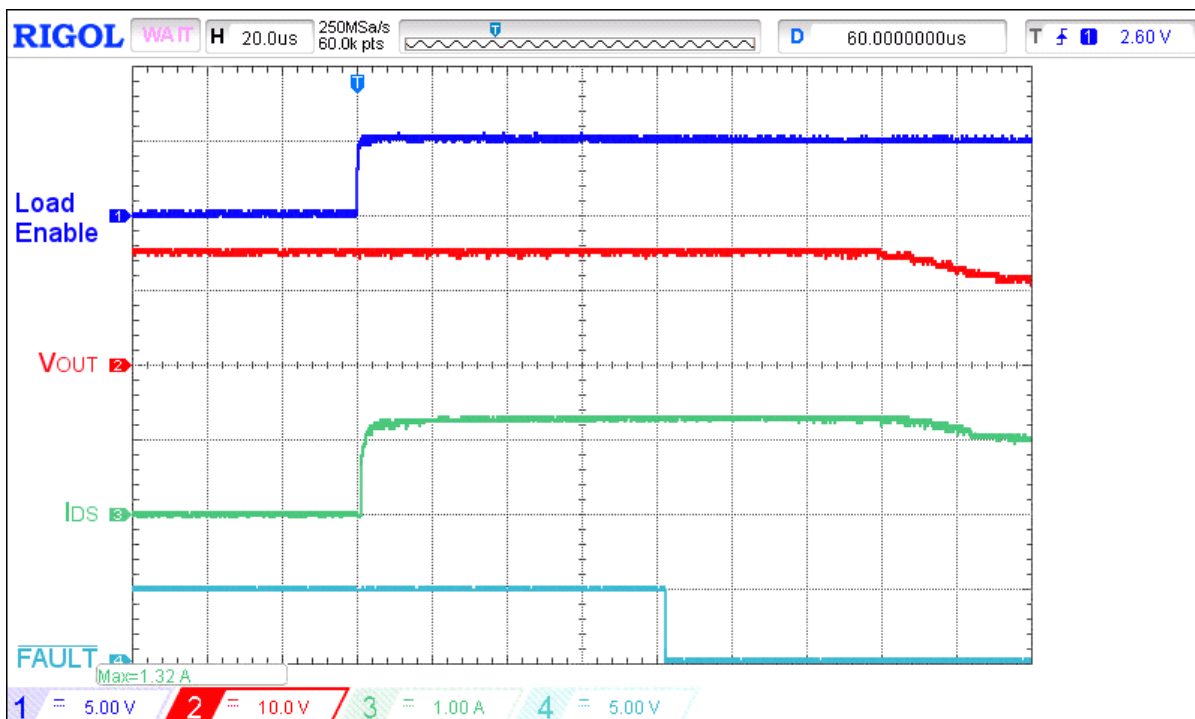


Figure 26. Typical FAULT assertion waveform for $V_{IN} = 15\text{ V}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $I_{ACL} = 1\text{ A}$, $R_{SET} = 91\text{ k}\Omega$, switch on $11.3\text{ }\Omega$ load

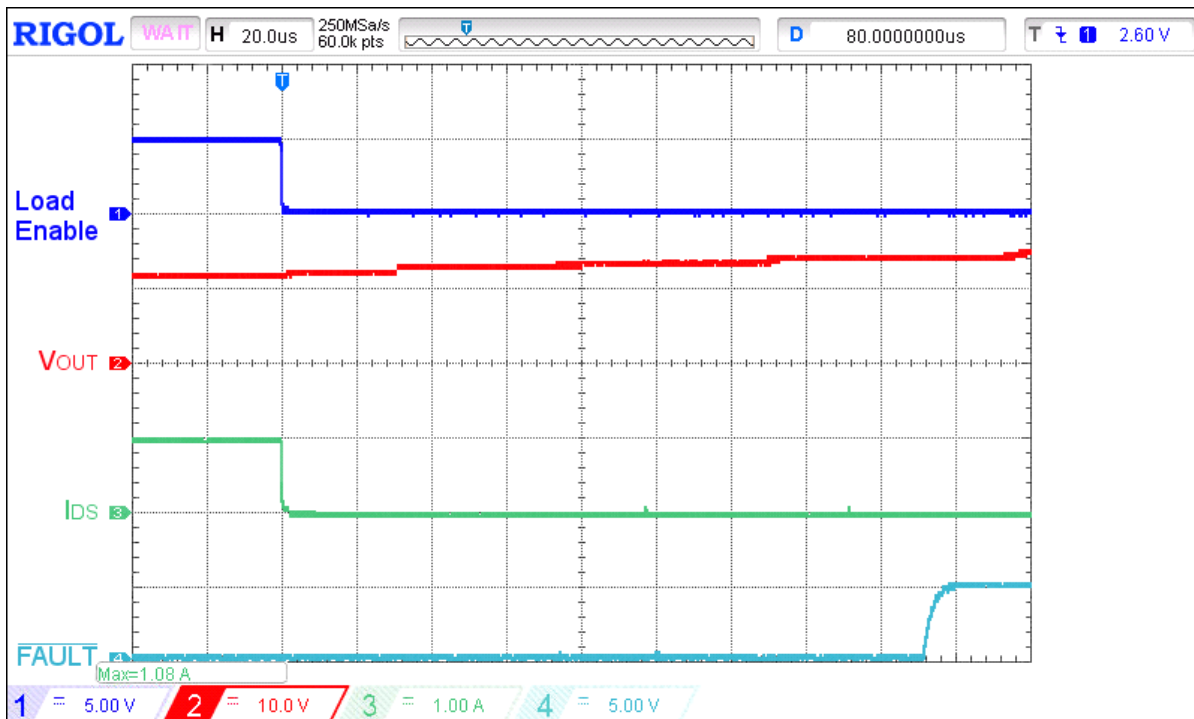


Figure 27. Typical $\overline{\text{FAULT}}$ de-assertion waveform for $V_{\text{IN}} = 15 \text{ V}$, $C_{\text{LOAD}} = 10 \mu\text{F}$, $I_{\text{ACL}} = 1 \text{ A}$, $R_{\text{SET}} = 91 \text{ k}\Omega$, switch out 11.3Ω load

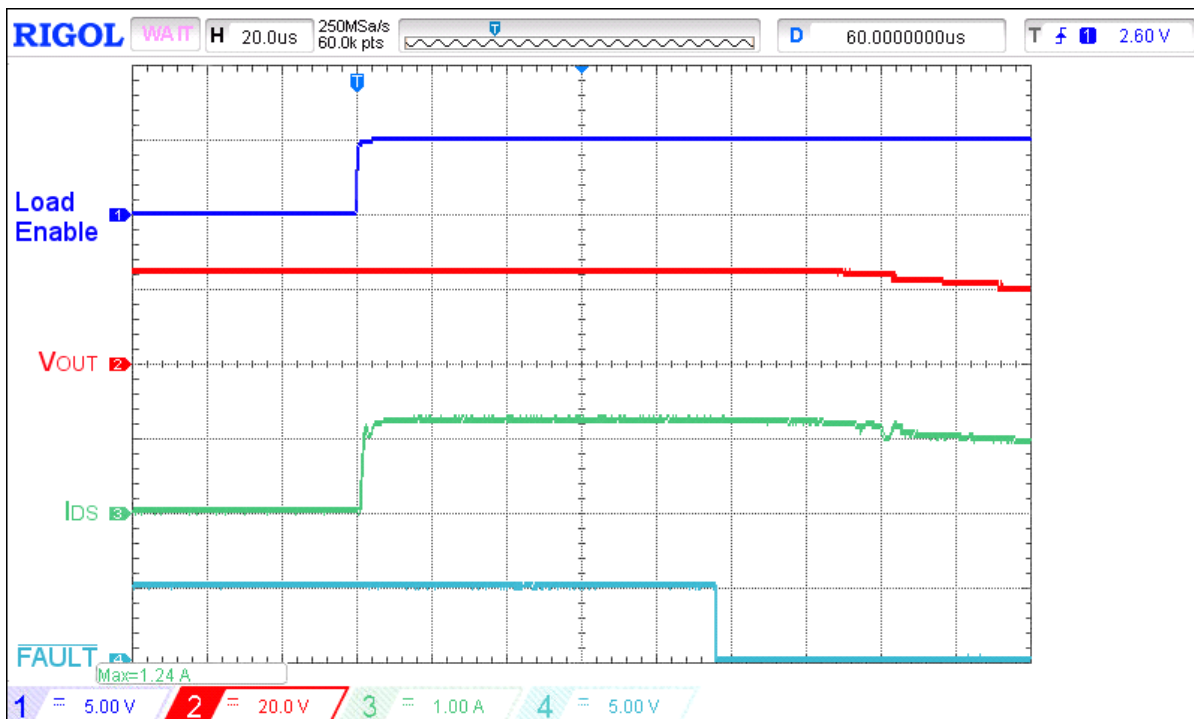


Figure 28. Typical $\overline{\text{FAULT}}$ assertion waveform for $V_{\text{IN}} = 25.2 \text{ V}$, $C_{\text{LOAD}} = 10 \mu\text{F}$, $I_{\text{ACL}} = 1 \text{ A}$, $R_{\text{SET}} = 91 \text{ k}\Omega$, switch on 20.5Ω load

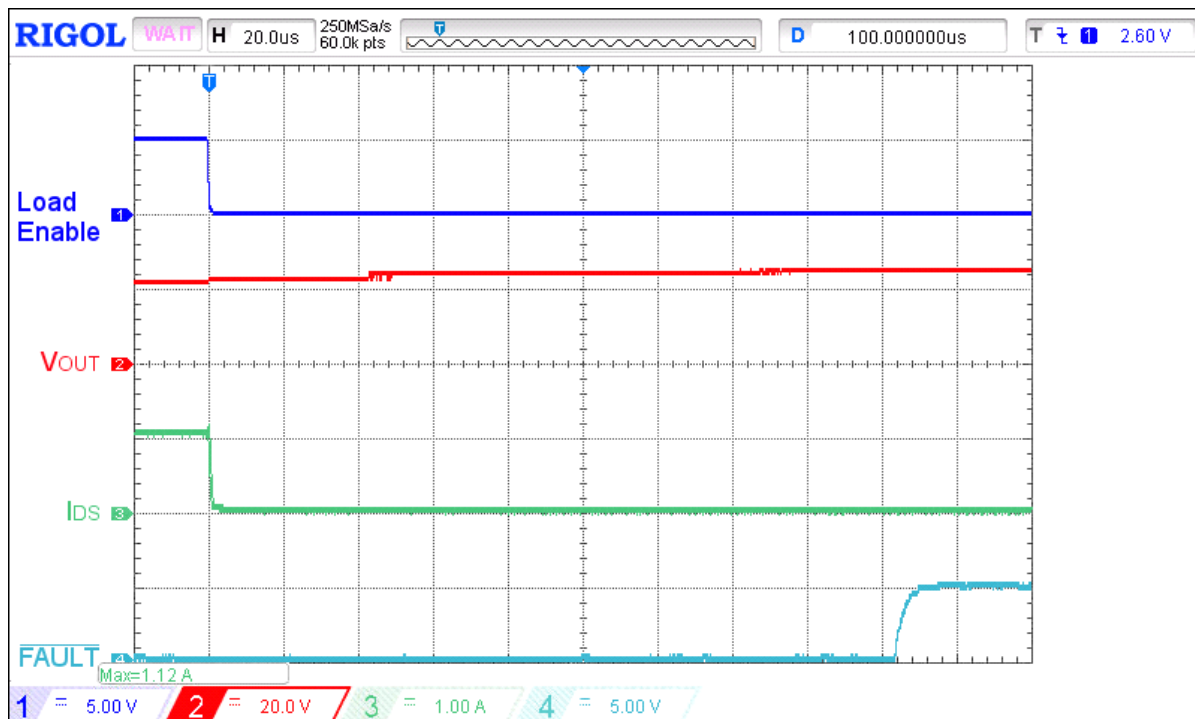


Figure 29. Typical FAULT de-assertion waveform for $V_{IN} = 25.2\text{ V}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $I_{ACL} = 1\text{ A}$, $R_{SET} = 91\text{ k}\Omega$, switch out $20.5\text{ }\Omega$ load

Typical I_{OUT} Response Time Waveforms

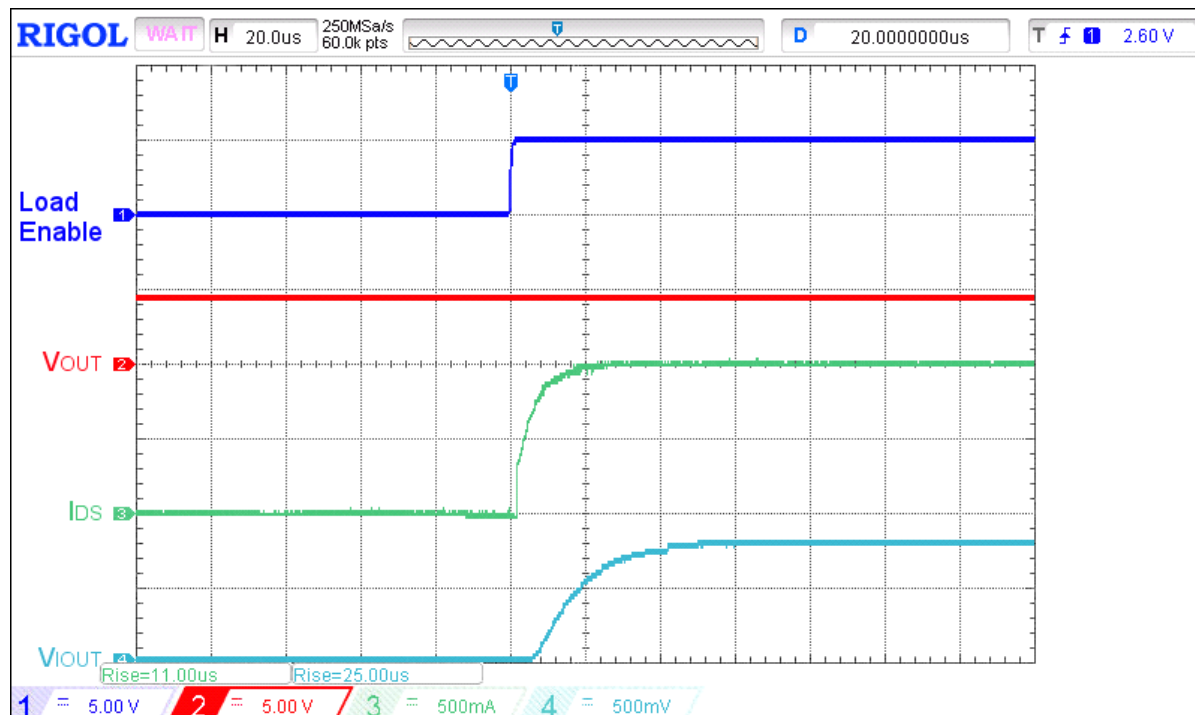


Figure 30. Typical I_{OUT} response time waveform for $V_{IN} = 4.5\text{ V}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{LOAD} = 4.5\text{ }\Omega$, $C_{IOUT} = 0.18\text{ nF}$, $R_{IOUT} = 84.5\text{ k}\Omega$, Load step 0 A to 1 A

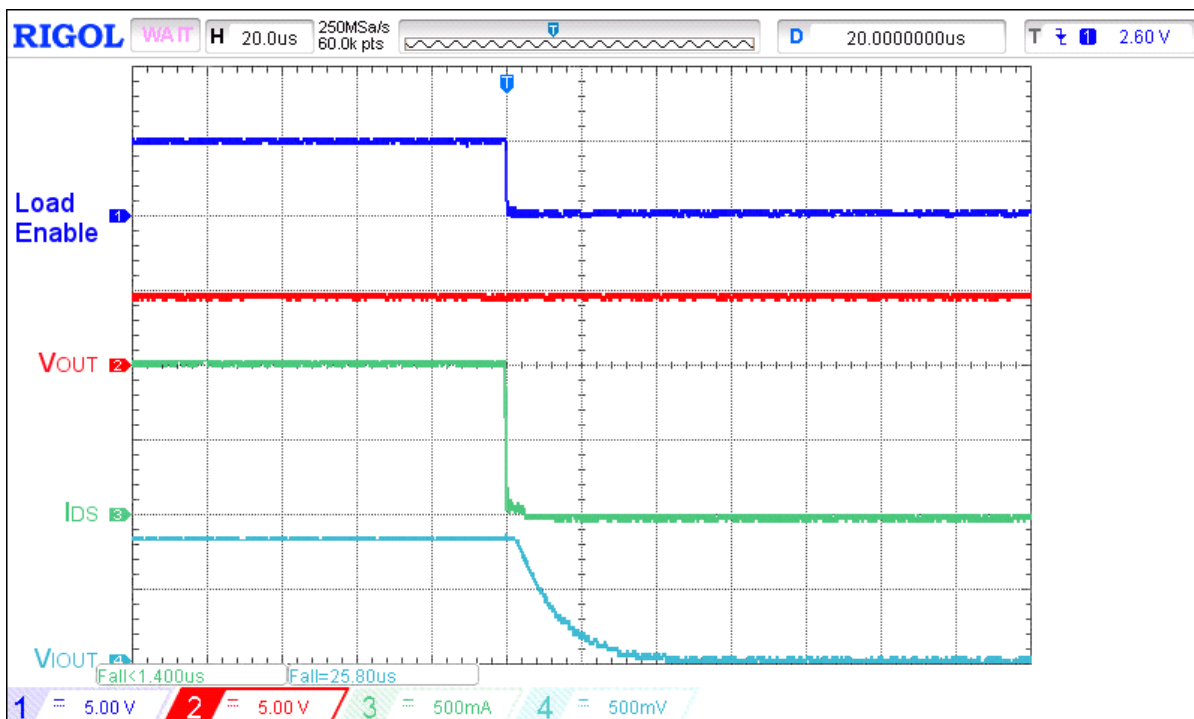


Figure 31. Typical I_{OUT} response time waveform for $V_{IN} = 4.5\text{ V}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{LOAD} = 4.5\text{ }\Omega$
 $C_{IOUT} = 0.18\text{ nF}$, $R_{IOUT} = 84.5\text{ k}\Omega$, Load step 1 A to 0 A

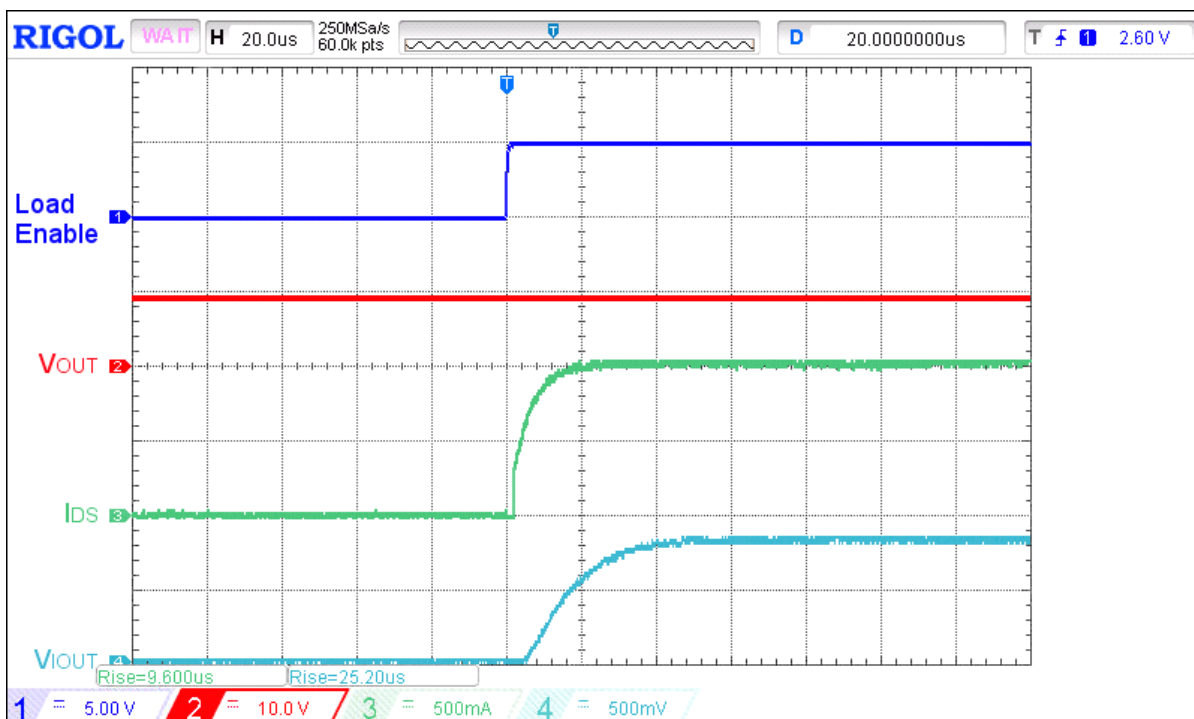


Figure 32. Typical I_{OUT} response time waveform for $V_{IN} = 9\text{ V}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{LOAD} = 4.5\text{ }\Omega$
 $C_{IOUT} = 0.18\text{ nF}$, $R_{IOUT} = 84.5\text{ k}\Omega$, Load step 0 A to 1 A

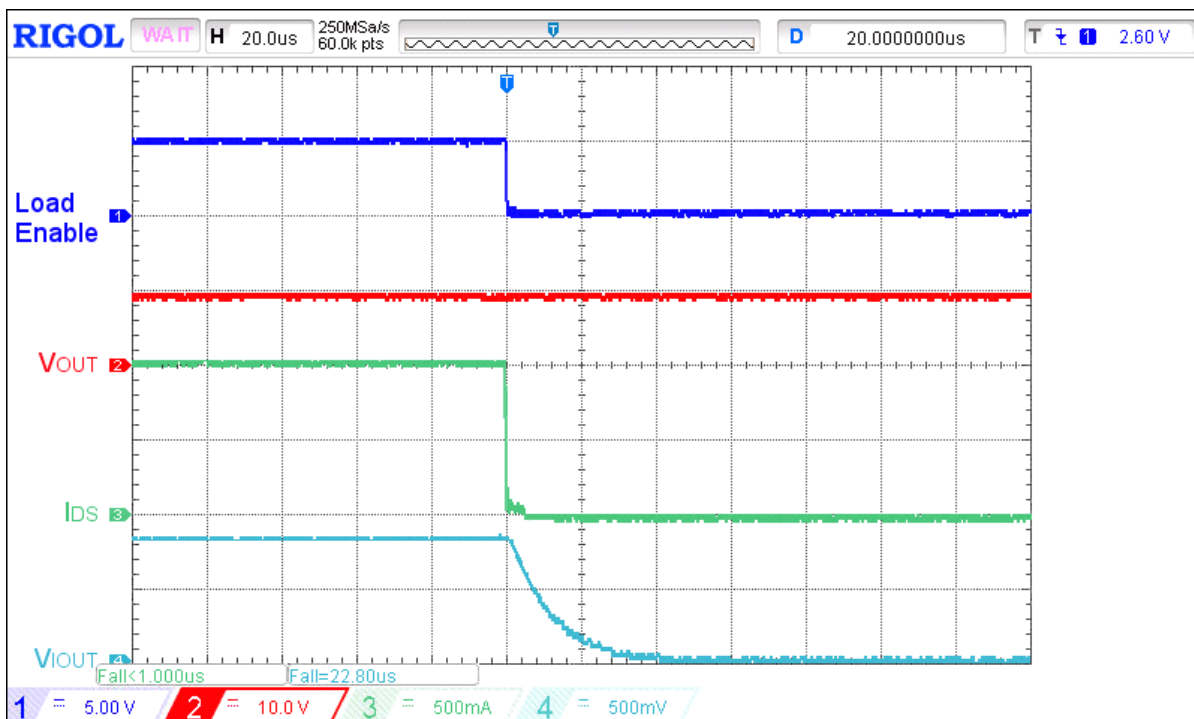


Figure 33. Typical I_{OUT} response time waveform for $V_{IN} = 9\text{ V}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{LOAD} = 9\text{ }\Omega$, $C_{IOUT} = 0.18\text{ nF}$, $R_{IOUT} = 84.5\text{ k}\Omega$, Load step 1 A to 0 A

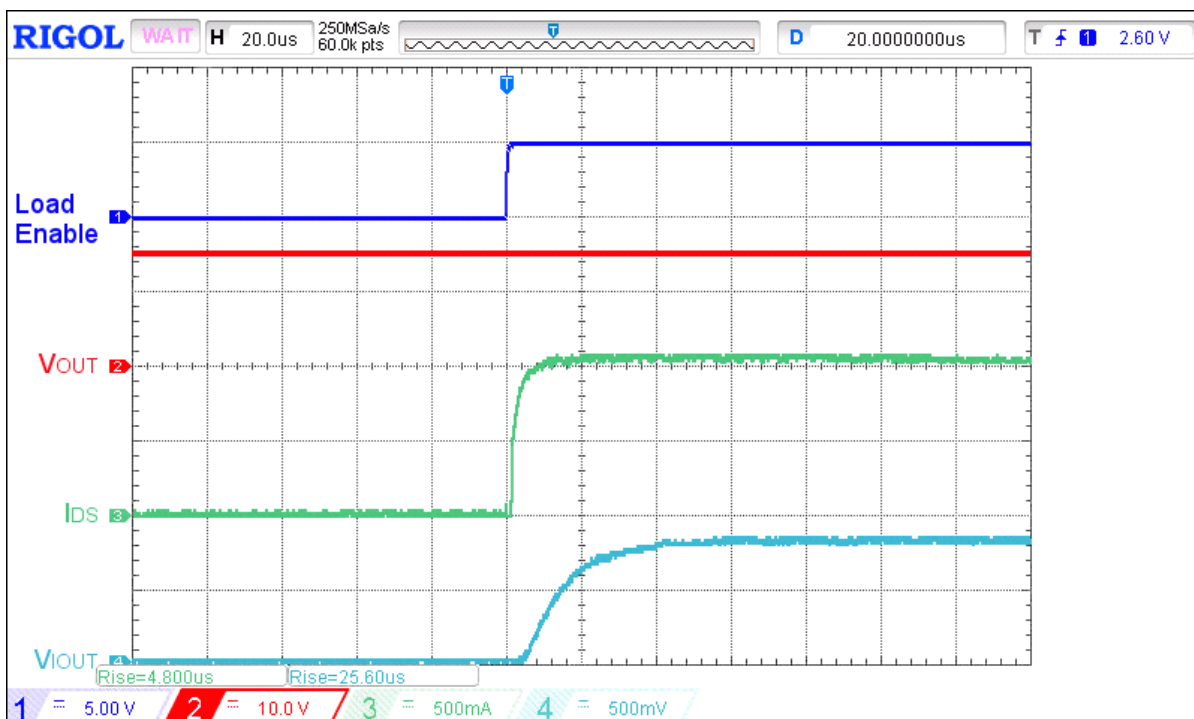


Figure 34. Typical I_{OUT} response time waveform for $V_{IN} = 15\text{ V}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{LOAD} = 15\text{ }\Omega$, $C_{IOUT} = 0.18\text{ nF}$, $R_{IOUT} = 84.5\text{ k}\Omega$, Load step 0 A to 1 A

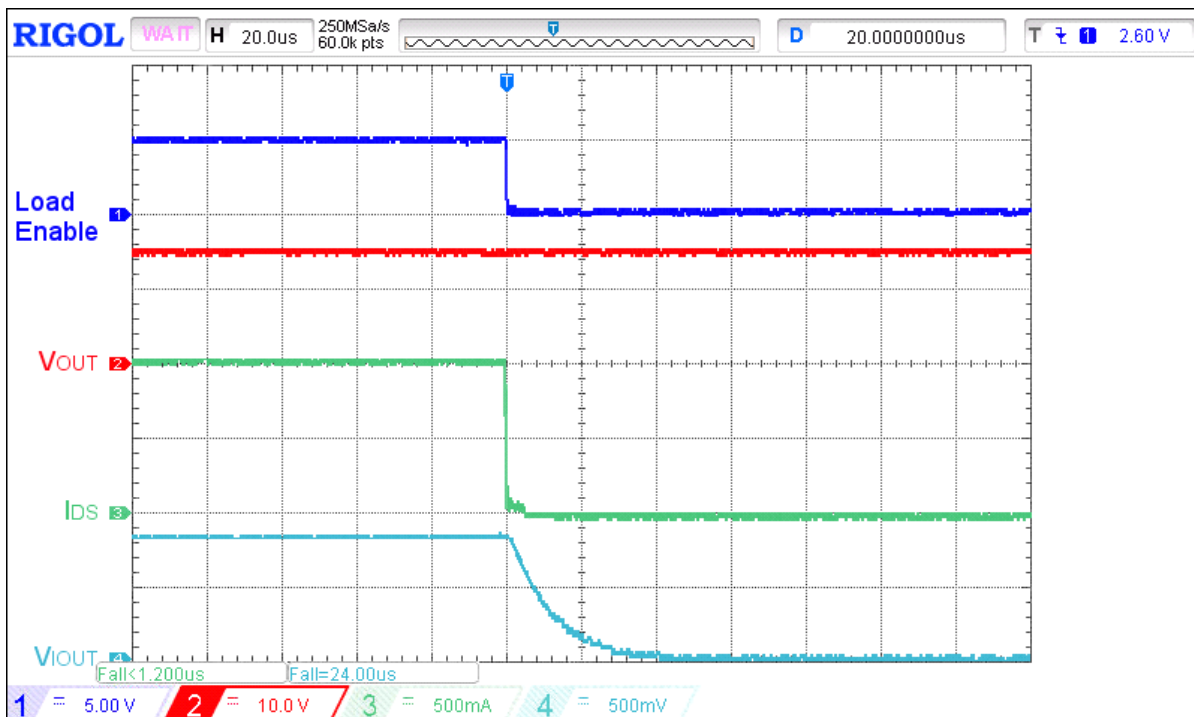


Figure 35. Typical I_{OUT} response time waveform for $V_{IN} = 15\text{ V}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{LOAD} = 15\text{ }\Omega$, $C_{IOUT} = 0.18\text{ nF}$, $R_{IOUT} = 84.5\text{ k}\Omega$, Load step 1 A to 0 A

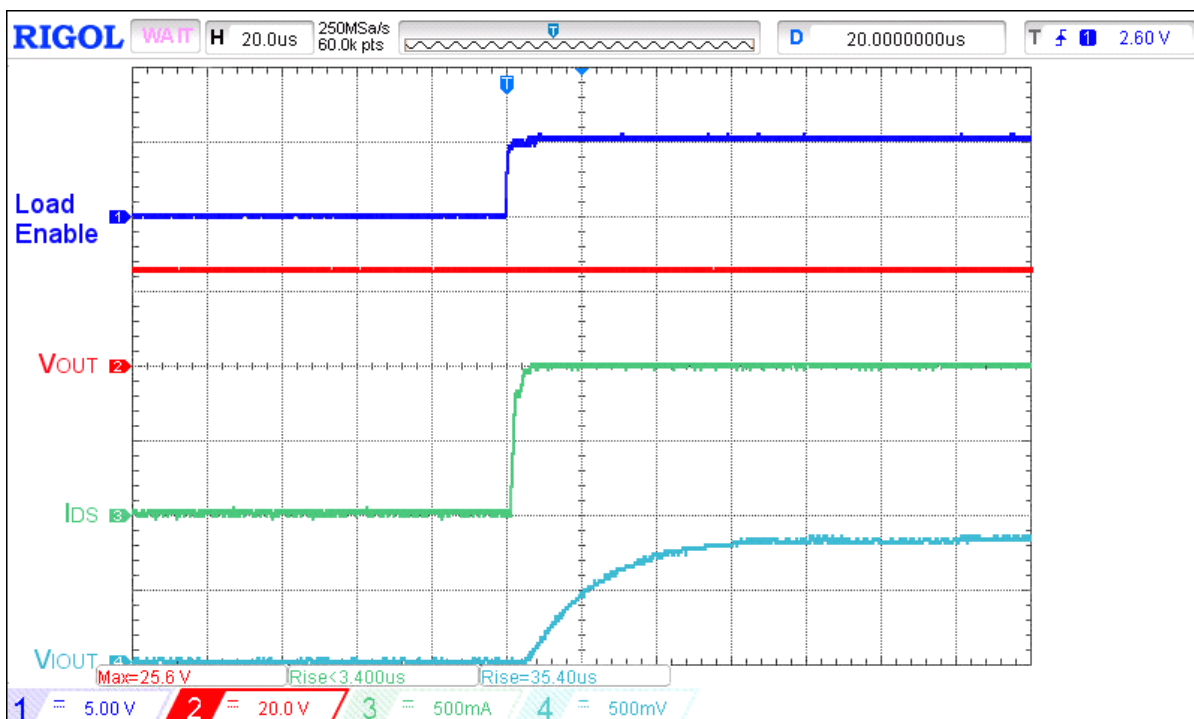


Figure 36. Typical I_{OUT} response time waveform for $V_{IN} = 25.2\text{ V}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{LOAD} = 25\text{ }\Omega$, $C_{IOUT} = 0.18\text{ nF}$, $R_{IOUT} = 84.5\text{ k}\Omega$, Load step 0 A to 1 A

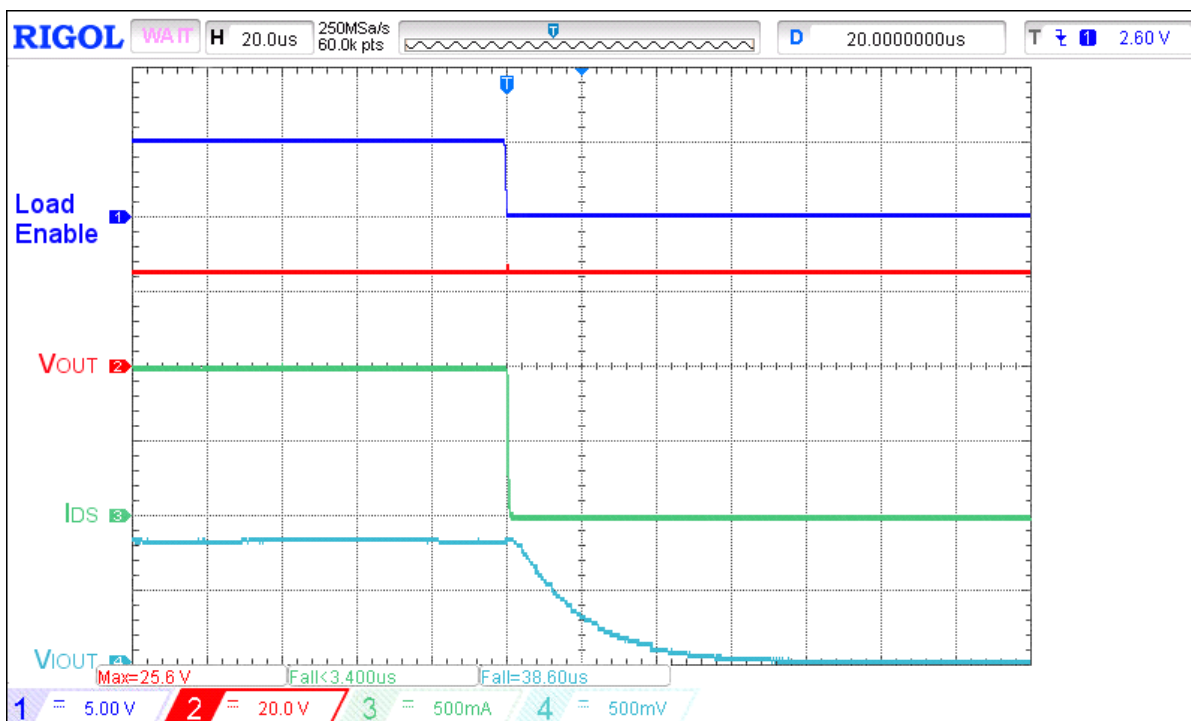


Figure 37. Typical I_{OUT} response time waveform for $V_{IN} = 25.2\text{ V}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{LOAD} = 25\text{ }\Omega$, $C_{IOUT} = 0.18\text{ nF}$, $R_{IOUT} = 84.5\text{ k}\Omega$, Load step 1 A to 0 A

Typical SOA Waveforms

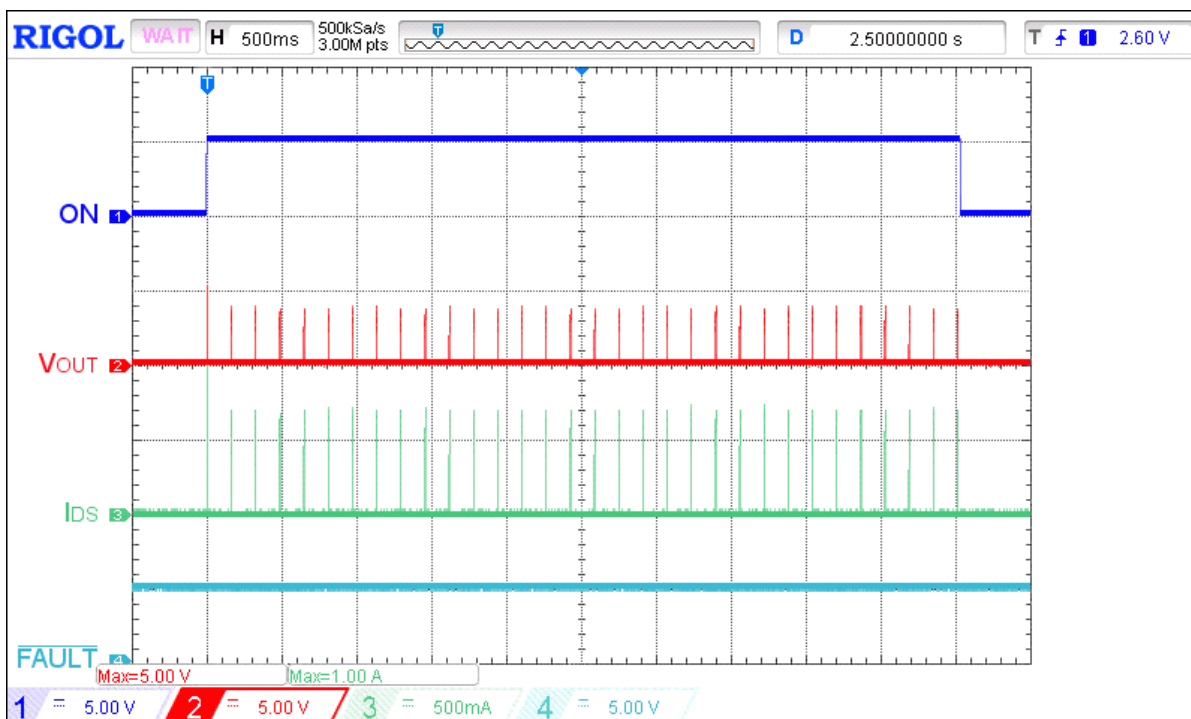


Figure 38. Typical SOA waveform during power up on heavy load for $V_{IN} = 15\text{ V}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{SET} = 18\text{ k}\Omega$, $R_{LOAD} = 4.5\text{ }\Omega$

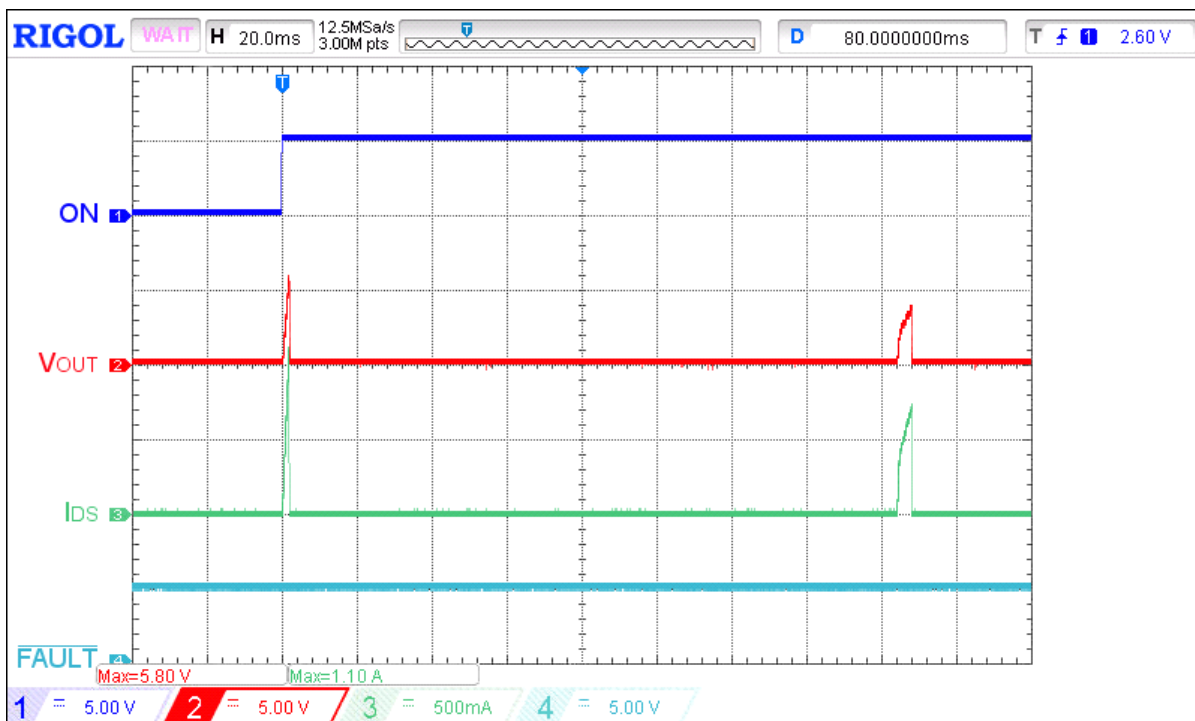


Figure 39. Extended typical SOA waveform during power up under heavy load for $V_{IN} = 15\text{ V}$,
 $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{SET} = 18\text{ k}\Omega$, $R_{LOAD} = 4.5\text{ }\Omega$

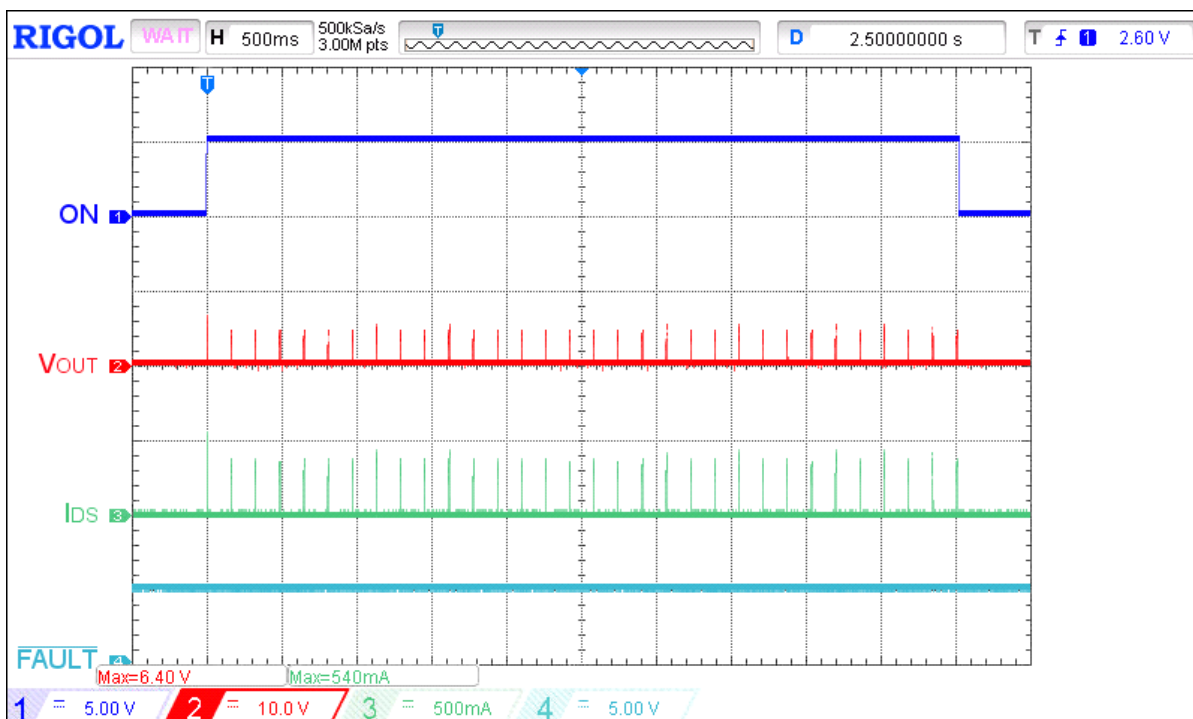


Figure 40. Typical SOA waveform during power up under heavy load for $V_{IN} = 25.2\text{ V}$,
 $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{SET} = 18\text{ k}\Omega$, $R_{LOAD} = 12\text{ }\Omega$

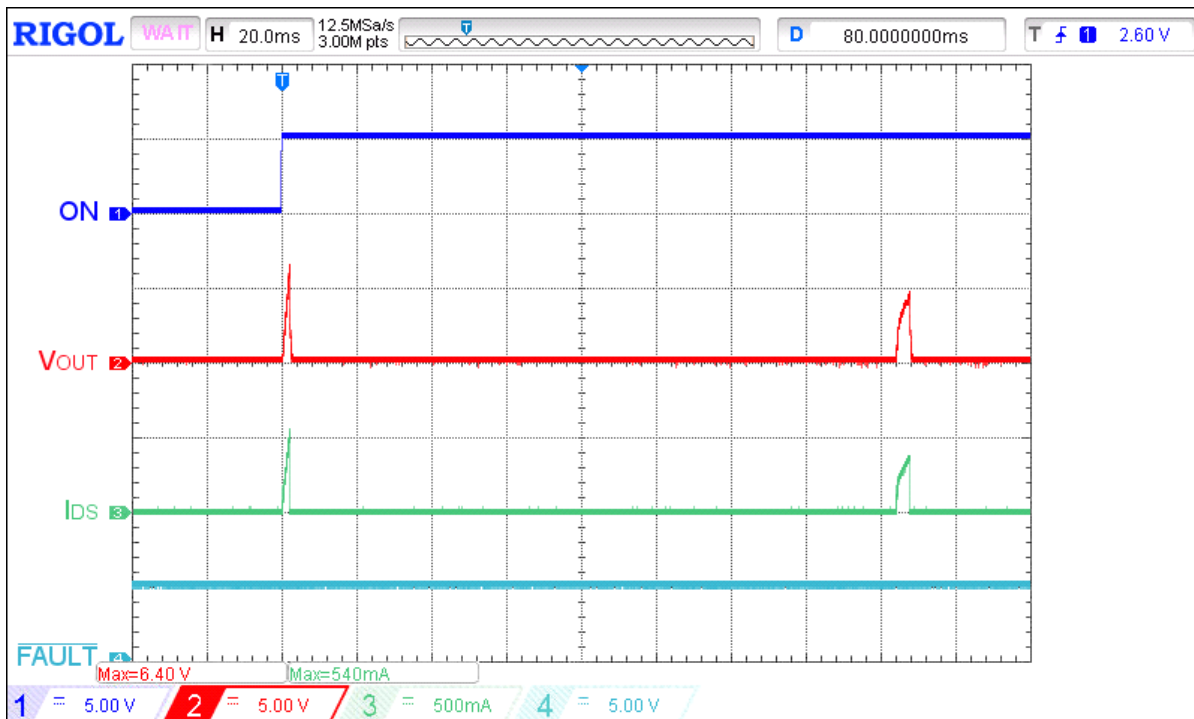


Figure 41. Extended typical SOA waveform during power up under heavy load for $V_{IN} = 25.2\text{ V}$, $C_{LOAD} = 10\text{ }\mu\text{F}$, $R_{SET} = 18\text{ k}\Omega$, $R_{LOAD} = 12\text{ }\Omega$

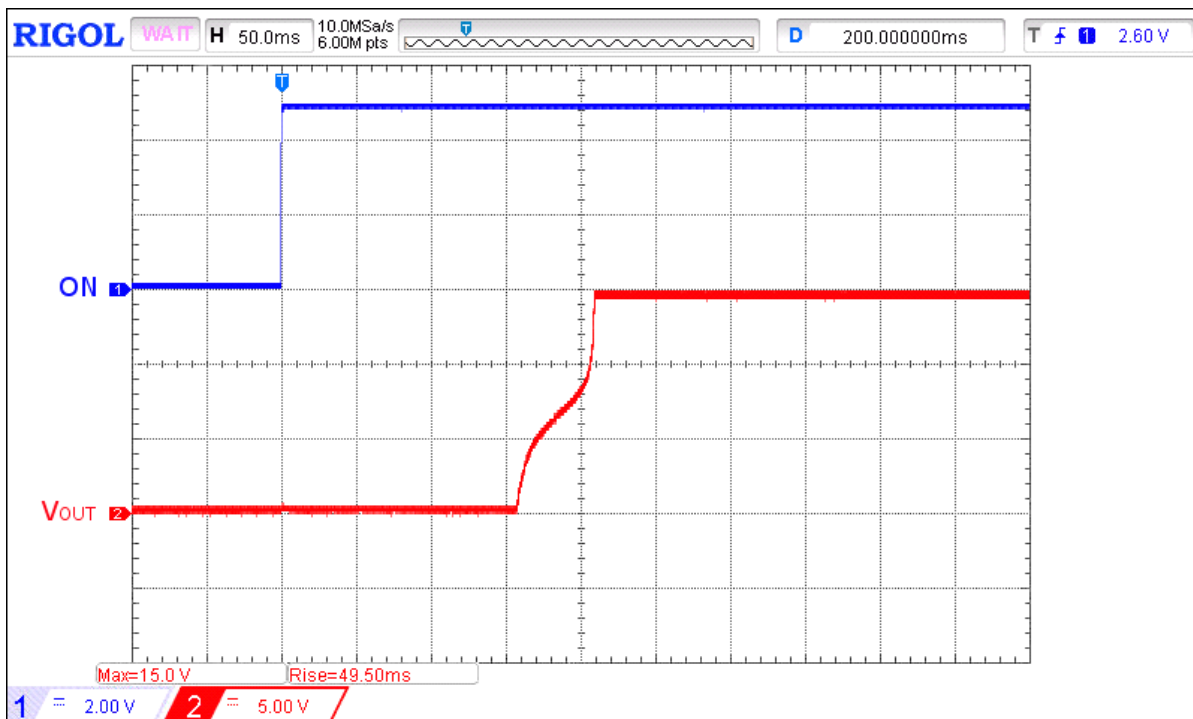


Figure 42. Typical non-monotonic V_{OUT} ramping waveform during power up on heavy load for $V_{IN} = 15\text{ V}$, $C_{LOAD} = 470\text{ }\mu\text{F}$, $C_{SLEW} = 10\text{ nF}$, $R_{SET} = 18\text{ k}\Omega$, $R_{LOAD} = 9.6\text{ }\Omega$



Applications Information

HFET1 Safe Operating Area Explained

Silego's HFET1 integrated power controllers incorporate a number of internal protection features that prevents them from damaging themselves or any other circuit or subcircuit downstream of them. One particular protection feature is their Safe Operation Area (SOA) protection. SOA protection is automatically activated under overpower and, in some cases, under overcurrent conditions. Overpower SOA is activated if package power dissipation exceeds an internal 15 W threshold and HFET1 devices will quickly switch off (open circuit) upon overpower detection and automatically resume (close) nominal operation once overpower condition no longer exists.

One of the possible ways to have an overpower condition trigger SOA protection is when HFET1 products are enabled into heavy output resistive loads and/or into large load capacitors. It is under these conditions to follow carefully the "Safe Start-up Loading" guidance in the Applications section of the datasheet. During an overcurrent condition, HFET1 devices will try to limit the output current to the level set by the external R_{SET} resistor. Limiting the output current, however, causes an increased voltage drop across the FET's channel because the FET's $R_{DS_{ON}}$ increased as well. Since the FET's $R_{DS_{ON}}$ is larger, package power dissipation also increases. If the resultant increase in package power dissipation is higher/equal than 15 W, internal SOA protection will be triggered and the FET will open circuit (switch off). Every time SOA protection is triggered, all HFET1 devices will automatically attempt to resume nominal operation after 160 ms. The automatic retry attempt only allows power-up with SOA at 5 W. This SOA fold back power ensures that the FET survives a short circuit condition. To clear the 5 W SOA fold back, switch the ON pin to "LOW" to power reset SOA to 15 W.

Safe Start-up Condition

SLG59H1019V has built-in protection to prevent over-heating during start-up into a heavy load. Overloading the VOUT pin with a capacitor and a resistor may result in non-monotonic V_{OUT} ramping (*Figure 42*) or repeated restarts (*Figure 38* to *Figure 41*). In general, under light loading on VOUT, V_{OUT} ramping can be controlled with C_{SLEW} value. The following equation serves as a guide:

$$C_{SLEW} = \frac{T_{RISE}}{V_{IN}} \times 4,9 \mu A \times \frac{20}{3}$$

where

T_{RISE} = Total rise time from 10% V_{OUT} to 90% V_{OUT}

V_{IN} = Input Voltage

C_{SLEW} = Capacitor value for CAP pin

When capacitor and resistor loading on VOUT during start up, the following tables will ensure V_{OUT} ramping is monotonic without triggering internal SOA protection:

Safe Start-up Loading for $V_{IN} = 25.2$ V (Monotonic Ramp)			
Slew Rate (V/ms)	C_{SLEW} (nF) ²	C_{LOAD} (μF)	R_{LOAD} (Ω)
0.5	66.7	500	60
1.0	33.3	250	60
1.5	22.2	160	60
2.0	16.7	120	60
2.5	13.3	100	60



Safe Start-up Loading for $V_{IN} = 15\text{ V}$ (Monotonic Ramp)			
Slew Rate (V/ms)	C_{SLEW} (nF) ²	C_{LOAD} (μF)	R_{LOAD} (Ω)
1	33.3	500	12
2	16.7	250	12
3	11.1	160	12
4	8.3	120	12
5	6.7	100	12

Note 2: Select the closest-value tolerance capacitor.

Setting the SLG59H1019V's Active Current Limit

R_{SET} (kΩ)	Active Current Limit (A) ³
91	1
45	2
30	3
18	5

Note 3: Active Current Limit accuracy is $\pm 15\%$ over voltage range and over temperature range.



Power Dissipation

The junction temperature of the SLG59H1019V depends on different factors such as board layout, ambient temperature, and other environmental factors. The primary contributor to the increase in the junction temperature of the SLG59H1019V is the power dissipation of its power MOSFET. Its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD = R_{DS(ON)} \times I_{DS}^2$$

where:

PD = Power dissipation, in Watts (W)

$R_{DS(ON)}$ = Power MOSFET ON resistance, in Ohms (Ω)

I_{DS} = Output current, in Amps (A)

and

$$T_J = PD \times \theta_{JA} + T_A$$

where:

T_J = Junction temperature, in Celsius degrees ($^{\circ}\text{C}$)

θ_{JA} = Package thermal resistance, in Celsius degrees per Watt ($^{\circ}\text{C}/\text{W}$)

T_A = Ambient temperature, in Celsius degrees ($^{\circ}\text{C}$)

In current-limit mode, the SLG59H1019V's power dissipation can be calculated by taking into account the voltage drop across the power switch ($V_{IN}-V_{OUT}$) and the magnitude of the output current in current-limit mode (I_{ACL}):

$$PD = (V_{IN}-V_{OUT}) \times I_{ACL} \text{ or}$$

$$PD = (V_{IN} - (R_{LOAD} \times I_{ACL})) \times I_{ACL}$$

where:

PD = Power dissipation, in Watts (W)

V_{IN} = Input Voltage, in Volts (V)

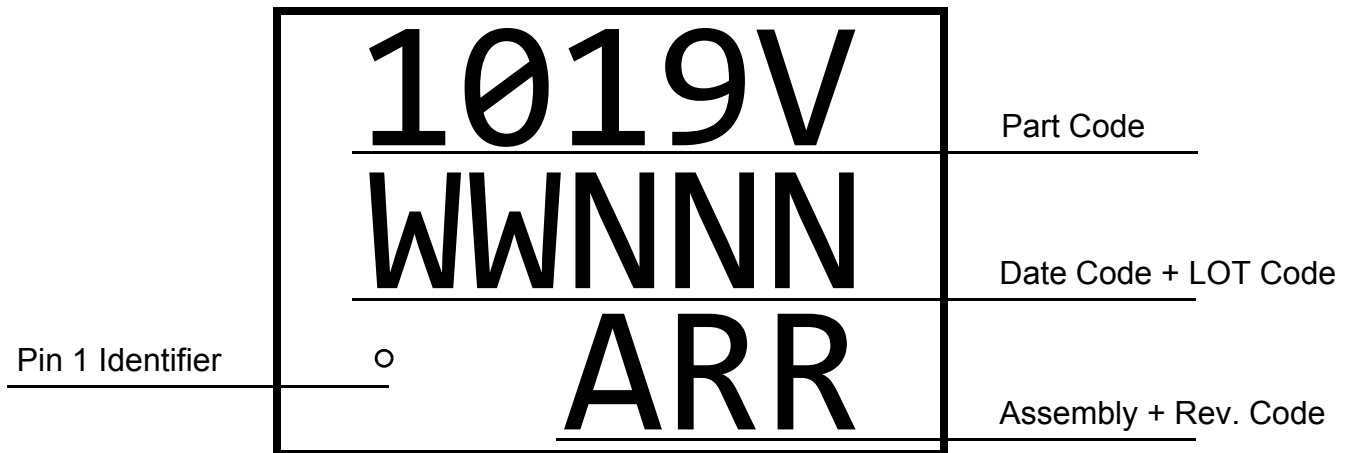
R_{LOAD} = Load Resistance, in Ohms (Ω)

I_{ACL} = Output limited current, in Amps (A)

$V_{OUT} = R_{LOAD} \times I_{ACL}$



Package Top Marking System Definition



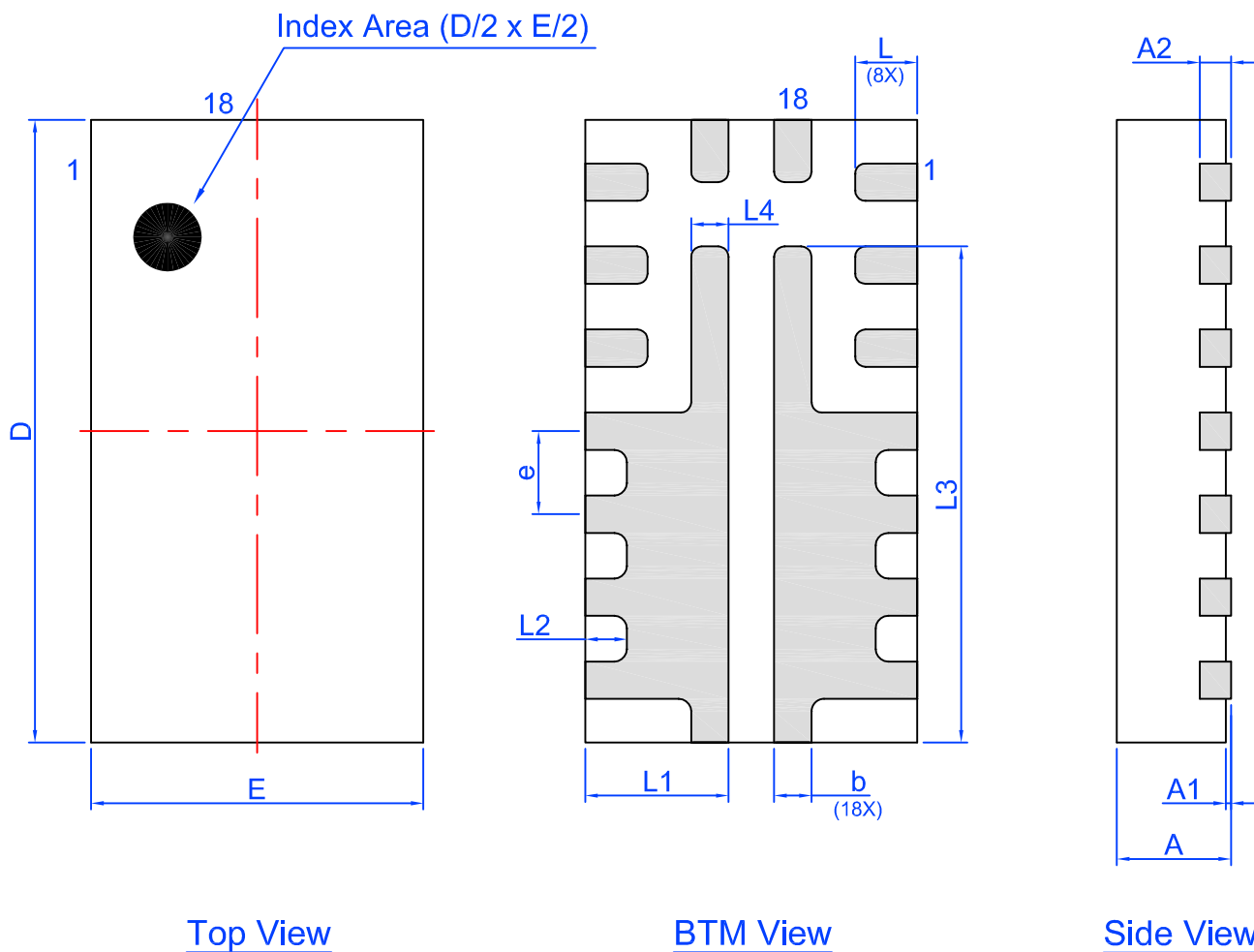
1019V - Part ID Field
WW - Date Code Field¹
NNN - Lot Traceability Code Field¹
A - Assembly Site Code Field²
RR - Part Revision Code Field²

Note 1: Each character in code field can be alphanumeric A-Z and 0-9
Note 2: Character in code field can be alphabetic A-Z



Package Drawing and Dimensions

18 Lead TQFN Package 1.6 x 3 mm (Fused Lead)
JEDEC MO-220, Variation WCEE



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.05	E	1.55	1.60	1.65
A2	0.10	0.15	0.20	L	0.25	0.30	0.35
b	0.13	0.18	0.23	L1	0.64	0.69	0.74
e	0.40 BSC			L2	0.15	0.20	0.25
L3	2.34	2.39	2.44	L4	0.13	0.18	0.23

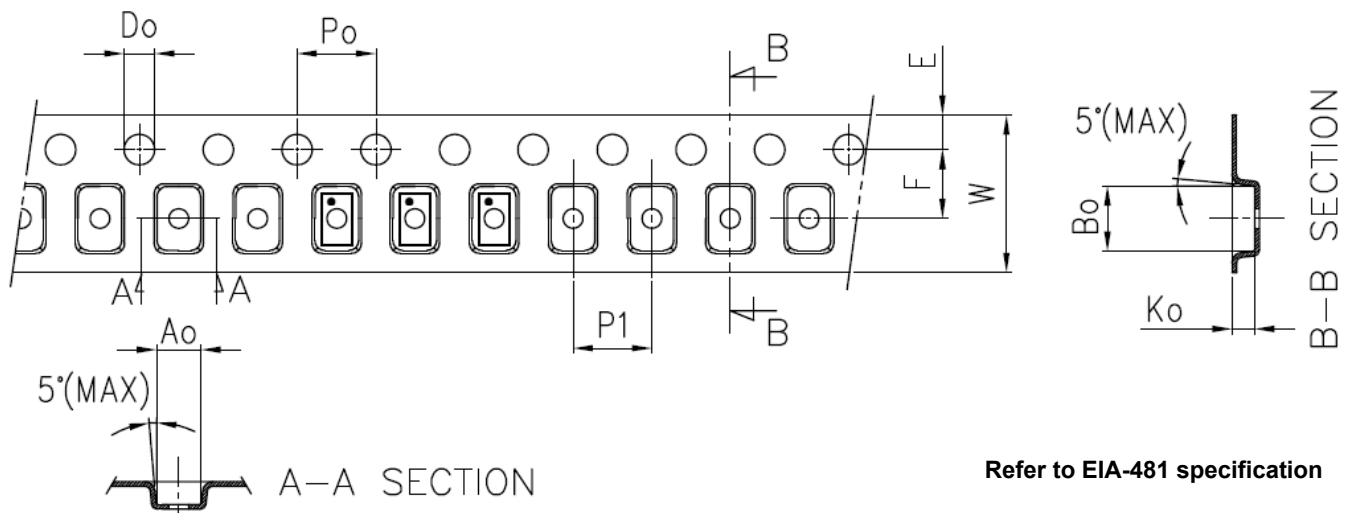


Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 18L 0.4P FC Green	18	1.6 x 3 x 0.55	3,000	3,000	178 / 60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 18L 0.4P FC Green	1.78	3.18	0.76	4	4	1.5	1.75	3.5	8



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.64 mm³ (nominal). More information can be found at www.jedec.org.



SILEGO

SLG59H1019V

Revision History

Date	Version	Change
12/15/2017	1.00	Production Release

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Dialog Semiconductor:](#)

[SLG59H1019VTR](#) [SLG59H1019V](#)