Ultra-Low Power Stereo Codec

General Description

DA7218 is a high-performance, low-power audio codec optimized for use in portable applications or wearable devices. It has single-ended headphone outputs with headphone detect for use in accessories, offering excellent left to right channel separation and common mode noise rejection. DA7218 also has a stereo DAC to headphone output path and ultra-low power operating modes to support always-on audio detect applications.

DA7218 contains two analog microphone input paths, or up to four digital microphone input paths, or a combination of both The other chip in this family, the DA7217 has differential headphone outputs without headphone detect, and has been designed for use inside headset devices.

Key Features

- High performance stereo DAC to headphone playback path with 110 dB dynamic range
- 4 mW stereo playback power consumption
- DAC digital filters with audio and voice mode options, five-band equalizer and five programmable biquad stages
- Dedicated low-latency digital sideband filter with three programmable biquad stages
- High performance microphone to ADC record path with a 105 dB dynamic range
- 2.5 mW stereo record power consumption
- ADC digital filters with audio and voice mode options
- 500 µW always-on record mode with automatic level detection
- Hybrid analog / digital automatic level control to dynamically control the record level
- Shutdown mode offering current consumption during standby of 2.5 µA
- Two low-noise microphone bias regulators with programmable output voltage and ultra-low power mode
- Ability to differentiate between stereo and mono headsets
- Automatic detection of headset removal and confirmation of headset insertion
- Flexible digital mixing from all seven inputs to all six outputs with independent gain on each mixer path
- Ability to run the ADCs at a different sample rate to the DACs on a single I^{2}S interface
- Digital tone generator with built-in support for DTMF
- System controller for simplified, pop-free start-up and shutdown
- Phase-locked loop with sample rate tracking supporting MCLK frequencies from 2 MHz to 54 MHz
- Automatic tuning of on-chip reference oscillator for clock-free operation in low-power modes
- 4-wire digital audio interface with support for I^{2}S, four-channel I^{2}S, TDM and other audio formats
- 2-wire I^{2}C compatible control interface with support for High Speed mode up to 3.4 MHz
- 24-bit data at up to 96 kHz sample rate
- A high efficiency two-level, true-ground charge pump for generating class-G headphone supplies
- Voice mode filtering up to 32 kHz

Applications

- Wired headsets
- Wired headphones
- Audio accessories
- Portable media players
- Gaming console controllers
- Tablets and eBooks

System Diagram

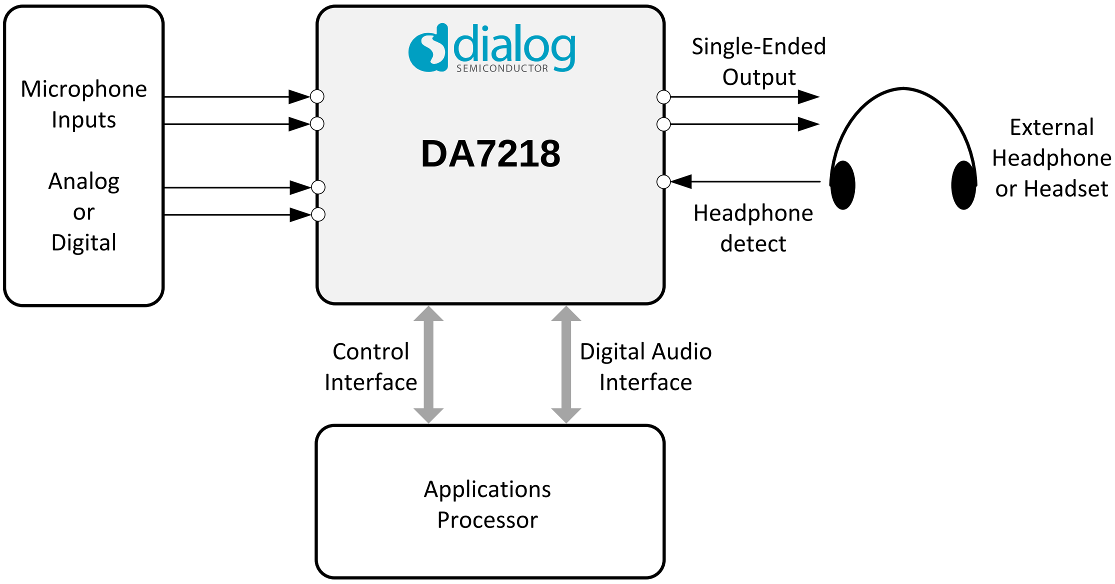


Figure 1: DA7218 with Single-Ended Headset Outputs

Contents

1 Terms and Definitions

ADC	Analog to Digital Converter
AGS	ADC Gain Swap (input Dynamic Range Extension)
ALC	Automatic Level Control
ANC	Active Noise Cancelling
BIQ	Biquad Filter
CIC	Cascaded Integrator and Comb
DAC	Digital to Analog Converter
DAI	Digital Audio Interface
DGS	DAC Gain Swap (output Dynamic Range Extension)
DMIC	Digital Microphone
DRE	Dynamic Range Extension
DTMF	Dual Tone Multi-Frequency
DWA	Data-Weighted Averager
HBM	Human Body Model
HPF	High-Pass Filter
I^2C	Inter-Integrated Circuit interface
I^2S	Inter-IC Sound
LDO	Low Dropout Regulator
LPF	Low-Pass Filter
MCLK	Master Clock
PC	Program Counter
PDM	Pulse Density Modulated
PGA	Programmable Gain Amplifier
PLL	Phase Locked Loop
PSRR	Power Supply Rejection Ratio[4]
RC	Resistance-Capacitance
SC	System Controller
SDM	Sigma Delta Modulator
SNR	Signal to Noise Ratio[5]
SRM	Sample Rate Matching
SWG	Sine Wave Generator
TDM	Time Division Multiplexing
THD+N	Total Harmonic Distortion plus Noise[6]
VCO	Voltage-Controlled Oscillator

2 Terminology

[1] Crosstalk (dB) is the level difference between the active path output and the idle path measured signal level, at the test signal frequency. The active path is configured and supplied with an input signal capable of driving a full scale output, with the signal measured at the output of the specified idle path.

[2] Mute Attenuation is the difference in level between the full scale output signal and the output with mute applied.

[3] Channel Separation (dB) [left-to-right and right-to-left] is the difference in level between the active channel (driven to maximum full scale output) and the signal level measured in the idle channel at the test signal frequency. The active channel is configured and supplied with an input signal capable of driving a full scale output, with the signal measured at the output of the associated idle channel.

[4] PSRR is the ratio of a given power supply change relative to the output signal that results from it. PSRR is measured under quiescent signal path conditions.

[5] SNR is the difference in level between the maximum full scale output signal and the output with no input signal applied.

[6] THD+N is the level of the rms value of the sum of harmonic distortion products plus noise in the specified bandwidth relative to the amplitude of the measured output signal.

All performance measurements carried out with 20 kHz low pass filter, and where noted an A-weighted filter. Failure to use such a filter will result in higher THD and lower SNR readings than are found in the Electrical Characteristics. The low-pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.

3 Block Diagram

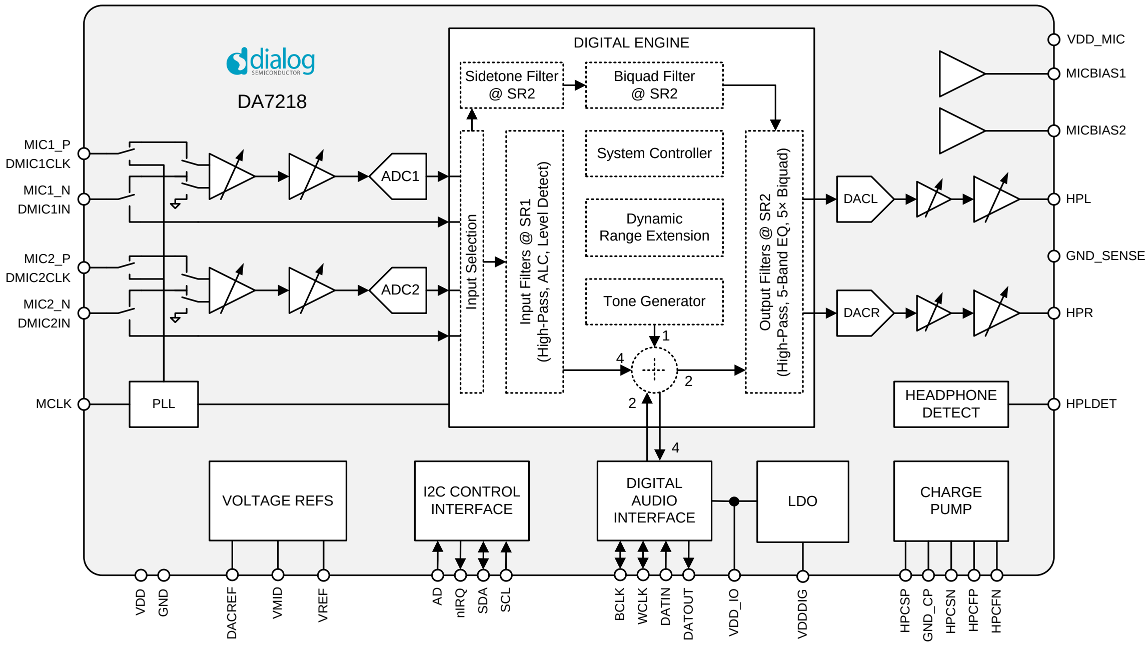


Figure 2: DA7218 Block Diagram

4 Pinout

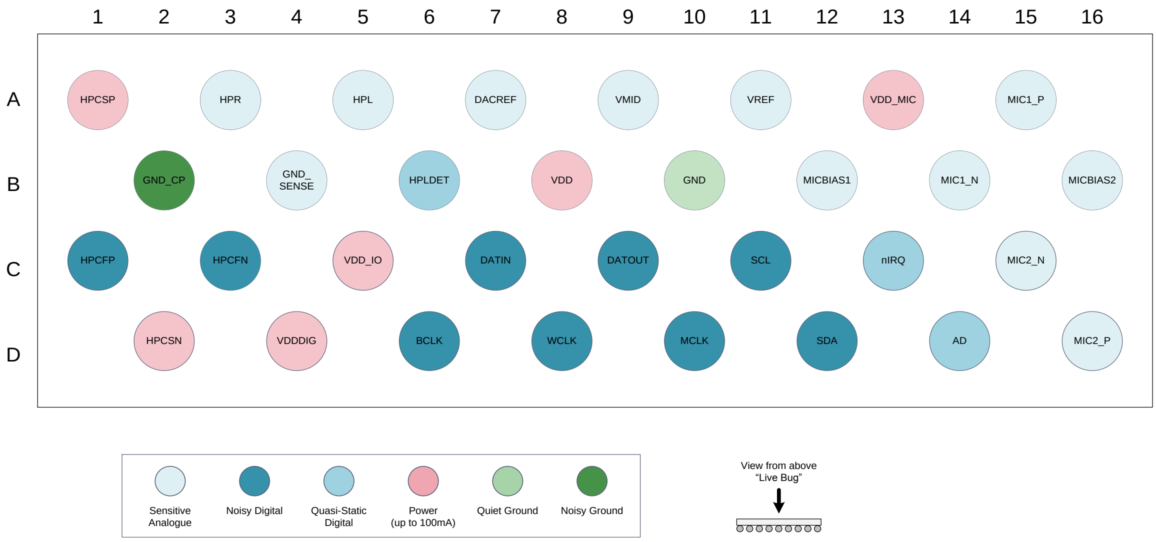


Figure 3: DA7218 Ballout Diagram

Table 1: DA7218 Pin Description

Pin No.	Pin Name	Type (Table 2)	Description
Microphone Inputs			
A15	MIC1_P DMIC1CLK	AI/DO	Differential analog microphone 1 input (Pos) Digital microphone 1 clock output
B14	MIC1_N DMIC1IN	AI/DI	Differential analog microphone 1 input (Neg) Digital microphone 1 data input
D16	MIC2_P DMIC2CLK	AI/DO	Differential analog microphone 2 input (Pos) Digital microphone 2 clock output
C15	MIC2_N DMIC2IN	AI/DI	Differential analog microphone 2 input (Neg) Digital microphone 2 data input
B12	MICBIAS1	AIO	Microphone bias output 1
B16	MICBIAS2	AIO	Microphone bias output 2
Headphone Outputs			
A5	HPL	AO	Single-ended headphone output (Left)
A3	HPR	AO	Single-ended headphone output (Right)
B6	HPLDET	AI	Current source for HP detect
B4	GND_SENSE	AI	Ground reference for single-ended headphone output
Charge Pump			
A1	HPCSP	AIO	Charge pump reservoir capacitor (Pos)
D2	HPCSN	AIO	Charge pump reservoir capacitor (Neg)
C1	HPCFP	AIO	Charge pump flying capacitor (Pos)
C3	HPCFN	AIO	Charge pump flying capacitor (Neg)
Digital Interface			
D12	SDA	DIOD	I^2C bi-directional data
C11	SCL	DI	I^2C clock
D14	AD	DI	I^2C slave address select (high = 1B, low = 1A)
C13	nIRQ	DIOD	Interrupt output (open drain active low)
C7	DATIN	DIO	DAI data input to DA7218
C9	DATOUT	DIO	DAI data output from DA7218
D6	BCLK	DIO	DAI bit clock
D8	WCLK	DIO	DAI word clock (L/R select)
D10	MCLK	DI	Master clock input
References			
A7	DACREF	AIO	DAC reference decoupling capacitor
A9	VMID	AIO	Mid-rail reference decoupling capacitor
A11	VREF	AIO	Bandgap reference decoupling capacitor
Linear Regulator			
D4	VDDDIG	AO	Output from digital supply LDO

Pin No.	Pin Name	Type (Table 2)	Description
Supplies			
B8	VDD	AI	Main analog supply
A13	VDD_MIC	AI	Supply for MICBIAS LDO
C5	VDD_IO	AI	Supply for digital interface and LDO
B10	GND	AI	Ground reference
B2	GND_CP	AI	Ground reference

Table 2: Pin Type Definition

Pin Type	Description	Pin Type	Description
DI	Digital Input	AI	Analog Input
DO	Digital Output	AO	Analog Output
DIO	Digital Input/Output	AIO	Analog Input/Output
DIOD	Digital Input/Output open drain	SPU	Switchable pull-up resistor
PU	Fixed pull-up resistor	SPD	Switchable pull-down resistor
PD	Fixed pull-down resistor		

4.1 Input Pins

4.1.1 MIC1_P (DMIC1CLK)

MIC1_P is the positive differential input for the first analog microphone channel. It can be used as a single-ended input (see Figure 8).

Alternatively for digital microphones, MIC1_P is used to provide a clock output.

4.1.2 MIC1_N (DMIC1IN)

MIC1_N is the negative differential input for the first analog microphone channel. It can be used as a single-ended input.

Alternatively for digital microphones and active noise cancelling (ANC) applications, MIC1_N is used as a pulse density modulated (PDM) data input.

4.1.3 MIC2_P (DMIC2CLK)

MIC2_P is the positive differential input for the second analog microphone channel. It can be used as a single-ended input.

Alternatively for digital microphones, MIC2_P is used to provide a clock output.

4.1.4 MIC2_N (DMIC2IN)

MIC2_N is the negative differential input for the second analog microphone channel. It can be used as a single-ended input.

Alternatively for digital microphones and ANC applications, MIC2_N is used as a PDM data input.

4.1.5 MCLK

MCLK is the master clock input pin. It is used as the main system clock either directly or via the PLL.

4.1.6 SCL

SCL is the control interface (I^2C) clock input and is used in conjunction with SDA to control the device.

4.1.7 AD

AD is used to select between one of two possible I^2C slave addresses by connecting the pin to GND or VDD_IO. (High = 1B, Low = 1A).

4.1.8 DATIN

DATIN is the data input pin which forms part of the digital audio interface (DAI). It is used to present audio playback data to the device.

4.2 Output Pins

4.2.1 nIRQ

nIRQ is the open drain active-low interrupt output to alert the host to either an accessory or a level-detect event.

4.2.2 DATOUT

DATOUT is the data output pin, which forms part of the DAI.

4.3 Bi-Directional Pins

4.3.1 SDA

SDA is the control interface (I^2C) data input/output and is used in conjunction with SCL to control the device.

4.3.2 BCLK

BCLK is the bit clock input/output pin which forms part of the DAI. It is used to clock audio data bits into or out from the device or both.

4.3.3 WCLK

WCLK is the word clock input/output pin that forms part of the DAI.

4.4 Single-Ended Headphone Pins

4.4.1 HPL

HPL is the left-channel headphone output. It is ground-centered so the headphone speaker can be connected directly between HPL and ground.

4.4.2 Pin HPR

HPR is the right-channel headphone output. It is ground-centered so the headphone speaker can be connected directly between HPR and ground.

4.4.3 GND_SENSE

GND_SENSE is the ground reference for the headphone output. The trace between the ball and the headphone connector must be grounded as close as possible to the headphone connector.

The GND_SENSE trace should run in parallel with the HPL and HPR traces in a differential-style routing for best common-node noise rejection.

4.4.4 HPLDET

HPLDET is used to detect the insertion or removal of a jack. If used it must be connected to the tip detect pin in the headphone socket.

If not required it must be left unconnected.

4.5 Charge Pump Pins

4.5.1 HPCSP

HPCSP is the positive output from the headphone charge pump. This pin should be connected to ground via a reservoir capacitor.

4.5.2 HPCSN

HPCSN is the negative output from the headphone charge pump. If using the charge pump, this pin must be connected to ground via a reservoir capacitor. If the charge pump is not being used, then this pin should be tied directly to ground.

4.5.3 HPCFP

HPCFP is one of the flying capacitor connections required by the headphone charge pump. If the charge pump is in use it must be connected to HPCFN via a capacitor. If the charge pump is not being used, then this pin can be left floating.

4.5.4 HPCFN

HPCFP is one of the flying capacitor connections required by the headphone charge pump. If the charge pump is in use it must be connected to HPCFP via a capacitor. If the charge pump is not being used, then this pin can be left floating.

4.6 References

4.6.1 VMID

VMID is mid-rail reference decoupling capacitor connection.

4.6.2 DACREF

DACREF is the DAC reference decoupling capacitor connection.

4.6.3 VREF

VREF is the bandgap reference decoupling capacitor connection.

4.6.4 MICBIAS1

MICBIAS1 is the first of two MICBIAS outputs. This must be decoupled with a 1 µF capacitor

4.6.5 MICBIAS2

MICBIAS2 is the second of two MICBIAS outputs. This must be decoupled with a 1 µF capacitor.

4.6.6 VDDDIG

VDDDIG is the internal digital supply rail decoupling pin and is used to monitor the LDO output. This must be decoupled with a 1 µF capacitor.

4.7 Supply Pins

4.7.1 VDD

VDD is main analog supply pin. It supplies all the analog circuits except the MICBIAS outputs and the HPAMP outputs.

4.7.2 VDD_IO

VDD_IO is the supply pin for the digital input/output signals.

4.7.3 VDD_MIC

VDD_MIC is the supply pin for the MICBIAS outputs.

4.8 Ground Pins

4.8.1 GND

GND is one of the two ground reference pins (the other is GND_CP) on the device. Connect this pin to a ground plane as close as possible to the device.

4.8.2 GND_CP

GND_CP is one of the two ground reference pins (the other is GND) on the device. Connect this pin to a ground plane as close as possible to the device.

5 Absolute Maximum Ratings

Table 3: Absolute Maximum Ratings (Note 1)

Parameter	Description	Conditions	Min	Max	Unit
	Storage temperature		–65	+165	°C
T_a	Operating temperature		–40	+85	°C
V_{DD}	Main supply voltage		–0.3	+2.75	V
V_{DD_IO}	Digital IO supply voltage		–0.3	+5.5	V
V_{DD_MIC}	Microphone bias supply voltage		–0.3	+5.5	V
V_{DDIO}	Digital IO pins	SDA, SCL, AD, BCLK, WCLK, DATIN, DATOUT, MCLK, nIRQ	–0.3	V_{DD_IO} + 0.3	V
	Digital microphone IO pins	DMIC1CLK, DMIC1IN	–0.3	$V_{MICBIAS1}$ + 0.3	V
	Digital microphone IO pins	DMIC2CLK, DMIC2IN	-0.3	$V_{MICBIAS2}$ + 0.3	V
	Accessory detect pins	HPLDET	–0.3	V_{DD_IO} + 0.3	V
	Analog input pins	MIC1_P, MIC1_N, MIC2_P, MIC2_N	–0.3	V_{DD} + 0.3	V
	Package thermal resistance		60		°CW
V_{ESD_HBM}	ESD susceptibility	Human body model (HBM)		2	kV

Note 1 Stresses beyond those listed under 'Absolute maximum ratings' may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6 Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_a	Operating temperature		–25		+85	°C
V_{DD}	Main supply voltage		+1.7		+2.65	V
V_{DD_IO}	Digital IO supply voltage		+1.5		+3.6	V
V_{DD_MIC}	Microphone bias supply voltage		+1.8		+3.6	V

7 Electrical Characteristics

Unless otherwise stated, test conditions are as follows: $V_{DD} = V_{DD\_IO} = 1.8$ V, $V_{DD\_MIC} = 3.3$ V, $V_{DDDIG} = 1.05$ V, $T_a = 25$ °C, MCLK = 12.288 MHz, SR = 48 kHz, PLL = Bypass mode, Slave mode.

Table 5: Power Consumption

Description	Conditions (Note 1)	Min	Typ	Max	Unit
Powerdown mode			2.5	7	µA
Digital playback to headphone, no load	DACL/R to HP_L/R, quiescent		4		mW
Digital playback to headphone, with load	DACL/R to HP_L/R, 32 Ω load, 0.1 mW at 0 dBFS		6.6		mW
Digital playback to headphone, with load	DACL/R to HP_L/R, 16 Ω load, 0.1 mW at 0 dBFS		7.7		mW
Microphone stereo record	MICL/R to ADCL/R		2.5		mW
Microphone stereo record and digital playback to Headphone, no load	MICL/R to ADCL/R and DACL/R to HP_L/R, quiescent		5.5		mW
Microphone stereo record and digital playback to headphone, with load	MICL/R to ADCL/R and DACL/R to HP_L/R, 16 Ω load, 0.1 mW at 0 dBFS		8.8		mW

Note 1 $V_{DD} = V_{DD\_IO} = V_{DD\_MIC} = 1.8$ V

Table 6: Electrical Characteristics: Microphone Bias

Description	Condition	Min	Typ	Max	Unit
Programmable output voltage	No load, $V_{DD\_MIC} > V_{MICBIAS} + 200$ mV	1.6		3.0	V
Output voltage step			200		mV
Output current	Output voltage droop < 50 mV	2			mA
Power supply rejection ratio	20 Hz to 2 kHz 2 kHz to 20 kHz	70 50			dB
Output voltage noise	$V_{MICBIAS} \leq 2.2$ V		5		μV_{RMS}

Table 7: Electrical Characteristics: Microphone Amplifier

Description	Condition	Min	Typ	Max	Unit
Full-scale input signal	0 dB gain, single-ended 0 dB gain, differential		$0.8 * V_{DD}$ $1.6 * V_{DD}$		V_{PP}
Input resistance		12	15	18	kΩ
Programmable gain		−6		36	dB
Gain step size			6		dB
Absolute gain accuracy	0 dB @ 1 kHz	-0.5		0.5	dB
Gain step error	20 Hz to 20 kHz	-0.1		0.1	dB
Input noise level	Inputs connected to GND, 24 dB gain, input-referred, A-weighted		5		μV_{RMS}
Amplitude ripple	20 Hz to 20 kHz	-0.5		0.5	dB

Description	Condition	Min	Typ	Max	Unit
Power supply rejection ratio	20 Hz to 2 kHz 2 kHz to 20 kHz	90 70			dB
Crosstalk	20 Hz to 20 kHz		88		dB

Table 8: Electrical Characteristics: Input Amplifier

Description	Condition	Min	Typ	Max	Unit
Full-scale input signal	0 dB gain		1.6 * V_{DD}		V_{PP}
Programmable gain		−4.5		18	dB
Gain step size			1.5		dB
Absolute gain accuracy	0 dB @ 1 kHz	-0.5		0.5	dB
Gain step error	20 Hz to 20 kHz	-0.1		0.1	dB
Amplitude ripple	20 Hz to 20 kHz	-0.5		0.5	dB
Power supply rejection ratio	20 Hz to 2 kHz 2 kHz to 20 kHz	90 70			dB

Table 9: Electrical Characteristics: ADC

Description	Condition	Min	Typ	Max	Unit
Full-scale input signal	0 dBFS digital output level		1.6 * V_{DD}		V_{PP}
Signal to noise ratio	A-weighted		90		dB
Dynamic range	ADC DRE enabled, A-weighted		105		dB
Total harmonic distortion plus noise	-1 dBFS ADC output level		-85		dB
Power supply rejection ratio	20 Hz to 2 kHz 2 kHz to 20 kHz	70 50			dB

Table 10: Electrical Characteristics: DAC

Description	Condition	Min	Typ	Max	Unit
Full-scale output signal	0 dBFS digital input level		1.6 * V_{DD}		V_{PP}
Signal to noise ratio	A-weighted		100		dB
Dynamic range	DAC DRE enabled, A-weighted		110		dB
Total harmonic distortion plus noise	-1 dBFS digital input level		-90		dB
Power supply rejection ratio	20 Hz to 2 kHz 2 kHz to 20 kHz	70 50			dB

Table 11: Electrical Characteristics: Headphone Amplifier

Description	Condition	Min	Typ	Max	Unit
Full-scale output signal	No load		1.6 * V_{DD}		V_{PP}
DC output offset	−30 dB gain			250	µV

Description	Condition	Min	Typ	Max	Unit
Maximum output power per channel	V_{DD} = 1.8 V, THD < 0.1 %, R_{LOAD} = 16 Ω, 1 kHz		27		mW_{RMS}
	V_{DD} = 2.5 V, THD < 0.1 %, R_{LOAD} = 16 Ω, 1 kHz		57		mW_{RMS}
Quiescent current per channel				150	µA
Load resistance		13	16		Ω
Load capacitance				500	pF
Load inductance				400	µH
Frequency Response	20 Hz to 20 kHz	-0.5		+0.5	dB
Signal to noise ratio	V_{DD} = 1.8 V, 0 dB gain A-weighted		98		dB
	V_{DD} = 2.5 V, 0 dB gain A-weighted		100		dB
Output noise level	20 Hz to 20 kHz, < -20 dB gain			2.5	$µV_{RMS}$
Total harmonic distortion plus noise	V_{DD} = 1.8 V, R_{LOAD} = 32 Ω, -5 dBFS, 1 kHz		−88		dB
Channel separation [3]	V_{DD} = 1.8V, R_{LOAD} = 32 Ω, 1 kHz		-110		dB
Programmable gain		−57		6	dB
Gain step size			1.5		dB
Absolute gain accuracy	0 dB @ 1 kHz	−0.5		0.5	dB
Left/right gain mismatch	20 Hz to 20 kHz	−0.1		0.1	dB
Gain step error	20 Hz to 20 kHz	−0.1		0.1	dB
Amplitude ripple	20 Hz to 20 kHz	−0.5		0.5	dB
Mute attenuation [2]			−70		dB
Power supply rejection ratio	20 Hz to 2 kHz 2 kHz to 20 kHz	70 50			dB

Table 12: Electrical Characteristics: Output Amplifier

Description	Condition	Min	Typ	Max	Unit
Full-scale input signal	0 dBFS output from the DAC		1.6 * V_{DD}		VPP
Programmable gain		−1.0		0	dB
Gain step size			0.5		dB
Absolute gain accuracy	0 dB @ 1 kHz	-0.5		0.5	dB
Amplitude ripple	20 Hz to 20 kHz	-0.5		0.5	dB
Power supply rejection ratio	20 Hz to 2 kHz 2 kHz to 20 kHz	90 70			dB

Table 13: Electrical Characteristics: Input Filters

Description	Condition	Min	Typ	Max	Unit
Pass band				0.45 * F_S	Hz
Pass band ripple	Voice mode Music mode			±0.3 ±0.1	dB
Stop band	F_S ≤ 48 kHz F_S = 88.2 kHz or 96 kHz	0.56 * F_S		7 * F_S 3.5 * F_S	Hz
Stop band attenuation	Voice mode Music mode	70 55			dB
Group delay	Voice mode Music mode F_S = 88.2 kHz or 96 kHz		4.3 / F_S 18 / F_S 9 / F_S		s
Gain step size			0.75		dB
Programmable gain		-83.25		12	dB

Table 14: Electrical Characteristics: Automatic Level Control

Description	Condition	Min	Typ	Max	Unit
Attack rate	F_S = 48 kHz	1.6		6500	dB/s
Release rate	F_S = 48 kHz	1.6		1675	dB/s
Hold time	F_S = 48 kHz	1.3		42300	ms
Maximum threshold		−94.5		0	dBFS
Minimum threshold		−94.5		0	dBFS
Noise threshold		−94.5		0	dBFS
Threshold step size			1.5		dB
Maximum overall gain		0		90	dB
Maximum overall attenuation		0		90	dB
Maximum analog gain		0		36	dB
Minimum analog gain		0		36	dB
Gain step size			1.5		dB

Table 15: Electrical Characteristics: DAC Filter Specifications

Description	Conditions	Min	Typ	Max	Unit
Pass band				0.45 * F_S	Hz
Pass band ripple	Voice mode Music mode			±0.3 ±0.1	dB
Stop band	$F_S \leq 48$ kHz F_S = 88.2 kHz or 96 kHz	0.56 * F_S		7 * F_S 3.5 * F_S	Hz
Stop band attenuation	Voice mode Music mode	70 55			dB
Group delay	Voice mode Music mode F_S = 88.2 kHz or 96 kHz		4.3 / F_S 18 / F_S 9 / F_S		s
Group delay variation	20 Hz to 20 kHz		1		µs
Left/right channel group delay mismatch			2		µs
Gain step size			0.75		dB
Programmable gain		-83.25		108	dB

Table 16: Electrical Characteristics: High-Pass Filter (Input and Output, ADC in High-Power Mode)

out_1_voice_en / in_1_voice_en	out_1_voice_hpf_corner / in_1_voice_hpf_corner	out_1_audio_hpf_corner/ in_1_audio_hpf_corner	SR Sample Rate (kHz)										
			8	11.025	12	16	22.05	24	32	44.1	48	88.2	96
0		00	0.33	0.46	0.5	0.67	0.92	1	1.33	1.84	2	3.68	4
		01	0.67	0.92	1	1.33	1.84	2	2.67	3.68	4	7.35	8
		10	1.33	1.84	2	2.67	3.68	4	5.33	7.35	8	14.7	16
		11	2.67	3.68	4	5.33	7.35	8	10.67	14.7	16	29.4	32
1	000		2.5	3.45	3.75	5	6.89	7.5	10	Voice HPF not available for sample rates above 32 kHz.			
	001		25	34.5	37.5	50	68.9	75	100				
	010		50	68.9	75	100	137.8	150	200				
	011		100	137.8	150	200	275.6	300	400				
	100		150	206.7	225	300	413.4	450	600				
	101		200	275.6	300	400	551.3	600	800				
	110		300	413.4	450	600	826.9	900	1200				
	111		400	551.3	600	800	1102.5	1200	1600				

Table 17: High-Pass Filter Settings (ADC in Low-Power Mode)

in_1_voice_en out_1_voice_en	in_1_voice_hpf_corner out_1_voice_hpf_corner	in_1_audio_hpf_corner out_1_audio_hpf_corner.	SR Sample Rate (kHz)										
			8	**11.025**	**12**	**16**	**22.05**	**24**	**32**	**44.1**	**48**	**88.2**	**96**
0		00	0.33	0.46	0.5	0.67	0.92	1	32 kHz sample rate not available in Low-Power mode	1.84	2	88.2 kHz and 96 kHz sample rates not available in Low-Power mode	
		01	0.67	0.92	1	1.33	1.84	2		3.68	4		
		10	1.33	1.84	2	2.67	3.68	4		7.35	8		
		11	2.67	3.68	4	5.33	7.35	8		14.7	16		
1	000		2.5	In low-power mode, the voice HPF is only available at a sample rate of 8 kHz									
	001		25										
	010		50										
	011		100										
	100		150										
	101		200										
	110		300										
	111		400										

Table 18: Electrical Characteristics: 5-Band Equalizer

FS (kHz)	Center Frequency (Hz) At Programmed Setting				
	Band 1	**Band 2**	**Band 3**	**Band 4**	**Band 5**
8	0	99	493	1528	4000
11.025	0	136	680	2106	5512
12	0	148	740	2293	6000
16	0	96	440	2128	8000
22.05	0	133	607	2933	11025
24	0	145	660	3191	12000
32	0	95	418	1797	16000
44.1	0	131	576	2386	22050
48	0	143	627	2596	24000
88.2	Not available				
96					

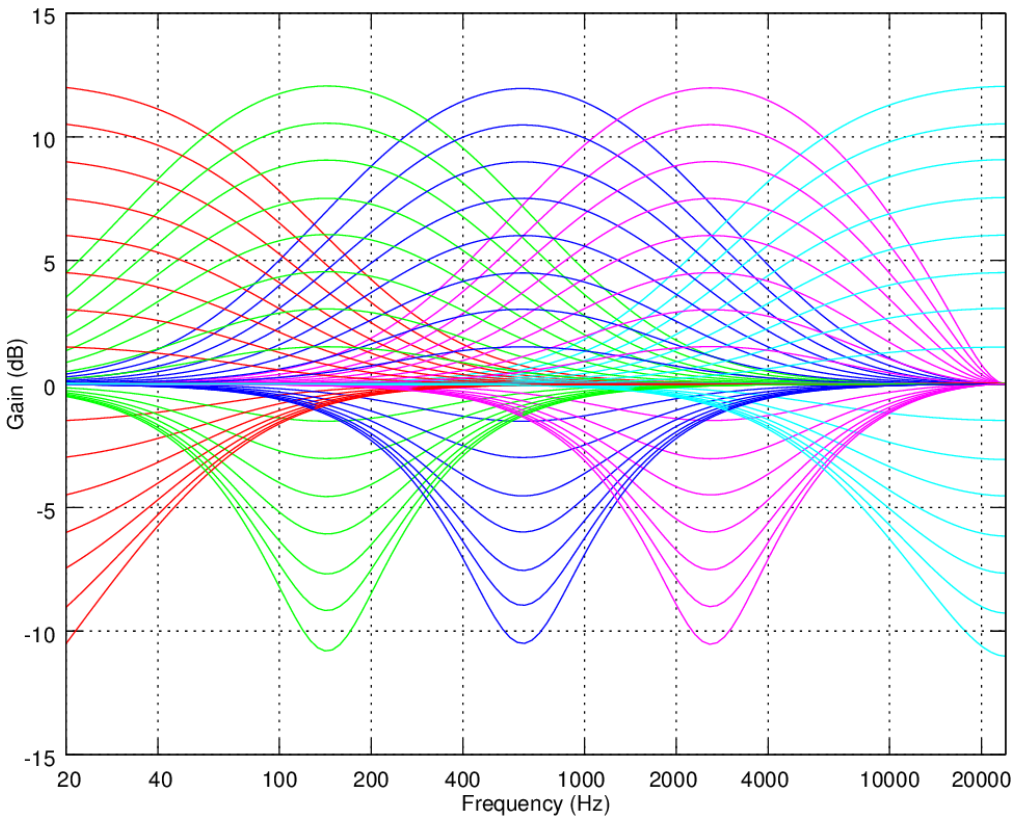


Figure 4: 5-Band Equalizer Response at 48 kHz

Table 19: PLL Mode

Description	Conditions	Min	Typ	Max	Unit
MCLK input jitter	Absolute jitter (rms) (Note 1)			540	ps
MCLK input frequency	Normal mode	2		54	MHz
SRM tracking range	DAI slave mode WCLK frequency variation	-4		4	%
SRM tracking rate	DAI slave mode WCLK drift rate			54	ppm/s

Note 1 Jitter in the 100 Hz to 40 kHz band

Table 20: Bypass Mode

Description	Conditions	Min	Typ	Max	Unit
MCLK input jitter	Absolute jitter (rms) (Note 1)			540	ps
MCLK input frequency	F_S = 11.025, 22.05, 44.1, 88.2 kHz F_S = 8, 12, 16, 24, 32, 48, 96 kHz		11.2896 12.288		MHz

Note 1 Jitter in the 100 Hz to 40 kHz band

Table 21: Tone Generator

Description	Conditions	Min	Typ	Max	Unit
Single-tone frequency	F_S = 8, 12, 16, 24, 32, 48, 96 kHz F_S = 11.025, 22.05, 44.1, 88.2 kHz	1 1		12000 11025	Hz
Single-tone frequency step	F_S = 8, 12, 16, 24, 32, 48, 96 kHz F_S = 11.025, 22.05, 44.1, 88.2 kHz		0.18 0.17		Hz
Dual-tone modulation frequency A			697 770 852 941		Hz
Dual-tone modulation frequency B			1209 1336 1477 1633		Hz
Output signal level			0		dBFS
On/off pulse duration		10		2000	ms
On/off pulse step size	10 ms to 200 ms duration 200 ms to 2000 ms duration		10 50		ms
On/off pulse repeat	Programmable Continuous		1, 2, 3, 4, 5, 6 ∞		Cycles

8 Digital Interfaces

Table 22: I/O Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	SCL, SDA, MCLK, BCLK, WCLK, DATIN, DATOUT, AD Input HIGH voltage		0.7 * V_{DD_IO}			V
V_{IL}	SCL, SDA, MCLK, BCLK, WCLK, DATIN, DATOUT Input LOW voltage				0.3 * V_{DD_IO}	V
V_{OL}	SDA, nIRQ Output LOW voltage	I_{OUT} = 3 mA			0.24	V
V_{OH}	DMIC1CLK Output HIGH voltage		0.7 * $V_{MICBIAS1}$			V
V_{OL}	DMIC1CLK Output HIGH voltage				0.3 * $V_{MICBIAS1}$	V
V_{IH}	DMIC1IN Input HIGH voltage		0.7 * $V_{MICBIAS1}$			V
V_{IL}	DMIC1IN Input LOW voltage				0.3 * $V_{MICBIAS1}$	V
V_{OH}	DMIC2CLK Output HIGH voltage		0.7 * $V_{MICBIAS2}$			V
V_{OL}	DMIC2CLK Output LOW voltage				0.3 * $V_{MICBIAS2}$	V
V_{IH}	DMIC2IN Input HIGH voltage		0.7 * $V_{MICBIAS2}$			V
V_{IL}	DMIC2IN Input LOW voltage				0.3 * $V_{MICBIAS2}$	V
V_{OH}	HPLDET Output HIGH voltage		0.7 * V_{DD_IO}			V
V_{OL}	HPLDET Ouput LOW voltage				0.3 * V_{DD_IO}	V

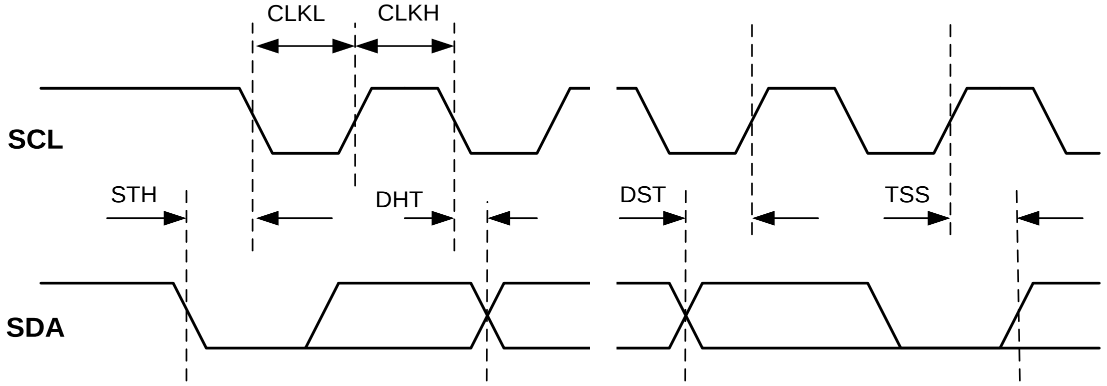


Figure 5: I²C Bus Timing

Table 23: I²C Control Bus (VDD_IO = 1.8 V)

Parameter	Description	Conditions	Min	Typ	Max	Unit
	Bus free time STOP to START		500			ns
	Bus line capacitive load				150	pF
Standard/Fast Mode						
	SCL clock frequency		0		1000	kHz
	Start condition setup time		260			ns
STH	Start condition hold time		260			ns
CLKL	SCL low time		500			ns
CLKH	SCL high time		260			ns
	SCL rise/fall time	Input requirement			1000	ns
	SDA rise/fall time	Input requirement			300	ns
DST	SDA setup time		50			ns
DHT	SDA hold time		0			ns
TSS	Stop condition setup time		260			ns
High-Speed Mode						
	SCL clock frequency		0		3400	kHz
	Start condition setup time		160			ns
STH	Start condition hold time		160			ns
CLKL	SCL low time		160			ns
CLKH	SCL high time		60			ns
	SCL rise/fall time	Input requirement			160	ns
	SDA rise/fall time	Input requirement			160	ns
DST	SDA setup time		10			ns
DHT	SDA hold time		0			ns
TSS	Stop condition setup time		160			ns

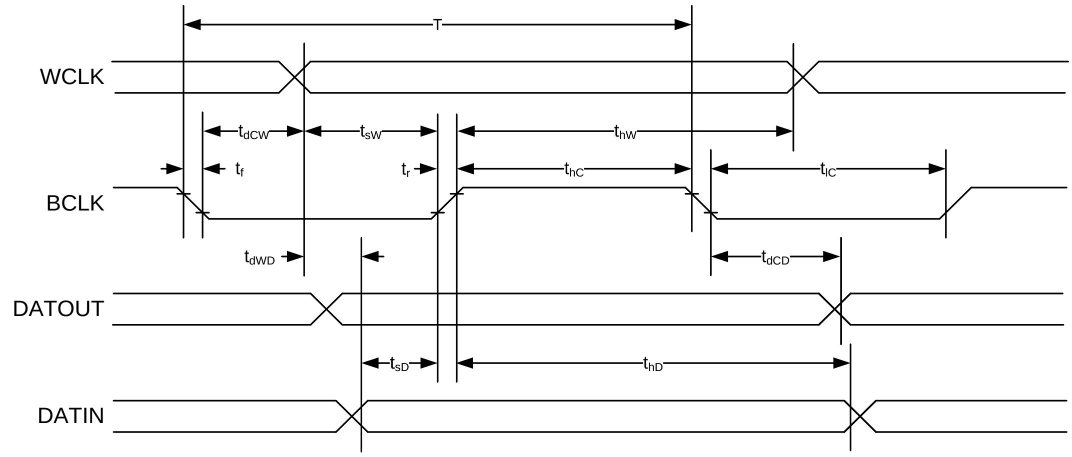


Figure 6: DAI Timing Diagram

NOTE
Diagram shown is valid for all modes except DSP. For DSP mode the BCLK signal is inverted

Table 24: DAI Timing (I^2S/DSP in Master/Slave Mode)

Parameter	Description	Conditions (VDD_IO = 1.8 V)	Min	Typ	Max	Unit
	Input impedance	DC impedance > 10 MΩ	300 1.0		 2.5	Ω pF
T	BCLK period		75			ns
t_r	BCLK rise time				8	ns
t_f	BCLK fall time				8	ns
t_{hC}	BCLK high period		40 %		60 %	T
t_{lC}	BCLK low period		40 %		60 %	T
t_{dCW}	BCLK to WCLK delay		-30 %		+30 %	T
t_{dCD}	BCLK to DATOUT delay		-30 %		+30 %	T
t_{hW}	WCLK high time	DSP mode	100 %			T
		Non-DSP mode	Word length (Note 1)			T
t_{lW}	WCLK low time	DSP mode	100 %			T
		Non-DSP mode	Word length (Note 2)			T
t_{sW}	WCLK setup time	Slave mode	7			ns
t_{hW}	WCLK hold time	Slave mode	2			ns
t_{sD}	DATIN setup time		7			ns
t_{hD}	DATIN hold time		2			ns
t_{dWD}	DATOUT to WCLK delay		DATOUT is synchronized to BCLK			

Note 1 WCLK must be high for at least the word length number of BCLK periods

Note 2 WCLK must be low for at least the word length number of BCLK periods

9 Functional Description

DA7218 is a high-performance, low-power audio codec optimized for use in headsets or wearable devices.

It contains two analog microphone-to-ADC and/or up to four digital microphone-to-input filter paths, and a DAI for input and output.

DA7218 has single-ended headphone outputs with headphone-detect for use in accessories. The other chip in this family, the DA7217 has differential headphone outputs without headphone-detect, and has been designed for use inside headset devices.

The digital engine input includes a high pass filter, automatic level control (ALC), and level detection. The output stage has a high pass filter, a 5-band EQ, and a 5-stage biquad filter.

The digital engine also has a dynamic range extension (DRE) block, and a tone generator that supports dual tone multi-frequency (DTMF).

The flexible digital mixer allows any or all of the seven inputs (four input filters, the tone generator, and DAI left and right inputs) to be routed to any or all of the six digital outputs (left and right output filters, and DAI outputs). There is an independently programmable gain on each of the 42 possible paths.

9.1 Device Operation

9.1.1 Power Modes

The DA7218 codec has two operating modes:

STANDBY – The device is asleep with all internal circuits disabled, but all register states are retained.

ACTIVE – The device is awake and ready to perform audio functions. Blocks can be enabled as required.

9.1.1.1 STANDBY Mode

In STANDBY mode, both the reference voltage generator and the reference oscillator are shut down so no audio functions are possible. All audio paths must be shut down before entering STANDBY mode (system_active = 0), as the transition to STANDBY mode is immediate and is not pop-free.

9.1.1.2 ACTIVE Mode

To put the device in ACTIVE mode, write system_active = 1. On entering ACTIVE mode, the reference voltage generator and reference oscillator are automatically enabled.

9.2 Input Paths

9.2.1 Microphone Inputs

The DA7218 analog inputs consist of two independent signal chains, each including two amplifiers and an ADC as shown in Figure 7.

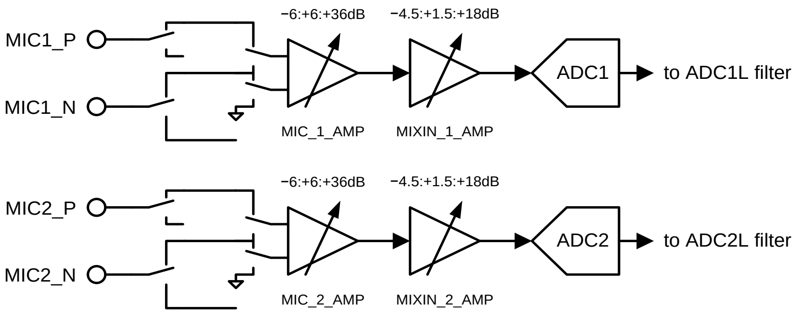


Figure 7: Analog Inputs Block Diagram

The two microphone amplifiers can be configured in

- fully differential mode for improved common-mode noise rejection
- pseudo-differential mode
- single-ended mode (MIC1|2_P or MIC1|2_N)

All configurations are illustrated in Figure 8.

Digital microphone connection details are described in section 9.2.1.3.

9.2.1.1 Microphone Biases

The DA7218 codec has two independently controlled microphone bias outputs.

Low Noise (Normal) Mode

Each bias output can be independently programmed from 1.6 V to 3.0 V in 0.2 V steps using micbias_1_level and micbias_2_level in MICBIAS_CTRL.

Each microphone bias level can only be changed while the associated MICBIAS circuit is disabled (micbias_1_en = 0 for MICBIAS1 or micbias_2_en = 0 for MICBIAS2).

Low-Power Mode

Both microphone bias circuits can also be used as low-power voltage sources optimized for always-on microphones. In low-power mode the output voltage is fixed at 1.2 V. Low-power mode is enabled by setting the micbias_1_lp_mode = 1 in the MICBIAS_CTRL register.

MICBIAS1 is enabled by setting micbias_1_en = 1.

The second microphone bias circuit (MICBIAS2) is controlled in the same way.

Low-power mode can only be changed while the MICBIAS circuits are disabled (micbias_1_en = 0 for low-power mode on MICBIAS1, and micbias_2_en = 0 for low-power mode on MICBIAS2).

Table 25: Microphone Bias Settings

micbias_1_level micbias_2_level	Output Voltage in Low-Noise Mode micbias_1|2_lp_mode = 0 (V)	Output Voltage in Low-Power Mode micbias_1|2_lp_mode = 1 (V)
000	1.6	1.2
001	1.8	
010	2.0	
011	2.2	
100	2.4	
101	2.6	
110	2.8	
111	3.0	

9.2.1.2 Microphone Amplifier

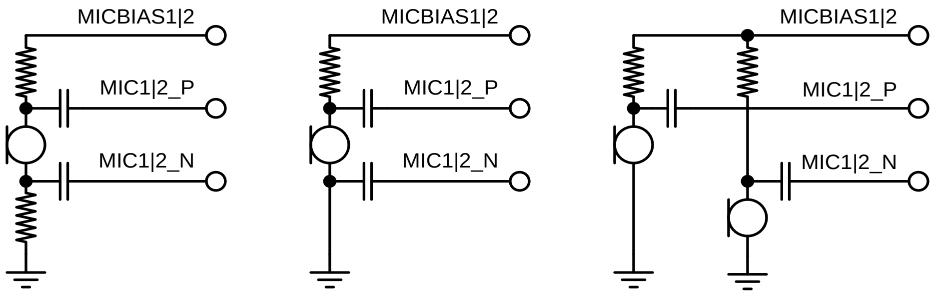


Figure 8: Analog Microphone Configurations

The configuration of the first microphone amplifier (MIC_1_CTRL) is specified using mic_1_amp_in_sel. It is enabled by setting mic_1_amp_en = 1, and is muted by setting mic_1_amp_mute_en = 1.

The gain of the amplifier can be set in the range of –6 dB to +36 dB in 6 dB steps using mic_1_amp_gain (see Table 26 :).

The second microphone amplifier (MIC_2_CTRL) is controlled in the same way.

Table 26 : MIC_1_GAIN and MIC_2_GAIN Gain Settings

mic_1_amp_gain mic_2_amp_gain	Amplifier Gain (dB)
000	-6
001	0
010	6
011	12
100	18
101	24
110	30
111	36

9.2.1.3 Digital Microphones

The DA7218 can support up to four digital microphones by reusing the MIC1_P and MIC_2P pins as clock outputs, and the MIC1_N and MIC_2N pins as digital data inputs.

The IO voltage level of DMIC1 is set by the voltage present on MICBIAS1 and the IO voltage level of DMIC2 is set by the voltage present on MICBIAS2. This voltage can be either an output of the MICBIAS LDO or, for minimum power consumption, the IO voltage of the DMIC can be connected as an input on the appropriate MICBIAS pin.

The first DMIC input is controlled using the DMIC_1_CTRL register. The left channel is enabled using dmic_1l_en and the right channel using dmic_1r_en. The DMIC clock rate can be set using dmic_1_clk_rate.

DMIC_1 data is sampled on both the rising and the falling edges of the DMIC clock. The register field dmic_1_data_sel determines which of the rising and the falling edges corresponds to the left channel, and which to the right.

The register field dmic_1_samplephase controls whether the sample point for the DMIC data is on the DMICCLK edges (dmic_1_samplephase = 0) or at the midpoint between the DMICCLK edges (dmic_1_samplephase = 1).

The second DMIC input is controlled in the same way using DMIC_2_CTRL.

Table 27: Digital Microphone Control Bits

Function	Register Bits	Bit Setting	
		0	1
Digital microphone enable/disable	dmic_1r_en dmic_1l_en dmic_2l_en dmic_2r_en	DMIC is disabled	DMIC is enabled
Digital microphone clock rate	dmic_l_clk_rate dmic_2_clk_rate	3.072 MHz or 2.8224 MHz	1.536 MHz or 1.4112 MHz
Digital microphone sample phase	dmic_1_samplephase dmic_2_samplephase	Data sampled on the clock edges	Data sampled between the clock edges
Digital microphone left/right data selection	dmic_1_data_sel dmic_2_data_sel	Rising edge = left Falling edge = right	Rising edge = right Falling edge = left

9.2.1.4 Input Amplifiers

The two input amplifiers provide an additional gain stage between the microphone amplifiers (see section 9.2.1.2 and Figure 7) and the ADC inputs. The input amplifier (MIXIN_1_CTRL) is enabled by setting mixin_1_amp_en = 1.

The gain can be set in the range of –4.5 dB to +18 dB in 1.5 dB steps using MIXIN_1_GAIN. It is recommended that gain updates be ramped through all intermediate values by setting mixin_1_amp_ramp_en = 1. This ramp setting overrides the settings of mixin_1_amp_zc_en.

As an alternative to zero-cross synchronization, gain updates can be synchronized with signal zero-crossings by setting mixin_1_amp_zc_en = 1. If no zero-crossing is detected within the timeout period of approximately 100 ms, the update is applied unconditionally.

The amplifier can be muted using mixin_1_amp_mute_en.The single input to the first amplifier can be deselected by setting mixin_1_mix_sel = 0.

The second input amplifier (MIXIN_2_CTRL) is controlled in the same manner as MIXIN_1_CTRL.

Table 28: MIXIN_1_GAIN and MIXIN_2_GAIN Gain Settings

mixin_1_amp_gain mixin_2_amp_gain	Amplifier Gain (dB)
0000	-4.5
0001	-3.0
0010	-1.5
0011	0.0
0100	1.5
0101	3.0
0110	4.5
0111	6.0
1000	7.5
1001	9.0
1010	10.5

mixin_1_amp_gain mixin_2_amp_gain	Amplifier Gain (dB)
1011	12.0
1100	13.5
1101	15.0
1110	16.5
1111	18.0

9.2.2 Analog to Digital Converters

The DA7218 codec contains the stereo audio analog to digital converters (ADCs). These can run either in low-power mode for always-on applications, or in high performance mode for other applications.

Each ADC is automatically enabled whenever the input filters are enabled and digital microphones are not enabled.

Not all sample rates are supported in all modes. Table 29 describes which sample rates are supported in each mode.

Table 29: Supported Sample Rates in Different Modes

Sample Rate (kHz)	Low Power Mode adc_lp_mode = 1		Normal Mode adc_lp_mode = 0	
	voice_en = 1	voice_en = 0	voice_en = 1	voice_en = 0
8.0	Supported	Supported	Supported	Supported
11.025/12.0	Not supported	Supported	Supported	Supported
16.0	Not supported	Supported	Supported	Supported
22.050/24.0	Not supported	Supported	Supported	Supported
32.0	Not supported	Not supported	Supported	Supported
44.100/48.0	Not supported	Supported	Not supported	Supported
88.200/96.0	Not supported	Not supported	Not supported	Supported

9.2.2.1 High Performance Mode

In normal (high performance) mode (adc_lp_mode = 0), the ADCs are clocked at a fixed rate of either 3.072 MHz or 2.8224 MHz, depending on the required input sample rate (SR1).

9.2.2.2 Low-Power Mode

The low-power mode of operation is designed for always-on applications. In low-power mode, the ADCs are clocked at half the 'normal' (high-performance) rate, that is, at either 1.5360 MHz or 1.4112 MHz. Low-power mode is set in both ADCs by setting adc_lp_mode = 1. In this mode there is a small increase in distortion.

9.2.2.3 Anti-Alias Filters

The anti-alias filters at the front-end of the ADC are enabled by default. The anti-alias filters can be disabled to save power by setting adc_1_aaf_en = 0 for channel 1, or adc_2_aaf_en = 0 for channel 2.

9.3 Digital Engine

The DA7218 chip contains a digital engine that performs the signal processing and also provides overall system control. Within the digital engine, all seven possible input signals can be mixed and output to any of the six possible outputs. See Figure 9 for a visual representation of this.

The output signals from either of the two ADCs or any of the four digital microphones are passed to the input filter block. The filter block includes a high-pass filter for wind noise suppression, an automatic level control, and input level detection.

The signals from the input filters are sent to the digital mixer where they can be combined with signals from the tone generator and the DAI, and routed to the output filters and the DAI. The output filters contain a high-pass filter for DC offset removal, a fixed 5-band equalizer, and a flexible 5-stage biquad filter to adjust the sound of the output signals.

There is also a sidetone path that can take one signal from either the ADCs or the digital microphones and perform filtering using three biquad sections before passing the signal straight to the output filters.

The digital engine contains a DRE module that can be used to automatically swap analog and digital gains on the input and output signal paths in order to maximize the dynamic range of the codec.

Finally a system controller module is included to ensure correct sequencing of the events required to bring up and shut down signal paths without creating pops and clicks.

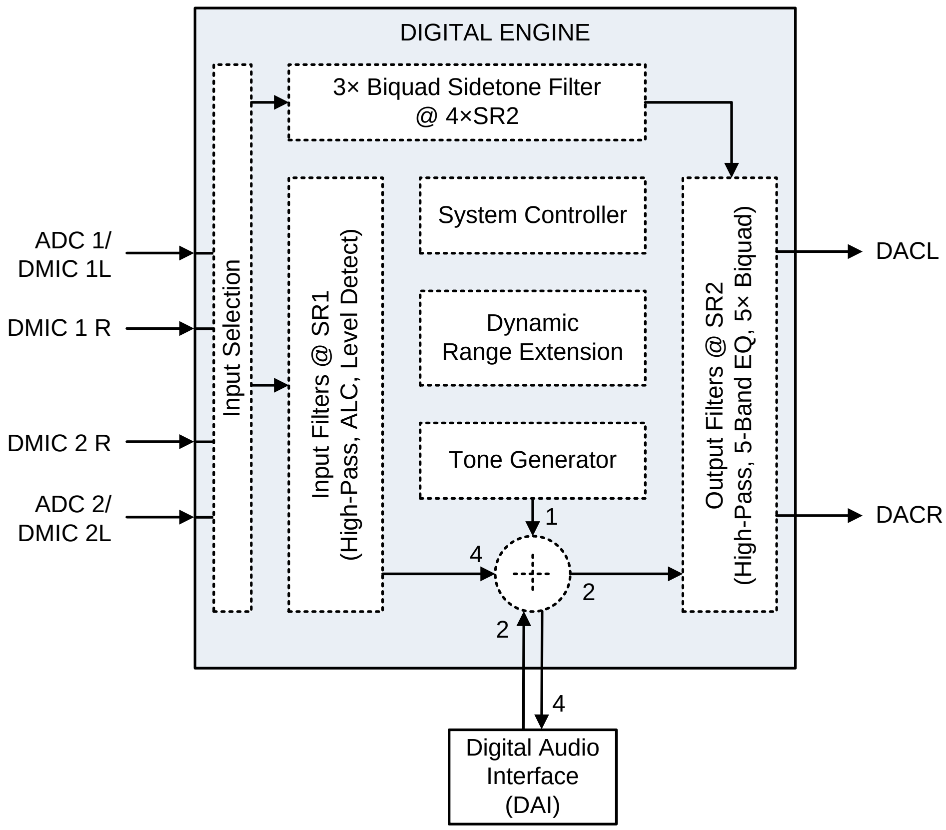


Figure 9: Digital Engine Block Diagram

9.3.1 Input Processing

9.3.1.1 Input Filters

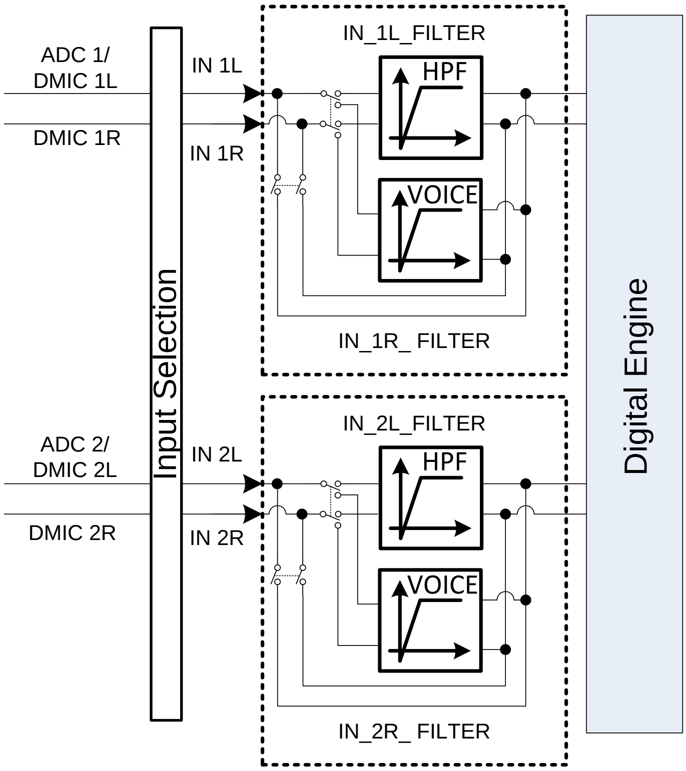


Figure 10: Input Filters Block Diagram

There are two stereo pairs of input filters (IN_1L_FILTER_CTRL and IN_1R_FILTER_CTRL, and IN_2L_FILTER_CTRL and IN_2R_FILTER_CTRL) that can be used to process signals from either the two mono ADCs, or from the two stereo digital microphone inputs. The input (ADC or DMIC) to the input filters is selected using dmic_1l_en (or dmic_1r_en) and dmic_2l_en (or dmic_2r_en).

If an ADC input is selected, the analog part of the ADC is enabled whenever the DMIC has not been enabled and the connected input filter has been enabled using one of the filter enabling bits (in_1l_filter_en, in_1r_filter_en, in_2l_filter_en, and in_2r_filter_en).

Left and right channels of the two input filters can be controlled independently. The left channel of the first input filter is enabled using in_1l_filter_en. It is muted using in_1l_mute_en and gain-ramping is enabled using in_1l_ramp_en. The gain can be set in the range of –83.25 dB to +12 dB in +0.75 dB steps using in_1l_digital_gain.

The right channel and the second input filter channels are all controlled in the same way.

Table 30: IN_FILT Digital Gain Settings

in_1l_digital_gain, in_1r_digital_gain, in_2l_digital_gain in_2r_digital_gain Setting		Gain (dB)	in_1l_digital_gain, in_1r_digital_gain, in_2l_digital_gain, in_2r_digital_gain Setting		Gain (dB)	in_1l_digital_gain, in_1r_digital_gain, in_2l_digital_gain, in_2r_digital_gain Setting		Gain (dB)
Binary	Hex		Binary	Hex		Binary	Hex	
0000000	0x00	-83.25	0101011	0x2B	-51	1010110	0x56	-18.75
0000001	0x01	-82.5	0101100	0x2C	-50.25	1010111	0x57	-18
0000010	0x02	-81.75	0101101	0x2D	-49.5	1011000	0x58	-17.25
0000011	0x03	-81	0101110	0x2E	-48.75	1011001	0x59	-16.5
0000100	0x04	-80.25	0101111	0x2F	-48	1011010	0x5A	-15.75
0000101	0x05	-79.5	0110000	0x30	-47.25	1011011	0x5B	-15
0000110	0x06	-78.75	0110001	0x31	-46.5	1011100	0x5C	-14.25
0000111	0x07	-78	0110010	0x32	-45.75	1011101	0x5D	-13.5
0001000	0x08	-77.25	0110011	0x33	-45	1011110	0x5E	-12.75
0001001	0x09	-76.5	0110100	0x34	-44.25	1011111	0x5F	-12
…Continuing in 0.75 dB steps until…								
0011110	0x1E	-60.75	1001001	0x49	-28.5	1110100	0x74	3.75
0011111	0x1F	-60	1001010	0x4A	-27.75	1110101	0x75	4.5
0100000	0x20	-59.25	1001011	0x4B	-27	1110110	0x76	5.25
0100001	0x21	-58.5	1001100	0x4C	-26.25	1110111	0x77	6
0100010	0x22	-57.75	1001101	0x4D	-25.5	1111000	0x78	6.75
0100011	0x23	-57	1001110	0x4E	-24.75	1111001	0x79	7.5
0100100	0x24	-56.25	1001111	0x4F	-24	1111010	0x7A	8.25
0100101	0x25	-55.5	1010000	0x50	-23.25	1111011	0x7B	9
0100110	0x26	-54.75	1010001	0x51	-22.5	1111100	0x7C	9.75
0100111	0x27	-54	1010010	0x52	-21.75	1111101	0x7D	10.5
0101000	0x28	-53.25	1010011	0x53	-21	1111110	0x7E	11.25
0101001	0x29	-52.5	1010100	0x54	-20.25	1111111	0x7F	12
0101010	0x2A	-51.75	1010101	0x55	-19.5			

9.3.1.2 High-Pass Filter

The DA7218 contains two stereo input high-pass filters (HPFs). The first filter is controlled using IN_1_HPF_FILTER_CTRL and IN_2_HPF_FILTER_CTRL to remove any DC components from the incoming audio. This filter operates at all sample rates. For this first filter, in music mode in_1_voice_en must be set to 0 and the HPF corner frequency is set using in_1_audio_hpf_corner.

A second high pass filter is available when the sample rate is 32 kHz or lower for voice filtering. This filter is controlled using in_1_voice_en and in_2_voice_en. It has a wider range of corner frequencies to help remove low frequency artefacts such as wind noise.

In voice mode, in_1_voice_en must = 1 in which case the HPF corner frequency is set using in_1_voice_en.

The value of the HPF corner frequency also depends on the input sample rate (SR1) as shown in Table 31 (ADC in high power mode) and Table 32 (ADC in low power mode). Note that when operating in ADC low power mode (adc_lp_mode = 1), the voice filter is only available at a sample rate of 8 kHz. Similarly the audio filter will not operate at sample rates of 32 kHz, 88.2 kHz, or 96 kHz.

The sample rates available in the different ADC power modes are summarized in Table 31 for the ADC in high-power mode (adc_lp_mode = 0), and Table 32 for the ADC in low-power mode (adc_lp_mode = 1).

Table 31: Input High-Pass Filter Settings (ADC in High-Power Mode)

in_1_voice_en out_1_voice_en	in_1_voice_hpf_corner out_1_voice_hpf_corner	in_1_audio_hpf_corner out_1_audio_hpf_corner	Sample Rate (kHz)										
			8	**11.025**	**12**	**16**	**22.05**	**24**	**32**	**44.1**	**48**	**88.2**	**96**
0		00	0.33	0.46	0.5	0.67	0.92	1	1.33	1.84	2	3.68	4
		01	0.67	0.92	1	1.33	1.84	2	2.67	3.68	4	7.35	8
		10	1.33	1.84	2	2.67	3.68	4	5.33	7.35	8	14.7	16
		11	2.67	3.68	4	5.33	7.35	8	10.67	14.7	16	29.4	32
1	000		2.5	3.45	3.75	5	6.89	7.5	10	Voice HPF not available for sample rates above 32 kHz.			
	001		25	34.5	37.5	50	68.9	75	100				
	010		50	68.9	75	100	137.8	150	200				
	011		100	137.8	150	200	275.6	300	400				
	100		150	206.7	225	300	413.4	450	600				
	101		200	275.6	300	400	551.3	600	800				
	110		300	413.4	450	600	826.9	900	1200				
	111		400	551.3	600	800	1102.5	1200	1600				

Table 32: Input High-Pass Filter Settings (ADC in Low-Power Mode)

in_1_voice_en out_1_voice_en	in_1_voice_hpf_corner out_1_voice_hpf_corner	in_1_audio_hpf_corner out_1_audio_hpf_corner.	Sample Rate (kHz)										
			8	**11.025**	**12**	**16**	**22.05**	**24**	**32**	**44.1**	**48**	**88.2**	**96**
0		00	0.33	0.46	0.5	0.67	0.92	1	32 kHz sample rate not available in low-power mode	1.84	2	88.2 kHz and 96 kHz sample rates not available in low-power mode	
		01	0.67	0.92	1	1.33	1.84	2		3.68	4		
		10	1.33	1.84	2	2.67	3.68	4		7.35	8		
		11	2.67	3.68	4	5.33	7.35	8		14.7	16		
1	000		2.5	In low-power mode, the voice HPF is only available at a sample rate of 8 kHz									
	001		25										
	010		50										
	011		100										
	100		150										
	101		200										
	110		300										
	111		400										

9.3.1.3 Automatic Level Control

For improved sound recordings of signals with a large volume range, the DA7218 offers a fully-configurable automatic recording level control (ALC) for microphone inputs. This is enabled via the ALC_CTRL1, and can be enabled independently on any of the four input channels. The ALC monitors the digital signal after the ADC and adjusts the microphones' analog and digital gain to maintain a constant recording level, regardless of the analog input signal level.

Operation of ALC is illustrated in Figure 11. When the input signal volume is high, the ALC system will reduce the overall gain until the output volume is below the specified maximum value. When the input signal volume is low, the ALC will increase the gain until the output volume increases above the specified minimum value. If the output signal is within the desired signal level (between the specified minimum and maximum levels), the ALC does nothing.

The minimum and the maximum thresholds that trigger a gain change of the ALC are programmed by the alc_threshold_min and alc_threshold_max controls.

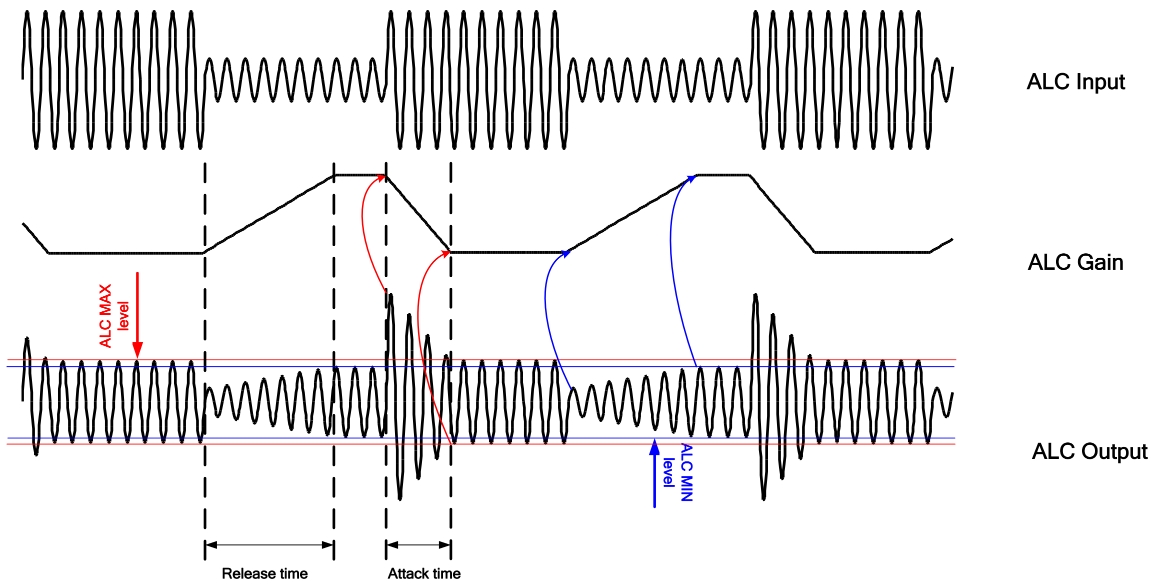


Figure 11: Principle of Operation of the ALC

The ALC can operate in two modes; Digital-Only mode and Hybrid (combined analog and digital gain) mode.

In Digital-Only mode only the digital gain in the ADC is altered. Note that although the ALC is controlling the gain, it does not modify any of the registers in_1l_digital_gain, in_1r_digital_gain, in_2l_digital_gain, or in_2r_digital_gain. These registers are ignored while the ALC is in operation. The minimum and maximum levels of digital gain that can be applied by the ALC are controlled using alc_atten_max and alc_gain_max.

When using analog microphones, Hybrid mode can be enabled using alc_sync_mode. See section 9.3.1.5 for details on ALC calibration in Hybrid mode.

In Hybrid mode, the total gain is made up of an analog gain (which is applied to the microphone amplifiers) and a digital gain, (which is implemented in the filtering stage).The ALC block monitors and controls the gain of the microphone and the ADC. Note that although the ALC is controlling the gain, it does not modify any of the registers mixin_1_amp_gain or mixin_2_amp_gain, nor does it modify any of the digital gain registers in_1l_digital_gain, in_1r_digital_gain, in_2l_digital_gain, or in_2r_digital_gain. These registers are ignored while the ALC is in operation.

Similarly the minimum and maximum levels of analog gain are controlled by alc_ana_gain_min and alc_ana_gain_max. The rates at which the gain is changed are defined by the attack and decay rates in register ALC_CTRL2. When attacking, the gain decreases with alc_attack rate. When decaying, the gain increases with alc_release rate.

Hybrid mode should be used whenever analog microphones are being used. Digital-Only mode should be used whenever digital microphones are being used.

The hold-time is defined by alc_hold in the ALC_CTRL3 register. This controls the length of time that the system maintains the current gain level before starting to decay. This prevents unwanted changes in the recording level when there is a short-lived ‘spike’ in input volume, for example when recording speech.

Typically the attack rate should be much faster than the decay rate. To avoid clipping it is necessary to reduce rapidly increasing waveforms as quickly as possible, whereas fast release times will result in the signal appearing to ‘pump’. The ALC also has an anti-clip function that applies a very fast attack rate when the input signal is close to full-scale. This prevents clipping of the signal by reducing the signal gain at a faster rate than would normally be applied. The anti-clip function is enabled using alc_anticlip_en, and the trigger threshold is set in the range 0.034 dB/F_S to 0.272 dB/F_S using alc_anticlip_step.

A recording noise-gate feature is provided to avoid increasing the gain of the channel when there is no signal, or when only a noise signal is present. Boosting a signal on which only noise is present is known as ‘noise pumping’, the noise-gate prevents this. Whenever the level of the input signal drops below the noise threshold configured in alc_noise, the channel gain remains constant.

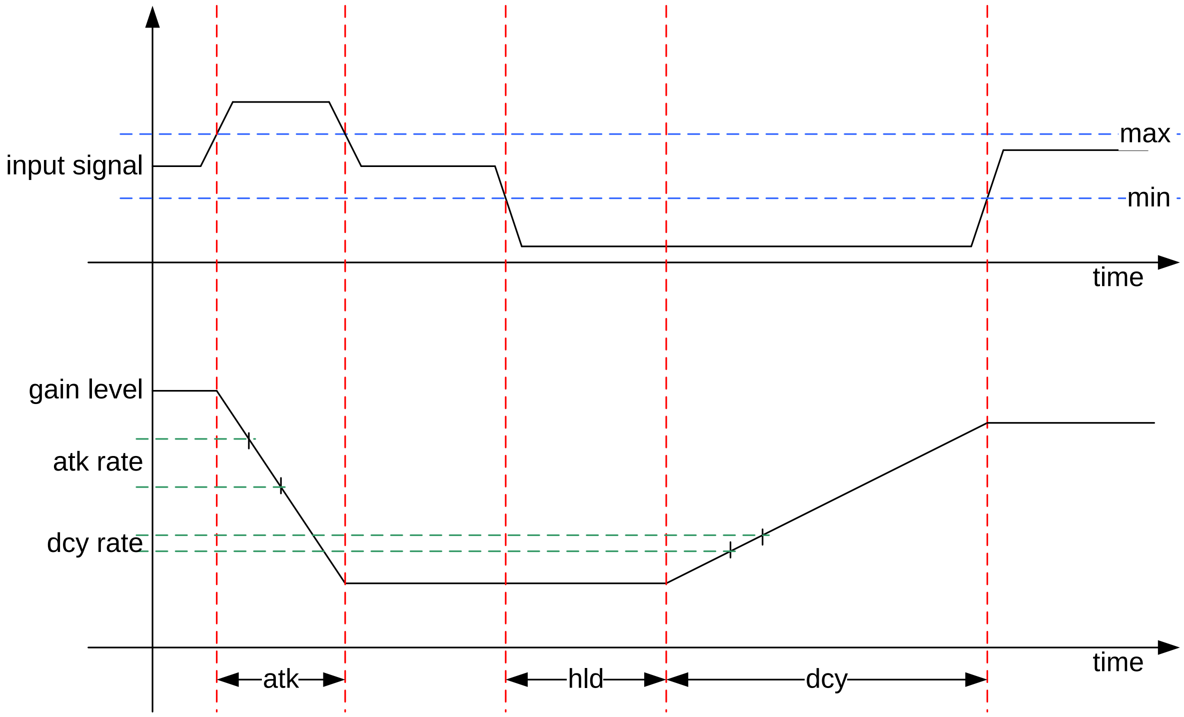


Figure 12: Attack, Delay and Hold Parameters

9.3.1.4 Input Dynamic Range Extension

When using analog microphones, the input dynamic range extension (DRE) automatically swaps the analog and digital gains to maximize the dynamic range at all times.

The DRE block, like the Hybrid-mode ALC, controls both the analog MICAMP gain and the digital gain. However it applies equal and opposite adjustments to analog and digital gains so that total path gain remains constant while the input dynamic range is increased.

DRE can be enabled for either or both ADCs using the ags_enable bits. The trigger level for the DRE can be set in the range of –90 dB to 0 dB in 6 dB steps using ags_trigger. The maximum attenuation that can be applied by the DRE can be set in the range of 0 dB to 36 dB in 6 dB steps using ags_att_max. There is also a timeout of 0.1 s that can be enabled using ags_timeout_en, and a mechanism to prevent clipping that can be enabled using ags_anticlip_en. Note that the input DRE cannot be used with ALC. Only one of these functions can be used at any one time.

9.3.1.5 Automatic Level Control and Input Dynamic Range Extension Calibration

When using the ALC in Hybrid mode or when using the input DRE, the DC offset at the output of the MICAMPs must be compensated for to prevent audible effects when the gains are changed. This compensation is performed automatically if the following sequence is followed:

1. Enable the required MICAMP(s) unmuted.
2. Mute the MICAMP(s). Note that it is important to enable the MICAMPS unmuted before using them in this step.
3. Enable the required MIXIN_1|2_AMP(s) and ADC(s) unmuted.
4. Enable the DAI or set the PC to Freerun mode.
5. Set calib_auto_en to 1 to start the calibration. This bit will clear to 0 once the calibration is complete.
6. Set calib_offset_en to 1.
7. Enable the ALC in Hybrid mode or the DRE. Note that ALC and input DRE are mutually exclusive, and only one should be enabled at any one time.
8. Unmute the MICAMP(s).

9.3.1.6 Level Detection

Level detection can be used to signal to the host processor (via the nIRQ pin) that the input signal has exceeded the threshold level determined by lvl_det_level. Level detection can be enabled on any or all of the four input filter channels using the lvl_det_en bits.

The threshold used for level detection can be programmed in the range of 1/128 full-scale to full-scale using lvl_det_level.

9.3.2 Sidetone Processing

There is a mono, low-latency filter channel between inputs and outputs for implementing a sidetone path. The input signal to any one of the four input channels (from DMIC or ADC) can also be routed to the sidetone channel using sidetone_in_select.

The output from the sidetone channel can be added to left or right (or both) output filters using outfilt_st_1l_src and outfilt_st_1r_src.

The sidetone filter itself contains a three-stage biquad filter that can be used to provide custom filtering of the input signal.

The biquad filter also has a programmable gain stage to adjust the level of the sidetone signal. This is controlled by sidetone_gain, and provides gain in the range -42 dB to +4.5 dB in 1.5 dB steps.

The sidetone path is enabled using sidetone_filter_en. and muted using sidetone_mute_en.

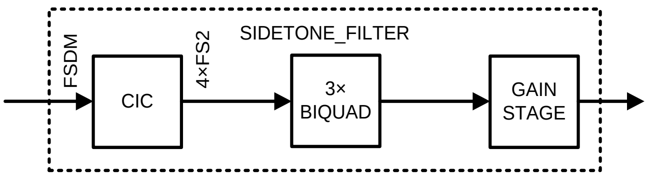


Figure 13: Sidetone Filter Block Diagram

The sidetone biquad filter can be used to provide custom filtering, for example microphone frequency response. Each of the three biquad stages has five 16-bit coefficients a0, a1, a2, b1 and b2 (see Figure 21). For the three stages, the coefficients are numbered a00, a01 etc. as shown in Figure 14:

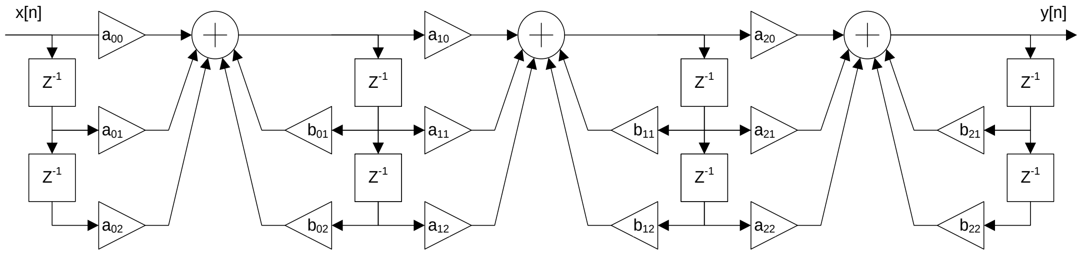


Figure 14: Cascade of Three Biquad Filter Stages

The coefficients are stored using 8-bit registers in a dedicated address space. They are programmed by first writing the coefficient data value to sidetone_biq_3stage_data and then the coefficient address to sidetone_biq_3stage_addr. The address location for each of the coefficients is described in Table 33: Each of the 16-bit coefficients is two's complement values that are programmed in the range of -2 (0x8000) to +2 (0x7FFF). It is the responsibility of the user to ensure that filter transfer function corresponding to the programmed coefficients is stable.

Table 33: Sidetone 3-Stage Biquad Filter Coefficient Address Map

Address	Name	Description
0x00	SIDETONE_BIQ_A00_LO	Lower byte of a00 coefficient for first sidetone biquad stage
0x01	SIDETONE_BIQ_A00_HI	Upper byte of a00 coefficient for first sidetone biquad stage
0x02	SIDETONE_BIQ_A01_LO	Lower byte of a01 coefficient for first sidetone biquad stage
0x03	SIDETONE_BIQ_A01_HI	Upper byte of a01 coefficient for first sidetone biquad stage
0x04	SIDETONE_BIQ_A02_LO	Lower byte of a02 coefficient for first sidetone biquad stage
0x05	SIDETONE_BIQ_A02_HI	Upper byte of a02 coefficient for first sidetone biquad stage
0x06	SIDETONE_BIQ_B01_LO	Lower byte of b01 coefficient for first sidetone biquad stage
0x07	SIDETONE_BIQ_B01_HI	Upper byte of b01 coefficient for first sidetone biquad stage
0x08	SIDETONE_BIQ_B02_LO	Lower byte of b02 coefficient for first sidetone biquad stage
0x09	SIDETONE_BIQ_B02_HI	Upper byte of b02 coefficient for first sidetone biquad stage
0x0A	SIDETONE_BIQ_A10_LO	Lower byte of a10 coefficient for second sidetone biquad stage
0x0B	SIDETONE_BIQ_A10_HI	Upper byte of a10 coefficient for second sidetone biquad stage
0x0C	SIDETONE_BIQ_A11_LO	Lower byte of a11 coefficient for second sidetone biquad stage
0x0D	SIDETONE_BIQ_A11_HI	Upper byte of a11 coefficient for first sidetone biquad stage
0x0E	SIDETONE_BIQ_A12_LO	Lower byte of a12 coefficient for first sidetone biquad stage
0x0F	SIDETONE_BIQ_A12_HI	Upper byte of a12 coefficient for first sidetone biquad stage
0x10	SIDETONE_BIQ_B11_LO	Lower byte of b11 coefficient for first sidetone biquad stage
0x11	SIDETONE_BIQ_B11_HI	Upper byte of b11 coefficient for second sidetone biquad stage
0x12	SIDETONE_BIQ_B12_LO	Lower byte of b12 coefficient for second sidetone biquad stage
0x13	SIDETONE_BIQ_B12_HI	Upper byte of b12 coefficient for second sidetone biquad stage
0x14	SIDETONE_BIQ_A20_LO	Lower byte of a20 coefficient for third sidetone biquad stage
0x15	SIDETONE_BIQ_A20_HI	Upper byte of a20 coefficient for third sidetone biquad stage
0x16	SIDETONE_BIQ_A21_LO	Lower byte of a21 coefficient for third sidetone biquad stage

0x17	SIDETONE_BIQ_A21_HI	Upper byte of a21 coefficient for third sidetone biquad stage
0x18	SIDETONE_BIQ_A22_LO	Lower byte of a22 coefficient for third sidetone biquad stage
0x19	SIDETONE_BIQ_A22_HI	Upper byte of a22 coefficient for third sidetone biquad stage
0x1A	SIDETONE_BIQ_B21_LO	Lower byte of b21 coefficient for third sidetone biquad stage
0x1B	SIDETONE_BIQ_B21_HI	Upper byte of b21 coefficient for third sidetone biquad stage
0x1C	SIDETONE_BIQ_B22_LO	Lower byte of b22 coefficient for third sidetone biquad stage
0x1D	SIDETONE_BIQ_B22_HI	Upper byte of b22 coefficient for third sidetone biquad stage

9.3.3 Tone Generator

The tone generator contains two independent Sine Wave Generators (SWGs). Each SWG can generate a sine wave at a frequency (FREQ) from approximately 1 Hz to 12 kHz according to the programmed 16-bit value:

- FREQ[15:0] = 2^{16} * f_{SWG}/12000, for SR2 = (8, 12, 16, 24, 32, 48,96) kHz
- FREQ[15:0] = 2^{16} * f_{SWG}/11025, for SR2 = (11.025, 22.05, 44.1, 88.2) kHz

The DA7218 should not be programmed with frequency greater than the Nyquist frequency.

Nyquist frequency = SR2/2

For the first SWG, the FREQ value is stored in two 8-bit registers as freq1_u = FREQ[15:8] and freq1_l = FREQ[7:0]. The second SWG frequency is programmed in the same way using freq2_u and freq2_l. The output of the tone generator can come from either of the SWGs, or from a combination of both of them as specified by swg_sel. In addition the tone generator can produce standard Dual Tone Multi-Frequency (DTMF) tones using the two SWGs if dtmf_en = 1 and the required keypad value is programmed in dtmf_reg as shown in Table 34.

Table 34: DTMF Tones Corresponding to dtmf_reg Value

SWG2 Freq (Hz)	SWG1 Frequency (Hz)			
	1209	**1336**	**1477**	**1633**
697	0x1	0x2	0x3	0xA
770	0x4	0x5	0x6	0xB
852	0x7	0x8	0x9	0xC
941	0xE (✳)	0x0	0xF (#)	0xD

The tone generator can produce 1, 2, 3, 4, 8, 16, or 32 beeps, or a continuous beep, as determined by beep_cycles. Each beep has an on period from 10 ms to 2 s as programmed in beep_on_per and an off period from 10 ms to 2 s as programmed in beep_off_per. The tone generator is started by setting the start_stopn bit, and is halted by clearing this bit. If start_stopn is cleared, the tone generator stops at the completion of the current beep cycle or at the next zero-cross if the number of beeps is set to continuous (beep_cycles = 110 or = 111). The start_stopn bit is automatically cleared once the programmed number of beep cycles has been completed.

The tone generator can also be used to produce an S-ramp by setting swg_sel to 0x03. This function is required for headphone load detection as described in Section 9.4.5.

9.3.4 System Controller

The system controller (SC) automates the sequencing of the multiple blocks required to set up one or more particular audio paths. It is an optional feature, and operates by performing register writes with optimal sequencing and timing, thus eliminating pops and clicks.

The inputs are controlled using SYSTEM_MODES_INPUT, and the outputs are controlled using SYSTEM_MODES_OUTPUT. Writing to the mode_submit field of either of these registers will cause the system controller (SC) to process both input and output paths.

When the SC is activated by asserting the mode_submit field, all of the register-writes that are required by the selected sub systems are performed automatically. Each sub-system is brought up, or down, in the correct order to avoid pops and clicks. In addition, within each sub system, the component parts are brought up in the correct pop-free and click-free sequence.

9.3.5 Output Processing

9.3.5.1 Output Filters

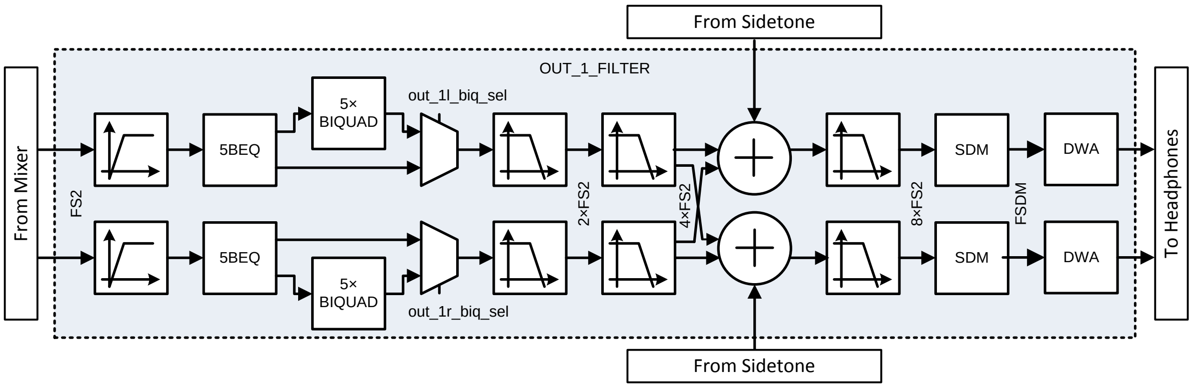


Figure 15: Output Filters Block Diagram

There is a stereo output filter chain that is used to process signals to be sent to the stereo DAC. The signals from the digital mixer (at SR2 rate) can be processed through a high-pass filter, a fixed 5-band equalizer and a 5-stage biquad filter. They can also be combined with signals from the sidetone filter (at 4 * SR2 rate).

Left and right channels of the output filter can be controlled independently. The left channel of the output filter is enabled using out_1l_filter_en and is muted using out_1l_mute_en. Gain ramping is enabled using out_1l_ramp_en.

If out_1l_subrange_en is also set, the ramping process will step though much finer gain increments. The 5-stage biquad filter is selected using out_1l_biq_5stage_sel. The gain of the left channel can be set in the range of -83.25 dB to +108 dB in 0.75 dB steps using OUT_1L_GAIN.

The right channel of the output filter is controlled in the same way.

9.3.5.2 High-Pass Filter

The output high-pass filters (HPFs) are controlled using OUT_1_HPF_FILTER_CTRL. In music mode out_1_voice_en must be set to 0 and the HPF corner frequency is set using out_1_audio_hpf_corner. In voice mode, out_1_voice_en must be set to 1, in which case the HPF corner frequency is set using out_1_voice_hpf_corner.

The value of the HPF corner frequency also depends on the output sample rate (SR2) as shown in Table 35.

The right channel of the HPF is controlled in the same way.

Table 35: Output High-Pass Filter Settings (ADC in High-Power Mode)

in_1_voice_en	out_1_voice_hpf_corner	out_1_audio_hpf_corner.	SR1 Sample Rate (kHz)										
			8	11.025	12	16	22.05	24	32	44.1	48	88.2	96
0		00	0.33	0.46	0.5	0.67	0.92	1	1.33	1.84	2	3.68	4
		01	0.67	0.92	1	1.33	1.84	2	2.67	3.68	4	7.35	8
		10	1.33	1.84	2	2.67	3.68	4	5.33	7.35	8	14.7	16
		11	2.67	3.68	4	5.33	7.35	8	10.67	14.7	16	29.4	32
1	000		2.5	3.45	3.75	5	6.89	7.5	10	Voice HPF not available for sample rates above 32 kHz.			
	001		25	34.5	37.5	50	68.9	75	100				
	010		50	68.9	75	100	137.8	150	200				
	011		100	137.8	150	200	275.6	300	400				
	100		150	206.7	225	300	413.4	450	600				
	101		200	275.6	300	400	551.3	600	800				
	110		300	413.4	450	600	826.9	900	1200				
	111		400	551.3	600	800	1102.5	1200	1600				

Table 36: Output High-Pass Filter Settings (ADC in Low-Power Mode)

in_1_voice_en	out_1_voice_hpf_corner	in_1_audio_hpf_corner	SR1 Sample Rate (kHz)										
			8	11.025	12	16	22.05	24	32	44.1	48	88.2	96
0		00	0.33	0.46	0.5	0.67	0.92	1	32 kHz sample rate not available in low-power mode	1.84	2	88.2 kHz and 96 kHz sample rates not available in low-power mode	
		01	0.67	0.92	1	1.33	1.84	2		3.68	4		
		10	1.33	1.84	2	2.67	3.68	4		7.35	8		
		11	2.67	3.68	4	5.33	7.35	8		14.7	16		
1	000		2.5	In low-power mode, the voice HPF is only available at a sample rate of 8 kHz									
	001		25										
	010		50										
	011		100										
	100		150										
	101		200										
	110		300										
	111		400										

9.3.5.3 5-Band Equalizer

The output filters can provide gain or attenuation in each of five separate (fixed) frequency bands using the 5-band equalizer (EQ). The equalizer, for both left and right channels, is enabled using out_1_eq_en.

The gain or attenuation of the first frequency band is programmable from -10.5 dB to 12.0 dB in 1.5 dB steps using out_1_eq_band1. The other four bands are programmable in the same way using out_1_eq_band2, out_1_eq_band3, out_1_eq_band4, and out_1_eq_band5. The center or cut-off frequency of each of the five bands depends on the output sample rate (SR2) as shown in Table 37.

The 5-band EQ and the 5-band biquad filter can be used at the same time for greater filtering control.

Table 37: Output 5-band Equalizer Centre and Cut-Off Frequencies

For equalizer bands 1 and 5, the cut-off frequency depends on the gain setting. The figures quoted in this table refer to the –1 dB point with the band gain set to –3 dB

SR2 (kHz)	Center/Cut-Off Frequency (Hz) at Programmed Setting				
	Band 1 Cut-Off	Band 2 Center	Band 3 Center	Band 4 Center	Band 5 Cut-Off
8	0	99	493	1528	4000
11.025	0	136	680	2106	5512
12	0	148	740	2293	6000
16	0	96	440	2128	8000
22.05	0	133	607	2933	11025
24	0	145	660	3191	12000
32	0	95	418	1797	16000
44.1	0	131	576	2386	22050
48	0	143	627	2596	24000
88.2	N/A	N/A	N/A	N/A	N/A
96	N/A	N/A	N/A	N/A	N/A

NOTE
The 5-band equalizer is only available for sample rates up to 48 kHz. The frequency response of the 5-band equalizer at sample rate of 48 kHz is shown graphically in Figure 16 to Figure 20:   The cut-off for equalizer bands 1 and 5 is dependent on gain setting. The figures quoted in Table 37 refer to the -1 dB point with the band gain set to -3 dB

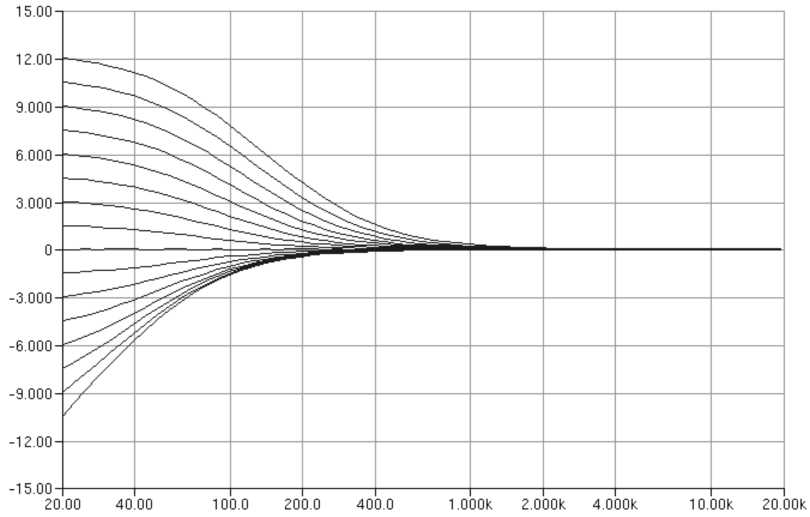


Figure 16: Equalizer Filter Band 1 Frequency Response at FS = 48 kHz

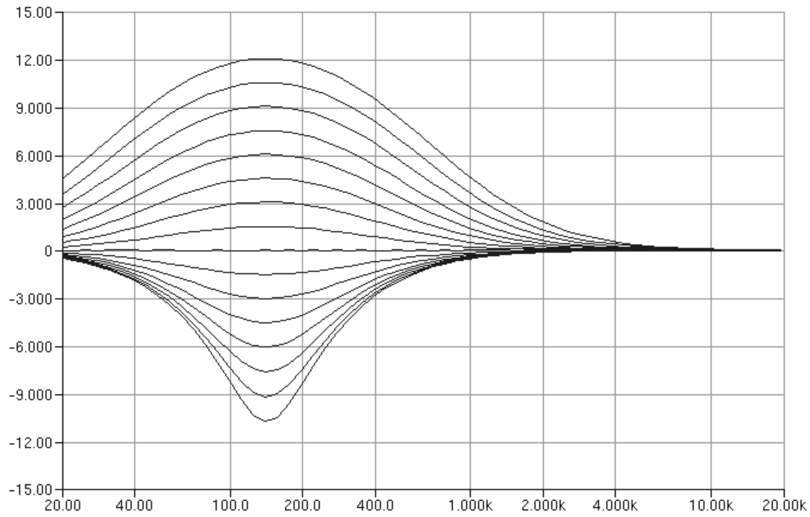


Figure 17: Equalizer Filter Band 2 Frequency Response at FS = 48 kHz

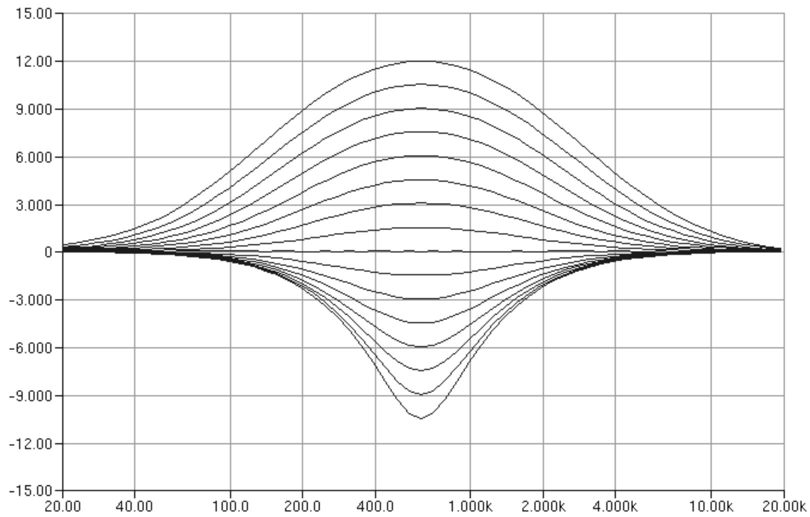


Figure 18: Equalizer Filter Band 3 Frequency Response at FS = 48 kHz

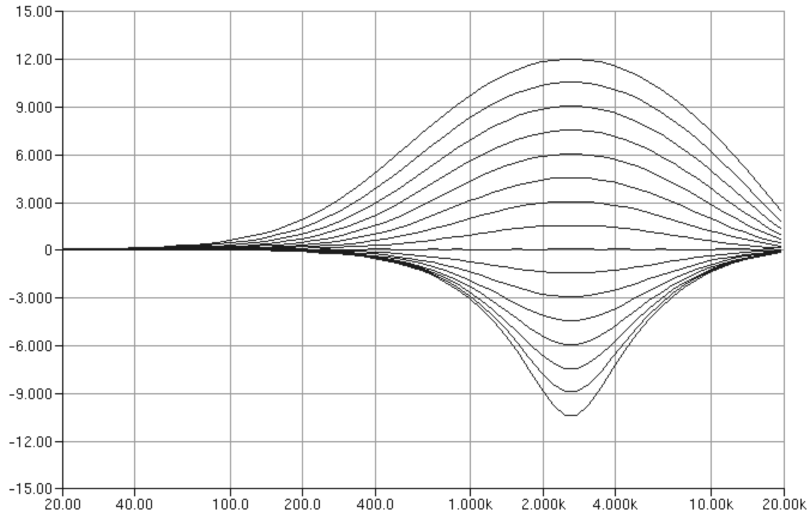


Figure 19: Equalizer Filter Band 4 Frequency Response at FS = 48 kHz

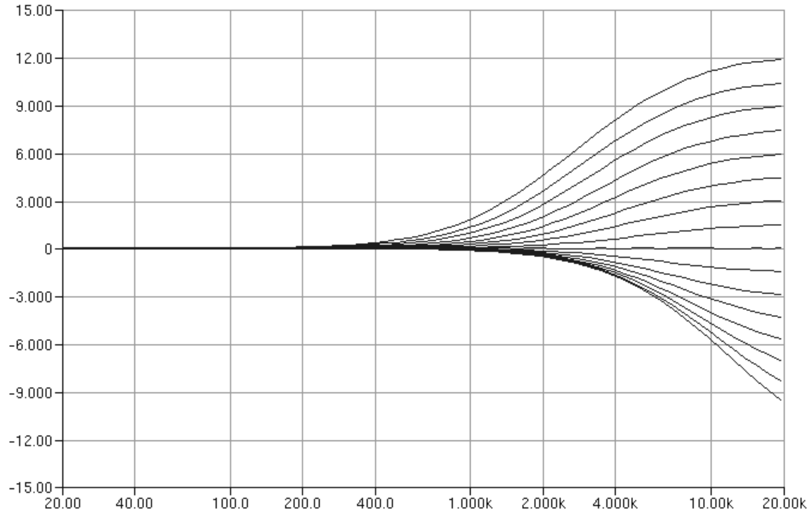


Figure 20: Equalizer Filter Band 5 Frequency Response at FS = 48 kHz

9.3.5.4 5-Stage Biquad Filter

The stereo 5-stage biquad filter can be used to provide more flexible filtering of the output signal than can be achieved using the 5-band equalizer. The biquad filters can be used for the implementation of low-pass, high-pass or notch filters.

The 5-band EQ and the 5-band biquad filter can be used at the same time for greater filtering control.

The biquad filter is enabled using out_1_biq_5stage_filter_en and can be muted using out_1_biq_5stage_mute_en.

The biquad filter on each channel can be selected independently using out_1l_biq_5stage_sel and out_1r_biq_5stage_sel in the OUT_1L_FILTER_CTRL and OUT_1R_FILTER_CTRL registers.

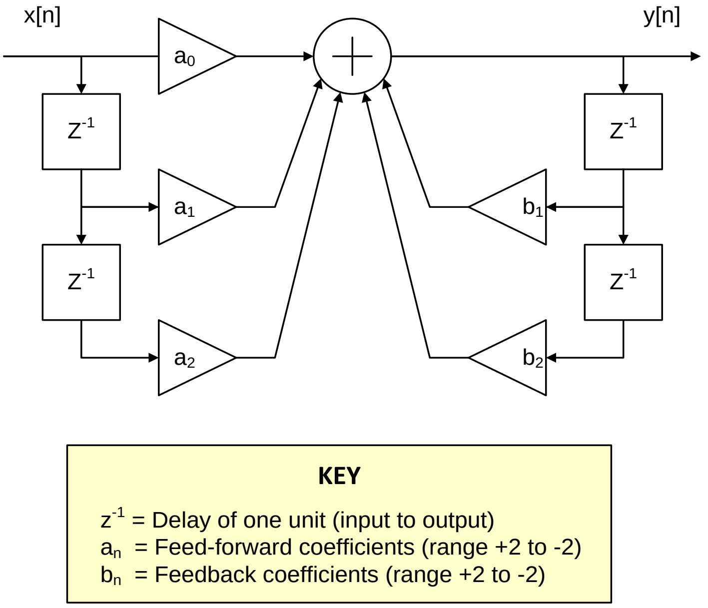


Figure 21: Single Biquad Filter Stage

Each of the five biquad stages has five 16-bit coefficients a0, a1, a2, b1 and b2 as shown in Figure 21. For the five stages the coefficients are numbered a00, a01 and so on as shown in Figure 22.

The filter sections are implemented using a direct form one architecture which implements the transfer function shown in Figure 21:

$$H(z)=\frac{a_0+a_1z^{-1}+a_2z^{-2}+a3z-3+a4z-4}{1-b_1z^{-1}-b_2z^{-2}}$$

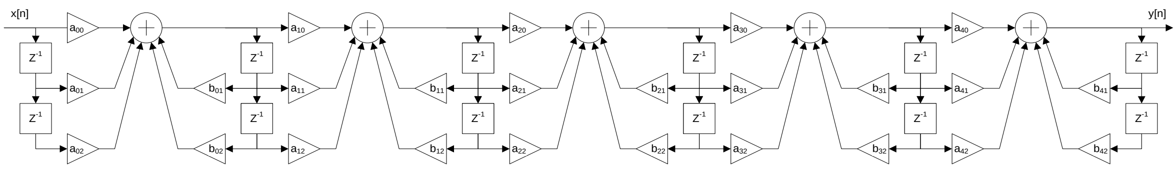


Figure 22: Cascade of Five Biquad Filter Stages

The biquad filters in both left and right channels share the same set of coefficients.

Each of the coefficients is stored using two 8-bit registers in a dedicated address space. All of the coefficients are programmed by first writing the coefficient data value to OUT_1_BIQ_5STAGE_DATA and then the coefficient address to OUT_1_BIQ_5STAGE_ADDR. The address location for each of the coefficients is described in Table 38.

Each of the 16-bit coefficients are two's complement values that can be programmed in the range of -2 (0x8000) to +2 (0x7FFF(0)). Checks should be made to ensure that the pre-programmed coefficients result in a stable transfer filter function.

The full numeric range of the coefficients is -2 to +1.999938964843750.

Table 38: Output 5-Stage Biquad Filter Coefficient Address Map

Address out_1_biq_5stage_addr	Name	Description	
0x00	OUT_1_BIQ_A00_LO	Lower byte of a00 coefficient for first output biquad stage	Biquad filter 1
0x01	OUT_1_BIQ_A00_HI	Upper byte of a00 coefficient for first output biquad stage	
0x02	OUT_1_BIQ_A01_LO	Lower byte of a01 coefficient for first output biquad stage	
0x03	OUT_1_BIQ_A01_HI	Upper byte of a01 coefficient for first output biquad stage	
0x04	OUT_1_BIQ_A02_LO	Lower byte of a02 coefficient for first output biquad stage	
0x05	OUT_1_BIQ_A02_HI	Upper byte of a02 coefficient for first output biquad stage	
0x06	OUT_1_BIQ_B01_LO	Lower byte of b01 coefficient for first output biquad stage	
0x07	OUT_1_BIQ_B01_HI	Upper byte of b01 coefficient for first output biquad stage	
0x08	OUT_1_BIQ_B02_LO	Lower byte of b02 coefficient for first output biquad stage	
0x09	OUT_1_BIQ_B02_HI	Upper byte of b02 coefficient for first output biquad stage	
0x0A	OUT_1_BIQ_A10_LO	Lower byte of a10 coefficient for second output biquad stage	Biquad filter 2
0x0B	OUT_1_BIQ_A10_HI	Upper byte of a10 coefficient for second output biquad stage	
0x0C	OUT_1_BIQ_A11_LO	Lower byte of a11 coefficient for second output biquad stage	
0x0D	OUT_1_BIQ_A11_HI	Upper byte of a11 coefficient for second output biquad stage	
0x0E	OUT_1_BIQ_A12_LO	Lower byte of a12 coefficient for second output biquad stage	
0x0F	OUT_1_BIQ_A12_HI	Upper byte of a12 coefficient for second output biquad stage	
0x10	OUT_1_BIQ_B11_LO	Lower byte of b11 coefficient for second output biquad stage	
0x11	OUT_1_BIQ_B11_HI	Upper byte of b11 coefficient for second output biquad stage	
0x12	OUT_1_BIQ_B12_LO	Lower byte of b12 coefficient for second output biquad stage	
0x13	OUT_1_BIQ_B12_HI	Upper byte of b12 coefficient for second output biquad stage	
0x14	OUT_1_BIQ_A20_LO	Lower byte of a20 coefficient for third output biquad stage	Biquad filter 3
0x15	OUT_1_BIQ_A20_HI	Upper byte of a20 coefficient for third output biquad stage	
0x16	OUT_1_BIQ_A21_LO	Lower byte of a21 coefficient for third output biquad stage	
0x17	OUT_1_BIQ_A21_HI	Upper byte of a21 coefficient for third output biquad stage	
0x18	OUT_1_BIQ_A22_LO	Lower byte of a22 coefficient for third output biquad stage	
0x19	OUT_1_BIQ_A22_HI	Upper byte of a22 coefficient for third output biquad stage	
0x1A	OUT_1_BIQ_B21_LO	Lower byte of b21 coefficient for third output biquad stage	
0x1B	OUT_1_BIQ_B21_HI	Upper byte of b21 coefficient for third output biquad stage	
0x1C	OUT_1_BIQ_B22_LO	Lower byte of b22 coefficient for third output biquad stage	
0x1D	OUT_1_BIQ_B22_HI	Upper byte of b22 coefficient for third output biquad stage	
0x1E	OUT_1_BIQ_A30_LO	Lower byte of a30 coefficient for fourth output biquad stage	Biquad filter 4
0x1F	OUT_1_BIQ_A30_HI	Upper byte of a30 coefficient for fourth output biquad stage	
0x20	OUT_1_BIQ_A31_LO	Lower byte of a31 coefficient for fourth output biquad stage	
0x21	OUT_1_BIQ_A31_HI	Upper byte of a31 coefficient for fourth output biquad stage	
0x22	OUT_1_BIQ_A32_LO	Lower byte of a32 coefficient for fourth output biquad stage	
0x23	OUT_1_BIQ_A32_HI	Upper byte of a32 coefficient for fourth output biquad stage	
0x24	OUT_1_BIQ_B01_LO	Lower byte of b31 coefficient for fourth output biquad stage	

Address out_1_biq_5stage_addr	Name	Description	
0x25	OUT_1_BIQ_B31_HI	Upper byte of b31 coefficient for fourth output biquad stage	
0x26	OUT_1_BIQ_B32_LO	Lower byte of b32 coefficient for fourth output biquad stage	
0x27	OUT_1_BIQ_B32_HI	Upper byte of b32 coefficient for fourth output biquad stage	
0x28	OUT_1_BIQ_A40_LO	Lower byte of a40 coefficient for fifth output biquad stage	Biquad filter 5
0x29	OUT_1_BIQ_A40_HI	Upper byte of a40 coefficient for fifth output biquad stage	
0x2A	OUT_1_BIQ_A41_LO	Lower byte of a41 coefficient for fifth output biquad stage	
0x2B	OUT_1_BIQ_A41_HI	Upper byte of a41 coefficient for fifth output biquad stage	
0x2C	OUT_1_BIQ_A42_LO	Lower byte of a42 coefficient for fifth output biquad stage	
0x2D	OUT_1_BIQ_A42_HI	Upper byte of a42 coefficient for fifth output biquad stage	
0x2E	OUT_1_BIQ_B41_LO	Lower byte of b41 coefficient for fifth output biquad stage	
0x2F	OUT_1_BIQ_B41_HI	Upper byte of b41 coefficient for fifth output biquad stage	
0x30	OUT_1_BIQ_B42_LO	Lower byte of b42 coefficient for fifth output biquad stage	
0x31	OUT_1_BIQ_B42_HI	Upper byte of b42 coefficient for fifth output biquad stage	

9.3.5.5 Output Dynamic Range Extension

The output dynamic range extension (DRE) block extends the range of the DA7218.

DRE can be enabled on either left, right or both output channels using dgs_enable. The input signal level at which the DRE starts swapping gains can be set in the range of -90 dB to 0 dB in 6 dB steps using dgs_signal_lvl. To prevent clipping, the input signal level at which all of the applied DRE steps are removed can be set in the range of -42 dB to 0 dB in 6 dB steps using dgs_anticlip_lvl. The maximum number of 1.5 dB gain steps that the DRE is allowed to apply can be controlled using dgs_steps.

The response time of the leaky integrator used to track the signal level at the input of the DRE is determined by the fraction of the signal added at each step. The fall rate is set by the fraction added when the signal is smaller than the current average, which can be programmed in the range 1/65536 to 1/4 using dgs_fall_coeff. The rise rate is set by the fraction added when the signal is larger than the current average, which can be programmed in the range 1/16384 to 1 using dgs_rise_coeff.

Ramping of any changes in gain levels is enabled by setting dgs_ramp_en = 1. When ramping is being performed, the changes in gain are made in 1.5 dB steps, with the maximum number of 1.5 dB steps controlled by dgs_steps.

Finer control of the ramping steps is provided if dgs_subr_en = 1. If dgs_subr_en = 1, each gain change of 1.5 dB is performed in smaller steps.

It is possible to disable the ramping of the 1.5 dB gain steps by setting dgs_ramp_en = 0, and similarly it is possible to disable the sub-ranging between the 1.5 dB gain steps by setting dgs_subr_en = 0. Note that clearing either of these two bits is likely to produce unacceptable audio artefacts such as pops and clicks.

9.3.5.6 DAC Noise Gate

The DAC noise gate can be used to automatically mute the outputs when the average signal level at the output of both left and right channel DACs falls below a programmed noise threshold for longer than a programmed hold time.

The DAC noise gate is enabled using dac_ng_en. The threshold below which the noise gate is activated can be set in the range of -102 dB to -60 dB in 6 dB steps using dac_ng_on_threshold. The threshold above which the noise gate deactivates can be set in the same range using dac_ng_off_threshold.

It is recommended to set dac_ng_off_threshold > dac_ng_on_threshold to provide some hysteresis.

The number of samples for which the DAC output signal must be below the on-threshold before the noise gate is activated can be set to 256, 512, 1024 or 2048 using dac_ng_setup_time. The noise gate is deactivated as soon as the signal level rises above the off threshold.

Prior to muting the output the gain is ramped down to minimum, and after un-muting the output the gain is ramped back up to its original value. The ramp rates can be adjusted using dac_ng_rampdn_rate and dac_ng_rampup_rate.

9.3.5.7 Digital Mixer

The DA7218 codec contains a flexible digital mixer. Any or all of the seven digital inputs (four input filters, one tone generator, and two DAI inputs) can be routed to any or all of the six digital outputs (Output Filter 1 and Output Filter 2, and four DAI outputs) with a programmable gain on each of the 42 possible paths.

The names of the registers that specify the data source, and the data output, take the form '<output target short name>_src'. Each of these 7-bit registers uses one of its bit positions to select a signal source. These registers and the bit positions corresponding to each of the seven possible signal source are listed in Table 39.

Example: Setting outdai_1l_src[2] = 1 selects source data from Input Filter 2L (determined by bit position [2]) and passes it to Output DAI 1L.

The gain on each of the 42 signal paths (seven possible inputs to six possible outputs) are independently controllable using registers whose names take the form '<output target short name>_<input source short name>_gain'. These register fields are listed in Table 40. Every register field uses the same set of settings to provide a gain range of -42 dB to 4.5 dB in -1.5 dB steps. The full set of possible gain settings for each register is listed in Table 41.

Example: Setting outdai_1l_infilt_2r_gain = 01001 provides -28.5 dB gain on the signal path Input Filter 2L to Output DAI 1L.

See Figure 23.for the input-to-output paths

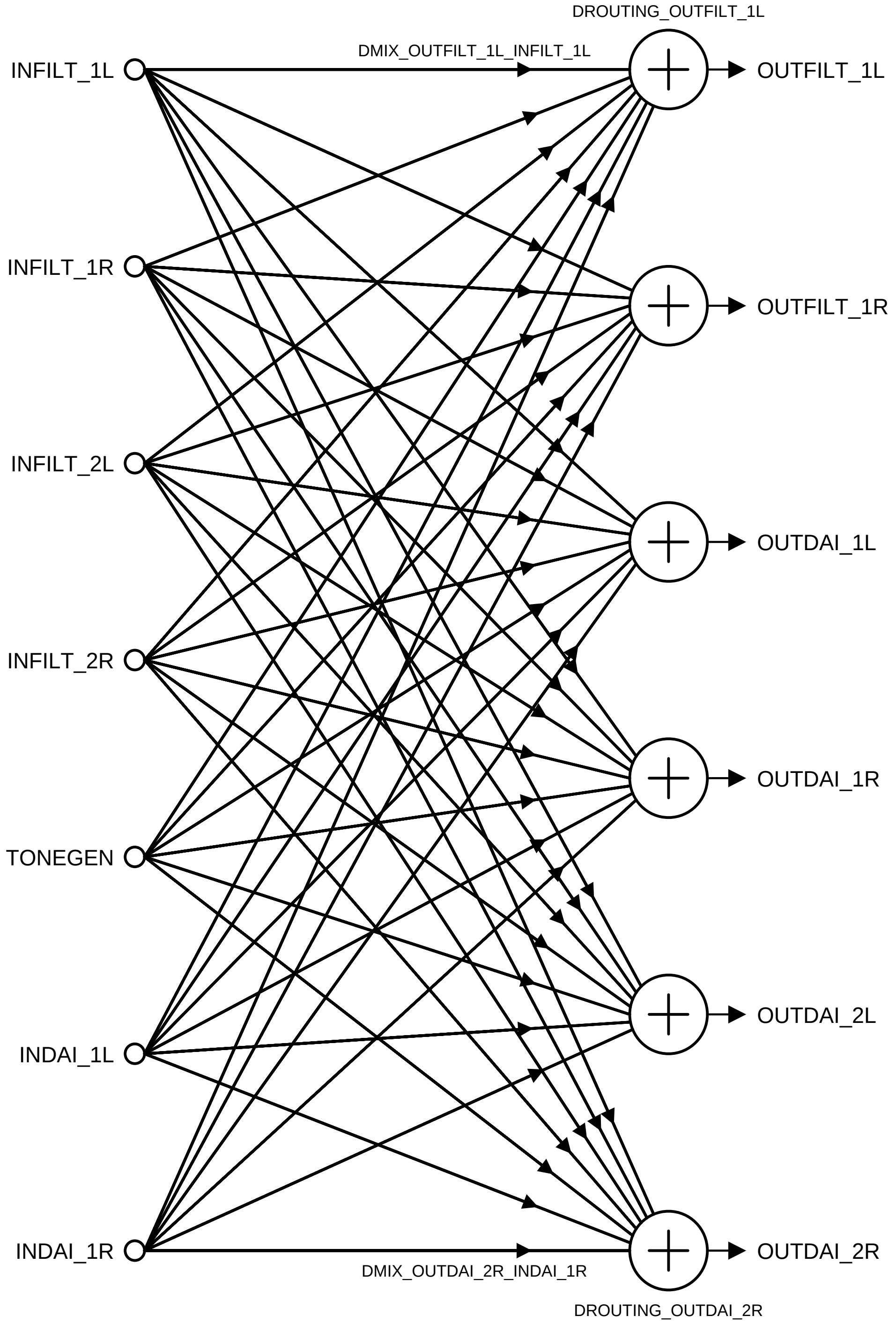


Figure 23: Possible Digital Mixer Routings

Table 39: Register Names [Bit Positions] for Selecting Digital Mixer Source and Output

	Output Stream Directed To…					
Input Source	**OUTDAI 1L**	**OUTDAI 1R**	**OUTDAI 2L**	**OUTDAI 2R**	**OUTFILT 1L**	**OUTFILT 1R**
IN FILT 1L	outdai_1l_src[0]	outdai_1r_src[0]	outdai_2l_src[0]	outdai_2r_src[0]	outfilt_1l_src[0]	outfilt_1r_src[0]
IN FILT 1R	outdai_1l_src[1]	outdai_1r_src[1]	outdai_2l_src[1]	outdai_2r_src[1]	outfilt_1l_src[1]	outfilt_1r_src[1]
IN FILT 2L	outdai_1l_src[2]	outdai_1r_src[2]	outdai_2l_src[2]	outdai_2r_src[2]	outfilt_1l_src[2]	outfilt_1r_src[2]
IN FILT 2R	outdai_1l_src[3]	outdai_1r_src[3]	outdai_2l_src[3]	outdai_2r_src[3]	outfilt_1l_src[3]	outfilt_1r_src[3]
TONE GEN	outdai_1l_src[4]	outdai_1r_src[4]	outdai_2l_src[4]	outdai_2r_src[4]	outfilt_1l_src[4]	outfilt_1r_src[4]
DAI 1L	outdai_1l_src[5]	outdai_1r_src[5]	outdai_2l_src[5]	outdai_2r_src[5]	outfilt_1l_src[5]	outfilt_1r_src[5]
DAI 1R	outdai_1l_src[6]	outdai_1r_src[6]	outdai_2l_src[6]	outdai_2r_src[6]	outfilt_1l_src[6]	outfilt_1r_src[6]

NOTE
For each listed bit position in each register, 0 = source/output combination disabled and 1 = source/output combination enable

Table 40: Cross Reference Listing the Gain-Control Registers for all Digital Mixer Sources and Outputs

	Output Stream					
Input Source	**OUTDAI 1L**	**OUTDAI 1R**	**OUTDAI 2L**	**OUTDAI 2R**	**OUTFILT 1L**	**OUTFILT 1R**
IN FILT 1L	outdai_1l_infilt_1l_gain	outdai_1r_infilt_1l_gain	outdai_2l_infilt_1l_gain	outdai_2r_infilt_1l_gain	outfilt_1l_infilt_1l_gain	outfilt_1r_infilt_1l_gain
IN FILT 1R	outdai_1l_infilt_1r_gain	outdai_1r_infilt_1r_gain	outdai_2l_infilt_1r_gain	outdai_2r_infilt_1r_gain	outfilt_1l_infilt_1r_gain	outfilt_1r_infilt_1r_gain
IN FILT 2L	outdai_1l_infilt_2l_gain	outdai_1r_infilt_2l_gain	outdai_2l_infilt_2l_gain	outdai_2r_infilt_2l_gain	outfilt_1l_infilt_2l_gain	outfilt_1r_infilt_2l_gain
IN FILT 2R	outdai_1l_infilt_2r_gain	outdai_1r_infilt_2r_gain	outdai_2l_infilt_2r_gain	outdai_2r_infilt_2r_gain	outfilt_1l_infilt_2r_gain	outfilt_1r_infilt_2r_gain
TONE GEN	outdai_1l_tonegen_gain	outdai_1r_tonegen_gain	outdai_2l_tonegen_gain	outdai_2r_tonegen_gain	outfilt_1l_tonegen_gain	outfilt_1r_tonegen_gain
DAI 1L	outdai_1l_indai_1l_gain	outdai_1r_indai_1l_gain	outdai_2l_indai_1l_gain	outdai_2r_indai_1l_gain	outfilt_1l_indai_1l_gain	outfilt_1r_indai_1l_gain
DAI 1R	outdai_1l_indai_1r_gain	outdai_1r_indai_1r_gain	outdai_2l_indai_1r_gain	outdai_2r_indai_1r_gain	outfilt_1l_indai_1r_gain	outfilt_1r_indai_1r_gain

NOTE
The gain settings for each gain-control register listed above are listed in Table 41

Table 41: Gain Settings and Values for all Registers Listed in Table 40

Gain Register Setting	Value (dB)	Gain Register Setting	Value (dB)
00000	-42.0	10000	-18.0
00001	-40.5	10001	-16.5
00010	-39.0	10010	-15.0
00011	-37.5	10011	-13.5
00100	-36.0	10100	-12.0
00101	-34.5	10101	-10.5
00110	-33.0	10110	-9.0
00111	-31.5	10111	-7.5
01000	-30.0	11000	-6.0
01001	-28.5	11001	-4.5
01010	-27.0	11010	-3.0
01011	-25.5	11011	-1.5
01100	-24.0	11100 (default setting on all registers)	0.0
01101	-22.5	11101	1.5
01110	-21.0	11110	3.0
01111	-19.5	11111	4.5

9.3.5.8 Digital Gain

Input Channel Gain

The four input filter channels can be set to apply gain in the range of -83.25 dB to +12 dB in 0.75 dB steps by programming in_1l_digital_gain, in_1r_digital_gain, in_2l_digital_gain, and in_2r_digital_gain.

Output Channel Gain

The two output filter channels can be set to apply gain in the range of -83.25 dB to +108 dB in 0.75 dB steps by programming out_1l_digital_gain and out_1r_digital_gain.

9.4 Output Paths

9.4.1 Digital to Analog Converter

The DA7218 codec includes a stereo audio digital to analog converter (DAC). Left and right channels of the DAC are independently and automatically enabled whenever the corresponding output filter channel is enabled.

The DAC is clocked at 3.072 MHz or 2.8224 MHz depending on the output sample rate (SR2). Left and right channels of the DAC are independently and automatically enabled whenever the corresponding output filter channel is enabled.

9.4.2 Headphone Amplifiers

Each headphone path has one finely adjustable amplifier (MIXOUT_L_GAIN and MIXOUT_R_GAIN) providing a gain of -1.0 dB to 0 dB in 0.5 dB steps. These are followed by a more powerful headphone amplifier stage providing a gain of –57 dB to +6 dB in 1.5 dB steps. Together they provide a total gain range of -58 dB to +6 dB in 0.5 dB steps.

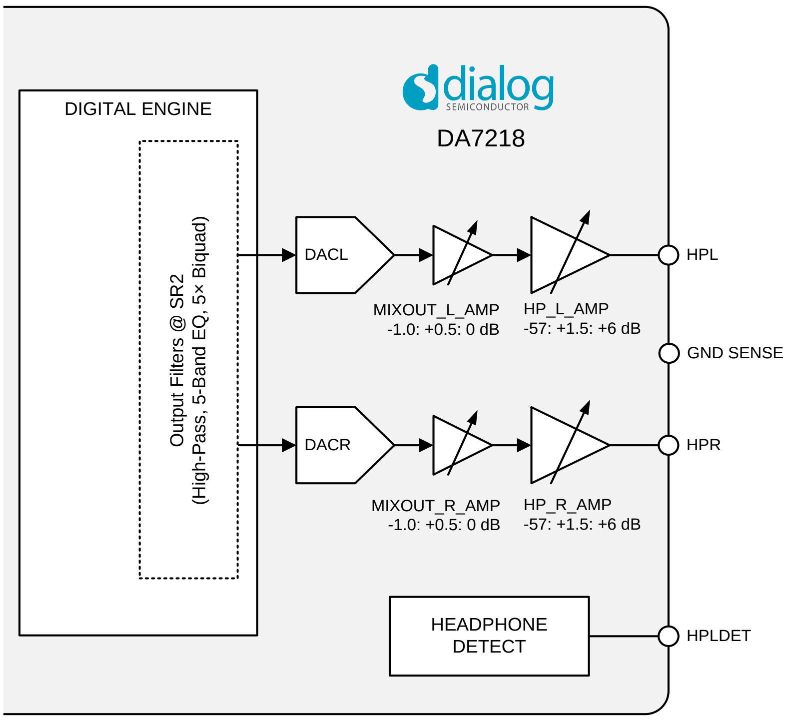


Figure 24: Headphone Output Paths

The left-channel amplifier (MIXOUT_L_CTRL) is enabled by setting mixout_l_amp_en = 1. The gain can be set in the range of –1.0 dB to 0 dB in 0.5 dB steps using mixout_l_amp_gain. This setting is static and is not synchronized with signal zero crossings and cannot be ramped. This amplifier is used to fine tune the overall analog gain level in the DAC to headphone path. The right channel output buffer (MIXOUT_R_CTRL) is controlled in the same manner.

The two finely adjustable amplifiers MIXOUT_L_GAIN and MIXOUT_R_GAIN offer no mixing capabilities. They allow additional fine-tuning of the gain on the headphone outputs from -1.0 dB to 0 dB in 0.5 dB steps.

The amplifiers are configured to be single-ended and to operate in true-ground mode. The headphone loads are connected between HPL and GND for the left headphone, and between HPR and GND for the right.

The mode in which the headphone amplifiers operate is controlled using the HP_DIFF_CTRL register. **Note**: the hp_amp_diff_mode_en bit must be set to 0.

The left-channel headphone amplifier (HP_L_CTRL) is enabled by setting hp_l_amp_en = 1. The output stage is enabled independently by setting hp_l_amp_oe = 1.

The amplifier gain can be set in the range of –57 dB to +6 dB in 1.5 dB steps using hp_l_amp_gain.

Gain updates can be ramped through all intermediate values by setting hp_l_amp_ramp_en = 1. This ramp setting overrides the settings of hp_l_amp_zc_en. To prevent zipper noise when gain ramping is selected, the gain is ramped through additional sub-range gain steps.

Alternatively, gain updates can be synchronized with signal zero-crossings by setting hp_l_amp_zc_en = 1. If no zero-crossing is detected within the timeout period, then the gain update is applied unconditionally. The timeout period is approximately 0.1 s, and is not user configurable.

The amplifier can be muted by setting hp_l_amp_mute_en = 1.

The amplifier can be put in its minimum gain configuration by setting hp_l_amp_min_gain_en = 1. If either zero-crossing or ramping are enabled when minimum gain is set, the ramping or the zero crossing will be performed while activating the minimum gain. The right-channel headphone amplifier (HP_R_CTRL) is controlled in the same manner.

Table 42: hp_l_amp_gain and hp_r_amp_gain Settings

hp_l_amp_gain and hp_r_amp_gain	Gain (dB)	hp_l_amp_gain and hp_r_amp_gain	Gain (dB)	hp_l_amp_gain and hp_r_amp_gain	Gain (dB)
000000 to 010100	Reserved	010101	-57.0	101011	-24.0
		010110	-55.5	101100	-22.5
		010111	-54.0	101101	-21.0
		011000	-52.5	101110	-19.5
		011001	-51.0	101111	-18.0
		011010	-49.5	110000	-16.5
		011011	-48.0	110001	-15.0
		011100	-46.5	110010	-13.5
		011101	-45.0	110011	-12.0
		011110	-43.5	110100	-10.5
		011111	-42.0	110101	-9.0
		100000	-40.5	110110	-7.5
		100001	-39.0	110111	-6.0
		100010	-37.5	111000	-4.5
		100011	-36.0	111001	-3.0
		100100	-34.5	111010	-1.5
		100101	-33.0	111011	0.0
		100110	-31.5	111100	1.5
		100111	-30.0	111101	3.0
		101000	-28.5	111110	4.5
		101001	-27.0	111111	6.0
		101010	-25.5		

9.4.3 Headphone Detection

DA7218 contains two forms of headphone detection. These are detection of the presence of a headphone, and detection of the impedance of the inserted device. These enable the host to determine whether or not a headphone has been plugged in to the device, and whether the headphone is mono or stereo. or a high-impedance or low-impedance load.

9.4.4 Jack Detection

Jack detection is enabled by setting hpldet_jack_en to 1, which enables an internal current source on the HPLDET pin. The insertion of a headphone must cause the HPLDET signal to be pulled low, either via an isolated switch in the headphone socket or by the HPL terminal of the headphone jack shorting HPL to the headphone detect pin in the socket. The transition on HPLDET can be used to trigger an interrupt to the host as described in Section 9.8.

The threshold level for jack detection can be set in the range of 84 % to 96 % of V_{DD} using hpldet_jack_thr. The number of debounce measurements required before triggering an interrupt can be adjusted using hpldet_jack_debounce, and the interval between measurements can be set using hpldet_jack_rate. The jack detector comparator output can be inverted for switches that are normally closed by setting hpldet_comp_inv = 1. The comparator hysteresis can enabled using hpldet_hyst_en.

9.4.4.1 Automatic MICBIAS1 Control

As the headphone jack is withdrawn from the socket, the HPL and HPR connections in the jack will come into contact with the MIC and GND contacts in the socket. If MICBIAS1 is enabled when the jack is withdrawn, this can result in a loud pop which is audible in the headphones. In order to prevent this, the MICBIAS1 output can be automatically discharged as soon as the jack withdrawal is detected. This MICBIAS1 discharge is enabled by setting hpldet_discharge_en = 1 and hpldet_jack_en = 1.

On reinsertion of the jack, MICBIAS1 will be automatically re-enabled if hpldet_discharge_en = 1 and MICBIAS1 is enabled.

9.4.5 Mono, Stereo and Load Detection

Once a jack has been inserted, it is possible to detect whether it is a stereo or mono headphone. This requires a software sequence to perform the following steps:

1. Select the tone generator to the headphone output path
2. Enable both headphone outputs
3. Ramp a DC level onto the headphone outputs using the tone generator SRAMP function
4. Enable mono/stereo detection using hp_amp_stereo_detect_en
5. Read the mono/stereo status of the headphone from hp_amp_stereo_detect_status
6. Disable mono/stereo detection
7. Ramp the headphone outputs back to 0 V using the tone generator SRAMP function

It is also possible to detect line loads (or open-circuit) independently on HPL and HPR outputs using hp_amp_load_detect_en.

9.4.6 Charge Pump Control

The charge pump is enabled by asserting cp_en in the CP_CTRL register. Once enabled, the charge pump can be controlled manually or automatically. When under manual control (cp_mchange = 00), the output voltage level is directly determined by cp_mod.

The amount of charge stored, and therefore the voltage generated, by the charge pump is controlled by the charge pump controller. As the power consumed by devices such as amplifiers is proportional to voltage, significant power savings are available by matching the charge pump's output with the system's power requirement.

Under automatic control, there are three modes of operation that are determined by the cp_mchange setting. All four modes (one manual and three automatic) are described in Table 43.

Table 43: Charge Pump Output Voltage Control

Charge Pump Tracking Mode cp_mchange	Charge Pump Output Voltage	Details
00	Manual	The charge pump's output voltage is determined by the settings of cp_mod
01	Voltage level depends on the programmed gain setting	The charge pump controller monitors the PGA volume settings and generates the minimum voltage that is required to drive a full-scale signal at the current gain level
10	Voltage level depends on the DAC signal envelope	The charge pump controller monitors the DAC signal, and generates the voltage that is required to drive a full-scale output at the current DAC signal volume level
11	Voltage level depends on the signal magnitude and the programmed gain setting	The charge pump monitors both the programmed volume settings and the actual signal size, and generates the appropriate output voltage This is the most power-efficient mode of operation

When cp_mchange is set to 10 (tracking DAC signal size, described in Table 43) or cp_mchange is set to 11 (tracking the output signal size), the charge pump switches its supply between the VDD rail and the VDD/2 rail depending on its power requirements. When low output voltages are needed, the charge pump saves power by using the lower-voltage VDD/2 rail.

The switching point between using the VDD rail and the VDD/2 rail is determined by the cp_thresh_vdd2 register setting. The switching points determined by cp_thresh_vdd2 vary between the two cp_mchange modes, and are summarized Table 44 and Table 45.

Table 44: cp_thresh_vdd2 Settings in DAC Signal Tracking Mode (cp_mchange = 10)

cp_thresh_vdd2 Setting	Approximate Switching Point	Notes
0x01	-30 dBFS	Do not use. Very power-inefficient as nearly always VDD/1
0x03	-24 dBFS	Not recommended. Very power-inefficient as nearly always VDD/1
0x07	-18 dBFS	May be used but not power efficient
0x0E	-12 dBFS	May be used
0x10	-10 dBFS	Recommended setting
0x3F to 0x13		Reserved, do not use

Table 45: cp_thresh_vdd2 Settings in Output Signal Tracking Mode (cp_mchange = 11)

cp_thresh_vdd2 Setting	Approximate Switching Point	Notes
0x00	Never	Not recommended. Always VDD/1 mode
0x01	Never	Not recommended. Always VDD/1 mode
0x02	-32 dBFS	Not recommended. Power-inefficient as nearly always VDD/1
0x03	-24 dBFS	May be used
0x04	-20 dBFS	May be used
0x05	-17 dBFS	May be used
0x06	-15 dBFS	Recommended setting
0x07	-13 dBFS	May be used
0x08	-12 dBFS	May be used
0x09	-11 dBFS	May be used
0x0A	-10 dBFS	May be used
0x0B	-9 dBFS	Not recommended. VDD/2 begins to clip
0x0C	Never	Not recommended. Always VDD/2 mode
0x0D	Never	Not recommended. Always VDD/2 mode
0x0E	Never	Not recommended. Always VDD/2 mode
0x0F	Never	Not recommended. Always VDD/2 mode

9.4.6.1 Charge Pump Initial and Switching Current

At start-up, and when moving from VDD/2 to VDD/1 the charge pump output capacitors will be charged from the VDD supply rail. The initial current spike of 100 ns will be approximately 500 mA for a 1 µF output capacitor. Ensure that the supply to VDD is capable of delivering this current. Placing a larger input capacitor on VDD will reduce the amount of instantaneous current pulled directly from the 1.8 V supply.Note that this does not apply to single supply mode operation.

Similarly, when moving from VDD/1 to VDD/2 the charge pump output capacitors will be discharged through the VDD supply rail. The initial current spike of 100 ns being sunk through VDD will be approximately 100 mA for a 1 µF capacitor. Ensure that the supply to VDD is capable of sinking this current. Note that this does not apply to single supply mode operation.

9.4.7 Tracking the Demands on the Charge Pump Output

There are three points at which the demands on the charge pump can be tracked. These tracking points are determined by cp_mchange.

9.4.7.1 cp_mchange = 00 (Manual Mode)

If cp_mchange = 00, the voltage level is controlled by the cp_mod setting.

9.4.7.2 cp_mchange = 01 (Tracking the PGA Gain Setting)

If cp_mchange = 01, the PGA gain setting is tracked, and provides feedback to boost the clock frequency when necessary.

9.4.7.3 cp_mchange = 10 (Tracking the DAC Signal Setting)

If cp_mchange = 01, the size of the DAC signal is tracked, and provides the feedback to boost the clock frequency when necessary.

9.4.7.4 cp_mchange = 11 (Tracking the Output Signal Magnitude)

If cp_mchange = 01, the magnitude of the output signal is tracked, and provides the feedback to boost the clock frequency when necessary.

9.4.8 Specifying Clock Frequencies when Tracking the Charge Pump Output Demand

cp_fcontrol specifies the frequency of the charge pump clock. The frequency is fixed and is set manually if cp_mchange = 00 (see section 9.4.7.1). The available frequency settings are SYS_CLK/8 (the absolute maximum), and SYS_CLK/16, /32, /64 and /128. Where SYS_CLK is 12.288 MHz or 11.2896 MHz depending on sample rate.

If cp_mchange does not = 00, the charge pump load is monitored and the clock frequency adjusted accordingly to allow the charge pump to supply the required current. Clock frequency varies depending on the charge pump requirements, and the cp_fcontrol settings specify the minimum frequency at which the clock will run. The maximum frequency is always SYS_CLK/8.

In addition to the cp_fcontrol settings outlined above, and which specify the minimum clock frequency, there is an extra setting of cp_fcontrol = 101 which has no minimum frequency. At this setting, the clock frequency is under the complete control of the tracking and feedback mechanism. The frequency can vary from 0 Hz when there is no load on the charge pump and no component leakage, up to the maximum of SYS_CLK/8.

In general this setting can be left at its default value of 001.

9.4.9 Other Charge Pump Controls

When a higher charge pump output voltage is needed, the charge pump increases its output at the fastest rate possible given the controls and settings in that currently in place. Once the higher output voltage is no longer needed, the charge pump controller waits for a period determined by the cp_tau_delay setting before reducing the output voltage.

For best performance Dialog Semiconductor recommend setting cp_tau_delay to 16 ms or greater.

cp_small_switch_freq_en enables a low-load, low-power switching mode. If cp_small_switch_freq_en is enabled and cp_fcontrol is set to a value between 000 and 100, any feedback from the analog level detector results in a switch from low-power to full-power. Full-power is maintained for one cp_tau_delay period after the pulse, any subsequent pulses restart the cp_tau_delay period.

If cp_fcontrol = 101, the first feedback from the analog level detector primes the change to full-power mode. If another pulse occurs within 32 clock cycles of the first feedback from the analog level detector, full power is enabled for one cp_tau_delay period.

9.4.10 True-Ground Supply Mode

In true-ground supply mode, the charge pump must be enabled to generate the ground-centered supply rails for the amplifiers.

9.5 Phase Locked Loop

The DA7218 contains a Phase Locked Loop (PLL) that can be used to generate the required 11.2896 MHz or 12.288 MHz internal system clock when a frequency of between 2 and 54 MHz is applied to MCLK. This allows sharing of clocks between devices in an application, reducing total system cost. For example, the codec may operate from common 13 MHz or 19.2 MHz system clock frequency.

9.5.1 PLL Bypass Mode

If an MCLK signal (of [11.2896, 12.288, 22.5792, 24.576, 45.1584, or 49.152] MHz) that is synchronous with WCLK and BCLK is available, the PLL is not required and should be disabled to save power. PLL bypass mode is activated by setting pll_mode = 00.

In this mode the PLL is bypassed and an audio frequency clock is applied to the MCLK pin of the codec. The required clock frequency depends on the sample rate at which the audio DACs and ADCs are operating. These clock frequencies are summarized in Table 46 for the range of DAC and ADC sample rates that can be configured using the SR register.

Table 46: Sample Rate Control Register and Corresponding System Clock Frequency

Sample Rate, FS (kHz)	SR Register	System Clock Frequency (MHz)
8	0001	12.288
11.025	0010	11.2896
12	0011	12.288
16	0101	12.288
22.05	0110	11.2896
24	0111	12.288
32	1001	12.288
44.1	1010	11.2896
48	1011	12.288
88.2	1110	11.2896
96	1111	12.288

If digital playback or record is required in bypass mode then the MCLK frequency should be set to (11.2896, 12.288, 22.5792, 24.576, 45.1584, or 49.152)MHz and pll_indiv should be programmed accordingly.

If no valid MCLK is detected, the output of the internal reference oscillator is used instead. However in this case only analog bypass paths may be used.

9.5.2 Normal PLL Mode (DAI Master)

The PLL is enabled by asserting pll_mode = 01. Once the PLL is enabled and has achieved phase lock, PLL bypass mode is disabled and the output of the PLL is used as the system clock.

The PLL input divider register (pll_indiv) is used to reduce the PLL reference frequency (2 MHz to 54 MHz) to the usable range of 2 MHz to 4.5 MHz as shown in Table 47, this reduces the PLL reference frequency according to the following equation:

FREF = FMCLK ÷ N

Table 47: PLL Input Divider

MCLK Input Frequency (MHz)	Input Divider (÷N)	pll_indiv Register (0x27 [3:2])
2 to 4.5	÷1	000
4.5 to 9	÷2	001
9 to 18	÷4	010
18 to 36	÷8	011
36 to 54	÷16	100

The value of the PLL feedback divider is used to set the voltage controlled oscillator (VCO) frequency to eight times the required system clock frequency (see Table 46).

FVCO = FREF * PLL feedback divider

The value of the PLL feedback divider is an unsigned number in the range of 0 to 128. It consists of seven integer bits and thirteen fractional bits split across three registers:

- PLL_INTEGER holds the seven integer bits
- PLL_FRAC_BOT holds the top bits (MSB) of the fractional part of the divisor
- PLL_FRAC_BOT holds the bottom bits (LSB) of the fractional part of the divisor

9.5.3 Example Calculation of the Feedback Divider Setting:

Example: A codec operating with a sample rate (F_S) = 48 kHz and a reference input clock frequency of 12.288 MHz. The required output frequency is 98.304 MHz.

The reference clock input = 12.288 MHz, which falls in the range 10-20 MHz, so pll_indiv must be set to 0b010 dividing the reference input frequency by 4 (see Table 48).

The formula for calculating the feedback divider is:

Feedback divider (F) = VCO output frequency * input divider (pll_indiv) / reference input clock

Therefore Feedback divider (F) = (98.304 * 4) / 12.288 = 32

So:

- pll_fbdiv_integer (holding the seven integer bits) = 0x20
- pll_fbdiv_frac_top (holding the top bits (MSB) of the fractional part of the divisor) = 0x00
- pll_fbdiv_frac_bot (holding the bottom bits (LSB) of the fractional part of the divisor) = 0x00

Table 48 shows example register settings that will configure the PLL when using a 13 MHz, 15 MHz or 19.2 MHz clock. Note that any MCLK input frequency between 2 MHz and 54 MHz is supported. pll_indiv must be used to reduce the PLL reference frequency to the usable range of 2 MHz to 5 MHz as shown in Table 48.

Table 48: Example PLL Configurations

MCLK Input Frequency (MHz)	System Clock Frequency (MHz)	pll_mode Register	PLL_FRAC_TOP Register	PLL_FRAC_BOT Register	PLL_INTEGER Register
13	11.2896	0x01	0x19	0x45	0x1B
13	12.288	0x01	0x07	0xEA	0x1E
15	11.2896	0x01	0x02	0xB4	0x18
15	12.288	0x01	0x06	0xDC	0x1A
19.2	11.2896	0x01	0x1A	0x1C	0x12
19.2	12.288	0x01	0x0F	0x5C	0x14

9.5.4 Sample Rate Matching PLL Mode (DAI Slave)

Sample rate matching (SRM) mode enables the PLL output clock to be synchronized to the incoming WCLK signal on the DAI. The SRM PLL mode is enabled by setting pll_mode = 10.

When using the DAI in slave mode with the SRM enabled, removing and re-applying the DAI interface word clock WCLK may cause the PLL lock to be lost. To re-lock the PLL disable the SRM (pll_mode = 00), reset the PLL by re-writing to register PLL_INTEGER, and then re-enable the SRM (pll_mode = 10) after the DAI WCLK has been reapplied.

When switching sample rates between 44.1 kHz and 48 kHz (or between the multiples of these sample rates), SRM must be disabled then re enabled using register bit pll_mode.

9.5.5 MCLK Input

MCLK is the master clock input which must be in the range of 2 MHz to 54 MHz.

MCLK can be applied as a full-amplitude square wave, or as a low-amplitude sine wave (if the MCLK squarer circuit has been enabled). The clock squarer circuit is enabled by writing pll_mclk_sqr_en = 1. The clock squarer circuit allows a sine wave or other low amplitude clock (down to 300 mVpp) to be applied to the chip. The MCLK input is AC coupled on chip when using the clock squarer circuit.

9.5.5.1 MCLK Detection

A clock detection circuit will set bit [0] of pll_srm_status = 1 whenever the applied MCLK frequency is above the minimum detection frequency of approximately 1 MHz. Whenever this bit is High, the MCLK signal is selected as the clock input to the PLL.

9.5.6 Audio Reference Oscillator

For best audio performance, a system clock within the specified range is required. The DA7218 codec has an internal reference oscillator that provides the system clock when there is no valid MCLK signal.

The reference oscillator is automatically enabled whenever the codec is in ACTIVE mode and the MCLK frequency is below the absolute minimum frequency of 1 MHz. When the codec enters STANDBY mode, the oscillator is automatically disabled to save power.

9.5.6.1 Oscillator Calibration

The reference oscillator can be calibrated for use in low-power applications where no MCLK signal is supplied but where the system clock needs to be reasonably accurate. For example when using the level detection, the device can be set to automatically stream data to the host. If the oscillator has been calibrated then the DAI clocks will run within 5 % of the nominal frequency, allowing the data to be processed correctly by the host. To perform this calibration, the device requires a valid WCLK signal on the DAI (in either master or slave mode). The SRM block uses this as a reference against which to tune the oscillator. See section 9.5.6.2 for the calibration procedure.

The entire calibration block is enabled by setting pll_refosc_cal_en = 1. This enables both the initial calibration of the reference oscillator and the later use of the calibrated oscillator.

As long as the reference oscillator block has been enabled, the oscillator can be calibrated by writing 1 to pll_refosc_cal_start. Once the calibration has been completed, the pll_refosc_cal_start bit will return a 0 value. The 5-bit calibration value is stored in pll_refosc_cal_ctrl.

The reference oscillator runs automatically when in ACTIVE mode and when there is no valid MCLK signal. In STANDBY mode, the oscillator is automatically disabled to save power.

9.5.6.2 Procedure for Calibrating the Reference Oscillator

1. Apply a valid WCLK frequency
2. Set register PLL_REFOSC_CAL (address 0x98) = 0x80
3. The reference oscillator is now calibrated and will run whenever it is required

9.5.7 Internal System Clock

The internal system clock (SYSCLK) from which all other clocks are derived is normally one of two possible frequencies:

- 12.288 MHz for SR1 and SR2 from the 48 kHz family (8, 12, 16, 24, 32, 48, 96 kHz)
- 11.2896 MHz for SR1 and SR2 from the 44.1kHz family (11.025, 22.05, 44.1, 88.2 kHz)

The only exception to this is when the DAI is not used. In this case there is no requirement for a specific internal system clock frequency.

9.6 Reference Generation

9.6.1 Voltage References

The audio circuits use supply-derived references of 0.45*VDD (VMID) and 0.9*VDD (DACREF). There is also bandgap-derived fixed voltage reference of 1.2 V (VREF). All three voltage references require off-chip decoupling capacitors (see section 12 for further details).

Both VREF and VMID are automatically enabled whenever the device enters ACTIVE mode. They are automatically disabled when entering STANDBY mode.

The VMID reference comes from a high-resistance voltage divider, which combines with the decoupling capacitor to create a large RC (resistance-capacitance) time constant. This ensures a noise-free VMID reference, however the charge time is longer.

The bandgap reference VREF also takes time to charge its decoupling capacitor, but an internal timer ensures that no circuit that requires VREF is enabled until VREF has reached 1.2 V.

The DACREF voltage reference is produced from VMID by a times-two buffer so is capable of charging its decoupling capacitor quickly.

9.6.2 Bias Currents

DA7218 has a master bias current generation block that is enabled by default using the bias_en bit. Master bias current generation is set to on by default. Each sub-system has its own local current generation block, which is automatically enabled whenever any of its sub-blocks are enabled.

9.6.3 Voltage Levels

9.6.3.1 Digital Regulator

The digital engine is supplied from VDD. An internal LDO regulator can produce the internal rail VDDDIG. The regulator is controlled using the LDO_CTRL register and is enabled using the ldo_en bit. VDDDIG must not be used to drive external circuitry.

When the LDO is disabled, the regulator is in bypass mode and VDDDIG is shorted to VDD.

When the LDO is enabled, VDDDIG is regulated by the setting of ldo_en (see Table 49:).

Table 49: Audio Sub-System Digital LDO Level

ldo_level_select Setting	LDO Level (V)
00	1.05
01	1.10
10	1.20
11	1.40

9.6.3.2 Digital Input/Output Pins Voltage Level

The digital input/output (I/O) pins can be set to operate in either a high voltage (2.5 V to 3.6 V) or low voltage (1.5 V to 2.5 V) range using the io_voltage_level bit. This bit should be set to the relevant value based on the IO voltage level of the host.

9.7 I^{2}C Control Interface

The DA7218 is completely software-controlled from the host via register writes. The DA7218 provides an I^{2}C compliant serial control interface to access these registers. Data is shifted into or out of the DA7218 under the control of the host processor, which also provides the serial clock.

The I^{2}C clock is supplied by the SCL line and the bi-directional I^{2}C data is carried by the SDA line. The I^{2}C interface is open-drain supporting multiple devices on a single line. The bus lines have to be pulled High by external pull-up resistors (1 kΩ to 20 kΩ range). The attached devices only drive the bus lines Low by connecting them to ground. This means that two devices cannot conflict if they drive the bus simultaneously.

Table 50: Device 7-Bit I²C Slave Addresses

Pin AD	Device I²C Address
High	1B
Low	1A

In standard/fast mode the highest frequency of the bus is 1 MHz. The exact frequency can be determined by the application and does not have any relation to the DA7218 internal clock signals. DA7218 will follow the host clock speed within the described limitations and does not initiate any clock arbitration or slow down.

In high-speed mode the maximum frequency of the bus can be increased up to 3.4 MHz. This mode is supported if the SCL line is driven with a push-pull stage from the host and if the host enables an external 3 mA pull-up at the SDA pin to decrease the rise time of the data. In this mode the SDA line on DA7218 is able to sink up to 12 mA. In all other respects the high speed mode behaves as the standard/fast mode. Communication on the I²C bus always takes place between two devices, one acting as the master and the other as the slave. The DA7218 will only operate as a SLAVE in I²C communication.

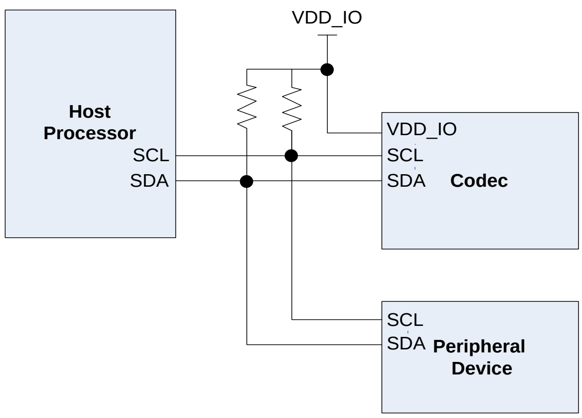


Figure 25: Schematic of the I²C Control Interface Bus

All data is transmitted across the I²C bus in groups of eight bits. To send a bit the SDA line is driven to the intended state while the SDA is Low (a LOW on SDA indicates a zero bit). Once the SDA has settled, the SCL line is brought HIGH and then LOW. This pulse on SCL clocks the SDA bit into the receiver's shift register.

A two byte serial protocol is used containing one byte for address and one byte for data. Data and address transfer is transmitted MSB first for both read and write operations. All transmission begins with the START condition from the master while the bus is in the IDLE state (the bus is free). It is initiated by a HIGH to LOW transition on the SDA line while the SCL is in the HIGH state (a STOP condition is indicated by a LOW to HIGH transition on the SDA line while the SCL line is in the HIGH state).

Figure 26: Timing of I²C START and STOP Conditions

The I²C bus is monitored by DA7218 for a valid SLAVE address whenever the interface is enabled. It responds with an Acknowledge immediately when it receives its own slave address. The Acknowledge is achieved by pulling the SDA line LOW during the following clock cycle (white blocks marked with ‘A’ in Figure 27 to Figure 30).

The protocol for a register write from master to slave consists of a start condition, a slave address with read/write bit and the 8-bit register address followed by eight bits of data terminated by a STOP condition (the DA7218 responds to all bytes with an Acknowledge).This is illustrated in Figure 27.

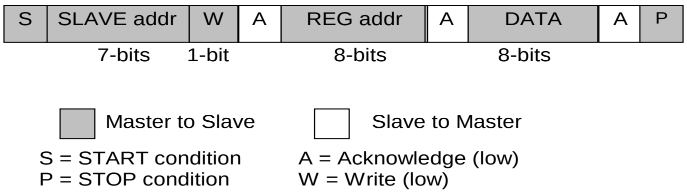


Figure 27: I²C Byte Write (SDA signal)

When the host reads data from a register it first has to write access DA7218 with the target register address and then read access DA7218 with a repeated START, or alternatively a second START condition. After receiving the data the host sends a Not Acknowledge (NAK) and terminates the transmission with a STOP condition:

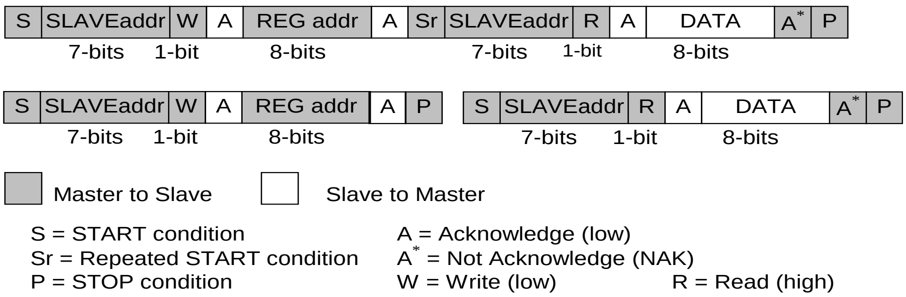


Figure 28: Examples of the I²C Byte Read (SDA line)

Consecutive (Page mode) Read-out mode (cif_i2c_write_mode = 0) is initiated from the master by sending an Acknowledge instead of Not Acknowledge (NAK) after receipt of the data word. The I²C control block then increments the address pointer to the next I²C address and sends the data to the master. This enables an unlimited read of data bytes until the master sends a NAK directly after the receipt of data, followed by a subsequent STOP condition. If a non-existent I²C address is read out, the DA7218 will return code zero.

S	SLAVEaddr	W	A	REG addr	A	Sr	SLAVEaddr	R	A	DATA	A	DATA	A	DATA	A*	P
	7-bits	1 bit		8-bits			7-bits	1-bit		8-bits		8-bits		8-bits		

S	SLAVEaddr	W	A	REG addr	A	P
	7-bits	1-bit		8-bits		

S	SLAVEaddr	R	A	DATA	A	DATA	A*	P
	7-bits	1-bit		8-bits		8-bits		

Master to Slave   Slave to Master

S = START condition
Sr = Repeat START condition
P = STOP condition

A = Acknowledge (low)
A* = Not Acknowledge (NAK)
W = Write (low)   R = Read (high)

Figure 29: Examples of I²C Page Read (SDA line)

The slave address after the Repeated START condition must be the same as the previous slave address.

Consecutive-write-mode (cif_i2c_write_mode = 0) is supported if the Master sends several data bytes following a slave register address. The I²C control block then increments the address pointer to the next I²C address, stores the received data and sends an Acknowledge until the master sends the STOP condition.

S	SLAVEaddr	W	A	REGadr	A	DATA	A	DATA	A	DATA	A	....	A	P
	7-bits	1 bit		8-bits		8-bits	1-bit	8-bits		8-bits		Repeated writes		

Master to Slave   Slave to Master

S = START condition
Sr = Repeat START condition
P = STOP condition

A = Acknowledge (low)
A* = Not Acknowledge (NAK)
W = Write (low)   R = Read (high)

Figure 30: I²C Page Write (SDA Line)

An alternative Repeated-write mode that uses non-consecutive slave register addresses is available using the cif_i2c_write_mode register. In this Repeat mode (cif_i2c_write_mode = 1), the slave can be configured to support a host's repeated write operations into several non-consecutive registers. Data is stored at the previously received register address. If a new START or STOP condition occurs within a message, the bus returns to IDLE mode. This is illustrated in Figure 31.

S	SLAVEaddr	W	A	REG addr	A	DATA	A	REG addr	A	DATA	A	....	A	P
	7-bits	1 bit		8-bits		8-bits	1-bit	8-bits		8-bits		Repeated writes		

Master to Slave   Slave to Master

S = START condition
Sr = Repeat START condition
P = STOP condition

A = Acknowledge (low)
A* = Not Acknowledge (NAK)
W = Write (low)   R = Read (high)

Figure 31: I²C Repeated Write (SDA Line)

In Page mode (cif_i2c_write_mode = 0), both Page mode reads and writes using auto incremented addresses, and Repeat mode reads and writes using non auto-incremented addresses, are supported. In Repeat mode (cif_i2c_write_mode = 1) however, only Repeat mode reads and writes are supported.

9.8 Digital Audio Interface

DA7218 provides one digital audio interface (DAI) to input DAC data or to output ADC data. It is enabled by asserting dai_en. The DAI provides flexible routing options allowing each interface to be connected to different signal paths as desired in each application.

The DAI consists of a four-wire serial interface, with bit clock (BCLK), word clock (WCLK), data-in (DATIN) and data-out (DATOUT) pins. Both Master and Slave clock modes are supported by the DA7218. Master mode is enabled by setting register dai_clk_en = 1. In Master mode, the bit clock and word clock signals are outputs from the codec. In Slave mode these are inputs to the codec.

In Master mode the frame length is configured using the dai_clk_enfield. In Slave mode this register is not used.

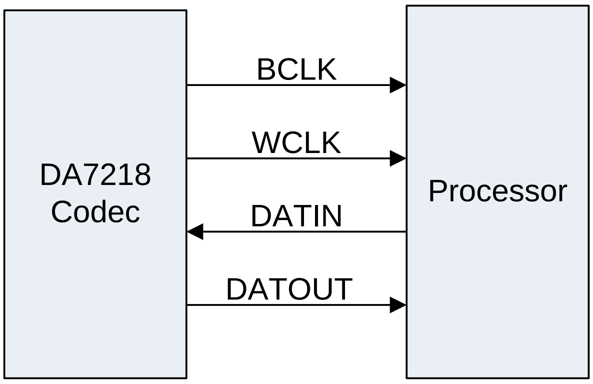


Figure 32: Master Mode (dai_clk_en = 1)

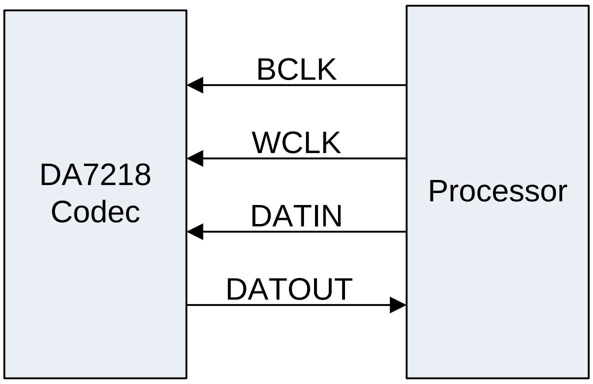


Figure 33: Slave Mode (dai_clk_en = 0)

The internal serialized DAI data is 24 bits wide. Serial data that is not 24 bits wide is either shortened or zero-filled at input to, or at output from, the DAI's internal 24-bit data width. The serial data word length can be configured to be 16, 20, 24 or 32 bits wide using the dai_word_length register bits.

Four different data formats are supported by the DAI. The data format is determined by the setting of the dai_format register bits.

- I^{2}S mode
- Left justified mode
- Right justified mode
- DSP mode

Time division multiplexing (TDM) is available in any of these modes to support the case where multiple devices are communicating simultaneously on the same bus. TDM is enabled by asserting the dai_tdm_mode_en bit.

9.8.1 DAI Channels

The DAI supports one to four channels, even in non-TDM modes. The number of channels required is specified by setting dai_ch_num bit which controls the position of the channels as shown in Figure 34.

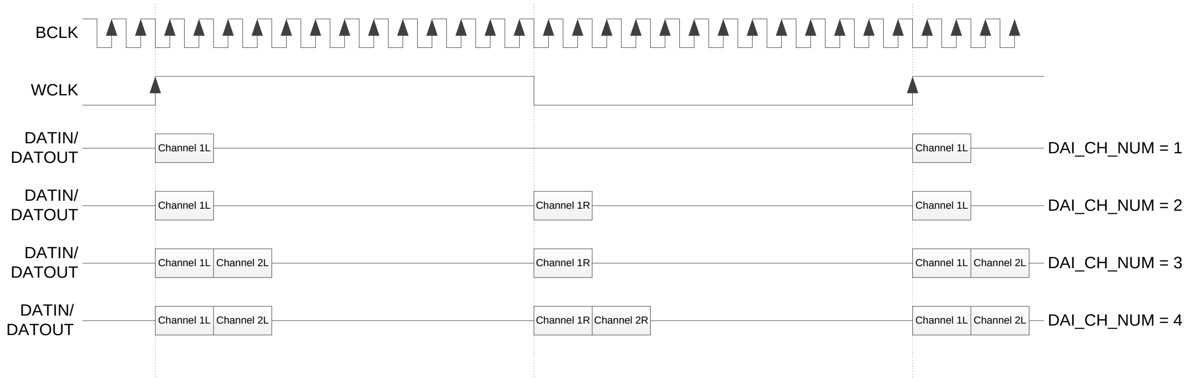


Figure 34: Effect of dai_ch_num Bit on DAI Channel Positions (Non-TDM Mode)

In TDM mode, each of the four channels can be individually enabled using the dai_tdm_mode_en bit as shown in Figure 35.

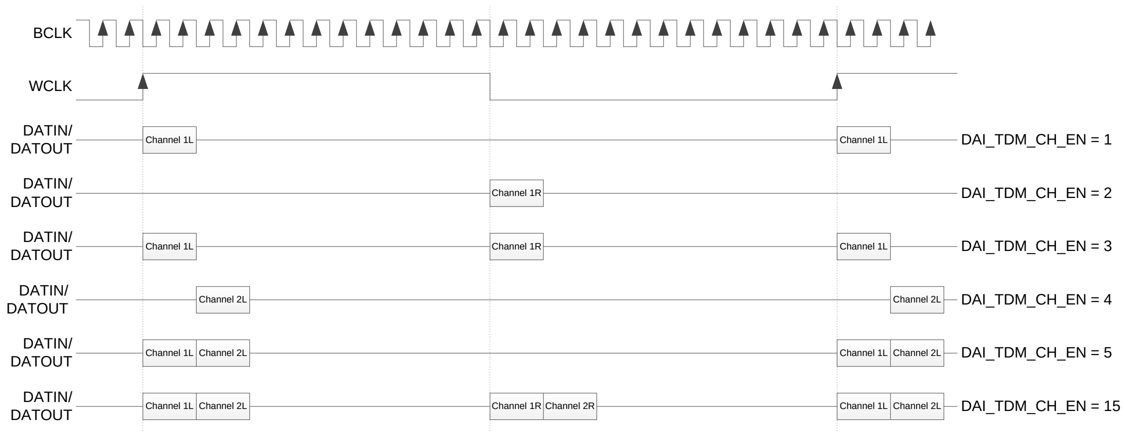


Figure 35: Effect of dai_tdm_ch_en Bit on DAI Channel Positions (TDM Mode)

9.8.2 DAI WCLK Tristate Mode

For systems that use the BCLK output of DA7218 as a reference clock, it is possible to tristate the WCLK signal even when BCLK is acting as an output. This is done by enabling DAI Master mode (dai_clk_en = 1) and WCLK tristate (dai_wclk_tri_state = 1).

9.9 Interrupt Control

The nIRQ output can be used to signal to the host that an event has been detected by the codec. The event that triggered the interrupt can be revealed by reading the EVENT register. Events can be excluded from generating interrupts using the EVENT_MASK register.

9.9.1 Level Detect Events

The input level-detect event status can be seen in lvl_det_event, and cleared by writing lvl_det_event = 1. Level-detect events can be excluded by setting lvl_det_event_msk = 1.

9.9.2 Jack Detect Events

The jack detect event status can be seen in hpldet_jack_event, and cleared by writing hpldet_jack_event = 1. The actual jack status (in or out) can be read from hpldet_jack_sts. Jack events can be masked from the interrupt mechanism by setting hpldet_jack_event_irq_msk = 1.

9.10 System Settings

9.10.1 Sample Rate

The inputs (ADC) and the outputs (DAC) can be set to operate at independent sample rates using sr_adc and sr_dac. The only condition is that either the ADC sample rate or the DAC sample rate must be an integer or multiple of the other. The DAI will operate at whichever of the ADC or DAC sample rates is faster, and samples for the slower of the two will be repeated on the DAI.

9.10.2 Gain Ramp Rate

The rate at which all gains are ramped is controlled by the one register field gain_ramp_rate. The four possible settings and ramping rates controllable by the GAIN_RAMP_CTRL register are:

Table 51: Ramp Rate Settings Applicable to All Ramp-Enabled Gains

gain_ramp_rate Setting	Ramping Rate (Note 1)
00	0 = nominal rate * 8 (fastest)
01	1 = nominal rate
10	2 = nominal rate / 8
11	3 = nominal rate / 16 (slowest)

Note 1 Nominal rate = 0.88 ms/dB

9.10.3 Program Counter Control

The program counter runs from the internal system clock and needs to be synchronized with the DAI so that data is sampled and delivered at the correct time with respect to the DAI clocks. Synchronization behavior is controlled using the PC_COUNT register.

The program counter can be set to automatically resync to the DAI using pc_resync_auto. It can be set to freerun without the need for DAI clocks using pc_freerun.

9.10.4 Soft Reset

The device can be reset (all register values reset to their default values) by writing cif_reg_soft_reset = 0x80.

This is an abrupt reset. To avoid pops and clicks, all audio paths must be shut down prior to issuing a soft reset.

10 Register Maps and Definitions

Table 52: Register map adc_cor_00 page 0

Address Name	#	7	6	5	4	3	2	1	0
Register Page 0									
0x000000C0 ADC_1_CTRL		Reserved					adc_1_aaf_en	Reserved	
0x000000C1 ADC_2_CTRL		Reserved					adc_2_aaf_en	Reserved	
0x000000C2 ADC_MODE		Reserved					adc_lvldet_auto_exit	adc_lvldet_mode	adc_lp_mode

Table 53: ADC_1_CTRL (Page 0: 0x000000C0)

Bit	Mode	Symbol	Description	Reset
2	R/W	adc_1_aaf_en	Anti-alias filter control on ADC1 0 = anti-alias filter disabled 1 = anti-alias filter enabled	0x1

Table 54: ADC_2_CTRL (Page 0: 0x000000C1)

Bit	Mode	Symbol	Description	Reset
2	R/W	adc_2_aaf_en	Anti-alias filter control on ADC2 0 = anti-alias filter disabled 1 = anti-alias filter enabled	0x1

Table 55: ADC_MODE (Page 0: 0x000000C2)

Bit	Mode	Symbol	Description	Reset
2	R/W	adc_lvldet_auto_exit	Controls the automatic exit of ADC Level Detection mode. When set, ADC Level Detection mode is exited automatically as soon as the input signal level exceeds the detection threshold level specified in lvl_det_level. When ADC Level Detection mode is exited, the ADC Level Detection control bit (adc_lvldet_mode) is automatically cleared. 0 = when the threshold level is exceeded, ADC Level Detection mode is not exited 1 = When the threshold level is exceeded, ADC Level Detection mode is exited, and adc_lvldet_mode is cleared	0x0
1	R/W	adc_lvldet_mode	ADC Level Detection Mode control 0 = Disabled 1 = Enabled	0x0
0	R/W	adc_lp_mode	ADC Low Power Mode control 0 = Disabled 1 = Enabled	0x0

Table 56: Register map ags_cor_00 page 0

Address Name	#	7	6	5	4	3	2	1	0
Register Page 0									
0x0000003C AGS_ENABLE		Reserved						ags_enable	
0x0000003D AGS_TRIGGER		Reserved				ags_trigger			
0x0000003E AGS_ATT_MAX		Reserved					ags_att_max		
0x0000003F AGS_TIMEOUT		Reserved							ags_timeout_en
0x00000040 AGS_ANTICLIP_CTRL		ags_anticlip_en	Reserved						

Table 57: AGS_ENABLE (Page 0: 0x0000003C)

Bit	Mode	Symbol	Description	Reset
1:0	R/W	ags_enable	ADC Gain Swap (AGS) control bit 0 controls the AGS on Channel 1 bit 1 controls the AGS on Channel 2 0 = Disabled 1 = Enabled	0x0

Table 58: AGS_TRIGGER (Page 0: 0x0000003D)

Bit	Mode	Symbol	Description	Reset
3:0	R/W	ags_trigger	AGS trigger level 0000 = 0 dB 0001 = -6 dB 0010 = -12 dB 0011 = -18 dB Continuing in -6 dB steps to 1001 = -54 dB (default) Continuing in -6 dB steps to 1110 = -84 dB 1111 = -90 dB	0x9

Table 59: AGS_ATT_MAX (Page 0: 0x0000003E)

Bit	Mode	Symbol	Description	Reset
2:0	R/W	ags_att_max	Maximum attenuation applied to the ADC by AGS 000 = 0 dB 001 = 6 dB 010 = 12 dB 011 = 18 dB 100 = 24 dB 101 = 30 dB 110 = 36 dB 111 = reserved	0x0

Table 60: AGS_TIMEOUT (Page 0: 0x0000003F)

Bit	Mode	Symbol	Description	Reset
0	R/W	ags_timeout_en	Timeout control 0 = Timeout disabled 1 = Timeout enabled	0x0

Table 61: AGS_ANTICLIP_CTRL (Page 0: 0x00000040)

Bit	Mode	Symbol	Description	Reset
7	R/W	ags_anticlip_en	ADC Gain Swap (AGS) clip prevention control 0 = Disabled 1 = Enabled	0x0

Table 62: Register map alc_cor_00 page 0

Address Name	#	7	6	5	4	3	2	1	0
Register Page 0									
0x00000030 ALC_CTRL1		alc_sync_mode				alc_en			
0x00000031 ALC_CTRL2		alc_release				alc_attack			
0x00000032 ALC_CTRL3		Reserved				alc_hold			
0x00000033 ALC_NOISE		Reserved		alc_noise					
0x00000034 ALC_TARGET_MIN		Reserved		alc_threshold_min					
0x00000035 ALC_TARGET_MAX		Reserved		alc_threshold_max					
0x00000036 ALC_GAIN_LIMITS		alc_gain_max				alc_atten_max			
0x00000037 ALC_ANA_GAIN_LIMITS		Reserved	alc_ana_gain_max			Reserved	alc_ana_gain_min		
0x00000038 ALC_ANTICLIP_CTRL		alc_anticlip_en	Reserved					alc_anticlip_step	

Table 63: ALC_CTRL1 (Page 0: 0x00000030)

Bit	Mode	Symbol	Description	Reset
7:4	R/W	alc_sync_mode	ALC hybrid mode control (using analogue and digital gains) bit 0 = Channel 1 bit 1 = Reserved bit 2 = Channel 2 bit 3 = Reserved 0 = Disabled 1 = Enabled	0x0
3:0	R/W	alc_en	Controls the ALC operation on the ADC channel bit 0 = Channel 1 Left bit 1 = Channel 1 Right bit 2 = Channel 2 Left bit 3 = Channel 2 Right 0 = ALC disabled on this channel 1 = ALC enabled on this channel	0x0

Table 64: ALC_CTRL2 (Page 0: 0x00000031)

Bit	Mode	Symbol	Description	Reset
7:4	R/W	alc_release	Sets the ALC release rate This is the rate in ms/dB at which the ALC can increase the gain 0000 = 28.66/fs 0001 = 57.33/fs 0010 = 114.6/fs 0011 = 229.3/fs 0100 = 458.6/fs 0101 = 917.1/fs 0110 = 1834/fs 0111 = 3668/fs 1000 = 7337/fs 1001 = 14674/fs 1010 to 1111 = 29348/fs	0x0
3:0	R/W	alc_attack	Sets the ALC attack rate This is the speed at which the ALC can decrease the gain 0000 = 7.33/fs 0001 = 14.66/fs 0010 = 29.32/fs 0011 = 58.64/fs 0100 = 117.3/fs 0101 = 234.6/fs 0110 = 469.1/fs 0111 = 938.2/fs 1000 = 1876/fs 1001 = 3753/fs 1010 = 7506/fs 1011 = 15012/fs 1100 to 1111 = 30024/fs	0x0

Table 65: ALC_CTRL3 (Page 0: 0x00000032)

Bit	Mode	Symbol	Description	Reset
3:0	R/W	alc_hold	Sets the ALC hold time. This is the length of time that the ALC waits before releasing. 0000 = $62/F_S$ 0001 = $124/F_S$ 0010 = $248/F_S$ 0011 = $496/F_S$ 0100 = $992/F_S$ 0101 = $1984/F_S$ 0110 = $3968/F_S$ 0111 = $7936/F_S$ 1000 = $15872/F_S$ 1001 = $31744/F_S$ 1010 = $63488/F_S$ 1011 = $126976/F_S$ 1100 = $253952/F_S$ 1101 = $507904/F_S$ 1110 = $1015808/F_S$ 1111 = $2031616/F_S$	0x0

Table 66: ALC_NOISE (Page 0: 0x00000033)

Bit	Mode	Symbol	Description	Reset
5:0	R/W	alc_noise	Threshold below which input signals will not cause the ALC to change gain 00 0000 = 0 dBFS 00 0001 = -1.5 dBFS 00 0010 = -3.0 dBFS 00 0011 = -4.5 dBFS continuing in -1.5 dBFS steps to 11 1110 = -93.0 dBFS 11 1111 = -94.5 dBFS (default)	0x3F

Table 67: ALC_TARGET_MIN (Page 0: 0x00000034)

Bit	Mode	Symbol	Description	Reset
5:0	R/W	alc_threshold_min	Sets the minimum target amplitude of the ALC output signal. If the output signal drops below this level, the ALC will increase the gain until the output signal rises above this level. 00 0000 = 0 dBFS 00 0001 = -1.5 dBFS 00 0010 = -3.0 dBFS 00 0011 = -4.5 dBFS continuing in -1.5 dBFS steps to 11 1110 = -93.0 dBFS 11 1111 = -94.5 dBFS (default)	0x3F

Table 68: ALC_TARGET_MAX (Page 0: 0x00000035)

Bit	Mode	Symbol	Description	Reset
5:0	R/W	alc_threshold_max	Sets the maximum target amplitude of the ALC output signal. If the output signal exceeds this level, the ALC will decrease the gain until the output signal drops below this level. 00 0000 = 0 dBFS 00 0001 = -1.5 dBFS 00 0010 = -3.0 dBFS 00 0011 = -4.5 dBFS continuing in -1.5 dBFS steps to 11 1110 = -93.0 dBFS 11 1111 = -94.5 dBFS	0x0

Table 69: ALC_GAIN_LIMITS (Page 0: 0x00000036)

Bit	Mode	Symbol	Description	Reset
7:4	R/W	alc_gain_max	Sets the maximum amount of gain that can be applied by the ALC 0000 = 0 dB 0001 = 6 dB 0010 = 12 dB continuing in 6 dB steps to 1110 = 84 dB 1111 = 90 dB	0xF
3:0	R/W	alc_atten_max	Sets the maximum amount of attenuation that can be applied by the ALC 0000 = 0 dB 0001 = 6 dB 0010 = 12 dB continuing in 6 dB steps to 1110 = 84 dB 1111 = 90 dB	0xF

Table 70: ALC_ANA_GAIN_LIMITS (Page 0: 0x00000037)

Bit	Mode	Symbol	Description	Reset
6:4	R/W	alc_ana_gain_max	Sets the maximum amount of analog gain that can be applied by the ALC (mixed analog and digital hybrid gain mode only) 000 = reserved 001 = 0 dB 010 = 6 dB continuing in 6 dB steps to 101 = 24 dB 110 = reserved 111 = reserved	0x7
2:0	R/W	alc_ana_gain_min	Sets the minimum amount of analog gain that can be applied by the ALC (mixed analog and digital hybrid gain mode only) 000 = reserved 001 = 0 dB 010 = 6 dB continuing in 6 dB steps to 111 = 36 dB	0x1

Table 71: ALC_ANTICLIP_CTRL (Page 0: 0x00000038)

Bit	Mode	Symbol	Description	Reset
7	R/W	alc_anticlip_en	Controls the ALC signal clip prevention mechanism 0 = Disabled 1 = Enabled	0x0
1:0	R/W	alc_anticlip_step	Sets the ALC attack rate when the output signal exceeds the anticlip threshold level specified in alc_threshold_max 00 = 0.034 dB/F_S 01 = 0.068 dB/F_S 10 = 0.136 dB/F_S 11 = 0.272 dB/F_S	0x0

Table 72: Register map calib_cor_00 page 0

Address Name	#	7	6	5	4	3	2	1	0
Register Page 0									
0x00000044 CALIB_CTRL		Reserved				calib_overflow	calib_auto_en	Reserved	calib_offset_en
0x00000045 CALIB_OFFSET_AUTO_M_1		calib_offset_auto_m_1							
0x00000046 CALIB_OFFSET_AUTO_U_1		Reserved				calib_offset_auto_u_1			
0x00000047 CALIB_OFFSET_AUTO_M_2		calib_offset_auto_m_2							
0x00000048 CALIB_OFFSET_AUTO_U_2		Reserved				calib_offset_auto_u_2			

Table 73: CALIB_CTRL (Page 0: 0x00000044)

Bit	Mode	Symbol	Description	Reset
3	R	calib_overflow	Offset overflow during calibration	0x0
2	R/W	calib_auto_en	Control of automatic calibration 0 = Disabled 1 = Enabled This is a self clearing bit. It clears automatically as soon as the calibration routine has been completed.	0x0
0	R/W	calib_offset_en	DC offset cancellation control 0 = Disabled 1 = Enabled	0x0

Table 74: CALIB_OFFSET_AUTO_M_1 (Page 0: 0x00000045)

Bit	Mode	Symbol	Description	Reset
7:0	R	calib_offset_auto_m_1	Contains the lower bits [15:8] of the Offset Correction for the left channel when in automatic mode	0x0

Table 75: CALIB_OFFSET_AUTO_U_1 (Page 0: 0x00000046)

Bit	Mode	Symbol	Description	Reset
3:0	R	calib_offset_auto_u_1	Contains the upper bits [19:16] of the Offset Correction for the left channel when in automatic mode	0x0

Table 76: CALIB_OFFSET_AUTO_M_2 (Page 0: 0x00000047)

Bit	Mode	Symbol	Description	Reset
7:0	R	calib_offset_auto_m_2	Contains the lower bits [15:8] of the Offset Correction for the right channel when in automatic mode	0x0

Table 77: CALIB_OFFSET_AUTO_U_2 (Page 0: 0x00000048)

Bit	Mode	Symbol	Description	Reset
3:0	R	calib_offset_auto_u_2	Contains the upper bits [19:16] of the Offset Correction for the right channel when in automatic mode	0x0

Table 78: Register map charge_pump_cor_00 page 0

Address Name	#	7	6	5	4	3	2	1	0
Register Page 0									
0x000000AC CP_CTRL		cp_en	cp_small_switch_freq_en	cp_mchange		cp_mod		Reserved	
0x000000AD CP_DELAY		Reserved		cp_tau_delay			cp_fcontrol		
0x000000AE CP_VOL_THRESHOLD1		Reserved		cp_thresh_vdd2					

Table 79: CP_CTRL (Page 0: 0x000000AC)

Bit	Mode	Symbol	Description	Reset
7	R/W	cp_en	Charge pump control 0 = Charge pump is disabled 1 = Charge pump is enabled	0x0
6	R/W	cp_small_switch_freq_en	Charge pump low-load low-power mode control 0 = Disabled 1 = Enabled	0x1
5:4	R/W	cp_mchange	Charge pump tracking mode control 00 = voltage level is controlled by cp_mod 01 = voltage level is controlled by the largest output volume level 10 = voltage level is controlled by the dac volume level 11 = voltage level is controlled by the signal magnitude	0x2
3:2	R/W	cp_mod	Charge pump level control in manual mode 00 = Standby 01 = Reserved 10 = CPVDD/2 11 = CPVDD/1	0x0

Table 80: CP_DELAY (Page 0: 0x000000AD)

Bit	Mode	Symbol	Description	Reset
5:3	R/W	cp_tau_delay	Charge pump voltage decay rate control. This controls the rate of change when moving from a VDD supply voltage to a VDD/2 supply voltage 000 = 0 ms 001 = 2 ms 010 = 4 ms 011 = 16 ms 100 = 64 ms 101 = 128 ms 110 = 256 ms 111 = 512 ms	0x2
2:0	R/W	cp_fcontrol	Charge pump nominal clock rate. Lower rates provide lower power but can drive less load. 000 = SYS_CLK/8 001 = SYS_CLK/16 010 = SYS_CLK/32 011 = SYS_CLK/64 100 = SYS_CLK/128 101 = 0 kHz (analog feedback control only) 110 = Reserved 111 = Reserved	0x1

Table 81: CP_VOL_THRESHOLD1 (Page 0: 0x000000AE)

Bit	Mode	Symbol	Description	Reset
5:0	R/W	cp_thresh_vdd2	Threshold at and below which the charge pump can use the CPVDD/2 rail. Note: This setting is only effective when cp_mchange = 10 or cp_mchange= 11. It is ignored for cp_mchange settings of 00 and 01	0xE

Table 82: Register map common_ao_cor_00 page 0

Address Name	#	7	6	5	4	3	2	1	0
Register Page 0									
0x00000000 SYSTEM_ACTIVE		Reserved							system_active
0x00000001 CIF_CTRL		Reserved							cif_i2c_write_mode

Table 83: SYSTEM_ACTIVE (Page 0: 0x00000000)

Bit	Mode	Symbol	Description	Reset
0	R/W	system_active	System Standby Mode control 0 = Standby Mode 1 = Acitve Mode	0x0

Table 84: CIF_CTRL (Page 0: 0x00000001)

Bit	Mode	Symbol	Description	Reset
0	R/W	cif_i2c_write_mode	2-wire interface write mode 0 = Page mode. The register address is automatically incremented after the first write. 1 = Repeat mode. The register address and data are sent for each write.	0x0

Table 85: Register map common_cor_00 page 0

<table>
<tr><th>Address Name</th><th>#</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="10">Register Page 0</td></tr>
<tr><td>0x00000004
CHIP_ID1</td><td></td><td colspan="8">chip_id1</td></tr>
<tr><td>0x00000005
CHIP_ID2</td><td></td><td colspan="8">chip_id2</td></tr>
<tr><td>0x00000006
CHIP_REVISION</td><td></td><td colspan="4">chip_major</td><td colspan="4">chip_minor</td></tr>
<tr><td>0x00000009
SOFT_RESET</td><td></td><td>cif_reg_soft_reset</td><td colspan="7">Reserved</td></tr>
<tr><td>0x0000000B
SR</td><td></td><td colspan="4">sr_dac</td><td colspan="4">sr_adc</td></tr>
<tr><td>0x0000000C
PC_COUNT</td><td></td><td colspan="6">Reserved</td><td>pc_resync_auto</td><td>pc_freerun</td></tr>
<tr><td>0x0000000D
GAIN_RAMP_CTRL</td><td></td><td colspan="6">Reserved</td><td colspan="2">gain_ramp_rate</td></tr>
<tr><td>0x00000010
CIF_TIMEOUT_CTRL</td><td></td><td colspan="7">Reserved</td><td>i2c_timeout_en</td></tr>
</table>

Table 86: CHIP_ID1 (Page 0: 0x00000004)

Bit	Mode	Symbol	Description	Reset
7:0	R	chip_id1	Chip ID - first two numbers only	0x23

Table 87: CHIP_ID2 (Page 0: 0x00000005)

Bit	Mode	Symbol	Description	Reset
7:0	R	chip_id2	Chip ID - second two numbers only	0x39

Table 88: CHIP_REVISION (Page 0: 0x00000006)

Bit	Mode	Symbol	Description	Reset
7:4	R	chip_major	Chip major revision number	0x0
3:0	R	chip_minor	Chip minor revision number	0x1

Table 89: SOFT_RESET (Page 0: 0x00000009)

Bit	Mode	Symbol	Description	Reset
7	R/W	cif_reg_soft_reset	Software reset Writing to this bit causes all the registers to be reset, returning all the registers back to their default setting	0x0

Table 90: SR (Page 0: 0x0000000B)

Bit	Mode	Symbol	Description	Reset
7:4	R/W	sr_dac	DAC Sample rate control 0001 = 8.000 kHz 0010 = 11.025 kHz 0011 = 12.000 kHz 0101 = 16.000 kHz 0110 = 22.050 kHz 0111 = 24.000 kHz 1001 = 32.000 kHz 1010 = 44.100 kHz 1011 = 48.000 kHz 1110 = 88.200 kHz 1111 = 96.000 kHz	0xA
3:0	R/W	sr_adc	ADC Sample rate control 0001 = 8.000 kHz 0010 = 11.025 kHz 0011 = 12.000 kHz 0101 = 16.000 kHz 0110 = 22.050 kHz 0111 = 24.000 kHz 1001 = 32.000 kHz 1010 = 44.100 kHz 1011 = 48.000 kHz 1110 = 88.200 kHz 1111 = 96.000 kHz	0xA

Table 91: PC_COUNT (Page 0: 0x0000000C)

Bit	Mode	Symbol	Description	Reset
1	R/W	pc_resync_auto	PC resync mode control 0 = No resync - just double sample or skip a sample if the DAI drifts with respect to the system clock 1 = Automatically resync if the DAI drifts with respect to the system clock	0x1
0	R/W	pc_freerun	Enables the filter operation when DAI is not enabled or no DAI clocks are available (ADC to DAC processing path) 0 = ADC and DAC Filters synchronised to the DAI 1 = Filters free running Note: This should be set to 1 if the ADC is feeding the DAC directly and no DAI clocks are present	0x0

Table 92: GAIN_RAMP_CTRL (Page 0: 0x0000000D)

Bit	Mode	Symbol	Description	Reset
1:0	R/W	gain_ramp_rate	Controls the speed of the gain ramping when gain_ramping is activate (nominal rate = 0.88 ms/dB) 0 = nominal rate * 8 (fastest) 1 = nominal rate 2 = nominal rate / 8 3 = nominal rate / 16 (slowest)	0x0

Table 93: CIF_TIMEOUT_CTRL (Page 0: 0x00000010)

Bit	Mode	Symbol	Description	Reset
0	R/W	i2c_timeout_en	I2C timeout to release SCL if read/write access to the chip does not complete correctly 0 = No timeout (SCL will be held low by the chip) 1 = Timeout will occur after approximately 40 ms	0x1

Table 94: Register map dac_ng_cor_00 page 0

<table>
<tr><th>Address Name</th><th>#</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="10">Register Page 0</td></tr>
<tr><td>0x0000009C DAC_NG_CTRL</td><td></td><td>dac_ng_en</td><td colspan="7">Reserved</td></tr>
<tr><td>0x0000009D DAC_NG_SETUP_TIME</td><td></td><td colspan="4">Reserved</td><td>dac_ng_rampdn_rate</td><td>dac_ng_rampup_rate</td><td colspan="2">dac_ng_setup_time</td></tr>
<tr><td>0x0000009E DAC_NG_OFF_THRESH</td><td></td><td colspan="5">Reserved</td><td colspan="3">dac_ng_off_threshold</td></tr>
<tr><td>0x0000009F DAC_NG_ON_THRESH</td><td></td><td colspan="5">Reserved</td><td colspan="3">dac_ng_on_threshold</td></tr>
</table>

Table 95: DAC_NG_CTRL (Page 0: 0x0000009C)

Bit	Mode	Symbol	Description	Reset
7	R/W	dac_ng_en	DAC noise gate control 0 = DAC noise gate is disabled 1 = DAC noise gate is enabled	0x0

Table 96: DAC_NG_SETUP_TIME (Page 0: 0x0000009D)

Bit	Mode	Symbol	Description	Reset
3	R/W	dac_ng_rampdn_rate	Ramp down rate 0 = 0.88 ms/dB 1 = 14.08 ms/dB	0x0
2	R/W	dac_ng_rampup_rate	Ramp up rate 0 = 0.22 ms/dB 1 = 0.0138 ms/dB	0x0
1:0	R/W	dac_ng_setup_time	Length of time for which the largest signal through the DACs must be below dac_ng_on_threshold for the noise gate to mute the data 0 = 256 samples 1 = 512 samples 2 = 1024 samples 3 = 2048 samples	0x0

Table 97: DAC_NG_OFF_THRESH (Page 0: 0x0000009E)

Bit	Mode	Symbol	Description	Reset
2:0	R/W	dac_ng_off_threshold	Threshold above which the noise gate will deactivate 000 = -102 dB 001 = -96 dB 010 = -90 dB 011 = -84 dB 100 = -78 dB 101 = -72 dB 110 = -66 dB 111 = -60 dB	0x0

Table 98: DAC_NG_ON_THRESH (Page 0: 0x0000009F)

Bit	Mode	Symbol	Description	Reset
2:0	R/W	dac_ng_on_threshold	Threshold below which the noise gate will activate 000 = -102 dB 001 = -96 dB 010 = -90 dB 011 = -84 dB 100 = -78 dB 101 = -72 dB 110 = -66 dB 111 = -60 dB	0x0

Table 99: Register map dai_cor_00 page 0

<table>
<tr><th>Address Name</th><th>#</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="10">Register Page 0</td></tr>
<tr><td>0x0000008C
DAI_CTRL</td><td></td><td>dai_en</td><td colspan="3">dai_ch_num</td><td colspan="2">dai_word_length</td><td colspan="2">dai_format</td></tr>
<tr><td>0x0000008D
DAI_TDM_CTRL</td><td></td><td>dai_tdm_mode_en</td><td>dai_oe</td><td colspan="2">Reserved</td><td colspan="4">dai_tdm_ch_en</td></tr>
<tr><td>0x0000008E
DAI_OFFSET_LOWER</td><td></td><td colspan="8">dai_offset_lower</td></tr>
<tr><td>0x0000008F
DAI_OFFSET_UPPER</td><td></td><td colspan="5">Reserved</td><td colspan="3">dai_offset_upper</td></tr>
<tr><td>0x00000090
DAI_CLK_MODE</td><td></td><td>dai_clk_en</td><td colspan="2">Reserved</td><td>dai_wclk_tri_state</td><td>dai_wclk_pol</td><td>dai_clk_pol</td><td colspan="2">dai_bclks_per_wclk</td></tr>
</table>

Table 100: DAI_CTRL (Page 0: 0x0000008C)

Bit	Mode	Symbol	Description	Reset
7	R/W	dai_en	DAI control 0 = DAI disabled. No data transfer. 1 = DAI enabled. Input and output data channels can be enabled using dai_ch_num.	0x0
6:4	R/W	dai_ch_num	DAI Channel control 000 = No channels are enabled 001 = Channel 1L enabled 010 = Channel 1L and 1R enabled 011 = Channel 1L, 1R and 2L enabled 100 = Channel 1L, 1R, 2L and 2R enabled 101 to 111 = Reserved	0x2
3:2	R/W	dai_word_length	DAI data word length 00 = 16 bits per channel 01 = 20 bits per channel 10 = 24 bits per channel 11 = 32 bits per channel	0x2
1:0	R/W	dai_format	DAI data format 00 = I2S mode 01 = left justified mode 10 = right justified mode 11 = DSP mode	0x0

Table 101: DAI_TDM_CTRL (Page 0: 0x0000008D)

Bit	Mode	Symbol	Description	Reset
7	R/W	dai_tdm_mode_en	DAI TDM mode control. In TDM mode the output is high impedence when not actively driving data. This allows other devices to share the DATOUT line. 0 = DAI in normal mode 1 = DAI in TDM mode	0x0
6	R/W	dai_oe	DAI output control 0 = DAI DATOUT pin is high impedence 1 = DAI DATOUT pin is driven when required	0x1
3:0	R/W	dai_tdm_ch_en	DAI TDM channel control bit 0: Channel 1L bit 1: Channel 1R bit 2: Channel 2L bit 3: Channel 2R On each bit 0 = Channel is disabled 1 = Channel is enabled	0x0

Table 102: DAI_OFFSET_LOWER (Page 0: 0x0000008E)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	dai_offset_lower	DAI data offset with respect to WCLK 0x0 = No offset relative to the normal formatting 0x1 = One BCLK period offset relative to the normal formatting 0x2 = Two BCLK periods offset relative to the normal formatting n = n BCLK period offset relative to the normal formatting	0x0

Table 103: DAI_OFFSET_UPPER (Page 0: 0x0000008F)

Bit	Mode	Symbol	Description	Reset
2:0	R/W	dai_offset_upper	DAI data offset with respect to WCLK 000 = No offset relative to the normal formatting 001 = One BCLK period offset relative to the normal formatting n = n BCLK period offset relative to the normal formatting	0x0

Table 104: DAI_CLK_MODE (Page 0: 0x00000090)

Bit	Mode	Symbol	Description	Reset
7	R/W	dai_clk_en	DAI master mode control 0 = Slave mode (BCLK/WCLK inputs) 1 = Master mode (BCLK/WCLK outputs)	0x0
4	R/W	dai_wclk_tri_state	WCLK tri-state control 0 = WCLK state set by the dai_clk_en (WCLK is set as the output in master mode, and as the input in slave mode) 1 = WCLK forced as an input	0x0
3	R/W	dai_wclk_pol	DAI word clock polarity control 0 = Normal polarity 1 = Inverted polarity	0x0
2	R/W	dai_clk_pol	DAI bit clock polarity control 0 = Normal polarity 1 = Inverted polarity	0x0
1:0	R/W	dai_bclks_per_wclk	Number of BCLK cycles per WCLK period in DAI master mode 00 = 32 BCLK cycles per WCLK 01 = 64 BCLK cycles per WCLK 10 = 128 BCLK cycles per WCLK 11 = 256 BCLK cycles per WCLK	0x1

Table 105: Register map dgs_cor_00 page 0

Address Name	#	7	6	5	4	3	2	1	0
Register Page 0									
0x00000054 DGS_TRIGGER		Reserved		dgs_trigger_lvl					
0x00000055 DGS_ENABLE		Reserved							dgs_enable
0x00000056 DGS_RISE_FALL		Reserved	dgs_fall_coeff			Reserved	dgs_rise_coeff		
0x00000057 DGS_SYNC_DELAY		dgs_sync_delay							
0x00000058 DGS_SYNC_DELAY2		dgs_sync_delay2							
0x00000059 DGS_SYNC_DELAY3		Reserved	dgs_sync_delay3						
0x0000005A DGS_LEVELS		dgs_signal_lvl				Reserved	dgs_anticlip_lvl		
0x0000005B DGS_GAIN_CTRL		Reserved	dgs_subr_en	dgs_ramp_en	dgs_steps				

Table 106: DGS_TRIGGER (Page 0: 0x00000054)

Bit	Mode	Symbol	Description	Reset
5:0	R/W	dgs_trigger_lvl	DAC Gain Swap (DGS) input-amplitude trigger level control. This sets the volume level at which all DGS steps are applied. 0x00 = 0 dB 0x01 = -1.5 dB 0x02 = -3 dB continuing in -1.5 dB steps through... 0x24 = -54 dB (default) to... 0x3e = -93 dB 0x3f = -94.5 dB	0x24

Table 107: DGS_ENABLE (Page 0: 0x00000055)

Bit	Mode	Symbol	Description	Reset
1:0	R/W	dgs_enable	DAC Gain Swap (DGS) channel control 0 = DAC Channel Left 1 = DAC Channel Right	0x0

Table 108: DGS_RISE_FALL (Page 0: 0x00000056)

Bit	Mode	Symbol	Description	Reset
6:4	R/W	dgs_fall_coeff	Control volume estimation Leaky-integrator fall rate. This register sets the fraction of the input signal that is used to calculate the rolling average for all input channels in the DAC Gain Swap (DGS) when the input signal is smaller than signal average. 000 = 1/4 001 = 1/16 010 = 1/64 011 = 1/256 100 = 1/1024 101 = 1/4096 110 = 1/16384 111 = 1/65536	0x5
2:0	R/W	dgs_rise_coeff	Control volume estimation Leaky-integrator rise rate. This register sets the fraction of the input signal that is used to calculate the rolling average for all input channels in the DAC Gain Swap (DGS) when the current input is larger than current average. 001 = 1/1 (average == signal) 010 = 1/16 011 = 1/64 100 = 1/256 101 = 1/1024 110 = 1/4096 111 = 1/16384	0x0

Table 109: DGS_SYNC_DELAY (Page 0: 0x00000057)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	dgs_sync_delay	User-defined sync-delay measured in Fs*8 clk periods. This delay is applied between Digital and Analogue gain updates to match the datapath delay through the DAC from the point of Digital gain application to the Analogue gain application. The delay is measured from the start of the frame in which the Digital gain is applied.	0xA3

Table 110: DGS_SYNC_DELAY2 (Page 0: 0x00000058)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	dgs_sync_delay2	User-defined sync-delay measured in Fs*8 clk periods (exactly as dgs_sync_delay), but this delay setting is applied when the data-delay has been reduced due to operating at faster sample rates of: 88/96k (non-low-power) 44/48k (low-power) This delay is applied between Digital and Analogue gain updates to match the datapath delay through the DAC from the point of Digital gain application to the Analogue gain application. The delay is measured from the start of the frame in which the Digital gain is applied. The switch to this delay value is performed automatically.	0x31

Table 111: DGS_SYNC_DELAY3 (Page 0: 0x00000059)

Bit	Mode	Symbol	Description	Reset
6:0	R/W	dgs_sync_delay3	User-defined sync-delay measured in Fs*16 clk periods (similar to dgs_sync_delay), but this delay setting is applied when the data-delay has been reduced due to operating in voice filter modes where the DGS operates on Fs*2 data. This delay is applied between Digital and Analogue gain updates to match the datapath delay through the DAC from the point of Digital gain application to the Analogue gain application. The delay is measured from the start of the frame in which the Digital gain is applied.	0x11

Table 112: DGS_LEVELS (Page 0: 0x0000005A)

Bit	Mode	Symbol	Description	Reset
7:4	R/W	dgs_signal_lvl	Trigger Level for application of gain. Once input drops below this level, the DGS will start applying the calculated gain-swaps. 0000 = 0 dB (swaps started immediately) 0001 = -6 dB 0010 = -12 dB continuing in -6 dB steps to... 1110 = -86 dB 1111 = -90 dB	0x0
2:0	R/W	dgs_anticlip_lvl	Trigger Level for the Anti-clip feature. Once input rises above this level, the DAC Gain Swap (DGS) will turn off immediately, removing all steps to prevent clipping. This parameter should not need to be changed from the default. 000 = 0 dB 001 = -6 dB 010 = -12 dB continuing in -6 dB steps to... 110 = -36 dB 111 = -42 dB	0x1

Table 113: DGS_GAIN_CTRL (Page 0: 0x0000005B)

Bit	Mode	Symbol	Description	Reset
6	R/W	dgs_subr_en	DGS Gain-subrange Mode. If DAC Gain Swapping (DGS) ramping is enabled, DGS normally ramps the gain in 1.5 dB steps. Setting this register field reduces the ramp step-size so there are no audible artifacts. 0 = Gain-ramping is performed in 1.5 dB steps 1 = Gain-ramping is performed in more gradual steps without audible artifacts Note that this register only has an effect if dgs_ramp_en = 1	0x1
5	R/W	dgs_ramp_en	DGS Gain-Ramping control 0 = Ramping is disabled. The gain steps are applied immediately 1 = Ramping is enabled. The gain steps are ramped in 1.5 dB increments (or in 0.5 dB steps if dgs_sub_en is set)	0x1
4:0	R/W	dgs_steps	Maximum number of DAC Gain Swap (DGS) steps of 1.5 dB to apply. If sub-ranging is active, this setting still applies to the number of 1.5 dB steps to apply, and not to the number of sub-ranging steps.	0x14

Table 114: Register map dig_gain_cor_00 page 0

Address Name	#	7	6	5	4	3	2	1	0
Register Page 0									
0x000000F4 IN_1L_GAIN		Reserved	in_1l_digital_gain						
0x000000F5 IN_1R_GAIN		Reserved	in_1r_digital_gain						
0x000000F6 IN_2L_GAIN		Reserved	in_2l_digital_gain						
0x000000F7 IN_2R_GAIN		Reserved	in_2r_digital_gain						
0x000000F8 OUT_1L_GAIN		out_1l_digital_gain							
0x000000F9 OUT_1R_GAIN		out_1r_digital_gain							

Table 115: IN_1L_GAIN (Page 0: 0x000000F4)

Bit	Mode	Symbol	Description	Reset
6:0	R/W	in_1l_digital_gain	IN_1L digital gain control 000 0000 = -83.25 dB 000 0001 = -82.5 dB 000 0010 = -81.75 dB continuing in 0.75 dB steps through... 110 1111 = 0 dB to... 111 1110 = 11.25 dB 111 1111 = 12 dB	0x6F

Table 116: IN_1R_GAIN (Page 0: 0x000000F5)

Bit	Mode	Symbol	Description	Reset
6:0	R/W	in_1r_digital_gain	IN_1R digital gain control 000 0000 = -83.25 dB 000 0001 = -82.5 dB 000 0010 = -81.75 dB continuing in 0.75 dB steps through... 110 1111 = 0 dB to... 111 1110 = 11.25 dB 111 1111 = 12 dB	0x6F

Table 117: IN_2L_GAIN (Page 0: 0x000000F6)

Bit	Mode	Symbol	Description	Reset
6:0	R/W	in_2l_digital_gain	IN_2L digital gain control 000 0000 = -83.25 dB 000 0001 = -82.5 dB 000 0010 = -81.75 dB continuing in 0.75 dB steps through... 110 1111 = 0 dB to... 111 1110 = 11.25 dB 111 1111 = 12 dB	0x6F

Table 118: IN_2R_GAIN (Page 0: 0x000000F7)

Bit	Mode	Symbol	Description	Reset
6:0	R/W	in_2r_digital_gain	IN_2R digital gain control 000 0000 = -83.25 dB 000 0001 = -82.5 dB 000 0010 = -81.75 dB continuing in 0.75 dB steps through... 110 1111 = 0 dB to... 111 1110 = 11.25 dB 111 1111 = 12 dB	0x6F

Table 119: OUT_1L_GAIN (Page 0: 0x000000F8)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	out_1l_digital_gain	OUT_1L digital gain control 0000 0000 = -83.25 dB 0000 0001 = -82.5 dB 0000 0010 = -81.75 dB continuing in 0.75 dB steps through... 0110 1111 = 0 dB to... 1111 1110 = +107.25 dB 1111 1111 = +108 dB	0x6F

Table 120: OUT_1R_GAIN (Page 0: 0x000000F9)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	out_1r_digital_gain	OUT_1R digital gain control 0000 0000 = -83.25 dB 0000 0001 = -82.5 dB 0000 0010 = -81.75 dB continuing in 0.75 dB steps through... 0110 1111 = 0 dB to... 1111 1110 = 107.25 dB 1111 1111 = 108 dB	0x6F

Table 121: Register map dmic_cor_00 page 0

Address Name	#	7	6	5	4	3	2	1	0
Register Page 0									
0x000000F0 DMIC_1_CTRL		dmic_1r_en	dmic_1l_en	Reserved			dmic_1_clk_rate	dmic_1_samplephase	dmic_1_data_sel
0x000000F1 DMIC_2_CTRL		dmic_2r_en	dmic_2l_en	Reserved			dmic_2_clk_rate	dmic_2_samplephase	dmic_2_data_sel

Table 122: DMIC_1_CTRL (Page 0: 0x000000F0)

Bit	Mode	Symbol	Description	Reset
7	R/W	dmic_1r_en	DMIC_1 right channel control 0 = DMIC_1 right channel is disabled 1 = DMIC_1 right channel is enabled	0x0
6	R/W	dmic_1l_en	DMIC_1 left channel control 0 = DMIC_1 left channel is disabled 1 = DMIC_1 left channel is enabled	0x0
2	R/W	dmic_1_clk_rate	DMIC_1 clock control 0 = system clock divided by 4 (3.072 MHz or 2.8224 MHz) 1 = system clock divided by 8 (1.536 MHz, or 1.4112 MHz)	0x0
1	R/W	dmic_1_samplephase	DMIC_1 data sampling phase 0 = Sample on DMICCLK edges 1 = Sample between DMICCLK edges	0x0
0	R/W	dmic_1_data_sel	DMIC_1 data channel select 0 = Rising edge = Left. Falling edge = Right 1 = Rising edge = Right. Falling edge = Left	0x0

Table 123: DMIC_2_CTRL (Page 0: 0x000000F1)

Bit	Mode	Symbol	Description	Reset
7	R/W	dmic_2r_en	DMIC_2 right channel control 0 = DMIC_2 right channel is disabled 1 = DMIC_2 right channel is enabled	0x0
6	R/W	dmic_2l_en	DMIC_2 left channel control 0 = DMIC_2 left channel is disabled 1 = DMIC_2 left channel is enabled	0x0
2	R/W	dmic_2_clk_rate	DMIC_2 clock control 0 = system clock divided by 4 (3.072 MHz or 2.8224 MHz) 1 = system clock divided by 8 (1.536 MHz, or 1.4112 MHz)	0x0
1	R/W	dmic_2_samplephase	DMIC_2 data sampling phase 0 = Sample on DMICCLK edges 1 = Sample between DMICCLK edges	0x0
0	R/W	dmic_2_data_sel	DMIC_2 data channel select 0 = Rising edge = Left. Falling edge = Right 1 = Rising edge = Right. Falling edge = Left	0x0

Table 124: Register map env_track_cor_00 page 0

Address Name	#	7	6	5	4	3	2	1	0
Register Page 0									
0x0000004C ENV_TRACK_CTRL		Reserved		integ_release		Reserved		integ_attack	

Table 125: ENV_TRACK_CTRL (Page 0: 0x0000004C)

Bit	Mode	Symbol	Description	Reset
5:4	R/W	integ_release	Sets the rate at which the input signal envelope is tracked as the signal gets smaller 00 = 1/4 01 = 1/16 10 = 1/256 11 = 1/65536	0x0
1:0	R/W	integ_attack	Sets the rate at which the input signal envelope is tracked as the signal gets larger 00 = 1/4 01 = 1/16 10 = 1/256 11 = 1/65536	0x0

Table 126: Register map hp_cor_00 page 0

Address Name	#	7	6	5	4	3	2	1	0
Register Page 0									
0x000000D0 HP_L_CTRL		hp_l_amp_en	hp_l_amp_mute_en	hp_l_amp_ramp_en	hp_l_amp_zc_en	hp_l_amp_oe	hp_l_amp_min_gain_en	Reserved	
0x000000D1 HP_L_GAIN		Reserved		hp_l_amp_gain					
0x000000D2 HP_R_CTRL		hp_r_amp_en	hp_r_amp_mute_en	hp_r_amp_ramp_en	hp_r_amp_zc_en	hp_r_amp_oe	hp_r_amp_min_gain_en	Reserved	
0x000000D3 HP_R_GAIN		Reserved		hp_r_amp_gain					
0x000000D4 HP_SNGL_CTRL		hp_amp_stereo_detect_en	hp_amp_load_detect_en	Reserved			hpr_amp_load_detect_status	hpl_amp_load_detect_status	hp_amp_stereo_detect_status
0x000000D5 HP_DIFF_CTRL		Reserved			hp_amp_single_supply_en	Reserved			hp_amp_diff_mode_en
0x000000D7 HP_DIFF_UNLOCK		Reserved							hp_diff_unlock

Table 127: HP_L_CTRL (Page 0: 0x000000D0)

Bit	Mode	Symbol	Description	Reset
7	R/W	hp_l_amp_en	HP_L amplifier control 0 = Headphone left amplifier disabled 1 = Headphone right amplifier enabled	0x0
6	R/W	hp_l_amp_mute_en	HP_L amplifier mute control 0 = Headphone left amplifier unmuted 1 = Headphone left amplifier muted	0x1
5	R/W	hp_l_amp_ramp_en	HP_L amplifier gain ramping control 0 = gain changes are instant 1 = gain changes are ramped between old and new gain values Note that this setting overrides zero crossing	0x0
4	R/W	hp_l_amp_zc_en	HP_L amplifier zero cross control 0 = gain changes are instant 1 = gain changes are performed when the data crosses zero Note that this setting is overridden by the ramp setting	0x0
3	R/W	hp_l_amp_oe	HP_L amplfier output enabling control 0 = output is high impedence 1 = output is driven	0x0
2	R/W	hp_l_amp_min_gain_en	HP_L amplifier gain held at the minimum value 0 = Normal gain operation 1 = Minimum gain only	0x0

Table 128: HP_L_GAIN (Page 0: 0x000000D1)

Bit	Mode	Symbol	Description	Reset
5:0	R/W	hp_l_amp_gain	HP_L gain control in 1.5 dB steps 00 0000 to 01 0100 = reserved 01 0101 = -57.0 dB 01 0110 = -55.5 dB 01 0111 = -54.0 dB continuing in 1.5 dB steps through... 11 1011 = 0.0 dB to… 11 1101 = 3 dB 11 1110 = 4.5 dB 11 1111 = 6.0 dB	0x3B

Table 129: HP_R_CTRL (Page 0: 0x000000D2)

Bit	Mode	Symbol	Description	Reset
7	R/W	hp_r_amp_en	HP_R amplifier control 0 = Headphone right amplifier disabled 1 = Headphone right amplifier enabled	0x0
6	R/W	hp_r_amp_mute_en	HP_R amplifier mute control 0 = Headphone right amplifier unmuted 1 = Headphone right amplifier muted	0x1
5	R/W	hp_r_amp_ramp_en	HP_R amplifier gain ramping control 0 = gain changes are instant 1 = gain changes are ramped between old and new gain values Note that this setting overrides zero crossing	0x0
4	R/W	hp_r_amp_zc_en	HP_R amplifier zero cross control 0 = gain changes are instant 1 = gain changes are performed when the data crosses zero Note that this setting is overridden by the ramp setting	0x0
3	R/W	hp_r_amp_oe	HP_R amplfier output enabling control 0 = output is high impedence 1 = output is driven	0x0
2	R/W	hp_r_amp_min_gain_en	HP_R amplifier gain held at the minimum value 0 = Normal gain operation 1 = Minimum gain only	0x0

Table 130: HP_R_GAIN (Page 0: 0x000000D3)

Bit	Mode	Symbol	Description	Reset
5:0	R/W	hp_r_amp_gain	HP_R gain control in 1.5 dB steps 00 0000 to 01 0100 = reserved 01 0101 = -57.0 dB 01 0110 = -55.5 dB 01 0111 = -54.0 dB continuing in 1.5 dB steps through... 11 1011 = 0.0 dB to… 11 1101 = 3 dB 11 1110 = 4.5 dB 11 1111 = 6.0 dB	0x3B

Table 131: HP_SNGL_CTRL (Page 0: 0x000000D4)

Bit	Mode	Symbol	Description	Reset
7	R/W	hp_amp_stereo_detect_en	Enable the detection of stereo headphones	0x0
6	R/W	hp_amp_load_detect_en	Enable the load detect function on both HPL and HPR.	0x0
2	R	hpr_amp_load_detect_status	HPR load detect comparator status. 0 = No headphone load preset 1 = Headphone load present	0x0
1	R	hpl_amp_load_detect_status	HPL load detect comparator status 0 = No headphone load preset 1 = Headphone load present	0x0
0	R	hp_amp_stereo_detect_status	HP stereo detect status 0 = Mono 1 = Stereo	0x0

Table 132: HP_DIFF_CTRL (Page 0: 0x000000D5)

Bit	Mode	Symbol	Description	Reset
0	R/W	hp_amp_diff_mode_en	Enables differential headphone output 0 = Single-ended output 1 = Reserved	0x0

Table 133: Register map hpldet_cor_00 page 0

Address Name	#	7	6	5	4	3	2	1	0
Register Page 0									
0x000000D8 HPLDET_JACK		hpldet_jack_en	hpldet_jack_thr		hpldet_jack_debounce		hpldet_jack_rate		
0x000000D9 HPLDET_CTRL		hpldet_discharge_en	Reserved					hpldet_hyst_en	hpldet_comp_inv
0x000000DA HPLDET_TEST		Reserved			hpldet_comp_sts	Reserved			

Table 134: HPLDET_JACK (Page 0: 0x000000D8)

Bit	Mode	Symbol	Description	Reset
7	R/W	hpldet_jack_en	Accessory detect jack detection 0 = Disabled 1 = Enabled	0x0
6:5	R/W	hpldet_jack_thr	Threshold level for jack detection measured as a percentage of VDD 00 = 84% 01 = 88% 10 = 92% 11 = 96%	0x0
4:3	R/W	hpldet_jack_debounce	HPL jack detection debounce control. Number of debounce measurements taken before a jack insertion is confirmed and the host is informed. Debounce measurements are separated by the time defined by accdet_jack_rate, so it will take up to accdet_jack_rate*accdet_jack_deb to successfully determine a jack insertion. No debouncing is performed for removal. 00 = no debounce 01 = 2 10 = 3 11 = 4	0x1
2:0	R/W	hpldet_jack_rate	Time between jack detection measurements when there is no jack or a 3-pole jack is inserted 0 = 5 us 1 = 10 us 2 = 20 us 3 = 40 us 4 = 80 us 5 = 160 us 6 = 320 us 7 = 640 us	0x3

Table 135: HPLDET_CTRL (Page 0: 0x000000D9)

Bit	Mode	Symbol	Description	Reset
7	R/W	hpldet_discharge_en	Control of automatic discharge of MICBIAS on jack removal 0 = Disabled 1 = Enabled	0x0
1	R/W	hpldet_hyst_en	HPL detection hysteresis control 0 = Disabled 1 = Enabled	0x0
0	R/W	hpldet_comp_inv	HPL detector output inversion control Setting this register causes the HPL detector comparator output signal tobe inverted 0 = Not inverted 1 = Inverted	0x0

Table 136: HPLDET_TEST (Page 0: 0x000000DA)

Bit	Mode	Symbol	Description	Reset
4	R	hpldet_comp_sts	HPLDET Comparator output 0 = No headphone detected 1 = Headphone detected	0x0

Table 137: Register map in_filter_cor_00 page 0

Address Name	#	7	6	5	4	3	2	1	0
Register Page 0									
0x00000018 IN_1L_FILTER_CTRL		in_1l_filter_en	in_1l_mute_en	in_1l_ramp_en	Reserved				
0x00000019 IN_1R_FILTER_CTRL		in_1r_filter_en	in_1r_mute_en	in_1r_ramp_en	Reserved				
0x0000001A IN_2L_FILTER_CTRL		in_2l_filter_en	in_2l_mute_en	in_2l_ramp_en	Reserved				
0x0000001B IN_2R_FILTER_CTRL		in_2r_filter_en	in_2r_mute_en	in_2r_ramp_en	Reserved				

Table 138: IN_1L_FILTER_CTRL (Page 0: 0x00000018)

Bit	Mode	Symbol	Description	Reset
7	R/W	in_1l_filter_en	IN_1L_FILTER control 0 = IN_1L_FILTER disabled 1 = IN_1L_FILTER enabled	0x0
6	R/W	in_1l_mute_en	IN_1L_FILTER mute control 0 = IN_1L_FILTER unmuted 1 = IN_1L_FILTER muted	0x0
5	R/W	in_1l_ramp_en	IN_1L_FILTER gain ramping control 0 = Ramping is disabled. The gain steps are applied immediately. 1 = Ramping is enabled.	0x0

Table 139: IN_1R_FILTER_CTRL (Page 0: 0x00000019)

Bit	Mode	Symbol	Description	Reset
7	R/W	in_1r_filter_en	IN_1R_FILTER control 0 = IN_1R_FILTER disabled 1 = IN_1R_FILTER enabled	0x0
6	R/W	in_1r_mute_en	IN_1R_FILTER mute control 0 = IN_1R_FILTER unmuted 1 = IN_1R_FILTER muted	0x0
5	R/W	in_1r_ramp_en	IN_1R_FILTER gain ramping control 0 = Ramping is disabled. The gain steps are applied immediately. 1 = Ramping is enabled.	0x0

Table 140: IN_2L_FILTER_CTRL (Page 0: 0x0000001A)

Bit	Mode	Symbol	Description	Reset
7	R/W	in_2l_filter_en	IN_2L_FILTER control 0 = IN_2L_FILTER disabled 1 = IN_2L_FILTER enabled	0x0
6	R/W	in_2l_mute_en	IN_2L_FILTER mute control 0 = IN_2L_FILTER unmuted 1 = IN_2L_FILTER muted	0x0
5	R/W	in_2l_ramp_en	IN_2L_FILTER gain ramping control 0 = Ramping is disabled. The gain steps are applied immediately. 1 = Ramping is enabled.	0x0

Table 141: IN_2R_FILTER_CTRL (Page 0: 0x0000001B)

Bit	Mode	Symbol	Description	Reset
7	R/W	in_2r_filter_en	IN_2R_FILTER control 0 = IN_2R_FILTER disabled 1 = IN_2R_FILTER enabled	0x0
6	R/W	in_2r_mute_en	IN_2R_FILTER mute control 0 = IN_2R_FILTER unmuted 1 = IN_2R_FILTER muted	0x0
5	R/W	in_2r_ramp_en	IN_2R_FILTER gain ramping control 0 = Ramping is disabled. The gain steps are applied immediately. 1 = Ramping is enabled.	0x0

Table 142: Register map in_hpf_filter_cor_00 page 0

Address Name	#	7	6	5	4	3	2	1	0
Register Page 0									
0x000000BC IN_1_HPF_FILTER_CTRL		in_1_hpf_en	Reserved	in_1_audio_hpf_corner		in_1_voice_en	in_1_voice_hpf_corner		
0x000000BD IN_2_HPF_FILTER_CTRL		in_2_hpf_en	Reserved	in_2_audio_hpf_corner		in_2_voice_en	in_2_voice_hpf_corner		

Table 143: IN_1_HPF_FILTER_CTRL (Page 0: 0x000000BC)

Bit	Mode	Symbol	Description	Reset
7	R/W	in_1_hpf_en	ADC high-pass filter control 0 = ADC high-pass filter disabled 1 = ADC high-pass filter enabled	0x1
5:4	R/W	in_1_audio_hpf_corner	3 dB cut-off control for the High Pass Filter At 48 kHz, the 3 dB cut-off is at: 00 = 2 Hz 01 = 4 Hz 10 = 8 Hz 11 = 16 Hz For other sample rates the corner cut-off points scale proprtionately	0x0
3	R/W	in_1_voice_en	ADC voice filter control 0 = ADC voice filter disabled 1 = ADC voice filter enabled	0x0
2:0	R/W	in_1_voice_hpf_corner	3 dB cut-off control for the high-pass voice filter At 8 kHz, the 3 dB cut-off is at: 000 = 2.5 Hz 001 = 25 Hz 010 = 50 Hz 011 = 100 Hz 100 = 150 Hz 101 = 200 Hz 110 = 300 Hz 111 = 400 Hz	0x0

Table 144: IN_2_HPF_FILTER_CTRL (Page 0: 0x000000BD)

Bit	Mode	Symbol	Description	Reset
7	R/W	in_2_hpf_en	ADC high-pass filter control 0 = ADC high-pass filter disabled 1 = ADC high-pass filter enabled	0x1
5:4	R/W	in_2_audio_hpf_corner	3 dB cut-off control for the High Pass Filter At 48 kHz, the 3 dB cut-off is at: 00 = 2 Hz 01 = 4 Hz 10 = 8 Hz 11 = 16 Hz For other sample rates the corner cut-off points scale proprtionately	0x0
3	R/W	in_2_voice_en	ADC voice filter control 0 = ADC voice filter disabled 1 = ADC voice filter enabled	0x0
2:0	R/W	in_2_voice_hpf_corner	3 dB cut-off control for the Voice filter At 8 kHz, the 3 dB cut-off is at: 000 = 2.5 Hz 001 = 25 Hz 010 = 50 Hz 011 = 100 Hz 100 = 150 Hz 101 = 200 Hz 110 = 300 Hz 111 = 400 Hz	0x0

Table 145: Register map irq_cor_00 page 0

Address Name	#	7	6	5	4	3	2	1	0
Register Page 0									
0x000000EC EVENT_STATUS		hpldet_jack_sts	Reserved						
0x000000ED EVENT		hpldet_jack_event	Reserved						lvl_det_event
0x000000EE EVENT_MASK		hpldet_jack_event_irq_msk	Reserved						lvl_det_event_msk

Table 146: EVENT_STATUS (Page 0: 0x000000EC)

Bit	Mode	Symbol	Description	Reset
7	R	hpldet_jack_sts	Status of jack insertion 0 - No jack inserted 1 - Jack Inserted	0x0

Table 147: EVENT (Page 0: 0x000000ED)

Bit	Mode	Symbol	Description	Reset
7	R/W	hpldet_jack_event	Jack event, write 1 to clear	0x0
0	R/W	lvl_det_event	Level Detect Event	0x0

Table 148: EVENT_MASK (Page 0: 0x000000EE)

Bit	Mode	Symbol	Description	Reset
7	R/W	hpldet_jack_event_irq_msk	Mask HPL jack_event from nIRQ pin 0 = HPL Jack interrupts are sent to the nIRQ pin 1 = No HPL Jack interrupts are sent to the nIRQ pin	0x0
0	R/W	lvl_det_event_msk	Level Detect Event mask 0 = Level Detect interrupts are sent to the nIRQ pin 1 = No Level Detect interrupts are sent to the nIRQ pin	0x0

Table 149: Register map levels_cor_00 page 0

<table>
<tr><th>Address Name</th><th>#</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="10">Register Page 0</td></tr>
<tr><td>0x000000E0
IO_CTRL</td><td></td><td colspan="7">Reserved</td><td>io_voltage_level</td></tr>
<tr><td>0x000000E1
LDO_CTRL</td><td></td><td>ldo_en</td><td>Reserved</td><td colspan="2">ldo_level_select</td><td colspan="4">Reserved</td></tr>
</table>

Table 150: IO_CTRL (Page 0: 0x000000E0)

Bit	Mode	Symbol	Description	Reset
0	R/W	io_voltage_level	Digital I/O voltage range control 0 = 2.5 to 3.6 V 1 = 1.5 to 2.5 V	0x0

Table 151: LDO_CTRL (Page 0: 0x000000E1)

Bit	Mode	Symbol	Description	Reset
7	R/W	ldo_en	Audio sub-system digital LDO control. The master bias must be enabled for the LDO to operate. 0 = LDO bypassed 1 = LDO active	0x0
5:4	R/W	ldo_level_select	Audio sub-system digital LDO level select 00 = 1.05 V 01 = 1.10 V 10 = 1.20 V 11 = 1.40 V	0x0

Table 152: Register map lvl_det_cor_00 page 0

<table>
<tr><th>Address Name</th><th>#</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="10">Register Page 0</td></tr>
<tr><td>0x00000050
LVL_DET_CTRL</td><td></td><td colspan="4">Reserved</td><td colspan="4">lvl_det_en</td></tr>
<tr><td>0x00000051
LVL_DET_LEVEL</td><td></td><td>Reserved</td><td colspan="7">lvl_det_level</td></tr>
</table>

Table 153: LVL_DET_CTRL (Page 0: 0x00000050)

Bit	Mode	Symbol	Description	Reset
3:0	R/W	lvl_det_en	Level Detect channel enable bit 0 = Channel 1 Left bit 1 = Channel 1 Right bit 2 = Channel 2 Left bit 3 = Channel 2 Right For all bits, 0 = Channel is disabled 1 = Channel is enabled	0x0

Table 154: LVL_DET_LEVEL (Page 0: 0x00000051)

Bit	Mode	Symbol	Description	Reset
6:0	R/W	lvl_det_level	Sets the threshold above which the ALC enters anti-clip operation. The threshold represented by this field setting, where x is the value of the bit-field, is x = ((x+1)/128) FS 000 0000 = 0.0078 FS 000 0001 = 0.0156 FS 000 0010 = 0.0234 FS continuing in 0.0078 FS steps to... 111 1101 = 0.9844 FS 111 1110 = 0.9922 FS 111 1111 = 1.0000FS	0x7F

Table 155: Register map mic_cor_00 page 0

Address Name	#	7	6	5	4	3	2	1	0
Register Page 0									
0x000000B4 MIC_1_CTRL		mic_1_amp_en	mic_1_amp_mute_en	Reserved					
0x000000B5 MIC_1_GAIN		Reserved					mic_1_amp_gain		
0x000000B7 MIC_1_SELECT		Reserved						mic_1_amp_in_sel	
0x000000B8 MIC_2_CTRL		mic_2_amp_en	mic_2_amp_mute_en	Reserved					
0x000000B9 MIC_2_GAIN		Reserved					mic_2_amp_gain		
0x000000BB MIC_2_SELECT		Reserved						mic_2_amp_in_sel	

Table 156: MIC_1_CTRL (Page 0: 0x000000B4)

Bit	Mode	Symbol	Description	Reset
7	R/W	mic_1_amp_en	MIC_1 amplifier control 0 = MIC_1 amplifier is disabled 1 = MIC_1 amplifier is enabled	0x0
6	R/W	mic_1_amp_mute_en	MIC_1 amplifier mute control 0 = MIC_1 amplifier unmuted 1 = MIC_1 amplifier muted	0x1

Table 157: MIC_1_GAIN (Page 0: 0x000000B5)

Bit	Mode	Symbol	Description	Reset
2:0	R/W	mic_1_amp_gain	MIC_1 amplifier gain control 000 = -6 dB 001 = 0 dB 010 = 6 dB 011 = 12 dB 100 = 18 dB 101 = 24 dB 110 = 30 dB 111 = 36 dB	0x1

Table 158: MIC_1_SELECT (Page 0: 0x000000B7)

Bit	Mode	Symbol	Description	Reset
1:0	R/W	mic_1_amp_in_sel	MIC_1 input source select 00 = differential 01 = MIC_1_P single-ended 10 = MIC_1_N single-ended 11 = reserved	0x0

Table 159: MIC_2_CTRL (Page 0: 0x000000B8)

Bit	Mode	Symbol	Description	Reset
7	R/W	mic_2_amp_en	MIC_2 amplifier control 0 = MIC_2 amplifier is disabled 1 = MIC_2 amplifier is enabled	0x0
6	R/W	mic_2_amp_mute_en	MIC_2 amplifier mute control 0 = MIC_2 amplifier is unmuted 1 = MIC_2 amplifier is muted	0x1

Table 160: MIC_2_GAIN (Page 0: 0x000000B9)

Bit	Mode	Symbol	Description	Reset
2:0	R/W	mic_2_amp_gain	MIC_2 amplifier gain control 000 = -6 dB 001 = 0 dB 010 = 6 dB 011 = 12 dB 100 = 18 dB 101 = 24 dB 110 = 30 dB 111 = 36 dB	0x1

Table 161: MIC_2_SELECT (Page 0: 0x000000BB)

Bit	Mode	Symbol	Description	Reset
1:0	R/W	mic_2_amp_in_sel	MIC_2 input source select 00 = Differential 01 = MIC_1_P single-ended 10 = MIC_1_N single-ended 11 = Reserved	0x0

Table 162: Register map micbias_cor_00 page 0

Address Name	#	7	6	5	4	3	2	1	0
Register Page 0									
0x000000FC MICBIAS_CTRL		micbias_2_lp_mode	micbias_2_level			micbias_1_lp_mode	micbias_1_level		
0x000000FD MICBIAS_EN		Reserved			micbias_2_en	Reserved			micbias_1_en

Table 163: MICBIAS_CTRL (Page 0: 0x000000FC)

Bit	Mode	Symbol	Description	Reset
7	R/W	micbias_2_lp_mode	MICBIAS2 low-power mode control 0 = MICBIAS2 low-power mode disabled 1 = MICBIAS2 low-power mode enabled Note that the microphone bias power mode can only be changed while the associated micbias circuit is disabled (micbias_2_en = 0)	0x0
6:4	R/W	micbias_2_level	Microphone bias 2 level control 000 = 1.6 V 001 = 1.8 V 010 = 2.0 V 011 = 2.2 V 100 = 2.4 V 101 = 2.6 V 110 = 2.8 V 111 = 3.0 V Note that the microphone bias level can only be changed while the associated micbias circuit is disabled (micbias_2_en = 0)	0x0
3	R/W	micbias_1_lp_mode	MICBIAS1 low-power mode control 0 = MICBIAS1 low-power mode disabled 1 = MICBIAS1 low-power mode enabled Note that the microphone bias power mode can only be changed while the associated micbias circuit is disabled (micbias_1_en = 0)	0x0
2:0	R/W	micbias_1_level	Microphone bias 1 level control 000 = 1.6 V 001 = 1.8 V 010 = 2.0 V 011 = 2.2 V 100 = 2.4 V 101 = 2.6 V 110 = 2.8 V 111 = 3.0 V Note that the microphone bias level can only be changed while the associated micbias circuit is disabled (micbias_1_en = 0)	0x0

Table 164: MICBIAS_EN (Page 0: 0x000000FD)

Bit	Mode	Symbol	Description	Reset
4	R/W	micbias_2_en	Microphone bias 2 control 0 = MICBIAS_2 is disabled 1 = MICBIAS_2 is enabled	0x0
0	R/W	micbias_1_en	Microphone bias 1 control 0 = MICBIAS_1 is disabled 1 = MICBIAS_1 is enabled	0x0

Table 165: Register map mixin_cor_00 page 0

Address Name	#	7	6	5	4	3	2	1	0
Register Page 0									
0x0000002C MIXIN_1_CTRL		mixin_1_amp_en	mixin_1_amp_mute_en	mixin_1_amp_ramp_en	mixin_1_amp_zc_en	mixin_1_mix_sel	Reserved		
0x0000002D MIXIN_1_GAIN		Reserved				mixin_1_amp_gain			
0x0000002E MIXIN_2_CTRL		mixin_2_amp_en	mixin_2_amp_mute_en	mixin_2_amp_ramp_en	mixin_2_amp_zc_en	mixin_2_mix_sel	Reserved		
0x0000002F MIXIN_2_GAIN		Reserved				mixin_2_amp_gain			

Table 166: MIXIN_1_CTRL (Page 0: 0x0000002C)

Bit	Mode	Symbol	Description	Reset
7	R/W	mixin_1_amp_en	MIXIN_1 amplifier control 0 = Amplifier disabled 1 = Amplifier enabled	0x0
6	R/W	mixin_1_amp_mute_en	MIXIN_1 amplifier mute control 0 = Amplifier unmuted 1 = Amplifier muted	0x1
5	R/W	mixin_1_amp_ramp_en	MIXIN_1 amplifier gain ramping control. Gain ramping overrides the zero crossing setting. 0 = Ramping is disabled. The gain steps are applied immediately. 1 = Ramping is enabled	0x0
4	R/W	mixin_1_amp_zc_en	MIXIN_1 amplifier zero cross control. When set, gain changes are applied only when the signal crosses zero. 0 = Gain changes are instant 1 = Gain changes are performed when the signal crosses zero	0x0
3	R/W	mixin_1_mix_sel	MIXIN_1 amplifier control 0 = MIXIN_1 amplifier is disabled 1 = MIXIN_1 amplifier is enabled	0x1

Table 167: MIXIN_1_GAIN (Page 0: 0x0000002D)

Bit	Mode	Symbol	Description	Reset
3:0	R/W	mixin_1_amp_gain	MIXIN_1_AMP gain control 0000 = -4.5 dB 0001 = -3.0 dB 0010 = -1.5 dB continuing in 1.5 dB steps to… 1110 = 16.5 dB 1111 = 18.0 dB	0x3

Table 168: MIXIN_2_CTRL (Page 0: 0x0000002E)

Bit	Mode	Symbol	Description	Reset
7	R/W	mixin_2_amp_en	MIXIN_2 amplifier control 0 = MIXIN_2 amplifier disabled 1 = MIXIN_2 amplifier enabled	0x0
6	R/W	mixin_2_amp_mute_en	MIXIN_2 amplifier mute control 0 = MIXIN_2 amplifier unmuted 1 = MIXIN_2 amplifier muted	0x1
5	R/W	mixin_2_amp_ramp_en	MIXIN_2 amplifier gain ramping control. Gain ramping overrides the zero crossing setting. 0 = Ramping is disabled. The gain steps are applied immediately. 1 = Ramping is enabled	0x0
4	R/W	mixin_2_amp_zc_en	MIXIN_2 amplifier zero cross control. When set, gain changes are applied only when the signal crosses zero. 0 = Gain changes are instant 1 = Gain changes are performed when the signal crosses zero	0x0
3	R/W	mixin_2_mix_sel	MIXIN_2 mixer enable. 0 = MIXIN_2 mixer is disabled 1 = MIXIN_2 mixer is enabled	0x1

Table 169: MIXIN_2_GAIN (Page 0: 0x0000002F)

Bit	Mode	Symbol	Description	Reset
3:0	R/W	mixin_2_amp_gain	MIXIN_2_AMP gain control 0000 = -4.5 dB 0001 = -3.0 dB 0010 = -1.5 dB continuing in 1.5 dB steps to… 1110 = 16.5 dB 1111 = 18.0 dB	0x3

Table 170: Register map mixout_cor_00 page 0

Address Name	#	7	6	5	4	3	2	1	0
Register Page 0									
0x000000CC MIXOUT_L_CTRL		mixout_l_amp_en	Reserved						
0x000000CD MIXOUT_L_GAIN		Reserved						mixout_l_amp_gain	
0x000000CE MIXOUT_R_CTRL		mixout_r_amp_en	Reserved						
0x000000CF MIXOUT_R_GAIN		Reserved						mixout_r_amp_gain	

Table 171: MIXOUT_L_CTRL (Page 0: 0x000000CC)

Bit	Mode	Symbol	Description	Reset
7	R/W	mixout_l_amp_en	MIXOUT_L mixer amplifier control 0 = Disabled 1 = Enabled	0x0

Table 172: MIXOUT_L_GAIN (Page 0: 0x000000CD)

Bit	Mode	Symbol	Description	Reset
1:0	R/W	mixout_l_amp_gain	MIXOUT_L gain control 00 = reserved 01 = -1.0 dB 10 = -0.5 dB 11 = 0.0 dB	0x3

Table 173: MIXOUT_R_CTRL (Page 0: 0x000000CE)

Bit	Mode	Symbol	Description	Reset
7	R/W	mixout_r_amp_en	MIXOUT_R mixer amplifier control 0 = Disabled 1 = Enabled	0x0

Table 174: MIXOUT_R_GAIN (Page 0: 0x000000CF)

Bit	Mode	Symbol	Description	Reset
1:0	R/W	mixout_r_amp_gain	MIXOUT_R gain control 00 = Reserved 01 = -1.0 dB 10 = -0.5 dB 11 = 0.0 dB	0x3

Table 175: Register map out_filter_config_cor_00 page 0

Address Name	#	7	6	5	4	3	2	1	0
Register Page 0									
0x00000024 OUT_1_HPF_FILTER_CTRL		out_1_hpf_en	Reserved	out_1_audio_hpf_corner		out_1_voice_en	out_1_voice_hpf_corner		
0x00000025 OUT_1_EQ_12_FILTER_CTRL		out_1_eq_band2				out_1_eq_band1			
0x00000026 OUT_1_EQ_34_FILTER_CTRL		out_1_eq_band4				out_1_eq_band3			
0x00000027 OUT_1_EQ_5_FILTER_CTRL		out_1_eq_en	Reserved			out_1_eq_band5			
0x00000028 OUT_1_BIQ_5STAGE_CTRL		out_1_biq_5stage_filter_en	out_1_biq_5stage_mute_en	Reserved					
0x00000029 OUT_1_BIQ_5STAGE_DATA		out_1_biq_5stage_data							
0x0000002A OUT_1_BIQ_5STAGE_ADDR		Reserved		out_1_biq_5stage_addr					

Table 176: OUT_1_HPF_FILTER_CTRL (Page 0: 0x00000024)

Bit	Mode	Symbol	Description	Reset
7	R/W	out_1_hpf_en	Output audio high pass filter control 0 = Disabled 1 = Enabled	0x1
5:4	R/W	out_1_audio_hpf_corner	Audio HPF 3 dB cut-off control for the Audio HPF At 48 kHz sample rate, the 3 dB cut-off is at: 00 = 2 Hz 01 = 4 Hz 10 = 8 Hz 11 = 16 Hz For other sample rates, the corner cut-off points scale proportionately	0x0
3	R/W	out_1_voice_en	Output voice high pass filter control 0 = Disabled 1 = Enable	0x0
2:0	R/W	out_1_voice_hpf_corner	3dB cut-off for the Voice HPF At 8 kHz sample rate, the 3 dB cut-off is at: 000 = 2.5 Hz 001 = 25 Hz 010 = 50 Hz 011 = 100 Hz 100 = 150 Hz 101 = 200 Hz 110 = 300 Hz 111 = 400 Hz For other sample rates, the corner cut-off points scale proportionately	0x0

Table 177: OUT_1_EQ_12_FILTER_CTRL (Page 0: 0x00000025)

Bit	Mode	Symbol	Description	Reset
7:4	R/W	out_1_eq_band2	Gain control for the band 2 of the 5-Band EQ 0000 = -10.5dB 0001 = -9.0 dB 0010 = -7.5 dB continuing in 1.5 dB steps through… 0111 = 0 dB to... 1101 = 9.0 dB 1110 = 10.5 dB 1111 = 12.0 dB	0x7
3:0	R/W	out_1_eq_band1	Gain control for the band 1 of the 5-Band EQ 0000 = -10.5dB 0001 = -9.0 dB 0010 = -7.5 dB continuing in 1.5 dB steps through… 0111 = 0 dB to... 1101 = 9.0 dB 1110 = 10.5 dB 1111 = 12.0 dB	0x7

Table 178: OUT_1_EQ_34_FILTER_CTRL (Page 0: 0x00000026)

Bit	Mode	Symbol	Description	Reset
7:4	R/W	out_1_eq_band4	Gain control for the band 4 of the 5-Band EQ 0000 = -10.5dB 0001 = -9.0 dB 0010 = -7.5 dB continuing in 1.5 dB steps through… 0111 = 0 dB to... 1101 = 9.0 dB 1110 = 10.5 dB 1111 = 12.0 dB	0x7
3:0	R/W	out_1_eq_band3	Gain control for the band 3 of the 5-Band EQ 0000 = -10.5dB 0001 = -9.0 dB 0010 = -7.5 dB continuing in 1.5 dB steps through… 0111 = 0 dB to... 1101 = 9.0 dB 1110 = 10.5 dB 1111 = 12.0 dB	0x7

Table 179: OUT_1_EQ_5_FILTER_CTRL (Page 0: 0x00000027)

Bit	Mode	Symbol	Description	Reset
7	R/W	out_1_eq_en	5-band EQ control. Note that when enabled, the 5-band EQ will apply a 12 dB attenuation, which can be compensated by OUTFILT digital gain 0 = 5-band EQ disabled 1 = 5-band EQ enabled	0x0
3:0	R/W	out_1_eq_band5	Gain control for the band 5 of the 5-Band EQ 0000 = -10.5dB 0001 = -9.0 dB 0010 = -7.5 dB continuing in 1.5 dB steps through… 0111 = 0 dB to... 1101 = 9.0 dB 1110 = 10.5 dB 1111 = 12.0 dB	0x7

Table 180: OUT_1_BIQ_5STAGE_CTRL (Page 0: 0x00000028)

Bit	Mode	Symbol	Description	Reset
7	R/W	out_1_biq_5stage_filter_en	5-stage BiQuad filter control 0 = 5-stage BiQ filter disabled 1 = 5-stage BiQ filter enabled	0x0
6	R/W	out_1_biq_5stage_mute_en	5-stage BiQuad filter mute control 0 = 5-stage BiQ filter unmuted 1 = 5-stage BiQ filter muted	0x1

Table 181: OUT_1_BIQ_5STAGE_DATA (Page 0: 0x00000029)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	out_1_biq_5stage_data	Data to be written to the coefficient registers of the 5-stage BiQuad filter	0x0

Table 182: OUT_1_BIQ_5STAGE_ADDR (Page 0: 0x0000002A)

Bit	Mode	Symbol	Description	Reset
5:0	R/W	out_1_biq_5stage_addr	Address of the 5-stage biquad coefficient register Even numbered addresses in this register field write the lower byte of the 16-bit cooefficient, and odd numbered addresses write the upper byte of the 16-bit cooefficient A write to the biq_addr register triggers a write of the data	0x0

Table 183: Register map out_filter_cor_00 page 0

Address Name	#	7	6	5	4	3	2	1	0
Register Page 0									
0x00000020 OUT_1L_FILTER_CTRL		out_1l_filter_en	out_1l_mute_en	out_1l_ramp_en	out_1l_subrange_en	out_1l_biq_5stage_sel	Reserved		
0x00000021 OUT_1R_FILTER_CTRL		out_1r_filter_en	out_1r_mute_en	out_1r_ramp_en	out_1r_subrange_en	out_1r_biq_5stage_sel	Reserved		

Table 184: OUT_1L_FILTER_CTRL (Page 0: 0x00000020)

Bit	Mode	Symbol	Description	Reset
7	R/W	out_1l_filter_en	DAC_L control 0 = DAC_L disabled 1 = DAC_L enabled	0x0
6	R/W	out_1l_mute_en	DAC_L mute control 0 = DAC_L unmuted 1 = DAC_L muted	0x1
5	R/W	out_1l_ramp_en	DAC_L digital gain-ramping control 0 = Ramping is disabled. The gain steps are applied immediately. 1 = Ramping is enabled.	0x0
4	R/W	out_1l_subrange_en	DAC_L gain-subrange mode. This register only has an effect if out_1l_ramp_en is set If DAC _L digital gain ramping is enabled (out_1l_ramp_en = 1), and this subranging register field is also set, the ramping process will step though much finer gain increments. 0 = Gain-ramping does not use the intermediate subrange steps 1 = Gain-ramping uses the intermediate subrange steps	0x0
3	R/W	out_1l_biq_5stage_sel	DAC_L 5-stage BiQuad left filter control 0 = 5-stage BiQuad left filter not selected 1 = 5-stage BiQuad left filter selected	0x0

Table 185: OUT_1R_FILTER_CTRL (Page 0: 0x00000021)

Bit	Mode	Symbol	Description	Reset
7	R/W	out_1r_filter_en	DAC_R control 0 = DAC_R disabled 1 = DAC_R enabled	0x0
6	R/W	out_1r_mute_en	DAC_R mute control 0 = DAC_R unmuted 1 = DAC_R muted	0x1
5	R/W	out_1r_ramp_en	DAC_R digital gain-ramping control 0 = Ramping is disabled. The gain steps are applied immediately. 1 = Ramping is enabled.	0x0
4	R/W	out_1r_subrange_en	DAC_R gain-subrange Mode. This register only has an effect if out_1r_ramp_en is set If DAC _R digital gain ramping is enabled (out_1r_ramp_en = 1), and this subranging register field is also set, the ramping process will step though much finer gain increments. 0 = Gain-ramping does not use the intermediate subrange steps 1 = Gain-ramping uses the intermediate subrange steps	0x0
3	R/W	out_1r_biq_5stage_sel	DAC_R 5-stage BiQuad right filter control 0 = 5-stage BiQuad right filter not selected 1 = 5-stage BiQuad right filter selected	0x0

Table 186: Register map pll_cor_00 page 0

Address Name	#	7	6	5	4	3	2	1	0
Register Page 0									
0x00000091 PLL_CTRL		pll_mode		Reserved	pll_mclk_sqr_en	Reserved	pll_indiv		
0x00000092 PLL_FRAC_TOP		Reserved				pll_fbdiv_frac_top			
0x00000093 PLL_FRAC_BOT		pll_fbdiv_frac_bot							
0x00000094 PLL_INTEGER		Reserved	pll_fbdiv_integer						
0x00000095 PLL_STATUS		pll_srm_status							
0x00000098 PLL_REFOSC_CAL		pll_refosc_cal_en	pll_refosc_cal_start	Reserved	pll_refosc_cal_ctrl				

Table 187: PLL_CTRL (Page 0: 0x00000091)

Bit	Mode	Symbol	Description	Reset
7:6	R/W	pll_mode	PLL mode control 00 = Bypass - PLL disabled, and the system clock is MCLK (after input divider) 01 = Normal - PLL enabled, the system clock is a fixed multiple of MCLK 10 = SRM - PLL enabled, and the system clock tracks WCLK 11 = reserved	0x0
4	R/W	pll_mclk_sqr_en	PLL MCLK clock-squarer circuit control 0 = Clock-squarer disabled 1 = Clock-squarer enabled	0x0
2:0	R/W	pll_indiv	PLL reference input clock (MCLK) control 000 = 2 to 4.5 MHz 001 = 4.5 to 9 MHz 010 = 9 to 18 MHz 011 = 18 to 36 MHz 100 = 36 to 54 MHz 101 to 111 = reserved	0x4

Table 188: PLL_FRAC_TOP (Page 0: 0x00000092)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	pll_fbdiv_frac_top	PLL fractional division value (top bits)	0x0

Table 189: PLL_FRAC_BOT (Page 0: 0x00000093)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	pll_fbdiv_frac_bot	PLL fractional division value (bottom bits)	0x0

Table 190: PLL_INTEGER (Page 0: 0x00000094)

Bit	Mode	Symbol	Description	Reset
6:0	R/W	pll_fbdiv_integer	PLL integer division value. Writing to this register causes the entire pll_fbdiv value (PLL_INTEGER, PLL_FRAC_TOP, PLL_FRAC_BOT) to be updated.	0x20

Table 191: PLL_STATUS (Page 0: 0x00000095)

Bit	Mode	Symbol	Description	Reset
7:0	R	pll_srm_status	PLL/SRM status The eight bits represent: bit 0 = MCLK status bit 1 = unused bit 2 = unused bit 3 = PLL lock bit 4 = PLL/SRM active bit 5 = unused bit 6 = unused bit 7 = SRM lock For each bit position: 0 = Inactive or invalid 1 = Active or valid	0x0

Table 192: PLL_REFOSC_CAL (Page 0: 0x00000098)

Bit	Mode	Symbol	Description	Reset
7	R/W	pll_refosc_cal_en	Reference oscillator calibration control 0 = Reference oscillator calibration block is disabled 1 = Reference oscillator calibration block is enabled This register does not control whether or not the reference oscillator runs. The reference oscillator always runs when it is required, that is, when there is no valid MCLK detected and the device is not in standby mode.	0x0
6	R/W	pll_refosc_cal_start	Reference oscillator calibration start control 0 = Do not trigger the reference oscillator calibration 1 = Trigger the reference oscillator calibration	0x0
4:0	R	pll_refosc_cal_ctrl	Reference oscillator control value. This read-only field contains the calibration data for the reference oscillator once it has been calibrated.	0x0

Table 193: Register map references_cor_00 page 0

Address Name	#	7	6	5	4	3	2	1	0
Register Page 0									
0x000000DC REFERENCES		Reserved				bias_en	Reserved		

Table 194: REFERENCES (Page 0: 0x000000DC)

Bit	Mode	Symbol	Description	Reset
3	R/W	bias_en	Master bias control 0 = Master bias disabled 1 = Master bias enabled	0x1

Table 195: Register map router_cor_00 page 0

Address Name	#	7	6	5	4	3	2	1	0
Register Page 0									
0x0000005C DROUTING_OUTDAI_1L		Reserved	outdai_1l_src						
0x0000005D DMIX_OUTDAI_1L_INFILT_1L_GAIN		Reserved			outdai_1l_infilt_1l_gain				
0x0000005E DMIX_OUTDAI_1L_INFILT_1R_GAIN		Reserved			outdai_1l_infilt_1r_gain				
0x0000005F DMIX_OUTDAI_1L_INFILT_2L_GAIN		Reserved			outdai_1l_infilt_2l_gain				
0x00000060 DMIX_OUTDAI_1L_INFILT_2R_GAIN		Reserved			outdai_1l_infilt_2r_gain				
0x00000061 DMIX_OUTDAI_1L_TONEGEN_GAIN		Reserved			outdai_1l_tonegen_gain				
0x00000062 DMIX_OUTDAI_1L_INDAI_1L_GAIN		Reserved			outdai_1l_indai_1l_gain				
0x00000063 DMIX_OUTDAI_1L_INDAI_1R_GAIN		Reserved			outdai_1l_indai_1r_gain				
0x00000064 DROUTING_OUTDAI_1R		Reserved	outdai_1r_src						
0x00000065 DMIX_OUTDAI_1R_INFILT_1L_GAIN		Reserved			outdai_1r_infilt_1l_gain				
0x00000066 DMIX_OUTDAI_1R_INFILT_1R_GAIN		Reserved			outdai_1r_infilt_1r_gain				
0x00000067 DMIX_OUTDAI_1R_INFILT_2L_GAIN		Reserved			outdai_1r_infilt_2l_gain				
0x00000068 DMIX_OUTDAI_1R_INFILT_2R_GAIN		Reserved			outdai_1r_infilt_2r_gain				

Address Name	#	7	6	5	4	3	2	1	0
Register Page 0									
0x00000069 DMIX_OUTDAI_1R_TONEGEN_GAIN		Reserved				outdai_1r_tonegen_gain			
0x0000006A DMIX_OUTDAI_1R_INDAI_1L_GAIN		Reserved				outdai_1r_indai_1l_gain			
0x0000006B DMIX_OUTDAI_1R_INDAI_1R_GAIN		Reserved				outdai_1r_indai_1r_gain			
0x0000006C DROUTING_OUTFILT_1L		Reserved	outfilt_1l_src						
0x0000006D DMIX_OUTFILT_1L_INFILT_1L_GAIN		Reserved				outfilt_1l_infilt_1l_gain			
0x0000006E DMIX_OUTFILT_1L_INFILT_1R_GAIN		Reserved				outfilt_1l_infilt_1r_gain			
0x0000006F DMIX_OUTFILT_1L_INFILT_2L_GAIN		Reserved				outfilt_1l_infilt_2l_gain			
0x00000070 DMIX_OUTFILT_1L_INFILT_2R_GAIN		Reserved				outfilt_1l_infilt_2r_gain			
0x00000071 DMIX_OUTFILT_1L_TONEGEN_GAIN		Reserved				outfilt_1l_tonegen_gain			
0x00000072 DMIX_OUTFILT_1L_INDAI_1L_GAIN		Reserved				outfilt_1l_indai_1l_gain			
0x00000073 DMIX_OUTFILT_1L_INDAI_1R_GAIN		Reserved				outfilt_1l_indai_1r_gain			
0x00000074 DROUTING_OUTFILT_1R		Reserved	outfilt_1r_src						
0x00000075 DMIX_OUTFILT_1R_INFILT_1L_GAIN		Reserved				outfilt_1r_infilt_1l_gain			

Address Name	#	7	6	5	4	3	2	1	0
Register Page 0									
0x00000076 DMIX_OUTFILT_1R_INFILT_1R_GAIN		Reserved				outfilt_1r_infilt_1r_gain			
0x00000077 DMIX_OUTFILT_1R_INFILT_2L_GAIN		Reserved				outfilt_1r_infilt_2l_gain			
0x00000078 DMIX_OUTFILT_1R_INFILT_2R_GAIN		Reserved				outfilt_1r_infilt_2r_gain			
0x00000079 DMIX_OUTFILT_1R_TONEGEN_GAIN		Reserved				outfilt_1r_tonegen_gain			
0x0000007A DMIX_OUTFILT_1R_INDAI_1L_GAIN		Reserved				outfilt_1r_indai_1l_gain			
0x0000007B DMIX_OUTFILT_1R_INDAI_1R_GAIN		Reserved				outfilt_1r_indai_1r_gain			
0x0000007C DROUTING_OUTDAI_2L		Reserved	outdai_2l_src						
0x0000007D DMIX_OUTDAI_2L_INFILT_1L_GAIN		Reserved				outdai_2l_infilt_1l_gain			
0x0000007E DMIX_OUTDAI_2L_INFILT_1R_GAIN		Reserved				outdai_2l_infilt_1r_gain			
0x0000007F DMIX_OUTDAI_2L_INFILT_2L_GAIN		Reserved				outdai_2l_infilt_2l_gain			
0x00000080 DMIX_OUTDAI_2L_INFILT_2R_GAIN		Reserved				outdai_2l_infilt_2r_gain			
0x00000081 DMIX_OUTDAI_2L_TONEGEN_GAIN		Reserved				outdai_2l_tonegen_gain			
0x00000082 DMIX_OUTDAI_2L_INDAI_1L_GAIN		Reserved				outdai_2l_indai_1l_gain			

Address Name	#	7	6	5	4	3	2	1	0
Register Page 0									
0x00000083 DMIX_OUTDAI_2L_INDAI_1R_GAIN		Reserved				outdai_2l_indai_1r_gain			
0x00000084 DROUTING_OUTDAI_2R		Reserved	outdai_2r_src						
0x00000085 DMIX_OUTDAI_2R_INFILT_1L_GAIN		Reserved				outdai_2r_infilt_1l_gain			
0x00000086 DMIX_OUTDAI_2R_INFILT_1R_GAIN		Reserved				outdai_2r_infilt_1r_gain			
0x00000087 DMIX_OUTDAI_2R_INFILT_2L_GAIN		Reserved				outdai_2r_infilt_2l_gain			
0x00000088 DMIX_OUTDAI_2R_INFILT_2R_GAIN		Reserved				outdai_2r_infilt_2r_gain			
0x00000089 DMIX_OUTDAI_2R_TONEGEN_GAIN		Reserved				outdai_2r_tonegen_gain			
0x0000008A DMIX_OUTDAI_2R_INDAI_1L_GAIN		Reserved				outdai_2r_indai_1l_gain			
0x0000008B DMIX_OUTDAI_2R_INDAI_1R_GAIN		Reserved				outdai_2r_indai_1r_gain			

Table 196: DROUTING_OUTDAI_1L (Page 0: 0x0000005C)

Bit	Mode	Symbol	Description	Reset
6:0	R/W	outdai_1l_src	Data input selection control for the OUTDAI_1L output stream bit 0 = Input filter 1 left bit 1 = Input filter 1 right bit 2 = Input filter 2 left bit 3 = Input filter 2 right bit 4 = Tone generator bit 5 = DAI 1 input left data bit 6 = DAI 1 input right data bit 7 = reserved For each bit position: 0 = Input not selected 1 = Input selected	0x1

Table 197: DMIX_OUTDAI_1L_INFILT_1L_GAIN (Page 0: 0x0000005D)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outdai_1l_infilt_1l_gain	Gain control for the INFILT_1L to OUTDAI_1L mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 198: DMIX_OUTDAI_1L_INFILT_1R_GAIN (Page 0: 0x0000005E)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outdai_1l_infilt_1r_gain	Gain control for the INFILT_1R to OUTDAI_1L mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 199: DMIX_OUTDAI_1L_INFILT_2L_GAIN (Page 0: 0x0000005F)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outdai_1l_infilt_2l_gain	Gain control for the INFILT_2L to OUTDAI_1L mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 200: DMIX_OUTDAI_1L_INFILT_2R_GAIN (Page 0: 0x00000060)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outdai_1l_infilt_2r_gain	Gain control for the INFILT_2R to OUTDAI_1L mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 201: DMIX_OUTDAI_1L_TONEGEN_GAIN (Page 0: 0x00000061)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outdai_1l_tonegen_gain	Gain control for the TONEGEN to OUTDAI_1L mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 202: DMIX_OUTDAI_1L_INDAI_1L_GAIN (Page 0: 0x00000062)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outdai_1l_indai_1l_gain	Gain control for the INDAI_1L to OUTDAI_1L mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 203: DMIX_OUTDAI_1L_INDAI_1R_GAIN (Page 0: 0x00000063)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outdai_1l_indai_1r_gain	Gain control for the INDAI_1R to OUTDAI_1L mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 204: DROUTING_OUTDAI_1R (Page 0: 0x00000064)

Bit	Mode	Symbol	Description	Reset
6:0	R/W	outdai_1r_src	Data input selection control for the OUTDAI_1R output stream bit 0 = Input filter 1 left bit 1 = Input filter 1 right bit 2 = Input filter 2 left bit 3 = Input filter 2 right bit 4 = Tone generator bit 5 = DAI 1 input left data bit 6 = DAI 1 input right data bit 7 = reserved For each bit position: 0 = Input not selected 1 = Input selected	0x4

Table 205: DMIX_OUTDAI_1R_INFILT_1L_GAIN (Page 0: 0x00000065)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outdai_1r_infilt_1l_gain	Gain control for the INFILT_1L to OUTDAI_1R mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 206: DMIX_OUTDAI_1R_INFILT_1R_GAIN (Page 0: 0x00000066)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outdai_1r_infilt_1r_gain	Gain control for the INFILT_1R to OUTDAI_1R mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 207: DMIX_OUTDAI_1R_INFILT_2L_GAIN (Page 0: 0x00000067)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outdai_1r_infilt_2l_gain	Gain control for the INFILT_2L to OUTDAI_1R mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 208: DMIX_OUTDAI_1R_INFILT_2R_GAIN (Page 0: 0x00000068)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outdai_1r_infilt_2r_gain	Gain control for the INFILT_2R to OUTDAI_1R mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 209: DMIX_OUTDAI_1R_TONEGEN_GAIN (Page 0: 0x00000069)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outdai_1r_tonegen_gain	Gain control for the TONEGEN to OUTDAI_1R mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 210: DMIX_OUTDAI_1R_INDAI_1L_GAIN (Page 0: 0x0000006A)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outdai_1r_indai_1l_gain	Gain control for the INDAI_1L to OUTDAI_1R mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 211: DMIX_OUTDAI_1R_INDAI_1R_GAIN (Page 0: 0x0000006B)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outdai_1r_indai_1r_gain	Gain control for the INDAI_1R to OUTDAI_1R mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 212: DROUTING_OUTFILT_1L (Page 0: 0x0000006C)

Bit	Mode	Symbol	Description	Reset
6:0	R/W	outfilt_1l_src	Data input selection control for the OUTFILT_1L output stream bit 0 = Input filter 1 left bit 1 = Input filter 1 right bit 2 = Input filter 2 left bit 3 = Input filter 2 right bit 4 = Tone generator bit 5 = DAI 1 input left data bit 6 = DAI 1 input right data bit 7 = reserved For each bit position: 0 = Input not selected 1 = Input selected	0x1

Table 213: DMIX_OUTFILT_1L_INFILT_1L_GAIN (Page 0: 0x0000006D)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outfilt_1l_infilt_1l_gain	Gain control for the INFILT_1L to OUTFILT_1L mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 214: DMIX_OUTFILT_1L_INFILT_1R_GAIN (Page 0: 0x0000006E)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outfilt_1l_infilt_1r_gain	Gain control for the INFILT_1R to OUTFILT_1L mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 215: DMIX_OUTFILT_1L_INFILT_2L_GAIN (Page 0: 0x0000006F)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outfilt_1l_infilt_2l_gain	Gain control for the INFILT_2L to OUTFILT_1L mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 216: DMIX_OUTFILT_1L_INFILT_2R_GAIN (Page 0: 0x00000070)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outfilt_1l_infilt_2r_gain	Gain control for the INFILT_2R to OUTFILT_1L mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 217: DMIX_OUTFILT_1L_TONEGEN_GAIN (Page 0: 0x00000071)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outfilt_1l_tonegen_gain	Gain control for the TONEGEN to OUTFILT_1L mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 218: DMIX_OUTFILT_1L_INDAI_1L_GAIN (Page 0: 0x00000072)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outfilt_1l_indai_1l_gain	Gain control for the INDAI_1L to OUTFILT_1L mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 219: DMIX_OUTFILT_1L_INDAI_1R_GAIN (Page 0: 0x00000073)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outfilt_1l_indai_1r_gain	Gain control for the INDAI_1R to OUTFILT_1L mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 220: DROUTING_OUTFILT_1R (Page 0: 0x00000074)

Bit	Mode	Symbol	Description	Reset
6:0	R/W	outfilt_1r_src	Data input selection control for the OUTFILT_1R output stream bit 0 = Input filter 1 left bit 1 = Input filter 1 right bit 2 = Input filter 2 left bit 3 = Input filter 2 right bit 4 = Tone generator bit 5 = DAI 1 input left data bit 6 = DAI 1 input right data bit 7 = reserved For each bit position: 0 = Input not selected 1 = Input selected	0x4

Table 221: DMIX_OUTFILT_1R_INFILT_1L_GAIN (Page 0: 0x00000075)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outfilt_1r_infilt_1l_gain	Gain control for the INFILT_1L to OUTFILT_1R mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 222: DMIX_OUTFILT_1R_INFILT_1R_GAIN (Page 0: 0x00000076)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outfilt_1r_infilt_1r_gain	Gain control for the INFILT_1R to OUTFILT_1R mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 223: DMIX_OUTFILT_1R_INFILT_2L_GAIN (Page 0: 0x00000077)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outfilt_1r_infilt_2l_gain	Gain control for the INFILT_2L to OUTFILT_1R mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 224: DMIX_OUTFILT_1R_INFILT_2R_GAIN (Page 0: 0x00000078)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outfilt_1r_infilt_2r_gain	Gain control for the INFILT_2R to OUTFILT_1R mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 225: DMIX_OUTFILT_1R_TONEGEN_GAIN (Page 0: 0x00000079)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outfilt_1r_tonegen_gain	Gain control for the TONEGEN to OUTFILT_1R mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 226: DMIX_OUTFILT_1R_INDAI_1L_GAIN (Page 0: 0x0000007A)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outfilt_1r_indai_1l_gain	Gain control for the INDAI_1L to OUTFILT_1R mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 227: DMIX_OUTFILT_1R_INDAI_1R_GAIN (Page 0: 0x0000007B)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outfilt_1r_indai_1r_gain	Gain control for the INDAI_1R to OUTFILT_1R mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 228: DROUTING_OUTDAI_2L (Page 0: 0x0000007C)

Bit	Mode	Symbol	Description	Reset
6:0	R/W	outdai_2l_src	Data input selection control for the OUTDAI_2L output stream bit 0 = Input filter 1 left bit 1 = Input filter 1 right bit 2 = Input filter 2 left bit 3 = Input filter 2 right bit 4 = Tone generator bit 5 = DAI 1 input left data bit 6 = DAI 1 input right data bit 7 = reserved For each bit position: 0 = Input not selected 1 = Input selected	0x4

Table 229: DMIX_OUTDAI_2L_INFILT_1L_GAIN (Page 0: 0x0000007D)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outdai_2l_infilt_1l_gain	Gain control for the INFILT_1L to OUTDAI_2L mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 230: DMIX_OUTDAI_2L_INFILT_1R_GAIN (Page 0: 0x0000007E)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outdai_2l_infilt_1r_gain	Gain control for the INFILT_1R to OUTDAI_2L mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 231: DMIX_OUTDAI_2L_INFILT_2L_GAIN (Page 0: 0x0000007F)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outdai_2l_infilt_2l_gain	Gain control for the INFILT_2L to OUTDAI_2L mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 232: DMIX_OUTDAI_2L_INFILT_2R_GAIN (Page 0: 0x00000080)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outdai_2l_infilt_2r_gain	Gain control for the INFILT_2R to OUTDAI_2L mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 233: DMIX_OUTDAI_2L_TONEGEN_GAIN (Page 0: 0x00000081)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outdai_2l_tonegen_gain	Gain control for the TONEGEN to OUTDAI_2L mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 234: DMIX_OUTDAI_2L_INDAI_1L_GAIN (Page 0: 0x00000082)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outdai_2l_indai_1l_gain	Gain control for the INDAI_1L to OUTDAI_2L mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 235: DMIX_OUTDAI_2L_INDAI_1R_GAIN (Page 0: 0x00000083)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outdai_2l_indai_1r_gain	Gain control for the INDAI_1R to OUTDAI_2L mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 236: DROUTING_OUTDAI_2R (Page 0: 0x00000084)

Bit	Mode	Symbol	Description	Reset
6:0	R/W	outdai_2r_src	Data input selection control for the OUTDAI_2R output stream bit 0 = Input filter 1 left bit 1 = Input filter 1 right bit 2 = Input filter 2 left bit 3 = Input filter 2 right bit 4 = Tone generator bit 5 = DAI 1 input left data bit 6 = DAI 1 input right data bit 7 = reserved For each bit position: 0 = Input not selected 1 = Input selected	0x8

Table 237: DMIX_OUTDAI_2R_INFILT_1L_GAIN (Page 0: 0x00000085)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outdai_2r_infilt_1l_gain	Gain control for the INFILT_1L to OUTDAI_2R mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 238: DMIX_OUTDAI_2R_INFILT_1R_GAIN (Page 0: 0x00000086)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outdai_2r_infilt_1r_gain	Gain control for the INFILT_1R to OUTDAI_2R mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 239: DMIX_OUTDAI_2R_INFILT_2L_GAIN (Page 0: 0x00000087)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outdai_2r_infilt_2l_gain	Gain control for the INFILT_2L to OUTDAI_2R mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 240: DMIX_OUTDAI_2R_INFILT_2R_GAIN (Page 0: 0x00000088)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outdai_2r_infilt_2r_gain	Gain control for the INFILT_2R to OUTDAI_2R mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 241: DMIX_OUTDAI_2R_TONEGEN_GAIN (Page 0: 0x00000089)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outdai_2r_tonegen_gain	Gain control for the TONEGEN to OUTDAI_2R mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 242: DMIX_OUTDAI_2R_INDAI_1L_GAIN (Page 0: 0x0000008A)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outdai_2r_indai_1l_gain	Gain control for the INDAI_1L to OUTDAI_2R mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 243: DMIX_OUTDAI_2R_INDAI_1R_GAIN (Page 0: 0x0000008B)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	outdai_2r_indai_1r_gain	Gain control for the INDAI_1R to OUTDAI_2R mixer path 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 244: Register map sidetone_cor_00 page 0

Address Name	#	7	6	5	4	3	2	1	0
Register Page 0									
0x000000E4 SIDETONE_CTRL		sidetone_filter_en	sidetone_mute_en	Reserved					
0x000000E5 SIDETONE_IN_SELECT		Reserved						sidetone_in_select	
0x000000E6 SIDETONE_GAIN		Reserved			sidetone_gain				
0x000000E8 DROUTING_ST_OUTFILT_1L		Reserved					outfilt_st_1l_src		
0x000000E9 DROUTING_ST_OUTFILT_1R		Reserved					outfilt_st_1r_src		
0x000000EA SIDETONE_BIQ_3STAGE_DATA		sidetone_biq_3stage_data							
0x000000EB SIDETONE_BIQ_3STAGE_ADDR		Reserved			sidetone_biq_3stage_addr				

Table 245: SIDETONE_CTRL (Page 0: 0x000000E4)

Bit	Mode	Symbol	Description	Reset
7	R/W	sidetone_filter_en	SideTone path control 0 = Sidetone path disabled 1 = Sidetone path enabled	0x0
6	R/W	sidetone_mute_en	SideTone mute control 0 = Sidetone not muted 1 = Sidetone muted	0x1

Table 246: SIDETONE_IN_SELECT (Page 0: 0x000000E5)

Bit	Mode	Symbol	Description	Reset
1:0	R/W	sidetone_in_select	Input selection 0 = ADC 1L 1 = ADC 1R 2 = ADC 2L 3 = ADC 2R	0x0

Table 247: SIDETONE_GAIN (Page 0: 0x000000E6)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	sidetone_gain	Sidetone gain control 00000 = -42 dB 00001 = -40.5 dB 00010 = -39.0 dB continuing in 1.5 dB steps through... 11100 = 0 dB to… 11101 = 1.5 dB 11110 = 3.0 dB 11111 = 4.5 dB	0x1C

Table 248: DROUTING_ST_OUTFILT_1L (Page 0: 0x000000E8)

Bit	Mode	Symbol	Description	Reset
2:0	R/W	outfilt_st_1l_src	Data selection control for the OUTFILT_1L output stream: bit 0 = Output filter 1l bit 1 = Output filter 1r (out_1l_filter_en must equal 1 to enable this channel) bit 2 = SideTone For each bit: 0 = Data source not selected 1 = Data source selected	0x1

Table 249: DROUTING_ST_OUTFILT_1R (Page 0: 0x000000E9)

Bit	Mode	Symbol	Description	Reset
2:0	R/W	outfilt_st_1r_src	Data selection control for the OUTFILT_1R output stream bit 0 = Output filter 1l (out_1r_filter_en must equal 1 to enable this channel) bit 1 = Output filter 1r bit 2 = SideTone For each bit: 0 = Data source not selected 1 = Data source selected	0x2

Table 250: SIDETONE_BIQ_3STAGE_DATA (Page 0: 0x000000EA)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	sidetone_biq_3stage_data	Data to be written to the coefficient registers of the 3-stage BiQuad filter	0x0

Table 251: SIDETONE_BIQ_3STAGE_ADDR (Page 0: 0x000000EB)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	sidetone_biq_3stage_addr	Address of the 3-stage biquad coefficient register Even numbered addresses in this register field write the lower byte of the 16-bit cooefficient, and odd numbered addresses write the upper byte of the 16-bit cooefficient A write to the biq_addr register triggers a write of the data	0x0

Table 252: Register map system_controller_cor_00 page 0

<table>
<tr><th>Address Name</th><th>#</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="10">Register Page 0</td></tr>
<tr><td>0x00000014 SYSTEM_MODES_INPUT</td><td></td><td colspan="7">adc_mode</td><td>mode_submit</td></tr>
<tr><td>0x00000015 SYSTEM_MODES_OUTPUT</td><td></td><td colspan="7">dac_mode</td><td>mode_submit</td></tr>
<tr><td>0x00000016 SYSTEM_STATUS</td><td></td><td colspan="6">Reserved</td><td>sc2_busy</td><td>sc1_busy</td></tr>
</table>

Table 253: SYSTEM_MODES_INPUT (Page 0: 0x00000014)

Bit	Mode	Symbol	Description	Reset
7:1	R/W	adc_mode	Preconfigured system modes control (input side) Bit 1 = reserved Bit 2 = MIC_1 Bit 3 = MIC_2 Bit 4 = ADC_1L Bit 5 = ADC_1R Bit 6 = ADC_2L Bit 7 = ADC_2R For each bit: 0 = Disabled 1 = Enabled	0x0
0	R/W	mode_submit	Writing to this register bit causes the System Controller (SCL) to process and activate both the input and the output paths	0x0

Table 254: SYSTEM_MODES_OUTPUT (Page 0: 0x00000015)

Bit	Mode	Symbol	Description	Reset
7:1	R/W	dac_mode	Preconfigured system modes control (output side) [1] = reserved [2] = reserved [3] = reserved [4] = HP_L [5] = HP_R [6] = reserved [7] = reserved	0x0
0	-	mode_submit	Writing to this register bit causes the System Controller (SCL) to process and activate both the input and the output paths	0x0

Table 255: SYSTEM_STATUS (Page 0: 0x00000016)

Bit	Mode	Symbol	Description	Reset
1	R	sc2_busy	Indicates the current status of the System Controller 2 0 = Complete 1 = Busy	0x0
0	R	sc1_busy	Indicates the current status of the System Controller 1 0 = Complete 1 = Busy	0x0

Table 256: Register map tone_gen_cor_00 page 0

<table>
<tr><th>Address Name</th><th>#</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="10">Register Page 0</td></tr>
<tr><td>0x000000A0 TONE_GEN_CFG1</td><td></td><td>start_stopn</td><td colspan="2">Reserved</td><td>dtmf_en</td><td colspan="4">dtmf_reg</td></tr>
<tr><td>0x000000A1 TONE_GEN_CFG2</td><td></td><td colspan="6">Reserved</td><td colspan="2">swg_sel</td></tr>
<tr><td>0x000000A2 TONE_GEN_FREQ1_L</td><td></td><td colspan="8">freq1_l</td></tr>
<tr><td>0x000000A3 TONE_GEN_FREQ1_U</td><td></td><td colspan="8">freq1_u</td></tr>
<tr><td>0x000000A4 TONE_GEN_FREQ2_L</td><td></td><td colspan="8">freq2_l</td></tr>
<tr><td>0x000000A5 TONE_GEN_FREQ2_U</td><td></td><td colspan="8">freq2_u</td></tr>
<tr><td>0x000000A6 TONE_GEN_CYCLES</td><td></td><td colspan="5">Reserved</td><td colspan="3">beep_cycles</td></tr>
<tr><td>0x000000A7 TONE_GEN_ON_PER</td><td></td><td colspan="2">Reserved</td><td colspan="6">beep_on_per</td></tr>
<tr><td>0x000000A8 TONE_GEN_OFF_PER</td><td></td><td colspan="2">Reserved</td><td colspan="6">beep_off_per</td></tr>
</table>

Table 257: TONE_GEN_CFG1 (Page 0: 0x000000A0)

Bit	Mode	Symbol	Description	Reset
7	R/W	start_stopn	Start and stop control for the tone generator. 1 = Start the tone generator. After the tone-generator has finished, it will reset the register to 0. 0 = Stop the tone generator. The tone generator will stop after completion of the current beep cycle. In Continuous mode, setting this register to 0 causes the tone generator to stop after the next zero-cross. Note that this register is cleared automatically once the pre-programmed number of beep cycles has completed.	0x0
4	R/W	dtmf_en	DTMF control 0 = Use values in the freq1 & freq2 registers to generate sine wave(s) 1 = Use values from dtmf_reg to generate sine-waves	0x0
3:0	R/W	dtmf_reg	The DTMF keypad values 0 to 15 (0xE='*', 0xF='#')	0x0

Table 258: TONE_GEN_CFG2 (Page 0: 0x000000A1)

Bit	Mode	Symbol	Description	Reset
1:0	R/W	swg_sel	Sine wave selection control 00 = Sum of both Sine Wave Generator (SWG) values is mixed into the audio. 01 = Only the first SWG value is output 10 = Only the second SWG value is output 11 = 1-Cos(SWG1) or S_ramp function for headphone detection	0x0

Table 259: TONE_GEN_FREQ1_L (Page 0: 0x000000A2)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	freq1_l	Output frequency for first Sine Wave Generator (SWG) lower byte FREQ1=(2^16*(f/12000))-1 for SR=8/12/16/24/32/48/96 kHz FREQ1=(2^16*(f/11025))-1 for SR=11.025/22.05/44.4/88.2 kHz	0x55

Table 260: TONE_GEN_FREQ1_U (Page 0: 0x000000A3)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	freq1_u	Output frequency for first Sine Wave Generator (SWG) upper byte FREQ1=(2^16*(f/12000))-1 for SR=8/12/16/24/32/48/96 kHz FREQ1=(2^16*(f/11025))-1 for SR=11.025/22.05/44.4/88.2 kHz	0x15

Table 261: TONE_GEN_FREQ2_L (Page 0: 0x000000A4)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	freq2_l	Output frequency for second Sine Wave Generator (SWG) lower byte FREQ1=(2^16*(f/12000))-1 for SR=8/12/16/24/32/48/96 kHz FREQ1=(2^16*(f/11025))-1 for SR=11.025/22.05/44.4/88.2 kHz	0x0

Table 262: TONE_GEN_FREQ2_U (Page 0: 0x000000A5)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	freq2_u	Output frequency for second Sine Wave Generator (SWG) upper byte FREQ1=(2^16*(f/12000))-1 for SR=8/12/16/24/32/48/96 kHz FREQ1=(2^16*(f/11025))-1 for SR=11.025/22.05/44.4/88.2 kHz	0x40

Table 263: TONE_GEN_CYCLES (Page 0: 0x000000A6)

Bit	Mode	Symbol	Description	Reset
2:0	R/W	beep_cycles	Control of the number of beep cycles required 000 = 1 cycle 001 = 2 cycles 010 = 3 cycles 011 = 4 cycles 100 = 8 cycles 101 = 16 cycles 110 = 32 cycles 111 = Infinite (until start_stopn is set to 0)	0x0

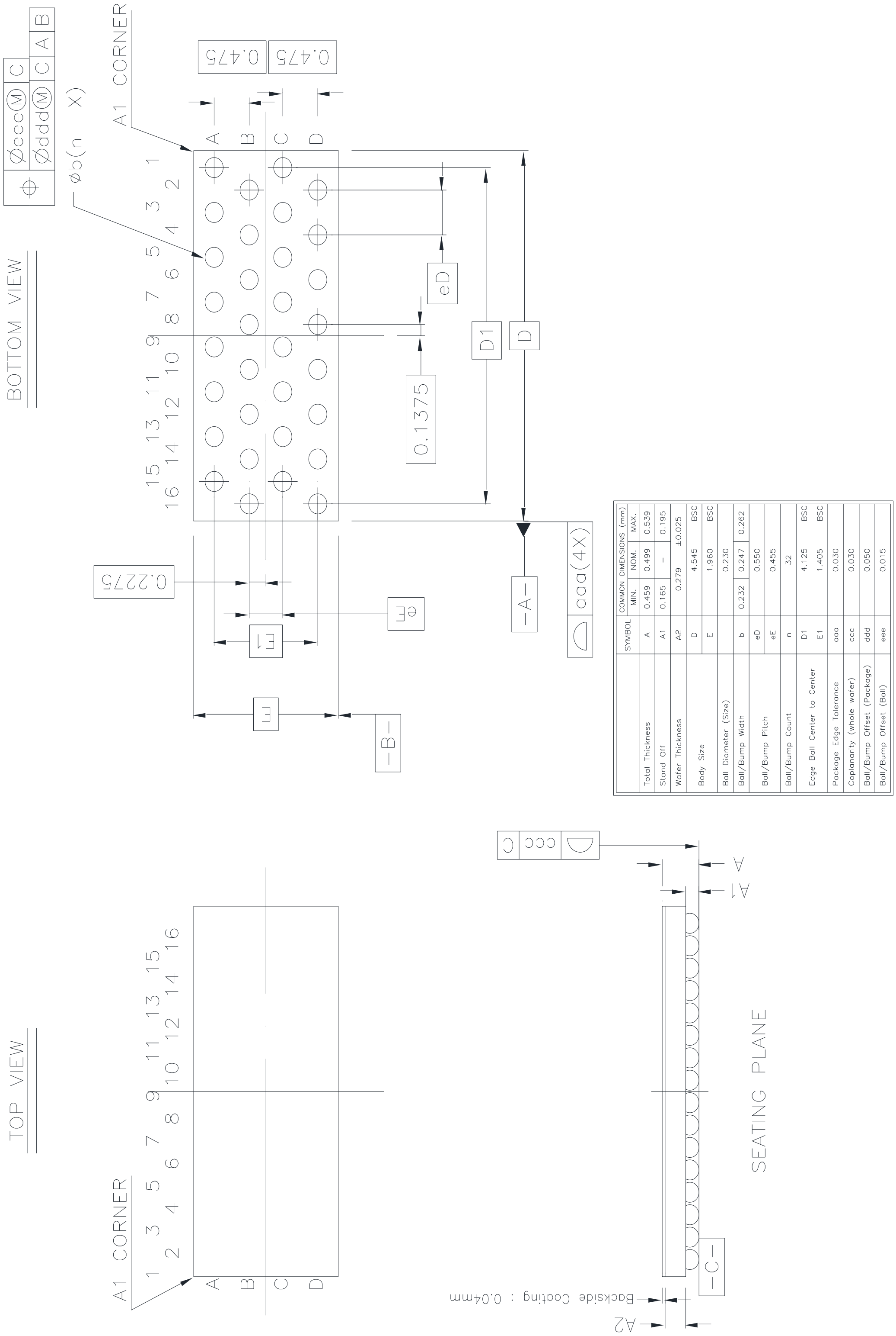
Table 264: TONE_GEN_ON_PER (Page 0: 0x000000A7)

Bit	Mode	Symbol	Description	Reset
5:0	R/W	beep_on_per	Beep cycle on-period control 00 0001 (0x1) = 10 ms 00 0010 (0x2)= 20 ms 00 0011 (0x3)= 30 ms continuing in 10 ms steps to... 01 0100 (0x14) = 200 ms then… 01 0101 (0x15) to 01 1000 (0x18) = reserved then... 01 1001 (0x19) = 250 ms 01 1010 (0x1A) = 300 ms and continuing in 50 ms steps to... 11 1100 (0x3C) = 2000 ms 11 1101 (0x3D) = reserved 11 1110 (0x3E) = reserved 11 1111 (0x3F) = continuous	0x2

Table 265: TONE_GEN_OFF_PER (Page 0: 0x000000A8)

Bit	Mode	Symbol	Description	Reset
5:0	R/W	beep_off_per	Beep cycle off-period control 00 0001 (0x1) = 10 ms 00 0010 (0x2)= 20 ms 00 0011 (0x3)= 30 ms continuing in 10 ms steps to... 01 0100 (0x14) = 200 ms then 01 0101 (0x15) to 01 1000 (0x18) = reserved then... 01 1001 (0x19) = 250 ms 01 1010 (0x1A) = 300 ms and continuing in 50 ms steps to... 11 1100 (0x3C) = 2000 ms 11 1101 (0x3D) = reserved 11 1110 (0x3E) = reserved 11 1111 (0x3F) = continuous	0x1

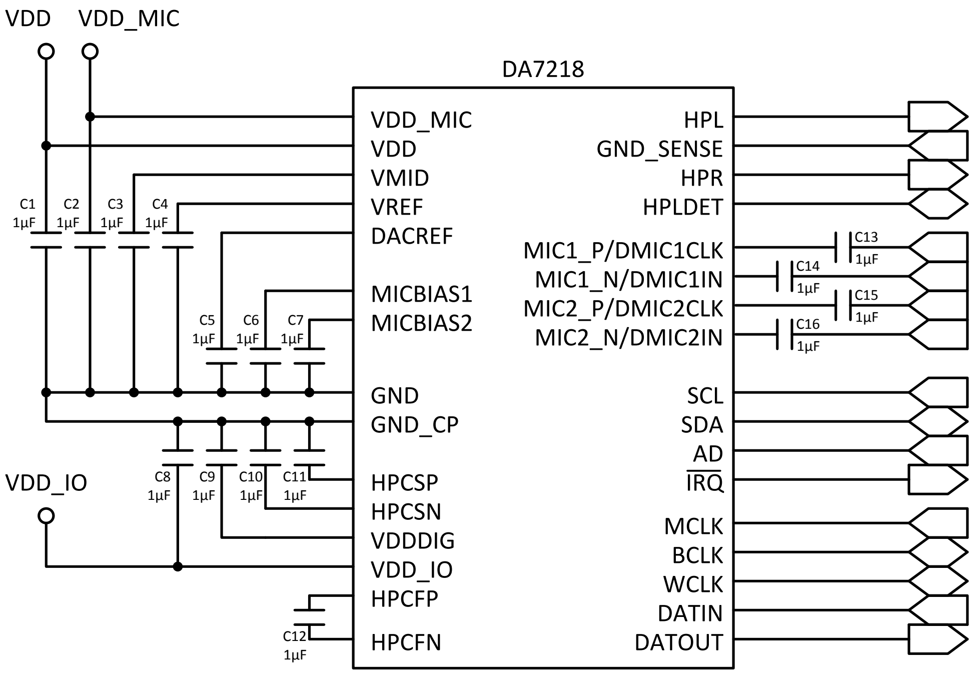
11 Package Information



	SYMBOL	COMMON DIMENSIONS (mm) MIN.	NOM.	MAX.
Total Thickness	A	0.459	0.499	0.539
Stand Off	A1	0.165	–	0.195
Wafer Thickness	A2	0.279	±0.025	
Body Size	D	4.545	BSC	
	E	1.960	BSC	
Ball Diameter (Size)		0.230		
Ball/Bump Width	b	0.232	0.247	0.262
Ball/Bump Pitch	eD	0.550		
	eE	0.455		
Ball/Bump Count	n	32		
Edge Ball Center to Center	D1	4.125	BSC	
	E1	1.405	BSC	
Package Edge Tolerance	aaa	0.030		
Coplanarity (whole wafer)	ccc	0.030		
Ball/Bump Offset (Package)	ddd	0.050		
Ball/Bump Offset (Ball)	eee	0.015		

Figure 36: DA7218 Package Outline Drawing (Rev C)

12 External Components



Notes:

- C2, C6, C7 only required if either MICBIAS is to be used
- C13, C14, C15, C16 only required if analogue inputs are used – DMIC interface has no ac-coupling
- IRQ is open drain and must be pulled up to VDD_IO
- SCL and SDA require pull-up resistors – typical value - 2K2 Ω

Figure 37: DA7218 External Component Requirements

13 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult Dialog Semiconductor's customer portal or your local sales representative.

Table 266: Ordering Information (Samples)

Part Number	Package	Shipment Form	Pack Quantity
DA7218-00U32	32-bump WL-CSP Pb free/green	Tape and Reel (mini reel) (engineering samples only - not for mass production)	100/1000
DA7218-00U36	32-bump WL-CSP Pb free/green	Tray/Waffle Pack (engineering samples only - not for mass production)	77

Table 267: Ordering Information (Production)

Part Number	Package	Shipment Form	Pack Quantity
DA7218-00U32	32-bump WL-CSP Pb free/green	Tape and Reel (13 inch reel)	7500

Appendix A Applications Information

A.1 Codec Initialization

Depending on the specific application, some general settings need to be set. Examples of these settings include the sample rate, the PLL, and the DAI. Then the amplifiers, the mixers and channels of the ADC/DAC have to be configured and enabled via their respective control registers.

An example sequence is shown below:

1. Configure clock mode as required for operation, (for example PLL or PLL bypass).
2. Configure the DAI.
3. Configure the charge pump if the headphone path is in use.
4. Set input and output mixer paths and gains.
5. Enable input and output paths using the Level 2 System Controller (SLC2).

A.2 Automatic Level Control Calibration

When using the automatic level control (ALC or AGS) in sync-mode the DC offset between the digital and analog PGAs must be cancelled. This is performed automatically if the following procedure is performed:

1. Enable microphone amplifiers unmuted.
2. Mute microphones.
3. Enable input mixer and ADC unmuted.
4. Enable AIF interface.
5. Set calib_auto_en in CALIB_CTRL to '1' (CALIB_CTRL = 0x44). This bit will auto-clear when calibration is complete.
6. When calibration is complete, enable the ALC with alc_sync_mode (ALC_CTRL1 = 0x30) and calib_offset_en (CALIB_CTRL = 0x44).
7. Unmute microphones.

Appendix B Components

The following recommended components are examples selected from requirements of a typical application. The electrical characteristics (that is, the supported voltage/current ranges) have to be cross-checked and component types may need to be adapted for the individual needs of the target circuitry.

B.1 Audio Inputs

Table 268: Audio Inputs

Pin Name	Ball No.	Power Domain	Description	Type
MIC1_P/DMIC1CLK	A15	VDD	Differential mic. input 1 (positive) / Single-ended mic. input 1 (left) Or Digital microphone 1 clock	Analog input or digital output
MIC1_N/DMIC1N	B14	VDD	Differential mic. input 1 (negative) / Single-ended mic. input 2 (left) Or Digital microphone 1 data	Analog input or digital input
MIC2_P/DMIC2CLK	D16	VDD	Differential mic. input 2 (positive) / Single-ended mic. input 1 (right) Or Digital microphone 2 clock	Analog input or digital output
MIC2_N/DMIC2IN	C15	VDD	Differential mic. input 2 (negative) / Single-ended mic. input 2 (right) Or Digital microphone 2 data	Analog input or digital input

The DA7218 microphone inputs can be configured to accommodate single-ended or differential analog microphones, line inputs or digital microphones.

When using the inputs in an analog configuration, a DC blocking capacitor is required for each used input. The choice of capacitor is determined by the filter that is formed between that capacitor and the input impedance of the input pin which can be found in Table 6, the Microphone amplifier electrical characteristics section of the datasheet.

$$C = \frac{1}{2\pi . R . F_c}$$

Where Fc is the 3 dB cut off frequency of the low pass filter (typically 20 Hz for audio applications). A 1 µF capacitor is suitable for most applications.

Due to their high stability tantalum capacitors are particularly suitable for this application. Ceramic equivalents with an X5R dielectric are recommended as a cost effective alternative. Care should be taken to ensure that the desired capacitance is maintained over operating temperature and voltage.

Z5U dielectric ceramics should be avoided due to their susceptibility to microphonic effects.

Unused inputs can be left floating or connected via a capacitor to ground.

When the inputs are configured for digital microphones, these pins can be routed directly to a digital microphones clock and data lines. In stereo mode they can be connected to two digital microphones for each data/clock pair to allow up to four digital microphones to be connected to the device. Each data lane is configured to receive data on the rising clock edge for one channel, and on the falling edge for the other channel. The clock output operates at 3.072 MHz or 2.8224 MHz, or 1.536 MHz or 1.4112 MHz. The appropriate layout considerations for clock signals should be followed.

B.2 Microphone Bias

Table 269: Microphone Bias

Pin Name	Bump/Pin	Power Domain	Description	Type
MICBIAS1	B12	VDD_MIC	Microphone bias output 1	Analog output
MICBIAS2	B16	VDD_MIC	Microphone bias output 2	Analog output

A 1 µF capacitor to GND should be used to decouple the MICBIAS output.

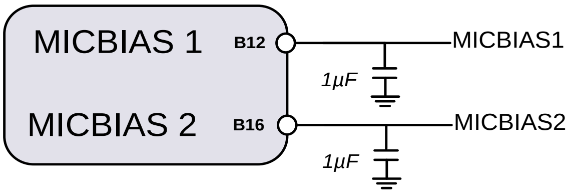


Figure 38: MICBIAS Decoupling

B.3 Audio Outputs

Table 270: DA7218 Headphone Outputs

Pin Name	Bump/Pin	Power Domain	Description	Type
HPL	A5	VDD	Headphone output (left)	Analog output
HPR	A3	VDD	Headphone output (right)	Analog output
GND_SENSE	B4	VDD	Ground reference for headphone output	Analog input
HPLDET	B6	VDD	Headphone left jack detect	Analog input

DA7218 contains a capless true-ground Class-G headphone amplifier with a ground sense connection. For optimum noise immunity the headphone ground sense should be tracked between the HP_L and HP_R signals before being grounded at the headphone connector. In this configuration the ground sense connector cancels common mode noise on the headphone from the PCB.

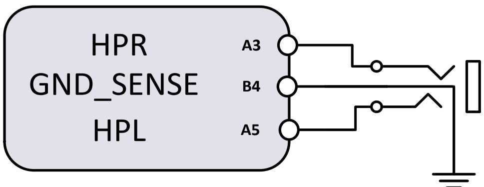


Figure 39: DA7218 Recommended Headphone Layout

B.4 Headphone Charge Pump

Table 271: Headphone Charge Pump

Pin Name	Bump/Pin	Power Domain	Description	Type
HPCSP	A1	VDD	Charge pump reservoir capacitor (pos)	Charge pump
HPCSN	D2	VDD	Charge pump reservoir capacitor (neg)	Charge pump
HPCFP	C1	VDD	Charge pump flying capacitor (pos)	Charge pump
HPCFN	C3	VDD	Charge pump flying capacitor (neg)	Charge pump

A 1 µF reservoir capacitor is required between the HPCSP and GND and between HPCSN and GND when the charge pump is used. For best performance the capacitors should be fitted as near to the device as possible.

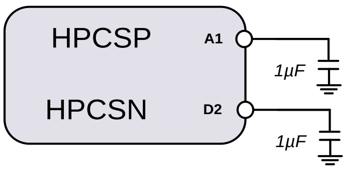


Figure 40: Charge Pump Decoupling

A 1 µF flying capacitor is required between HPCFP and HPCFN. For best performance the capacitor should be fitted as near to the device as possible.

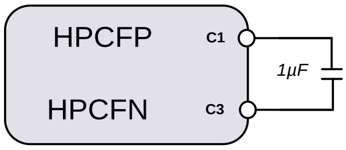


Figure 41: Charge Pump Flying Capacitor

To ensure stable charge pump operation the effective series resistance of the flying capacitor should be kept to a minimum. This can be achieved by selecting an appropriate capacitor dielectric (X5R, X7R) and ensuring that the capacitor is placed as near to the device as possible. Ideally the connection between the pins and the capacitor should not run through any vias. Connect on top layer of PCB only.

B.5 Digital Interfaces

Table 272: Digital Interfaces I^{2}C

Pin Name	Bump/Pin	Power Domain	Description	Type
SDA	D12	VDD_IO	I^{2}C bidirectional data	Digital input / output
SCL	C11	VDD_IO	I^{2}C clock input	Digital input

The I^{2}C data and clock lines are powered from VDD_IO. Both I^{2}C line require a pull up to VDD_IO. The value of this pull up is dependent on I^{2}C bus speed, bus length and supply voltage. A 2.2 kΩ resistor is satisfactory in most applications.

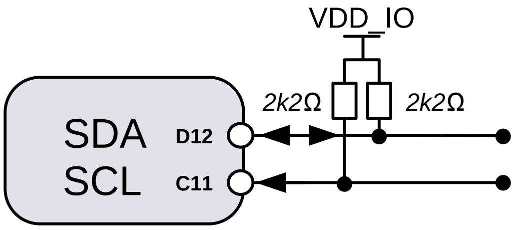


Figure 42: I^2C Pull Ups

Table 273: Digital Interfaces I^2S

Pin Name	Bump/Pin	Power Domain	Description	Type
DATIN	C7	VDD_IO	DAI data input	Digital input
DATOUT	C9	VDD_IO	DAI data output	Digital output
BCLK	D6	VDD_IO	DAI bit clock	Digital input / output
WCLK	D8	VDD_IO	DAI word clock (L/R select)	Digital input / output
MCLK	D10	VDD_IO	Master clock	Digital input

The DAI interface pins should be treated as clock signals and the appropriate layout rules for routing clocks should be adhered to.

B.6 References

Table 274: References

Pin Name	Bump/Pin	Power Domain	Description	Type
VDDDIG	D4	VDD	Digital supply reference capacitor	Reference
VMID	A9	VDD	Audio mid-rail reference capacitor	Reference
VREF	A11	VDD	Bandgap reference capacitor	Reference
DACREF	A7	VDD	Audio DAC reference capacitor	Reference

A 1 µF capacitor should be connected between each of the references and GND. For best performance the capacitors should be fitted as near to the device as possible.

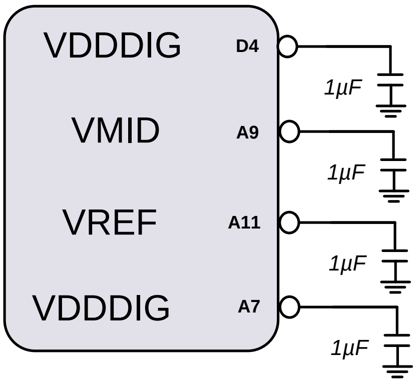


Figure 43: Reference Capacitors

B.7 Supplies

Table 275: Power Supplies

Pin Name	Bump/Pin	Power Domain	Description	Type
VDD	B8	Min: 1.7 V Max: 2.65 V	Supply for analog circuits / Supply for headphone charge pump	Power supply
VDD_IO	C5	Min: 1.5 V Max: 3.6 V	Supply for digital interfaces	Power supply
VDD_MIC	A13	Min: 1.8 V Max: 3.6 V	Supply for microphone bias circuits	Power supply

Decoupling capacitors are recommended between all supplies and GND. These capacitors should be located as near to the device as possible.

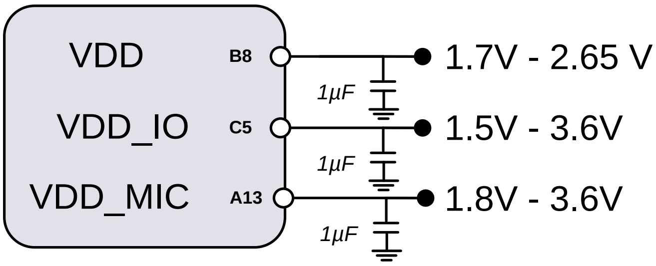


Figure 44: Power Supply Decoupling

B.8 Ground

Table 276: Ground

Pin Name	Bump/Pin	Power Domain	Description	Type
GND	B10		Analog ground	Power ground
GND_CP	B2		Charge pump/digital ground	Power ground

GND and GND_CP should be connected directly to the system ground.

B.9 Capacitor Selection

Ceramic capacitors are manufactured with a variety of dielectrics, each with a different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range, dc bias conditions and low Equivalent Series Resistance (ESR). X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended for best performance. Y5V and Z5U dielectrics are not recommended for use because of their poor temperature and dc bias characteristics.

The worst-case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage is calculated using the following equation:

$$C_{EFF} = C_{OUT}\ x\ (1 - TEMPCO)\ x\ (1 - TOL)$$

Where: CEFF is the effective capacitance at the operating voltage. TEMPCO is the worst-case capacitor temperature coefficient. TOL is the worst-case component tolerance. These figures can be found in the manufacturer’s datasheet.

In the example below, the worst-case temperature coefficient (TEMPCO) over −55 °C to +85 °C is assumed to be 15 %. The tolerance of the capacitor (TOL) is assumed to be 10 %, and COUT is 0.65 µF at 1.8 V.

Substituting these values in the equation yields

$$C_{EFF} = 0.65\mu F\ x\ (1 - 0.15)\ x\ (1 - 0.1) = 0.497\ \mu F$$

Table 277: Recommended Capacitor Types

Application	Value	Size	Temp. Char.	Tolerance	Rated Voltage	Type
VDD,VDD_IO, VDD_MIC, VDDDIG, DACREF, VMID,VREF, HPCFP/HPCFN, HPCSP, HPCSN, MICBIAS1, MICBIAS2	12x 1 µF	0201	X5R +/- 15 %	+/-10 %	6.3 V	Murata GRM033R60J105M

Appendix C PCB Layout Guidelines

DA7218 uses Dialog Semiconductor's 'Route Easy™' technology allowing the device to be routed using conventional, low cost, PCB technology. All device balls are routable on the top level and conventional plated through hole vias can be used throughout.

This design is fully realizable using a 2-layer PCB however for optimum performance it is recommended that a 4-layer PCB is used with layers 2 and 3 as solid ground planes.

Decoupling and reference capacitors should be located as close to the device as possible and appropriately sized tracks should be used for all power connections.

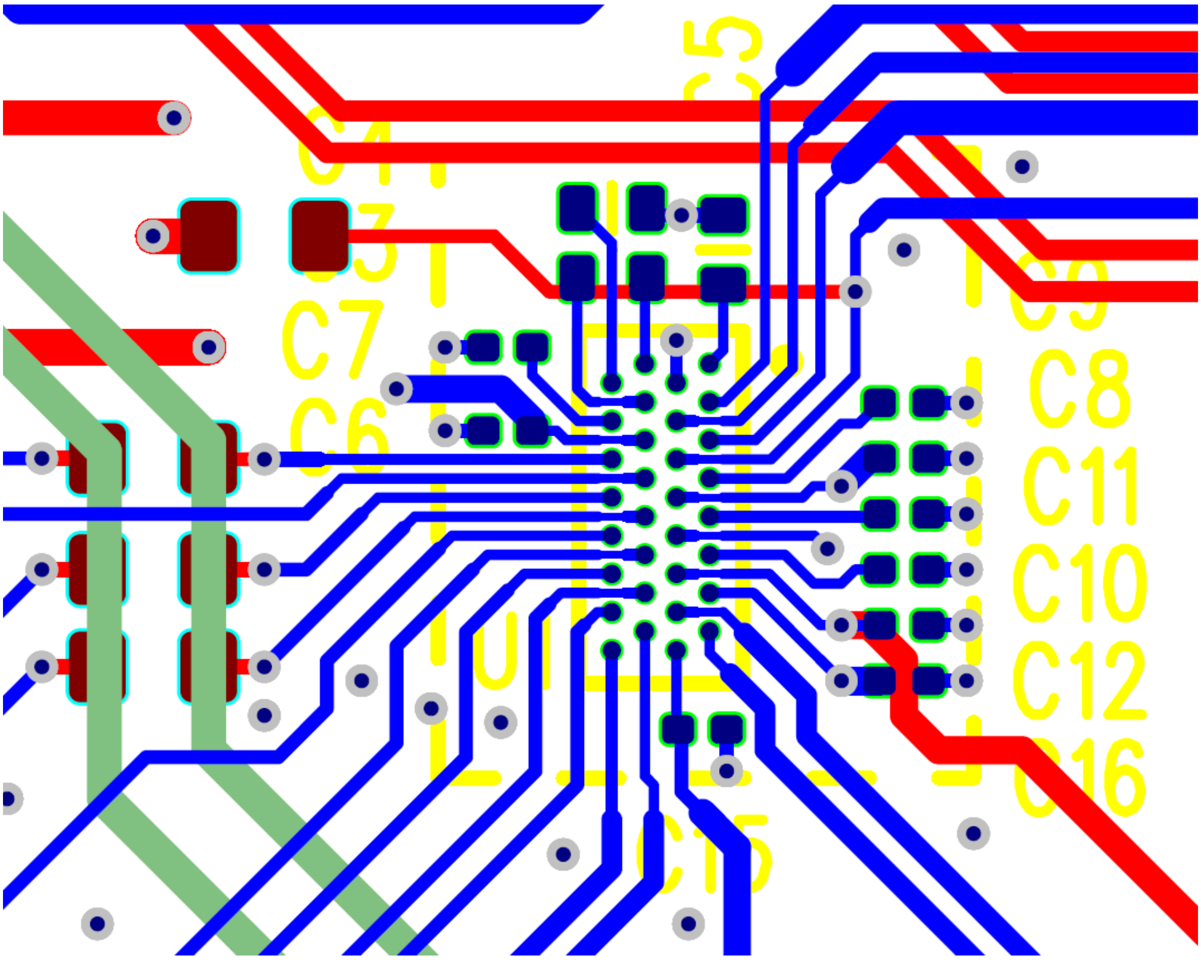


Figure 45: DA7218 Example Layout

C.1 Layout and Schematic Support

Copies of the evaluation board schematics and layout are available on request to aid in PCB development. Dialog Semiconductor also offer a schematic and layout review service for all designs utilizing Dialog's devices. Please contact your local Dialog Semiconductor office.

C.2 General Recommendations

- Appropriate trace width and number of vias should be used for all power supply paths
- A common ground plane should be used, which allows proper electrical and thermal performance
- Noise-sensitive analog signals such as feedback lines or clock connections should be kept away from traces carrying pulsed analog or digital signals. This can be achieved by separation (distance) or by shielding with quiet signals or ground traces
- Decoupling capacitors should be X5R ceramics and should be placed as near to the device as possible
- Charge pump capacitors should be X5R ceramics and should be placed as near to the device as possible

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.dialog-semiconductor.com.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

RoHS Compliance

Dialog Semiconductor's suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

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