

## Data Sheet

Rev. 1.03 / September 2012

# ZSPM4012

High Efficiency 2A Synchronous Buck Converter



*Power and Precision*



# ZSPM4012

High Efficiency 2A Synchronous Buck Converter

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The Analog Mixed Signal Company



## Brief Description

The ZSPM4012 is a DC/DC synchronous switching regulator with fully integrated power switches, internal compensation, and full fault protection. The 1MHz switching frequency enables using small filter components, resulting in reduced board space and reduced bill-of-materials costs.

The ZSPM4012 utilizes current mode feedback in normal regulation pulse-width modulation (PWM) mode. When the regulator is disabled (EN pin is low), the ZSPM4012 draws less than 10 $\mu$ A quiescent current.

The ZSPM4012 integrates a wide range of protection circuitry, including input supply under-voltage lockout, output voltage soft start, current limit, V<sub>OUT</sub> over-voltage, and thermal shutdown.

The ZSPM4012 includes supervisory reporting through the PG (Power Good) open drain output to interface other components in the system.

## Features

- Output voltage options depending on order code:
  - Fixed output voltages: 1.5V, 1.8V, 2.5V, 3.3V, or 5V with  $\pm 2\%$  output tolerance
  - Adjustable output voltage range: 0.9V to 5V with  $\pm 1.5\%$  reference
- Wide input voltage range: 6V to 24V
- 1MHz  $\pm 10\%$  fixed switching frequency
- 2A continuous output current
- High efficiency – up to 95%
- Current mode PWM control with pulse-frequency modulation (PFM) mode for improved light load efficiency
- Voltage supervisor for V<sub>OUT</sub> reported at the PG pin
- Input supply under voltage lockout
- Soft start for controlled startup with no overshoot
- Full protection for over-current, over-temperature, and V<sub>OUT</sub> over-voltage
- Less than 10 $\mu$ A in Disabled Mode
- Low external component count

## Benefits

- Increased battery life
- Minimal external component count (3 capacitors, 1 inductor)
- Inherent fault protection and reporting

## Available Support

- Evaluation Kit
- Documentation

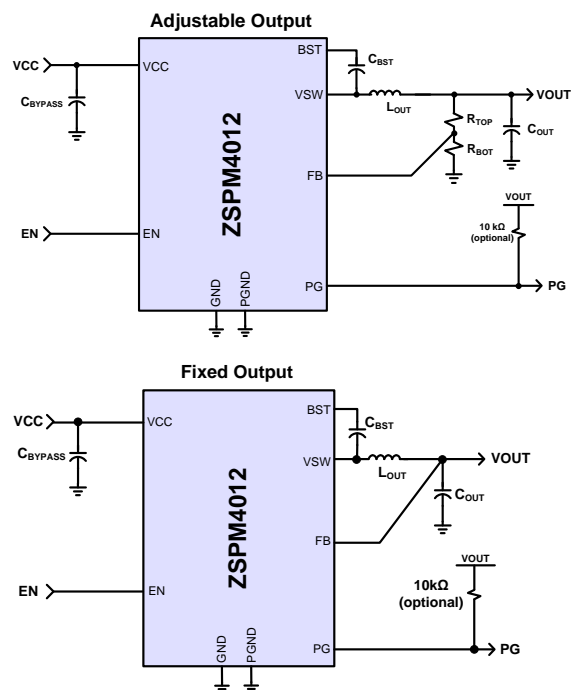
## Physical Characteristics

- Junction operating temperature -40°C to 125°C
- Packaged in a 16pin QFN (3x3mm)

## Related ZMDI Products

- ZSPM4011/ZSPM4013: 1A/3A synchronous buck converters, available with adjustable output from 0.9 to 5V or fixed output voltages at 1.5V, 1.8V, 2.5V, 3.3V, 5.0V (16-pin 3x3 QFN)
- ZSPM1000: >5A single-phase, single-rail, true digital PWM controller (24-pin 4x4mm QFN)

## ZSPM4012 Application Circuits



For more information, contact ZMDI via [analog@zmdi.com](mailto:analog@zmdi.com).

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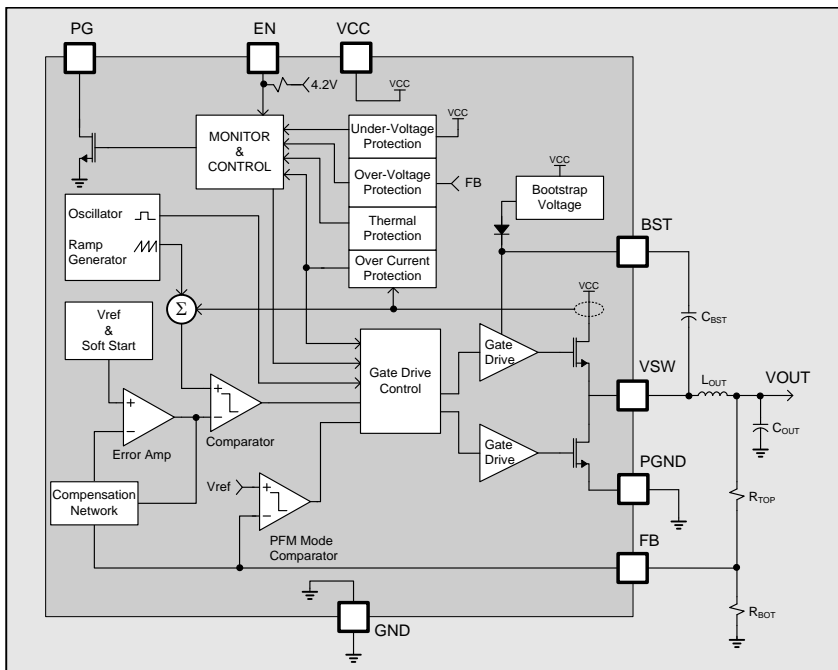
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## ZSPM4012 Block Diagram

### Typical Applications

- Wireless access points, cable modems
- Set-top boxes
- DVD, LCD, LED supplies
- Portable products, including GPS, smart phones, tablet PCs
- Printers



## Ordering Information

| Ordering Code  | Description  | Package               |
|----------------|--|-----------------------|
| ZSPM4012AA1W00 | ZSPM4012, 2A Synchronous Buck Converter: adjustable output, 0.9V to 5V, 16-pin 3x3mm QFN | 7" reel with 1000 ICs |
| ZSPM4012AA1W15 | ZSPM4012, 2A Synchronous Buck Converter: fixed output, 1.5V, 16-pin 3x3mm QFN            | 7" reel with 1000 ICs |
| ZSPM4012AA1W18 | ZSPM4012, 2A Synchronous Buck Converter: fixed output, 1.8V, 16-pin 3x3mm QFN            | 7" reel with 1000 ICs |
| ZSPM4012AA1W25 | ZSPM4012, 2A Synchronous Buck Converter: fixed output, 2.5V, 16-pin 3x3mm QFN            | 7" reel with 1000 ICs |
| ZSPM4012AA1W33 | ZSPM4012, 2A Synchronous Buck Converter: fixed output, 3.3V, 16-pin 3x3mm QFN            | 7" reel with 1000 ICs |
| ZSPM4012AA1W50 | ZSPM4012, 2A Synchronous Buck Converter: fixed output, 5.0V, 16-pin 3x3mm QFN            | 7" reel with 1000 ICs |
| ZSPM4012KIT    | ZSPM4012KIT, Evaluation Kit for 2A Synchronous Buck Converter                            | Kit                   |

## Sales and Further Information

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# ZSPM4012

High Efficiency 2A Synchronous Buck Converter



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## 1 ZSPM4012 Characteristics

Important: Stresses beyond those listed under “Absolute Maximum Ratings” (section 1.1) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” (section 1.3) is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

### 1.1. Absolute Maximum Ratings

Over operating free–air temperature range unless otherwise noted.

**Table 1.1** Absolute Maximum Ratings

| Parameter   | Value <sup>1)</sup> | UNIT |
|---|---------------------|------|
| Voltage on VCC pin  | -0.3 to 26.4        | V    |
| Voltage on BST pin  | -0.3 to (VCC+6)     | V    |
| Voltage on VSW pin  | -1 to 26.4          | V    |
| Voltage on EN, PG, FB pins                                  | -0.3 to 6           | V    |
| Electrostatic Discharge – Human Body Model <sup>2)</sup>    | +/-2k               | V    |
| Electrostatic Discharge – Charge Device Model <sup>2)</sup> | +/-500              | V    |
| Lead Temperature (soldering, 10 seconds)                    | 260                 | °C   |

1) All voltage values are with respect to network ground terminal.  
2) ESD testing is performed according to the respective JESD22 JEDEC standard.

### 1.2. Thermal Characteristics

**Table 1.2** Thermal Characteristics

| Parameter  | Symbol        | Value      | Unit |
|--|---------------|------------|------|
| Thermal Resistance Junction to Air <sup>1)</sup> | $\theta_{JA}$ | 38         | °C/W |
| Storage Temperature Range                        | $T_{STG}$     | -65 to 150 | °C   |
| Maximum Junction Temperature                     | $T_{J\ MAX}$  | 150        | °C   |
| Operating Junction Temperature Range             | $T_J$         | -40 to 125 | °C   |

1) Assumes 1 in<sup>2</sup> area of 2 oz. copper and 25°C ambient temperature.

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## 1.3. Recommended Operating Conditions

**Table 1.3 Recommended Operating Conditions**

| Parameter  | Symbol               | Min  | Typ         | Max  | Unit |
|--|----------------------|------|-------------|------|------|
| Input Operating Voltage  | VCC                  | 6    | 12          | 24   | V    |
| Bootstrap Capacitor  | C <sub>BST</sub>     | 17.6 | 22          | 26.4 | nF   |
| Output Filter Inductor Typical Value <sup>1)</sup>   | L <sub>OUT</sub>     | 3.76 | 4.7         | 5.64 | μH   |
| Output Filter Capacitor Typical Value <sup>2)</sup>  | C <sub>OUT</sub>     | 33   | 44 (2 x 22) |      | μF   |
| Output Filter Capacitor ESR  | C <sub>OUT-ESR</sub> | 2    | 35          | 100  | mΩ   |
| Input Supply Bypass Capacitor Typical Value <sup>3)</sup>  | C <sub>BYPASS</sub>  | 8    | 10          |      | μF   |
| <p>1) For best performance, an inductor with a saturation current rating higher than the maximum V<sub>OUT</sub> load requirement plus the inductor current ripple.</p> <p>2) For best performance, a low ESR ceramic capacitor should be used.</p> <p>3) For best performance, a low ESR ceramic capacitor should be used. If C<sub>BYPASS</sub> is not a low ESR ceramic capacitor, a 0.1μF ceramic capacitor should be added in parallel to C<sub>BYPASS</sub>.</p> |                      |      |             |      |      |

## 1.4. Electrical Characteristics

Electrical Characteristics, T<sub>J</sub> = -40°C to 125°C, VCC = 12V (unless otherwise noted)

**Table 1.4 Electrical Characteristics**

| Parameter  | Symbol                   | Condition   | Min | Typ  | Max | Unit |
|--|--------------------------|---|-----|------|-----|------|
| <b>VCC Supply Voltage</b>                          |                          |   |     |      |     |      |
| Input Supply Voltage                               | VCC                      |   | 6   |      | 24  | V    |
| Quiescent Current:<br>Normal Mode                  | I <sub>CC-NORM</sub>     | VCC = 12V, I <sub>LOAD</sub> = 0A, EN ≥ 2.2               |     | 5.2  |     | mA   |
| Quiescent Current:<br>Normal Mode, Non-switching   | I <sub>CC-NOSWITCH</sub> | VCC=12V, I <sub>LOAD</sub> =0A, EN ≥ 2.2<br>Non-switching |     | 2.3  |     | mA   |
| Quiescent Current:<br>Disabled Mode                | I <sub>CC-DISABLE</sub>  | VCC = 12V, EN = 0V  |     | 5    | 10  | μA   |
| <b>VCC Under Voltage Lockout</b>                   |                          |   |     |      |     |      |
| Input Supply Under Voltage<br>Threshold            | VCC-UV                   | VCC Increasing  | 5.5 | 5.75 | 6.0 | V    |
| Input Supply Under Voltage<br>Threshold Hysteresis | VCC-<br>UV_HYST          |   |     | 650  |     | mV   |
| <b>Oscillator</b>                                  |                          |   |     |      |     |      |
| Oscillator Frequency                               | f <sub>OSC</sub>         |   | 0.9 | 1    | 1.1 | MHz  |



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| Parameter                             | Symbol               | Condition                  | Min | Typ  | Max  | Unit |
|---------------------------------------|----------------------|----------------------------|-----|------|------|------|
| PG Open Drain Output                  |                      |                            |     |      |      |      |
| PG Release Timer                      | T <sub>PG</sub>      |                            |     | 10   |      | Ms   |
| High-Level Output Leakage             | I <sub>OH-PG</sub>   | V <sub>PG</sub> = 5V       |     | 0.5  |      | μA   |
| Low-Level Output Voltage              | V <sub>OL-PG</sub>   | I <sub>PG</sub> = -0.3mA   |     |      | 0.01 | V    |
| EN Input Voltage Thresholds           |                      |                            |     |      |      |      |
| High Level Input Voltage              | V <sub>IH-EN</sub>   |                            | 2.2 |      |      | V    |
| Low Level Input Voltage               | V <sub>IL-EN</sub>   |                            |     |      | 0.8  | V    |
| Input Hysteresis                      | V <sub>HYST-EN</sub> |                            |     | 480  |      | mV   |
| Input Leakage                         | I <sub>IN-EN</sub>   | V <sub>EN</sub> =5V        |     | 3.5  |      | μA   |
|                                       |                      | V <sub>EN</sub> =0V        |     | -1.5 |      | μA   |
| Thermal Shutdown                      |                      |                            |     |      |      |      |
| Thermal Shutdown Junction Temperature | TSD                  | Note: Guaranteed by design | 150 | 170  |      | °C   |
| TSD Hysteresis                        | TSD <sub>HYST</sub>  |                            |     | 10   |      | °C   |

## 1.5. Regulator Characteristics

Electrical Characteristics,  $T_J = -40^{\circ}C$  to  $125^{\circ}C$ ,  $V_{CC} = 12V$  (unless otherwise noted)

| Parameter   | Symbol        | Condition                             | Min             | Typ             | Max               | Unit       |
|---|---------------|---------------------------------------|-----------------|-----------------|-------------------|------------|
| <b>Switch Mode Regulator: <math>L_{OUT}=4.7\mu H</math> and <math>C_{OUT}=2 \times 22\mu F</math></b> |               |                                       |                 |                 |                   |            |
| Output Voltage Tolerance in PWM Mode  | $V_{OUT-PWM}$ | $I_{LOAD} = 1A$                       | $V_{OUT} - 2\%$ | $V_{OUT}$       | $V_{OUT} + 2\%$   | V          |
| Output Voltage Tolerance in PFM Mode  | $V_{OUT-PFM}$ | $I_{LOAD} = 0A$                       | $V_{OUT} - 1\%$ | $V_{OUT} + 1\%$ | $V_{OUT} + 3.5\%$ | V          |
| High Side Switch On Resistance  | $R_{DS(on)}$  | $I_{VSW} = -1A$<br>(See table note 1) |                 | 180             |                   | m $\Omega$ |
| Low Side Switch On Resistance   |               | $I_{VSW} = 1A$<br>(See table note 1)  |                 | 120             |                   | m $\Omega$ |
| Output Current  | $I_{OUT}$     |                                       |                 |                 | 2                 | A          |
| Over Current Detect   | $I_{OCD}$     | HS switch current                     | 2.4             | 2.8             | 3.4               | A          |
| Feedback Reference (Adjustable Mode)  | $FB_{TH}$     |                                       | 0.886           | 0.9             | 0.914             | V          |
| Feedback Reference Tolerance  | $FB_{TH-TOL}$ |                                       | -1.5            |                 | 1.5               | %          |
| Soft Start Ramp Time  | $T_{SS}$      |                                       |                 | 4               |                   | ms         |
| PFM Mode FB Comparator Threshold  | $FB_{TH-PFM}$ |                                       |                 | $V_{OUT} + 1\%$ |                   | V          |



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| Parameter   | Symbol                   | Condition          | Min                  | Typ                   | Max                  | Unit |
|---|--------------------------|--------------------|----------------------|-----------------------|----------------------|------|
| V <sub>OUT</sub> Under Voltage Threshold  | V <sub>OUT-UV</sub>      |                    | 91% V <sub>OUT</sub> | 93% V <sub>OUT</sub>  | 95% V <sub>OUT</sub> |      |
| V <sub>OUT</sub> Under Voltage Hysteresis   | V <sub>OUT-UV_HYST</sub> |                    |                      | 1.5% V <sub>OUT</sub> |                      |      |
| V <sub>OUT</sub> Over Voltage Threshold   | V <sub>OUT-OV</sub>      |                    |                      | 103% V <sub>OUT</sub> |                      |      |
| V <sub>OUT</sub> Over Voltage Hysteresis  | V <sub>OUT-OV_HYST</sub> |                    |                      | 1% V <sub>OUT</sub>   |                      |      |
| Max Duty Cycle  | DUTY <sub>MAX</sub>      | (See table note 2) | 95%                  | 97%                   | 99%                  |      |
| 1) R <sub>DS(on)</sub> is characterized at 1A and tested at lower current in production.          |                          |                    |                      |                       |                      |      |
| 2) Regulator VSW pin is forced off for 240ns every 8 cycles to ensure the BST cap is replenished. |                          |                    |                      |                       |                      |      |

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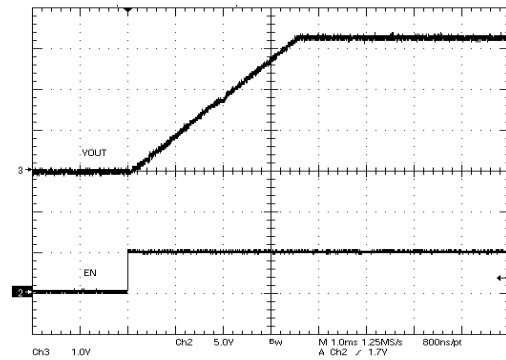
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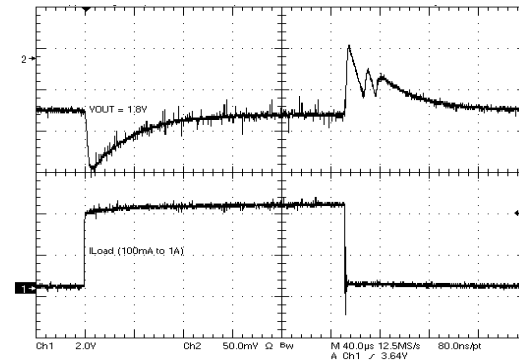
## 2 Typical Performance Characteristics – ZSPM401x Family

Graphs apply to ZSPM401x ICs. See section 1 for ZSPM4012 characteristics. Unless otherwise noted,  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{CC} = 12\text{V}$ .

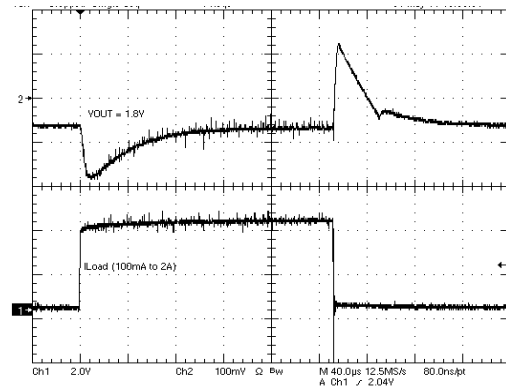
**Figure 2.1 Startup Response**



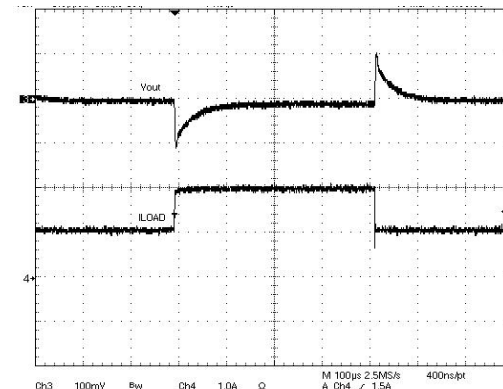
**Figure 2.2 100mA to 1A Load Step ( $V_{CC} = 12\text{V}$ ,  $V_{out} = 1.8\text{V}$ )**



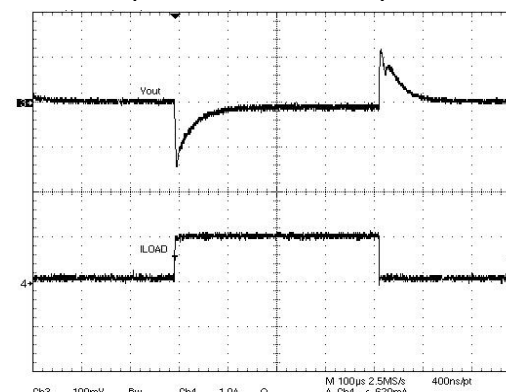
**Figure 2.3 100mA to 2A Load ( $V_{CC} = 12\text{V}$ ,  $V_{out} = 1.8\text{V}$ )**



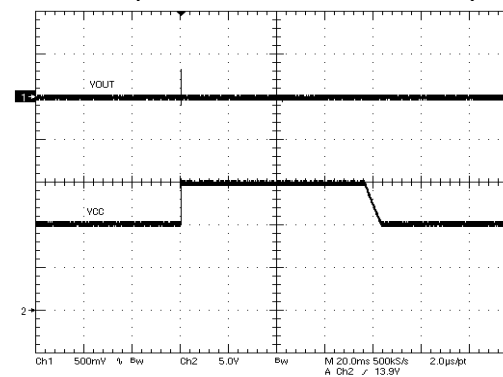
**Figure 2.4 100mA to 1A Load Step ( $V_{CC} = 12\text{V}$ ,  $V_{out} = 3.3\text{V}$ )**



**Figure 2.5 100mA to 2A Load Step ( $V_{CC} = 12\text{V}$ ,  $V_{out} = 3.3\text{V}$ )**



**Figure 2.6 Line Transient Response ( $V_{CC} = 10\text{V}$  to  $15\text{V}$ ,  $V_{out} = 3.3\text{V}$ )**



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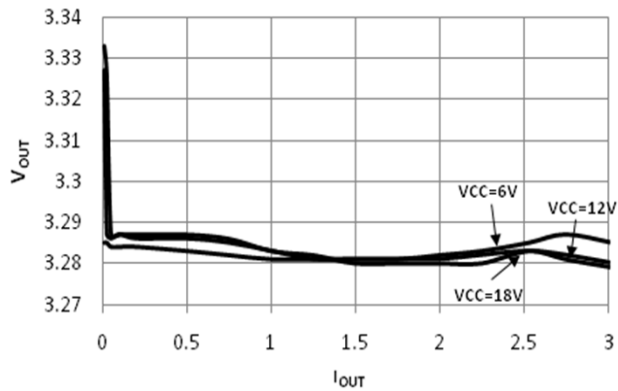
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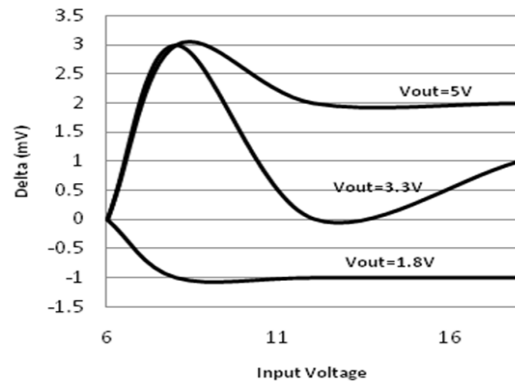
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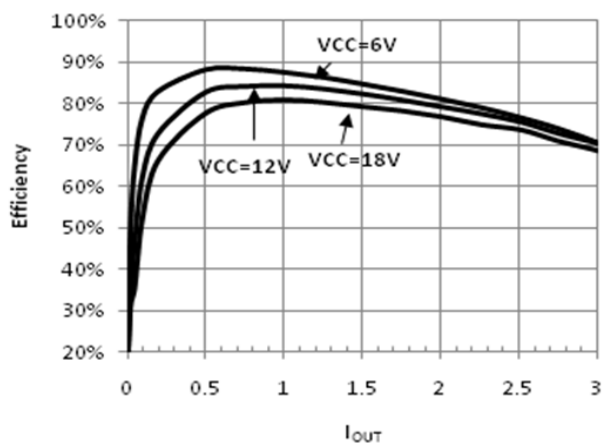
**Figure 2.7 Load Regulation**



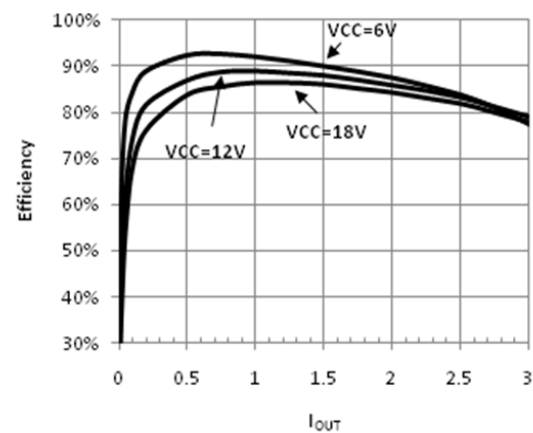
**Figure 2.8 Line Regulation ( $I_{OUT}=1A$ )**



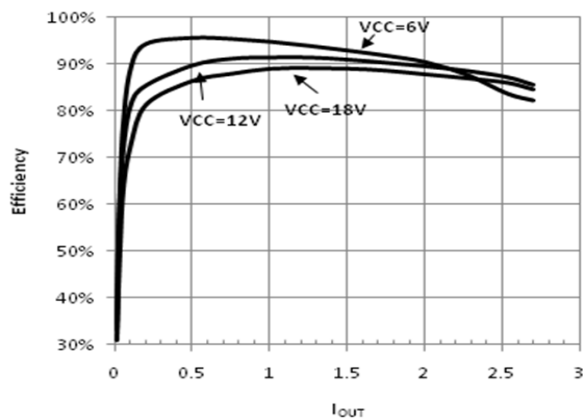
**Figure 2.9 Efficiency vs. Output Current ( $V_{OUT} = 1.8V$ )**



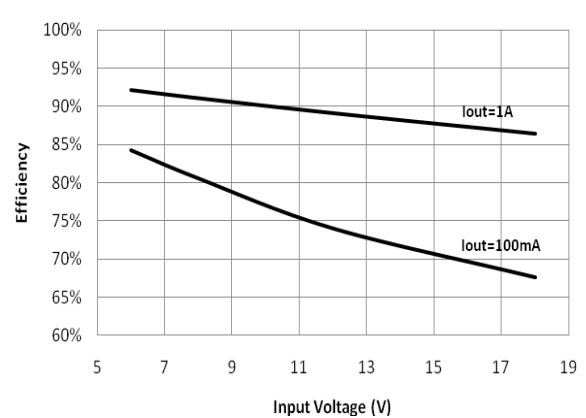
**Figure 2.10 Efficiency vs. Output Current ( $V_{OUT} = 3.3V$ )**



**Figure 2.11 Efficiency vs. Output Current ( $V_{OUT} = 5V$ )**



**Figure 2.12 Efficiency vs. Input Voltage ( $V_{OUT} = 3.3V$ )**



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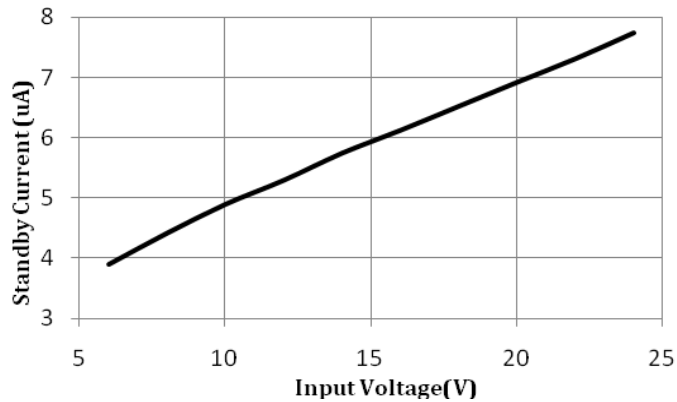
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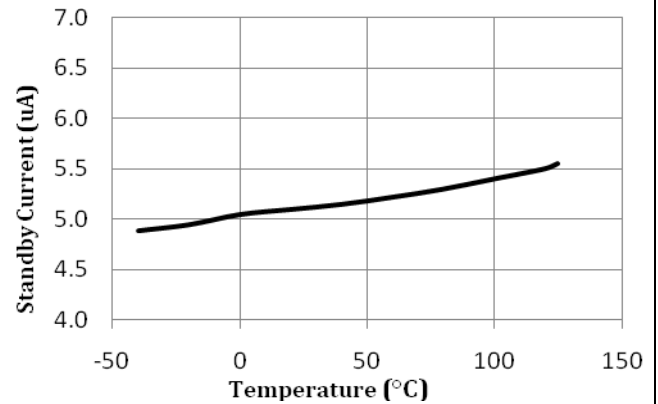
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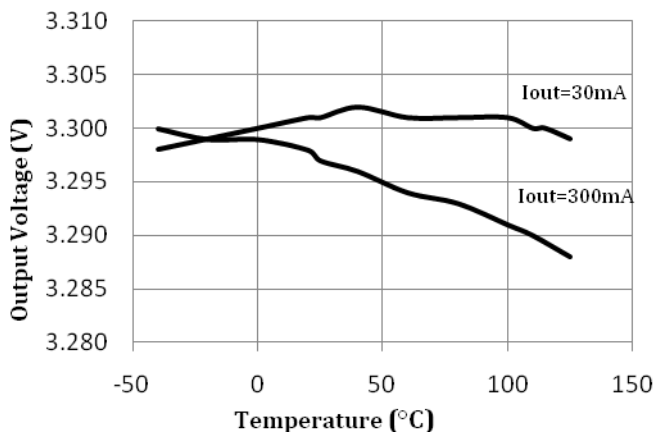
**Figure 2.13 Standby Current vs. Input Voltage**



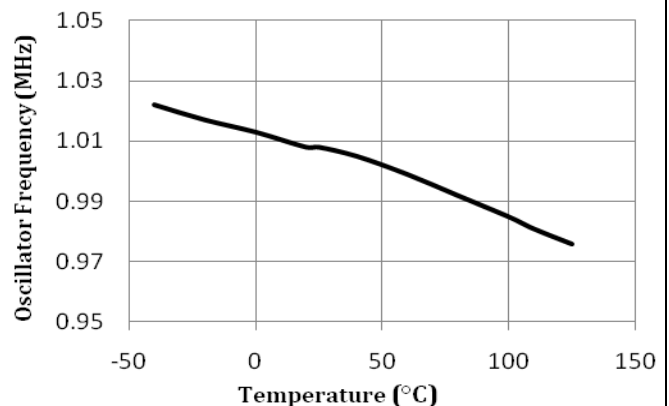
**Figure 2.14 Standby Current vs. Temperature**



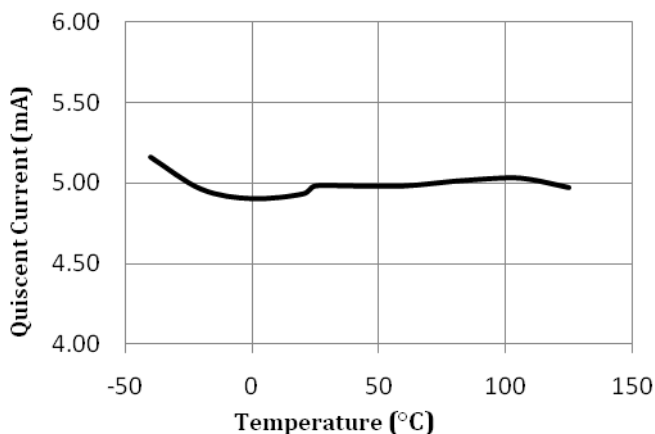
**Figure 2.15 Output Voltage vs. Temperature**



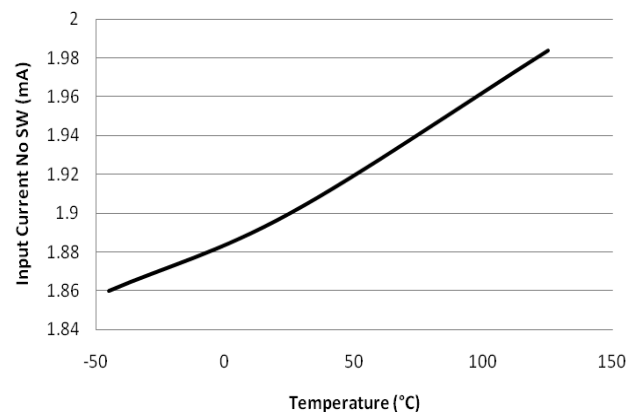
**Figure 2.16 Oscillator Frequency vs. Temperature (Iout=300mA)**



**Figure 2.17 Quiescent Current vs. Temperature (No load)**



**Figure 2.18 Input Current vs. Temperature (No load, No switching)**



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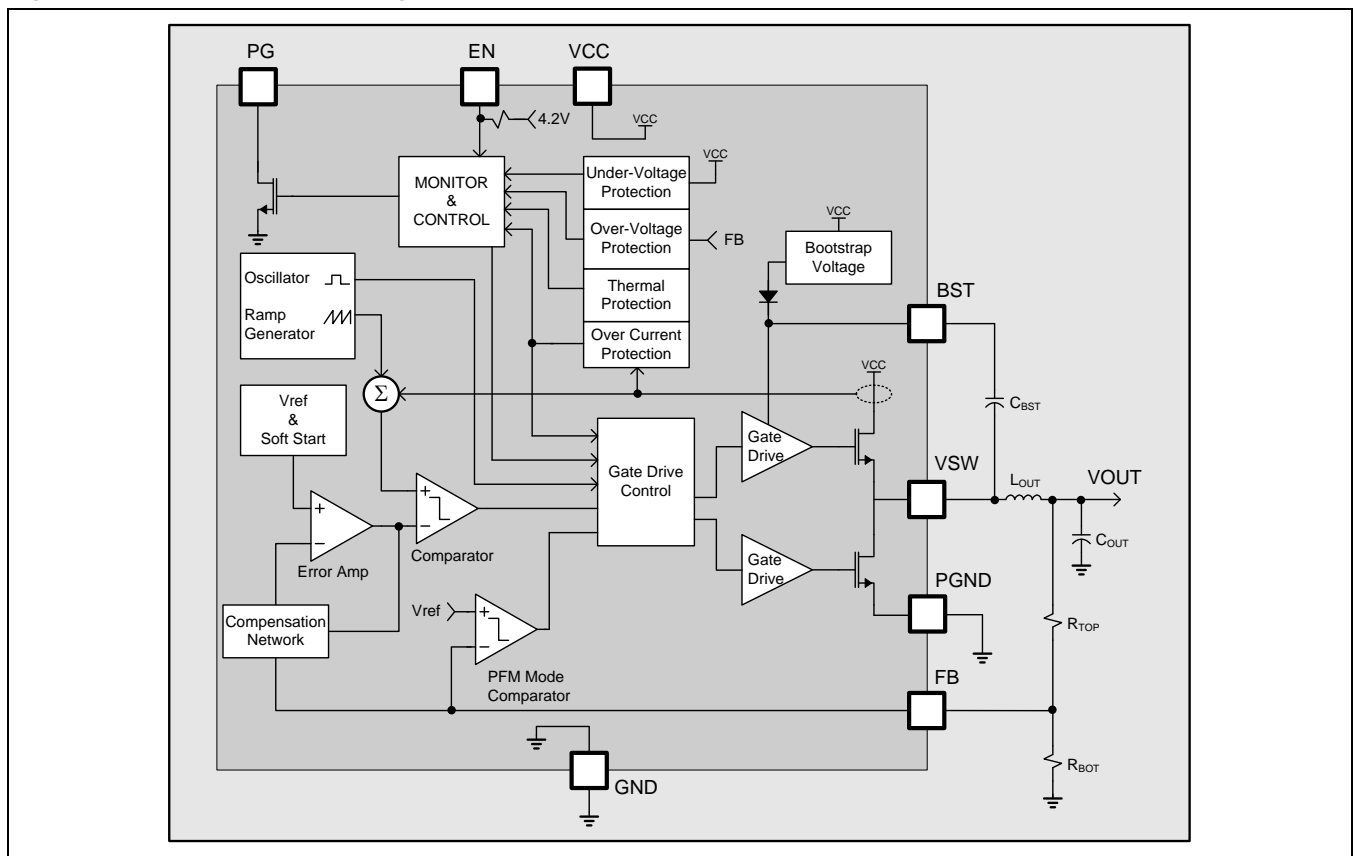
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## 3 Description of Circuit

The ZSPM4012 current-mode synchronous step-down power supply product can be used in the commercial, industrial, and automotive market segments. It includes flexibility for a wide range of output voltages and is optimized for high efficiency power conversion with low  $R_{DS(on)}$  integrated synchronous switches. A 1MHz internal switching frequency facilitates low-cost LC filter combinations. Additionally, the fixed-output versions enable a minimum external component count to provide a complete regulation solution with only 4 external components: an input bypass capacitor, an inductor, an output capacitor, and the bootstrap capacitor. The regulator automatically transitions between PFM and PWM mode to maximize efficiency for the load demand.

**Figure 3.1 ZSPM4012 Block Diagram**



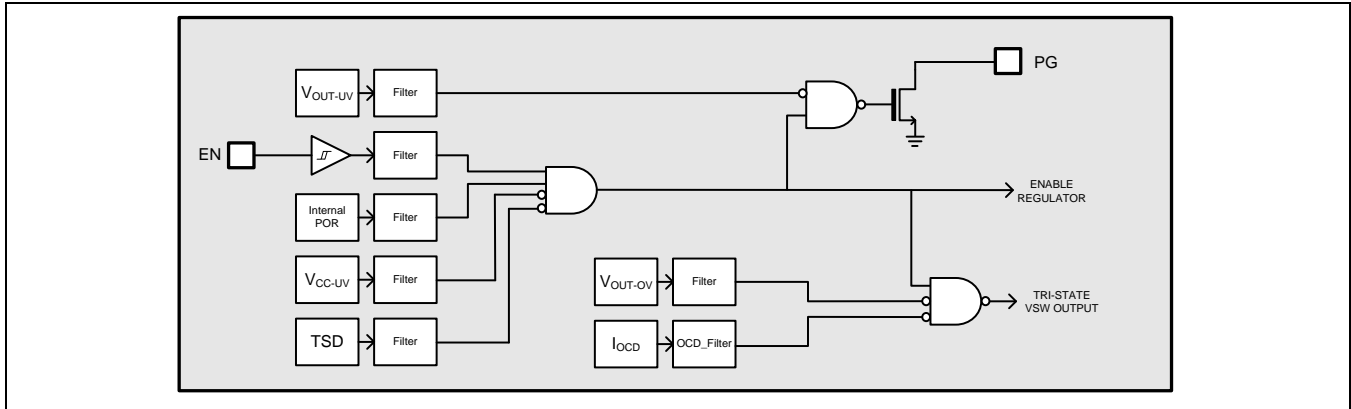
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**Figure 3.2** Monitor and Control Logic Functionality



## 3.1. Internal Protection Details

### 3.1.1. Internal Current Limit

The current through the high side FET is sensed on a cycle-by-cycle basis, and if the current limit is reached, it will abbreviate the cycle. In addition, the device senses the FB pin to identify hard short conditions and will direct the VSW output to skip 4 cycles if the current limit occurs when FB is low. This allows current built up in the inductor during the minimum on time to decay sufficiently. The current limit is always active when the regulator is enabled. Soft start ensures that current limit does not prevent regulator startup.

An additional feature of the over-current protection circuitry is that under extended over-current conditions, the device will automatically disable. A simple toggle of the EN enable pin will return the device to normal operation.

### 3.1.2. Thermal Shutdown

If the temperature of the die exceeds 170°C (typical), the VSW outputs will tri-state to protect the device from damage. The PG and all other protection circuitry will stay active to inform the system of the failure mode. Once the ZSPM4012 cools to 160°C (typical), the device will attempt to start up again, following the normal soft start sequence. If the device reaches 170°C, the shutdown/restart sequence will repeat.

### 3.1.3. Reference Soft-Start

The reference in this device is ramped at a rate of 4ms to prevent the output from overshoot during startup. This ramp restarts whenever there is a rising edge sensed on the EN pin. This occurs in both the fixed and adjustable versions. During the soft start ramp, current limit is still active and still protects the device if the output is shorted.

### 3.1.4. Output Over-Voltage

If the output of the regulator exceeds 103% of the regulation voltage, the VSW outputs will tri-state to protect the ZSPM4012 from damage. This check occurs at the start of each switching cycle. If it occurs during the middle of a cycle, the switching for that cycle will complete and the VSW outputs will tri-state at the start of the next cycle.

### 3.1.5. VCC Under-Voltage Lockout

The ZSPM4012 is held in the off state until VCC reaches 5.75V (typical). There is hysteresis on this input (see section 1.4).



## 4 Application Circuits

### 4.1. Selection of External Components

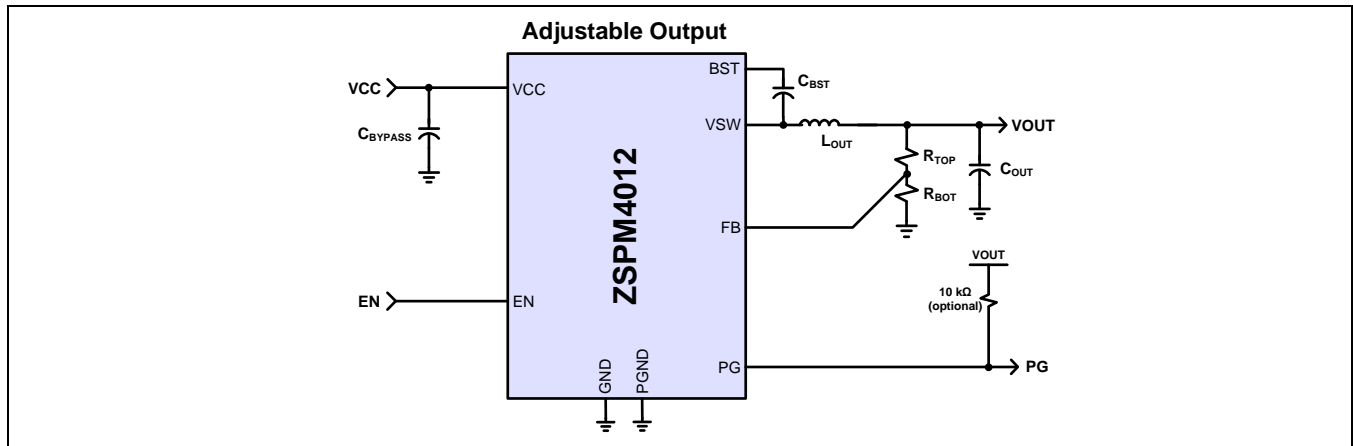
The internal compensation is optimized for a  $44\mu\text{F}$  output capacitor and a  $4.7\mu\text{H}$  inductor. The minimum allowable value for the output capacitor is  $33\mu\text{F}$ . To keep the output ripple low, a low ESR (less than  $35\text{m}\Omega$ ) ceramic is recommended. The inductor range is  $4.7\mu\text{H} \pm 20\%$ . For optimal over-current protection, the inductor should be able to handle up to the regulator current limit without saturation.

Connect the VCC pin to the bypass capacitor  $C_{\text{BYPASS}}$  to improve performance (see section 5.3.1). See Table 1.3 for the recommended value.

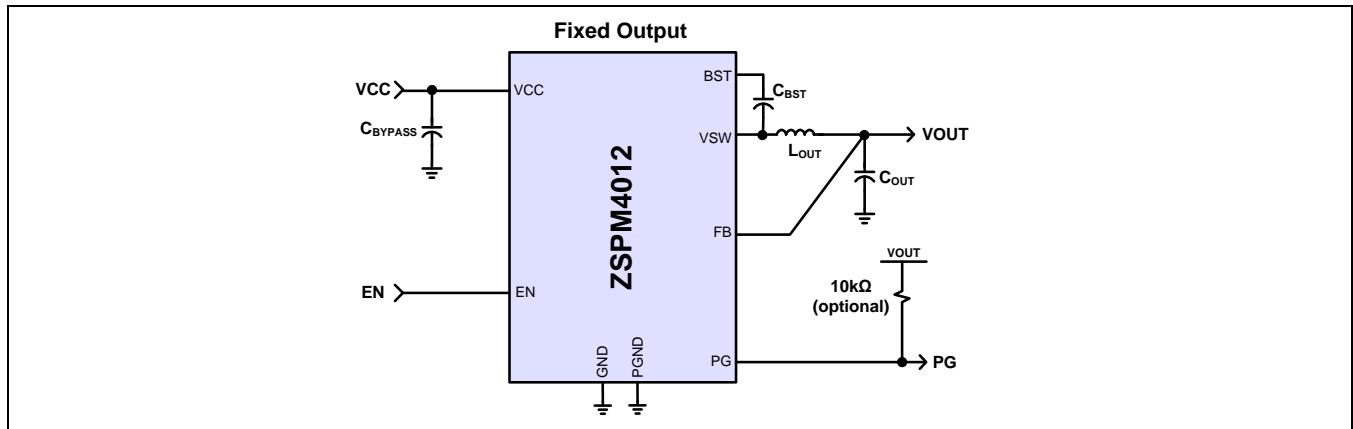
Connect the BST pin to the bootstrap capacitor  $C_{\text{BST}}$  as described in section 5.3.2. See Table 1.3 for the recommended value.

### 4.2. Typical Application Circuits

**Figure 4.1** Typical Application for Adjustable Output Voltage



**Figure 4.2** Typical Application for Fixed Output Voltage





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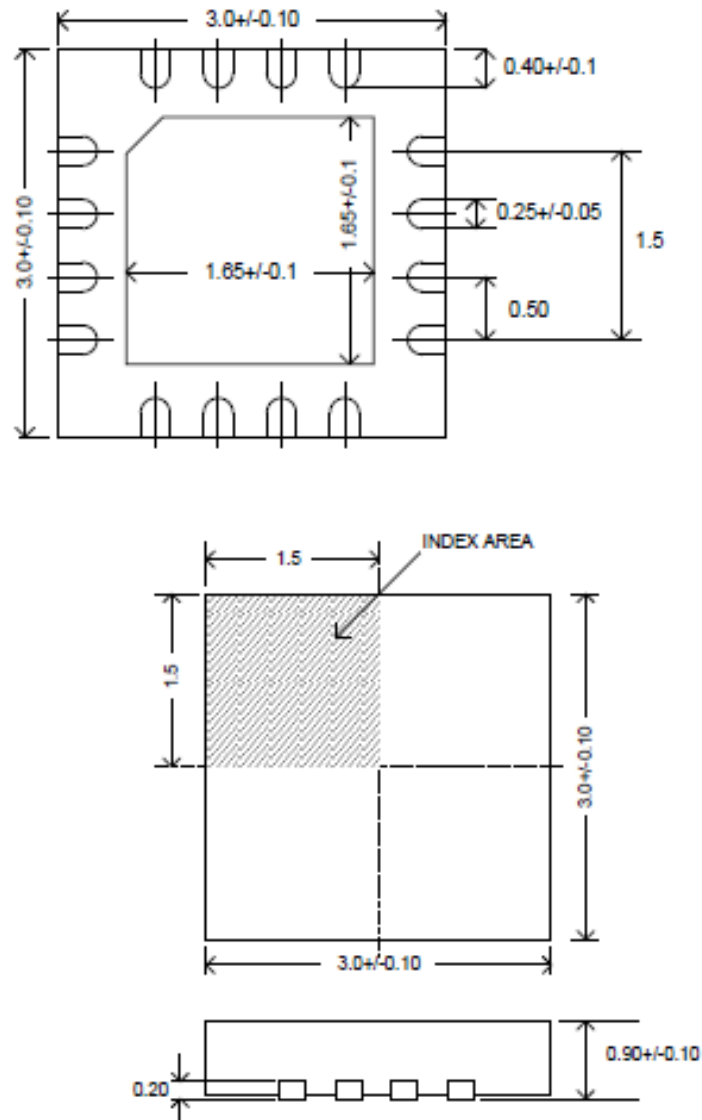
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## 5 Pin Configuration and Package

Figure 5.1 ZSPM4012 Package Drawing



# ZSPM4012

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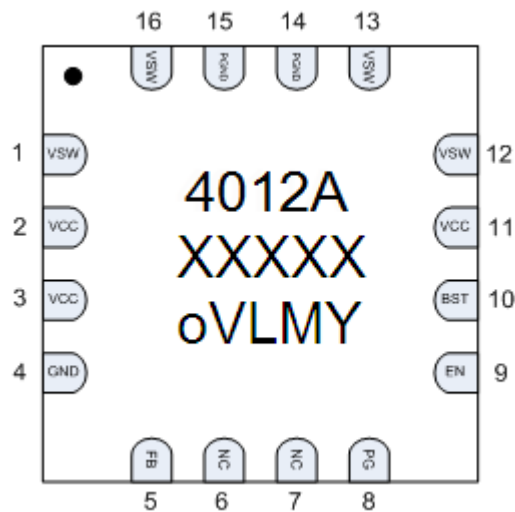
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## 5.1. Marking Diagram & Pin-out

Figure 5.2 16 Lead 3x3mm QFN (top view)



**4012:** Part Name

**A:** Revision

**XXXXX:** Lot number (last five digits)

**O:** Pin 1 mark

**VL:** Voltage level

- 15 1.5V
- 18 1.8V
- 25 2.5V
- 33 3.3V
- 50 5.0V
- 00 0.9V – 5.0V variable

**MY:** Date Code

M = Month

- 1 January
- 2 February
- 3 March
- 4 April
- 5 May
- 6 June
- 7 July
- 8 August
- 9 September
- A October
- B November
- C December

Y = Year

- A 2011
- B 2012
- C 2013
- Etc.

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## 5.2. Pin Description for 16 LEAD 3x3mm QFN

Table 5.1 Pin Description, 16 lead, 3x3mm QFN

| Name | Pin # | Function               | Description  |
|------|-------|------------------------|--|
| VSW  | 1     | Switching Voltage Node | Connected to a 4.7 $\mu$ H (typical) inductor. Also connect to additional VSW pins 12, 13, and 16.               |
| VCC  | 2     | Input Voltage          | Input voltage. Also connect to additional VCC pins 3 and 11.   |
| VCC  | 3     | Input Voltage          | Input voltage. Also connect to additional VCC pins 2 and 11.   |
| GND  | 4     | GND                    | Primary ground for the majority of the device except the low-side power FET.                                     |
| FB   | 5     | Feedback Input         | Regulator FB voltage. Connects to $V_{OUT}$ for fixed-mode and the output resistor divider for adjustable mode.  |
| NC   | 6     | No Connect             | Not connected.   |
| NC   | 7     | No Connect             | Not connected.   |
| PG   | 8     | PG Output              | Open-drain output.   |
| EN   | 9     | Enable Input           | Above 2.2V the device is enabled. Ground this pin to disable the ZSPM4012. Includes internal pull-up.            |
| BST  | 10    | Bootstrap Capacitor    | Bootstrap capacitor for the high-side FET gate driver. Connect a 22nF ceramic capacitor from BST pin to VSW pin. |
| VCC  | 11    | Input Voltage          | Input voltage. Also connect to additional VCC pins 2 and 3.  |
| VSW  | 12    | Switching Voltage Node | Connected to 4.7 $\mu$ H (typical) inductor. Also connect to additional VSW pins 1, 13, and 16.                  |
| VSW  | 13    | Switching Voltage Node | Connected to 4.7 $\mu$ H (typical) inductor. Also connect to additional VSW pins 1, 12, and 16.                  |
| PGND | 14    | Power GND              | GND supply for internal low-side FET/integrated diode. Also connect to additional PGND pin 15.                   |
| PGND | 15    | Power GND              | GND supply for internal low-side FET/integrated diode. Also connect to additional PGND pin 14.                   |
| VSW  | 16    | Switching Voltage Node | Connected to 4.7 $\mu$ H (typical) inductor. Also connect to additional VSW pins 1, 12, and 13.                  |



### 5.3. Detailed Pin Description

#### 5.3.1. Unregulated Input, VCC (Pins # 2, 3)

This terminal is the unregulated input voltage source for the ZSPM4012. It is recommended that a 10 $\mu$ F bypass capacitor be placed close to the device for best performance. Since this is the main supply for the ZSPM4012, good layout practices must be followed for this connection.

#### 5.3.2. Bootstrap Control, BST (Pin #10)

This terminal will provide the bootstrap voltage required for the upper internal NMOS switch of the buck regulator. An external ceramic capacitor placed between the BST input terminal, and the VSW pin will provide the necessary voltage for the upper switch. In normal operation, the capacitor is re-charged on every low side synchronous switching action. If the switch mode approaches 100% duty cycle for the high side FET, the device will automatically reduce the duty cycle switch to a minimum off time on every 8<sup>th</sup> cycle to allow this capacitor to re-charge.

#### 5.3.3. Sense Feedback, FB (Pin #5)

This is the input terminal for the output voltage feedback. For the fixed-mode versions, this should be connected directly to V<sub>OUT</sub>. The connection on the PCB should be kept as short as possible and should be made as close as possible to the capacitor. The trace should not be shared with any other connection. For adjustable-mode versions of the ZSPM4012, this should be connected to the external resistor divider. To choose the resistors, use the following equation:

$$V_{OUT} = 0.9 (1 + R_{TOP}/R_{BOT})$$

The input to the FB pin is high impedance, and input current should be less than 100nA. As a result, good layout practices are required for the feedback resistors and feedback traces. When using the adjustable version, the feedback trace should be kept as short and narrow as possible to reduce stray capacitance and the injection of noise.

#### 5.3.4. Switching Output, VSW (Pins #12, 13)

This is the switching node of the regulator. It should be connected directly to the 4.7 $\mu$ H inductor with a wide, short trace and to one end of the bootstrap capacitor. It is switching between VCC and PGND at the switching frequency.

#### 5.3.5. Ground, GND (Pin #4)

This ground is used for the majority of the device including the analog reference, control loop, and other circuits.

#### 5.3.6. Power Ground, PGND (Pins #14, 15)

This is a separate ground connection used for the low-side synchronous switch to isolate switching noise from the rest of the device.

#### 5.3.7. Enable, High-Voltage, EN (Pin #9)

This is the input terminal to activate the regulator. The input threshold is TTL/CMOS compatible. It also has an internal pull-up to ensure a stable state if the pin is disconnected.

#### 5.3.8. PG Output, PG (Pin #8)

This is an open drain, active low output. The switched mode output voltage is monitored, and the PG line will remain low until the output voltage reaches the V<sub>OUT-UV</sub> threshold. Once the internal comparator detects that the output voltage is above the desired threshold, an internal delay timer is activated and the PG line is de-asserted (to high) once this delay timer expires. In the event that the output voltage decreases below V<sub>OUT-UV</sub>, the PG line will be asserted low and remain low until the output rises above V<sub>OUT-UV</sub> and the delay timer times out. (See Figure 3.2.)

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## 6 Ordering Information

| Ordering Code  | Description  | Package               |
|----------------|--|-----------------------|
| ZSPM4012AA1W00 | ZSPM4012, 2A Synchronous Buck Converter: adjustable output, 0.9V to 5V, 16-pin 3x3mm QFN | 7" reel with 1000 ICs |
| ZSPM4012AA1W15 | ZSPM4012, 2A Synchronous Buck Converter: fixed output, 1.5V, 16-pin 3x3mm QFN            | 7" reel with 1000 ICs |
| ZSPM4012AA1W18 | ZSPM4012, 2A Synchronous Buck Converter: fixed output, 1.8V, 16-pin 3x3mm QFN            | 7" reel with 1000 ICs |
| ZSPM4012AA1W25 | ZSPM4012, 2A Synchronous Buck Converter: fixed output, 2.5V, 16-pin 3x3mm QFN            | 7" reel with 1000 ICs |
| ZSPM4012AA1W33 | ZSPM4012, 2A Synchronous Buck Converter: fixed output, 3.3V, 16-pin 3x3mm QFN            | 7" reel with 1000 ICs |
| ZSPM4012AA1W50 | ZSPM4012, 2A Synchronous Buck Converter: fixed output, 5.0V, 16-pin 3x3mm QFN            | 7" reel with 1000 ICs |
| ZSPM4012KIT    | ZSPM4012KIT, Evaluation Kit for 2A Synchronous Buck Converter                            | Kit                   |

## 7 Related Documents

| Document                                   | File Name                                       |
|--|---|
| <i>ZSPM4012 Feature Sheet</i>              | <i>ZSPM4012_Feature_Sheet_rev_X_xy.pdf</i>      |
| <i>ZSPM4012 Evaluation Kit Description</i> | <i>ZSPM4012_12_13_Eval_Kit_Manual__X_xy.pdf</i> |

Note: X\_xy denotes the current revision of the document. Visit ZMDI's website [www.zmdi.com](http://www.zmdi.com) or contact your nearest sales office for the latest version of these documents.

## 8 Glossary

| Term                      | Description   |
|---------------------------|---|
| Buck converter            | Step-down converter; converts a higher DC input voltage to a lower DC output voltage with high efficiency.  |
| Synchronous Rectification | A technique for improving the efficiency of rectification by replacing diodes with actively controlled switches, such as transistors.   |
| PWM                       | Pulse width modulation (fixed frequency).   |
| PFM                       | Pulse frequency modulation (fixed pulse width).   |
| ESR                       | Equivalent series resistance.   |
| Bootstrap Control         | When using an N-Channel Power MOSFET transistor as a high-side switch for the converter switching output, a gate voltage higher than the supply voltage is needed to turn the transistor fully on. For this purpose, a charge pump circuit, called the bootstrap control, is implemented to provide this high supply voltage for the high-side power MOSFET driver block. |

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## 9 Document Revision History

| Revision | Date        | Description  |
|----------|-------------|--|
| 1.00     | 23-Jan-2012 | First release.   |
| 1.01     | 26-Jan-2012 | Revision to delete note under Table 1.2.   |
| 1.02     | 17-Sep-2012 | Correction of application circuits. PG can only be connected to VOUT through the optional resistor.  |
| 1.03     | 21-Sep-2012 | Table 1.1 removed reference to "Dissipation Table."<br>Added instructions to connect duplicate pins in the pin description table.<br>Revised block diagram graphic for block titled "Under and Over Voltage Protection" to read "Over-Voltage Protection."<br>Removed reference to the R code in the part-ordering table in section 6. This option is not available.<br>Revised reference to "Figure 2" in section 5.3.8 to refer to Figure 3.2. |

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Data Sheet

September 21, 2012

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