X9118

Dual Supply/Low Power/1024-Tap/2-Wire Bus Single Digitally-Controlled (XDCP™) Potentiometer

FN8161
Rev 5.00
April 9, 2014

The X9118 is a single digitally controlled potentiometer (XDCP) on a monolithic CMOS integrated circuit.

The digital controlled potentiometer is implemented using 1023 resistive elements in a series array. Between each element are tap points connected to the wiper terminal through switches. The position of the wiper on the array is controlled by the user through the 2-wire bus interface. The potentiometer has associated with it a volatile Wiper Counter Register (WCR) and a four non-volatile Data Registers that can be directly written to and read by the user. The contents of the WCR controls the position of the wiper on the resistor array though the switches. Power-up recalls the contents of the default data register (DR0) to the WCR.

The XDCP can be used as a three-terminal potentiometer or as a two terminal variable resistors in a wide variety of applications including control, parameter adjustments, and signal processing.

Features

- 1024 resistor taps – 10-bit resolution
- 2-wire serial interface for write, read and transfer operations of the potentiometer
- Wiper resistance, 40Ω typical @ 5V
- Four non-volatile data registers for each potentiometer
- Non-volatile storage of multiple wiper positions
- Power on recall: Loads saved wiper position on power-up
- Standby current < 15µA Max
- System V_{CC}: 2.7V to 5.5V operation
- Analog V+/V-: -5V to +5V
- 100kΩ end-to-end resistance
- Endurance: 100,000 data changes per bit per register
- 100 years data retention
- 14 Ld TSSOP
- Low power CMOS
- Pb-free (RoHS compliant)

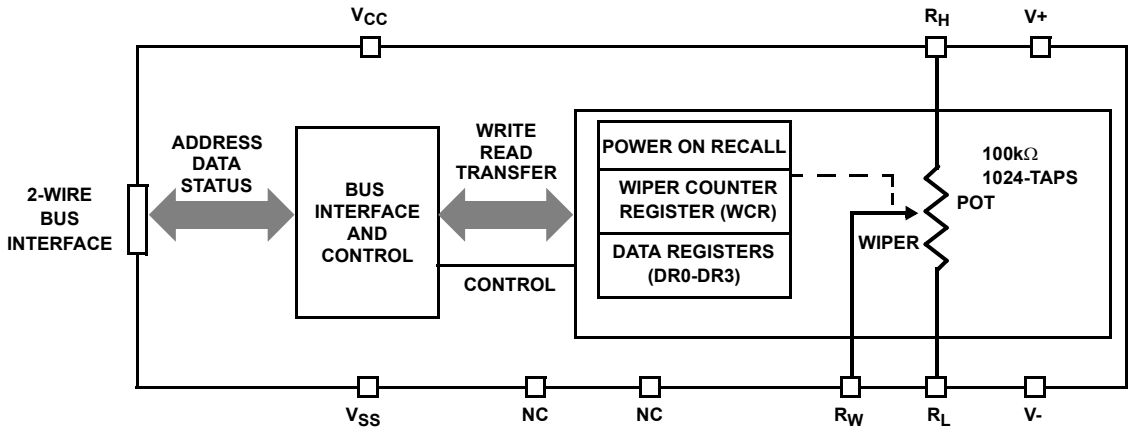
Ordering Information

PART NUMBER (Notes 1, 2)	PART MARKING	VCC LIMITS (V)	POTENTIOMETER ORGANIZATION (kΩ)	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
X9118TV14IZ	X9118 TVZI	5 ±10%	100	-40 to +85	14 Ld TSSOP	M14.173
X9118TV14IZ-2.7	X9118 TVZG	2.7 to 5.5	100	-40 to +85	14 Ld TSSOP	M14.173
X9118TV14Z	X9118 TVZ	5 ±10%	100	0 to +70	14 Ld TSSOP	M14.173
X9118TV14Z-2.7	X9118 TVZF	2.7 to 5.5	100	0 to +70	14 Ld TSSOP	M14.173

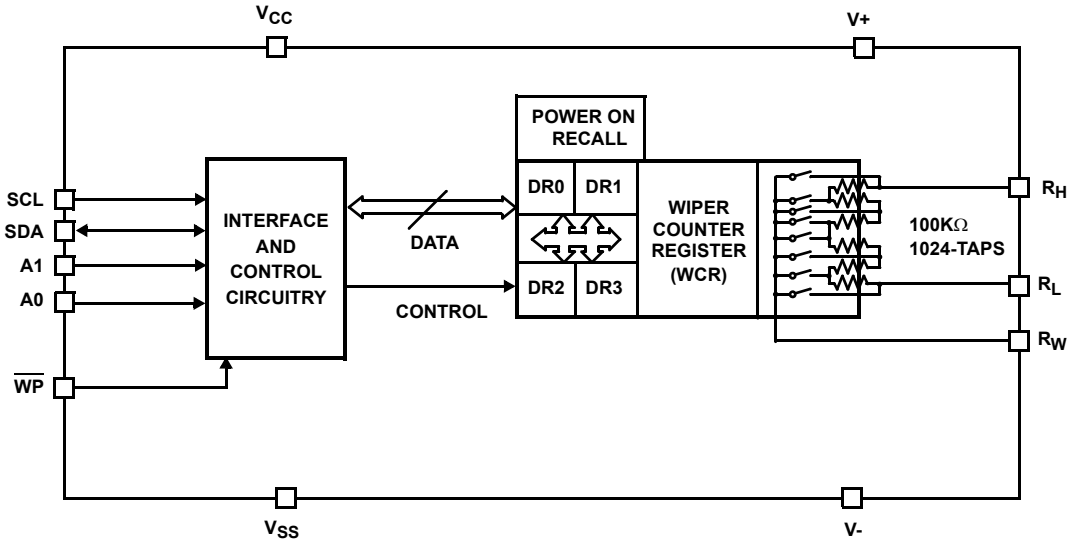
NOTES:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. For Moisture Sensitivity Level (MSL), please see product information page for X9118. For more information on MSL, please see tech brief TB363.

Functional Diagram



Detailed Functional Diagram



Circuit Level Applications

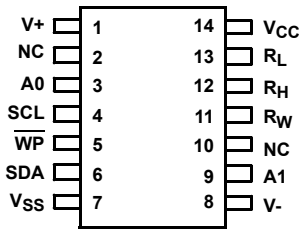
- Vary the gain of a voltage amplifier
- Provide programmable DC reference voltages for comparators and detectors
- Control the volume in audio circuits
- Trim out the offset voltage error in a voltage amplifier circuit
- Set the output voltage of a voltage regulator
- Trim the resistance in Wheatstone bridge circuits
- Control the gain, characteristic frequency and Q-factor in filter circuits
- Set the scale factor and zero point in sensor signal conditioning circuits
- Vary the frequency and duty cycle of timer ICs
- Vary the DC biasing of a pin diode attenuator in RF circuits
- Provide a control variable (I, V, or R) in feedback circuits

System Level Applications

- Adjust the contrast in LCD displays
- Control the power level of LED transmitters in communication systems
- Set and regulate the DC biasing point in an RF power amplifier in wireless systems
- Control the gain in audio and home entertainment systems
- Provide the variable DC bias for tuners in RF wireless systems
- Set the operating points in temperature control systems
- Control the operating point for sensors in industrial systems
- Trim offset and gain errors in artificial intelligent systems

Pinout

X9118
(14 LD TSSOP)
TOP VIEW



Pin Assignments

PIN #	PIN NAME	FUNCTION
1	V+	Analog Supply Voltage
2, 10	NC	No Connect
3	A0	Device Address for 2-wire bus
4	SCL	Serial Clock for 2-wire bus
5	$\overline{WP}$	Hardware Write Protect
6	SDA	Serial Data Input/Output for 2-wire bus
7	V_{SS}	System Ground
8	V-	Analog Supply Voltage
9	A1	Device Address for 2-wire bus
11	R_W	Wiper terminal of the Potentiometer
12	R_H	High terminal of the Potentiometer
13	R_L	Low terminal of the Potentiometer
14	V_{CC}	System Supply Voltage

Pin Descriptions

Bus Interface Pins

SERIAL DATA INPUT/OUTPUT (SDA)

The SDA is a bi-directional serial data input/output pin for a 2-wire slave device and is used to transfer data into and out of the device. It receives device address, opcode, wiper register address and data sent from a 2-wire master at the rising edge of the serial clock SCL, and it shifts out data after each falling edge of the serial clock SCL.

It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs. An open drain output requires the use of a pull-up resistor. The user must account for the capacitance on the bus line and the desired rise and fall times when selecting a pull-up resistor. 2kΩ to 2.5kΩ are typical values when using the maximum clock frequency.

SERIAL CLOCK (SCL)

This input is used by 2-wire master to supply 2-wire serial clock to the X9118.

DEVICE ADDRESS (A1–A0)

The address inputs are used to set the least significant 2 bits of the 8-bit slave address. A match in the slave address serial data stream must be made with the Address input, in order to initiate communication with the X9118. A maximum of 4 XDCP devices may occupy the 2-wire serial bus.

HARDWARE WRITE PROTECT INPUT ($\overline{WP}$)

The $\overline{WP}$ pin when LOW prevents nonvolatile writes to the Data Registers.

Potentiometer Pins

R_H, R_L

The R_H and R_L pins are equivalent to the terminal connections on a mechanical potentiometer.

R_W

The wiper pin is equivalent to the wiper terminal of a mechanical potentiometer.

Bias Supply Pins

SYSTEM SUPPLY VOLTAGE (V_{CC}) AND SUPPLY GROUND (V_{SS})

The V_{CC} pin is the system or digital supply voltage. The V_{SS} pin is the system ground.

ANALOG SUPPLY VOLTAGES (V+ AND V-)

These supplies are the analog voltage supplies for the potentiometer. The V+ supply is tied to the wiper switches while the V- supply is used to bias switches and the internal P+ substrate of the integrated circuit. Both of these supplies set the voltage limits of the potentiometer.

Other Pins

NO CONNECT

No connect pins should be left open. These pins are used for Intersil manufacturing and testing purposes.

Principles of Operation

The X9118 is an integrated microcircuit incorporating a resistor array and its registers and counters and the serial interface logic providing direct communication between the host and the digitally controlled potentiometer. This section provides a detailed description of the following:

- Resistor Array Description
- Serial Interface Description
- Instruction and Register Description

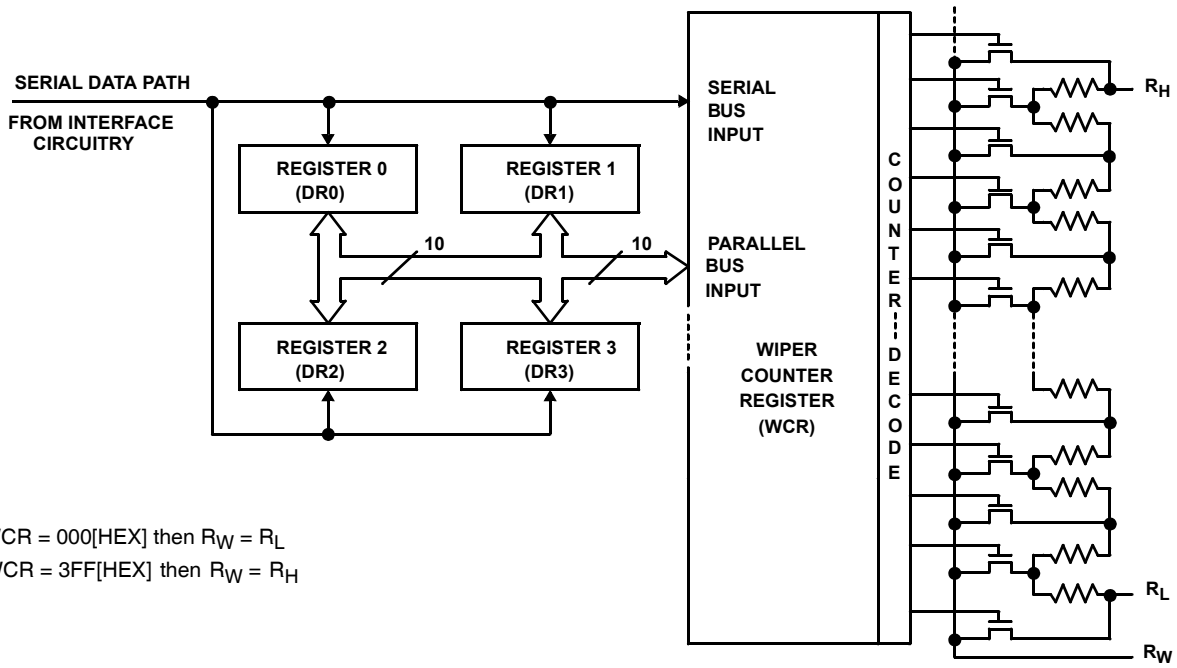


FIGURE 1. DETAILED POTENTIOMETER BLOCK DIAGRAM

Resistor Array Description

The X9118 is comprised of a resistor array. The array contains 1023, in effect, discrete resistive segments that are connected in series (see Figure 1). The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer (R_H and R_L inputs).

At both ends of each array and between each resistor segment is a CMOS switch (transmission gate) connected to the wiper (R_W) output. Within each individual array only one switch may be turned on at a time. These switches are controlled by the wiper counter register (WCR). The 10 bits of the WCR (WCR[9:0]) are decoded to select, and enable, one of 1024 switches.

The WCR may be written directly. The Data Registers and the WCR can be read and written by the host system.

Serial Interface Description

SERIAL INTERFACE – 2-WIRE

The X9118 supports a bi-directional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X9118 will be considered a slave device in all applications.

CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW periods. The SDA state changes during SCL HIGH are reserved for indicating start and stop conditions,
see Figure 3.

START CONDITION

All commands to the X9118 are preceded by the start condition, which is a HIGH-to-LOW transition of SDA while SCL is HIGH. The X9118 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition is met, see Figure 3.

STOP CONDITION

All communications must be terminated by a stop condition, which is a LOW-to-HIGH transition of SDA while SCL is HIGH, see Figure 3.

ACKNOWLEDGE

Acknowledge is a software convention used to provide a positive handshake between the master and slave devices on the bus to indicate the successful receipt of data. The transmitting device, either the master or the slave, will release the SDA bus after transmitting 8 bits. The master generates a ninth clock cycle and during this period the receiver pulls the SDA line LOW to acknowledge that it successfully received the eight bits of data.

The X9118 will respond with an acknowledge after recognition of a start condition and its slave address and once again after successful receipt of the command byte. If the command is followed by a data byte, the X9118 will respond with a final acknowledge, see Figure 2.

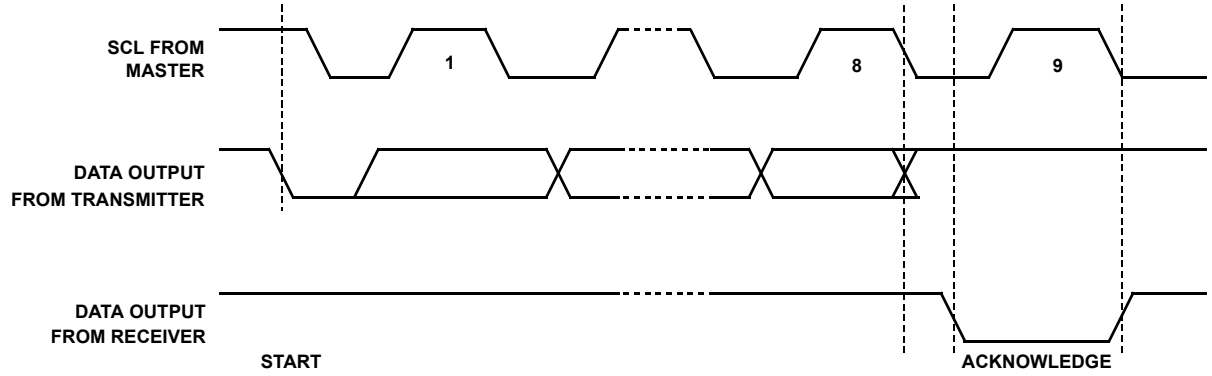
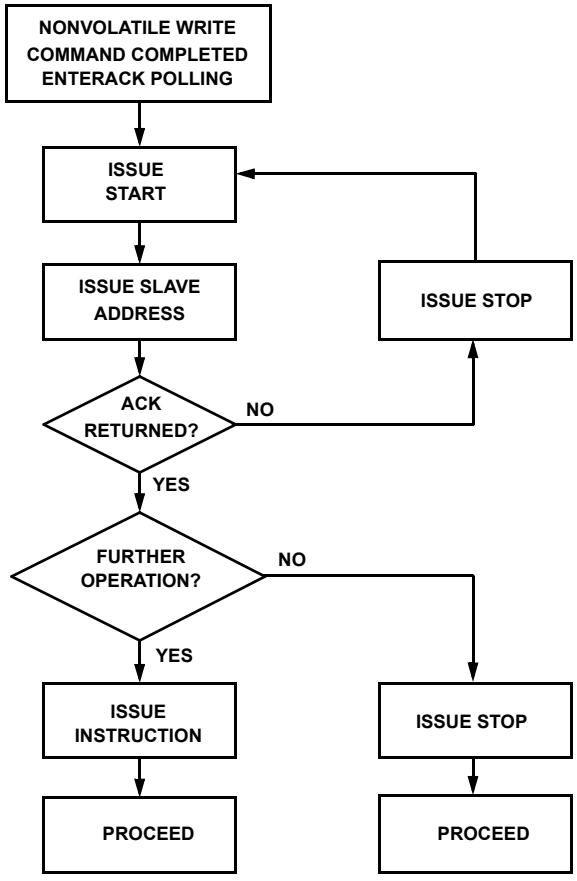


FIGURE 2. ACKNOWLEDGE RESPONSE FROM RECEIVER

ACKNOWLEDGE POLLING

The disabling of the inputs during the internal nonvolatile write operation, can be used to take advantage of the typical 5ms EEPROM write cycle time. Once the stop condition is issued to indicate the end of the nonvolatile write command the X9118 initiates the internal write cycle. The ACK polling, Flow 1, can be initiated immediately. This involves issuing the start condition followed by the device slave address. If the X9118 is still busy with the write operation no ACK will be returned. If the X9118 has completed the write operation an ACK will be returned and the master can then proceed with the next operation.

Flow 1. ACK Polling Sequence



INSTRUCTION AND REGISTER DESCRIPTION

Device Addressing: Identification Byte (ID and A)

Following a start condition, the master must output the address of the slave it is accessing. The most significant 4 bits of the slave address are the device type identifier. The ID[3:0] bits is the device ID for the X9118; this is fixed as 0101[B] (refer to Table 1 on page 6).

The A[1:0] bits in the ID byte are the internal slave address. The physical device address is defined by the state of the A1-A0 input pins. The slave address is externally specified by the user. The X9118 compares the serial data stream with the address input state; a successful compare of both address bits is required for the X9118 to successfully continue the command sequence. Only the device which slave address matches the incoming device address sent by the master executes the instruction. The A1 to A0 inputs can be actively driven by CMOS input signals or tied to V_{CC} or V_{SS}. The $R/\overline{W}$ bit is the LSB and used to set the device for read or write operations.

INSTRUCTION BYTE AND REGISTER SELECTION

The next byte sent to the X9118 contains the instruction and register pointer information. The three most significant bits are used to provide the instruction opcode (I[2:0]). The RB and RA bits point to one of the four registers. The format is shown in Table 2.

Table 3 provides a complete summary of the instruction set opcodes.

TABLE 1. IDENTIFICATION BYTE FORMAT

DEVICE TYPE IDENTIFIES				SET TO 0 FOR PROPER OPERATION	INTERNAL SLAVE ADDRESS		READ OR WRITE BIT
ID3	**ID2**	**ID1**	**ID0**	**0**	**A1**	**A0**	**R/$\overline{W}$**
0	1	0	1	0	A1	A0	R/$\overline{W}$
(MSB)							(LSB)

TABLE 2. INSTRUCTION BYTE FORMAT

INSTRUCTION OPCODE			SET TO 0 FOR PROPER OPERATION	REGISTER SELECTION		SET TO 0 FOR PROPER OPERATION	
I2	**I1**	**I0**	**0**	**RB**	**RA**	**0**	**0**
(MSB)							(LSB)

REGISTER SELECTED	RB	RA
DR0	0	0
DR1	0	1
DR2	1	0
DR3	1	1

TABLE 3. INSTRUCTION SET

INSTRUCTION	R/$\overline{W}$	INSTRUCTION SET								OPERATION
		I_2	I_1	I_0	0	RB	RA	0	0	
Read Wiper Counter Register	1	1	0	0	0	0	0	0	0	Read the contents of the Wiper Counter Register
Write Wiper Counter Register	0	1	0	1	0	0	0	0	0	Write new value to the Wiper Counter Register
Read Data Register	1	1	0	1	0	1/0	1/0	0	0	Read the contents of the Data Register pointed to RB-RA.
Write Data Register	0	1	1	0	0	1/0	1/0	0	0	Write new value to the Data Register pointed to RB-RA.
XFR Data Register to Wiper Counter Register	1	1	1	0	0	1/0	1/0	0	0	Transfer the contents of the Data Register pointed to by RB-RA to the Wiper Counter Register
XFR Wiper Counter Register to Data Register	0	1	1	1	0	1/0	1/0	0	0	Transfer the contents of the Wiper Counter Register to the Data Register pointed to by RB-RA.

NOTE:

3. 1/∅ = data is one or zero.

Instruction and Register Description

Device Addressing

WIPER COUNTER REGISTER (WCR)

The X9118 contains a Wiper Counter Register (see Table 4) for the XDCP potentiometer. The WCR is equivalent to a serial-in, parallel-out register/counter with its outputs decoded to select one of 1024 switches along its resistor array. The contents of the WCR can be altered in one of three ways:

1. It may be written directly by the host via the write Wiper Counter Register instruction (serial load).
2. It may be written indirectly by transferring the contents of one of four associated Data Registers via the XFR Data register.
3. It is loaded with the contents of its Data Register zero (R0) upon power-up.

The Wiper Counter Register is a volatile register; that is, contents are lost when the X9118 is powered down. Although the register is automatically loaded with the value in DR0 upon power-up, this may be different from the value present at power-down. Power-up guidelines are recommended to ensure proper loadings of the DR0 value into the WCR.

DATA REGISTERS (DR)

The potentiometer has four 10-bit non-volatile Data Registers. These can be read or written directly by the host. Data can be transferred between any of the four data registers and the Wiper Counter Register. All operations changing data in one of the Data Registers is a nonvolatile operation and will take a maximum of 10ms.

If the application does not require storage of multiple settings for the potentiometer, the Data Registers can be used as regular memory locations for system parameters or user preference data.

Bit 9 to Bit 0 are used to store one of the 1024 wiper position (0 ~1023).

Four of the six instructions are four bytes in length. These instructions are:

- **Read Wiper Counter Register** – Read the current wiper position of the potentiometer.
- **Write Wiper Counter Register** – Change current wiper position of the potentiometer.
- **Read Data Register** – Read the contents of the selected Data Register.
- **Write Data Register** – Write a new value to the selected Data Register.

The basic sequence of the four byte instructions is illustrated in Figure 3. These four-byte instructions exchange data between the WCR and one of the Data Registers. A transfer from a data register to a WCR is essentially a write to a static RAM, with the static RAM controlling the wiper position. The response of the wiper to this action will be delayed by t_{WRL}. A transfer from the WCR (current wiper position), to a data register is a write to nonvolatile memory and takes a minimum of t_{WR} to complete. The transfer can occur between the potentiometer and one of its associated registers.

Two instructions (see Figure 4) require a two-byte sequence to complete. These instructions transfer data between the host and the X9118; either between the host and one of the Data Registers or directly between the host and the Wiper Counter Register. These instructions are:

- **XFR Data Register to Wiper Counter Register** – This transfers the contents of one specified Data Register to the Wiper Counter Register.
- **XFR Wiper Counter Register to Data Register** –This transfers the contents of the specified Wiper Counter Register to the specified Data Register.

Refer to “Instruction Format” on page 8 for more details.

Other

POWER-UP AND POWER-DOWN REQUIREMENTS

At all times, the V+ voltage must be greater than or equal to the voltage at R_H or R_L, and the voltage at R_H or R_L must be greater than or equal to the voltage at V-. During power-up and power-down, V_{CC}, V+, and V- must reach their final values within 1ms of each other.

TABLE 4. WIPER CONTROL REGISTER, WCR (10-BIT), WCR9 TO WCR0: USED TO STORE THE CURRENT WIPER POSITION (VOLATILE, V)

WCR9	WCR8	WCR7	WCR6	WCR5	WCR4	WCR3	WCR2	WCR1	WCR0
V	V	V	V	V	V	V	V	V	V
(MSB)									(LSB)

TABLE 5. DATA REGISTER, DR (10-BIT), BIT 9 TO BIT 0: USED TO STORE WIPER POSITIONS OR DATA (NON-VOLATILE, NV)

BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NV	NV	NV	NV	NV	NV	NV	NV	NV	NV
MSB									LSB

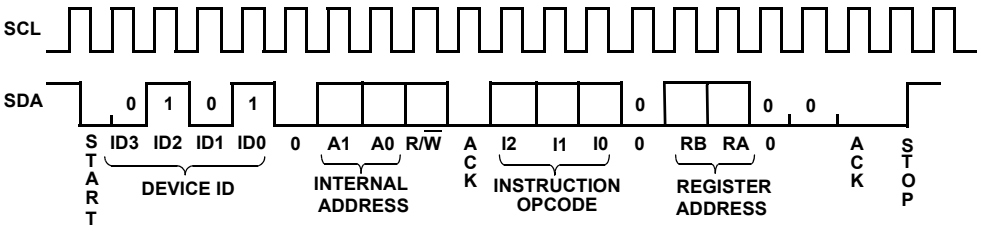


FIGURE 3. TWO-BYTE INSTRUCTION SEQUENCE

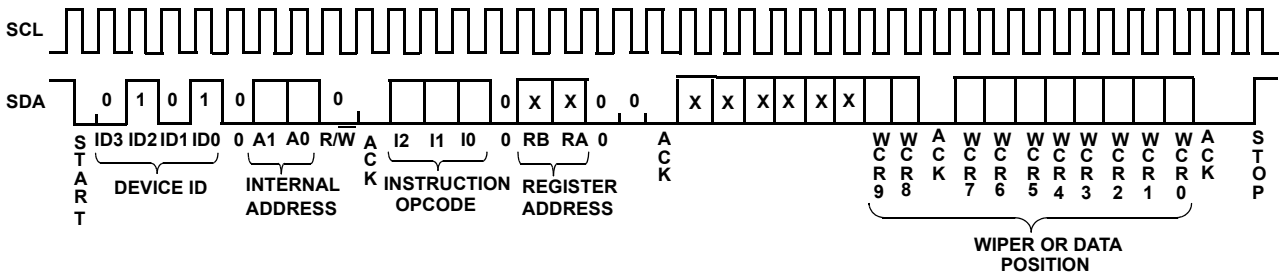


FIGURE 4. FOUR-BYTE INSTRUCTION SEQUENCE (WRITE OR READ FOR WCR OR DATA REGISTERS)

Instruction Format

Read Wiper Counter Register (WCR)

S	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				S	INSTRUCTION OPCODE				REGISTER ADDRESSES				S	WIPER POSITION (SENT BY SLAVE ON SDA)								M	WIPER POSITION (SENT BY SLAVE ON SDA)								M	S
T	0	1	0	1	0	A1	A0	R/$\overline{W}$ = 1	A	1	0	0	0	0	0	0	0	A	X	X	X	X	X	X	WCR9	WCR8	A	WCR7	WCR6	WCR5	WCR4	WCR3	WCR2	WCR1	WCR0	A	T
A									C									C									C									C	O
R									K									K									K									K	P
T																																					

Write Wiper Counter Register (WCR)

S	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				S	INSTRUCTION OPCODE				REGISTER ADDRESSES				S	WIPER POSITION (SENT BY MASTER ON SDA)								S	WIPER POSITION (SENT BY MASTER ON SDA)								S	S
T	0	1	0	1	0	A1	A0	R/$\overline{W}$ = 0	A	1	0	1	0	0	0	0	0	A	X	X	X	X	X	X	WCR9	WCR8	A	WCR7	WCR6	WCR5	WCR4	WCR3	WCR2	WCR1	WCR0	A	T
A									C									C									C									C	O
R									K									K									K									K	P
T																																					

Read Data Register (DR)

S	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				S	INSTRUCTION OPCODE				REGISTER ADDRESSES				S	WIPER POSITION (SENT BY SLAVE ON SDA)								M	WIPER POSITION OR DATA (SENT BY SLAVE ON SDA)								M	S
T	0	1	0	1	0	A1	A0	R/$\overline{W}$ = 1	A	1	0	1	0	RB	RA	0	0	A	X	X	X	X	X	X	WCR9	WCR8	A	WCR7	WCR6	WCR5	WCR4	WCR3	WCR2	WCR1	WCR0	A	T
A									C									C									C									C	O
R									K									K									K									K	P
T																																					

Write Data Register (DR)

START	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				SACK	INSTRUCTION OPCODE				REGISTER ADDRESSES				SACK	WIPER POSITION OR DATA (SENT BY MASTER ON SDA)								SACK	WIPER POSITION OR DATA (SENT BY MASTER ON SDA)								SACK	STOP	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	0	A 1	A 0	$R/\overline{W}$ = 0		1	1	0	0	RB	RA	0	0		X	X	X	X	X	X	WCR9	WCR8		WCR7	WCR6	WCR5	WCR4	WCR3	WCR2	WCR1	WCR0			

Transfer Wiper Counter Register (WCR) to Data Register (DR)

START	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				SACK	INSTRUCTION OPCODE				REGISTER ADDRESSES				SACK	STOP	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	0	A 1	A 0	$R/\overline{W}$ = 0		1	1	1	0	RB	RA	0	0			

Transfer Data Register (DR) to Wiper Counter Register (WCR)

START	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				SACK	INSTRUCTION OPCODE				REGISTER ADDRESSES				SACK	STOP
	0	1	0	1	0	A 1	A 0	$R/\overline{W}$ = 1		1	1	0	0	RB	RA	0	0		

NOTES:

1. “A1 ~ A0”: stands for the device addresses sent by the master.
2. WCRx refers to wiper position data in the Wiper Counter Register.

Absolute Maximum Ratings

Temperature Under Bias . . . . . -65°C to +135°C
Voltage on SCL, SDA, or Any Address Input with Respect to VSS. . . . . -1V to +7V
Voltage on V+ (referenced to V_{SS}) (Note 8) 10V
Voltage on V- (referenced to V_{SS}) (Note 8) . . . . . -10V
(V+) – (V-) 12V
Any Voltage on R_H/R_L . . . . . .V+
Any Voltage on R_L/R_H . . . . . V-
I_W (10s) . . . . . ±6mA
Supply Voltage (VCC) Limits (Note 8)
X9118 . . . . . 5V ±10%
X9118-2.7 . . . . . .2.7V to 5.5V

Thermal Information

Thermal Resistance (Typical, Note 3, 4)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
14 Ld TSSOP	92	25

Storage Temperature . . . . . .-65°C to +150°C
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Commercial . . . . . 0°C to +70°C
Industrial . . . . . .-40°C to +85°C
Power Rating (each pot) 50mW
Wiper current (max) . . . . . ±3mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
4. For θ_{JC}, the “case temp” location is taken at the package top center.

Analog Specifications

T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range , -40°C to +85°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 10)	TYP	MAX (Note 10)	UNITS
R_{TOTAL}	End to End Resistance			100		kΩ
	End to End Resistance Tolerance				**±20**	%
R_W	Wiper Resistance	$I_W = (V_{RH} - V_{RL})/R_{TOTAL}$, V_{CC} = 3V, V_{RL} = -3V		150	**500**	Ω
R_W	Wiper Resistance	$I_W = (V_{RH} - V_{RL})/R_{TOTAL}$, V_{CC} = 5V, V_{RL} = 0V		40	**100**	Ω
Vv+	Voltage on V+ Pin	X9118 (Note 8)	**+4.5**		**+5.5**	V
		X9118-2.7 (Note 8)	**+2.7**		**+5.5**	V
Vv-	Voltage on V- Pin	X9118	**-5.5**		**-4.5**	V
		X9118-2.7	**-5.5**		**-2.7**	V
V_{TERM}	Voltage on any R_H or R_L Pin	V_{SS} = 0V	**V-**		**V+**	V
	Noise	Ref: 1kHz		-120		dBV
	Resolution			0.1		%
	Absolute Linearity (Note 5)	$R_{w(n)(actual)} – R_{w(n)(expected)}$, where n = 1 to 1023			**±1.5**	MI (Note 7)
	Relative Linearity (Note 6)	$R_{w(m + 1)} – [R_{w(m)} + MI]$, where m = 1 to 1023			**±1.5**	MI (Note 7)
	Temperature Coefficient of R_{TOTAL}			±300		ppm/°C
	Ratiometric Temperature Coefficient	Wiper at middle point		±20		ppm/°C
$C_H/C_L/C_W$	Potentiometer Capacitances	See Macro model		10/10 /25		pF

NOTES:

5. Absolute linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.
6. Relative linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.
7. MI = $R_{TOT}/1023$ or $(R_H – R_L)/1023$, single pot.
8. V_{CC}, V+, V- must reach their final values within 1ms of each other.
9. n = 0, 1, 2, …,1023; m = 0, 1, 2, …, 1022.

DC Operating Specifications

T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range , -40°C to +85°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 10)	TYP	MAX (Note 10)	UNITS
I_{CC1}	V_{CC} Supply Current (Active)	f_{SCL} = 400kHz; V_{CC} = +5.5V; SDA = Open; (for 2-wire, Active, Read and Volatile Write States only)			**3**	mA
I_{CC2}	V_{CC} Supply Current (Nonvolatile Write)	f_{SCL} = 400kHz; V_{CC} = +5.5V; SDA = Open; (for 2-wire, Active, Non-volatile Write State only)			**7**	mA
I_{SB}	V_{CC} Current (Standby)	V_{CC} = +5.5V; V_{IN} = V_{SS} or V_{CC}; SDA = V_{CC}; (for 2-wire, Standby State only)			**15**	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{SS} to V_{CC}			**10**	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{SS} to V_{CC}			**10**	µA
V_{IH}	Input HIGH Voltage		**V_{CC} x 0.7**		**V_{CC} + 1**	V
V_{IL}	Input LOW Voltage		**-1**		**V_{CC} x 0.3**	V
V_{OL}	Output LOW Voltage	I_{OL} = 3mA			**0.4**	V

NOTE:

10. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Endurance and Data Retention

PARAMETER	MIN	UNITS
Minimum Endurance	100,000	Data changes per bit per register
Data Retention	100	years

Capacitance

SYMBOL	TEST	TYP	UNITS	TEST CONDITIONS
$C_{IN/OUT}$ (Note 11)	Input/Output Capacitance (SI)	8	pF	V_{OUT} = 0V
C_{IN} (Note 11)	Input Capacitance (SCL, $\overline{WP}$, A1 and A0)	6	pF	V_{IN} = 0V

Power-Up Timing

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_r V_{CC} (Note 11)	V_{CC} Power-up Rate	0.2	50	V/ms
t_{PUR} (Note 12)	Power-up to Initiation of Read Operation		1	ms
t_{PUW} (Note 12)	Power-up to Initiation of Write Operation		50	ms

NOTES:

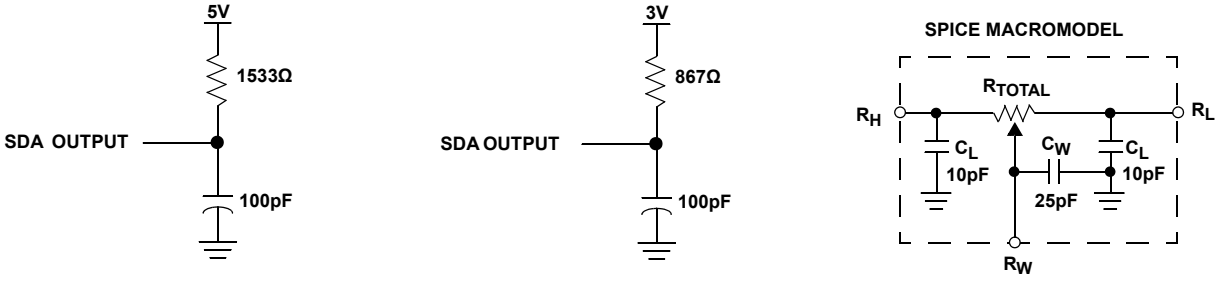
11. This parameter is not 100% tested.

12. t_{PUR} and t_{PUW} are the delays required from the time the (last) power supply (V_{CC}-) is stable until the specific instruction can be issued. These parameters are periodically sampled and not 100% tested.

AC Test Conditions

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Level	V_{CC} x 0.5

Equivalent A.C. Load Circuit



AC Timing High-Voltage Write Cycle Timing

SYMBOL	PARAMETER	MIN	MAX	UNITS
f_{SCL}	Clock Frequency		400	kHz
t_{CYC}	Clock Cycle Time	2500		ns
t_{HIGH}	Clock High-Time	600		ns
t_{LOW}	Clock Low-Time	1300		ns
$t_{SU:STA}$	Start Setup Time	600		ns
$t_{HD:STA}$	Start Hold Time	600		ns
$t_{SU:STO}$	Stop Setup Time	600		ns
$t_{SU:DAT}$	SDA Data Input Setup Time	100		ns
$t_{HD:DAT}$	SDA Data Input Hold Time	30		ns
t_R	SCL and SDA Rise Time		300	ns
t_F	SCL and SDA Fall Time		300	ns
t_{AA}	SCL Low to SDA Data Output Valid Time	250		ns
t_{DH}	SDA Data Output Hold Time	0		ns
t_I	Noise Suppression Time Constant at SCL and SDA inputs	50		ns
t_{BUF}	Bus Free Time (Prior to Any Transmission)	1300		ns
$t_{SU:WPA}$	A0, A1 Setup Time	0		ns
$t_{HD:WPA}$	A0, A1 Hold Time	0		ns

High-Voltage Write Cycle Timing

SYMBOL	PARAMETER	TYP	MAX	UNITS
t_{WR}	High-Voltage Write Cycle Time (store instructions)	5	10	ms

XDCP Timing

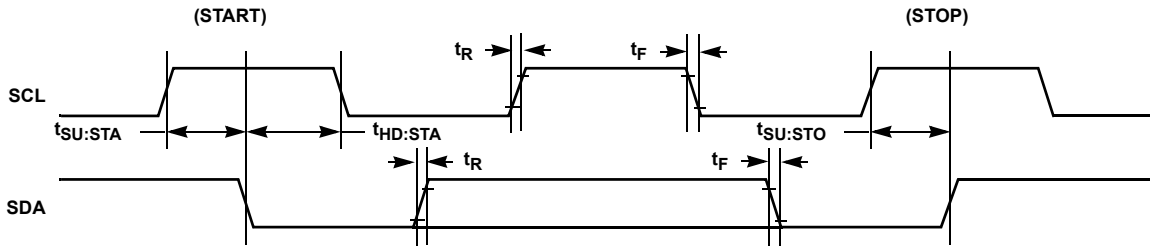
SYMBOL	PARAMETER	TYP	UNITS
t_{WRPO}	Wiper Response Time After the Third (last) Power Supply is Stable	8	µs
t_{WRL}	Wiper Response Time After Instruction Issued (all load instructions)	8	µs

Symbol Table

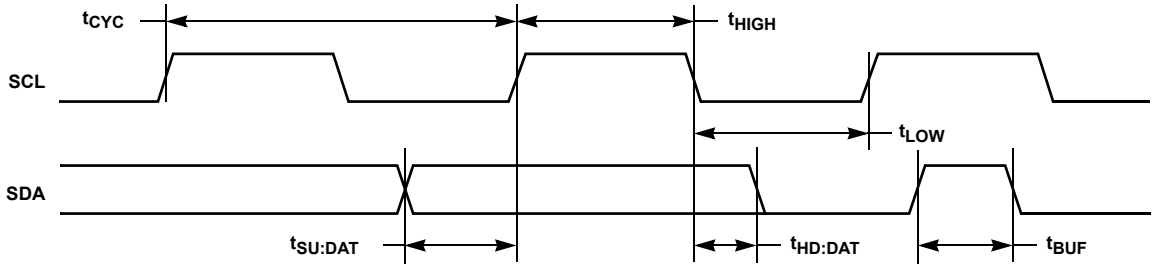
WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Timing Diagrams

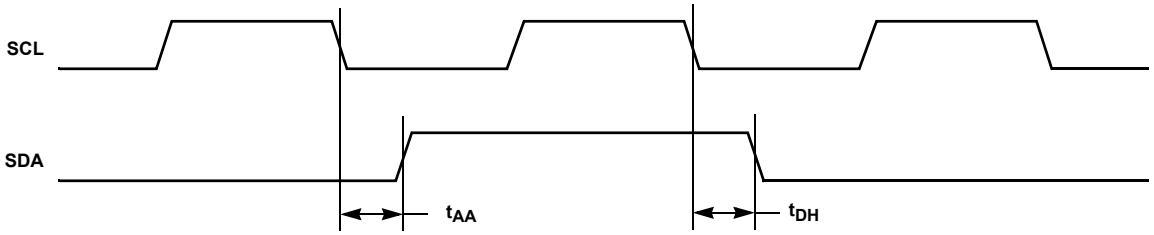
Start and Stop Timing



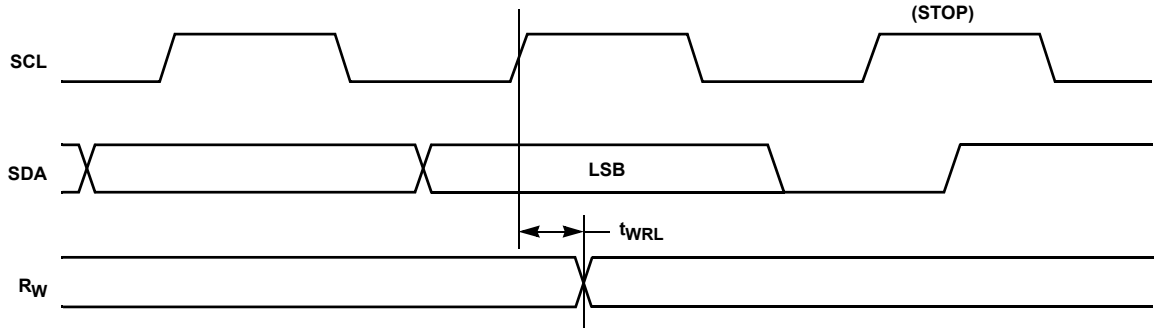
Input Timing



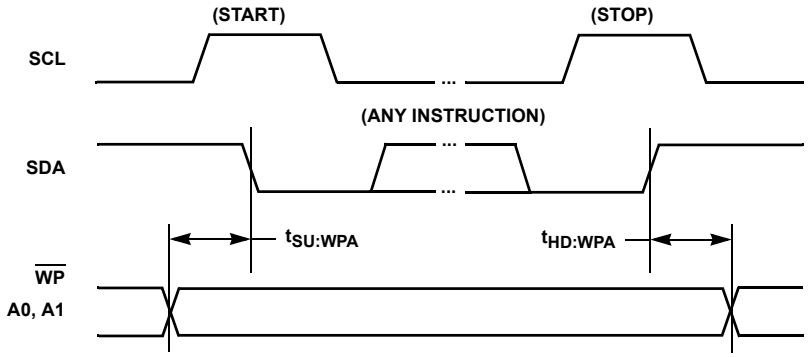
Output Timing



XDCP Timing (For All Load Instructions)

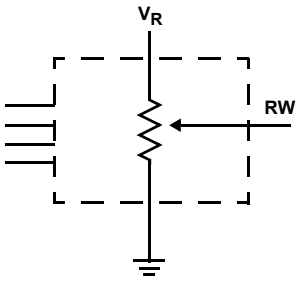


Write Protect and Device Address Pins Timing

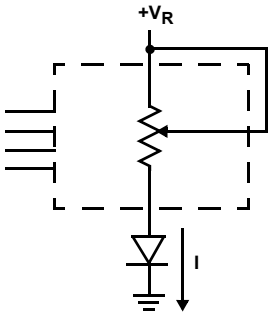


Applications Information

Basic Configurations of Electronic Potentiometers



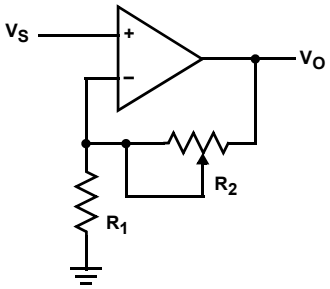
Three terminal Potentiometer;
Variable voltage divider



Two terminal Variable Resistor;
Variable current

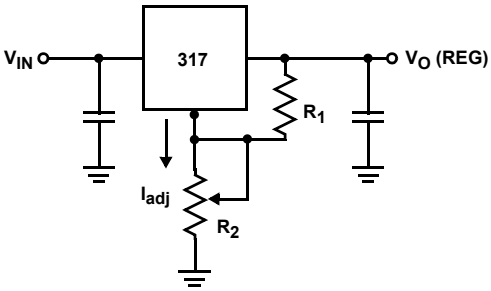
Application Circuits

NONINVERTING AMPLIFIER



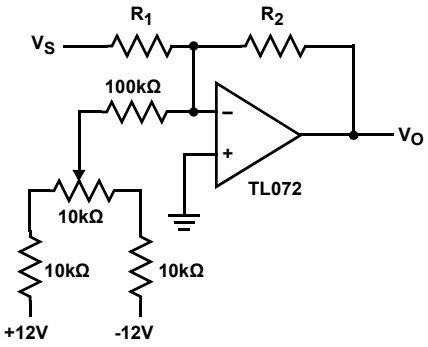
$V_O = (1+R_2/R_1)V_S$

VOLTAGE REGULATOR

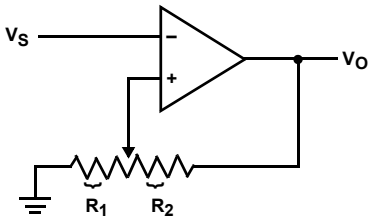


$V_O\ (REG) = 1.25V\ (1+R_2/R_1)+I_{adj}\ R_2$

OFFSET VOLTAGE ADJUSTMENT



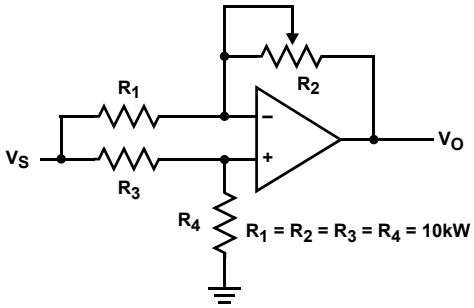
COMPARATOR WITH HYSTERISIS



$V_{UL} = \{R_1/(R_1+R_2)\}\ V_O(max)$
$RL_L = \{R_1/(R_1+R_2)\}\ V_O(min)$

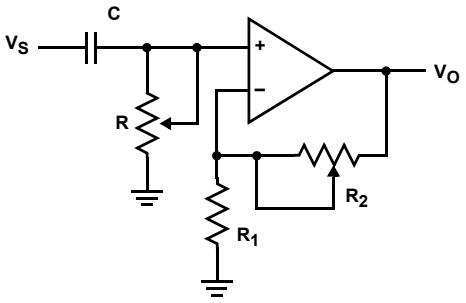
Application Circuits (Continued)

ATTENUATOR



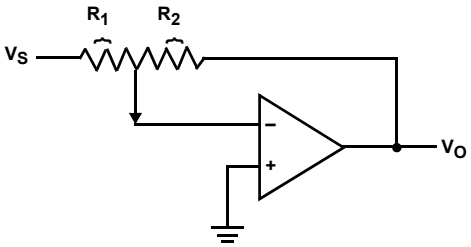
$V_O = G\ V_S$
$-1/2 \leq G \leq +1/2$

FILTER



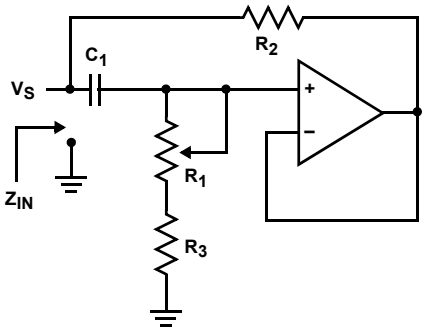
$G_O = 1 + R_2/R_1$
$fc = 1/(2\pi RC)$

INVERTING AMPLIFIER



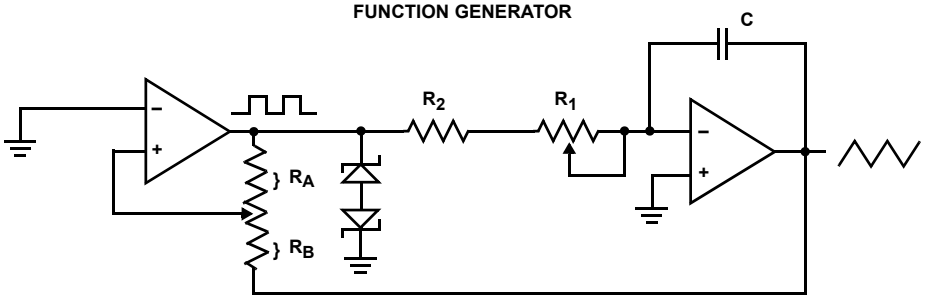
$V_O = G\ V_S$
$G = -R_2/R_1$

EQUIVALENT L-R CIRCUIT



$Z_{IN} = R_2 + s\ R_2\ (R_1 + R_3)\ C_1 = R_2 + s\ Leq$
$(R_1 + R_3) >> R_2$

FUNCTION GENERATOR

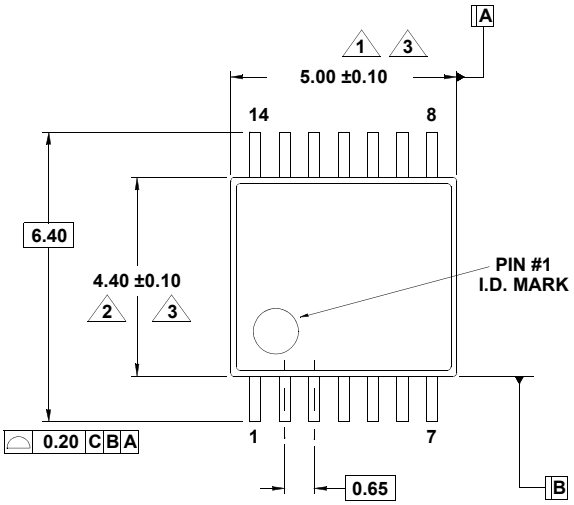


frequency $\propto R_1, R_2, C$
amplitude $\propto R_A, R_B$

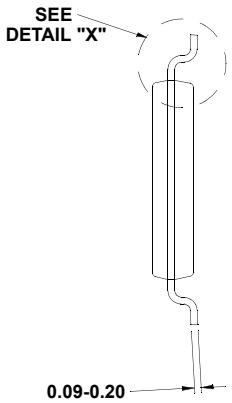
Package Outline Drawing

M14.173

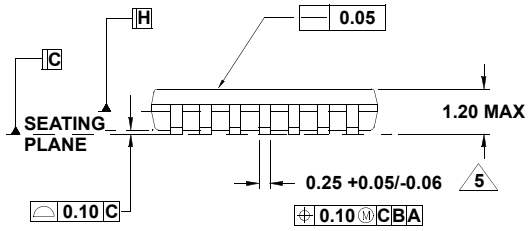
14 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)
Rev 3, 10/09



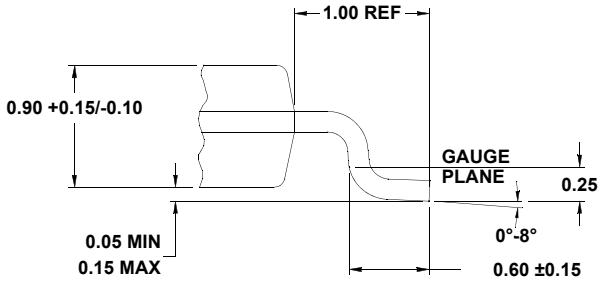
TOP VIEW



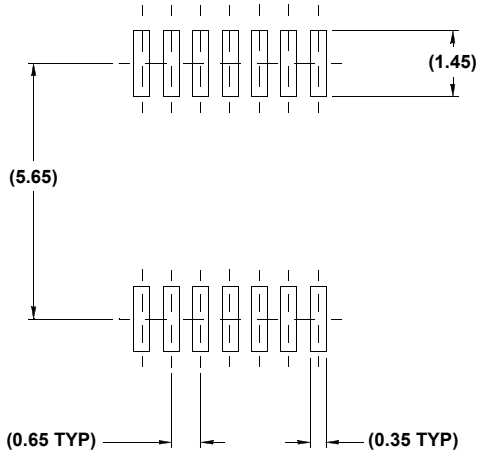
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.80mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153, variation AB-1.

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