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RENESAS

Data Sheet

32

SH7723

Renesas 32-Bit RISC Microcomputer
SH7780 Series
R8A7723

-Preliminary -

Renesas Electronics
www.renesas.com

Rev.1.00 2008.10

General Precautions on Handling of Product

1. Treatment of NC Pins

Note: Do not connect anything to the NC pins.
The NC (not connected) pins are either not connected to any of the internal circuitry or are used as test pins or to reduce noise. If something is connected to the NC pins, the operation of the LSI is not guaranteed.

2. Treatment of Unused Input Pins

Note: Fix all unused input pins to high or low level.
Generally, the input pins of CMOS products are high-impedance input pins. If unused pins are in their open states, intermediate levels are induced by noise in the vicinity, a pass-through current flows internally, and a malfunction may occur.

3. Processing before Initialization

Note: When power is first supplied, the product's state is undefined.
The states of internal circuits are undefined until full power is supplied throughout the chip and a low level is input on the reset pin. During the period where the states are undefined, the register settings and the output state of each pin are also undefined. Design your system so that it does not malfunction because of processing while it is in this undefined state. For those products which have a reset function, reset the LSI immediately after the power supply has been turned on.

4. Prohibition of Access to Undefined or Reserved Addresses

Note: Access to undefined or reserved addresses is prohibited.
The undefined or reserved addresses may be used to expand functions, or test registers may have been be allocated to these addresses. Do not access these registers; the system's operation is not guaranteed if they are accessed.

5. Reading from/Writing Reserved Bit of Each Register

Note: Treat the reserved bit of register used in each module as follows except in cases where the specifications for values which are read from or written to the bit are provided in the description.
The bit is always read as 0. The write value should be 0 or one, which has been read immediately before writing.
Writing the value, which has been read immediately before writing has the advantage of preventing the bit from being affected on its extended function when the function is assigned.

Configuration of This Manual

This manual comprises the following items:

1. General Precautions on Handling of Product
2. Configuration of This Manual
3. Preface
4. Contents
5. Overview
6. Description of Functional Modules
   - CPU and System-Control Modules
   - On-Chip Peripheral Modules

   The configuration of the functional description of each module differs according to the module. However, the generic style includes the following items:

   i) Feature
   ii) Input/Output Pin
   iii) Register Description
   iv) Operation
   v) Usage Note

When designing an application system that includes this LSI, take notes into account. Each section includes notes in relation to the descriptions given, and usage notes are given, as required, as the final part of each section.

7. List of Registers
8. Electrical Characteristics
9. Appendix
10. Main Revisions and Additions in this Edition (only for revised versions)

The list of revisions is a summary of points that have been revised or added to earlier versions. This does not include all of the revised contents. For details, see the actual locations in this manual.

11. Index

Preface

This LSI is a RISC (Reduced Instruction Set Computer) microcomputer which includes a Renesas Technology-original RISC CPU as its core, and the peripheral functions required to configure a system. This LSI includes the SH4A extended functions that have functional upward compatibility with the SH4A.

Target Users: This manual was written for users who will be using this LSI in the design of application systems. Users of this manual are expected to understand the fundamentals of electrical circuits, logical circuits, and microcomputers.

Objective: This manual was written to explain the hardware functions and electrical characteristics of this LSI to the above users.

Notes on reading this manual:

- In order to understand the overall functions of the chip

  Read the manual according to the contents. This manual can be roughly categorized into parts on the CPU, system control functions, peripheral functions and electrical characteristics.
- In order to understand the details of the instructions of the SH4A extended functions

  Read the SH4A Extended Function Software Manual.

Examples:	Register name:	The following notation is used for cases when the same or a similar function, e.g. serial communication, is implemented on more than one channel: XXX_N (XXX is the register name and N is the channel number)
	Bit order:	The MSB is on the left and the LSB is on the right.
	Number notation:	Binary is B'xxxx, hexadecimal is H'xxxx, decimal is xxxx.
	Signal notation:	An overbar is added to a low-active signal: $\overline{\text{xxxx}}$

Note: This data sheet contains references to the SH7723 Hardware Manual. The contents of the SH7723 Hardware Manual will be disclosed upon acceptance of a confidentiality agreement. For details, please contact a Renesas Technology sales representative.

Abbreviations

ALU	Arithmetic Logic Unit
ASID	Address Space Identifier
BEU	Blend Engine Unit
BSC	Bus State Controller
CEU	Capture Engine Unit
CMT	Compare Match Timer
CPG	Clock Pulse Generator
CPU	Central Processing Unit
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
DSP	Digital Signal Processor
ETU	Elementary Time Unit
FIFO	First-In First-Out
FLCTL	Flash Memory Controller
H-UDI	User Debugging Interface
IIC	Inter IC Bus
INTC	Interrupt Controller
IrDA	Infrared Data Association
JPU	JPEG Processing Unit
JPEG	Joint Photographic Experts Group
JTAG	Joint Test Action Group
KEYSC	Key Scan Interface

LCDC	LCD Controller
LRU	Least Recently Used
LSB	Least Significant Bit
MMC	Multi Media Card
MMU	Memory Management Unit
MPEG	Motion Picture Experts Group
MSB	Most Significant Bit
PC	Program Counter
PFC	Pin Function Controller
RISC	Reduced Instruction Set Computer
RWDT	RCLK Watchdog Timer
SBSC	SDRAM Bus State Controller
SCIF	Serial Communication Interface with FIFO
SDHI	SD Card Host Interface
SIM	Smart Card Interface Module
SIO	Serial Interface
SIOF	Serial Interface with FIFO
SIU	Sound Interface Unit
TAP	Test Access Port
TLB	Translation Lookaside Buffer
TMU	Timer Unit
TPU	Timer Pulse Unit
TSIF	Transport Stream Interface

UART	Universal Asynchronous Receiver/Transmitter
UBC	User Break Controller
USB	Universal Serial Bus
VEU	Video Engine Unit
VIO	Video I/O
VOU	Video Output Unit
VPU	Video Processing Unit

Contents

Section 1 Overview

Note: This section contains references to the SH7723 Hardware Manual. The contents of the SH7723 Hardware Manual will be disclosed upon acceptance of a confidentiality agreement. For details, please contact a Renesas Technology sales representative.

1.1 Features of This LSI

The SH7723 is a system LSI that incorporates a 32-bit RISC-type SuperH architecture CPU with a clock speed of up to 400 MHz and a FPU extension as its core and L2 Cache, together with a variety of functions required for multimedia applications. These include MPEG4 and H.264 accelerators, a 2D graphics accelerator, LCD controller, camera interface, and sound input/output module. With an on-chip DDR1 SDRAM interface and USB 2.0 high-speed Host and function, large amounts of data are transferable at high speeds. In addition, the strong power management functions keep both operating current and standby current low.

This LSI is ideal for use in multimedia devices that require both high-performance operation and low power consumption.

The features of this LSI are listed in table 1.1.

Table 1.1 Features of This LSI

Item	Features
CPU	• Renesas Technology original architecture • 32-bit internal data bus • General-register files — Sixteen 32-bit general registers (eight 32-bit shadow registers) — Seven 32-bit control registers — Four 32-bit system registers • RISC-type instruction set (upward compatible with SH-1, SH-2, SH-3, and SH-4 processors) — Instruction length: 16-bit fixed length for improved code efficiency — Load/store architecture — Delayed branch instructions — Conditional instruction execution — Instruction-set design based on the C language • Super-scalar architecture covering both the FPU and CPU provides for the simultaneous execution of any two instructions • Instruction-execution time: Two instructions per cycle (max.) • Virtual address space: 4 Gbytes • ASIDs (address-space identifiers): 8 bits, for 256 virtual address spaces • Internal multiplier • Eight-stage pipeline

Item	Features
FPU	• On-chip floating-point co-processor • Supports single (32-bit) and double (64-bit) precisions • Supports IEEE754-compliant data types and exceptions • Two rounding modes: Round to Nearest and Round to Zero • Handling of de-normalized numbers: Truncation to zero or interrupt generation for IEEE754 compliance • Floating-point registers: 32 bits × 16 registers × 2 banks (single-precision × 16 registers or double-precision × 8 registers) × 2 banks • 32-bit CPU-FPU floating-point communications register (FPUL) • FMAC (multiply-and-accumulate) instruction • FDIV (divide) and FSQRT (square root) instructions • FLDI0/FLDI1 (load constants 0 and 1) instructions • Instruction-execution times Latency (FADD/FSUB): 3 cycles (single-precision), 5 cycles (double-precision) Latency (FMAC/ FMUL): 5 cycles (single-precision), 7 cycles (double-precision) Pitch (FADD/FSUB): 1 cycle (single-precision/double-precision) Pitch (FMAC/FMUL): 1 cycle (single-precision), 3 cycles (double-precision) Note: FMAC only supports single-precision operands. • 3-D graphics instructions (single-precision only) — 4-dimensional vector-conversion and matrix operations (FTRV): 4cycles (pitch), 8 cycles (latency) — 4-dimensional vector (FIPR) inner product: 1 cycle (pitch), 5 cycles (latency)

Item	Features
Memory management unit (MMU)	• 4-Gbyte address space, 256 address spaces (8-bit ASID) • Single virtual memory mode and multiple virtual memory mode • Supports multiple page sizes: 1 Kbyte, 4 Kbytes, 64 Kbytes, or 1 Mbyte • 4-entry full associative TLB for instructions • 64-entry full associative TLB for instructions and operands • Specifies replacement way by software and supports random replacement algorithm • Address mapping allows direct access to TLB contents Note: This LSI does not support the 32-bit address extended mode or the 32-bit boot function.
Cache memory (L1C)	• Instruction cache (IC) — 32-Kbyte, 4-way set associative — 32-byte block length • Operand cache (OC) — 32-Kbyte, 4-way set associative — 32-byte block length — Selectable write mode (copy-back or write-through)
Secondary cache (L2C)	• 256-Kbyte L2 cache, mixed instruction/data • 32-byte block length • Write-through
IL memory (ILRAM)	• Three independent read/write ports — Instruction fetch access from CPU using virtual address — Instruction fetch access from CPU using physical address and 8-/16-/32-bit operand access from CPU — 8-/16-/32-/64-bit or 16-/32-byte access by Super-Hyway bus master • Total of 16 Kbytes
Interrupt controller (INTC)	• Nine external interrupt pins (NMI, IRQ7 to IRQ0) — NMI: Fall/rise selectable — IRQ: Fall/rise/high level/low level selectable • On-chip peripheral interrupts: Priority can be specified for each module

Item	Features
Bus state controller (BSC)	• Supports SRAM, burst ROM, and PCMCIA interfaces. • Physical address space is provided to support six areas in total: two areas (areas 0 and 4) of up to 64 Mbytes each and four areas (area 5A,5B,6A,6B) of up to 32 Mbytes. A chip select signal is output to the target area. • Data bus width: Selectable from 16 bits and 32 bits
Bus state controller for DDR SDRAM (SBSC)	• 2.5V DDR1-SDRAM can be directly connected • Physical address space is provided to support one area (DRAM area) of up to 128 Mbytes • Data bus width: 32 bits • Supports auto-refresh, self-refresh functions • Auto-precharge mode, bank active mode can be selected
Direct memory access controller (DMAC)	• Number of channels: 12 channels. Two of these channels (channel 0 and channel 1 of DMAC0) can receive an external request. • Address space: 4 Gbytes on architecture • Data transfer length: Bytes, words (2 bytes), longwords (4 bytes), 16 bytes, and 32 bytes • Maximum number of transfer times: 16,777,216 times • Address mode: Dual address mode • Transfer request: Selectable from external request, on-chip peripheral module request and auto request • Bus mode: Selectable from cycle steal mode (normal mode and intermittent mode) and burst mode • Priority: Selectable from fixed channel priority mode and round-robin mode • Interrupt request: Supports interrupt request to CPU at the end of data transfer • Repeat function: Automatically resets the transfer source, destination, and count at the end of DMA transfer • Reload function: Automatically resets the transfer source and destination at the end of the specified number of DMA transfers

Item	Features
Clock pulse generator (CPG)	• Clock mode: Input clock selectable from external inputs (EXTAL or RCLK) or crystal oscillator. • Output clock: Bus clock (Bϕ) • Generates six types of system clocks — CPU clock (Iϕ): Maximum 400 MHz — SH clock (SHϕ): Maximum 133.4 MHz — SBSC clock (B3ϕ): Maximum 133.4 MHz (for DDR max frequency) — DDR-SDRAM clock (DDRϕ): Maximum 133.4 MHz (data rate 266.7 MHz) — Bus clock (Bϕ): Maximum 66.7 MHz — Peripheral clock (Pϕ): Maximum 33.4 MHz • Module standby function (stops clocks for individual modules.) • Sleep mode (stops clocks for the CPU core.) • Software standby mode (stops clocks in the LSI except the I/O area and the RCLK operation area) • U-standby mode (turns off the power in the LSI except the I/O area and the RCLK operation area
RCLK watchdog timer (RWDT)	• Single watchdog timer with RCLK as the operating clock (RCLK must be input to operate this LSI.) • Generates a system reset when the counter overflows
Timer unit (TMU)	• Six internal 32-bit TMU timers • Auto-reload type 32-bit down counter • Internal prescaler for Pϕ • Interrupt request
Timer pulse unit (TPU)	• 4 channel of 16-bit timers • Four pulse outputs possible • Maximum of 4-phase PWM output possible • Interrupt request
Compare match timer (CMT)	• One 32-bit CMT timer (16 bits/32 bits can be selected) • Source clock: RCLK • Compare match function provided • Interrupt request

Item	Features
Clock-synchronized serial interface with FIFO (MSIOF)	• 2 channels • Internal 64-byte transmit/receive FIFOs • Supports 8-/16-bit data and 16-bit stereo audio input/output and 24-bit stereo audio input/output • Sampling rate clock input selectable from Bϕ and external pin • Internal prescaler for Bϕ • Module stop function • Interrupt request and DMAC request • SPI mode — Provides continuous full-duplex communication with SPI slave device in fixed master mode. — Serial clock (SCK) rise or fall edge selectable for data sampling timing — SCK clock phase selectable for transmit timing — Three slave devices selectable — Transmit/receive data length to 8 bits and 16bits and 32 bits
Serial communication interface with FIFO (SCIF)	• 3 channels • Internal 16-byte transmit/receive FIFOs • High-speed UART for Bluetooth • Internal prescaler for Pϕ • Both asynchronous and clock synchronous serial communications possible • Interrupt request and DMAC request
Serial communication interface with FIFO (SCIFA)	• 3 channels • Internal 64-byte transmit/receive FIFOs • High-speed UART for Bluetooth • Internal prescaler for Bϕ • Both asynchronous and clock synchronous serial communications possible • On-chip modem-control function (RTS and CTS) for channel 3 • Interrupt request and DMAC request
Realtime clock (RTC)	• Operates at RCLK and includes clock and calendar • Generates alarm interrupt and periodic interrupt
IrDA interface (IrDA)	• Conforms to version 1.2a • CRC generation function • Interrupt request and DMA transfer request

Item	Features
Key scan interface (KEYSC)	• Key scan: Chattering elimination in key input interrupt detection is possible • Input or output bit numbers can be set to be programmable (5 inputs/6 outputs, 6 inputs/5 outputs, 7 inputs/4 outputs.) • Generates the key input interrupt in Software standby or U-standby mode • Interrupt request
USB Host & Function Module (USB)	• USB 2.0 High Speed Host & High Speed Function • Possible to switch from USB host to USB function with the registers • Supports USB 2.0 high-speed mode (480 Mbps), full-speed mode (12Mbps) and low-speed mode (1.5Mbps) • Internal USB transceivers • Adopt to all the USB transfer type Provides Control-transfer, Bulk-transfer, Interrupt-transfer (not adaptive to high bandwidth) and Isochronous-transfer (not adaptive to high bandwidth). • Maximum of ten endpoints including the default endpoint are supported in total. • Able to allocate any numbers to endpoint 1 to 9 • Each endpoint transfer setting Endpoint 0: Control-transfer Endpoint 1 and 2: Bulk-transfer or Isochronous-transfer Endpoint 3 to 5: Bulk-transfer Endpoint 6 to 9: Interrupt-transfer • Module input clock: 48 MHz • Interrupt request and DMA transfer request
I^2C bus interface (IIC)	• 1 channel • Supports single master transmission/reception • Supports standard mode (100 kHz) and high-speed mode (400 kHz) • Interrupt request
NAND flash memory controller (FLCTL)	• Directly connected memory interface with NAND-type flash memory • Read/write in sectors • Two types of transfer modes: Command access mode and sector access mode (512-byte data + 16-byte management code: with 4-bit ECC) • Interrupt request and DMAC transfer request

Item	Features
Video processing unit (VPU5F)	• MPEG-4 single video object plane (VOP) encoding and decoding • Applicable standard: MPEG-4 Simple Profile, MPEG-4 H.264 (Baseline)*[1], VC1(WMV) Simple profile, and Main Profiles *[2] • Image size: Sub-QCIF to VGA • Bit rate: Maximum 8 Mbps • Motion detection: Layer tracking (Renesas Technology original method) • Rate control: Control with quantizing amount predicted (Renesas Technology original method), both VOP and MB supported • Interrupt request Note: 1. Some of Baseline tools are not supported. 2. Some of Baseline tools (Dynamic Resolution Change, B-Frame, and Range Reduction) are not supported.
Video I/O module (VIO5)	Provides the interface with camera module and image processing • CEU (Capture engine unit; image capturing from camera module) A. Camera module interface: Data (8 bits: YCbCr 4:2:2), horizontal sync signal (HD), vertical sync signal (VD) B. Size of captured image: 5M pixels, 3M pixels, 2M pixels, UXGA, SXGA, XGA, SVGA, VGA, CIF, QVGA, QCIF, QQVGA, Sub-QCIF, etc. C. Output image format: YCbCr (4:2:2/4:2:0) D. Image format conversion function: Reduced image generating prefilter function YCbCr 4:2:2 → YCbCr 4:2:2, YCbCr 4:2:0 YCbCr format (Y: 8 bits and CbCr: 16 bits)

Item	Features
Video I/O module (VIO5)	• VEU2H (Video engine unit; image processing in memory) A. Video image processing function Input image format: YCbCr image (Y/CbCr plane image), RGB image (RGB pack image) Output image format: YCbCr image (Y/CbCr plane image), RGB image (RGB pack image) Image processing function: Scaling image generating filter function YCbCr$\rightarrow$RGB/RGB$\rightarrow$YCbCr conversion function Dithering function (in RGB color subtraction) B. Filter processing function Mirroring, vertical inversion, point symmetry, $\pm$90-degree image conversion functions Deblocking filter Median filter High Qualitization FIR filter(Edge Enhancement) C. Video image processing and filter processing combined operation • BEU (Blend engine unit; image blending) A. PinP function Input image format: YCbCr image (Y/CbCr plane image), RGB image (RGB pack image) Output image format: YCbCr image (Y/CbCr plane image), RGB image (RGB pack image) B. Graphic processing function Input graphic format: YCbCr/RGB image Output graphic format: YCbCr/RGB image C. PinP and graphic combined operation Two PinP planes and one graphic plane can be blended simultaneously D. Results of processing are written back to memory • Frame drop function (1/2, 1/3, 1/4, 1/5, or 1/6 drop) • Interrupt request

Item	Features
2D graphics accelerator (2DG)	• Drawing function 4-vertex surface drawing, polygon drawing, line drawing, high functional bold line drawing, antialiasing, raster operation/BitBLT with alpha blending • Color representation Source: 1/8/16 bit/pixel, Drawing: 8/16 bit/pixel Work: Binary • Screen coordinates X-direction: 0 to 4095 Y-direction: 0 to 4095 • Interrupt request
LCD controller (LCDC)	• Supported LCD panel: TFT color LCD • Input data format: 8, 12, 16, 18, or 24 bpp • LCD driver interface — Specialized LCD bus, independent of memory bus — RGB interface or 80-series CPU bus interface selectable — Bus width: 8, 9, 12, 16, 18, or 24 bits — One-pixel one-time, two-time, or three-time transfer mode selectable — Signal polarity and SYNC output timing and width programmable in RGB interface — Access cycle programmable in 80-series CPU bus interface • Dot clock: Bus clock, peripheral clock, or external clock selectable as the source clock • Display data fetch: Continuous mode (according to the refresh rate of the LCD panel) and one-shot mode (according to the frame rate of the movie) are supported. Image data can be fetched only for updated sections. • 256-entry, 24-bit-output built-in color palette • An interrupt can be generated at the frame and the user-specified line • Interrupt request

Item	Features
Video output unit (VOU)	• Output data format: 16-bit interface with 8-bit Y and 8-bit C • Output pixel frequency: 13.5 MHz and 27 MHz • Partial image display: Any background color (selectable by a register) plus images to be displayed • Supported source image: Sub-QCIF, QVGA, VGA, etc. • Interrupt request
TS interface (TSIF)	• Serial TS data input • Filters 38 kinds of PIDs in total (The PID values of PAT and CAT packets are fixed. For PCR, video, and audio packets, the PID values are predefined.) • Interrupt request and DMA transfer request
Sound interface unit (SIUA, SIUB)	• Internal two channels • 16-bit stereo • Supports PCM and I2S formats • IEC60958 (SPDIF) supports stereo consumer mode • Two sound output systems and two sound input systems • DSP functions (FIR filter, IIR filter, equalizer, etc.) • Serial I/O can be directly connected to external A/D or D/A converter. • Internal prescaler • Supports master/slave mode • Interrupt request and DMA transfer request
ATAPI interface (ATAPI)	• Supports primary channel • Supports master/slave • Supports PIO modes 0 to 4, multiword DMA modes 0 to 2, and Ultra DMA modes 0 to 4 • Supports descriptor mode • I/O: Supports 3.3 V • Interrupt request

Item	Features
SD card host interface (SDHI)	• Internal two channels • SD memory/SDIO interface supported • Card detecting function • Interrupt request and DMA transfer request • Maximum operation frequency: 50MHz (support high peed)
A/D converter (ADC)	• 10 bits ± 4 LSB, 4 channels • Conversion time: 15μS • Input range: 0–AVcc (max. 3.6 V) • Interrupt request and DMA transfer request
I/O port	• I/O port is switchable for each bit
User break controller (UBC)	• Debugging with user break interrupts supported • Two break channels • All of address, data value, access type, and data size can be set as break conditions • Supports sequential break function
User debugging interface (H-UDI)	• Supports E10A emulator • Real-time branch trace • 4-Kbyte on-chip memory for executing high-speed emulation program
Package	• BGA package with 449 pins: 21 mm × 21 mm, 0.8 mm-pitch
Power-supply voltage	• I/O: 3.0 to 3.6 V (V_{CC}Q, USB power-supply pins) • DDR1-SDRAM I/O: 2.3 to 2.7 V (VccQ_DDR power-supply pins) • ADC: 3.0 to 3.6 V (AVcc power-supply pins) • Internal: 1.15 to 1.30 V (VDD and USB power-supply pins)
Process	• 0.09-μm CMOS, 7 metal layers
Product lineup	• R8A77230C400BG: The operating temperature of a guarantee –20 to 70°C • R8A77230D400BG: The operating temperature of a guarantee –40 to 85°C

1.2 Block Diagram

Figure 1.1 shows a block diagram of this LSI.

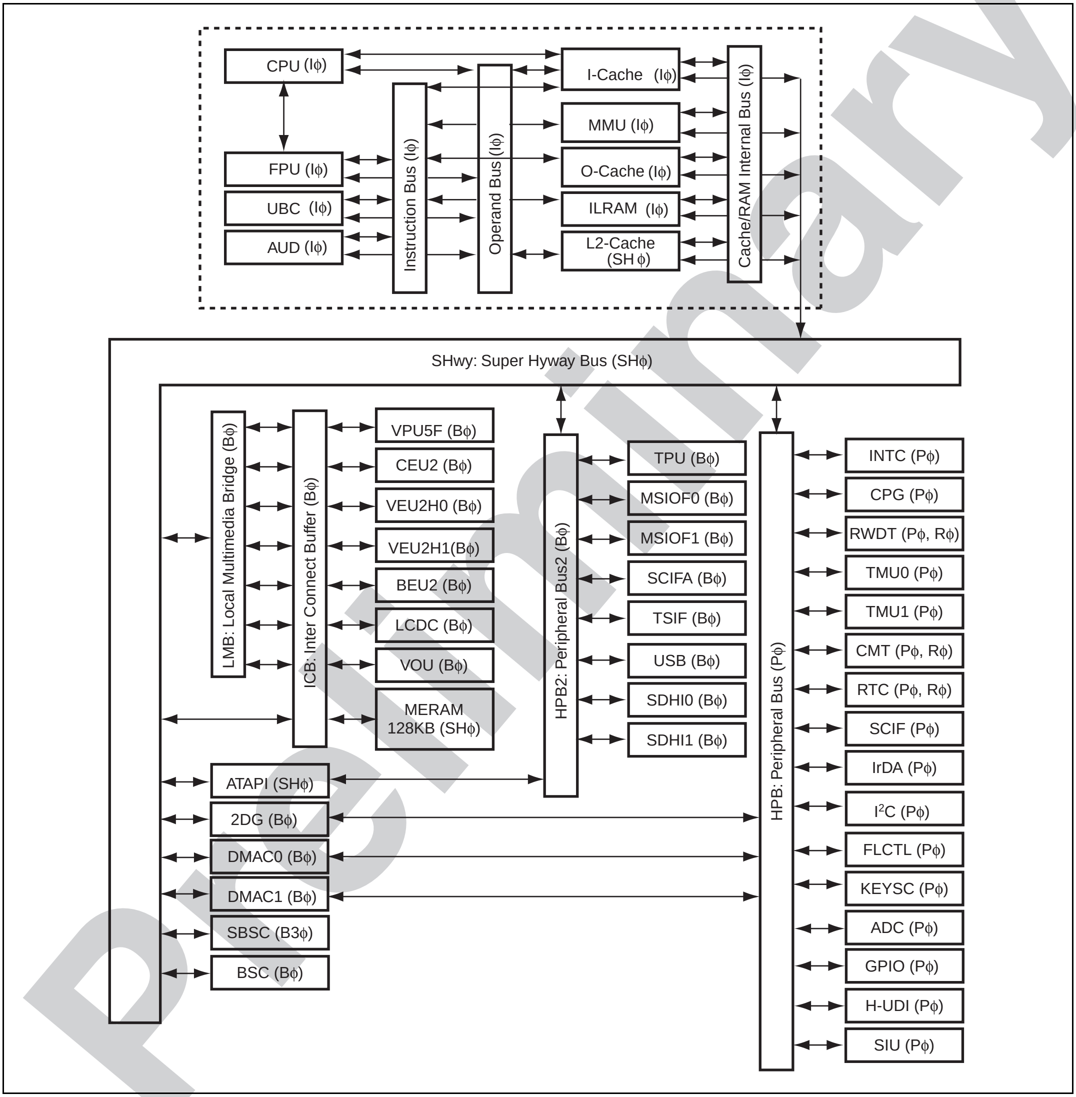


Figure 1.1 Block Diagram

1.3 Pin Assignments

Figure 1.2 shows the pin assignments.

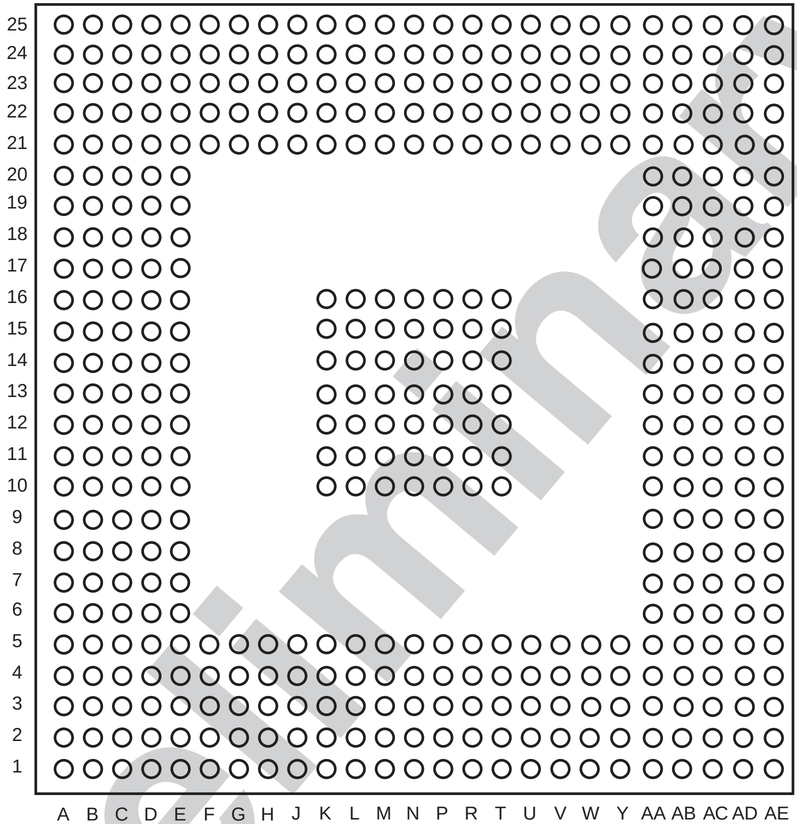


Figure 1.2 Pin Assignments (Top View)

Table 1.2 Pin Assignments

Pin No.	Pin Name
A1	V_{SS}
A2	UV12
A3	AV12
A4	DV12
A5	DP
A6	DM
A7	PTQ2/AN2
A8	PTY0/VIO_D0
A9	PTY5/VIO_D5
A10	PTZ0/VIO_CLK1/SIUBISLD
A11	PTZ3/VIO_FLD/SIUBFCK
A12	XTAL
A13	EXTAL
A14	PTG2/AUDATA2/TPUTO2
A15	$\overline{\text{TRST}}$
A16	TDI
A17	$\overline{\text{TST}}$
A18	RCLK
A19	PTJ7/STATUS0
A20	PTW5/IRQ5
A21	PTH0/LCDVEPWC
A22	PTH5/LCDVSYN/DV_CLK
A23	PTN7/LCDD23/SCIF5_SCK
A24	V_{SS}_DLL
A25	V_{SS}
B1	EXTALUSB
B2	PTW2/IRQ2/$\overline{\text{BS}}$/VIO_CKO
B3	AV33
B4	DG12
B5	DG33
B6	DV33

Pin No.	Pin Name
B7	PTQ0/AN0
B8	PTX6/DREQ1/MSIOF0_MCK
B9	PTY3/VIO_D3
B10	PTY7/VIO_D7
B11	PTZ1/VIO_VD1/SIUBIBT
B12	NMI
B13	MPMD
B14	PTG3/AUDATA3/TPUTO3
B15	TDO
B16	TCK
B17	$\overline{\text{RESETP}}$
B18	$\overline{\text{RESETA}}$
B19	$\overline{\text{TSTMD}}$
B20	PTW4/IRQ4/LCDLCLK
B21	PTH1/LCDDCK/$\overline{\text{LCDWR}}$
B22	PTH6/$\overline{\text{LCDRD}}$/DV_CLKI
B23	PTN6/LCDD22/SCIF5_RXD
B24	V_{DD}_DLL
B25	PTN5/LCDD21/SCIF5_TXD
C1	XTALUSB
C2	PTX2/TS0_SCK
C3	PTW1/IRQ1/SIUAISPD
C4	AG12
C5	VBUS
C6	AV_{SS}
C7	PTQ1/AN1
C8	PTX4/DREQ0/$\overline{\text{IrDA\_IN}}$
C9	PTX5/DACK0/IrDA_OUT
C10	PTY2/VIO_D2
C11	PTY6/VIO_D6
C12	PTZ2/VIO_HD1/SIUBILR
C13	PTG0/AUDATA0/TPUTO0

Pin No.	Pin Name
C14	PTG4/AUDSYNC
C15	TMS
C16	$\overline{\text{RESETOUT}}$
C17	BOOT
C18	MD8
C19	MD1
C20	PTW7/IRQ7
C21	PTH2/LCDDON
C22	PTH7/LCDVCPWC
C23	V_{SS}
C24	PTN3/LCDD19/SCIF4_RXD
C25	PTN2/LCDD18/SCIF4_TXD
D1	PTT1/SCIF2_RXD/$\overline{\text{MSIOF0\_SS1}}$/MSIOF0_RSCK
D2	PTX0/TS0_SPSYNC
D3	PTW0/IRQ0/SIUAOSPD
D4	PTW3/IRQ3/ADTRG
D5	AG33
D6	UG12
D7	PTQ3/AN3
D8	V_{SS}
D9	PTX7/DACK1
D10	PTY4/VIO_D4
D11	PTY1/VIO_D1
D12	$\overline{\text{ASEBRK}}$/BRKAK
D13	PTG1/AUDATA1/TPUTO1
D14	PTG5/AUDCK
D15	MD5
D16	PTJ5/PDSTATUS
D17	MD2
D18	MD0
D19	PTW6/IRQ6
D20	PTH3/LCDHSYN/$\overline{\text{LCDCS}}$

Pin No.	Pin Name
D21	PTH4/LCDDISP/LCDRS
D22	VSS
D23	PTN1/LCDD17/DV_VSYNC
D24	PTL5/LCDD13/DV_D13
D25	PTL6/LCDD14/DV_D14
E1	SCL
E2	PTT4/SCIF0_RXD/MSIOF0_RXD
E3	PTX1/TS0_SDEN
E4	PTX3/TS0_SDAT
E5	V_{SS}
E6	REFRIN
E7	AV_{CC}
E8	V_{SS}
E9	V_{SS}
E10	$V_{CC}Q$
E11	$V_{CC}Q$
E12	V_{SS}
E13	V_{SS}
E14	$V_{CC}Q$
E15	$V_{CC}Q$
E16	V_{SS}
E17	V_{SS}
E18	$V_{CC}Q$
E19	$V_{CC}Q$
E20	V_{DD}_PLL
E21	V_{SS}_PLL
E22	PTN4/LCDD20/SCIF4_SCK
E23	PTN0/LCDD16/DV_HSYNC
E24	PTL2/LCDD10/DV_D10
E25	PTL1/LCDD9/DV_D9
F1	SDA
F2	PTS4/$\overline{\text{SCIF3\_CTS}}$/SDHI0D2

Pin No.	Pin Name
F3	PTT2/SCIF2_SCK/MSIOF0_TSYNC
F4	PTT0/SCIF2_TXD/$\overline{\text{MSIOF0\_SS2}}$/MSIOF0_RSYNC
F5	V_{ss}
F21	V_{ss}
F22	PTL7/LCDD15/DV_D15
F23	PTL3/LCDD11/DV_D11
F24	PTM5/LCDD5/DV_D5
F25	PTM4/LCDD4/DV_D4
G1	PTS0/SCIF3_TXD/SDHI0CLK
G2	PTS1/SCIF3_RXD/SDHI0CMD
G3	PTS6/SCIF1_RXD/SDHI0WP
G4	PTT3/SCIF0_TXD/MSIOF0_TXD
G5	$V_{cc}Q$
G21	$V_{cc}Q$
G22	PTL4/LCDD12/DV_D12
G23	PTM7/LCDD7/DV_D7
G24	PTM1/LCDD1/DV_D1
G25	PTM0/LCDD0/DV_D0
H1	PTK5/SIUAIBT/$\overline{\text{MSIOF1\_SS1}}$/MSIOF1_RSCK
H2	PTK6/SIUAILR/$\overline{\text{MSIOF1\_SS2}}$/MSIOF1_RSYNC
H3	PTS2/SCIF3_SCK/SDHI0D0
H4	PTS7/SCIF1_SCK/$\overline{\text{SDHI0CD}}$
H5	$V_{cc}Q$
H21	$V_{cc}Q$
H22	PTL0/LCDD8/DV_D8
H23	PTM2/LCDD2/DV_D2
H24	PTF1/IDEA1/MSIOF0_TXD
H25	PTF2/IDEA2/MSIOF0_RXD
J1	PTK2/SIUAOBT/MSIOF1_TSCK
J2	PTK3/SIUAOLR/MSIOF1_TSYNC
J3	PTK7/SIUAFCK
J4	PTS3/$\overline{\text{SCIF3\_RTS}}$/SDHI0D1

Pin No.	Pin Name
J5	V_{SS}
J21	V_{SS}
J22	PTM3/LCDD3/DV_D3
J23	PTF0/IDEA0/MSIOF0_MCK
J24	PTF4/$\overline{\text{IDECS1}}$/MSIOF0_TSYNC
J25	PTF5/$\overline{\text{IDEIORD}}$/$\overline{\text{MSIOF0\_SS1}}$/MSIOF0_RSCK
K1	PTZ7/SIUBOLR
K2	PTK1/SIUAOSLD/MSIOF1_TXD
K3	PTK4/SIUAISLD/MSIOF1_RXD
K4	PTT5/SCIF0_SCK/MSIOF0_TSCK
K5	V_{SS}
K10	V_{DD}
K11	V_{DD}
K12	V_{DD}
K13	V_{DD}
K14	V_{DD}
K15	V_{DD}
K16	V_{DD}
K21	$V_{CC}Q$
K22	PTM6/LCDD6/DV_D6
K23	PTF3/$\overline{\text{IDECS0}}$/MSIOF0_TSCK
K24	PTD0/IDED0/SDHI0CLK
K25	PTD1/IDED1/SDHI0CMD
L1	PTZ4/SIUBMCK
L2	PTZ6/SIUBOBT
L3	PTK0/SIUAMCK/MSIOF1_MCK
L4	PTS5/SCIF1_TXD/SDHI0D3
L5	$V_{CC}Q$
L10	V_{DD}
L11	V_{DD}
L12	V_{SS}
L13	V_{SS}

Pin No.	Pin Name
L14	V_{SS}
L15	V_{DD}
L16	V_{DD}
L21	$V_{CC}Q$
L22	PTF6/$\overline{\text{IDEIOWR}}$/$\overline{\text{MSIOF0\_SS2}}$/MSIOF0_RSYNC
L23	PTF7/IDEINT
L24	PTD3/IDED3/SDHI0D1
L25	PTD5/IDED5/SDHI0D3
M1	PTU2/FOE/SCIF2_SCK/VIO_VD2
M2	PTU3/$\overline{\text{FWE}}$/SCIF0_TXD
M3	PTU4/FSC/SCIF0_RXD
M4	PTZ5/SIUBOSLD
M5	$V_{CC}Q$
M10	V_{DD}
M11	V_{SS}
M12	V_{SS}
M13	V_{SS}
M14	V_{SS}
M15	V_{SS}
M16	V_{DD}
M21	V_{SS}
M22	PTD2/IDED2/SDHI0D0
M23	PTD4/IDED4/SDHI0D2
M24	PTD6/IDED6/SDHI0WP
M25	PTC0/IDED8/SDHI1CLK
N1	PTV0/NAF0/SCIF3_TXD/VIO_D8
N2	PTU0/$\overline{\text{FCE}}$/SCIF2_TXD/VIO_HD2
N3	PTU1/FRB/SCIF2_RXD/VIO_CLK2
N4	PTU5/FCDE/SCIF0_SCK
N5	V_{SS}
N10	V_{DD}
N11	V_{SS}

Pin No.	Pin Name
N12	V_{SS}
N13	V_{SS}
N14	V_{SS}
N15	V_{SS}
N16	V_{DD}
N21	V_{SS}
N22	PTD7/IDED7/$\overline{\text{SDHI0CD}}$
N23	PTC1/IDED9/SDHI1CMD
N24	PTC2/IDED10/SDHI1D0
N25	PTC3/IDED11/SDHI1D1
P1	PTV3/NAF3/$\overline{\text{SCIF3\_RTS}}$/VIO_D11
P2	PTV1/NAF1/SCIF3_RXD/VIO_D9
P3	PTV2/NAF2/SCIF3_SCK/VIO_D10
P4	PTV4/NAF4/$\overline{\text{SCIF3\_CTS}}$/VIO_D12
P5	V_{SS}
P10	V_{DD}
P11	V_{SS}
P12	V_{SS}
P13	V_{SS}
P14	V_{SS}
P15	V_{SS}
P16	V_{DD}
P21	$V_{CC}Q$
P22	PTC4/IDED12/SDHI1D2
P23	PTC5/IDED13/SDHI1D3
P24	PTC6/IDED14/SDHI1WP
P25	PTC7/IDED15/$\overline{\text{SDHI1CD}}$
R1	PTV5/NAF5/SCIF1_TXD/VIO_D13
R2	PTV7/NAF7/SCIF1_SCK/VIO_D15
R3	RDWR
R4	PTV6/NAF6/SCIF1_RXD/VIO_D14
R5	$V_{CC}Q$

Pin No.	Pin Name
R10	V_{DD}
R11	V_{DD}
R12	V_{SS}
R13	V_{SS}
R14	V_{SS}
R15	V_{DD}
R16	V_{DD}
R21	$V_{CC}Q$
R22	PTE4/$\overline{\text{EXBUF\_ENB}}$/SCIF5_RXD
R23	PTE0/IDEIORDY/SCIF4_TXD
R24	PTE1/IODREQ/SCIF4_RXD
R25	PTE2/$\overline{\text{IODACK}}$/SCIF4_SCK
T1	D15
T2	D7
T3	D6
T4	D4
T5	$V_{CC}Q$
T10	V_{DD}
T11	V_{DD}
T12	V_{DD}
T13	V_{DD}
T14	V_{DD}
T15	V_{DD}
T16	V_{DD}
T21	V_{SS}
T22	PTE5/DIRECTION/SCIF5_SCK
T23	PTE3/$\overline{\text{IDERST}}$/SCIF5_TXD
T24	$V_{CC}Q$
T25	$V_{CC}Q$_DDR
U1	D14
U2	D13
U3	D11

Pin No.	Pin Name
U4	D1
U5	V_{SS}
U21	V_{SS}
U22	V_{CC}Q_DDR
U23	HPA1
U24	HPA2
U25	HPA3
V1	D5
V2	D12
V3	D2
V4	$\overline{\text{CS0}}$
V5	V_{SS}
V21	V_{CC}Q_DDR
V22	HPA0
V23	HPA10
V24	HPA5
V25	HPA4
W1	D3
W2	D10
W3	D0
W4	PTR3/$\overline{\text{IOIS16}}$/LCDLCLK
W5	V_{CC}Q
W21	V_{CC}Q_DDR
W22	HPA15
W23	HPA14
W24	HPA7
W25	HPA6
Y1	D9
Y2	D8
Y3	PTR5/$\overline{\text{CS5B}}$/$\overline{\text{CE1A}}$
Y4	MD3
Y5	V_{CC}Q

Pin No.	Pin Name
Y21	V_{ss}
Y22	$\overline{\text{HPRAS}}$
Y23	$\overline{\text{HPCS}}$
Y24	HPA9
Y25	HPA8
AA1	$\overline{\text{RD}}$
AA2	PTR4/$\overline{\text{CS5A}}$/$\overline{\text{CE2A}}$
AA3	$\overline{\text{WE0}}$
AA4	PTJ0/A22
AA5	V_{ss}
AA6	V_{ss}
AA7	V_{cc}Q
AA8	V_{cc}Q
AA9	V_{ss}
AA10	V_{ss}
AA11	V_{cc}Q
AA12	V_{cc}Q
AA13	V_{ss}
AA14	V_{ss}
AA15	V_{cc}Q_DDR
AA16	V_{cc}Q_DDR
AA17	V_{ss}
AA18	V_{ss}
AA19	V_{cc}Q_DDR
AA20	V_{cc}Q_DDR
AA21	V_{ss}
AA22	VREF
AA23	HPRDWR
AA24	$\overline{\text{HPCAS}}$
AA25	HPA11
AB1	$\overline{\text{WE1}}$
AB2	PTR0/$\overline{\text{WE2}}$/$\overline{\text{ICIORD}}$

Pin No.	Pin Name
AB3	PTJ2/A24
AB4	A20
AB5	A16
AB6	A13
AB7	A7
AB8	A11
AB9	A9
AB10	A1
AB11	PTB4/D28
AB12	PTA2/D18/KEYIN2
AB13	PTB0/D24/KEYOUT3
AB14	V_{CC}Q_DDR
AB15	HPD21
AB16	HPDQM2
AB17	HPD26
AB18	HPD29
AB19	HPD1
AB20	HPD6
AB21	HPD8
AB22	HPD10
AB23	HPA13
AB24	HPCKE
AB25	HPA12
AC1	PTR1/$\overline{\text{WE3}}$/$\overline{\text{ICIOWR}}$
AC2	PTJ3/A25
AC3	A18
AC4	A14
AC5	A10
AC6	A5
AC7	A3
AC8	A0
AC9	PTR7/$\overline{\text{CS6B}}$/$\overline{\text{CE1B}}$

Pin No.	Pin Name
AC10	PTA7/D23/KEYOUT2
AC11	PTA5/D21/KEYOUT0
AC12	PTB2/D26/KEYOUT5/IN5
AC13	PTA1/D17/KEYIN1
AC14	HPD18
AC15	HPD22
AC16	HPDQM3
AC17	HPD25
AC18	HPD30
AC19	HPD2
AC20	HPD5
AC21	HPDQM0
AC22	HPD9
AC23	HPD13
AC24	HPCLK
AC25	$\overline{\text{HPCLK}}$
AD1	PTJ1/A23
AD2	A21
AD3	A17
AD4	A12
AD5	A6
AD6	A2
AD7	$\overline{\text{CS4}}$
AD8	PTR2/$\overline{\text{WAIT}}$
AD9	PTB6/D30
AD10	PTB5/D29
AD11	PTB3/D27
AD12	PTB1/D25/KEYOUT4/IN6
AD13	$V_{CC}Q$
AD14	HPD17
AD15	HPD20
AD16	HPDQS2

Pin No.	Pin Name
AD17	HPD24
AD18	HPD28
AD19	HPD0
AD20	HPD4
AD21	HPDQS0
AD22	HPDQS1
AD23	HPD12
AD24	HPD15
AD25	V_{cc}Q_DDR
AE1	V_{ss}
AE2	A19
AE3	A15
AE4	A8
AE5	A4
AE6	CKO
AE7	PTR6/$\overline{\text{CS6A}}$/$\overline{\text{CE2B}}$
AE8	PTB7/D31
AE9	PTA6/D22/KEYOUT1
AE10	PTA4/D20/KEYIN4
AE11	PTA3/D19/KEYIN3
AE12	PTA0/D16/KEYIN0
AE13	V_{cc}Q_DDR
AE14	HPD16
AE15	HPD19
AE16	HPD23
AE17	HPDQS3
AE18	HPD27
AE19	HPD31
AE20	HPD3
AE21	HPD7
AE22	HPDQM1
AE23	HPD11

Pin No.	Pin Name
AE24	HPD14
AE25	V_{SS}

1.4 Pin Functions

Table 1.3 lists the pin functions.

Table 1.3 Pin Functions of This LSI

Classification	Symbol	I/O	Name	Function
Power supply	V_{DD}	Input	Power supply	Internal LSI power supply. Connect all V_{DD} pins to system power supply. If there is any open pin, the system will not work.
	V_{SS}	Input	Ground	Ground pin. Connect all V_{SS} pins to system power supply (0 V). If there is any open pin, the system will not work.
	$V_{CC}Q$	Input	Power supply	Power supply for I/O pins. Connect all V_{CC} pins to system power supply. If there is any open pin, the system will not work.
	DV33, DV12, AV33, AV12, UV12	Input	Power supply for USB	USB power supply pins
	DG33, DG12, AG33, AG12, UG12	Input	Ground for USB	USB ground pins
	VccQ_DDR	Input	Power supply for DDR I/O	2.5V power supply for DDR I/O
	AVcc	Input	Power supply for ADC	3.3V Power supply for ADC
	AVss	Input	Ground for ADC	Ground for ADC
	V_{DD}_PLL	Input	PLL power supply	Power supply pin for on-chip PLL
	V_{SS}_PLL	Input	PLL ground	Ground pin for on-chip PLL
	V_{DD}_DLL	Input	DLL power supply	Power supply pin for on-chip DLL
	V_{SS}_DLL	Input	DLL ground	Ground pin for on-chip DLL

Classification	Symbol	I/O	Name	Function
Clock	EXTAL	Input	External clock	These are the system clock pins. When the clock mode is 0 or 1, input the external clock from the EXTAL. In this case, the XTAL should be open. When the clock mode is 2, connect the crystal oscillator between the EXTAL and XTAL. When the clock mode is 3, connect the EXTAL to the V_{ss} and the XTAL should be open. Refer to section 14, Clock Pulse Generator (CPG), in the SH7723 Hardware Manual for the details on clock mode.
	XTAL	Output	Clock output	
	RCLK	Input	RTC clock	Connects the RTC clock of 32.768 kHz. This clock must always be input while this LSI is operating.
	SIUAMCK SIUBMCK	Input	SIU external clock	Supplies external clock to the SIU module.
	EXTALUSB	Input	USB clock	48-MHz clock pins for USB. Connect the crystal oscillator between the EXTALUSB and the XTALUSB. When inputting the external clock, connect the external clock signal to the EXTALUSB. In this case, the XTALUSB should be open.
	XTALUSB	Output	USB clock	
Operating mode control	MD8, MD5, MD3, $\overline{\text{TSTMD}}$, MD2, MD1, MD0	Input	Mode setting	Sets operating mode. Do not change any of these pins during operation. MD2 to MD0 are for setting clock mode; MD5 for setting endian. Refer to section 11, Bus State Controller (BSC) or section 14, Clock Pulse Generator (CPG), in the SH7723 Hardware Manual for details. MD8 and $\overline{\text{TSTMD}}$ are for testing. Connect MD8 to $V_{CC}Q$ or GND, and connect $\overline{\text{TSTMD}}$ to $V_{CC}Q$.

Classification	Symbol	I/O	Name	Function
System control	$\overline{\text{RESETP}}$	Input	Power-on reset	System enters power-on reset state when this pin goes low.
	$\overline{\text{RESETOUT}}$	Output	Reset output	This pin goes low while this LSI is in the reset state.
	$\overline{\text{RESETA}}$	Input	Reset input	System enters reset state when this pin goes low with power being supplied.
	STATUS0	Output	Status output	This pin goes high while this LSI is in software standby state.
	PDSTATUS	Output	Power-down status output	This pin goes high during U-standby mode.
	BOOT	Input	Boot mode	Connect it to Vss
	$\overline{\text{TST}}$	Input	Test pin	Connect it to $V_{CC}Q$
Interrupt	NMI	Input	Nonmaskable interrupt	Nonmaskable interrupt request pin. Fix the pin high when not used.
	IRQ7 to IRQ0	Input	Interrupt request 7 to 0	Maskable interrupt request pins. Either level input or edge input is selectable. For level input, the high or low level is selectable. For edge input, rising, falling, and both edges are selectable.

Classification	Symbol	I/O	Name	Function
BSC (asynchronous bus controller)	A25 to A0	Output	Address bus	Outputs an address.
	D31 to D0	I/O	Data bus	16/32-bit bidirectional bus
	$\overline{CS0}$, $\overline{CS4}$, $\overline{CS5A}$, $\overline{CS5B}$, $\overline{CS6A}$, $\overline{CS6B}$,	Output	Chip select	Chip select signal for external memory or device
	$\overline{RD}$	Output	Read strobe	Indicates that data is read from an external device.
	RDWR	Output	Read/write	Read/write signal pin
	$\overline{WE3}$ to $\overline{WE0}$	Output	Write enable	Indicates that data is written to an external memory or device.
	$\overline{WAIT}$	Input	Wait	Input for inserting a wait cycle into bus cycle during access to the external space
	$\overline{BS}$	Output	Bus start	Indicates the start of bus cycle. Asserted by normal space, burst ROM (clock asynchronous), or accessing PCMCIA.
	$\overline{CE1A}$, $\overline{CE2A}$, $\overline{CE1B}$, $\overline{CE2B}$	Output	PCMCIA card select	PCMCIA card select signals
	$\overline{ICIOWR}$	Output	PCMCIA IO write	Strobe signal Indicating I/O write
	$\overline{ICIORD}$	Output	PCMCIA IO read	Strobe signal Indicating I/O read
	$\overline{WE}$	Output	PCMCIA write	Indicates PCMCIA memory write
	$\overline{IOIS16}$	Input	PCMCIA 16bit I/O	Indicates PCMCIA 16-bit I/O. Valid only in little-endian mode. Fix this pin at low in big-endian mode.
	CKO	Output	System clock	Supplies system clock to an external device.

Classification	Symbol	I/O	Name	Function
SBSC (synchronous bus controller for DDR1-SDRAM)	HPA15 to HPA0	Output	Address bus	Outputs an address.
	HPD31 to HPD0	I/O	Data bus	32-bit bidirectional bus
	$\overline{\text{HPCS}}$	Output	Chip select	Chip select signal for DDR-SDRAM
	HPCLK, $\overline{\text{HPCLK}}$	Output	Synchronous clock	Synchronous clock output for DDR-SDRAM
	HPRDWR	Output	Read/write	Read/write signal pin
	HPDQM3 to HPDQM0	Output	Data mask	Write mask enable signals
	HPDQS3 to HPDQS0	Output	Data strobe	Data strobe signals
	$\overline{\text{HPCAS}}$	Output	Column address	Specifies the DDR-SDRAM column address.
	$\overline{\text{HPRAS}}$	Output	Row address	Specifies the DDR-SDRAM row address
	HPCKE	Output	Clock enable	DDR-SDRAM clock enable signal
	Vref	Input	Reference input	Reference power supply for SSTL2
Direct memory access controller (DMAC)	DREQ0, DREQ1	Input	DMA transfer request	External DMA transfer request input pin
	DACK0, DACK1	Output	DMA transfer request acknowledge	Output pin for acknowledgement of external DMA transfer request

Classification	Symbol	I/O	Name	Function
Clock-synchronized serial interface with FIFO (MSIOF0/ MSIOF1)	MSIOF0_MCK MSIOF1_MCK	Input	Master clock	Master clock input
	MSIOF0_TXD MSIOF1_TXD	Output	Transmit data	Transmit data output
	MSIOF0_RXD MSIOF1_RXD	Input	Receive data	Receive data input
	MSIOF0_TSCK MSIOF1_TSCK	I/O	Transmission serial clock	Transmission serial clock input/output Used as SCK when transmission and reception use a common clock.
	MSIOF0_TSYNC MSIOF1_TSYNC	I/O	Transmission frame synchronizing signal	Transmission frame synchronizing signal channel 0 input/output Used as SYNC when transmission and reception use a sync signal.
	$\overline{\text{MSIOF0\_SS1}}$ $\overline{\text{MSIOF1\_SS1}}$	Output	Transmission frame synchronizing signal	Transmission frame synchronizing signal channel 1 output Only slave devices are selectable.
	$\overline{\text{MSIOF0\_SS2}}$ $\overline{\text{MSIOF1\_SS2}}$	Output	Transmission frame synchronizing signal	Transmission frame synchronizing signal channel 2 output Only slave devices are selectable.
	MSIOF0_RSCK MSIOF1_RSCK	I/O	Reception serial clock	Reception serial clock
	MSIOF0_RSYNC MSIOF1_RSYNC	I/O	Reception frame synchronizing signal	Reception frame synchronizing signal

Classification	Symbol	I/O	Name	Function
Serial communication interface with FIFO (SCIF)	SCIF0_TXD, SCIF1_TXD, SCIF2_TXD	Output	Transmit data	Transmit data pin
	SCIF0_RXD, SCIF1_RXD, SCIF2_RXD	Input	Receive data	Receive data pin
	SCIF0_SCK, SCIF1_SCK, SCIF2_SCK	I/O	Serial clock	Clock I/O pin
Serial communication interface with FIFO (SCIFA)	SCIF3_TXD, SCIF4_TXD, SCIF5_TXD	Output	Transmit data	Transmit data pin
	SCIF3_RXD, SCIF4_RXD, SCIF5_RXD	Input	Receive data	Receive data pin
	SCIF3_SCK, SCIF4_SCK, SCIF5_SCK	I/O	Serial clock	Clock I/O pin
	$\overline{\text{SCIF3\_RTS}}$	Output	$\overline{\text{RTS}}$ signal	$\overline{\text{RTS}}$ output pin
	$\overline{\text{SCIF3\_CTS}}$	Input	$\overline{\text{CTS}}$ signal	$\overline{\text{CTS}}$ input pin
Timer pulse unit (TPU)	TPUT3 to TPUT0	Output	Timer pulse output	Pulse output from the TPU
IrDA interface (IrDA)	$\overline{\text{IrDA\_IN}}$	Input	Receive data input	Receive data input
	IrDA_OUT	Output	Transmit data output	Transmit data output
I^{2}C bus interface (IIC)	SCL	I/O	I^{2}C clock I/O	I^{2}C bus clock I/O pin with bus drive function. Output type is NMOS open drain.
	SDA	I/O	I^{2}C data I/O	I^{2}C bus data I/O pin with bus drive function. Output type is NMOS open drain.

Classification	Symbol	I/O	Name	Function
NAND flash memory controller (FLCTL)	FOE	Output	Flash memory output enable	Address latch enable: Asserted for address output and negated for data I/O.
	FSC	Output	Flash memory serial clock	Read enable: Reads data at falling edge.
	$\overline{\text{FCE}}$	Output	Flash memory chip enable	Chip enable: Enables the flash memory connected to this LSI.
	FCDE	Output	Flash memory command data enable	Command latch enable: Asserted at command output.
	FRB	Input	Flash memory ready/busy	Ready/busy: High level indicates ready state and low level indicates busy state.
	$\overline{\text{FWE}}$	Output	Flash memory write enable	Write enable: Flash memory latches commands, addresses, and data at rising edge.
	NAF7 to NAF0	Input	Flash memory data	Data I/O pins
Video I/O (VIO)	VIO_D15 to VIO_D0	Input	VIO data bus	VIO camera image data input
	VIO_CLK1, VIO_CLK2	Input	VIO clock	VIO camera clock input
	VIO_VD1, VIO_VD2	Input	VIO vertical sync	VIO camera vertical sync signal input
	VIO_HD1, VIO_HD2	Input	VIO Horizontal sync	VIO camera horizontal sync signal input
	VIO_FLD	Input	Field signal	Field identification signal
	VIO_CKO	Output	Clock output for camera	Clock output to camera

Classification	Symbol	I/O	Name	Function
LCD controller (RGB interface)	LCDD23 to LCDD0	Output	LCD data bus	24-bit LCD panel data
	LCDDON	Output	Display ON/OFF signal	Display ON/OFF signal (for main LCD)
	LCDHSYN	Output	Horizontal sync signal	Horizontal sync signal
	LCDDISP	Output	Display enable signal	Display enable signal
	LCDVSYN	Output	Vertical sync signal	Vertical sync signal
	LCDVCPWC	Output	Power supply control	LCD module power supply control signal (for main LCD)
	LCDVEPWC	Output	Power supply control	LCD module power supply control signal (for main LCD)
	LCDDCK	Output	Dot clock signal	Data synchronizing signal
	LCDLCLK	Input	Input clock	Input clock signal
LCD controller (SYS interface)	LCDD23 to LCDD0	I/O	Data	Data I/O
	LCDDON	Output	Display ON/OFF signal	Display ON/OFF signal
	$\overline{\text{LCDCS}}$	Output	Chip select	Chip select signal
	$\overline{\text{LCDRD}}$	Output	Read strobe	Read strobe signal
	LCDRS	Output	Register select	Register select signal
	LCDVSYN	I/O	Vertical sync signal	Vertical sync signal
	LCDVCPWC	Output	Power supply control	LCD module power supply control signal
	LCDVEPWC	Output	Power supply control	LCD module power supply control signal
	$\overline{\text{LCDWR}}$	Output	Write strobe	Write strobe signal
	LCDLCLK	Input	Input clock	Input clock signal

Classification	Symbol	I/O	Name	Function
Video output unit (VOU)	DV_D15 to DV_D0	Output	Data output	Data output
	DV_CLK	Output	Clock output	Pixel clock output
	DV_VSYNC	Output	Vertical sync signal output	Vertical sync signal output by the VOU
	DV_HSYNC	Output	Horizontal sync signal output	Horizontal sync signal output by the VOU
	DV_CLKI	Input	Video clock input	Video clock input pin
TS interface (TSIF)	TS_SCK	Input	Clock	TS input clock
	TS_SDAT	Input	Receive data	TS serial data
	TS_SDEN	Input	Data enable	TS data enable signal
	TS_SPSYNC	Input	Data sync signal	TS data sync signal
USB host & function (USB)	VBUS	Input	USB power source detection	USB cable connection monitor pin
	DP	I/O	D+ I/O	USB internal transceiver D+ I/O
	DM	I/O	D- I/O	USB internal transceiver D- I/O
	REFRIN	Input	Reference input	Reference resistor connection pin Connect this pin to AG33 in pull down.

Classification	Symbol	I/O	Name	Function
Sound interface unit (SIUA/SIUB)	SIUAOLR, SIUBOLR	I/O	Sound output L/R clock	Sound output L/R clock pin (master or slave)
	SIUAOBT, SIUBOBT	I/O	Sound output bit clock	Sound output bit clock pin (master or slave)
	SIUAOSLD, SIUBOSLD	Output	Sound output serial data	Sound output serial data pin
	SIUAOSPD	Output	SPDIF output serial data	SPDIF output serial data pin
	SIUAILR, SIUBILR	I/O	Sound input L/R clock	Sound input L/R clock pin (master or slave)
	SIUAIBT, SIUBIBT	I/O	Sound input bit clock	Sound input bit clock pin (master or slave)
	SIUAISLD SIUBISLD	Input	Sound input serial data	Sound input serial data pin
	SIUAISPD	Input	SPDIF input serial data	SPDIF input serial data pin
	SIUAFCK SIUBFCK	Output	Sampling clock output	Sampling clock(clk_fsa and clk_fsb) output pin

Classification	Symbol	I/O	Name	Function
ATAPI interface (ATAPI)	IDED15 to IDED0	I/O	Data bus	16-bit bidirectional data bus
	IDEA2 to IDEA0	Output	Address bus	Address bus
	IDEINT	Input	Interrupt request	Primary channel interrupt request
	$\overline{\text{IDEIOWR}}$	Output	WR enable	Primary channel disk write
	$\overline{\text{IDEIORD}}$	Output	RD enable	Primary channel disk read
	$\overline{\text{IDECS0}}$, $\overline{\text{IDECS1}}$	Output	Chip select	Primary channel chip select
	$\overline{\text{IODACK}}$	Output	DMA acknowledge	Primary channel DMA acknowledge
	IODREQ	Input	DMA request	Primary channel DMA request
	IDEIORDY	Input	Ready	Primary channel ready signal
	$\overline{\text{IDERST}}$	Output	Reset	Primary channel ATAPI device reset
	$\overline{\text{EXBUF\_ENB}}$	Output	External data enable	External level shifter enable
	DIRECTION	Output	External data direction	External level shifter direction
Key scan interface (KEYSC)	KEYIN6 to KEYIN0	Input	Key input	Key scan interface for input
	KEYOUT5 to KEYOUT0	Output	Key output	Key scan interface for output
I/O ports	PTA to PTZ	I/O Input Output	General port	General I/O port pins

Classification	Symbol	I/O	Name	Function
SD host interface (SDHI0 to SDHI1)	$\overline{\text{SDHI0CD}}$, $\overline{\text{SDHI1CD}}$	Input	Card detection	SD card detection signal
	SDHI0WP, SDHI1WP	Input	Write-protection	SD write-protection signal
	SDHI0D3 to SDHI0D0, SDHI1D3 to SDHI1D0	I/O	Data bus	SD data bus signals
	SDHI0CMD, SDHI1CMD	I/O	Command output and response input	SD command output and response input signal
	SDHI0CLK, SDHI1CLK	Output	Clock	SD clock output pin
AD converter (ADC)	AN3 to AN0	Input	Analog input	AD converter input
User debugging interface (H-UDI)*	TCK	Input	Test clock	Test clock input pin
	TMS	Input	Test mode select	Test mode select signal input pin
	TDI	Input	Test data input	Serial input pin for instructions and data
	TDO	Output	Test data output	Serial output pin for instructions and data
	$\overline{\text{TRST}}$	Input	Test reset	Initialization signal input pin
	$\overline{\text{ASEBRK}}$/BRKACK	I/O	Break input/acknowledge	Break signal input from E10A emulator/break acknowledge output signal
	MPMD	Input	ASE mode	Sets emulation support mode
Advanced user debugger (AUD)	AUDATA3 to AUDATA0	Output	AUD data	Branch destination address output pins in branch trace mode
	AUDCK	Output	AUD clock	Synchronizing clock output pin in branch trace mode
	AUDSYNC	Output	AUD synchronizing signal	Data start position recognition signal output pin in branch trace mode

Note: * Refer to the user manual for emulator interface when using the emulator for setting details.

Section 2 Floating-Point Unit (FPU)

2.1 Features

The FPU has the following features.

- Conforms to IEEE754 standard
- 32 single-precision floating-point registers (can also be referenced as 16 double-precision registers)
- Two rounding modes: Round to Nearest and Round to Zero
- Two denormalization modes: Flush to Zero and Treat Denormalized Number
- Six exception sources: FPU Error, Invalid Operation, Divide By Zero, Overflow, Underflow, and Inexact
- Comprehensive instructions: Single-precision, double-precision, graphics support, and system control

When the FD bit in SR is set to 1, the FPU cannot be used, and an attempt to execute an FPU instruction will cause an FPU disable exception (general FPU disable exception or slot FPU disable exception).

Section 3 Memory Management Unit (MMU)

Note: This section contains references to the SH7723 Hardware Manual. The contents of the SH7723 Hardware Manual will be disclosed upon acceptance of a confidentiality agreement. For details, please contact a Renesas Technology sales representative.

This LSI supports an 8-bit address space identifier, a 32-bit virtual address space, and a 29-bit physical address space. Address translation from virtual addresses to physical addresses is enabled by the memory management unit (MMU) in this LSI. The MMU performs high-speed address translation by caching user-created address translation table information in an address translation buffer (translation lookaside buffer: TLB).

This LSI has four instruction TLB (ITLB) entries and 64 unified TLB (UTLB) entries. UTLB copies are stored in the ITLB by hardware. A paging system is used for address translation, with four page sizes (1, 4, and 64 Kbytes, and 1 Mbyte) supported. It is possible to set the virtual address space access right and implement memory protection independently for privileged mode and user mode.

In view of flag functions of the MMU, TLB compatible mode (four paging sizes with four protection bits) and TLB extended mode (eight paging sizes with six protection bits) are provided.

Selection between TLB compatible mode and TLB extended mode is made by setting the relevant control register (bit ME in the MMUCR register) by software.

3.1 Overview of MMU

The MMU was conceived as a means of making efficient use of physical memory. As shown in (0) in figure 3.1, when a process is smaller in size than the physical memory, the entire process can be mapped onto physical memory, but if the process increases in size to the point where it does not fit into physical memory, it becomes necessary to divide the process into smaller parts, and map the parts requiring execution onto physical memory as occasion arises ((1) in figure 3.1). Having this mapping onto physical memory executed consciously by the process itself imposes a heavy burden on the process. The virtual memory system was devised as a means of handling all physical memory mapping to reduce this burden ((2) in figure 3.1). With a virtual memory system, the size of the available virtual memory is much larger than the actual physical memory, and processes are mapped onto this virtual memory. Thus processes only have to consider their operation in virtual memory, and mapping from virtual memory to physical memory is handled by the MMU. The MMU is normally managed by the OS, and physical memory switching is carried out so as to enable the virtual memory required by a process to be mapped smoothly onto physical memory. Physical memory switching is performed via secondary storage, etc.

The virtual memory system that came into being in this way works to best effect in a time sharing system (TSS) that allows a number of processes to run simultaneously ((3) in figure 3.1). Running a number of processes in a TSS did not increase efficiency since each process had to take account of physical memory mapping. Efficiency is improved and the load on each process reduced by the use of a virtual memory system ((4) in figure 3.1). In this virtual memory system, virtual memory is allocated to each process. The task of the MMU is to map a number of virtual memory areas onto physical memory in an efficient manner. It is also provided with memory protection functions to prevent a process from inadvertently accessing another process's physical memory.

When address translation from virtual memory to physical memory is performed using the MMU, it may happen that the translation information has not been recorded in the MMU, or the virtual memory of a different process is accessed by mistake. In such cases, the MMU will generate an exception, change the physical memory mapping, and record the new address translation information.

Although the functions of the MMU could be implemented by software alone, having address translation performed by software each time a process accessed physical memory would be very inefficient. For this reason, a buffer for address translation (the translation lookaside buffer: TLB) is provided by hardware, and frequently used address translation information is placed here. The TLB can be described as a cache for address translation information. However, unlike a cache, if address translation fails—that is, if an exception occurs—switching of the address translation information is normally performed by software. Thus memory management can be performed in a flexible manner by software.

There are two methods by which the MMU can perform mapping from virtual memory to physical memory: the paging method, using fixed-length address translation, and the segment method, using variable-length address translation. With the paging method, the unit of translation is a fixed-size address space called a page.

In the following descriptions, the address space in virtual memory in this LSI is referred to as virtual address space, and the address space in physical memory as physical address space.

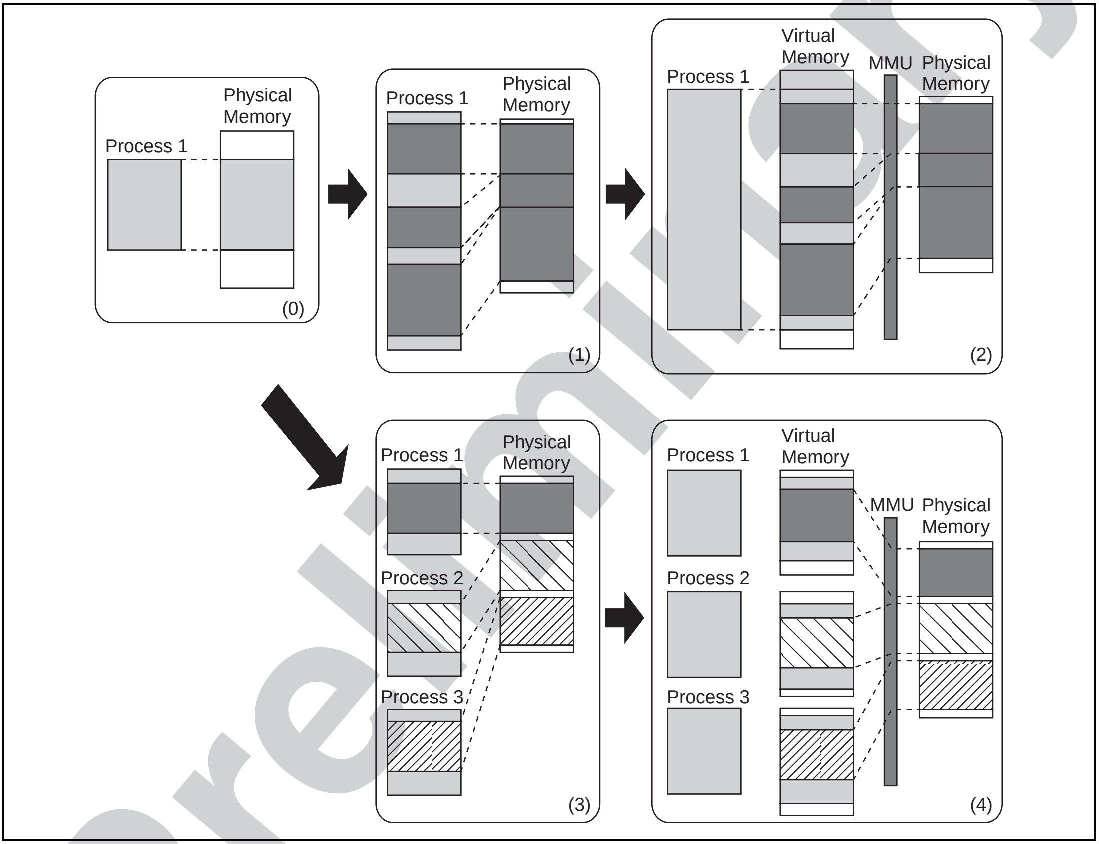


Figure 3.1 Role of MMU

3.1.1 Address Spaces

(1) Virtual Address Space

This LSI supports a 32-bit virtual address space, and can access a 4-Gbyte address space. The virtual address space is divided into a number of areas, as shown in figure 3.2. In privileged mode, the 4-Gbyte space from the P0 area to the P4 area can be accessed. In user mode, a 2-Gbyte space in the U0 area can be accessed. When the RMD bit in the on-chip memory control register (RAMCR) is 1, a 16-Mbyte space in on-chip memory area can be accessed. Accessing areas other than the U0 area and on-chip memory area in user mode will cause an address error.

When the AT bit in MMUCR is set to 1 and the MMU is enabled, the P0, P3, and U0 areas can be mapped onto any physical address space in 1-, 4-, 64-Kbyte, or 1-Mbyte page units in TLB compatible mode and in 1-, 4-, 8-, 64-, 256-Kbyte, 1-, 4-, or 64-Mbyte page units in TLB extended mode. By using an 8-bit address space identifier, the P0, P3, and U0 areas can be increased to a maximum of 256. Mapping from the virtual address space to the 29-bit physical address space is carried out using the TLB.

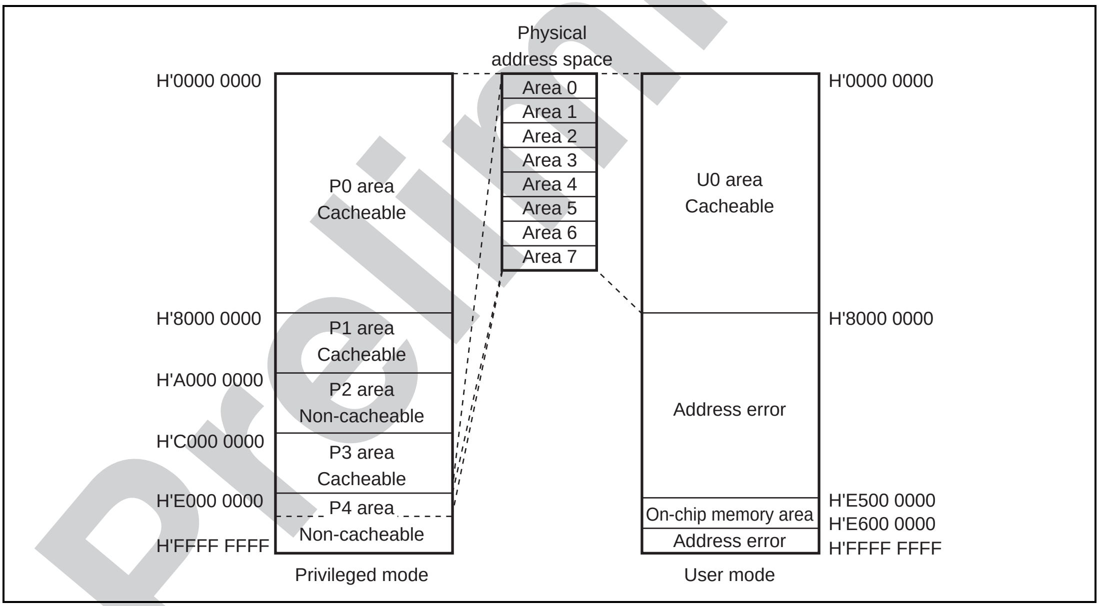


Figure 3.2 Virtual Address Space (AT in MMUCR= 0)

Section 4 Caches

Note: This section contains references to the SH7723 Hardware Manual. The contents of the SH7723 Hardware Manual will be disclosed upon acceptance of a confidentiality agreement. For details, please contact a Renesas Technology sales representative.

This LSI has an on-chip 32-Kbyte instruction cache (IC) for instructions and an on-chip 32-Kbyte operand cache (OC) for data. In addition, this LSI includes an on-chip 256-Kbyte secondary cache with an instruction/data unified structure.

4.1 Features

The features of the cache are given in table 4.1.

Table 4.1 Cache Features

Item	Instruction Cache	Operand Cache
Capacity	32-Kbyte cache	32-Kbyte cache
Type	4-way set-associative, virtual address index/physical address tag	4-way set-associative, virtual address index/physical address tag
Line size	32 bytes	32 bytes
Entries	256 entries/way	256 entries/way
Write method	—	Copy-back/write-through selectable
Replacement method	LRU (least-recently-used) algorithm	LRU (least-recently-used) algorithm

The operand cache of this LSI is 4-way set-associative, each way comprising 256 cache lines. Figure 4.1 shows the configuration of the operand cache.

The instruction cache is 4-way set-associative, each way comprising 256 cache lines. Figure 4.2 shows the configuration of the instruction cache.

This LSI has an IC way prediction scheme to reduce power consumption. In addition, memory-mapped associative writing, which is detectable as an exception, can be enabled by using the non-support detection exception register (EXPMASK). For details, see section 5, Exception Handling, in the SH7723 Hardware Manual.

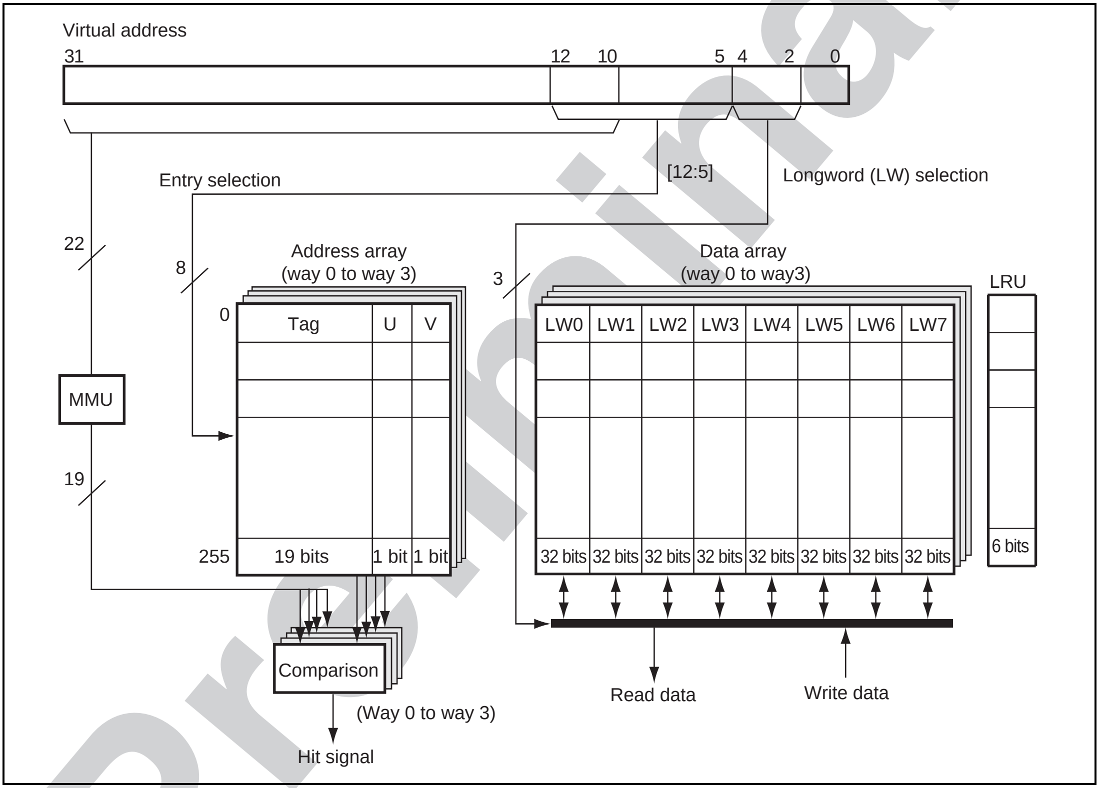


Figure 4.1 Configuration of Operand Cache

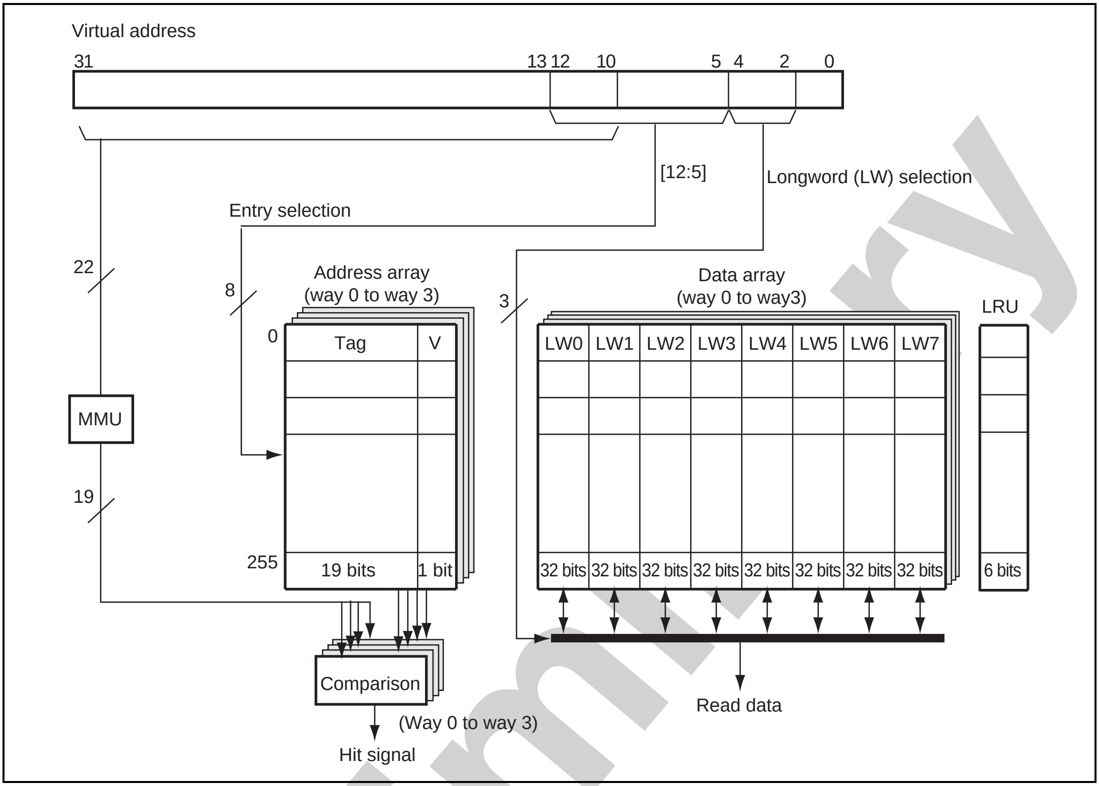


Figure 4.2 Configuration of Instruction Cache

- Tag

  Stores the upper 19 bits of the 29-bit physical address of the data line to be cached. The tag is not initialized by a power-on or manual reset.
- V bit (validity bit)

  Indicates that valid data is stored in the cache line. When this bit is 1, the cache line data is valid. The V bit is initialized to 0 by a power-on reset, but retains its value in a manual reset.
- U bit (dirty bit)

  The U bit is set to 1 if data is written to the cache line while the cache is being used in copy-back mode. That is, the U bit indicates a mismatch between the data in the cache line and the data in external memory. The U bit is never set to 1 while the cache is being used in write-through mode, unless it is modified by accessing the memory-mapped cache (see section 8.6, Memory-Mapped Cache Configuration, in the SH7723 Hardware Manual). The U bit is initialized to 0 by a power-on reset, but retains its value in a manual reset.

- Data array

  The data field holds 32 bytes (256 bits) of data per cache line. The data array is not initialized by a power-on or manual reset.

- LRU

  In a 4-way set-associative method, up to 4 items of data can be registered in the cache at each entry address. When an entry is registered, the LRU bit indicates which of the 4 ways it is to be registered in. The LRU mechanism uses 6 bits of each entry, and its usage is controlled by hardware. The LRU (least-recently-used) algorithm is used for way selection, and selects the less recently accessed way. The LRU bits are initialized to 0 by a power-on reset but not by a manual reset. The LRU bits cannot be read from or written to by software.

Section 5 IL Memory

This LSI incorporates a 16-Kbyte IL memory which is suitable for instruction storage.

5.1 Features

(1) IL Memory

- Capacity
  16 Kbytes
- Page
  The IL memory is divided into four pages (pages 0, 1, 2, and 3).
- Memory map
  The IL memory is allocated to the addresses shown in table 5.1 in both the virtual address space and the physical address space.

Table 5.1 IL Memory Addresses

Page	Memory Size 16 Kbyte
Page 0	H'E520 0000 to H'E520 0FFF
Page 1	H'E520 1000 to H'E520 1FFF
Page 2	H'E520 2000 to H'E520 2FFF
Page 3	H'E520 3000 to H'E520 3FFF

- Ports

  The page has three independent read/write ports and is connected to the SuperHyway bus, the cache/RAM internal bus, and the instruction bus. The instruction bus is used when the IL memory is accessed through instruction fetch. The cache/RAM internal bus is used when the IL memory is accessed through operand access. The SuperHyway bus is used for IL memory access from the SuperHyway bus master module.

- Priority

  In the event of simultaneous accesses to the same page from different buses, the access requests are processed according to priority. The priority order is: SuperHyway bus > cache/RAM internal bus > instruction bus.

Section 6 Interrupt Controller (INTC)

The interrupt controller (INTC) determines the priority of interrupt sources and controls interrupt requests to the CPU. Some INTC registers set the priority of each interrupt and interrupt requests are processed according to the user-set priority.

6.1 Features

The INTC has the following features.

- Fifteen levels of interrupt priority can be set

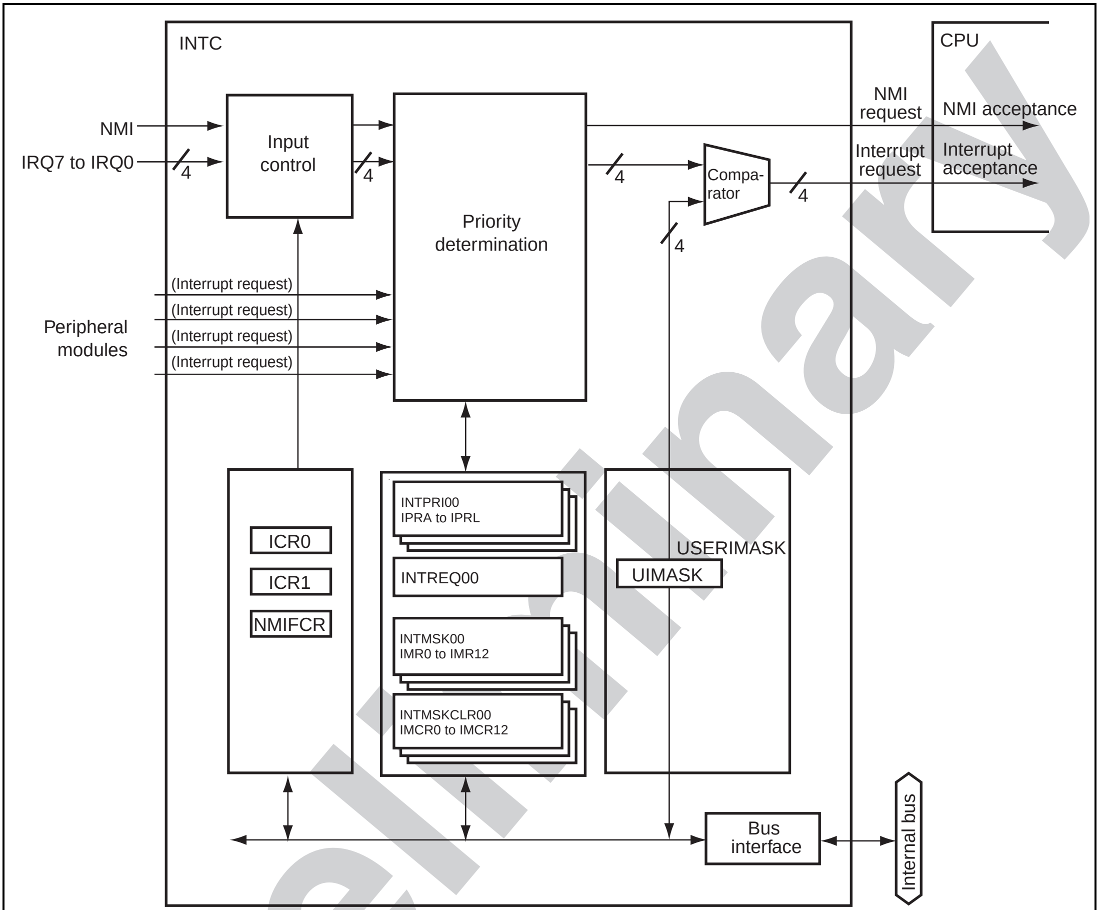
  By setting the interrupt priority registers, the priorities of on-chip peripheral module interrupts can be selected from 15 levels for individual request sources.
- NMI noise canceler function

  An NMI input-level bit indicates the NMI pin state. By reading this bit in the interrupt exception handling routine, the pin state can be checked, enabling it to be used as a noise canceler.
- NMI request masking when the block bit (BL) in the status register (SR) is set to 1

  Whether to mask NMI requests when the BL bit in SR is set to 1 can be selected.
- User-mode interrupt disabling function

  Specifying an interrupt mask level in the user interrupt mask level register (USERIMASK) disables interrupts which are not higher in priority than the specified mask level in user mode.

Figure 6.1 shows a block diagram of the INTC.



[Legend]

ICR0, ICR1:	Interrupt control registers 0, 1
NMIFCR:	NMI flag control register
INTPRI00, IPRA to IPRL:	Interrupt priority registers
INTREQ00:	Interrupt request register
INTMSK00, IMR0 to IMR12:	Interrupt mask registers
INTMSKCLR00, IMCR0 to IMCR12:	Interrupt mask clear registers
USERIMASK:	User interrupt mask level register

Figure 6.1 Block Diagram of INTC

6.2 Input/Output Pins

Table 6.1 shows the INTC pin configuration.

Table 6.1 Pin Configuration

Pin Name	Function	I/O	Description
NMI	Nonmaskable interrupt input pin	Input	Input of interrupt request signal that is not maskable
IRQ7 to IRQ0	IRQ7 to IRQ0 interrupt input pins	Input	Input of IRQ7 to IRQ0 interrupt request signals (maskable by the IMASK bit setting in SR)

6.3 Interrupt Sources

There are three types of interrupt sources: NMI, IRQ, and on-chip peripheral modules. Each interrupt has a priority level (16 to 0), with 1 the lowest and 16 the highest. Priority level 0 masks an interrupt, so the interrupt request is ignored.

6.3.1 NMI Interrupt

The NMI interrupt has the highest priority level of 16. When the BL bit in SR of the CPU is 0, NMI interrupts are always accepted. In sleep or standby mode, NMI interrupts are accepted regardless of the BL setting. In addition, NMI interrupts are accepted by setting the NMIB bit in ICR0 regardless of the BL setting.

The NMI signal is edge-detected. The NMIE bit in ICR0 is used to select either rising or falling edge detection. After the NMIE bit in ICR0 is modified, NMI interrupts are not detected for a maximum of six bus clock cycles.

NMI interrupt exception handling does not affect the interrupt mask level (IMASK) in SR.

6.3.2 IRQ Interrupts

IRQ interrupts are input from pins IRQ7 to IRQ0. When level-sensing is selected for IRQ interrupts by the IRQnS bits (n = 0 to 7) in ICR1, the pin levels must be retained until the CPU accepts the interrupts and starts interrupt handling.

If an interrupt request is canceled before the CPU accepts it, the INTC holds the interrupt source until the CPU accepts another interrupt. The interrupt held in the INTC can be cleared by setting the corresponding interrupt mask bit (IMR bit in the interrupt mask register) to 1.

When the INTMU bit in CPUOPM is set to 1, the interrupt mask level (IMASK) in SR is automatically modified to the level of the accepted interrupt. When the INTMU bit is cleared to 0, the IMASK value in SR is not affected by the accepted interrupt.

6.3.3 On-Chip Peripheral Module Interrupts

On-chip peripheral module interrupts are generated by the peripheral modules.

Not every interrupt source is assigned a different interrupt vector. Sources are reflected in the interrupt event register (INTEVT). It is easy to identify sources by using the value of INTEVT as a branch offset in the exception handling routine.

A priority level (from 15 to 0) can be set for each module by writing to IPRA to IPRL.

When the INTMU bit in the CPUOPM is set to 1, the interrupt mask level (IMASK) in SR is automatically modified to the level of the accepted interrupt. When the INTMU bit in CPUOPM is cleared to 0, the IMASK value in SR is not affected by the accepted interrupt.

The interrupt source flags and interrupt enable flags in each peripheral module must be updated only while the BL bit in SR is set to 1 or corresponding interrupt request is masked by the IMASK bit in SR, IMRs, or USERIMASK. To prevent accepting unintentional interrupts that should have been updated, read the on-chip peripheral register with the corresponding flag, wait for the priority determination time for peripheral modules shown in table 6.4 (e.g. a period required to read a register in INTC once which are driven by the peripheral module clock), and then clear the BL bit to 0 or clear the corresponding interrupt mask by changing the mask setting. Thus, the necessary interval for internal processing is ensured. To update multiple flags, after updating the last flag, read only the register that includes the last flag.

If a flag is updated while the BL bit is 0, execution may branch to the interrupt handling routine with INTEVT = 0; interrupt handling may start depending on the timing relationship between flag updating and interrupt request detection in the LSI. In this case, operation can be continued without causing any problems by executing the RTE instruction.

6.3.4 Interrupt Exception Handling and Priority

Tables 6.2 and 6.3 show the interrupt sources, the codes for the interrupt event register (INTEVT), and the interrupt priority.

Each interrupt source is assigned to a unique INTEVT code. The start address of the exception handling routine is common for all interrupt sources. This is why, for instance, the value of INTEVT is used as an offset at the start of the exception handling routine to branch execution in order to identify the interrupt source.

On-chip peripheral module interrupt priorities can be set freely between 15 and 0 for each module by using IPRA to IPRL. A reset assigns priority level 0 to the on-chip peripheral module interrupts.

If the same priority level is assigned to two or more interrupt sources and interrupts from those sources occur simultaneously, their priority is determined according to the default priority indicated at the right in tables 6.2 and 6.3.

Interrupt priority registers and interrupt mask registers must be updated only while the BL bit in SR is set to 1. To prevent accepting unintentional interrupts, read any interrupt priority register and then clear the BL bit to 0, which ensures the necessary interval for internal processing.

Table 6.2 External Interrupt Sources and Priority

Interrupt Source		INTEVT Code	Interrupt Priority (Initial Value)	IPR (Bit Numbers)	Priority within IPR Setting Range	Default Priority
NMI		H'1C0	16	—	—	High
IRQ	IRQ0	H'600	15 to 0 (0)	INTPRI00 (31 to 28)	—	↑
	IRQ1	H'620	15 to 0 (0)	INTPRI00 (27 to 24)	—	
	IRQ2	H'640	15 to 0 (0)	INTPRI00 (23 to 20)	—	
	IRQ3	H'660	15 to 0 (0)	INTPRI00 (19 to 16)	—	
	IRQ4	H'680	15 to 0 (0)	INTPRI00 (15 to 12)	—	
	IRQ5	H'6A0	15 to 0 (0)	INTPRI00 (11 to 8)	—	
	IRQ6	H'6C0	15 to 0 (0)	INTPRI00 (7 to 4)	—	↓
	IRQ7	H'6E0	15 to 0 (0)	INTPRI00 (3 to 0)	—	Low

Table 6.3 On-Chip Peripheral Module Interrupt Sources and Priority

Interrupt Source		INTEVT Code	Interrupt Priority (Initial Value)	Corresponding IPR (Bit Numbers)	Priority within IPR Setting Range	Default Priority
HUDI		H'5E0	15	—	—	High
DMAC1A	DEI0	H'700	15 to 0 (0)	IPRB (7 to 4)	High	↑
	DEI1	H'720	15 to 0 (0)		↕	
	DEI2	H'740	15 to 0 (0)			
	DEI3	H'760	15 to 0 (0)		Low	
2DG	TRI	H'780	15 to 0 (0)	IPRI (3 to 0)	High	
	INI	H'7A0	15 to 0 (0)		↕	
	CEI	H'7C0	15 to 0 (0)		Low	
DMAC0A	DEI0	H'800	15 to 0 (0)	IPRE (15 to 12)	High	
	DEI1	H'820	15 to 0 (0)		↕	
	DEI2	H'840	15 to 0 (0)			
	DEI3	H'860	15 to 0 (0)		Low	
VIO	CEUI	H'880	15 to 0 (0)	IPRE (11 to 8)	High	
	BEUI	H'8A0	15 to 0 (0)		↕	
	VEUI	H'8C0	15 to 0 (0)			
	VOUI	H'8E0	15 to 0 (0)		Low	
SCIFA	SCIFA0	H'900	15 to 0 (0)	IPRE (7 to 4)	—	
VPU	VPUI	H'980	15 to 0 (0)	IPRE (3 to 0)	—	
TPU	TPUI	H'9A0	15 to 0 (0)	IPRL (7 to 4)	—	
ADC	ADI	H'9E0	15 to 0 (0)	IPRJ (15 to 12)	—	
USB	USI0	H'A20	15 to 0 (0)	IPRF (7 to 4)	—	
RTC	ATI	H'A80	15 to 0 (0)	IPRK (15 to 12)	High	
	PRI	H'AA0	15 to 0 (0)		↕	
	CUI	H'AC0	15 to 0 (0)		Low	
DMAC1B	DEI4	H'B00	15 to 0 (0)	IPRK (11 to 8)	High	
	DEI5	H'B20	15 to 0 (0)		↕	↓
	DADERR	H'B40	15 to 0 (0)		Low	Low

Interrupt Source		INTEVT Code	Interrupt Priority (Initial Value)	Corresponding IPR (Bit Numbers)	Priority within IPR Setting Range	Default Priority
DMAC0B	DEI4	H'B80	15 to 0 (0)	IPRF (11 to 8)	High	High
	DEI5	H'BA0	15 to 0 (0)			
	DADERR	H'BC0	15 to 0 (0)		Low	
KEYSC	KEYI	H'BE0	15 to 0 (0)	IPRF (15 to 12)	—	
SCIF	SCIF0	H'C00	15 to 0 (0)	IPRG (15 to 12)	—	
	SCIF1	H'C20	15 to 0 (0)	IPRG (11 to 8)	—	
	SCIF2	H'C40	15 to 0 (0)	IPRG (7 to 4)	—	
MSIOF	MSIOFI0	H'C80	15 to 0 (0)	IPRH (15 to 12)	—	
	MSIOFI1	H'CA0	15 to 0 (0)	IPRH (11 to 8)	—	
SCIFA	SCIFA1	H'D00	15 to 0 (0)	IPRI (15 to 12)	—	
ICB	ICBI	H'D20	15 to 0 (0)	IPRI (11 to 8)	—	
FLCTL	FLSTEI	H'D80	15 to 0 (0)	IPRH (7 to 4)	High	
	FLTENDI	H'DA0	15 to 0 (0)			
	FLTREQ0I	H'DC0	15 to 0 (0)			
	FLTREQ1I	H'DE0	15 to 0 (0)		Low	
I^{2}C	ALI	H'E00	15 to 0 (0)	IPRH (3 to 0)	High	
	TACKI	H'E20	15 to 0 (0)			
	WAITI	H'E40	15 to 0 (0)			
	DTEI	H'E60	15 to 0 (0)		Low	
SDHI0	SDHII0	H'E80	15 to 0 (0)	IPRK (3 to 0)	High	
	SDHII1	H'EA0	15 to 0 (0)			
	SDHII2	H'EC0	15 to 0 (0)		Low	
CMT	CMTI	H'F00	15 to 0 (0)	IPRF (3 to 0)	—	
TSIF	TSIFI	H'F20	15 to 0 (0)	IPRI (7 to 4)	—	Low

Interrupt Source		INTEVT Code	Interrupt Priority (Initial Value)	Corresponding IPR (Bit Numbers)	Priority within IPR Setting Range	Default Priority
SIU	SIUI	H'F80	15 to 0 (0)	IPRJ (7 to 4)	—	High
SCIFA	SCIFA2	H'FA0	15 to 0 (0)	IPRL (15 to 12)	—	
TMU0	TUNI0	H'400	15 to 0 (0)	IPRA (15 to 12)	—	
	TUNI1	H'420	15 to 0 (0)	IPRA (11 to 8)	—	
	TUNI2	H'440	15 to 0 (0)	IPRA (7 to 4)	—	
IrDA	IRDAI	H'480	15 to 0 (0)	IPRA (3 to 0)	—	
ATAPI	ATAPII	H'4A0	15 to 0 (0)	IPRL (3 to 0)	—	
SDHI1	SDHII0	H'4E0	15 to 0 (0)	IPRJ (3 to 0)	High	
	SDHII1	H'500	15 to 0 (0)			
	SDHII2	H'520	15 to 0 (0)		Low	
VEU2H1	VEU2HI	H'560	15 to 0 (0)	IPRB (15 to 12)	—	
LCDC	LCDCI	H'580	15 to 0 (0)	IPRB (11 to 8)	—	
TMU1	TUNI0	H'920	15 to 0 (0)	IPRC (15 to 12)	—	
	TUNI1	H'940	15 to 0 (0)	IPRC (11 to 8)	—	
	TUNI2	H'960	15 to 0 (0)	IPRC (7 to 4)	—	Low

6.4 Operation

6.4.1 Interrupt Sequence

The sequence of interrupt operations is described below. Figures 6.2 and 6.3 are flowcharts of the operations.

1. The interrupt request sources send interrupt request signals to the INTC.
2. The INTC selects the highest-priority interrupt from the sent interrupt requests according to the interrupt priority registers. Lower-priority interrupts are held pending. If two of these interrupts have the same priority level or if multiple interrupts occur within a single module, the interrupt with the highest priority is selected according to tables 6.2 and 6.3.
3. The priority level of the interrupt selected by the INTC is compared with the interrupt mask level (IMASK) set in SR of the CPU. If the priority level is higher than the mask level, the INTC accepts the interrupt and sends an interrupt request signal to the CPU.
4. The CPU accepts an interrupt at a break in instructions.
5. The interrupt source code is set in the interrupt event register (INTEVT).
6. SR and program counter (PC) are saved to SSR and SPC, respectively. R15 is saved to SGR at this time.
7. The BL, MD, and RB bits in SR are set to 1.
8. Execution jumps to the start address of the interrupt exception handling routine (the sum of the value set in the vector base register (VBR) and H'0000 0600).

In the exception handling routine, execution may branch with the INTEVT value used as its offset in order to identify the interrupt source. This enables execution to branch to the handling routine for the individual interrupt source.

Notes: 1. When the INTMU bit in the CPU operating mode register (CPUOPM) is set to 1, the interrupt mask level (IMASK) in SR is automatically set to the level of the accepted interrupt. When the INTMU bit is cleared to 0, the IMASK value in SR is not affected by the accepted interrupt.

2. The interrupt source flag should be cleared in the interrupt handler. To ensure that an interrupt source that should have been cleared is not inadvertently accepted again, read the interrupt source flag, wait for the priority determination time for peripheral modules shown in table 6.4 (e.g. a period required to read a register in INTC once which is driven by the peripheral module clock), and then clear the BL bit or execute an RTE instruction.

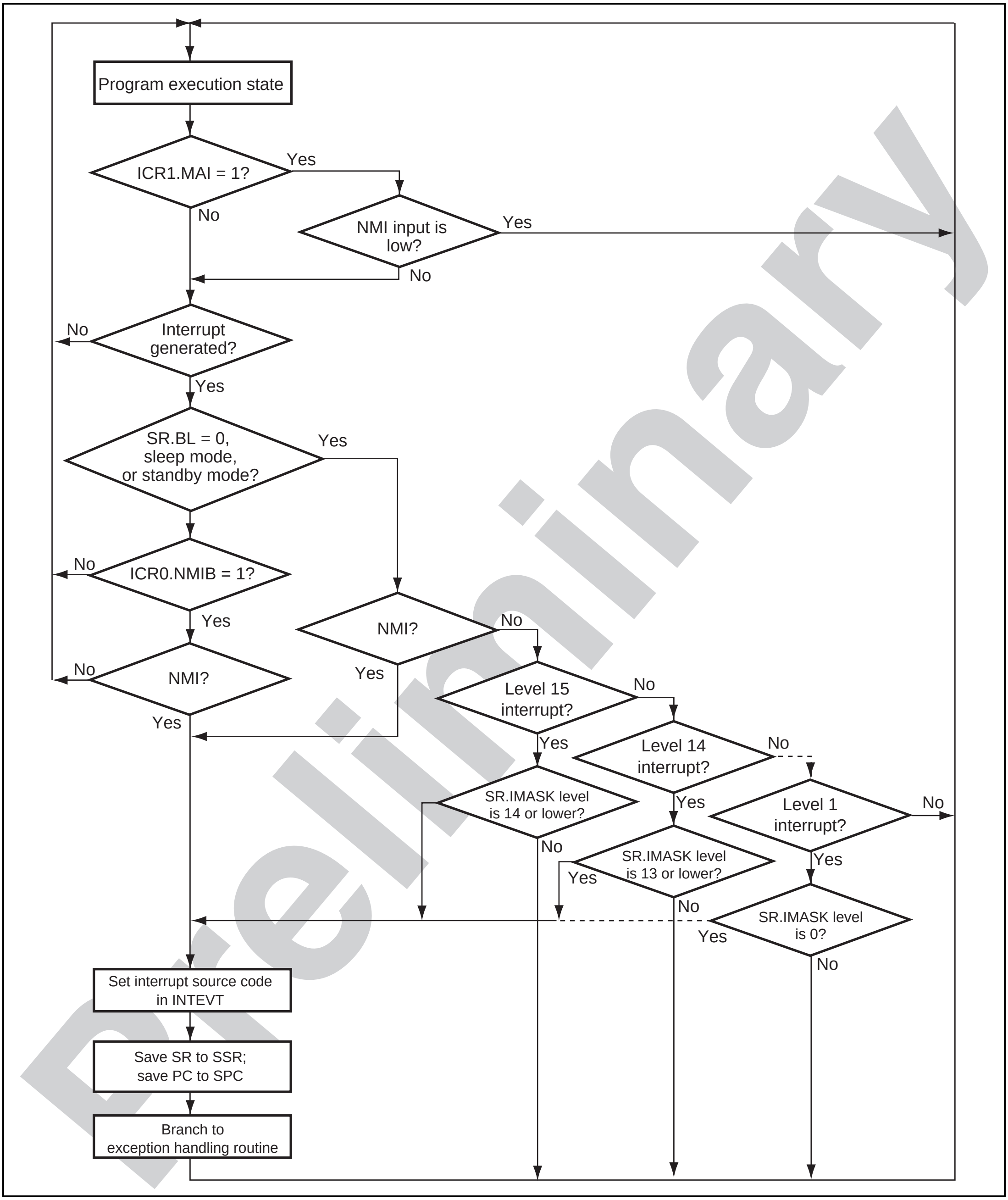


Figure 6.2 Interrupt Operation Flowchart (when CPUOPM.INTMU = 0)

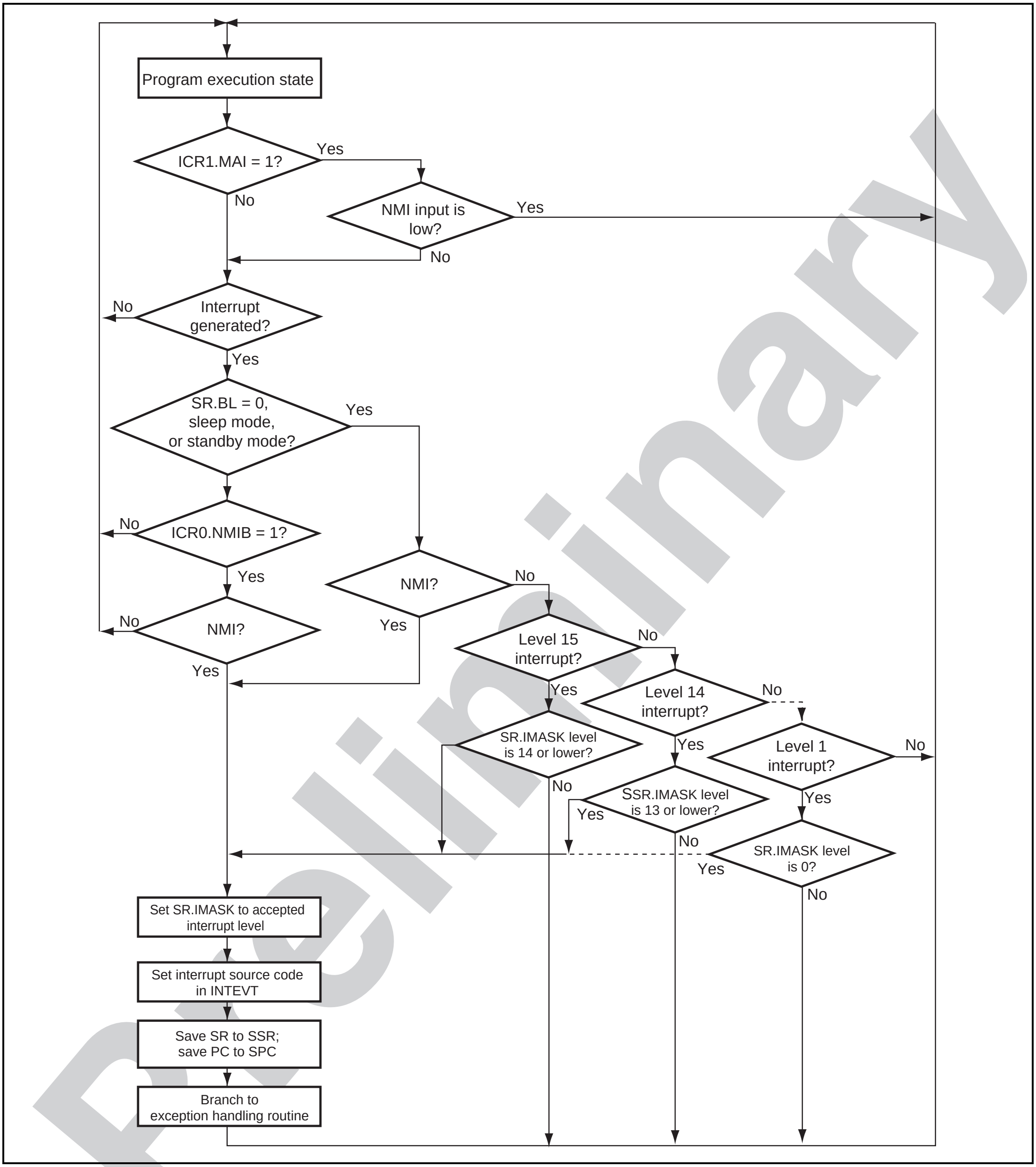


Figure 6.3 Interrupt Operation Flowchart (when CPUOPM.INTMU = 1)

6.4.2 Multiple Interrupts

When handling multiple interrupts, an interrupt handling routine should include the following procedures:

1. To identify the interrupt source, branch to a specific interrupt handling routine for the interrupt source by using the INTEVT code as an offset.
2. Clear the interrupt source in each specific interrupt handling routine.
3. Save SSR and SPC to the stack.
4. Clear the BL bit in SR. When the INTMU bit in CPUOPM is set to 1, the interrupt mask level (IMASK) in SR is automatically modified to the level of the accepted interrupt. When the INTMU bit in CPUOPM is cleared to 0, set the IMASK bit in SR by software to the accepted interrupt level.
5. Handle the interrupt as required.
6. Set the BL bit in SR to 1.
7. Restore SSR and SPC from memory.
8. Execute the RTE instruction.

When these procedures are followed in order, an interrupt of higher priority than the one being handled can be accepted if multiple interrupts occur after step 4. This reduces the interrupt response time for urgent processing.

6.4.3 Interrupt Masking by MAI Bit

Setting the MAI bit in ICR0 to 1 masks interrupts while the NMI signal is low regardless of the BL and IMASK bit settings in SR.

- Normal operation or sleep mode

  All interrupts are masked while the NMI signal is low. Note that only NMI interrupts due to NMI signal input occur.
- Standby mode

  All interrupts including NMI are masked while the NMI signal is low. And an NMI interrupt is not generated by the change of NMI pin state, too. While the MAI bit is set to 1, the NMI interrupt cannot be used to clear standby mode.

6.4.4 Interrupt Disabling Function in User Mode

Setting the interrupt mask level in USERIMASK disables interrupts having an equal or lower priority level than the specified mask level. This function can disable less-urgent interrupts in a task (such as device driver) operating in user mode to accelerate urgent processing.

USERIMASK is allocated to a different 64-Kbyte page than where the other INTC registers are allocated. When accessing this register in user mode, translate the address through the MMU. In the system that uses a multitasking OS, processes that can access USERIMASK must be controlled by using memory protection functions of the MMU. When terminating the task or switching to another task, be sure to clear USERIMASK to 0 before quitting the task. If the UIMASK bits are left set to a non-zero value, interrupts which are not higher in priority than the UIMASK level are held disabled, and correct operation may not be performed (for example, the OS cannot switch tasks).

A sample sequence of user-mode interrupt disabling operation is described below.

1. Classify interrupts into A and B shown below, and assign higher interrupt levels to A than B.
   A. Interrupts that should be accepted in the device driver
      (interrupts used by the OS, such as timer interrupts)
   B. Interrupts that should be disabled in the device driver
2. Make the MMU settings so that the address space including USERIMASK can only be accessed by the device driver in which interrupts should be disabled.
3. Branch to the device driver.
4. Specify the UIMASK bits so that interrupts B are masked in the device driver operating in user mode.
5. Perform urgent processing in the device driver.
6. Clear the UIMASK bits to 0 to return from the device driver processing.

6.5 Interrupt Response Time

Table 6.4 shows the interrupt response time, which is the interval from when an interrupt request occurs until the interrupt exception handling is started and the start instruction of the exception handling routine is fetched.

Table 6.4 Interrupt Response Time

<table>
<tr><th rowspan="2" colspan="2">Item</th><th colspan="3">Number of States</th><th rowspan="2">Remarks</th></tr>
<tr><th>NMI</th><th>IRQ</th><th>Peripheral Module</th></tr>
<tr><td colspan="2">Priority determination time</td><td>5 Bcyc + 2 Pcyc</td><td>4 Bcyc + 2 Pcyc</td><td>5 Pcyc</td><td></td></tr>
<tr><td colspan="2">Wait time until the CPU finishes the current sequence</td><td colspan="3">S - 1 (≥ 0) × Icyc</td><td></td></tr>
<tr><td colspan="2">Interval from when interrupt exception handling begins (saving SR and PC) until a SuperHyway bus request is issued to fetch the start instruction of the exception handling routine</td><td colspan="3">11 Icyc + 1 Scyc</td><td></td></tr>
<tr><td rowspan="2">Response time</td><td>Total</td><td>(S + 10) Icyc + 1 Scyc + 5 Bcyc + 2 Pcyc</td><td>(S + 10) Icyc + 1 Scyc + 4 Bcyc + 2 Pcyc</td><td>(S + 10) Icyc + 1 Scyc + 5 Pcyc</td><td></td></tr>
<tr><td>Minimum</td><td>18 Icyc + S × Icyc</td><td>17 Icyc + S × Icyc</td><td>16 Icyc + S × Icyc</td><td>When Icyc:Scyc:Bcyc: Pcyc = 1:1:1:1</td></tr>
</table>

[Legend]

Icyc: Period for one CPU clock cycle

Scyc: Period for one SH clock cycle

Bcyc: Period for one bus clock cycle

Pcyc: Period for one peripheral clock cycle

S: Number of instruction execution states

Section 7 Bus State Controller (BSC)

Note: This section contains references to the SH7723 Hardware Manual. The contents of the SH7723 Hardware Manual will be disclosed upon acceptance of a confidentiality agreement. For details, please contact a Renesas Technology sales representative.

The bus state controller (BSC) outputs control signals for various types of memory that is connected to the external address space and external devices. The BSC functions enable this LSI to connect directly with SRAM, burst ROM, and other memory storage devices, and external devices. SDRAM is controlled by the bus state controller for SDRAM (SBSC).

7.1 Features

The BSC has the following features:

1. External address space
- Supports totally 256 Mbytes at a maximum. The space is divided into either six or four areas as shown below.
  - Address map 1: Six areas of $\overline{\text{CS0}}$, $\overline{\text{CS4}}$, $\overline{\text{CS5A}}$, $\overline{\text{CS5B}}$, $\overline{\text{CS6A}}$, and $\overline{\text{CS6B}}$
  - Address map 2: Four areas of $\overline{\text{CS0}}$, $\overline{\text{CS4}}$, $\overline{\text{CS5}}$, and $\overline{\text{CS6}}$
- Can specify the normal space interface, SRAM interface with byte selection, burst ROM (clock asynchronous), or various PCMCIA interfaces for each address space
- Can select the data bus width (8, 16, or 32 bits) for each address space
- Controls insertion of wait cycle for each address space
- Controls insertion of wait cycle for each read access and write access
- Can set independent idle cycles in the continuous access for five cases: read-write (in the same space/different spaces), read-read (in the same space/different spaces), or the first cycle is a write access

2. Normal space interface
- Supports the interface that can be connected directly to SRAM

3. Burst ROM interface (clock asynchronous)
- High-speed access to ROM that has the page mode function

4. SRAM interface with byte selection
- Supports the interface that can be connected directly to SRAM with byte selection

5. PCMCIA direct-connection interfaces
- Supports the "IC memory card and I/O card interface" provided with JEIDA Ver4.2 (PCMCIA2.1)

- Controls the insertion of wait states by the program
- Supports the bus-sizing function of the I/O bus width. (only in little endian mode.)

Note: For the PCMCIA direct-connection interfaces, the BSC supports only the signals and bus protocols listed in table 7.1. Use an external circuit for the other control signals.

A block diagram of the BSC is shown in figure 7.1.

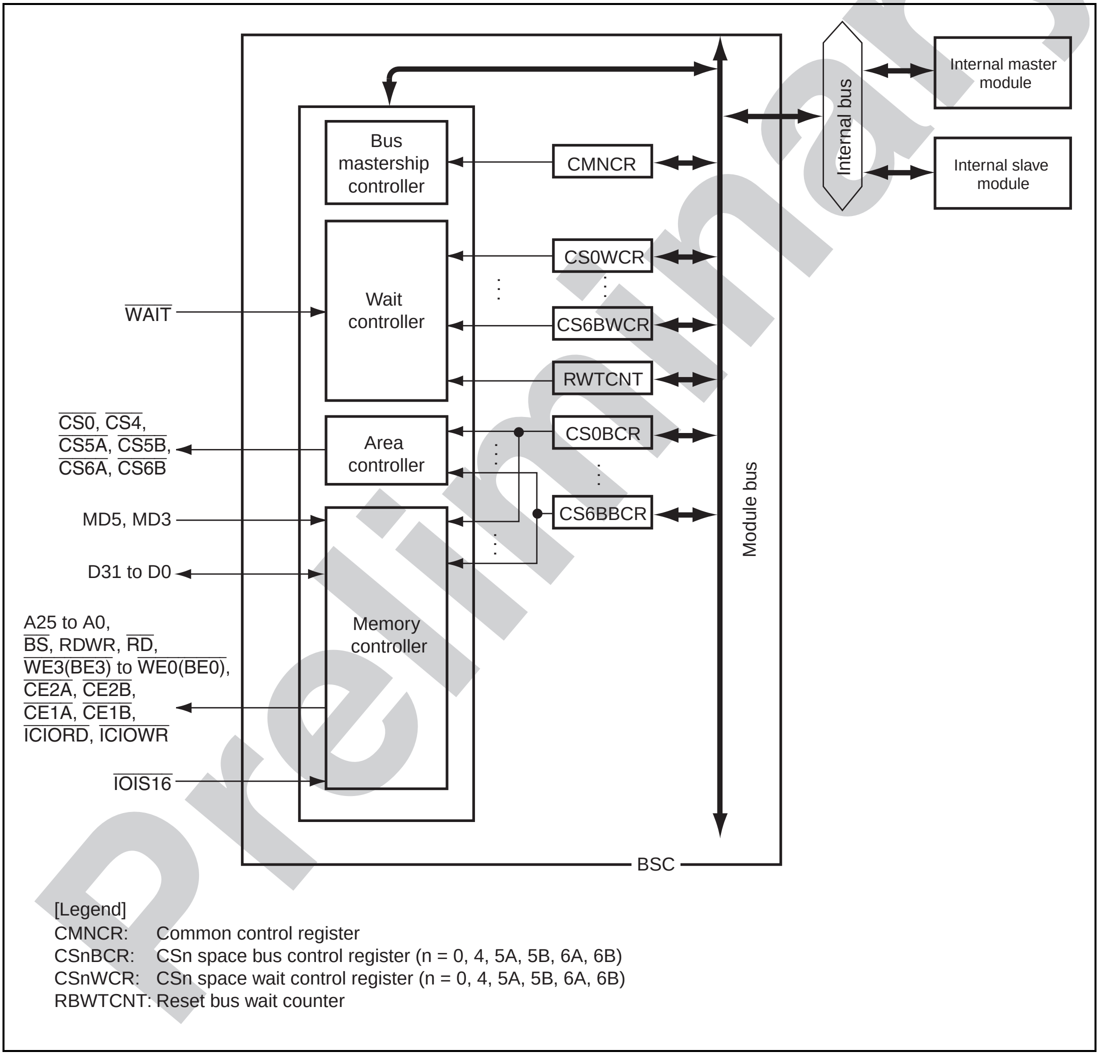


Figure 7.1 Block Diagram of BSC

7.2 Input/Output Pins

Table 7.1 lists the BSC pin configuration.

Table 7.1 Pin Configuration

Name	I/O	Description
A25 to A0	Output	Address output
D31 to D0	I/O	Data bus
$\overline{\text{BS}}$	Output	Signal to indicate the start of bus cycles Asserted when normal space, burst ROM (clock asynchronous), or PCMCIA is accessed.
$\overline{\text{CS0}}$, $\overline{\text{CS4}}$	Output	Chip select
$\overline{\text{CS5A}}$/$\overline{\text{CE2A}}$	Output	Chip select Activated only when address map 1 is selected Correspond to PCMCIA card select signals D15 to D8 when PCMCIA is used
$\overline{\text{CS5B}}$/$\overline{\text{CE1A}}$	Output	Chip select Correspond to PCMCIA card select signals D7 to D0 when PCMCIA is used
$\overline{\text{CS6A}}$/$\overline{\text{CE2B}}$	Output	Chip select Activated only when address map 1 is selected Correspond to PCMCIA card select signals D15 to D8 when PCMCIA is used
$\overline{\text{CS6B}}$/$\overline{\text{CE1B}}$	Output	Chip select Correspond to PCMCIA card select signals D7 to D0 when PCMCIA is used
RDWR	Output	Read/write signal Connected to the $\overline{\text{WE}}$ pin when SRAM with byte selection is connected
$\overline{\text{RD}}$	Output	Read pulse signal (read data output enable signal) Strobe signal to indicate memory read cycles when PCMCIA is used
$\overline{\text{WE3(BE3)}}$/ $\overline{\text{ICIOWR}}$	Output	Byte write indication signal corresponding to D31 to D24 Connected to the byte select pin when SRAM with byte selection is connected Strobe signal to indicate the I/O write when PCMCIA is used

Name	I/O	Description
$\overline{\text{WE2(BE2)}}$/ $\overline{\text{ICIORD}}$	Output	Byte write indication signal corresponding to D23 to D16 Connected to the byte select pin when SRAM with byte selection is connected Strobe signal to indicate the I/O read when PCMCIA is used
$\overline{\text{WE1(BE1)}}$/ $\overline{\text{WE}}$	Output	Byte write indication signal corresponding to D15 to D8 Connected to the byte select pin when SRAM with byte selection is connected Strobe signal to indicate the memory write cycles when PCMCIA is used
$\overline{\text{WE0(BE0)}}$	Output	Byte write indication signal corresponding to D7 to D0 Connected to the byte select pin when SRAM with byte selection is connected
$\overline{\text{IOIS16}}$	Input	Signal to indicate the 16-bit I/O of PCMCIA Enabled only in little endian mode. In big endian mode, drive this pin low.
$\overline{\text{WAIT}}$	Input	External wait input
MD5, MD3	Input	MD5: Data alignment (big/little endian selectable) MD3: Bus width of area 0 (16/32 bits)

7.3 Area Overview

7.3.1 Area Division

In the architecture, this LSI has 32-bit virtual address spaces. The cache access method that is classified into P0 to P4 spaces by the upper three bits is shown. For details, see section 7, Memory Management Unit (MMU), in the SH7723 Hardware Manual. The remaining 29 bits are used for division of the space into ten areas (address map 1) or eight areas (address map 2) according to the setting of the MAP bit in CMNCR. The BSC performs control for this 29-bit space.

As listed in tables 7.2 and 7.3, this LSI can connect eight or six physical areas to each type of memory, and it outputs chip select signals ($\overline{\text{CS0}}$, $\overline{\text{HPCS}}$, $\overline{\text{CS4}}$, $\overline{\text{CS5A}}$, $\overline{\text{CS5B}}$, $\overline{\text{CS6A}}$, and $\overline{\text{CS6B}}$) for each of them. $\overline{\text{HPCS}}$ is a control signal of DRAM area used for DDR-SDRAM exclusively (areas 2 and 3) and controls 128-Mbyte spaces by a chip select.

The relation between virtual address spaces and physical address spaces is shown in figure 7.2.

7.3.2 Shadow Area

Each area in physical address spaces is decoded by physical addresses A28 to A25. Address bits 31 to 29 are ignored. This means that the range of area 0 addresses, for example, is H'00000000 to H'03FFFFFF, and its corresponding shadow space is the address space obtained by adding to it H'2000 0000 × n (n = 1 to 6).

The address range for area 7 is H'1C000000 to H'1FFFFFFF. The address space H'1C000000 + H'20000000 × n to H'1FFFFFFF + H'20000000 × n (n = 0 to 6), including the addresses corresponding to the area 7 shadow space, is reserved, so do not use it.

Area P4 (H'E0000000 to H'FFFFFFFF) is an I/O area and is assigned for internal register addresses. Area P4 does not become a shadow space.

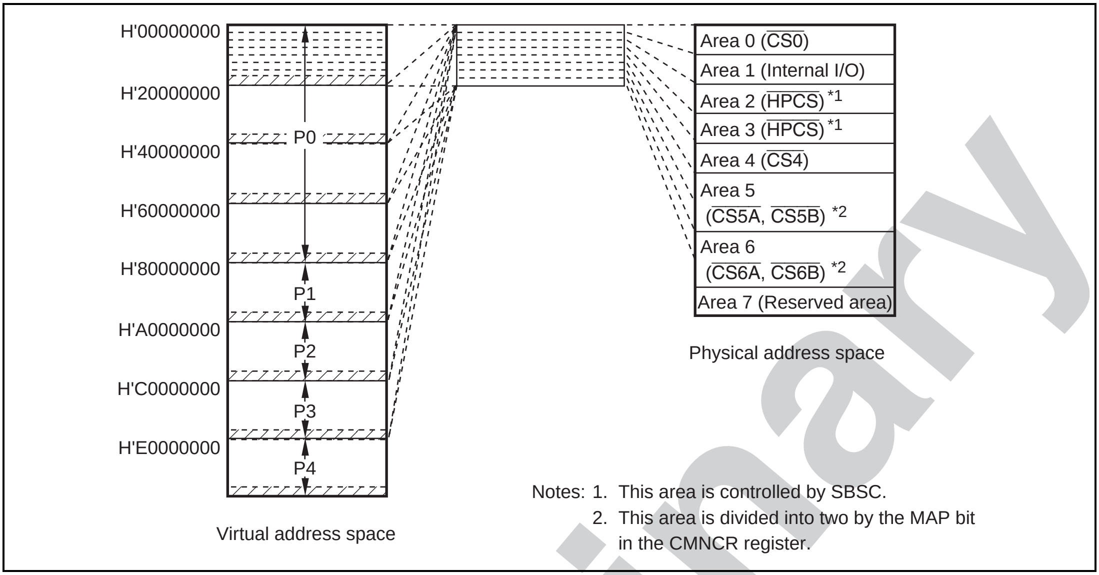


Figure 7.2 Address Space

7.3.3 Address Map

The external address space has a capacity of 384 Mbytes and is used divided into eight partial spaces (address map 1) or six partial spaces (address map 2). The type of memory to be connected and the data bus width are specified in each partial space. The address map for the external address space is listed in tables 7.2 and 7.3.

Table 7.2 Address Map 1 (CMNCR.MAP = 0)

Address	Area	Chip select	Memory to be Connected	Capacity
H'00000000 to H'03FFFFFF	Area 0	$\overline{\text{CS0}}$	Normal memory Burst ROM (asynchronous) SRAM with byte selection	64 Mbytes
H'04000000 to H'07FFFFFF	Area 1	—	Internal I/O register area*2	64 Mbytes
H'08000000 to H'0FFFFFFF	DRAM area (areas 2 and 3)	$\overline{\text{HPCS}}$	DDR1-SDRAM*3	128 Mbytes
H'10000000 to H'13FFFFFF	Area 4	$\overline{\text{CS4}}$	Normal memory SRAM with byte selection Burst ROM (asynchronous)	64 Mbytes
H'14000000 to H'15FFFFFF	Area 5A	$\overline{\text{CS5A}}$	Normal memory	32 Mbytes
H'16000000 to H'17FFFFFF	Area 5B	$\overline{\text{CS5B}}$	Normal memory SRAM with byte selection	32 Mbytes
H'18000000 to H'19FFFFFF	Area 6A	$\overline{\text{CS6A}}$	Normal memory	32 Mbytes
H'1A000000 to H'1BFFFFFF	Area 6B	$\overline{\text{CS6B}}$	Normal memory SRAM with byte selection	32 Mbytes
H'1C000000 to H'1FFFFFFF	Area 7	—	Reserved area*1	64 Mbytes

Notes: 1. Do not access the reserved area. If the reserved area is accessed, correct operation cannot be guaranteed.
2. Set the top three bits of the address of the internal I/O register to B'101 for allocation in area P2.
3. DRAM area is controlled by the SBSC.

Table 7.3 Address Map 2 (CMNCR.MAP = 1)

Address	Area	Chip select	Memory to be Connected	Capacity
H'00000000 to H'03FFFFFF	Area 0	$\overline{\text{CS0}}$	Normal memory Burst ROM (asynchronous)	64 Mbytes
H'04000000 to H'07FFFFFF	Area 1	—	Internal I/O register area*3	64 Mbytes
H'08000000 to H'0FFFFFFF	DRAM area (areas 2 and 3)	$\overline{\text{HPCS}}$	DDR1-SDRAM*4	128 Mbytes
H'10000000 to H'13FFFFFF	Area 4	$\overline{\text{CS4}}$	Normal memory SRAM with byte selection Burst ROM (asynchronous)	64 Mbytes
H'14000000 to H'17FFFFFF	Area 5*2	$\overline{\text{CS5B}}$	Normal memory SRAM with byte selection PCMCIA	64 Mbytes
H'18000000 to H'1BFFFFFF	Area 6*2	$\overline{\text{CS6B}}$	Normal memory SRAM with byte selection PCMCIA	64 Mbytes
H'1C000000 to H'1FFFFFFF	Area 7	—	Reserved area*1	64 Mbytes

Notes: 1. Do not access the reserved area. If the reserved area is accessed, correct operation cannot be guaranteed.

2. For area 5, CS5BBCR and CS5BWCR are valid.
   For area 6, CS6BBCR and CS6BWCR are valid.

3. Set the top three bits of the address of the internal I/O register to B'101 for allocation in area P2.

4. Area 3 and area 2 are controlled by the SBSC.

7.3.4 Memory Bus Width

The memory bus width of this LSI can be specified for each address space. In area 0, the bus width of 16 or 32 bits is selected by the external pin (MD3) at a power-on reset. In other areas except area 0 and DRAM area, the bus width is specified by the register. The memory type of area 0 at a power-on reset is normal space.

Table 7.4 Correspondence between External Pin (MD3) and Bus Width

MD3	Bus Width of Area 0
0	16 bits
1	32 bits

7.3.5 Data Alignment

This LSI supports the big endian and little endian methods of data alignment. The data alignment method is specified using the external pin (MD5) at a power-on reset.

Table 7.5 Correspondence between External Pin (MD5) and Endians

MD5	Endian
0	Big endian
1	Little endian

Section 8 Bus State Controller for SDRAM (SBSC)

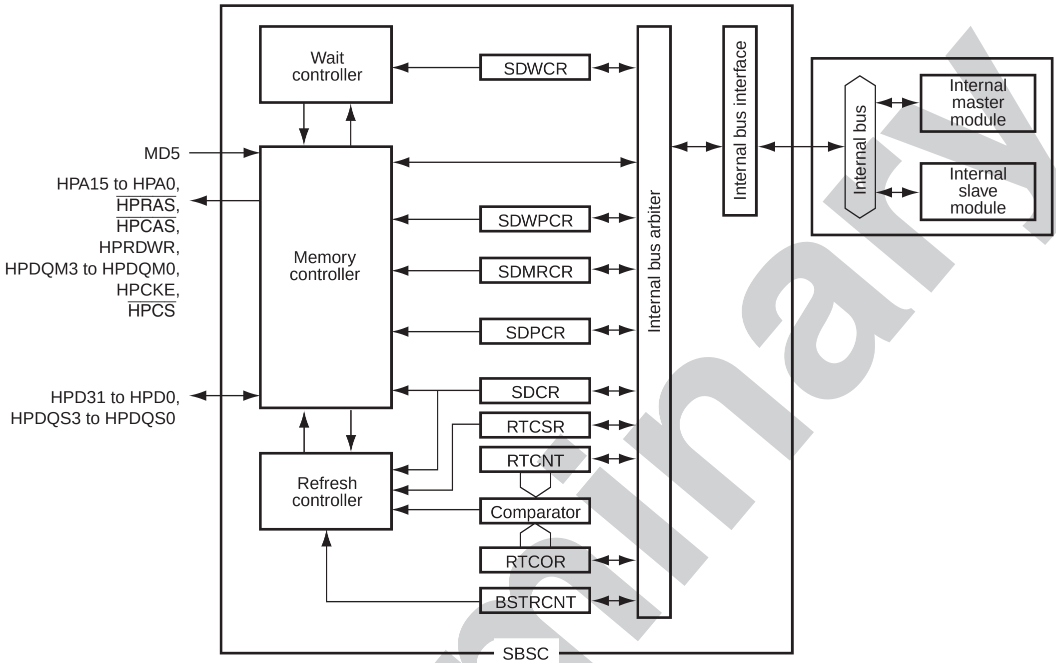
The bus state controller for SDRAM (SBSC) outputs control signals for DDR-SDRAM that is connected to the external address space. The SBSC functions enable this LSI to connect directly with DDR-SDRAM.

8.1 Features

The SBSC has the following features:

- DDR-SDRAM interface
  Multiplexed output for row address/column address
  Single read/write and burst read/write is selectable.
  Controllable insertion of wait cycles according to the DDR-SDRAM specifications
  High-speed access by bank-active mode
  Supports auto-refresh and self-refresh.
- External address space
  The SBSC has a maximum 128M byte of external address space.
- Data bus width
  32 bit only
- Data alignment
  Supports big endian and little endian
- Memory configuration that can be connected
  Two 128M-bit DDR-SDRAM (× 16) connected in parallel
  Two 256 M-bit DDR-SDRAM (× 16) connected in parallel
  Two 512 M-bit DDR-SDRAM (× 16) connected in parallel
- Burst length
  2 only
- CAS latency
  2 only

Figure 8.1 shows a block diagram of the SBSC.



[Legend]

SDCR:	SDRAM control register
SDWCR:	SDRAM wait control register
SDPCR:	SDRAM pin control register
SDWPCR:	SDRAM write protected area control resister
RTCSR:	Refresh timer control/status register
RTCNT:	Refresh timer counter
RTCOR:	Refresh time constant register
SDMRCR:	SDRAM mode resister setting control resister
BSTRCNT:	Burst refresh count resister

Figure 8.1 Block Diagram of SBSC

8.2 Input/Output Pins

Tables 8.1 lists the SBSC pin configurations.

Table 8.1 SBSC Pin Configuration

Name	Function	I/O	Description
HPA15 to HPA0	Address bus	Output	Address output
HPD31 to HPD0	Data bus	I/O	32-bit bidirectional bus
$\overline{\text{HPCS}}$	Chip select	Output	Chip select signal for external memory or device
HPRDWR	Read/write	Output	Read/write signal pin. Connected to the $\overline{\text{WE}}$ pin of DDR-SDRAM.
HPDQM3	UU-side data mask	Output	Byte-selection signal corresponding to D31 to D24 of DDR-SDRAM
HPDQM2	UL-side data mask	Output	Byte-selection signal corresponding to D23 to D16 of DDR-SDRAM
HPDQM1	LU-side data mask	Output	Byte-selection signal corresponding to D15 to D8 of DDR-SDRAM
HPDQM0	LL-side data mask	Output	Byte-selection signal corresponding to D7 to D0 of DDR-SDRAM
$\overline{\text{HPRAS}}$	Row address	Output	Specifies the DDR-SDRAM row address. Connected to the $\overline{\text{RAS}}$ pin of DDR-SDRAM.
$\overline{\text{HPCAS}}$	Column address	Output	Specifies the DDR-SDRAM column address. Connected to the $\overline{\text{CAS}}$ pin of DDR-SDRAM.
HPCKE	Clock enable	Output	DDR-SDRAM clock enable signal. Connected to the CKE pin of DDR-SDRAM.
HPCLK	Synchronous clock	Output	Synchronous clock output
$\overline{\text{HPCLK}}$	Synchronous clock	Output	Inverted HPCLK clock output for DDR-SDRAM
HPDQS3	Data strobe	I/O	Data strobe signal corresponding to D31 to D24 of DDR-SDRAM
HPDQS2	Data strobe	I/O	Data strobe signal corresponding to D23 to D16 of DDR-SDRAM
HPDQS1	Data strobe	I/O	Data strobe signal corresponding to D15 to D8 of DDR-SDRAM
HPDQS0	Data strobe	I/O	Data strobe signal corresponding to D7 to D0 of DDR-SDRAM
Vref	Reference	Input	Input for SSTL2

8.3 Area Overview

8.3.1 Address Map

This LSI has 384 Mbytes for the external address space. Among this space, the SBSC controls 128Mbytes of external address space only for DDR-SDRAM.

Table 8.2 Address Map

Address	Area	Memory to be connected	Capacity
H'0000 0000 to H'03FF FFFF	Area 0 (BSC)	See section 11, Bus State Controller (BSC).	64Mbytes
H'0800 0000 to H'0FFF FFFF	DRAM Area (SBSC)	DDR1-SDRAM	128Mbytes
H'1000 0000 to H'1BFF FFFF	Area 4 to 6B (BSC)	See section 11, Bus State Controller (BSC).	192Mbytes

8.3.2 Memory Bus Width

The DDR-SDRAM bus width in this LSI can be set as 32 bits only.

8.3.3 Data Alignment

This LSI supports big endian and little endian method for data alignment. The data alignment is specified by the setting of the external pin (MD5) at a power-on reset.

Table 8.3 Data Alignment specified by External Pin (MD5)

MD5	Data Alignment
0	Big endian
1	Little endian

Section 9 Direct Memory Access Controller (DMAC)

This LSI includes the direct memory access controller of two modules (DMAC0/1).

The DMAC0 and DMAC1 operate as independent bus-master, and can be used in place of the CPU to perform high-speed transfers between external devices that have DACK (transfer request acknowledge signal), external memory, on-chip memory, memory-mapped external devices, and on-chip peripheral modules.

9.1 Features

- Six channels for each module (12 channels in total)
- 4-Gbyte physical address space
- Data transfer unit is selectable: Byte, word (2 bytes), longword (4 bytes), 8 bytes, 16 bytes, and 32 bytes
- Maximum transfer count: 16,777,216 transfers
- Address mode: Dual address mode
- Transfer requests:

  External request, on-chip peripheral module request, or auto request can be selected.

  The following modules can issue an on-chip peripheral module request.

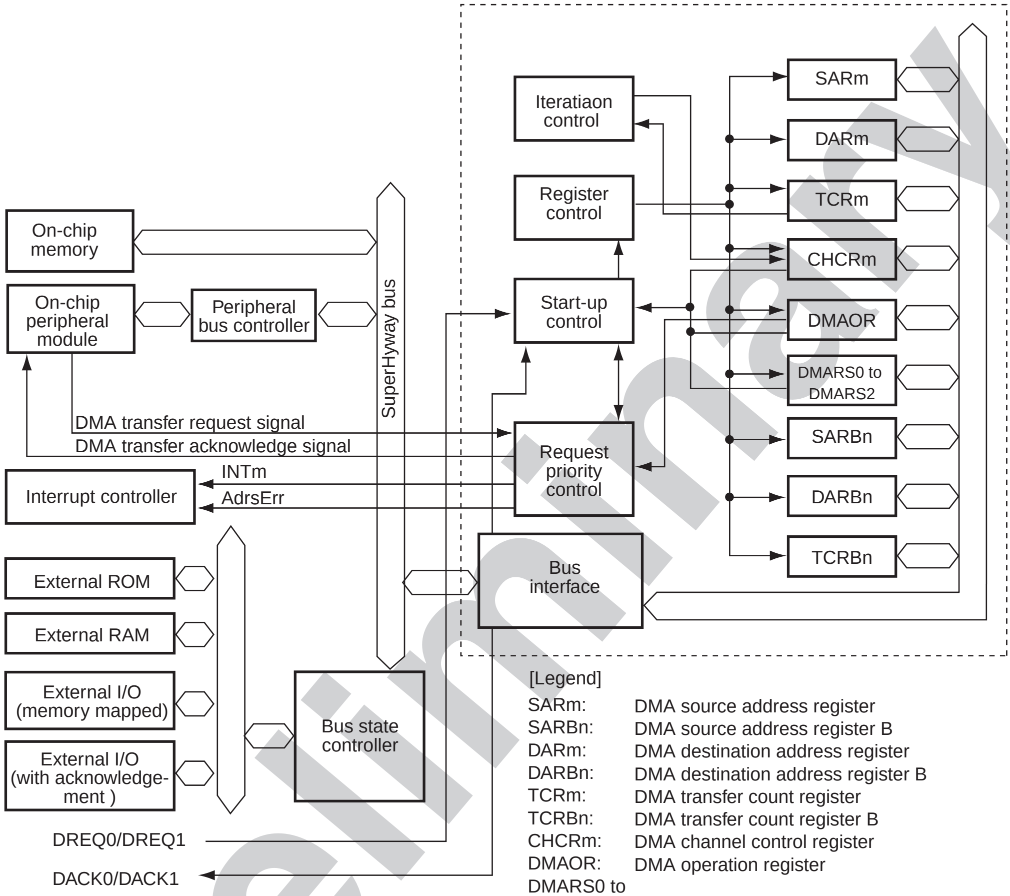
  — SCIF0 to 5, MSIOF0, MSIOF1, FLCTL, SIUA, SIUB, SDHI0, SDHI1, TSIF, IrDA, USB, and ADC
- Selectable bus modes:

  Cycle steal mode (normal mode and intermittent mode) or burst mode can be selected.
- Selectable channel priority levels:

  The channel priority levels are selectable between fixed mode and round-robin mode.
- Interrupt request: An interrupt request can be generated to the CPU after half of the transfers ended, all transfers ended, or an address error occurred.

- External request detection: There are following four types of DREQ input detection (channel 0 and channel 1 of DMAC0).
  - Low-level detection, high-level detection
  - Rising-edge detection, falling-edge detection
- Transfer request acknowledge signal:
  Active levels for DACK can be set independently (channel 0 and channel 1 of DMAC0).
- Two channels can receive an external request (channel 0 and channel 1 of DMAC0).

Figure 9.1 shows the block diagram of the DMAC.



[Legend]

SARm:	DMA source address register
SARBn:	DMA source address register B
DARm:	DMA destination address register
DARBn:	DMA destination address register B
TCRm:	DMA transfer count register
TCRBn:	DMA transfer count register B
CHCRm:	DMA channel control register
DMAOR:	DMA operation register
DMARS0 to DMARS2:	DMA extended resource selectors
INTm:	DMA transfer end/half-end interrupt request*
AdrsErr:	Address error interrupt request
m:	0, 1, 2, 3, 4, 5
n:	0, 1, 2, 3

Note: * The half-end interrupt request is available in channels 0 to 3.

Figure 9.1 Block Diagram of DMAC

9.2 Input/Output Pins

The external pins for the DMAC0 are described below. Table 9.1 lists the configuration of the pins that are connected to external bus. The DMAC0 has pins for one channel (channel 0) for external bus use. The DMAC1 doesn't have external pins.

Table 9.1 Pin Configuration

Channel	Pin Name	Function	I/O	Description
0	DREQ0	DMA transfer request	Input	DMA transfer request input from external device to channel 0 of DMAC0
	DACK0	DMA transfer request acknowledge	Output	DMA transfer request acknowledge output from channel 0 of DMAC0 to external device
1	DREQ1	DMA transfer request	Input	DMA transfer request input from external device to channel 1 of DMAC0
	DACK1	DMA transfer request acknowledge	Output	DMA transfer request acknowledge output from channel 1 of DMAC0 to external device

Section 10 Clock Pulse Generator (CPG)

Note: This section contains references to the SH7723 Hardware Manual. The contents of the SH7723 Hardware Manual will be disclosed upon acceptance of a confidentiality agreement. For details, please contact a Renesas Technology sales representative.

The clock pulse generator generates the clocks used in this LSI and consists of a PLL circuit, a DLL circuit, dividers, and the associated control circuit.

10.1 Features

- Generation of the various clocks for LSI internal operations

  CPU clock (Iϕ): Operating clock for the CPU core

  U clock (Uϕ): Operating clock for the CPU core

  SH clock (SHϕ): Operating clock for the SuperHyway bus

  Bus clock (Bϕ): Operating clock for the BSC. Operating clock for peripheral modules on the SuperHyway bus

  SDRAM clock (B3ϕ): Operating clock for the SBSC

  Peripheral clock (Pϕ): Operating clock for peripheral modules on the HPB (peripheral bus).
- Generation of clocks for external interfaces

  Bus clock (CKO): Clock for the BSC bus interface (same as Bϕ)

  SDRAM clock (HPCLK): Clock for the SDRAM interface (same as B3ϕ)

  Video clock (VIO_CKO): Clock output for cameras

  SIU clock A (SIUCKA): Clock for the SIU external interface

  SIU clock B (SIUCKB): Clock for the SIU external interface

  IrDA clock (IrDACK): IrDA clock output
- Frequency-change function

  The frequency of each clock can be changed independently by using the PLL circuit, DLL circuit, or dividers within the CPG. Frequencies are changed under software control by register settings.
- Clock mode

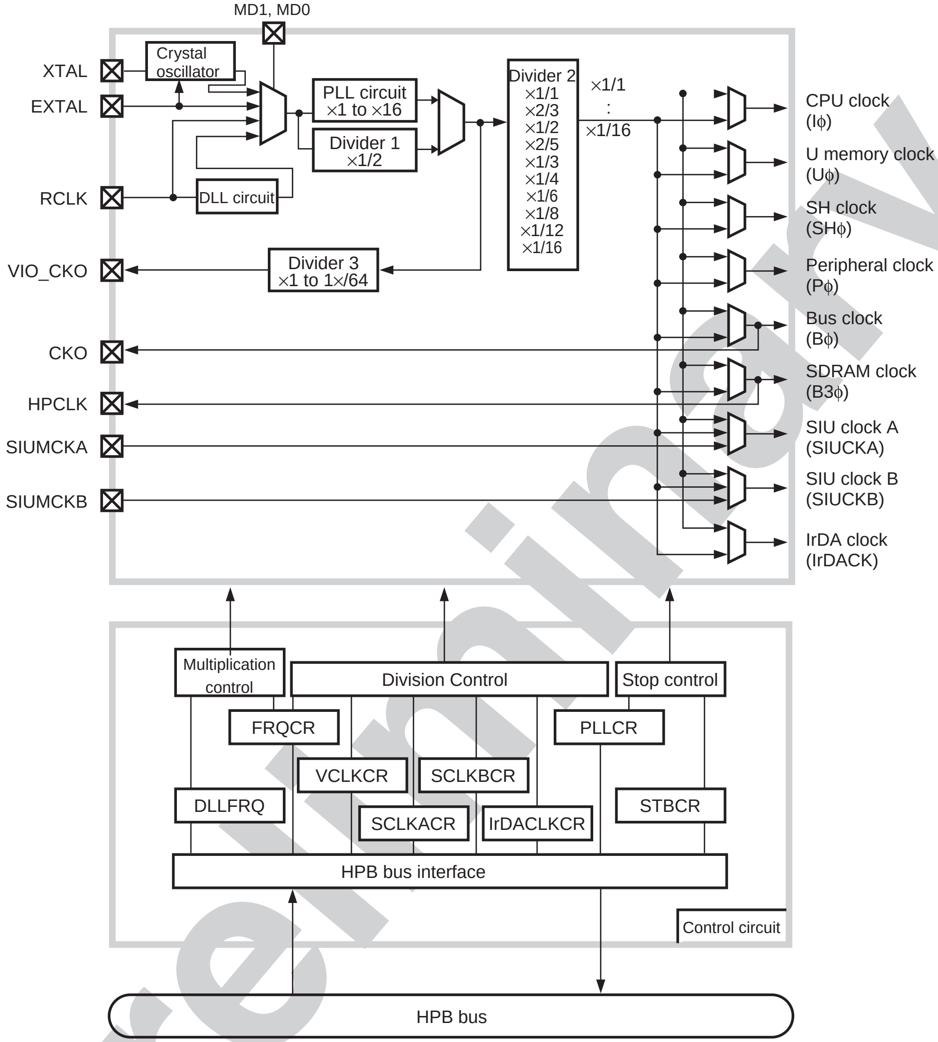
  The clock mode pin setting selects external inputs (EXTAL or RCLK) or crystal oscillator as the clock source. In addition, the PLL and DLL can be turned on or off by the clock mode pin setting after a power-on reset.

- Power-down mode control

  The clocks are stopped in sleep mode, software standby mode, and U-standby mode; clocks for specific modules can be stopped by using the module standby function. For details, see section 15, Reset and Power-Down Modes, in the SH7723 Hardware Manual.

10.2 Block Diagram

A block diagram of the CPG is shown in figure 10.1.



[Legend]

FRQCR	:	Frequency control register
PLLCR	:	PLL control register
DLLFRQ	:	DLL multiplication register
STBCR	:	Standby control register (For details, see section 15, Reset and Power-Down Modes, in the SH7723 Hardware Manual.)
VCLKCR	:	Video clock frequency control register
SCLKACR	:	SIU clock A frequency control register
SCLKBCR	:	SIU clock B frequency control register
IrDACLKCR	:	IrDA clock frequency control register

Figure 10.1 Block Diagram of CPG

The CPG blocks function as follows:

(1) DLL Circuit

The DLL circuit multiples the clock frequency (32.768 kHz) input from the RCLK pin. This circuit is only enabled in clock mode 3. The multiplication rate is set in the DLL multiplication register (DLLFRQ). The initial value of the multiplication rate is 1017 and the generated clock is at 32.768 kHz × 1017 = 33.33 MHz.

The output clock frequency for the DLL circuit is in the range from 20 to 33.4 MHz/

(2) PLL Circuit

The PLL circuit multiples, by factors from 6 to 16, the frequency of the clock input from the EXTAL pin or of the multiplied clock signal produced by the DLL circuit. The multiplication rate is set in the frequency control register (FRQCR). The PLL circuit is turned on or off by the settings of the clock mode pins or the PLL control register (PLLCR).

The input clock frequency for the PLL circuit is in the range from 15 to 50 MHz. The output clock frequency is in the range from 180 to 400 MHz.

(3) Divider 1

Divider 1 halves the frequency of the clock input from the EXTAL pin or of the multiplied clock produced by the DLL circuit. When the PLL circuit is turned off, the clock output from divider 1 is input to dividers 2 and 3.

(4) Divider 2

Divider 2 divides the frequency of the clock output from the PLL circuit or divider 1 and generates the operating clocks. The division ratio is set in the relevant frequency control register.

(5) Divider 3

Divider 3 generates the video clock (VIO_CKO) by dividing the frequency of the clock output by the PLL circuit or divider 1. The division ratio is set by VCLKCR.

(6) Control Circuit

The control circuit controls the clock frequency according to the settings of the MD0 and MD1 pins and the frequency control registers.

10.3 Input/Output Pins

Table 10.1 lists the CPG pin configuration.

Table 10.1 Pin Configuration and Functions of CPG

Pin Name	Function	I/O	Description
MD0	Clock mode control pins	Input	Sets the clock operating mode.
MD1		Input	Sets the clock operating mode.
MD2		Input	Reserved*[1]
EXTAL	Clock pins	Input	Connects the crystal oscillator. Or used as an external clock input pin.
XTAL		Output	Connects the crystal oscillator.
RCLK		Input	Inputs the RTC clock (32.768 kHz).*[2]
SIUMCKA		Input	Clock input for SIU interface
SIUMCKB		Input	Clock input for SIU interface
CKO	Bus clock output pin	Output	Used as a BSC interface clock output pin.
HPCLK	SDRAM clock output pin	Output	Used as a SDRAM interface clock output pin.
VIO_CKO	Video clock	Output	Used as a clock output pin for cameras.

Notes: 1. Always input low level to the MD2 pin.
2. Always input RCLK in this LSI even when the DLL circuit is not used.

Section 11 Reset and Power-Down Modes

This LSI supports U-standby mode, in which low power consumption is achieved by turning off the internal power-supply to part of the chip. This LSI also supports sleep mode, software standby mode, and module standby function, in which clock supply to the LSI is controlled optimally.

11.1 Features

- Supports a variety of power-down modes, i.e. sleep, software standby, module standby, and U-standby modes.
- In U-standby mode, the RWDT, CMT, KEYSC, and RTC that operate on RCLK are operational.

11.1.1 Division of Power-Supply Areas

To realize power-down modes, this LSI is divided into the following three power-supply areas.

- Core area

  This area is operated by the V_{DD} power supply and encompasses all areas other than the following two. Power consumption on standby is greatly reduced in U-standby mode by turning off the power to this area.
- Sub area

  This area is operated by the V_{DD} power supply and encompasses the RWDT, CMT, KEYSC, and RTC.
- I/O area

  This area is operated by the V_{CC} power supply and encompasses the I/O buffer.

11.1.2 Types of Resets and Power-Down Modes

This LSI has the following types of power-down modes. Table 11.1 shows the state in each mode and methods for making transitions and canceling each mode.

- Sleep mode: Supply of the clock to the CPU core is stopped.
- Software standby mode: Supply of the clock is stopped throughout the LSI.
- Module standby function: The operation of modules that are not in use can be stopped under software control.
- U-standby mode: The supply of power to core areas is stopped. (A power is supplied to I/O area and sub area.)

Table 11.1 States of Resets and Power-Down Modes

		State						
Power-Down Mode	**Transition Conditions**	**CPG**	**CPU Core**	**CPU Registers**	**On-Chip Memory**	**On-Chip Peripheral Modules***[1]	**External SDRAM**	**Canceling Method**
Sleep mode	Execute the SLEEP instruction with STBY = 0 and USTBY = 0 in STBCR.	Operating	Stopped	Retained	Stopped (contents retained)	Operating	Auto-refreshing	• Interrupt • Power-on reset • System reset
Software standby mode	Execute the SLEEP instruction with STBY = 1 and USTBY = 0 in STBCR.	Stopped	Stopped	Retained	Stopped (contents retained)	Stopped*[2]	Self-refreshing	• IRQ, NMI, CMT, KEYSC, RTC • Power-on reset • System reset
Module standby function	Set the MSTP bit of the respective module to 1 in MSTPCR.	Operating	Operating or stopped	Retained	Specified module stopped (contents retained)	Specified module stopped	Auto-refreshing	• Clear the MSTP bit to 0.

		State						
Power-Down Mode	**Transition Conditions**	**CPG**	**CPU Core**	**CPU Registers**	**On-Chip Memory**	**On-Chip Peripheral Modules***[1]	**External SDRAM**	**Canceling Method**
U-standby mode	Execute the SLEEP instruction with USTBY = 1 and STBY = 0 in STBCR.	Stopped	Stopped	Not retained	Not retained	Stopped*[2]	Self-refreshing	• CMT, KEYSC, RTC • Power-on reset • System reset
Power-on reset	Drive the $\overline{\text{RESETP}}$ pin low.	Initial state	Initial state	Initial state	Initial state	Initial state	Initial state	—
System reset	Drive the $\overline{\text{RESETA}}$ pin low. RWDT overflows.	Initial state	Initial state	Initial state	Initial state	Initial state	Initial state	—
Manual reset	Generate an exception other than a user break while SR.BL = 1.	Retained	Initial state	Initial state	Initial state/retained*[3]	Initial state/retained*[3]	Auto-refreshing	—

Notes: 1 The on-chip peripheral modules refer to modules that are directly connected to the Super-Hyway bus or peripheral bus.

2 Modules with RCLK operation (RWDT, CMT, KEYSC, and RTC) continue to operate.

3. This depends on the module. See the sections on the individual modules.

11.2 Input/Output Pins

Table 11.2 lists the pin configuration related to resets and power-down modes.

Table 11.2 Pin Configuration

Pin Name	Function	I/O	Description
STATUS0	Processing state 0	Output	Becomes high level in various standby modes (software standby mode and U-standby mode).
$\overline{\text{RESETP}}$	Reset input pin	Input	This LSI enters the power-on reset state when this pin becomes low level.
$\overline{\text{RESETA}}$	Reset input pin	Input	This LSI enters the system reset state when this pin becomes low level.
$\overline{\text{RESETOUT}}$	Reset output signal	Output	Becomes low level while this LSI is being reset.
PDSTATUS	Power-down state signal	Output	Becomes high level when the power-supply separating region is turned off. PDSTATUS can control the supply current to the regulator.

Section 12 RCLK Watchdog Timer (RWDT)

This LSI includes the RCLK watchdog timer (RWDT).

The RWDT is a single-channel timer that uses a RTC clock as an input and can be used as a watchdog timer for the system monitoring.

This LSI can be reset by the overflow of the counter when the value of the counter has not been updated because of a system runaway.

12.1 Features

- Can be used as a watchdog timer. A system reset is generated when the counter overflows.
- Choice of eight counter input clocks.
  Eight clocks (RCLK/1 to RCLK/4096) that are obtained by dividing the RCLK.

Figures 12.1 shows block diagrams of the RWDT.

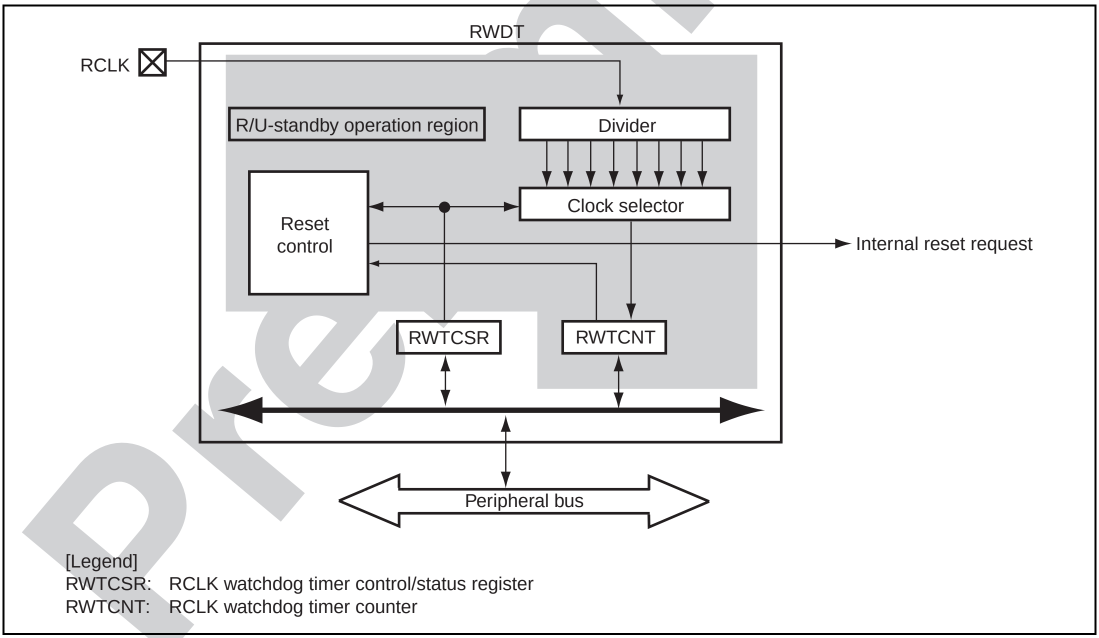


Figure 12.1 Block Diagram of RWDT

12.2 Input/Output Pins for RWDT

Table 12.1 lists the pin configuration and functions of the RWDT.

Table 12.1 RWDT Pin Configuration

Pin Name	Function	I/O	Description
RCLK	RTC clock	Input	Clock input from an external RTC (32.768 kHz)

.

Section 13 Timer Unit (TMU)

This LSI includes two three-channel 32-bit timer units (TMU).

13.1 Features

- Each channel is provided with an auto-reload 32-bit down counter
- All channels are provided with 32-bit constant registers and 32-bit down counters that can be read or written to at any time
- All channels generate interrupt requests when the 32-bit down counter underflows (H'00000000 → H'FFFFFFFF)
- Allows selection among five counter input clocks: Pϕ/4, Pϕ/16, Pϕ/64, Pϕ/256, and Pϕ/1024

Figure 13.1 shows a block diagram of the TMU.

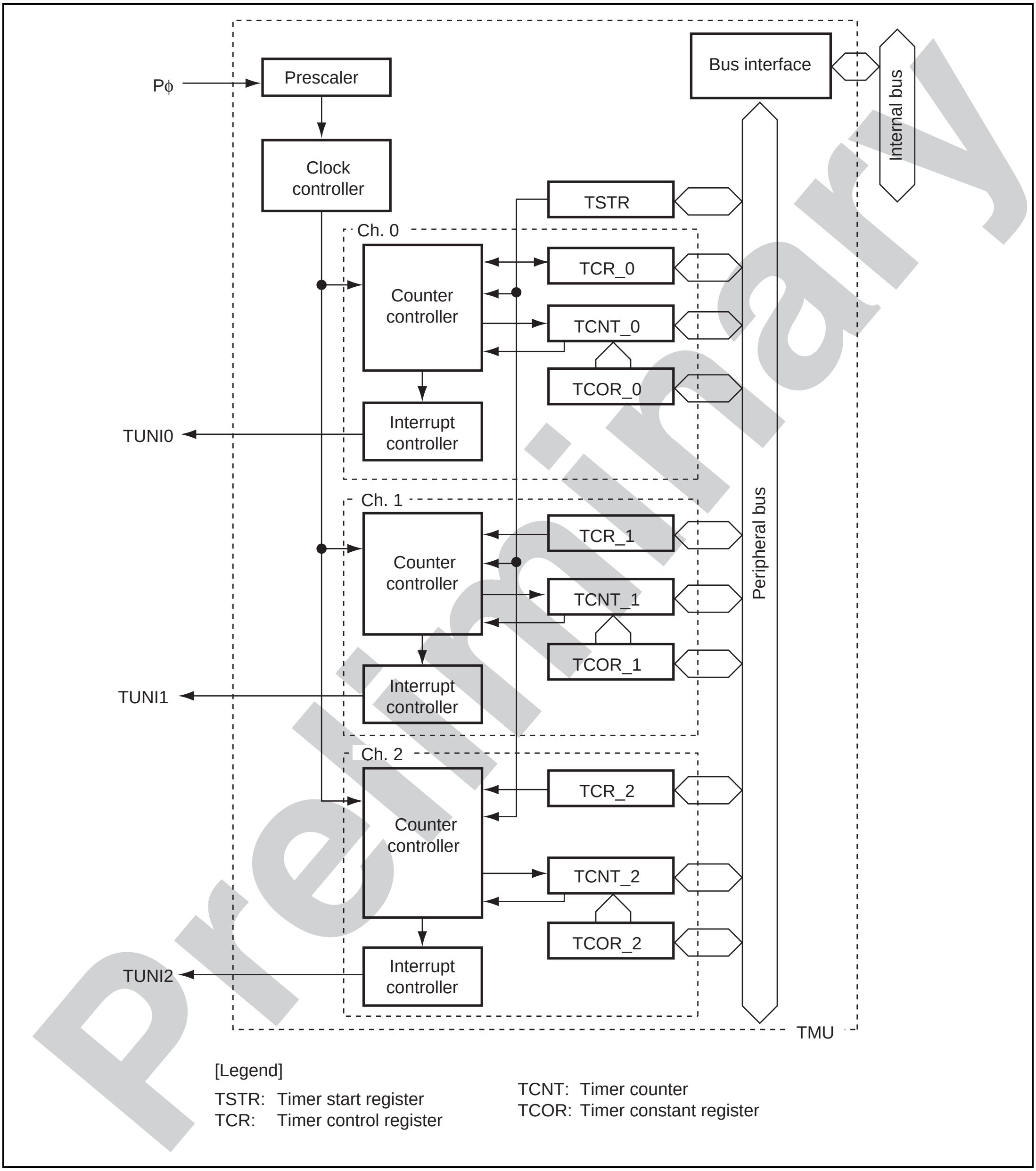


Figure 13.1 Block Diagram of TMU

Section 14 16-Bit Timer Pulse Unit (TPU)

This LSI has an on-chip 16-bit timer pulse unit (TPU) which consists of four 16-bit timer channels.

14.1 Features

- Various timer general registers

  TPU has a total of 16 timer general registers provided with four registers (TPU_TGRA to TPU_TGRD) for each channel. TPU_TGRA enables an output compare setting. TPU_TGRB, TPU_TGRC, and TPU_TGRD in each channel can be used as the timer counter clear registers. TPU_TGRC and TPU_TGRD can be used as the buffer registers.
- The following operation can be set for each channel:

  Counter clear operation: Counter clearing possible by compare match
- Buffer operation settable for each channel

  Automatic rewriting of output compare register possible
- One interrupt request

  Enabling or disabling the compare match/overflow interrupt request can be set independently for each interrupt source.
- The following output can be made from every channel.

  Waveform output at compare match: Selection of 0, 1, or toggle output

  PWM mode: Any PWM output duty cycle can be set

Table 14.1 describes the TPU functions.

Table 14.1 TPU Functions

Item		TPU: Channel 0	TPU: Channel 1	TPU: Channel 2	TPU: Channel 3
Count clock		Bϕ/1 Bϕ/4 Bϕ/16 Bϕ/64	Bϕ/1 Bϕ/4 Bϕ/16 Bϕ/64	Bϕ/1 Bϕ/4 Bϕ/16 Bϕ/64	Bϕ/1 Bϕ/4 Bϕ/16 Bϕ/64
General register		TPU_TGR0A TPU_TGR0B	TPU_TGR1A TPU_TGR1B	TPU_TGR2A TPU_TGR2B	TPU_TGR3A TPU_TGR3B
General register/ Buffer register		TPU_TGR0C TPU_TGR0D	TPU_TGR1C TPU_TGR1D	TPU_TGR2C TPU_TGR2D	TPU_TGR3C TPU_TGR3D
Output pin		TPUTO	TPUTO1	TPUTO2	TPUTO3
Counter clear function		TPU_TGR compare match	TPU_TGR compare match	TPU_TGR compare match	TPU_TGR compare match
Compare match output	0 output	O	O	O	O
	1 output	O	O	O	O
	Toggle output	O	O	O	O
PWM mode		O	O	O	O
Buffer mode		O	O	O	O
Interrupt request		5 sources • Compare match • Overflow	5 sources • Compare match • Overflow	5 sources • Compare match • Overflow	5 sources • Compare match • Overflow

14.2 Block Diagram

A block diagram of the TPU is shown in figure 14.1.

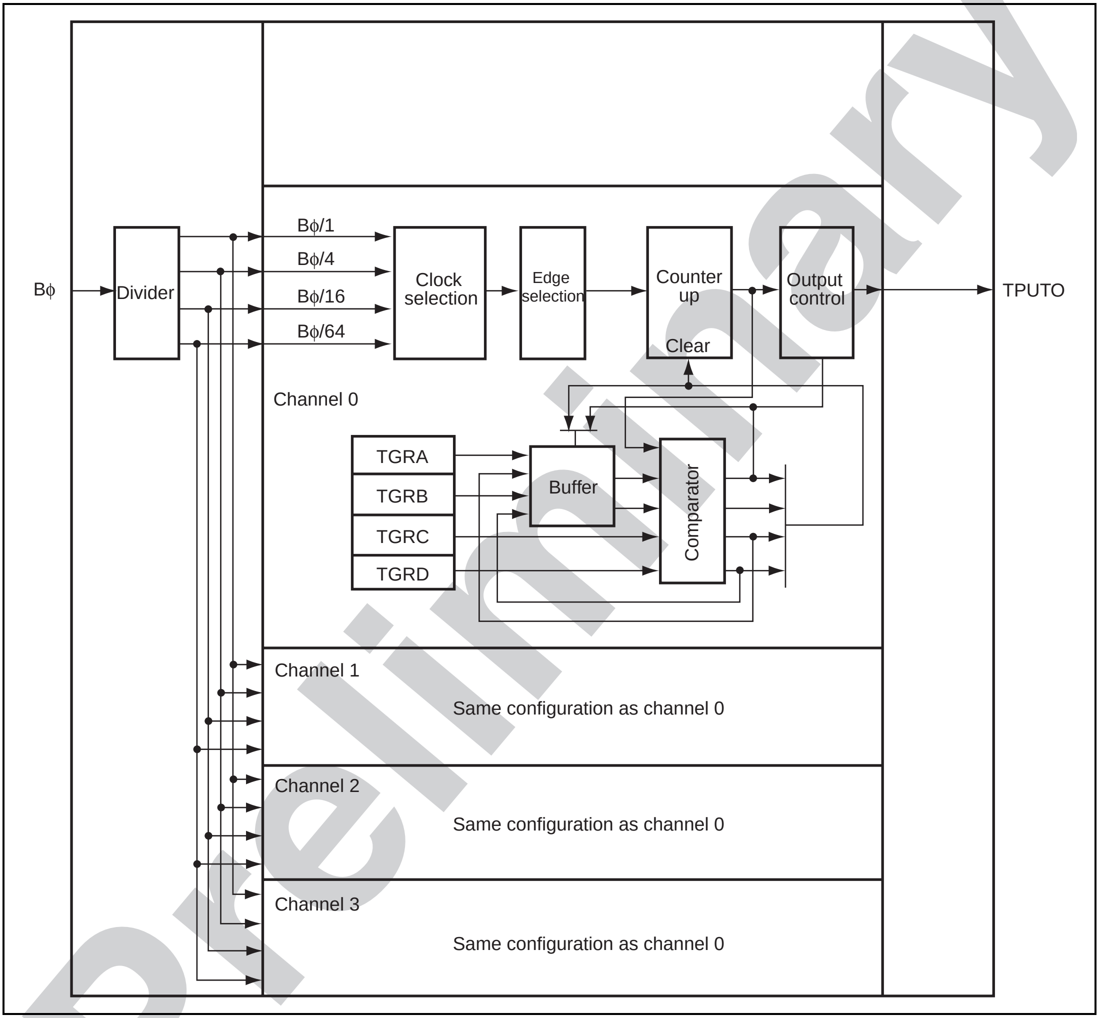


Figure 14.1 TPU Block Diagram

14.3 Input/Output Pin

Table 14.2 shows the pin configuration of the TPU.

Table 14.2 Pin Configuration

Channel	Pin Name	Function	I/O	Description
0	TPUTO0	TPU output compare match 0	Output	TPU_TGR0A output compare output/ PWM output pin
1	TPUTO1	TPU output compare match 1	Output	TPU_TGR1A output compare output/ PWM output pin
2	TPUTO2	TPU output compare match 2	Output	TPU_TGR2A output compare output/ PWM output pin
3	TPUTO3	TPU output compare match 3	Output	TPU_TGR3A output compare output/ PWM output pin

Section 15 Compare Match Timer (CMT)

This LSI includes a 32-bit compare match timer (CMT) of one channel.

15.1 Features

- 16 bits/32 bits can be selected.
- Provided with an auto-reload up counter.
- Provided with 32-bit constant registers and 32-bit up counters that can be written or read at any time.
- The CMT of this LSI can operate the counting even in U-standby mode.
- Allows selection among 3 counter input clocks:
  — External clock (RCLK) input: 1/8, 1/32, and 1/128
- One-shot operation and free-running operation are selectable.
- Allows selection of compare match or overflow for the interrupt source.
- Supports canceling of the standby state in U-standby mode.
- Module standby mode can be set.

Figure 15.1 shows a block diagram of the CMT.

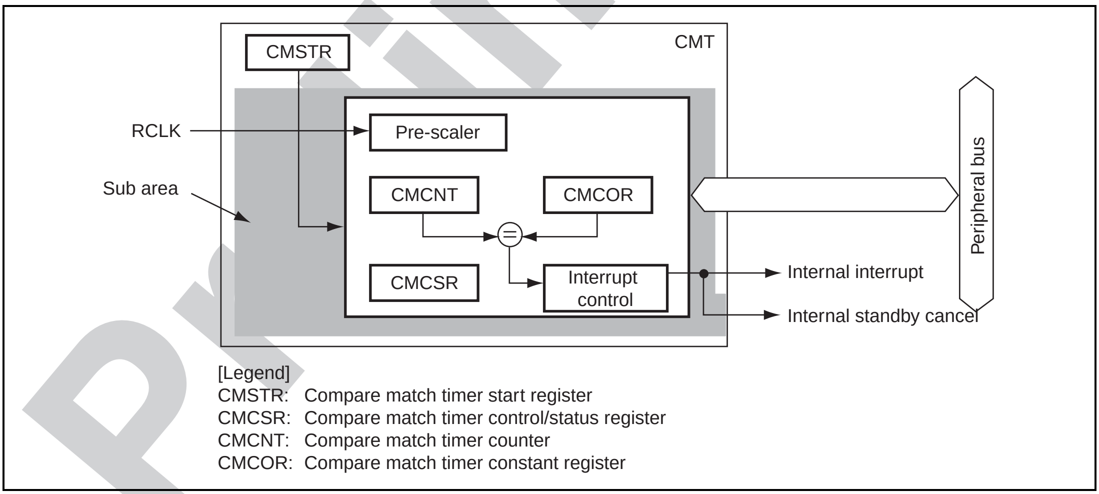


Figure 15.1 Block Diagram of CMT

Section 16 Clock-Synchronized Serial Interface with FIFO (MSIOF)

This LSI includes two-channel of clock-synchronized serial I/O module with FIFO (MSIOF0, MSIOF1).

16.1 Features

- FIFO capacity: 32 bits × 64 stages for transmission and 32 bits × 64 stages for reception
- MSB first or LSB first selectable for data transmission and reception
- Synchronization by frame synchronization pulse, level, or left/right channel switch
- Supports both master and slave modes
- Independent clock and synchronization signals for transmission and reception (common clock and synchronization signals are also selectable)
- Supports multiple-channel communication
  - Transfers multiple groups or words of data in one frame.
  - The word data size for each group can be selected from eight to 32 bits
  - Up to 256 words can be transferred in each group when one or two groups are used, or up to 16 words can be transferred in each group when three or four groups are used.
- Interrupts: One type in each channel
- Serial clock

  The internal clock (Bϕ) or external pin input (MSIOF0_MCK/MSIOF1_MCK) can be selected as the clock source.
- DMA transfer

  Supports DMA transfer by a transfer request for transmission and reception
- Serial format

  Supports serial format such as IIS, SPI (both master and slave modes), and μWIRE.

Figure 16.1 shows a block diagram of the MSIOF.

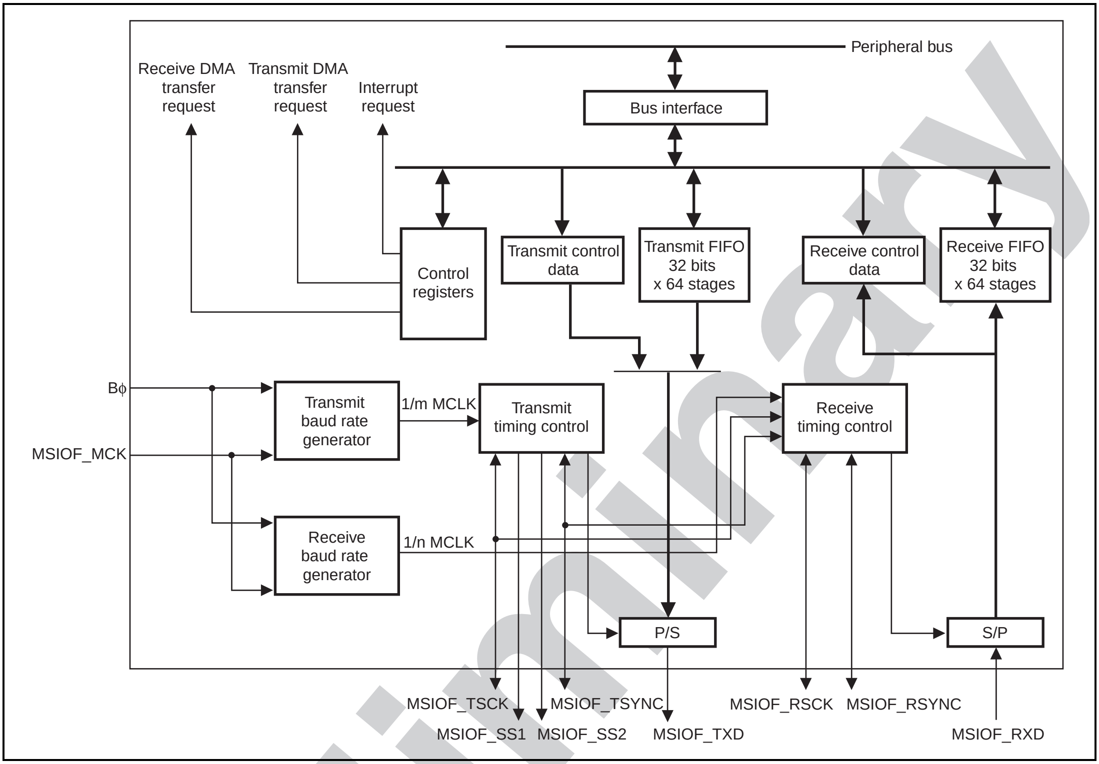


Figure 16.1 Block Diagram of MSIOF

16.2 Input/Output Pins

The pin configuration in this module is shown in table 16.1.

Table 16.1 Pin Configuration

Pin Name	Abbreviation*	I/O	Function
MSIOF0_MCK MSIOF1_MCK	MSIOFMCK	Input	Master clock input
MSIOF0_TSCK MSIOF1_TSCK	MSIOFTSCK (SCK)	I/O	Serial clock for transmission Works as SCK when a common clock is used for transmission and reception.
MSIOF0_TSYNC MSIOF1_TSYNC	MSIOFTSYNC ($\overline{\text{SS0}}$)	I/O	Frame synchronization signal channel 0 for transmission Works as SYNC when a common synchronization signal is used for transmission and reception.
MSIOF0_SS1 MSIOF1_SS1	MSIOFSS1 ($\overline{\text{SS1}}$)	Output	Frame synchronization signal channel 1 for transmission Only the slave device can select this signal.
MSIOF0_SS2 MSIOF1_SS2	MSIOFSS2 ($\overline{\text{SS2}}$)	Output	Frame synchronization signal channel 2 for transmission Only the slave device can select this signal.
MSIOF0_RSCK MSIOF1_RSCK	MSIOFRSCK	I/O	Serial clock for reception
MSIOF0_RSYNC MSIOF1_RSYNC	MSIOFRSYNC	I/O	Frame synchronization signal for reception
MSIOF0_TXD MSIOF1_TXD	MSIOFTXD (MOSI/MISO)	Output	Transmit data
MSIOF0_RXD MSIOF1_RXD	MSIOFRXD (MISO/MOSI)	Input	Receive data

Note: * In SPI mode, the pins are called SCK, $\overline{\text{SS0}}$, $\overline{\text{SS1}}$, $\overline{\text{SS2}}$, MOSI, and MISO.

Section 17 Serial Communication Interface with FIFO (SCIF)

This LSI has a three-channel serial communication interface with FIFO (SCIF) that supports both asynchronous and clock synchronous serial communication. It also has 16-stage FIFO registers for both transmission and reception independently for each channel that enable this LSI to perform efficient high-speed continuous communication.

17.1 Features

- Asynchronous serial communication:
  - Serial data communication is performed by start-stop in character units. The SCIF can communicate with a universal asynchronous receiver/transmitter (UART), an asynchronous communication interface adapter (ACIA), or any other communications chip that employs a standard asynchronous serial system. There are eight selectable serial data communication formats.
  - Data length: 7 or 8 bits
  - Stop bit length: 1 or 2 bits
  - Parity: Even, odd, or none-
  - Receive error detection: Parity, framing, and overrun errors
  - Break detection: Break is detected when a framing error is followed by at least one frame at the space 0 level (low level).
- Clock synchronous serial communication:
  - Serial data communication is synchronized with a clock signal. The SCIF can communicate with other chips having a clock synchronous communication function. There is one serial data communication format.
  - Data length: 8 bits
  - Receive error detection: Overrun errors
- Full duplex communication: The transmitting and receiving sections are independent, so the SCIF can transmit and receive simultaneously. Both sections use 16-stage FIFO buffering, so high-speed continuous data transfer is possible in both the transmit and receive directions.
- On-chip baud rate generator with selectable bit rates

- Internal or external transmit/receive clock source: From either baud rate generator (internal) or SCK pin (external)
- Four types of interrupts: Transmit-FIFO-data-empty interrupt, break interrupt, receive-FIFO-data-full interrupt, and receive-error interrupts are requested independently on each channel.
- When the transmit FIFO is empty or the receive FIFO contains any received data, the DMA controller (DMAC) can be activated to perform data transfer by generating a DMA transfer request.
- When the SCIF is not in use, it can be stopped by halting the clock supplied to it, saving power.
- The quantity of data in the transmit and receive FIFO data registers and the number of receive errors of the received data in the receive FIFO data register can be ascertained.
- A time-out error (DR) can be detected when receiving in asynchronous mode.

Figure 17.1 shows a block diagram of the SCIF.

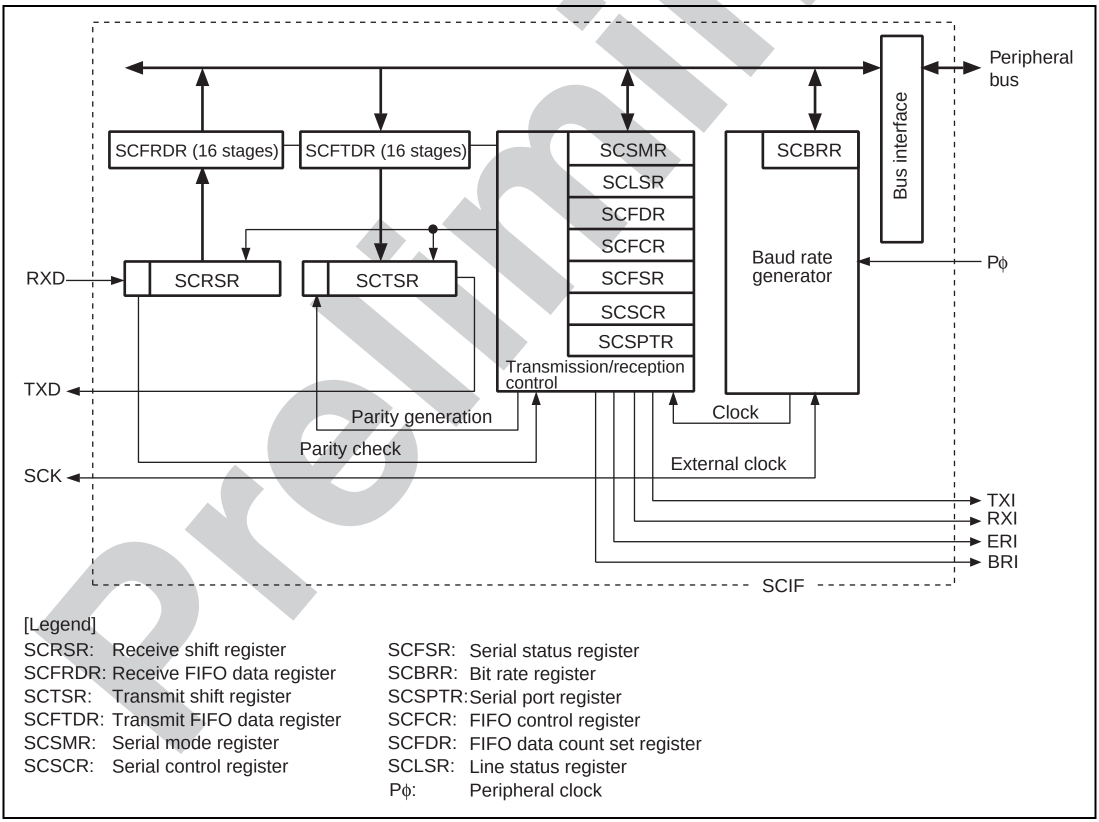


Figure 17.1 Block Diagram of SCIF

17.2 Input/Output Pins

Table 17.1 shows the pin configuration of the SCIF.

Table 17.1 Pin Configuration

Channel	Pin Name	Function	I/O	Description
0	SCIF0_TXD	Transmit data	Output	Transmit data pin
	SCIF0_RXD	Received data	Input	Received data pin
	SCIF0_SCK	Serial clock	I/O	Clock I/O pin
1	SCIF1_TXD	Transmit data	Output	Transmit data pin
	SCIF1_RXD	Received data	Input	Received data pin
	SCIF1_SCK	Serial clock	I/O	Clock I/O pin
2	SCIF2_TXD	Transmit data	Output	Transmit data pin
	SCIF2_RXD	Received data	Input	Received data pin
	SCIF2_SCK	Serial clock	I/O	Clock I/O pin

Note: In the following descriptions, channel numbers in pin names and signal names are omitted and TXD, RXD, and SCK are used as generic terms.

Section 18 Serial Communication Interface with FIFO A (SCIFA)

This LSI has three channels (channel 3 to channel 5) of serial communication interface (SCIFA) that includes FIFO buffers. The SCIFA can perform asynchronous and synchronous serial communications. It has 64-stage FIFO registers for both transmission and reception, which allow efficient high-speed continuous communication.

18.1 Features

- Asynchronous or synchronous mode can be selected for serial communication mode.
- On-chip baud rate generator with selectable bit rates
- Internal or external transmit/receive clock source: From either baud rate generator (internal) or SCK pin (external)
- Six types of interrupts (asynchronous mode):

  Transmit-data-stop, transmit-FIFO-data-empty, receive-FIFO-data-full, receive-error (framing error/parity error), break-receive, and receive-data-ready interrupts. A common interrupt vector is assigned to each interrupt source.
- Two types of interrupts (synchronous mode)
- The direct memory access controller (DMAC) can be activated to transfer data in the event of transmit-FIFO-data-empty, transmit-data-stop, or receive-FIFO-data-full. Note that the transfer request to the DMAC is common to transmit-FIFO-data-empty and transmit-data-stop.
- On-chip modem control functions ($\overline{\text{CTS}}$ and $\overline{\text{RTS}}$)
- Transmit data stop function is available
- While the SCIFA is not used, it can be stopped by stopping the clock for it to reduce power consumption.
- The number of data bytes in the transmit and receive FIFO registers and the number of receive errors of the received data in the receive FIFO register can be known.
- Full-duplex communication capability

  The transmitter and receiver are independent units, enabling transmission and reception to be performed simultaneously.

  The transmitter and receiver both have a 64-stage FIFO buffer structure, enabling fast and continuous serial data transmission and reception.

- Asynchronous mode:

  Serial data communications are performed by start-stop in character units. The SCI can communicate with a universal asynchronous receiver/transmitter (UART), an asynchronous communication interface adapter (ACIA), or any other communications chip that employs a standard asynchronous serial system. There are eight selectable serial data communication formats.

  — Data length: Seven or eight bits

  — Stop bit length: One or two bits

  — Parity: Even, odd, or none

  — LSB first

  — Receive error detection: Parity, framing, and overrun errors

  — Break detection: Break is detected when the received data next the generated framing error is the space 0 level and has the framing error.

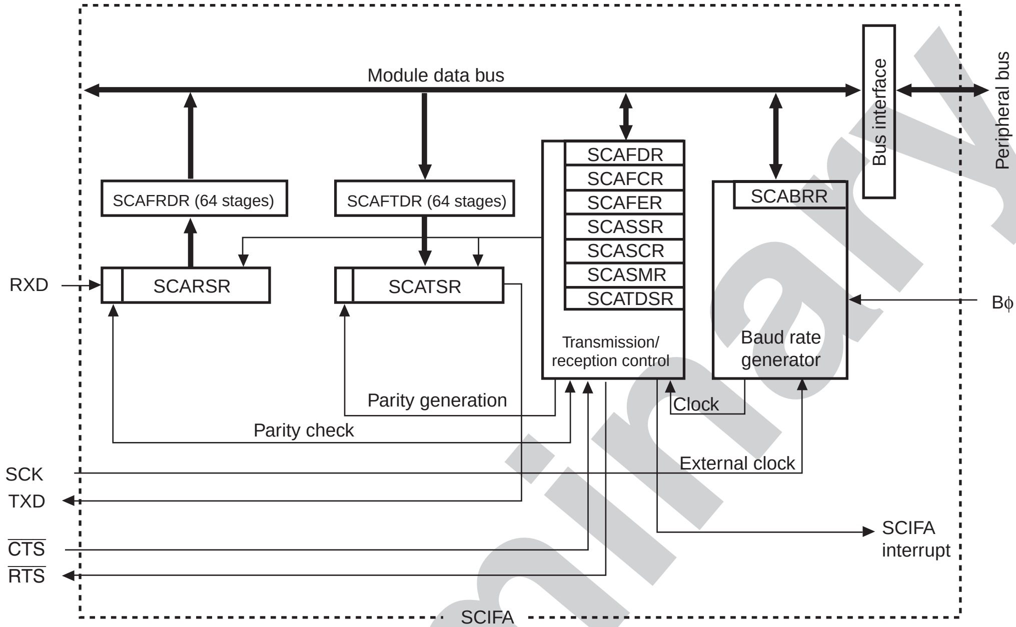
- Synchronous mode:

  Serial data communication is synchronized with a clock. Serial data communication can be carried out with other chips that have a synchronous communication function.

  — Data length: 8 bits

  — LSB-first transfer

Figure 18.1 shows the block diagram of SCIFA.



[Legend]

SCARSR: Receive shift register
SCAFRDR: Receive FIFO data register
SCATSR: Transmit shift register
SCAFTDR: Transmit FIFO data register
SCASMR: Serial mode register
SCASCR: Serial control register
SCAFER: FIFO error count register
SCASSR: Serial status register
SCABRR: Bit rate register
SCAFCR: FIFO control register
SCAFDR: FIFO data count register
SCATDSR: Transmit data stop register
Bϕ: Bus clock

Figure 18.1 Block Diagram of SCIFA

18.2 Input/Output Pins

Table 18.1 shows the pin configuration of SCIFA.

Table 18.1 Pin configuration

Channel	Pin Name	I/O	Function
3	SCIF3_SCK	Input/output	Clock input/output
	SCIF3_RXD	Input	Received data input
	SCIF3_TXD	Output	Transmit data output
	$\overline{\text{SCIF3\_CTS}}$	Input	Clear to send
	$\overline{\text{SCIF3\_RTS}}$	Output	Request to send
4	SCIF4_SCK	Input/output	Clock input/output
	SCIF4_RXD	Input	Received data input
	SCIF4_TXD	Output	Transmit data output
5	SCIF5_SCK	Input/output	Clock input/output
	SCIF5_RXD	Input	Received data input
	SCIF5_TXD	Output	Transmit data output

Note: In the following description, channel numbers in pin names are omitted and SCK, RXD, TXD, $\overline{\text{CTS}}$, and $\overline{\text{RTS}}$ are used as the generic abbreviations.

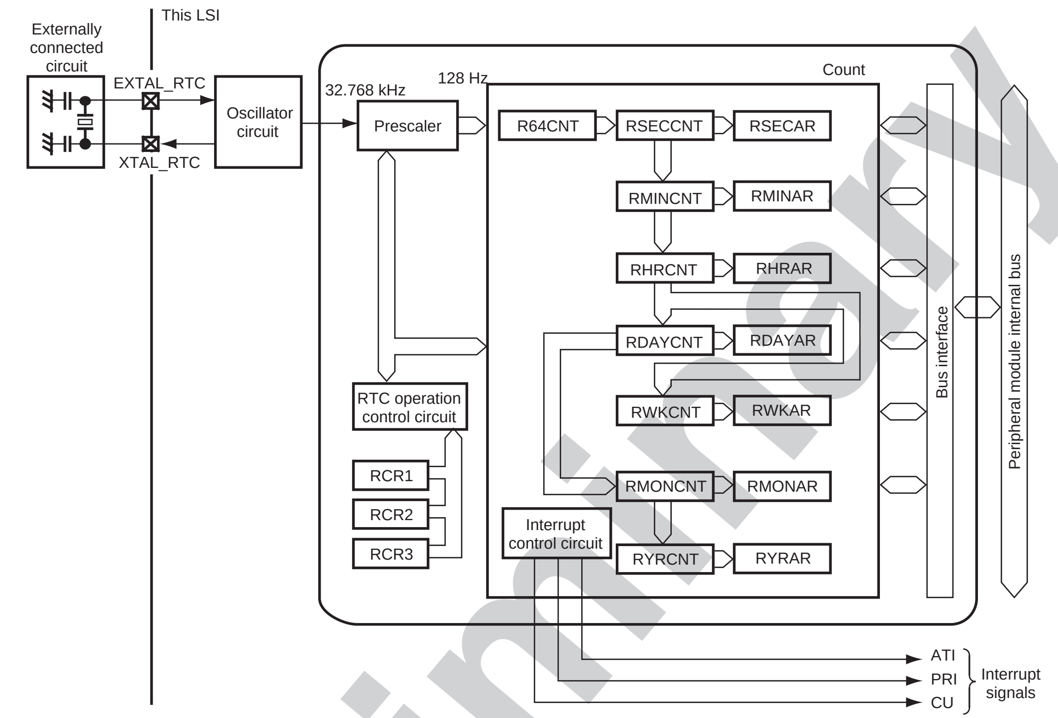
Section 19 Realtime Clock (RTC)

This LSI has a realtime clock (RTC).

19.1 Features

- Clock and calendar functions (BCD format): Seconds, minutes, hours, date, day of the week, month, and year
- 1-Hz to 64-Hz timer (binary format)
  64-Hz counter indicates the state of the RTC divider circuit between 64 Hz and 1 Hz
- Start/stop function
- 30-second adjust function
- Alarm interrupt: Frame comparison of seconds, minutes, hours, date, day of the week, month, and year can be used as conditions for the alarm interrupt
- Periodic interrupts: the interrupt cycle may be 1/256 second, 1/64 second, 1/16 second, 1/4 second, 1/2 second, 1 second, or 2 seconds
- Carry interrupt: indicates when a carry occurs or 64-Hz counter carry occurs during a 64-Hz counter read
- Automatic leap year adjustment

Figure 19.1 shows the block diagram of RTC.



[Legend]

RSECCNT:	Second counter (8 bits)	RSECAR:	Second alarm register (8 bits)
RMINCNT:	Minute counter (8 bits)	RMINAR:	Minute alarm registger (8 bits)
RHRCNT:	Hour counter (8 bits)	RHRAR:	Hour alarm register (8 bits)
RWKCNT:	Day of week counter (8 bits)	RWKAR:	Day of week alarm register (8 bits)
RDAYCNT:	Date counter	RDAYAR:	Date alarm register (8 bits)
RMONCNT:	Month counter (8 bits)	RMONAR:	Month alarm register (8 bits)
RYRCNT:	Year counter (16 bits)	RYRAR:	Year alarm register (16 bits)
R64CNT:	64-Hz counter (8 bits)	RCR2:	RTC control register 2 (8 bits)
RCR1:	RTC control register 1 (8 bits)	RCR3:	RTC control register 3

Figure 19.1 RTC Block Diagram

19.2 Input/Output Pin

Table 19.1 shows the RTC pin configuration.

Table 19.1 Pin Configuration

Name	Abbreviation	I/O	Function
External clock for RTC	RCLK	Input	Inputs the external clock for the RTC.

Section 20 IrDA Interface (IrDA)

The IrDA interface (IrDA) performs infrared data communication conforming to IrDA standard 1.2a through an external infrared transceiver unit connected to this LSI.

The IrDA includes a UART block to control data transmission and reception as well as an infrared transmit and receive (light-emit and light-receive) pulse modulator/demodulator block and a CRC engine block in front of the UART. The UART block controls serial data transmission and reception in the asynchronous mode. The infrared transmit and receive pulse modulator/demodulator block controls communication pulses and checks pulses received through infrared baseband modulation/demodulation conforming to IrDA standard 1.2a. The CRC engine block reads 8-bit input data and outputs a 16-bit CRC calculation result.

20.1 Features

The IrDA has the following UART features.

- Asynchronous serial communication
  - Data length: Eight bits
  - Stop bit: One bit
  - Parity bit: None
- Reception error detection: Overrun error and framing error
- Baud rate error correction: 16 decimal fractions can be selected.
- Baud rate count: Up to 65536 can be specified.

The IrDA has the following infrared transmit and receive pulse modulator/demodulator features.

- Infrared transmit (light-emit) pulse width: 1-bit width × 3/16 or 1.63 μs can be selected.
- Pulse width check: An out-of-standard pulse (insufficient or excess width) can be detected.
- 1.8432-MHz clock generator
  - Up to 16 can be specified for the integer part of the baud rate count.
  - The fractional part can be selected from 16 values.

The IrDA has the following CRC calculation features.

- Generator polynomial: $X^{16} + X^{12} + X^{5} + 1$
- Data input
  - — Input in bytes
  - — CRC is calculated in 8-bit units starting from the lower bits.
- CRC output: 16-bit CRC is output.
- Maximum data length: 4096 bytes

Figure 20.1 shows a block diagram of the IrDA.

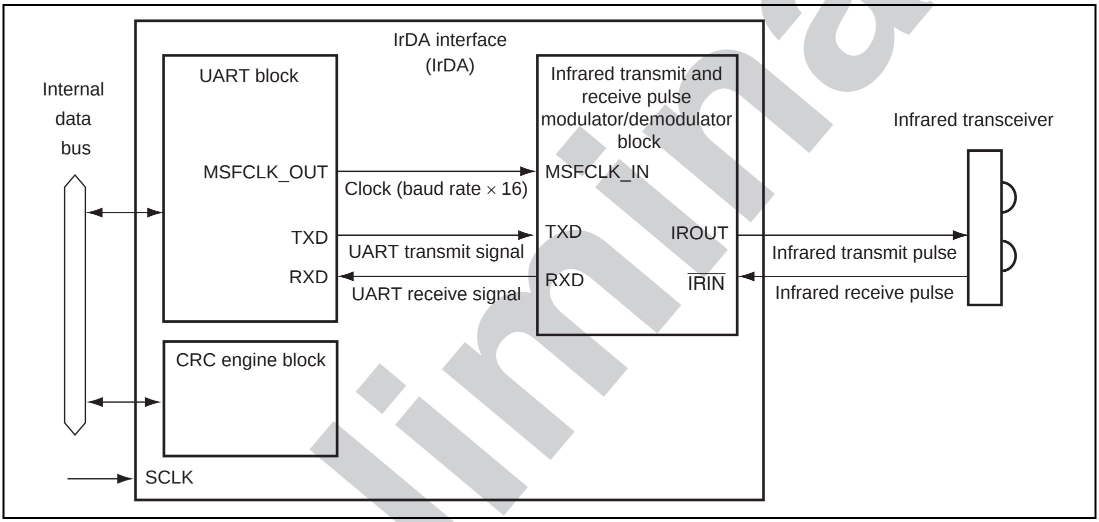


Figure 20.1 Block Diagram of IrDA

20.2 Input/Output Pins

Table 20.1 shows the IrDA pin configuration.

Table 20.1 Pin Configuration

Pin Name	Abbreviation	I/O	Function
$\overline{\mathrm{IrDA\_IN}}$	$\overline{\mathrm{IRIN}}$	Input	Infrared receive (light-receive) pulse input (negative logic)
IrDA_OUT	IROUT	Output	Infrared transmit (light-emit) pulse output (positive logic)

Section 21 Key Scan Interface (KEYSC)

This LSI has a key scan interface (KEYSC) that can set the input or output bit numbers to be programmable.

21.1 Features

- On-chip chattering elimination circuit
- Chattering elimination time can be set to be programmable
- Measures to deal with multiple key presses
- Level/edge-selectable internal interrupts
- Canceling software standby and U-standby modes by the key input (level) interrupt.
- Input or output bit numbers can be set to be programmable

Figure 21.1 shows a block diagram of the key scan interface.

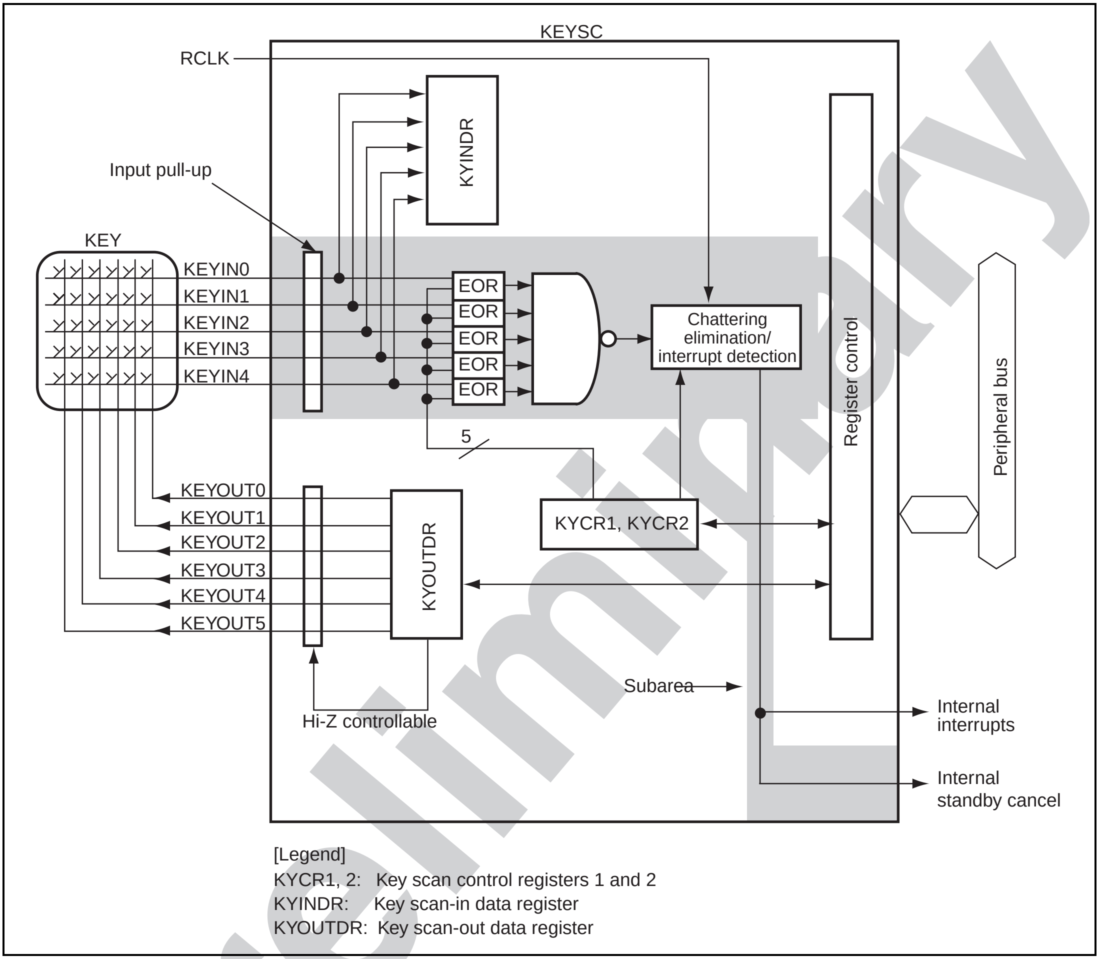


Figure 21.1 Block Diagram of Key Scan Interface (Key Pin Mode 1)

21.2 Input/Output Pins

The pin configuration of the key scan interface is listed in table 21.1.

Table 21.1 Pin Configuration

Name	Abbreviation	I/O	Function
Input key scan interface 6 to 0	KEYIN6 to KEYIN0	Input	Key scan interface for input
Output key scan interface 5 to 0	KEYOUT5 to KEYOUT0	Output	Key scan interface for output

The KEYOUT5 and KEYOUT4 pins are multiplexed with the KEYIN5 and KEYIN6 pins respectively. Setting the KYMD1 and KYMD0 bits in the key scan control register 1 (KYCR1) selects either those functions. Table 21.2 shows the possible combinations between the KEYIN and KEYOUT pins.

Table 21.2 Multiplex Pin Setting

Name	KYMD1	KYMD0	KEYOUT5/KEYIN5 Pin	KEYOUT4/KEYIN6 Pin
Key pin mode 1	0	0	Selects KEYOUT5 pin	Selects KEYOUT4 pin
Key pin mode 2	0	1	Selects KEYIN5 pin	Selects KEYOUT4 pin
Key pin mode 3	1	0	Selects KEYIN5 pin	Selects KEYIN6 pin

Section 22 USB 2.0 Host/Function Module (USB)

The USB 2.0 host/function module (USB) is a USB controller which provides capabilities as a USB host controller and USB function controller function. This module supports high-speed transfer defined by USB (universal serial bus) Specification 2.0, full-speed transfer, and low-speed transfer when used as the host controller, and supports high-speed transfer and full-speed transfer when used as the function controller. This module has a USB transceiver and supports all of the transfer types defined by the USB specification.

This module has an 16-kbyte buffer memory for data transfer, providing a maximum of ten pipes. Any endpoint numbers can be assigned to PIPE1 to PIPE9, based on the peripheral devices or user system for communication.

22.1 Features

(1) Host Controller and Function Controller Supporting USB High-Speed Operation

- The USB host controller and USB function controller are incorporated.
- The USB host controller and USB function controller can be switched by register settings.
- USB transceiver is incorporated.

(2) Reduced Number of External Pins and Space-Saving Installation

- The VBUS signal can be directly connected to the input pin of this module.
- On-chip D+ pull-up resistor (during USB function operation)
- On-chip D+ and D- pull-down resistor (during USB host operation)
- On-chip D+ and D- terminal resistor (during high-speed operation)
- On-chip D+ and D- output impedance (during full-speed operation)

(3) All Types of USB Transfers Supported

- Control transfer
- Bulk transfer
- Interrupt transfer (high bandwidth transfers not supported)
- Isochronous transfer (high bandwidth transfers not supported)

(4) Internal Bus Interfaces

- Two DMA interface channels are incorporated.

(5) Pipe Configuration

- Up to 16 kbytes of buffer memory for USB communications are supported
- Up to ten pipes can be selected (including the default control pipe)
- Programmable pipe configuration
- Endpoint numbers can be assigned flexibly to PIPE1 to PIPE9.
- Transfer conditions that can be set for each pipe:

  PIPE0: Control transfer (default control pipe: DCP), 64-byte fixed single buffer

  PIPE1 and PIPE2: Bulk transfers/isochronous transfer, continuous transfer mode, programmable buffer size (up to 2-kbytes: double buffer can be specified)

  PIPE3 to PIPE5: Bulk transfer, continuous transfer mode, programmable buffer size (up to 2-kbytes: double buffer can be specified)

  PIPE6 to PIPE9: Interrupt transfer, 64-byte fixed single buffer

(6) Features of the USB Host Controller

- High-speed transfer (480 Mbps), full-speed transfer (12 Mbps), and low-speed transfer (1.5 Mbps) are supported.
- Communications with multiple peripheral devices connected via a single HUB
- Automatic response to the reset handshake
- Automatic scheduling for SOF and packet transmissions
- Programmable intervals for isochronous and interrupt transfers

(7) Features of the USB Function Controller

- Both high-speed transfer (480 Mbps) and full-speed transfer (12 Mbps) are supported.
- Automatic recognition of high-speed operation or full-speed operation based on automatic response to the reset handshake
- Control transfer stage control function
- Device state control function
- Auto response function for SET_ADDRESS request
- NAK response interrupt function (NRDY)
- SOF interpolation function

(8) Other Features

- Transfer ending function using transaction count
- BRDY interrupt event notification timing change function (BFRE)
- Function that automatically clears the buffer memory after the data for the pipe specified at the DnFIFO (n = 0 or 1) port has been read (DCLRM)
- NAK setting function for response PID generated by end of transfer (SHTNAK)

22.2 Input/Output Pins

Table 22.1 shows the pin configuration of the USB.

Table 22.1 USB Pin Configuration

Pin Name	Name	I/O	Function
DP	USB D+ data	I/O	D+ I/O of the USB on-chip transceiver This pin should be connected to the D+ pin of the USB bus.
DM	USB D- data	I/O	D– I/O of the USB on-chip transceiver This pin should be connected to the D- pin of the USB bus.
VBUS	VBUS input	Input	USB cable connection monitor pin This pin should be connected directly to the VBUS of the USB bus. Whether the VBUS is connected or disconnected can be detected. If this pin is not connected with the VBUS of the USB bus, it should be supplied with 5 V. It should be supplied with 5 V also when the host controller function is selected.
REFRIN	Reference input	Input	Reference resistor connection pin This pin should be connected to AG33 through a 5.6 kΩ ±1% resistor.
XTAL_USB	Crystal input output pin (Clock input pin)	Output	These pins should be connected to crystal oscillators for the USB. The EXTAL_USB pin can be used for external clock input.
EXTAL_USB		Input	

Section 23 I^{2}C Bus Interface (IIC)

This LSI has an I^{2}C bus interface of one channel.

Each I^{2}C bus interface uses only one data line (SDA) and one clock line (SCL) to transfer data, saving board and connector space.

23.1 Features

- Start and stop conditions generated automatically
- Selection of acknowledge output levels when receiving
- Automatic loading of acknowledge bit when transmitting
- Data transfer conforming to the I^{2}C format
- Wait function

  A wait can be inserted by driving the SCL pin low after data transfer, excluding acknowledgement.

  The wait can be cleared by clearing the interrupt flag.
- I^{2}C module corresponds to single master bus only

  This module is always in master mode. Since the slave mode is not incorporated, operation stops with bus open during loss of arbitration in data transfer.
- Four interrupt sources
  - Data transfer enable
  - Wait state
  - Non-acknowledge detection
  - Arbitration lost (operation stops with bus open when bus conflict is detected)
- Data transfer speed
  - Standard mode (100 kHz) and high-speed mode (400 kHz)
  - SCL clock can be set by clock control register setting
- Clock synchronous processing of SCL line

  A hazard (spike noise) generated in the high-count period by SCL is detected as an arbitration loss.

Figure 23.1 shows a block diagram of the I^{2}C bus interface.

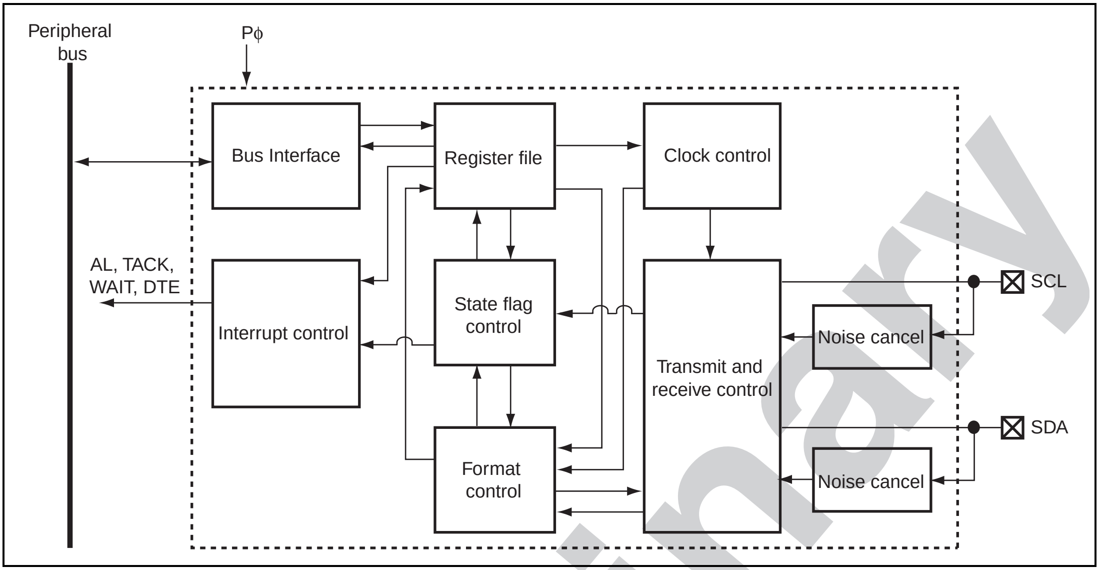


Figure 23.1 Block Diagram of I²C Bus Interface

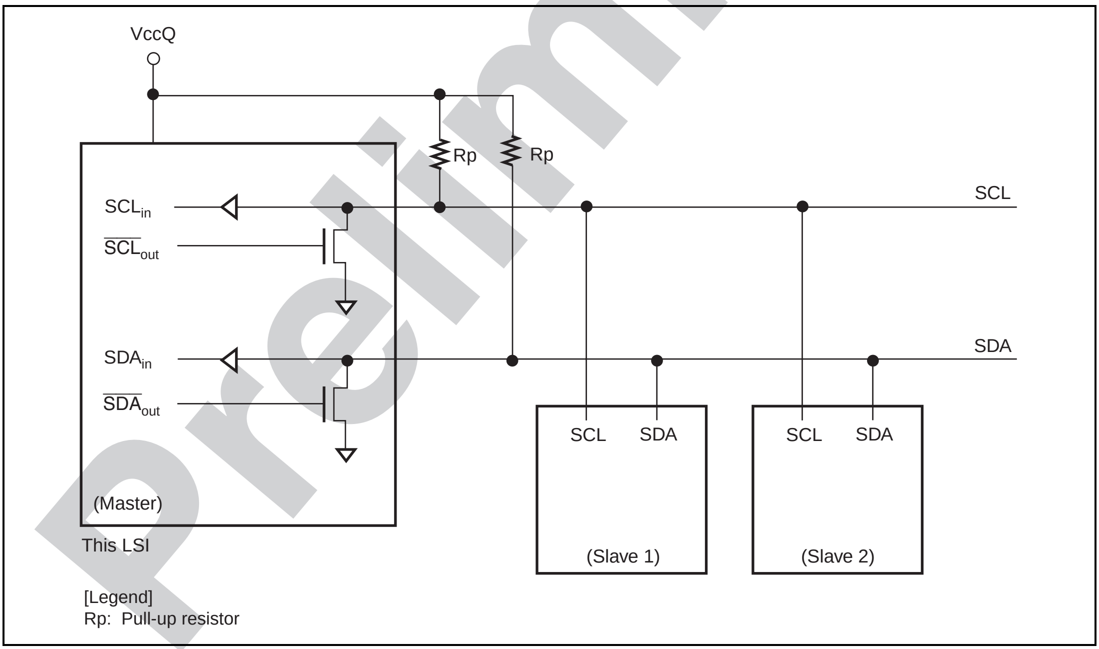


Figure 23.2 I²C Bus Interface Connections

23.2 Input/Output Pins

Table 23.1 summarizes the input/output pins used by the I^{2}C bus interface.

Table 23.1 I^{2}C Bus Interface Pins

Abbreviation	Function	I/O	Description
SCL (O/D)	I^{2}C clock input/ output	I/O	I^{2}C bus clock input/output pin Equipped with the bus drive function (NMOS open-drain).
SDA (O/D)	I^{2}C data input/ output	I/O	I^{2}C bus data input/output pin Equipped with the bus drive function (NMOS open-drain).

Section 24 NAND Flash Memory Controller (FLCTL)

The NAND flash memory controller (FLCTL) provides a memory interface for an external NAND-type flash memory. To take measures for errors specific to flash memory, the FLCTL supports the ECC-code generation function and error detection function. In addition to a 3-symbol ECC detection circuit to support MLC products, the FLCTL generates ECC code with up to 4 symbols, detects ECC code errors and has an error pattern generation circuit.

24.1 Features

(1) NAND-Type Flash Memory Interface

- Interface directly connectable to NAND-type flash memory
- Read or write in sector units (512 + 16 bytes) and ECC processing executed
- Read or write in byte units
- Supports addresses of up to 5 bytes

Note: An access unit of 512 + 16bytes is referred to as a page in some datasheets for NAND-type flash memory. In this manual, this access unit of 512 + 16 bytes is always referred to as a sector. Each page of 2048 + 64 bytes is divided into four sectors, each consisting of 512 + 16 bytes.

(2) Access Modes

The FLCTL can select one of the following two access modes.

- Command access mode: Performs an access by specifying a command to be issued from the FLCTL to flash memory, address, and data size to be input or output. Read, write, or erasure of data without ECC processing can be achieved.
- Sector access mode: Performs a read or write in sector units by specifying a sector address and controls ECC-code generation and check. By specifying the number of sectors, the continuous sectors can be read or written (specify addresses in sector addresses).
- High-speed sector access mode: The following commands are supported to access the flash memory at a high speed. Note that some flash memory products do not support these commands:
  - “Auto Page Program Operation with Data Cache”
  - “Read Operation with Read Cache”

(3) Sectors and Control Codes

- A sector is comprised of 512-byte data and 16-byte control code. The 16-byte control code includes 8-byte ECC.
- The control code includes 10-byte ECC when using a 4-symbol ECC circuit.
- The position of the ECC in the control code can be specified in 4-byte units.
- The user can write any data into bytes 0 to 5 in the control area when using a 4-symbol ECC circuit.
- User information can be written to the control code other than the ECC.

(4) 3-symbol ECC

- 8-byte ECC code is generated and error check is performed for a sector (512-byte data + 16-byte control code). (Note that the ECC code generation in the 16-byte control code and the number of bytes to be checked differ depending on the specifications.)
- Error correction capability is up to three errors.
- In a write operation, an ECC code is generated for data and control code prior to the ECC. The control code following the ECC is not considered.
- In a read operation, an ECC error is checked for data and control code prior to the ECC. An ECC on the control code in the FIFO is replaced with the check result by the ECC circuit, not an ECC code read from flash memory.
- An error correction is not performed even when an ECC error occurs. Error corrections must be performed by software.

(5) 4-symbol ECC

- 80-bit (10-byte) ECC code is added to a sector (512-byte data + 6-byte control code).
- Error correction and detection capability covers up to four random errors (up to 40 bits).
- In a write operation, an ECC code is generated for data and control code prior to the ECC.
- In a read operation, an ECC error is checked for data and control code prior to the ECC. An ECC on the control code in the FIFO is replaced with the check result by the ECC circuit, not an ECC code read from flash memory.
- The 4-symbol ECC circuit in this FLCTL can generate error correction patterns using the hardware. The error correction pattern generation and checking are performed in sector units.
- The hardware-based error correction outputs addresses indicating the locations of errors and error patterns to correct errors.

(6) Data Error

- When a program error or erase error occurs, the error is reflected on the error source flags. Interrupts for each source can be specified.
- When a read error occurs, an ECC in the control code is other than 0. This read error is reflected on the ECC error source flag.
- When an ECC error occurs, perform an error correction, specify another sector to be replaced, and copy the contents of the block to another sector as required.

(7) Data Transfer FIFO and Data Register

- The 224-byte FLDTFIFO is incorporated for data transfer of flash memory.
- The 32-byte FLECFIFO is incorporated for data transfer of control code.
- The overrun/underrun detection flag is provided for the access from the CPU and DMA.

(8) DMA Transfer

- By individually specifying the destinations of data and control code of flash memory to the DMA controller, data and control code can be sent to different areas.

(9) Access Size

- Registers can be accessed in 32 bits or 8 bits. Registers must be accessed in the specified access size.
- The FIFO is accessed in 32-bit (4-byte) units. If the specified number of bytes for read and write accesses is not a multiple of 4, the fractional bytes are handled as padding bytes.
- The register contents are damaged if the access size is violated.

(10) Access Time

- The operating frequency of the FLCTL pins can be specified by the FCKSEL bit and the QTSEL bit in the common control register (FLCMNCR), regardless of the operating frequency of the peripheral bus.
- Before changing the CPG specification, the FLCTL must be placed in a module stop state.
- In NAND-type flash memory, the FSC and $\overline{\text{FWE}}$ pins operate with the frequency on the pins which CPG designated. To ensure the setup time, these operating frequencies must be specified within the maximum operating frequency of memory to be connected.
- The operating clock FCLK on the pins for the NAND-type flash memory is generated by dividing the peripheral bus operating clock $P\phi$.

Figure 24.1 shows a block diagram of the FLCTL.

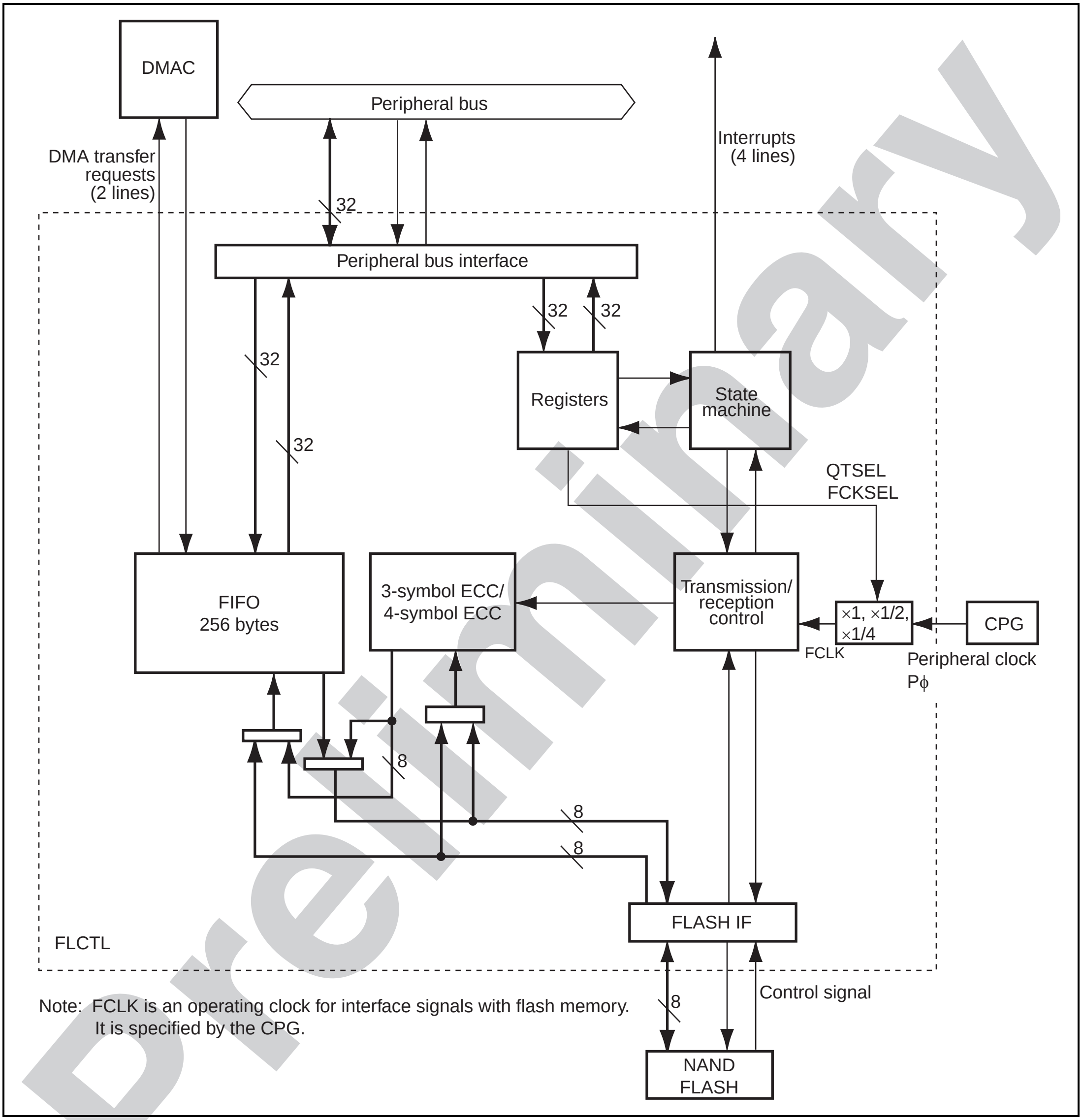


Figure 24.1 FLCTL Block Diagram

24.2 Input/Output Pins

The pin configuration of the FLCTL is listed in table 24.1.

Table 24.1 Pin Configuration

Pin Name	Function	I/O	Corresponding NAND Type Flash Memory Pin	Description
$\overline{\text{FCE}}$	Chip enable	Output	$\overline{\text{CE}}$	Enables flash memory connected to this LSI.
NAF7 to NAF0	Data I/O pins	I/O	I/O7 to I/O0	I/O pins for command, address, and data.
FCDE	Command data enable	Output	CLE	Command Latch Enable (CLE) Asserted when a command is output. Command Data Enable ($\overline{\text{CDE}}$) Asserted when a command is output.
FOE	Output enable	Output	ALE	Address Latch Enable (ALE) Asserted when an address is output and negated when data is input or output. Output Enable ($\overline{\text{OE}}$) Asserted when data is input or when a status is read.
FSC	Serial clock	Output	$\overline{\text{RE}}$	Read Enable ($\overline{\text{RE}}$) Reads data at the falling edge of $\overline{\text{RE}}$. Serial Clock (SC) Inputs or outputs data synchronously with the SC.
$\overline{\text{FWE}}$	Write enable	Output	$\overline{\text{WE}}$	Write Enable Flash memory latches a command, address, and data at the rising edge of $\overline{\text{WE}}$.
FRB	Ready/busy	Input	R/$\overline{\text{B}}$	Ready/Busy Indicates ready state at high level; indicates busy state at low level.
—*	—	—	$\overline{\text{WP}}$	Write Protect/Reset When this pin goes low, erroneous erasure or programming at power on or off can be prevented.
—*	—	—	$\overline{\text{SE}}$	Spare Area Enable Used to access spare area. This pin must be fixed at low in sector access mode.

Note: * Not supported in this LSI.

Section 25 Video Processing Unit (VPU)

25.1 Function Overview

25.1.1 Functions

The VPU (video processing unit) is an IP that can:
(1) Decode bit streams that conform to VC-1 (SMPTE 412M-2006), and
(2) Encode and decode bit streams that conform to MPEG-4 (ISO/IEC 14496).

The VPU supports the following MPEG-4 video standards: Simple Profile, Advanced Simple Profile, and Short Header (hereafter collectively called MPEG-4); AVC Baseline Profile (hereafter called AVC); and VC-1 Simple Profile and Main Profile (hereafter collectively called VC-1).

The VPU has the following excellent features:

- Dynamic Timeslot Method (DTME)

  The length of slots used in pipelining can be changed dynamically according to the bus state. This makes it possible to maintain the optimal processing time for slots when the volume of bus traffic is large.
- VOP encoding for MPEG-4 and AVC

  The VPU encodes MPEG-4 images in memory in VOP units and AVC images in memory in slice units to generate bit streams. For MPEG-4, B-VOP encoding (bidirectional search) is supported. For AVC, multi-reference encoding (two-plane) is supported. In addition, Quarter-pel-precision searches in units of 8 × 8 blocks at minimum are available in AVC encoding.

  ARME (adaptive realtime motion estimation): The quality of motion estimation can be enhanced by expanding the search range and increasing the search count (common to MPEG-4 and AVC).

  POI (predict from original image): An intra prediction mode allowing searches in realtime is available (for AVC).

  ASP (active skip prediction): Controlling searches in such a way that the number of skipped macroblocks can be increased improves the image quality at a low bit rate (for AVC).

  CWQ (custom weighted quantization): Code amount control is available for each macroblock (MB) in a plane to be encoded. When encoding a portrait, for example, assigning more codes to the center of the image can enable more detailed expression.
- Video decoding for MPEG-4, AVC, and VC-1

  The VPU reads bit streams from memory and decodes them in VOP units for MPEG-4, in slice units for AVC, and in picture units for VC-1.

Multiple concealment modes are supported so that, if an error occurs, the error area and error block boundary can be concealed.

- Deblocking filter

  A deblocking filtered image can be output additionally for both a decoded image and a local decode image when encoding.

- Video header search for MPEG-4

  A bit stream is read from memory to detect the next start code.

See table 25.1 for details of the specification of the VPU. In addition, the video syntax layer that the VPU processes for acceleration varies from one profile to another. See table 25.2 for details.

Table 25.1 VPU Basic Specification

Decoding

Applicable Standard			MPEG-4 Simple Profile L2	MPEG-4 Advanced-Simple Profile L3*[1]
General	Image size	Maximum	720 × 480 @30 fps 720 × 576 @25 fps	720 × 480 @30 fps 720 × 576 @25 fps
		Minimum	48 × 48	48 × 48
		Unit of size	Four horizontal pixels and four vertical pixels	Four horizontal pixels and four vertical pixels
	Maximum bit rate		384 Kbps	8 Mbps
	Supported type		I, P: VOP	I, P, B: VOP
	Supported format		4:2:0	4:2:0
	Supported structure		Progressive	Progressive Interlace
ME/MC	Supported MV		UMV, 4MV	UMV, 4MV, Direct B
	Unit of MV		Half-pel	Half-pel
	Maximum detection range		—	—
	Detection mode		—	—
	Unit of processed blocks		8 × 8, 16 × 16	8 × 8, 16 × 16
	Maximum number of reference planes		1	2
	Deblocking filter		Output in parallel with post-processing	Output in parallel with post-processing
Prediction	Mode		IntraDC/AC	IntraDC/AC
Q/IQ	Mode		type 1/2	type 1/2
VLC	Error resilience		Resync Maker Data Partitioning Reversible VLC (no inverse decoding is performed) Error concealment	Resync Maker Data Partitioning Reversible VLC (no inverse decoding is performed) Error concealment
Others			ShortHeader	—
Remarks				

Decoding

General Specifications	Applicable Standard		H.264 (BaseLine) @L2.1	VC-1 Main Profile[*2] Medium Level
General	Image size	Maximum	720 × 480 @30 fps 720 × 576 @25 fps	720 × 480 @30 fps 720 × 576 @25 fps
		Minimum	48 × 48	48 × 48
		Unit of size	16 horizontal pixels and 16 vertical pixels[*3]	Four horizontal pixels and four vertical pixels
	Maximum bit rate		8 Mbps	8 Mbps
	Supported type		IDR, I, P: slice	I, P
	Supported format		4:2:0	4:2:0
	Supported structure		Progressive	Progressive
ME/MC	Supported MV		UMV 1MV to 16MV	UMV 4MV
	Unit of MV		Quarter-pel	Quarter-pel
	Maximum detection range		—	—
	Detection mode		—	—
	Unit of processed blocks		4 × 4 to 16 × 16	8 × 8, 16 × 16
	Maximum number of reference planes		16	1
	Deblocking filter		Within loop	Output in parallel with post-processing
Prediction	Mode		IntraDC/V/H/Diag	IntraDC/AC
Q/IQ	Mode		IntTrans + QHadamard	HalfQP
VLC	Error resilience		Error concealment	Error concealment
VSOT	Integer transform		—	Integer transform of variable block size (8 × 8, 8 × 4, 4 × 8, 4 × 4) Overlap transform
Others			MV output function	Bit planes are specified externally.

Notes: 1. Except for GMC, Qpel, and 4MV.
2. Except for dynamic resolution change, B-frame, and range reduction.
3. Images are output always in 16-pixel units; no cropping is performed.

[Legend]

ME: Motion estimation

MC: Motion compensation

Q: Quantization

IQ: Inverse quantization

VLC: Variable length coding and decoding

Encoding

General Specifications	Applicable Standard		MPEG-4 Simple Profile L2	MPEG-4 Advanced-Simple Profile L3*	H.264 (BaseLine*) @L2.1
General	Image size	Maximum	720 × 480 @30 fps 720 × 576 @25 fps	720 × 480 @30 fps 720 × 576 @25 fps	720 × 480 @30 fps 720 × 576 @25 fps
		Minimum	48 × 48	48 × 48	48 × 48
		Unit of size	Four horizontal pixels and four vertical pixels	Four horizontal pixels and four vertical pixels	Four horizontal pixels and four vertical pixels
	Maximum bit rate		384 Kbps	10 Mbps	10 Mbps
	Supported type		I, P: VOP	I, P, B: VOP	IDR, I, P: slice
	Supported format		4:2:0	4:2:0	4:2:0
	Supported structure		Progressive	Progressive Interlace	Progressive
ME/MC	Supported MV		UMV	UMV	UMV 1MV to 4MV
	Unit of MV		Half-pel	Half-pel	Quarter-pel
	Maximum detection range		±32	±32	±32
	Detection mode		Tracking type	Tracking type	Tracking type
	Unit of processed blocks		16 × 16	16 × 16	8 × 8 to 16 × 16
	Maximum number of reference planes		1	2	2
	Deblocking filter		—	—	Within loop
Prediction	Mode		IntraDC/AC	IntraDC/AC	IntraDC/V/H/Diag
Q/IQ	Mode		type 1/2	type 1/2	IntTrans + QHadamard
VLC	Error resilience		Resync Maker Data Partitioning Reversible VLC	Resync Maker Data Partitioning Reversible VLC	—
Others			ShortHeader	Interlace	MV output function
Remarks					

Note: Except for GMC, QuarterPel, and 4MV

[Legend]
ME: Motion estimation
MC: Motion compensation
Q: Quantization
IQ: Inverse quantization
VLC: Variable length coding and decoding

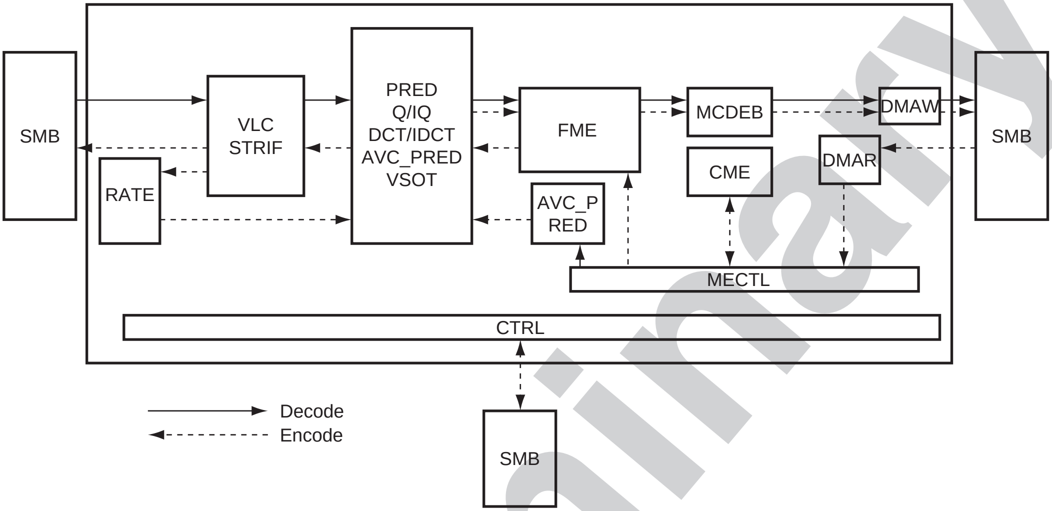
Table 25.2 Scope of VPU Processing

Unit of Processing	Encoding	Decoding
VC-1	Unavailable	Picture layer Macroblock layer Block layer Note: No picture header can be decoded.
MPEG-4ASP, SP	Video object plane (VOP) Video packet Group of block (GOB) Macroblock Block	Video object plane (VOP) Video packet Group of block (GOB) Macroblock Block
MPEG-4AVC	I-slice P-slice Instantaneous Decoding Refresh (IDR) Slice in Raw Byte Sequence Payload (RBSP) Note: No slice header can be encoded.	I-slice P-slice Instantaneous Decoding Refresh (IDR) Slice in Raw Byte Sequence Payload (RBSP) Note: No slice header can be decoded.

[Legend]
VOP: Video Object Plane
GOB: Group of Block
IDR: Instantaneous Decoding Refresh in RBSP (Raw Byte Sequence Payload)

25.1.2 Block Diagram

Figure 25.1 shows the block diagram of the VPU.



[Legend]

SMB:	SHwy multimedia brouter	CTRL:	Overall control block
DMAR:	Image read	DMAW:	Image write
CME:	Coarse-search motion estimation	FME:	Fine-search motion estimation
MCDEB:	Motion compensation and deblocking filter		
DCT:	Discrete cosine transform	IDCT:	Inverse discrete cosine transform
Q:	Quantization	IQ:	Inverse quantization
AVC_PRED:	Integer transform, Hadamard transform		
VSOT:	VC1 integer transform and overlap transform		
PRED:	DCT coefficient prediction	RATE:	Rate control
VLC:	Variable length coding and decoding	STRIF:	Stream input/output

Figure 25.1 VPU Block Diagram

Section 26 Video I/O (VIO)

Note: This section contains references to the SH7723 Hardware Manual. The contents of the SH7723 Hardware Manual will be disclosed upon acceptance of a confidentiality agreement. For details, please contact a Renesas Technology sales representative.

This LSI incorporates a video I/O (VIO) module that can be used to perform capturing of an externally input image, format conversion of a YCbCr/RGB image, scaling, tone reduction, and blending of displays.

26.1 Features

The VIO consists of a capture engine unit (CEU), two video engine units (VEU2H0/VEU2H1), and a blending engine unit (BEU). The features of each unit are listed below.

(1) CEU : Capture Engine Unit

The CEU is a capture module that fetches image data externally input and transfers it to the memory. The CEU is connected to the system bus via bus bridge modules.

(2) VEU2H : Video Engine Unit (Includes 2 VEU2H units)

The VEU2H is a module used connected to the buses via bus bridge modules. The VEU2H reads an image from a specified memory area, and writes it back to a specified address.

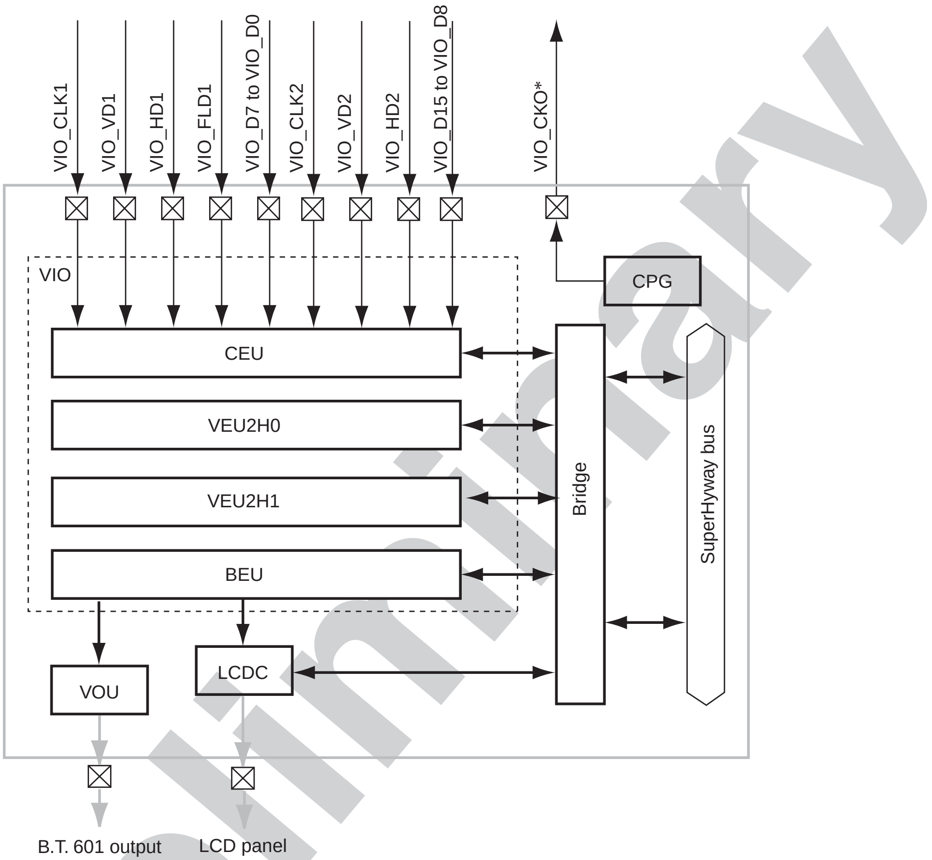
- Format conversion using the RGB ↔ YCbCr conversion function
- Scaling of an image using the filter function
- Tone reduction (quantization) to pack RGB data in 32-bit units
- Dithering for tone reduction of RGB data
- Removal of high-frequency components using the low-pass filter function
- Low-pass filter is applied to only the boundary of the blocks using the deblocking filter function
- Median filter function
- FIR filter function
- Edge enhancement of an image (enhancer function)

(3) BEU (Blending Engine Unit)

The BEU is a module used connected to the buses via bus bridge modules, and also connected to the VOU and the LCDC. The BEU blends three displays, and has a multiwindow function that displays four windows overlaying the blended display.

- Supports Video display
- Supports OSD (On Screen Display)
- Supports Graphic display
- Blends the three planes of Video1, Video2, and OSD/Graphic
- A facility for the RGB ↔ YCbCr transformations is included, enabling said format transformations (color transformations). After one blend (output system) by the input system, two units for format conversion (color conversion) are mounted, so the format is selectable as desired for three input planes and for the output.
- The three displays can be blended at desired positions.
- Any one of the three inputs can be used as the parent display.
- The location of a child display can overflow from the parent display, but the overflowed area is not output.
- Raster operation 2 function
- Multiwindow function (four windows are displayed overlaying the three blended displays)
- Selection between output to the memory, output to the VOU, output to the LCDC, and simultaneous output to the memory and VOU or LCDC

Figure 26.1 shows a block diagram of the VIO.



Note: * For details on the VIO_CKO function, see section 14, Clock Pulse Generator (CPG), in the SH7723 Hardware Manual.

Figure 26.1 Block Diagram of VIO

26.2 Functional Overview of CEU

The CEU (Capture Engine Unit) is a capture module that fetches image data externally input and transfers it to the memory. The CEU is connected to the system bus via bus bridge modules. The functional overview of the CEU is shown in table 26.1, and the main functions and their details are shown in table 26.2.

Table 26.1 Functional Overview of CEU

Classification	Item	Function	Description	Note
Connectable camera	Size	5M pixels	2560 pixels × 1920 lines	Horizontal: 4-pixel units Vertical: 4-line units
		3M pixels	2048 pixels × 1536 lines	
		2M pixels	1632 pixels × 1224 lines	
		UXGA	1600 pixels × 1200 lines	
		SXGA (1)	1280 pixels × 1024 lines	
		SXGA (2)	1280 pixels × 960 lines	
		XGA	1024 pixels × 768 lines	
		SVGA	800 pixels × 600 lines	
		VGA	640 pixels × 480 lines	
		CIF	352 pixels × 288 lines	
		QVGA	320 pixels × 240 lines	
		QCIF	176 pixels × 144 lines	
		QQVGA	160 pixels × 120 lines	
		Sub-QCIF	128 pixels × 96 lines	
	Input format	YCbCr 4:2:2 8 bits	Cb_0, Y_0, Cr_0, $Y_{1\ldots}$	Supports clock ratio of 1:1
			Cr_0, Y_0, Cb_0, $Y_{1\ldots}$	
			Y_0, Cb_0, Y_1, $Cr_{0\ldots}$	
			Y_0, Cr_0, Y_1, $Cb_{0\ldots}$	
		YCbCr 4:2:2 16 bits	{Y0, Cb0}, {Y1, Cr0}, …	
			{Y0, Cr0}, {Y1, Cb0}, …	

Classification	Item	Function	Description	Note
Connectable camera	Input format	Binary data	Specified amount to be fetched on edges of the sync signal	Written sequentially
			Data is fetched with the horizontal sync signal as an enable signal.	
	Horizontal and vertical sync signal polarities	Arbitrary	High-active and low-active	
	Capture start location	Arbitrary	Can be specified in camera input clock units	Horizontal: 1-cycle units Vertical: 1-HD (horizontal sync signal) units
	Number of captured pixels	Arbitrary	Can be specified in 4-pixel units horizontally and in 4-line units vertically	
	Interlace	Both-field capture	Stored as a field image	Capture: 2-VD (vertical sync signal) units
			Stored as a frame image	
		One-field capture	Top field or bottom field can be specified	Capture: 1-VD units
Memory write	Output format	YCbCr 4:2:2 YCbCr 4:2:0	YCbCr 4:2:0 is realized by simple skipping	
Filter function	No scaling or scale-down	Scale-down of captured display	Desired scaling factor from 1/16 to 1 (scaled-down display must not exceed VGA)	
	Low-pass filter		Removal of high-frequency components	Only in the horizontal direction
Display information acquisition	Complexity level	Acquisition of complexity level of captured display	Variation of pixel values is indicated	Used for MPEG-4 16-line units, 8-line units, or 1-display units can be selected

Table 26.2 Main Functions of CEU and Their Details

Main Function	Detailed Description
Image data fetch	• Captures an image output from an external module and writes YCbCr data to the memory with it separated into Y data and CbCr data. • Fetches image data other than YCbCr data, e.g. JPEG data, from an externally connected module, such as a camera, and sequentially writes the image data to the memory. • Fetches an interlace source image in both-field units or one-field units and writes it to the memory. In both-field capture, an image can be stored in the memory as a frame image.
Filter processing	Performs scale-down and removal of high-frequency components (only in the horizontal direction) for an image using internal filters. Note that the scaled-down image must not exceed VGA. The filter processing can be applied to only YCbCr input data.
Display information acquisition	Acquires the complexity level of the captured display and writes it to the memory. This information output at MPEG-4 encoding is useful for determining the scene change.
Format conversion	Converts image data input in the YCbCr 4:2:2 format into the YCbCr 4:2:0 format and writes it to the memory. Note that the conversion algorithm is simple skipping in which the chrominance component (CbCr) of the even-numbered lines is skipped.

Figure 26.2 shows a block diagram of the CEU.

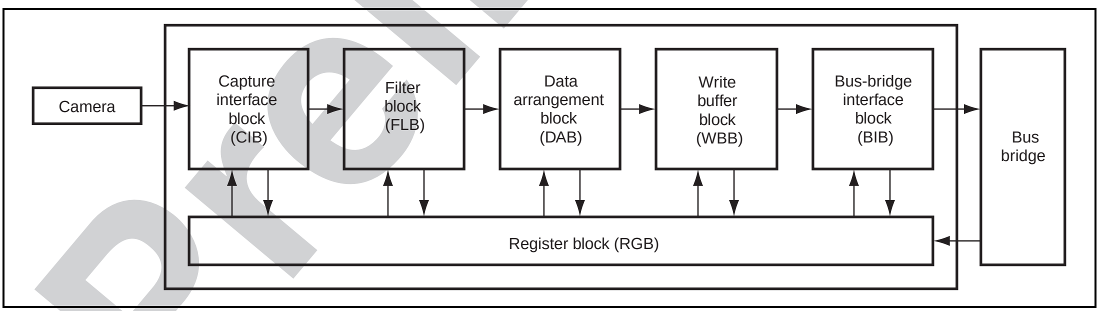


Figure 26.2 Block Diagram of CEU

26.3 Pin Configuration of CEU

The pin configuration of the CEU is shown in table 26.3.

Table 26.3 Pin Configuration of CEU

Pin Name	Function	I/O	Description
VIO_D15 to VIO_D8/ VIO_D7 to VIO_D0	VIO data bus	Input	Camera image data input to the VIO
VIO_CLK1/VIO_CLK2	VIO clock	Input	Camera clock input to the VIO
VIO_VD1/VIO_VD2	VIO vertical sync	Input	Camera vertical sync signal input to the VIO
VIO_HD1/VIO_HD2	VIO horizontal sync	Input	Camera horizontal sync signal input to the VIO
VIO_FLD	Field signal	Input	Field identification signal
VIO_CKO	Camera clock output	Output	Clock output to the camera

Note: * For VIO_CLK1/VIO_CLK2, VIO_VD1/VIO_VD2, VIO_HD1/VIO_HD2, and VIO_D15 to VIO_D8/VIO_D7 to VIO_D0, either of the functions can be used. In the 16-bit interface, VIO_D15 to VIO_D8/VIO_D7 to VIO_D0 are not switched since the data path is 16-bit. For the switching method, see section 38, Pin Function Controller (PFC), in the SH7723 Hardware Manual. When the distinction according to the bus width for the data bus is not needed, VIO_D is used in this manual. Otherwise, VIO_CLK, VIO_VD, and VIO_HD are used.

26.4 Functional Overview of VEU2H

The VEU2H is a module used connected to the buses via bus bridge modules. The VEU2H reads an image from a specified memory area, and writes it back to a specified address.

This LSI includes two unit of VEU2H.

The functional overview of the VEU2H is shown in table 26.4. Some functions of the VEU2H cannot be used at the same time unless the VEU2H is re-activated. Table 26.5 shows which functions can/cannot be used simultaneously during one VEU2H activation.

Table 26.4 Functional Overview of VEU2H

Item	Function	Description	Note
Input format	YCbCr (4:4:4/4:2:2/4:2:0) RGB pack		
Output format	YCbCr (4:4:4/4:2:2/4:2:0) RGB pack		
Read mode	Normal read Bundle read	8 to 960 lines can be set as the number of lines in bundle read	
Low-pass filter	Removal of high-frequency components		
Deblocking filter	Removal of high-frequency components only at the boundary of blocks		
Enhancer	Enhancement of image		
Median filter	Removal of shot noise		
FIR filter	FIR filter	8 bits, 11 tap, signed FIR filter	Not possible to use the median filter and deblocking filter at the same time.

Item	Function	Description	Note
Rotation/ inversion of image	Vertical or horizontal inversion	Can be specified independently	A combination of both functions can realize rotation by 180 degrees
	Rotation by 90 or 270 degrees	Rotated clockwise	
Scale-up, scale-down, or no scaling	Scale-up or scale-down of memory display	Any scaling factor from × 1/16 to × 8	
Format conversion	YCbCr ⇔ RGB conversion	Bidirectional conversion between YCbCr format and RGB format	
Dithering (tone reduction)	24 bpp	Full colors (16,777,216 colors)	Dithering not possible
	18 bpp	262,144 colors	Dithering not possible
	16 bpp	High colors (65,536 colors)	
	12 bpp	4,096 colors	
	8 bpp	256 colors	
Maximum image size	5M pixels	2560 pixels × 1920 lines	
Minimum image size	16 × 16 pixels	16 pixels × 16 lines	

Note: The scaling factor of the filter can be set between 1/16 and 8. For details, see section 30.7.11, VEU2H Resize Filter Control Register (V0RFCR, V1RFCR), and section 30.7.12, VEU2H Resize Filter Size Clip Register (V0RFSR, V1RFSR), in the SH7723 Hardware Manual.

Table 26.5 Simultaneous Usage of Functions in One VEU2H Activation

	Bundle Mode	Color Conversion	Low-Pass Filter	Deblocking Filter	Median Filter	FIR Filter	Enhancer	Vertical/ Horizontal Inversion	90°/270° Rotation	Scale-Up/ Scale-Down
Bundle Mode	—	O	×	×	×	×	O	O	×	O*2
Color Conversion	O	—	O	O	O	O	O	O	O	O
Low-Pass Filter	×	O	—	×	×	×	×	O	O	×
Deblocking Filter	×	O	×	—	O*1	×	×	O	O	×
Median Filter	×	O	×	×*1	—	×	×	O	O	×
FIR Filter	×	O	×	×	×	—	×	O	O	×
Enhancer	O	O	×	×	×	×	—	O	×	O
Vertical/ Horizontal Inversion	O	O	O	O	O	O	O	—	O	O
90°/270° Rotation	×	O	O	O	O	O	×	O	—	×
Scale-Up/ Scale-Down	O	O	×	×	×	×	O	O	×	—

[Legend]

O: Possible

×: Not possible

Figure 26.3 shows a block diagram of the VEU2H.

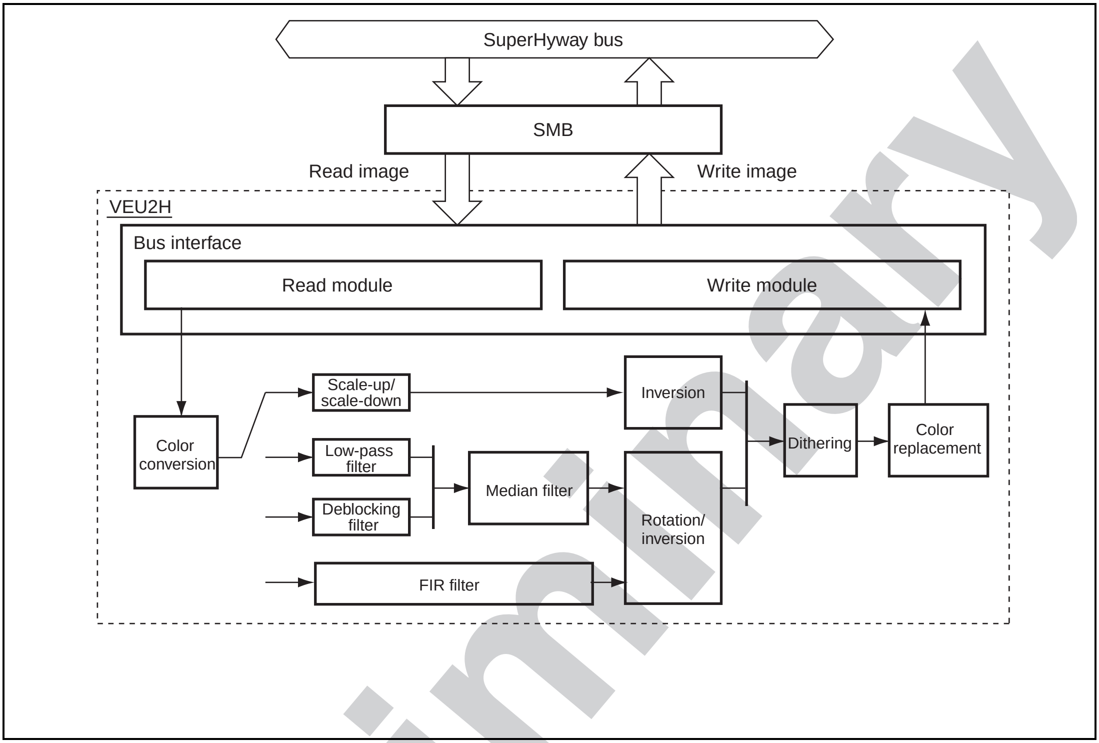


Figure 26.3 Block Diagram of VEU2H

Note: In figure 26.3, inversion indicates horizontal or vertical inversion, and rotation indicates 90° or 270° rotation.
In the inversion circuit after scale-up/scale-down, horizontal inversion, vertical inversion, or 180° rotation, which is a combination of the two types of inversion, can be performed.
In the rotation/inversion circuit after the median filter, in addition to the possible operations in the inversion circuit after scale-up/scale-down, 90° rotation, 270° rotation, a combination of 90° rotation and horizontal inversion, or a combination of 90° rotation and vertical inversion can be performed.

26.5 Functional Overview of BEU

The functional overview of the BEU (Blending Engine Unit) is shown in table 26.6.

Table 26.6 Functional Overview of BEU

Classification	Item	Function	Description	Note
Input format	YCbCr format	YCbCr 4:4:4/4:2:2/4:2:0 αYCbCr 4:4:4/4:2:2/4:2:0	α, Y, and C are input from separate planes For YCbCr 4:2:0, the vertical line is read twice	
	RGB format	RGB pack		
Output format	YCbCr format	YCbCr 4:4:4/4:2:2/4:2:0	Y and C are output to separate planes	
	RGB format	RGB pack	RGB pack output	
Source/ destination image size	Maximum	5M pixels (2560 × 1920)	Can be specified in 4-pixel units	
	Minimum	4 × 4 pixels: Parent display 4 × 4 pixels: Child display		
Dithering	Dithering (tone reduction)	24 bpp	Full colors (16,777,216 colors)	Dithering not possible
		18 bpp	262,144 colors	Dithering not possible
		16 bpp	High colors (65,536 colors)	
		12 bpp	4,096 colors	
		8 bpp	256 colors	

Classification	Item	Function	Description	Note
Blending	PinP	Three planes (two video image planes and OSD/Graphic) are blended.	• Any of the three inputs can be used as the parent display • The three displays can be blended at desired locations • Overflow from the parent display area is allowed, but the overflowed area is not output • The tile pattern can be blended • Transparent color can be specified for input systems 1 to 3*[2]	*[1]
OSD	Data format	8 bpp		
	CLUT size	32-bit αRGB 32-bit αYCbCr		
Raster operation 2		Three types of drawing color processing	Addition, replacement, and subtraction	
Multiwindow function		Four windows	Four windows are overlaid on the blended three planes	• Image size can be specified only in 4-pixel units • Overlapping between windows is prohibited
Display data output	Destination setting	Output system + write back to memory	Outputting display data to an output system is done simultaneously with writing the data back to memory	
	Interlace	Automatic field output at NTSC output	Addresses of even-numbered lines and odd-numbered lines are switched automatically	

Notes: 1. When the format for reading images is set to the RGB format, the source image also has to be in the RGB format. Likewise, when the format for reading images is set to the YCbCr format, the source image also has to be in the YCbCr format. However, input system 1 can use either the RGB format or YCbCr format as the source image format, regardless of the selected format for reading images. Therefore, if the source image format differs from the format for reading images, color conversion must be performed in input system 1. The pack form can be specified independently for each input system.

2. The transparent color can be specified for RGB565, RGB666, RGB888, and YCbCr input formats.

Figure 26.4 shows a block diagram of the BEU.

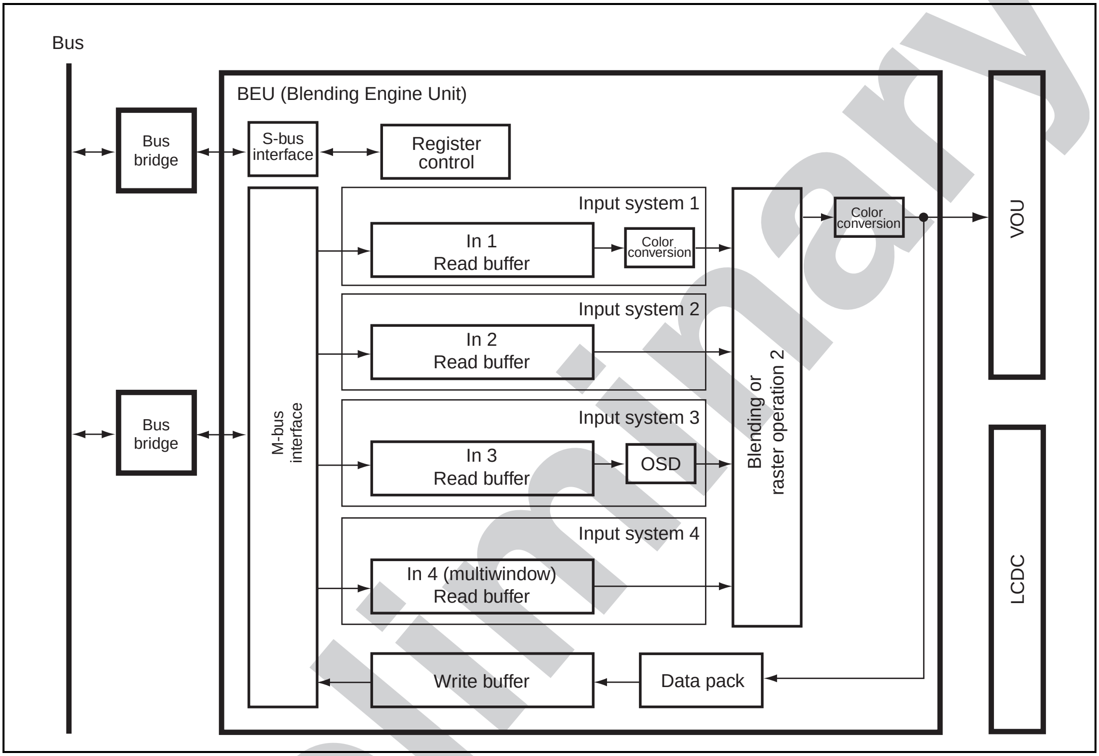


Figure 26.4 Block Diagram of BEU

Section 27 2DG

27.1 Basic Functions

27.1.1 Basic Functions

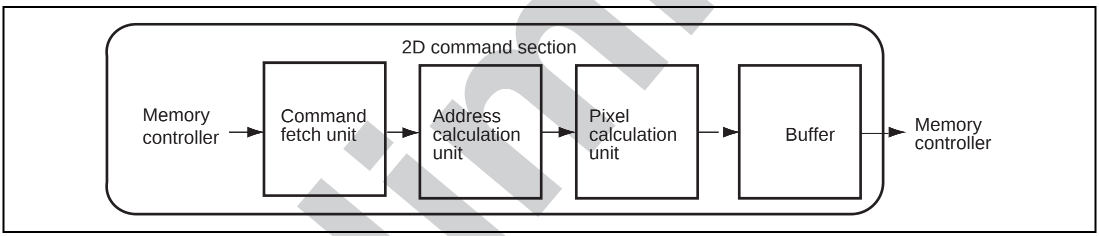
(1) Features

- Extended 2D functions

  High-functional bold line drawing, antialias line drawing, and BITBLT type commands with ROP/alpha blending
- Upgraded control command functions

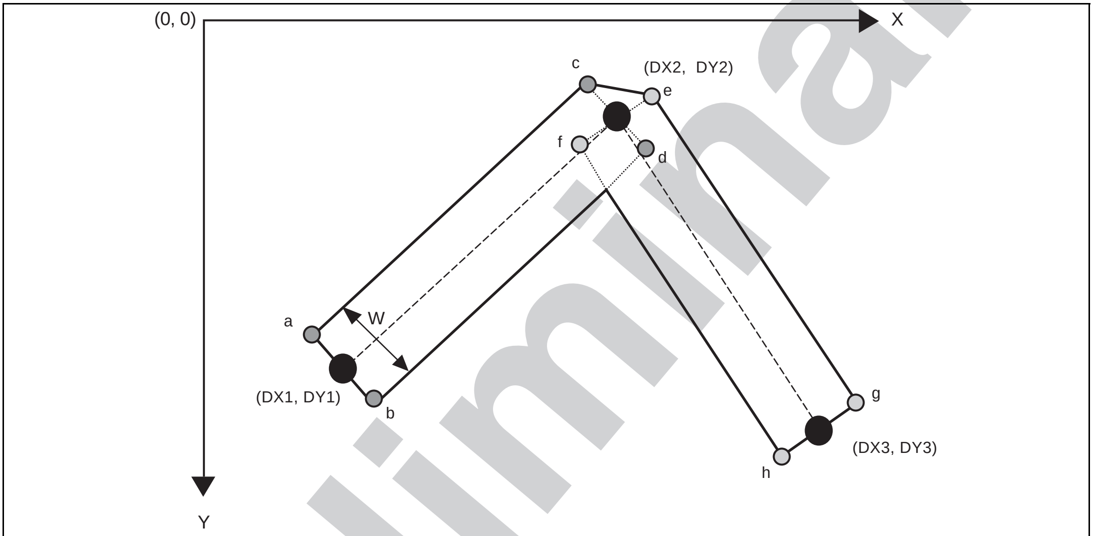
  Two command systems: GOSUB/RET and INT command, and upgraded WPR and TRAP command functions

(2) 2DG Block Diagram



(3) Bold Line Drawing

A bold line can be drawn by setting a value greater than 0 as line width W in a LINE type or RLINE type command. The bold line coordinates a, b, c, and d are obtained from the starting and final coordinate points and line width W, and the bold line drawn. W is set in the 6-bit integer part. When 0 is set in W, a line of line width 1 is drawn. The connection drawing mask bit (COM) in the rendering control register (RCLR) is used to select whether the linkage parts of bold lines are drawn or not. When the starting and final coordinate points of a line segment match in bold line drawing, nothing is drawn.



(4) Antialiasing

Antialiasing which reduces alias can be used in a LINEA/B/C/D, RLINEA/B/C/D or 3DLINE command.

For LINEA/B/C/D commands and RLINEA/B/C/D commands, antialiasing is performed by setting the rendering attribute AA (antialias enable) bit to 1.

- For a dashed line in LINEA/B or RLINEA/B command, antialiasing is not performed for the gaps in the dashed line.
- When the starting and final coordinate points of a line segment match in the LINEA, LINEB, LINEC, RLINEA, RLINEB, or RLINEC command, a single dot is drawn for a 1-bit-wide line (W = 0) without antialiasing and nothing is drawn for bold line drawing.

- When the starting and final coordinate points of a line segment match in the LINED or RLINED command, nothing is drawn.
- Antialiasing is not performed for horizontal, vertical, and 45-degree diagonal line segments in the LINEA, LINEB, LINEC, RLINEA, RLINEB, or RLINEC command.
- Antialiasing is not performed for horizontal and vertical line segments in the LINED or RLINED command.

Figure 27.1 Example of Antialias Specification

Section 28 LCD Controller (LCDC)

The LCD controller (LCDC) reads display data from an external memory or receives display data from the blend engine unit (BEU). The LCDC uses the palette memory to determine the colors according to the settings and then sends the data to the LCD module. This LCDC allows connection of TFT LCD modules that support the RGB interface or the 80-Series CPU's bus interface (SYS interface). (However, LCD modules with the NTSC/PAL type or LVDS interface cannot be connected.)

28.1 Features

The LCDC has the following features.

- Supports TFT LCD modules
- LCD module interface
  RGB interface (8/9/12/16/18/24-bit bus width)
  80-Series CPU's bus interface (SYS interface, 8/9/12/16/18/24-bit bus width)
- SYS interface supports the input/output mode for VSYNC
- Supports 8/12/16/18/24-bpp display image data formats
- Display image data is read in continuous or one-shot mode: continuous mode where display image data is continuously read according to the refresh rate of the LCD module and one-shot mode where display image data is read at intervals of the frame rate.
- Display image data is read in full or partial screen mode: full screen mode where the size of the display image data to be read depends on the panel size of the LCD module and partial screen mode where the size of the display image data to be read depends on the size of the screen to be updated.
- Display image data can be written back to the external memory
- Each of the RGB colors can be corrected by the 256-entry, 24-bit-input/output internal color palette memory
- Supports inversion of output signals to agree with the LCD module's signal polarity
- Interrupts can be generated every frame or user-specified line
- YCbCr signals are read and converted into RGB signals for output to the LCD module
- Supports YCbCr output function mode

Table 28.1 shows the LCDC functions.

Table 28.1 LCDC Functions

		Function	Remakes
Input data format	8 bpp	RGB 332	
	12 bpp	RGB 444	
	16 bpp	RGB 565	
	18 bpp	RGB 666	
		BGR 666	
	24 bpp	RGB 888	
		BGR 888	
	YCbCr	YCbCr 4:2:0, 4:2:2, 4:4:4	
Output data format	RGB interface	RGB8	3 cycle/pixel
		RGB9	2 cycle/pixel
		RGB12a	2 cycle/pixel
		RGB12b	1 cycle/pixel
		RGB16	1 cycle/pixel
		RGB18	1 cycle/pixel
		RGB24	1 cycle/pixel
	SYS interface	SYS8a	3 cycle/pixel
		SYS8b	3 cycle/pixel
		SYS8c	3 cycle/pixel
		SYS8d	2 cycle/pixel
		SYS9	2 cycle/pixel
		SYS12	2 cycle/pixel
		SYS16a	1 cycle/pixel
		SYS16b	2 cycle/pixel
		SYS16c	2 cycle/pixel
		SYS18	1 cycle/pixel
		SYS24	1 cycle/pixel
	Display data write-back	WB8a	• Packed format available • Write-back operation in units of 32 bits • Byte or word swap
		WB8d	
		WB9	
		WB16	
		WB18	
		WB24	
	YCbCr output	YCbCr 4:2:2	

		Function	Remakes
LCD driver interface	RGB interface	Interface with HSYNC and VSYNC • Polarity inversion • Output pulse width and position setting	
	SYS interface	80-Series bus interface • Support of VSYNC input/output	
Dot clock	Source clock	Bus clock, peripheral clock, external clock	
	Division ratio	n/m m = 60, 54, 48, 42 $1 \leq n \leq m/3, m/2$	
Interrupt	User setting	Interrupt generated when reading of specified lines of data is completed	
	Frame	Interrupt generated when the first pixel data of a frame starts to be output	
		Interrupt generated when output of the last pixel data of a frame is completed	
	VRAM read	Interrupt generated when access to a frame of data in VRAM is completed	
		Interrupt generated when access to a line of data in VRAM is completed	
	VSYNC	Interrupt generated when VSYNC is asserted	
		Interrupt generated when VSYNC is negated	
Display image	Image data read	Image data read depending on the refresh rate of LCD module	
		Image data read depending on the frame rate of display image	
	Display image size	Full screen	
		Only the specified area is updated.	
	Image data processing	Each color of R, G, and B is converted using the color palette • 256 entries • 24-bit input/output	
Format conversion	YCbCr to RGB	YCbCr data is converted into RGB for output.	

Figure 28.1 is a block diagram of the LCDC.

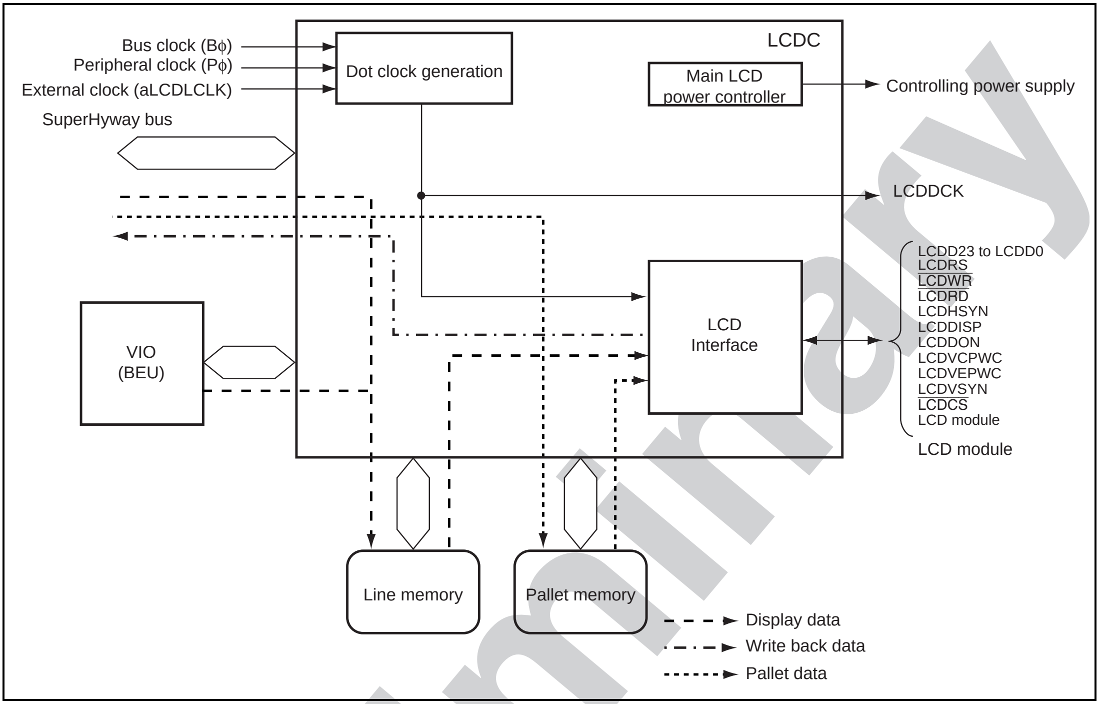


Figure 28.1 Block Diagram of LCDC

28.2 Input/Output Pins

Table 28.2 shows the pin configuration of the LCDC.

Table 28.2 Pin Configuration

Name	Function	I/O	Description
LCDDON	Display on signal	Output	Display start signal (DON)
LCDVCPWC	Power control	Output	Main LCD module power control (V_{CC})
LCDVEPWC	Power control	Output	Main LCD module power control (V_{EE})
LCDDCK/ $\overline{\text{LCDWR}}$	Dot clock/ write strobe	Output	Dot clock signal (RGB interface)/write strobe signal (SYS interface)
LCDVSYN	Vertical sync signal	Output/ I/O	Vertical sync signal (VSYNC) for main LCD (output for RGB interface, I/O for SYS interface, or output for YCbCr output mode)
LCDHSYN/ $\overline{\text{LCDCS}}$	Horizontal sync signal/chip select	Output	Horizontal sync signal (RGB interface and YCbCr output mode)/chip select signal for main LCD (SYS interface)
LCDDISP/ LCDRS	Display enable/ Register select	Output	Display enable signal (RGB interface)/register select signal (SYS interface)
$\overline{\text{LCDRD}}$	Read strobe	Output	Read strobe signal (SYS interface)
LCDD23 to LCDD0	LCD data bus	Output/ I/O	LCD panel data (output for RGB interface, I/O for SYS interface, or output for YCbCr output mode)
LCDLCLK	Input clock	Input	LCD source clock (external input)

Section 29 Video Output Unit (VOU)

The video output unit (VOU) converts image data that is obtained from the blend engine unit (BEU) or memory and outputs it as ITU-R BT.601 or ITU-R BT.656 digital data.

The VOU also scales up images.

29.1 Features

The VOU has the following features.

- Supported video system: NTSC
- Output digital level: Conforms to ITU-R BT.601, ITU-R BT.656
- Output interface: 16-bit Y/C interface, 8-bit multiplexed YC interface
- Output timing: 13.5 MHz in 16-bit Y/C interface, 27 MHz in 8-bit multiplexed YC interface
- Output pixel frequency: 13.5 MHz, 27 MHz
- Supported source image: sub-QCIF, QVGA, WQVGA, VGA
- Maximum destination image size: 720 × 240 per field
- Source image format: YCbCr 4:2:2, YCbCr 4:2:0, YCbCr 4:4:4, RGB
- Scaling up of images
  Horizontal factor: 1, 1.125, 2, 2.25, or 4
  Vertical factor: 1, 2, or 4
- RGB → YCbCr conversion function: Outputs YCbCr after converting obtained RGB data
- Double-buffered register: Efficient register access through a double-buffered mechanism

Note: The image is enlarged by 4 pixels in the horizontal and vertical directions.

Figure 29.1 shows a block diagram of the VOU.

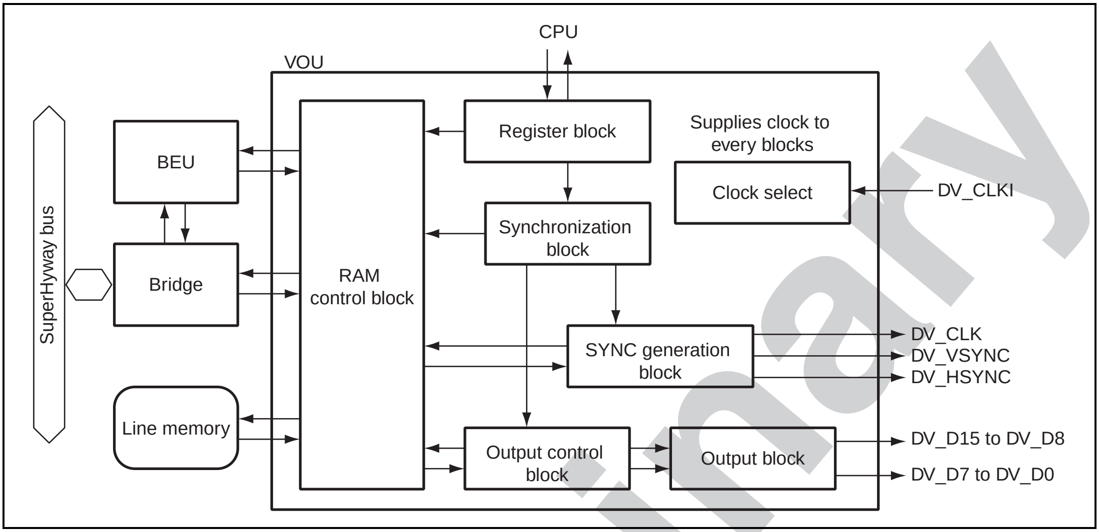


Figure 29.1 VOU Block Diagram

29.2 Pin Configuration

The VOU pin configuration is shown in table 29.1.

Table 29.1 Pin Configuration

Name	Function	I/O	Description
DV_CLK	Pixel clock output	Output	Pixel clock output (13.5 MHz, 27 MHz)
DV_VSYNC	Vertical sync signal	Output	VOU vertical sync signal output
DV_HSYNC	Horizontal sync signal output	Output	VOU horizontal sync signal output
DV_D15 to DV_D8	Data output	Output	Upper pixel data (Y: 16-bit interface) (YC: 8-bit multiplexed YC interface) (Rec. 656 output)
DV_D7 to DV_D0	Data output	Output	Lower pixel data (C: 16-bit interface) (0: 8-bit multiplexed YC interface) (0: Rec. 656 output)
DV_CLKI	Video clock input	Input	Video clock input pin (27 MHz)

Section 30 Media RAM (MERAM)

This LSI has a 128-Kbyte media RAM (MERAM). Up to 32 interconnect buffers (ICB) can be defined on the MERAM. Each ICB functions as a read buffer or write buffer for transactions of an image module, and also allows data transmission/reception between image modules through the ICB. The use of ICBs enables the number of accesses to the SDRAM to be reduced and the access efficiency to be improved.

Furthermore, by combining multiple areas in the MERAM, it can be defined as a frame buffer cache. When the LCDC accesses data through the frame buffer cache, the data is cached and the second access and the following accesses are made from the MERAM, which reduces accesses to the SDRAM.

Accesses from the following modules are supported: CEU, two VEUs, BEU, VPU, VOU, and LCDC

Note: When using any of these modules, set the MSTP221 bit in MSTPCR2 to 0 even when the interconnect buffer function is not used. To use the interconnect buffer function, also set the MSTP000 bit in MSTPCR0 to 0.

30.1 Features

(1) Features of Interconnect Buffers (ICB)

- Up to 32 buffers can be defined.
- Each ICB functions as a read buffer, which prefetches data from the specified area of the SDRAM and then stores the data in the buffer according to read transactions from a module. The ICB can also start reading before a transaction from the module occurs.
- Each ICB also functions as a write buffer, which receives write transactions from a module and stores them in the buffer. Whether to write data back to the SDRAM or not is selectable.
- The write buffer for a module can be used as the read buffer for another module, which allows data transfer in the MERAM. Data write to the SDRAM is also possible.

(2) Features of Frame Buffer Cache

- An area of combined ICBs can be defined as a frame buffer cache.
- Data from the frame buffer within the SDRAM is supplied to the LCDC while also being used to fill the frame buffer cache. When the data doesn’t change, data is simply supplied from the frame buffer to the LCDC.

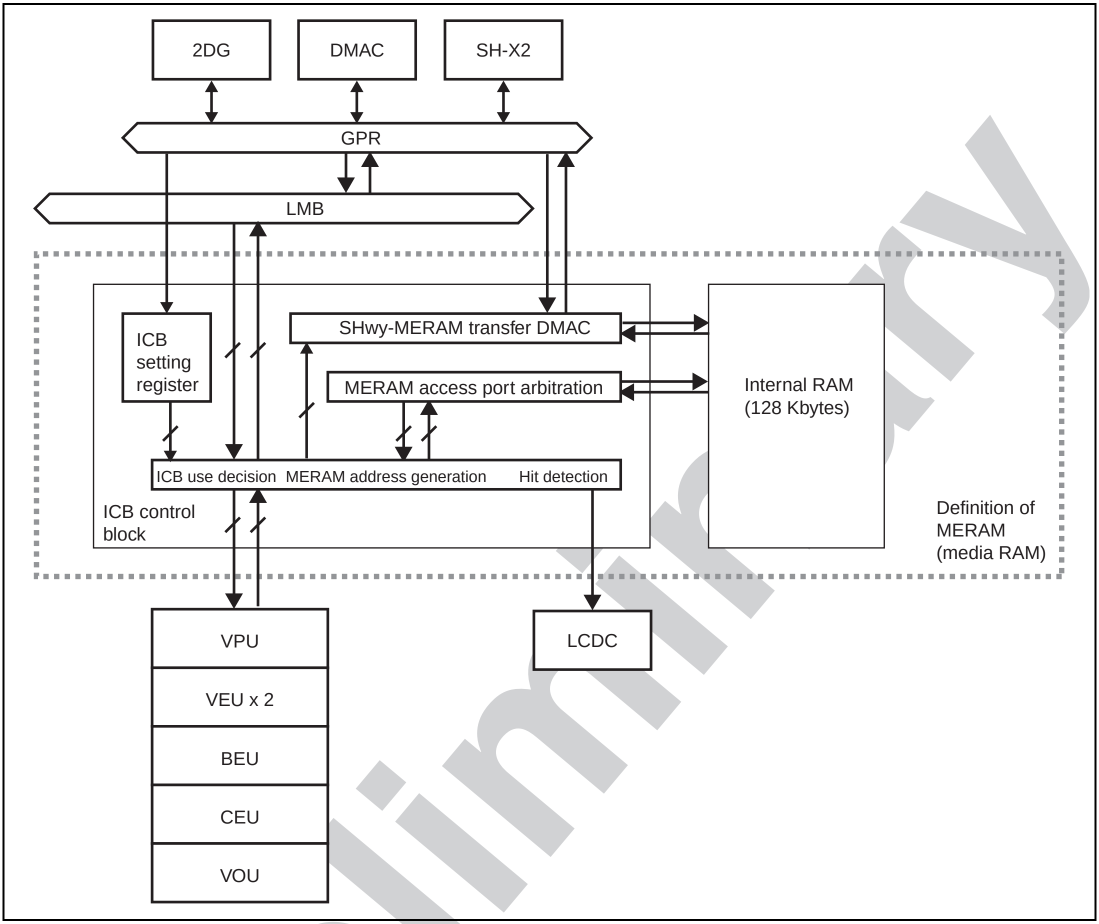


Figure 30.1 Relationship between MERAM and Other Modules

Section 31 TS Interface (TSIF)

The transport stream interface (TSIF) is a module for receiving the MPEG2 transport stream (TS) used in one-segment broadcasting implemented as part of the digital terrestrial broadcasting services. The TSIF extracts packet data and controls PCR, which are required to decode the system layer of the MPEG2 standard.

31.1 Features

The TSIF has the following features.

- Serial data input
- Support for TS data transfer by DMA auto request
- Acquisition of TS packets
  - Filters 38 kinds of PIDs (Packet ID) in total (The PID values of PAT and CAT packets are fixed. For PCR, video, and audio packets, the PID values are predefined.)
  - Supports all valid packet receive mode (Null packet is deleted).
  - Supports all packet receive mode including Null packet.
  - Supports duplicate packet delete mode.
  - The endian type at the TS packet data reading can be set.
  - Supports the time stamp function at the TS packet data acquisition.
- TS data analysis
  - Detects random access indicator.
  - Detects discontinuity indicator.
  - Detects video start code and short header.
- Extraction of PCR information
- Support for system clock generation

[Legend]

MPEG: Moving picture expert group

TS: Transport stream

PID: Packet ID

PAT: Program association table

CAT: Conditional access table

PCR: Program clock reference

ES: Elementary stream

Figure 31.1 shows a block diagram of the TSIF.

The signals to transfer or control TS data are input as an input signal, and the TS packet data filtered by this module will be output as an output signal.

The serially input TS data is converted into 8-bit parallel data and the header of the TS packet is detected by the TS synchronous detection circuit. The TS filter circuit then determines and filters the PID of the TS packet according to the predefined PID table and stores the TS packet in the buffer for TS packets. Following these processes, only predefined TS packets are stored in the buffer and transferred to memories via a bus interface.

The analysis circuit of a TS header is a block that analyses the header of a TS packet, acquires the header information, and generates a trigger signal sent to other blocks. The ES data search circuit searches the start code and short header of an elementary stream (ES) contained in a TS packet. This result can be used as supplementary data to control the start timing of image decoding through the upper-level software that controls image decoding.

Based on the PCR information extracted from the TS packet, the PCR control unit outputs information needed for system clock control.

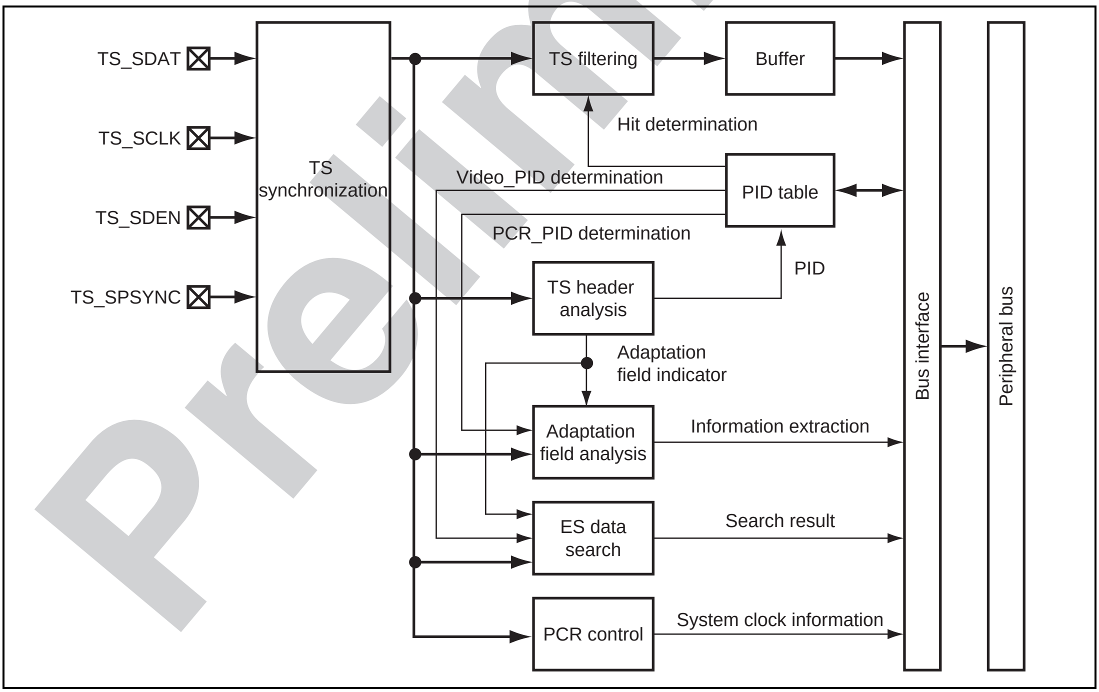


Figure 31.1 TSIF Block Diagram

31.2 Input/Output Pins

Table 31.1 shows the pin configuration.

Table 31.1 Pin Configuration

Pin Name	Function	I/O	Description
TS_SDAT	TS serial data	Input	Serial input pin of TS packet data Polarity inversion is enabled by register setting.
TS_SCK	TS serial clock	Input	Serial input clock pin Polarity inversion is enabled by register setting. The initial value is synchronized with the rising edge.
TS_SDEN	TS data enable	Input	Serial input enable signal pin Polarity inversion and On/Off setting are enabled by register setting. The initial value is On and enabled after the TS_SDEN signal is driven high.
TS_SPSYNC	TS data synchronization	Input	Byte boundary signal pin Polarity inversion is enabled by register setting. The initial value is set on a byte boundary at the rising edge.

Section 32 Sound Interface Unit (SIU)

Note: This section contains references to the SH7723 Hardware Manual. The contents of the SH7723 Hardware Manual will be disclosed upon acceptance of a confidentiality agreement. For details, please contact a Renesas Technology sales representative.

The sound interface unit (SIU) is a serial interface unit with FIFO which has an interface for sound input and output to be connected with the D/A and A/D converters, and it inputs/outputs PCM data and inputs digital data conforming to the IEC60958 (SPDIF: version of December, 1999). The SIU has a DSP dedicated for filter processing, and signal processing operation of the filter application can be performed by a DSP program.

32.1 Features

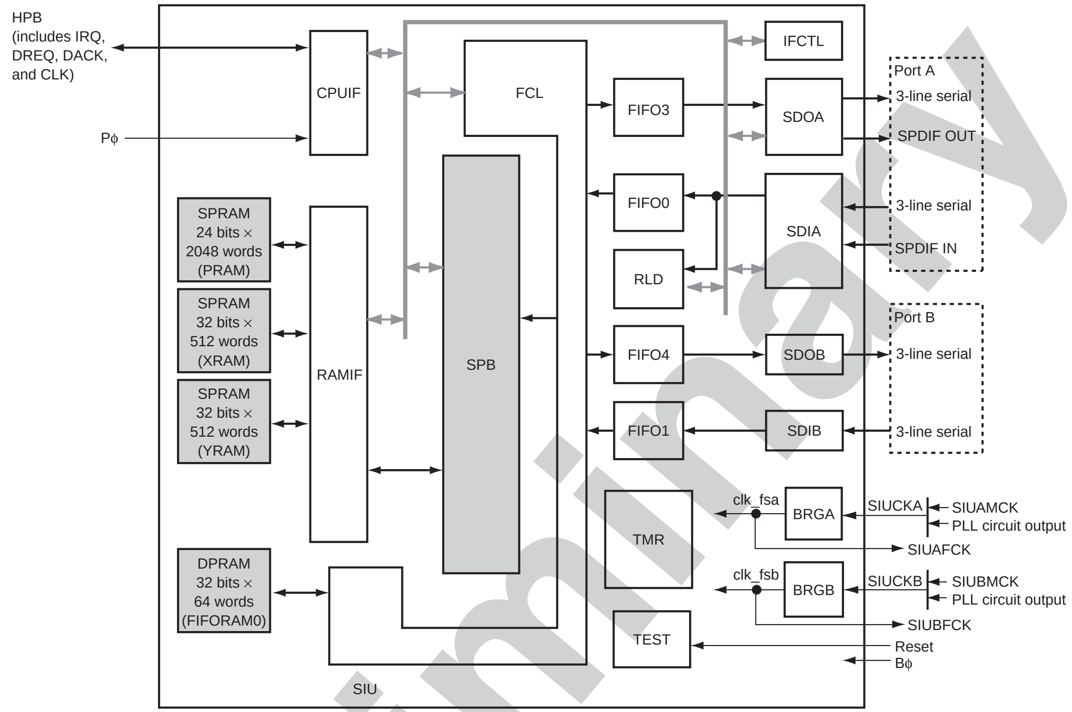
The features of the SIU are listed in table 32.1.

Table 32.1 SIU Functions

Item	Contents	Details
DSP functions	Memory	• PRAM: 24 bits × 2048 words • XRAM: 32 bits × 512 words • YRAM: 32 bits × 512 words
	Operators	• 24-bit × 24-bit multiplier • 16-bit divider • 42-bit ALU • General operator for pointers
	Special instructions	• Branch instruction with reference of flag at desired bit location • Instruction to set desired bit location • Instruction to reset desired bit location • Maximum value search instruction • Clipping instruction
	Special control	• Instruction loop • Modulo addressing • Subroutine
	FIFO control	On-chip FIFO control circuit

Item	Contents	Details
DSP functions	Applications	• FIR filter • IIR filter • Equalizer • SRC (sampling rate conversion)
Output interface	3-line serial output (× 2: ports A and B)	• Master mode, clock = 64, 128, 256, or 512 × fs (sampling frequency) • Supports slave mode • 32 or 64 bit/fs • 16-bit front filling or end filling at 64 bit/fs • Supports I2S (Inter IC Sound) format
	SPDIF output (port A)	• Master mode, clock = 512 × fs • Supports channel status and user data • Supports only 16-bit stereo
Input interface	3-line serial input (× 2: ports A and B)	• Master mode, clock = 64, 128, 256, or 512 × fs • Supports slave mode • 32 or 64 bit/fs • 16-bit front filling or end filling at 64 bit/fs • Supports I2S format
	SPDIF input (port A)	• Master mode, clock = 512 × fs • Supports channel status and user data • Supports only 16-bit stereo
Others	Volume	Supports digital volume
	Mixing	L/R mixing

Figure 32.1 shows a block diagram of the SIU.



[Legend]

CPUIF: CPU interface
FCL: FIFO control
IFCTL: Interface control
SDOA: Serial data through port A
SDIA: Serial data/SPDIF data input through port A
SDOB: Serial data output through port B
SDIB: Serial data input through port B
RLD: Record level detector
SPB: Sound processing block
TMR: Timer block
TEST: Testing block
RAMIF: RAM interface
BRGA: Baud rate generator A
BRGB: Baud rate generator B

Note: In this product, port A corresponds to external pins SIUA***, and port B corresponds to external pins SIUB***. For details on multiplexed pins, see the pin list of this product.

Figure 32.1 Block Diagram of SIU

The SIU operates in the following 18 blocks and four SRAMs.

(1) CPUIF

The CPU interface (CPUIF) is an interface that controls access to the registers and data transfer between the CPU that functions as the host and SRAM (PRAM, XRAM, YRAM, and FIFORAM0) controlled by the SIU. It is connected to the SH peripheral bus (HPB). The SIU operates according to the program written in PRAM via the CPUIF.

(2) FCL

The FIFO control (FCL) is a block that controls FIFOs for input/output data of ports A and B. The FCL automatically controls the FIFORAM addresses to write each FIFO data at the predetermined location and read data from the predetermined location.

(3) FIFO0, FIFO1, FIFO3, and FIFO4

The FIFOs store SPDIF input/output data, 3-line serial input/output data.

Each FIFO has its own use as shown below.

- FIFO0: Data input from port A is temporarily stored.
- FIFO1: Data input from port B is temporarily stored.
- FIFO3: Data to be output to port A is temporarily stored.
- FIFO4: Data to be output to port B is temporarily stored.

(4) IFCTL

The interface control (IFCTL) controls SPDIF input/output and 3-line serial input/output, according to the settings of the host.

(5) SDOA

The SDOA is an interface for serial data output through port A. 3-line serial data and SPDIF data can be output. The SDOA should be mainly used to output audio stereo data.

(6) SDIA

The SDIA is an interface for serial data input and SPDIF data input of port A. 3-line serial data and SPDIF data can be input. The SDIA should be mainly used to input audio stereo data.

(7) SDOB

The SDOB is an interface for serial data output through port B. 3-line serial data can be output. The SDOB should be mainly used to output audio monaural data.

(8) SDIB

The SDIB is an interface for serial data input through port B. 3-line serial data can be input. The SDIB should be mainly used to input audio monaural data.

(9) RLD

The record level detector (RLD) monitors the input level of port A, and is capable of fetching the peak level as an absolute value. The RLD incorporates a circuit for detecting the silent period, and can set a flag if a sound equal to or lower than the specified mute level continues for the specified sampling period.

(10) SPB

The sound processing block (SPB) is a block that plays the center role in SIU signal processing. It accesses PRAM for programs and XRAM and YRAM for saving data to implement signal processing. The SPB incorporates a DSP that operates by the program written in PRAM, and implements signal processing such as FIR filter, IIR filter, equalizer, or SRC.

(11) TMR

The timer block (TMR) generates the signal to activate the SPB hardware and the timer interrupt signal issued to the TSIF module. When the SPB hardware has been activated, the TMR is normally not used, and the FIFO event activation is used instead.

(12) TEST

The TEST is a module that generates a reset signal for the registers in each block.

(13) RAMIF

The RAM interface (RAMIF) is a module that controls input/output of RAM by switching between the host and internal control. Though the sound processing block (SPB) in the SIU has the privilege to access RAM during operation, the host control signal can be used to pass the privilege to access RAM to the host (CPUIF).

(14) BRGA

Baud rate generator A (BRGA) supplies SIUCKA directly or after dividing it as a basic operating clock to sound input/output port A. The SIUCKA dividing ratio can be specified by a register.

(15) BRGB

Baud rate generator B (BRGB) supplies SIUCKB directly or after dividing it as a basic operating clock to sound input/output port B. The SIUCKB dividing ratio can be specified by a register.

32.1.1 RAM Overview

(1) PRAM

PRAM is a single-port SRAM of 24 bits × 2048 words. It is used to store SIU programs consisting of 24-bit instructions, and the stored programs command the DSP in the SIU to carry out necessary signal processing.

(2) XRAM and YRAM

XRAM and YRAM are single-port SRAMs of 32 bits × 512 words. They store data such as audio samples or filter coefficients during processing such as filtering by the DSP in the SIU.

(3) FIFORAM0

FIFORAM0 is a dual-port SRAM of 32 bits × 64 words. Unlike audio data FIFOs (FIFO0, FIFO1, FIFO3, and FIFO4) for input/output outside the LSI, they are RAM FIFOs for audio data input/output from or to the CPU.

FIFORAM0 is divided into four 16-stage FIFOs; RAM port A input FIFO (FIFO5), RAM port B input FIFO (FIFO6), RAM port A output FIFO (FIFO7), and RAM port B output FIFO (FIFO8).

For details, refer to section 36.4, Memory Descriptions, and section 36.8.8, FIFO Specifications, in the SH7723 Hardware Manual.

32.2 Input/Output Pins

Table 32.2 shows the SIU pin configuration.

Table 32.2 Pin Configuration

SIU Block	Pin Name	Function	I/O	Description
SIUA	SIUAOLR	Port A sound output L/R clock	I/O*	Sound output L/R clock pin (master or slave)
	SIUAOBT	Port A sound output bit clock	I/O*	Sound output bit clock pin (master or slave)
	SIUAOSLD	Port A sound output serial data	Output	Sound output serial data pin
	SIUAOSPD	SPDIF output A serial data	Output	SPDIF serial data pin
	SIUAILR	Port A sound input L/R clock	I/O*	Sound input L/R clock pin (master or slave)
	SIUAIBT	Port A sound input bit clock	I/O*	Sound input bit clock pin (master or slave)
	SIUAISLD	Port A sound input serial data	Input	Sound input serial data pin
	SIUAISPD	Port A SPDIF input data	Input	SPDIF input serial data pin
	SIUAMCK	Port A master clock input	Input	Master clock input pin for port A
	SIUAFCK	Port A audio clock output	Output	Audio clock (clk_fsa) output pin for port A
SIUB	SIUBOLR	Port B sound output L/R clock	I/O*	Sound output L/R clock pin (master or slave)
	SIUBOBT	Port B sound output bit clock	I/O*	Sound output bit clock pin (master or slave)
	SIUBOSLD	Port B sound output serial data	Output	Sound output serial data pin
	SIUBILR	Port B sound input L/R clock	I/O*	Sound input L/R clock pin (master or slave)
	SIUBIBT	Port B sound input bit clock	I/O*	Sound input bit clock pin (master or slave)
	SIUBISLD	Port B sound input serial data	Input	Sound input serial data pin

SIU Block	Pin Name	Function	I/O	Description
SIUB	SIUBMCK	Port B master clock input	Input	Master clock input pin for port B
	SIUBFCK	Port B audio clock output	Output	Audio clock (clk_fsb) output pin for port B

Note: * Set to output when the master is specified or set to input when the slave is specified.

Section 33 ATAPI

33.1 General Description

The ATAPI interface provides both the ATA and ATAPI physical interfaces. This device also supports both the ATA task and ATAPI packet commands.

33.2 Features

- Supporting primary channel
- Supporting master/slave
- Supporting 3.3 V I/O interface
- Supporting PIO modes 0 to 4, the multiword DMA modes 0 to 2, and the Ultra DMA modes 0 to 4
- Supporting descriptor mode

Section 34 Pin Function Controller (PFC)

34.1 Overview

The pin function controller (PFC) consists of registers to select the functions of the general port and multiplexed pins. Pin functions and I/O directions can be individually selected for every pin regardless of the LSI operating mode.

Table 34.1 lists the multiplexed pins of this LSI. Functions are selectable from a general port, functions 1, 2, and 3 for each pin. For the multiplexed pins with function 1 only, function 1 can be selected by setting the port control register to enable the pin multiplex function. For the multiplexed pins with functions 1, 2, and 3, one of the functions can be selected by setting the port control register and by selecting the function using the pin select register.

The functions in the shaded area in the table are available immediately after a reset. The settings of the I/O buffer Hi-Z control registers have priorities over the setting of the port control register.

Table 34.1 Multiplexed Pins

General Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)
PTA7 input/output	D23 input/output (BSC)	KEYOUT2 output (KEYSC)	—
PTA6 input/output	D22 input/output (BSC)	KEYOUT1 output (KEYSC)	—
PTA5 input/output	D21 input/output (BSC)	KEYOUT0 output (KEYSC)	—
PTA4 input/output	D20 input/output (BSC)	KEYIN4 input (KEYSC)	—
PTA3 input/output	D19 input/output (BSC)	KEYIN3 input (KEYSC)	—
PTA2 input/output	D18 input/output (BSC)	KEYIN2 input (KEYSC)	—
PTA1 input/output	D17 input/output (BSC)	KEYIN1 input (KEYSC)	—
PTA0 input/output	D16 input/output (BSC)	KEYIN0 input (KEYSC)	—
PTB7 input/output	D31 input/output (BSC)	—	—
PTB6 input/output	D30 input/output (BSC)	—	—
PTB5 input/output	D29 input/output (BSC)	—	—
PTB4 input/output	D28 input/output (BSC)	—	—
PTB3 input/output	D27 input/output (BSC)	—	—

General Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)
PTB2 input/output	D26 input/output (BSC)	KEYOUT5/IN5 input/output (KEYSC)	—
PTB1 input/output	D25 input/output (BSC)	KEYOUT4/IN6 input/output (KEYSC)	—
PTB0 input/output	D24 input/output (BSC)	KEYOUT 3 output (KEYSC)	—
PTC7 input/output	IDED15 input/output (ATAPI)	$\overline{\text{SDHI1CD}}$ input (SDHI1)	—
PTC6 input/output	IDED14 input/output (ATAPI)	SDHI1WP input (SDHI1)	—
PTC5 input/output	IDED13 input/output (ATAPI)	SDHI1D3 input/output (SDHI1)	—
PTC4 input/output	IDED12 input/output (ATAPI)	SDHI1D2 input/output (SDHI1)	—
PTC3 input/output	IDED11 input/output (ATAPI)	SDHI1D1 input/output (SDHI1)	—
PTC2 input/output	IDED10 input/output (ATAPI)	SDHI1D0 input/output (SDHI1)	—
PTC1 input/output	IDED9 input/output (ATAPI)	SDHI1CMD input/output (SDHI1)	—
PTC0 input/output	IDED8 input/output (ATAPI)	SDHI1CLK output (SDHI1)	—
PTD7 input/output	IDED7 input/output (ATAPI)	$\overline{\text{SDHI0CD}}$ input (SDHI0*1)	—
PTD6 input/output	IDED6 input/output (ATAPI)	SDHI0WP input (SDHI0*1)	—
PTD5 input/output	IDED5 input/output (ATAPI)	SDHI0D3 input/output (SDHI0*1)	—
PTD4 input/output	IDED4 input/output (ATAPI)	SDHI0D2 input/output (SDHI0*1)	—
PTD3 input/output	IDED3 input/output (ATAPI)	SDHI0D1 input/output (SDHI0*1)	—
PTD2 input/output	IDED2 input/output (ATAPI)	SDHI0D0 input/output (SDHI0*1)	—
PTD1 input/output	IDED1 input/output (ATAPI)	SDHI0CMD input/output (SDHI0*1)	—

General Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)
PTD0 input/output	IDED0 input/output (ATAPI)	SDHI0CLK output (SDHI0*[1])	—
PTE5 input/output	DIRECTION output (ATAPI)	SCIF5_SCK input/output (SCIF5*[4])	—
PTE4 input/output	$\overline{\text{EXBUF\_ENB}}$ output (ATAPI)	SCIF5_RXD input (SCIF5*[4])	—
PTE3 input/output	$\overline{\text{IDERST}}$ output (ATAPI)	SCIF5_TXD output (SCIF5*[4])	—
PTE2 input/output	$\overline{\text{IODACK}}$ output (ATAPI)	SCIF4_SCK input/output (SCIF4*[4])	—
PTE1 input/output	IODREQ input (ATAPI)	SCIF4_RXD input (SCIF4*[4])	—
PTE0 input/output	IDEIORDY input (ATAPI)	SCIF4_TXD output (SCIF4*[4])	—
PTF7 input/output	IDEINT input (ATAPI)	—	—
PTF6 input/output	$\overline{\text{IDEIOWR}}$ output (ATAPI)	$\overline{\text{MSIOF0\_SS2}}$ output (MSIOF0)	MSIOF0_RSYNC input/output (MSIOF0)
PTF5 input/output	$\overline{\text{IDEIORD}}$ output (ATAPI)	$\overline{\text{MSIOF0\_SS1}}$ output (MSIOF0)	MSIOF0_RSCK input/output (MSIOF0)
PTF4 input/output	$\overline{\text{IDECS1}}$ output (ATAPI)	MSIOF0_TSYNC input/output (MSIOF0)	—
PTF3 input/output	$\overline{\text{IDECS0}}$ output (ATAPI)	MSIOF0_TSCK input/output (MSIOF0)	—
PTF2 input/output	IDEA2 output (ATAPI)	MSIOF0_RXD input (MSIOF0)	—
PTF1 input/output	IDEA1 output (ATAPI)	MSIOF0_TXD output (MSIOF0)	—
PTF0 input/output	IDEA0 output (ATAPI)	MSIOF0_MCK input (MSIOF0)	—
PTG5 output	AUDCK output (AUD)	—	—
PTG4 output	AUDSYNC output (AUD)	—	—
PTG3 output	AUDATA3 output (AUD)	TPUTO3 output (TPU)	—
PTG2 output	AUDATA2 output (AUD)	TPUTO2 output (TPU)	—
PTG1 output	AUDATA1 output (AUD)	TPUTO1 output (TPU)	—

General Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)
PTG0 output	AUDATA0 output (AUD)	TPUTO0 output (TPU)	—
PTH7 input/output	LCDVCPWC input/output (LCDC)	—	—
PTH6 input/output	$\overline{\text{LCDRD}}$ output (LCDC)	DV_CLKI input (VOU)	—
PTH5 input/output	LCDVSYN input/output (LCDC)	DV_CLK output (VOU)	—
PTH4 input/output	LCDDISP output (LCDC)	LCDRS output (LCDC)	—
PTH3 input/output	LCDHSYN output (LCDC)	$\overline{\text{LCDCS}}$ output (LCDC)	—
PTH2 input/output	LCDDON output (LCDC)	—	—
PTH1 input/output	LCDDCK output (LCDC)	$\overline{\text{LCDWR}}$ output (LCDC)	—
PTH0 input/output	LCDVEPWC output (LCDC)	—	—
PTJ7 output	STATUS0 output (System)	—	—
PTJ5 output	PDSTATUS output (System)	—	—
PTJ3 input/output	A25 output (BSC)	—	—
PTJ2 input/output	A24 output (BSC)	—	—
PTJ1 input/output	A23 output (BSC)	—	—
PTJ0 input/output	A22 output (BSC)	—	—
PTK7 input/output	SIUAFCK output (SIU)	—	—
PTK6 input/output	SIUAILR input/output (SIU)	$\overline{\text{MSIOF1\_SS2}}$ output (MSIOF1)	MSIOF1_RSYNC input/output (MSIOF1)
PTK5 input/output	SIUAIBT input/output (SIU)	$\overline{\text{MSIOF1\_SS1}}$ output (MSIOF1)	MSIOF1_RSCK input/output (MSIOF1)
PTK4 input/output	SIUAISLD input (SIU)	MSIOF1_RXD input (MSIOF1)	—
PTK3 input/output	SIUAOLR input/output (SIU)	MSIOF1_TSYNC input/output (MSIOF1)	—
PTK2 input/output	SIUAOBT input/output (SIU)	MSIOF1_TSCK input/output (MSIOF1)	—
PTK1 input/output	SIUAOSLD output (SIU)	MSIOF1_TXD output (MSIOF1)	—
PTK0 input/output	SIUAMCK input (SIU)	MSIOF1_MCK input (MSIOF1)	—

General Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)
PTL7 input/output	LCDD15 input/output (LCDC)	DV_D15 output (VOU)	—
PTL6 input/output	LCDD14 input/output (LCDC)	DV_D14 output (VOU)	—
PTL5 input/output	LCDD13 input/output (LCDC)	DV_D13 output (VOU)	—
PTL4 input/output	LCDD12 input/output (LCDC)	DV_D12 output (VOU)	—
PTL3 input/output	LCDD11 input/output (LCDC)	DV_D11 output (VOU)	—
PTL2 input/output	LCDD10 input/output (LCDC)	DV_D10 output (VOU)	—
PTL1 input/output	LCDD9 input/output (LCDC)	DV_D9 output (VOU)	—
PTL0 input/output	LCDD8 input/output (LCDC)	DV_D8 output (VOU)	—
PTM7 input/output	LCDD7 input/output (LCDC)	DV_D7 output (VOU)	—
PTM6 input/output	LCDD6 input/output (LCDC)	DV_D6 output (VOU)	—
PTM5 input/output	LCDD5 input/output (LCDC)	DV_D5 output (VOU)	—
PTM4 input/output	LCDD4 input/output (LCDC)	DV_D4 output (VOU)	—
PTM3 input/output	LCDD3 input/output (LCDC)	DV_D3 output (VOU)	—
PTM2 input/output	LCDD2 input/output (LCDC)	DV_D2 output (VOU)	—
PTM1 input/output	LCDD1 input/output (LCDC)	DV_D1 output (VOU)	—
PTM0 input/output	LCDD0 input/output (LCDC)	DV_D0 output (VOU)	—
PTN7 input/output	LCDD23 input/output (LCDC)	SCIF5_SCK input/output (SCIF5*[4])	—
PTN6 input/output	LCDD22 input/output (LCDC)	SCIF5_RXD input (SCIF5*[4])	—

General Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)
PTN5 input/output	LCDD21 input/output (LCDC)	SCIF5_TXD output (SCIF5*[4])	—
PTN4 input/output	LCDD20 input/output (LCDC)	SCIF4_SCK input/output (SCIF4*[4])	—
PTN3 input/output	LCDD19 input/output (LCDC)	SCIF4_RXD input (SCIF4*[4])	—
PTN2 input/output	LCDD18 input/output (LCDC)	SCIF4_TXD output (SCIF4*[4])	—
PTN1 input/output	LCDD17 input/output (LCDC)	DV_VSYNC output (VOU)	—
PTN0 input/output	LCDD16 input/output (LCDC)	DV_HSYNC output (VOU)	—
PTQ3 input	AN3 input (ADC)	—	—
PTQ2 input	AN2 input (ADC)	—	—
PTQ1 input	AN1 input (ADC)	—	—
PTQ0 input	AN0 input (ADC)	—	—
PTR7 input/output	$\overline{\text{CS6B}}$/$\overline{\text{CE1B}}$ output (BSC)	—	—
PTR6 input/output	$\overline{\text{CS6A}}$/$\overline{\text{CE2B}}$ output (BSC)	—	—
PTR5 input/output	$\overline{\text{CS5B}}$/$\overline{\text{CE1A}}$ output (BSC)	—	—
PTR4 input/output	$\overline{\text{CS5A}}$/$\overline{\text{CE2A}}$ output (BSC)	—	—
PTR3 input	$\overline{\text{IOIS16}}$ input (BSC)	LCKLCLK input (LCDC)	—
PTR2 input	$\overline{\text{WAIT}}$ input (BSC)	—	—
PTR1 input/output	$\overline{\text{WE3}}$/$\overline{\text{ICIOWR}}$ output (BSC)	—	—
PTR0 input/output	$\overline{\text{WE2}}$/$\overline{\text{ICIORD}}$ output (BSC)	—	—
PTS7 input/output	SCIF1_SCK input/output (SCIF1*[2])	$\overline{\text{SDHI0CD}}$ input (SDHI0*[1])	—
PTS6 input/output	SCIF1_RXD input (SCIF1*[2])	SDHI0WP input (SDHI0*[1])	—
PTS5 input/output	SCIF1_TXD output (SCIF1*[2])	SDHI0D3 input/output (SDHI0*[1])	—
PTS4 input/output	$\overline{\text{SCIF3\_CTS}}$ input (SCIF3*[2])	SDHI0D2 input/output (SDHI0*[1])	—

General Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)
PTS3 input/output	$\overline{\text{SCIF3\_RTS}}$ output (SCIF3*[2])	SDHI0D1 input/output (SDHI0*[1])	—
PTS2 input/output	SCIF3_SCK input/output (SCIF3*[2])	SDHI0D0 input/output (SDHI0*[1])	—
PTS1 input/output	SCIF3_RXD input (SCIF3*[2])	SDHI0CMD input/output (SDHI0*[1])	—
PTS0 input/output	SCIF3_TXD output (SCIF3*[2])	SDHI0CLK output (SDHI0*[1])	—
PTT5 input/output	SCIF0_SCK input/output (SCIF0*[3])	MSIOF0_TSCK input/output (MSIOF0*[5])	—
PTT4 input/output	SCIF0_RXD input (SCIF0*[3])	MSIOF0_RXD input (MSIOF0*[5])	—
PTT3 input/output	SCIF0_TXD output (SCIF0*[3])	MSIOF0_TXD output (MSIOF0*[5])	—
PTT2 input/output	SCIF2_SCK input/output (SCIF2*[3])	MSIOF0_TSYNC input/output (MSIOF0*[5])	—
PTT1 input/output	SCIF2_RXD input (SCIF2*[3])	$\overline{\text{MSIOF0\_SS1}}$ output (MSIOF0*[5])	MSIOF0_RSCK input/output (MSIOF0)
PTT0 input/output	SCIF2_TXD output (SCIF2*[3])	$\overline{\text{MSIOF0\_SS2}}$ output (MSIOF0*[5])	MSIOF0_RSYNC input/output (MSIOF0)
PTU5 input/output	FCDE output (FLCTL)	SCIF0_SCK input/output (SCIF0*[3])	—
PTU4 input/output	FSC output (FLCTL)	SCIF0_RXD input (SCIF0*[3])	—
PTU3 input/output	$\overline{\text{FWE}}$ output (FLCTL)	SCIF0_TXD output (SCIF0*[3])	—
PTU2 input/output	FOE output (FLCTL)	SCIF2_SCK input/output (SCIF2*[3])	VIO_VD2 input (VIO)
PTU1 input/output	FRB input (FLCTL)	SCIF2_RXD input (SCIF2*[3])	VIO_CLK2 input (VIO)
PTU0 input/output	$\overline{\text{FCE}}$ output (FLCTL)	SCIF2_TXD output (SCIF2*[3])	VIO_HD2 input (VIO)
PTV7 input/output	NAF7 input/output (FLCTL)	SCIF1_SCK input/output (SCIF1*[2])	VIO_D15 input (VIO)
PTV6 input/output	NAF6 input/output (FLCTL)	SCIF1_RXD input (SCIF1*[2])	VIO_D14 input (VIO)

General Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)
PTV5 input/output	NAF5 input/output (FLCTL)	SCIF1_TXD output (SCIF1*2)	VIO_D13 input (VIO)
PTV4 input/output	NAF4 input/output (FLCTL)	$\overline{\text{SCIF3\_CTS}}$ input (SCIF3*2)	VIO_D12 input (VIO)
PTV3 input/output	NAF3 input/output (FLCTL)	$\overline{\text{SCIF3\_RTS}}$ output (SCIF3*2)	VIO_D11 input (VIO)
PTV2 input/output	NAF2 input/output (FLCTL)	SCIF3_SCK input/output (SCIF3*2)	VIO_D10 input (VIO)
PTV1 input/output	NAF1 input/output (FLCTL)	SCIF3_RXD input (SCIF3*2)	VIO_D9 input (VIO)
PTV0 input/output	NAF0 input/output (FLCTL)	SCIF3_TXD output (SCIF3*2)	VIO_D8 input (VIO)
PTW7 input/output	IRQ7 input (Interrupt)	—	—
PTW6 input/output	IRQ6 input (Interrupt)	—	—
PTW5 input/output	IRQ5 input (Interrupt)	—	—
PTW4 input/output	IRQ4 input (Interrupt)	LCDLCLK input (LCDC)	—
PTW3 input/output	IRQ3 input (Interrupt)	ADTRG input (ADC)	—
PTW2 input/output	IRQ2 input (Interrupt)	$\overline{\text{BS}}$ output (BSC)	VIO_CKO output (VIO)
PTW1 input/output	IRQ1 input (Interrupt)	SIUAISPD input (SIU)	—
PTW0 input/output	IRQ0 input (Interrupt)	SIUAOSPD output (SIU)	—
PTX7 input/output	DACK1 output (DMAC1)	—	—
PTX6 input/output	DREQ1 input (DMAC1)	MSIOF0_MCK input (MSIOF0*5)	—
PTX5 input/output	DACK0 output (DMAC0)	IRDA_OUT output (IrDA)	—
PTX4 input/output	DREQ0 input (DMAC0)	IRDA_IN input (IrDA)	—
PTX3 input/output	TS0_SDAT input (TSIF)	—	—
PTX2 input/output	TS0_SCK input (TSIF)	—	—
PTX1 input/output	TS0_SDEN input (TSIF)	—	—
PTX0 input/output	TS0_SPSYNC input (TSIF)	—	—
PTY7 input/output	VIO_D7 input (VIO)	—	—

General Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)
PTY6 input/output	VIO_D6 input (VIO)	—	—
PTY5 input/output	VIO_D5 input (VIO)	—	—
PTY4 input/output	VIO_D4 input (VIO)	—	—
PTY3 input/output	VIO_D3 input (VIO)	—	—
PTY2 input/output	VIO_D2 input (VIO)	—	—
PTY1 input/output	VIO_D1 input (VIO)	—	—
PTY0 input/output	VIO_D0 input (VIO)	—	—
PTZ7 input/output	SIUBOLR input/output (SIU)	—	—
PTZ6 input/output	SIUBOBT input/output (SIU)	—	—
PTZ5 input/output	SIUBOSLD output (SIU)	—	—
PTZ4 input/output	SIUBMCK input (SIU)	—	—
PTZ3 input/output	VIO_FLD input (VIO)	SIUBFCK output (SIU)	—
PTZ2 input/output	VIO_HD1 input (VIO)	SIUBILR input/output (SIU)	—
PTZ1 input/output	VIO_VD1 input (VIO)	SIUBIBT input/output (SIU)	—
PTZ0 input/output	VIO_CLK1 input (VIO)	SIUBISLD input (SIU)	—

Notes: 1. SDHI0 (1ch) is multiplexed with PTD and PTS.
2. SCIF1 and SCIF3 are multiplexed with PTS and PTV.
3. SCIF0 and SCIF2 are multiplexed with PTT and PTU.
4. SCIF5 and SCIF4 are multiplexed with PTE and PTN.
5. MSIOF0 is multiplexed with PTF and PTT.

Section 35 A/D Converter

This LSI includes a 10-bit successive-approximation A/D converter allowing selection of up to four analog input channels.

35.1 Features

A/D converter features are listed below.

- 10-bit resolution
- Four input channels
- High-speed conversion
  - Conversion time: maximum 15 μs per channel
- Three conversion modes
  - Single mode: A/D conversion on one channel
  - Multi mode: A/D conversion on one to four channels
  - Scan mode: Continuous A/D conversion on one to four channels
- Four 16-bit data registers
  - A/D conversion results are transferred for storage into 16-bit data registers corresponding to the channels.
- Sample-and-hold function
- A/D interrupt requested at the end of conversion
  - At the end of A/D conversion, an A/D end interrupt (ADI) can be requested.
- A/D conversion can be externally triggered

Figure 35.1 shows a block diagram of the A/D converter.

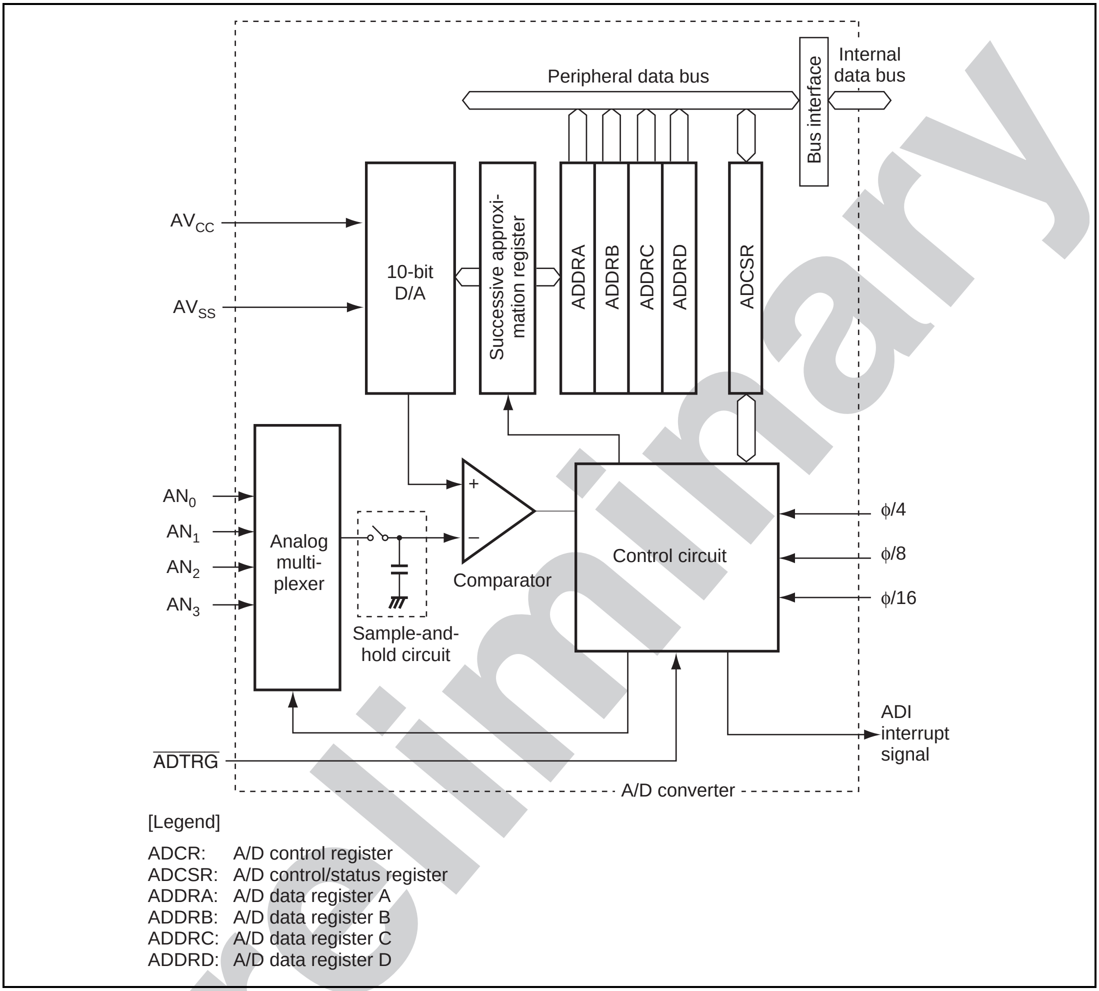


Figure 35.1 Block Diagram of A/D Converter

35.2 Input Pins

Table 35.1 summarizes the A/D converter's input pins. AV_{CC} and AV_{SS} are the power supply inputs for the analog circuits in the A/D converter. AV_{CC} also functions as the A/D converter reference voltage pin.

Table 35.1 Pin Configuration

Pin Name	Function	I/O	Descriptions
AVcc	Analog power supply pin	Input	Analog power supply and reference voltage for A/D conversion
AVss	Analog ground pin	Input	Analog ground and reference voltage for A/D conversion
AN0	Analog input pin 0	Input	Analog inputs 0 to 3
AN1	Analog input pin 1	Input	
AN2	Analog input pin 2	Input	
AN3	Analog input pin 3	Input	
$\overline{\text{ADTRG}}$	Analog trigger	Input	External trigger input for starting A/D conversion

Section 36 User Break Controller (UBC)

The user break controller (UBC) provides versatile functions to facilitate program debugging. These functions help to ease creation of a self-monitor/debugger, which allows easy program debugging using this LSI alone, without using the in-circuit emulator. Various break conditions can be set in the UBC: instruction fetch or read/write access of an operand, operand size, data contents, address value, and program stop timing for instruction fetch.

36.1 Features

1. The following break conditions can be set.

   Break channels: Two (channels 0 and 1)

   User break conditions can be set independently for channels 0 and 1, and can also be set as a single sequential condition for the two channels, that is, a sequential break. (Sequential break involves two cases such that the channel 0 break condition is satisfied in a certain bus cycle and then the channel 1 break condition is satisfied in a different bus cycle, and vice versa.)

- Address

  When 40 bits containing ASID and 32-bit address are compared with the specified value, all the ASID bits can be compared or masked.

  32-bit address can be masked bit by bit, allowing the user to mask the address in desired page sizes such as lower 12 bits (4-Kbyte page) and lower 10 bits (1-Kbyte page).

- Data

  32 bits can be masked only for channel 1.

- Bus cycle

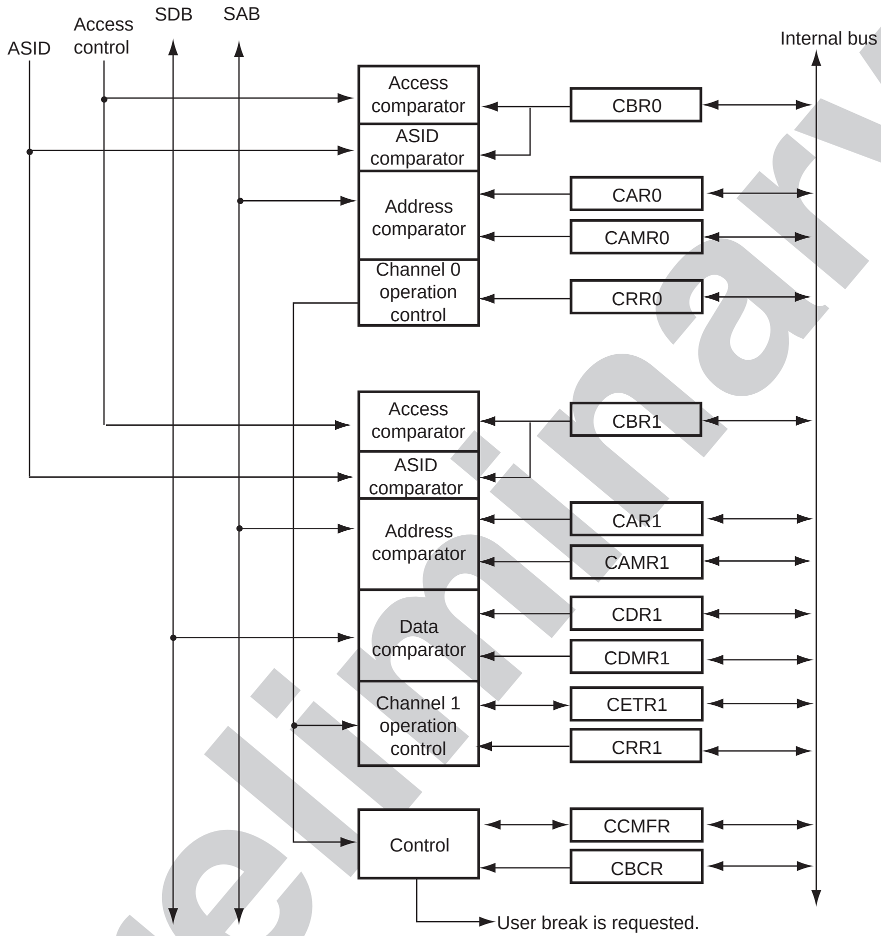
  The program can break either for instruction fetch (PC break) or operand access.

- Read or write access
- Operand sizes

  Byte, word, longword, and quadword are supported.

2. The user-designated exception handling routine for the user break condition can be executed.
3. Pre-instruction-execution or post-instruction-execution can be selected as the PC break timing.
4. A maximum of $2^{12} - 1$ repetition counts can be specified as the break condition (available only for channel 1).

Figure 36.1 shows the UBC block diagram.



[Legend]

CBR0: Match condition setting register 0
CRR0: Match operation setting register 0
CAR0: Match address setting register 0
CAMR0: Match address mask setting register 0
CBR1: Match condition setting register 1
CRR1: Match operation setting register 1
CAR1: Match address setting register 1
CAMR1: Match address mask setting register 1
CDR1: Match data setting register 1
CDMR1: Match data mask setting register 1
CETR1: Execution count break register
CCMFR: Channel match flag register
CBCR: Break control register
SAB: Operand address bus
SDB: Operand data bus

Figure 36.1 Block Diagram of UBC

Section 37 User Debugging Interface (H-UDI)

Note: This section contains references to the SH7723 Hardware Manual. The contents of the SH7723 Hardware Manual will be disclosed upon acceptance of a confidentiality agreement. For details, please contact a Renesas Technology sales representative.

The H-UDI is a serial interface which conforms to the JTAG (IEEE 1149.4: IEEE Standard Test Access Port and Boundary-Scan Architecture) standard. The H-UDI is also used for emulator connection.

37.1 Features

The H-UDI is a serial interface which conforms to the JTAG standard. The H-UDI is also used for emulator connection. When using an emulator, H-UDI functions should not be used. Refer to the appropriate emulator users manual for the method of connecting the emulator.

The H-UDI has six pins: TCK, TMS, TDI, TDO, $\overline{\text{TRST}}$, and $\overline{\text{ASEBRK}}$/BRKACK. The pin functions except $\overline{\text{ASEBRK}}$/BRKACK and serial communications protocol conform to the JTAG standard. This LSI has additional six pins for emulator connection: (AUDSYNC, AUDCK, and AUDATA3 to AUDATA0).

Figure 37.1 shows a block diagram of the H-UDI.

The TAP (Test Access Port) controller and five registers (SDBPR, SDIR, SDDRH, SDDRL, and SDINT). SDBPR supports the JTAG bypass mode, SDIR is used for commands, SDDR is used for data, and SDINT is used for H-UDI interrupts. SDIR is directly accessed from the TDI and TDO pins.

The TAP controller and control registers are initialized by driving the $\overline{\text{TRST}}$ pin low or by applying the TCK signal for five or more clock cycles with the TMS pin set to 1. This initialization sequence is independent of the reset pin for this LSI. Other circuits are initialized by a normal reset.

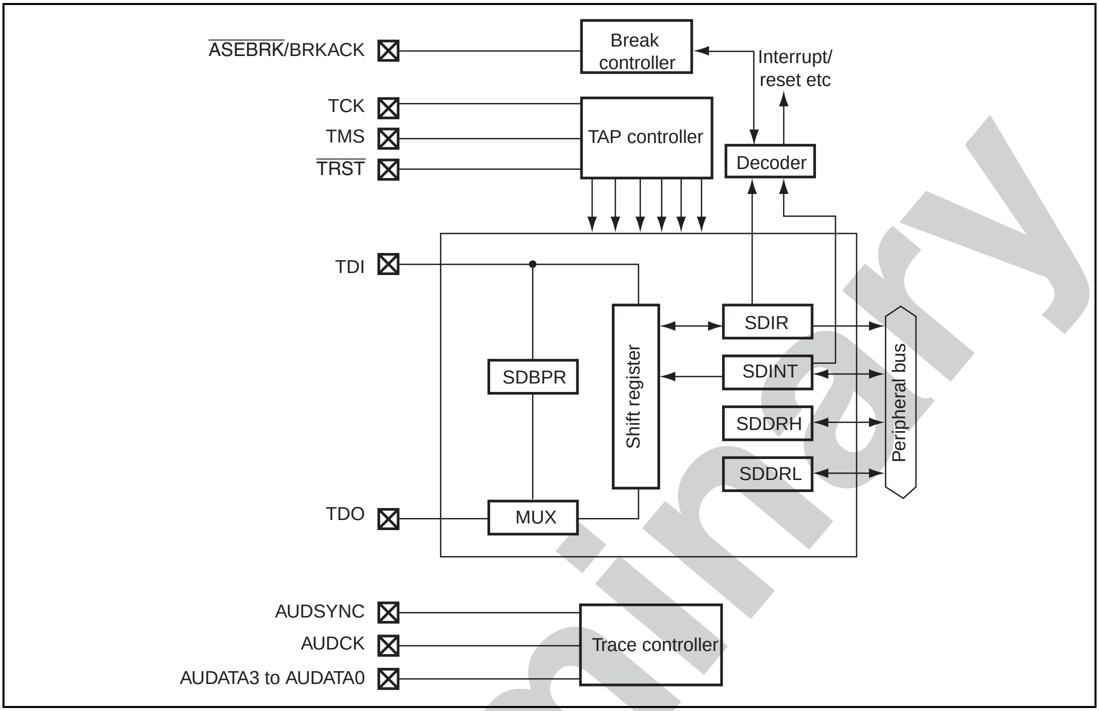


Figure 37.1 H-UDI Block Diagram

37.2 Input/Output Pins

Table 37.1 shows the pin configuration for the H-UDI.

Table 37.1 Pin Configuration

Pin Name	Function	I/O	Description	When Not in Use
TCK	Clock	Input	Functions as the serial clock input pin stipulated in the JTAG standard. Data input to the H-UDI via the TDI pin or data output via the TDO pin is performed in synchronization with this signal.	Open*[1]
TMS	Mode	Input	Mode Select Input Changing this signal in synchronization with the TCK signal determines the significance of data input via the TDI pin. Its protocol conforms to the JTAG standard (IEEE standard 1149.1).	Open*[1]

Pin Name	Function	I/O	Description	When Not in Use
$\overline{\text{TRST}}$*[2]	Reset	Input	H-UDI Reset Input This signal is received asynchronously with a TCK signal. Asserting this signal resets the JTAG interface circuit. When a power is supplied, the $\overline{\text{TRST}}$ pin should be asserted for a given period regardless of whether or not the JTAG function is used, which differs from the JTAG standard.	Fixed to ground or connected to the $\overline{\text{RESET}}$ pin.*[3]
TDI	Data input	Input	Data Input Data is sent to the H-UDI by changing this signal in synchronization with the TCK signal.	Open*[1]
TDO	Data output	Output	Data Output Data is read from the H-UDI in synchronization with the TCK signal.	Open
$\overline{\text{ASEBRK}}$/ BRKACK	Emulator	I/O	Pins for an emulator	Open*[1]
AUDSYNC, AUDCK, AUDATA3 to AUDATA0	Emulator	Output	Pins for an emulator	Open
MPMD	ASE (Emulation support mode setting)	Input	A low level on this pin places the chip in ASE mode, enabling use of the emulation support mode functions. When using an emulator such as the E10A, fix this pin at a low level.	Open*[1]

Notes: 1. This pin is pulled up in this LSI. When designing a board emulator is available or using interrupts or resets via the H-UDI or emulator, the use of external pull-up resistors will not cause any problem.

2. When designing a board emulator is available or using interrupts or resets via the H-UDI or emulator, the $\overline{\text{TRST}}$ pin should be designed so that it can be controlled independently and can be controlled to retain low level while the $\overline{\text{RESET}}$ pin is asserted at a power-on reset.

3. This pin should be connected to ground, the $\overline{\text{RESET}}$, or another pin which operates in the same manner as the $\overline{\text{RESET}}$ pin. However, when connected to a ground pin, the following problem occurs. Since the $\overline{\text{TRST}}$ pin is pulled up within this LSI, a weak current flows when the pin is externally connected to a ground pin. The value of the current is determined by a resistance of the pull-up MOS for the port pin. Although this current does not affect the operation of this LSI, it consumes unnecessary power. Pulling up the $\overline{\text{TRST}}$ pin can be disabled by the pull-down control register (PULCR) of the pin function controller (PFC). For details, see section 38, Pin Function Controller (PFC), in the SH7723 Hardware Manual.

The TCK clock or the CPG of this LSI should be set to ensure that the frequency of the TCK clock is less than the peripheral-clock frequency of this LSI.

Section 38 Electrical Characteristics

38.1 Absolute Maximum Ratings

Table 38.1 shows the absolute maximum ratings.

Table 38.1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage (I/O)	$V_{CC}Q$	–0.3 to 4.6	V
Power supply voltage (DDR)	$V_{CC}Q$_DDR	–0.3 to 3.6	V
Power supply voltage (Internal)	V_{DD}, V_{DD}_PLL, V_{DD}_DLL	–0.3 to 1.8	V
Input voltage	V_{in}DDR	–0.3 to $V_{CC}Q$_DDR + 0.3	V
Input voltage (except DDR)	V_{in}	–0.3 to $V_{CC}Q$ + 0.3	V
Analog power supply voltage (AD)	AV_{CC}	–0.3 to 4.6	V
Analog input voltage (AD)	V_{AN}	–0.3 to AV_{CC} + 0.3	V
Analog power supply voltage (USB I/O)	AV33, DV33	–0.3 to 4.6	V
Analog power supply voltage (USB internal)	AV12, DV12, UV12	–0.3 to 1.8	V
Storage temperature	T_{stg}	–55 to 125	°C

Caution: Operating the chip in excess of the absolute maximum ratings may result in permanent damage.

38.2 Recommended Operating Conditions

Table 38.2 lists the recommended operating conditions. The specification in this section assumes the use under the conditions of table 38.2 unless otherwise noted.

Table 38.2 Recommended Operating Conditions

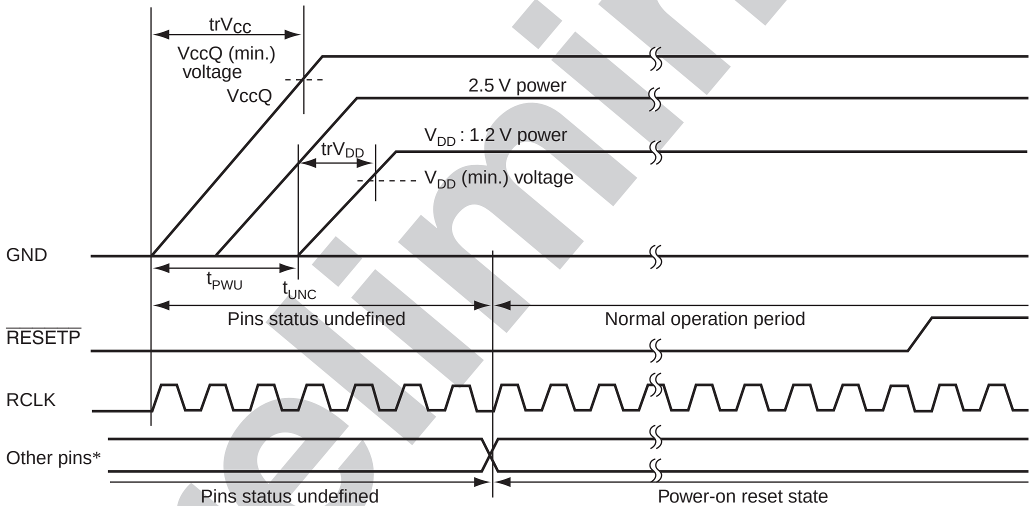
Item	Symbol	Min.	Typ.	Max.	Unit	Product number
Operating temperature (operating ambient temperature Ta)	T_{opr}	–20	—	70	°C	R8A77230C400BG
		–40	—	85		R8A77230D400BG

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Power supply voltage	Core power supply	V_{DD}	1.15	1.2	1.3	V	
	I/O power supply	$V_{CC}Q$	3.0	3.3	3.6	V	
	Power supply for PLL	V_{DD}_PLL	1.15	1.2	1.3	V	
	Power supply for DLL	V_{DD}_DLL	1.15	1.2	1.3	V	
	Power supply for DDR	$V_{CC}Q$_DDR	2.3	2.5	2.7	V	
	Analog power supply	AV_{CC}	3.0	3.3	3.6	V	
	USB analog 1.2-V power supply	AV12	1.15	1.2	1.3	V	
	USB digital 1.2-V power supply	UV12	1.15	1.2	1.3	V	
	USB digital 1.2-V power supply	DV12	1.15	1.2	1.3	V	
	USB analog 3.3-V power supply	AV33	3.0	3.3	3.6	V	
	USB digital 3.3-V power supply	DV33	3.0	3.3	3.6	V	

38.3 Power-On and Power-Off Order

1. Order of turning on 1.2 V power (V_{DD}, V_{DD}_PLL, V_{DD}_DLL, AV12, UV12, DV12), 2.5-V power (V_{CC}Q _DDR), and 3.3-V power (V_{CC}Q, AV_{CC}, AV33, DV33)

- Turn on the 3.3-V power, 2.5-V power, and 1.2-V power, in this order. This interval is as shown in table 38.3. The system design must ensure that the states of pins or undefined period of an internal state do not cause erroneous system operation. The power settling time (trV_{CC}Q) of the power supply voltage for V_{CC}Q must be shorter than those of any other 3.3-V power.
- First turn on the 3.3-V power, and input RCLK before turning on the 1.2-V.
- Until voltage is applied to all power supplies and a low level is input to the $\overline{\text{RESETP}}$ pin, internal circuits remain unsettled, and so pin states are also undefined. The system design must ensure that these undefined states do not cause erroneous system operation.
- Waveforms at power-on are shown in the following figure.



Note: * Except power/GND, clock-related, and analog pins

Table 38.3 Recommended Timing in Power-On

Item	Symbol	Time	Unit
$V_{CC}Q$ power settling time	$trV_{CC}Q$	300	µs
Time difference between 3.3-V V_{CC} and 1.2-V V_{DD} at power-on	t_{PWU}	0 to 10	ms
V_{DD} power settling time	trV_{DD}	≤ 1	ms
Time over which the state is undefined	t_{UNC}	t_{PWU} + trV_{DD} + 3tRCLK	ms

Note: The 3.3-V power should be turned on at the same time as much as possible.

The state-undefined time represents the time in which rising of each power is in transition. This ensures that the pins are in the reset state after t_{UNC} has elapsed.

2. Power-off order
   - In the reverse order of power-on, first turn off the 1.2-V V_{DD} power, then turn off the 3.3-V $V_{CC}Q$ power within 10 ms. This interval should be as short as possible. The system design must ensure that the states of pins or undefined period of an internal state do not cause erroneous system operation.
   - Pin states are undefined while only the 1.2-V V_{DD} power is off. The system design must ensure that these undefined states do not cause erroneous system operation.

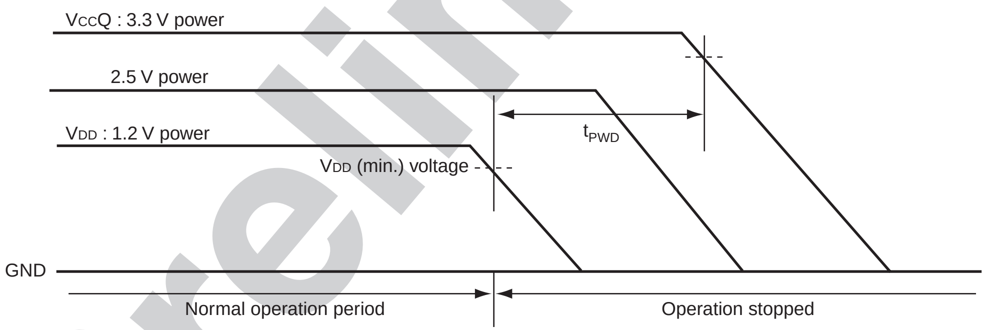


Table 38.4 Recommended Timing in Power-Off

Item	Symbol	Maximum Value	Unit
Time difference between the power-off of 1.2-V V_{DD} and 3.3-V $V_{CC}Q$ levels	t_{PWD}	0 to 10	ms

Note: * The values in the table above are recommended values, so they represent guidelines rather than strict requirements.

38.4 DC Characteristics

Tables 38.5, 38.6, and 38.7 list the DC characteristics.

Table 38.5 DC Characteristics

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input high voltage	MD0, MD1, MD2, MD3, MD5, MD8, $\overline{\text{TSTMD}}$, $\overline{\text{TST}}$, $\overline{\text{TRST}}$, MPMD, $\overline{\text{ASEBRK}}$/BRKAK, $\overline{\text{RESETP}}$, NMI, $\overline{\text{RESETA}}$, PTX2/TS0_SCK, BOOT, RCLK, EXTAL*, and EXTAL_USB* pins	V_{IHS}	$V_{CC}Q \times 0.8$	—	$V_{CC}Q + 0.3$	V	*: External clock input
	HPD31 to HPD0, HPDQS3 to HPDQS0	V_{IHDDR}	VREF + 0.6	—	$V_{CC}Q\_DDR + 0.3$	V	
	Other pins	V_{IH}	2.0	—	$V_{CC}Q + 0.3$	V	
Input low voltage	MD0, MD1, MD2, MD3, MD5, MD8, $\overline{\text{TSTMD}}$, $\overline{\text{TST}}$, $\overline{\text{TRST}}$, MPMD, $\overline{\text{ASEBRK}}$/BRKAK, $\overline{\text{RESETP}}$, NMI, $\overline{\text{RESETA}}$, PTX2/TS0_SCK, BOOT, RCLK, EXTAL*, and EXTAL_USB* pins	V_{ILS}	–0.3	—	$V_{CC}Q \times 0.2$	V	*: External clock input
	HPD31 to HPD0, HPDQS3 to HPDQS0	V_{ILDDR}	–0.3	—	VREF – 0.6	V	
	Other pins	V_{IL}	–0.3	—	0.8	V	

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	HPD31 to HPD0, HPA15 to HPA0, HPCKE, $\overline{\mathrm{HPCS}}$, $\overline{\mathrm{HPRAS}}$, $\overline{\mathrm{HPCAS}}$, HPRDWR, HPDQS3 to HPDQS0, HPDQM3 to HPDQM0	V_{OHDDR}	0.5 × V_{CC}Q_DDR + 0.31	—	—	V	
	Other pins	V_{OH}	2.4	—	—	V	I_{OH} = –2 mA
Output low voltage	HPD31 to HPD0, HPA15 to HPA0, HPCKE, $\overline{\mathrm{HPCS}}$, $\overline{\mathrm{HPRAS}}$, $\overline{\mathrm{HPCAS}}$, HPRDWR, HPDQS3 to HPDQS0, HPDQM3 to HPDQM0	V_{OLDDR}	—	—	0.5 × V_{CC}Q_DDR – 0.31	V	
	Output pins other than I^2C and SBSC	V_{OL}	—	—	0.5	V	I_{OL} = 2 mA
	SCL and SDA pins	V_{OL}	—	—	0.4	V	
Output differential voltage	HPCLK, $\overline{\mathrm{HPCLK}}$	V_{OD}	0.7	—		V	
Cross point voltage	HPCLK, $\overline{\mathrm{HPCLK}}$	V_{OX}	0.5 × V_{CC}Q_DDR – 0.2	—	0.5 × V_{CC}Q_DDR + 0.2	V	
DDR-VREF input voltage		VREF	0.49 × V_{CC}Q_DDR		0.51 × V_{CC}Q_DDR	V	

Table 38.6 DC Characteristics

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Current consumption	Normal operation	I_{DD}	—	380	580	mA	V_{DD} = 1.2 V Iϕ = 400 MHz Bϕ = 66.7 MHz B3ϕ = 133.4 MHz
		I_{CC}	—	60	80	mA	V_{CC}Q = 3.3 V
		I_{CC}_DDR	—	20	40	mA	V_{CC}Q_DDR = 2.5 V Bϕ = 66.7 MHz B3ϕ = 133.4 MHz Data bus width for BSC: 16 bits
	Sleep mode*	I_{DD}	—	100	200	mA	*: When external bus cycles other than the refresh cycle are not specified. *: All module stop: On V_{DD} = 1.2 V
		I_{CC}	—	30	40		
		I_{CC}_DDR	—	15	30	mA	V_{CC}Q = 3.3 V Bϕ = 66.7 MHz B3ϕ = 133.4 MHz
	Software standby mode	I_{stby}	—	20	80	mA	Ta = 25°C V_{CC}Q = 3.3 V V_{DD} = 1.2 V
	U-standby mode	I_{ustby}	—	—	100	μA	Ta = 25°C V_{CC}Q = 3.3 V V_{DD} = 1.2 V Input clock off
Input leak current	All input pins (except SBSC pins)	$\|I_{in}\|$	—	—	1	μA	V_{in} = 0.5 to V_{CC}Q – 0.5 V
	SBSC pins	$\|I_{inSB}\|$	—	—	3		
Three-state leak current	I/O, all output pins (off condition) (except SBSC pins)	$\|I_{STI}\|$	—	—	1	μA	V_{in} = 0.5 to V_{CC}Q – 0.5 V
	SBSC pins	$\|I_{inSB}\|$	—	—	3		

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Pull-up/ pull-down resistance	Port pins	P_{pull}	20	—	150	kΩ	
Pin capacitance	SBSC pins	C_{SB}	—	—	10	pF	
	All pins	C	—	—	10	pF	

Notes: 1. Make sure to supply the electric power to all the power supply pins anytime and the V_{SS} pin to the system ground (0 V).

2. Current consumption values in the table are for V_{IH}min = V_{CC}Q – 0.5 V and V_{IL}max = 0.5 V with all output pins unloaded.

3. I_{DD} is the total current flowing through the V_{DD}, V_{DD}-PLL, V_{DD}-DLL, DV12, AV12, and UV 12 pins. I_{CC} is the total current flowing through the V_{CC}Q, DV33, and AV33 pins. I_{CC}_DDR is the current flowing through the V_{CC}Q_DDR pin. I_{STBY} is the total of I_{DD}, I_{CC}, and I_{CC}_DDR in standby mode. I_{USTBY} is the total of I_{DD}, I_{CC}, and I_{CC}_DDR in U-standby mode.

Table 38.7 Permissible Output Current Values

Item	Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (per pin)	I_{OL}	—	—	2.0	mA
Permissible output low current (total)	ΣI_{OL}	—	—	40	mA
Permissible output high current (per pin)	$–I_{OH}$	—	—	2.0	mA
Permissible output high current (total)	$\Sigma (–I_{OH})$	—	—	40	mA
Permissible I^2C output low current (SCL, SDA)	I_{OL}	—	—	10	mA

Note: * To ensure chip reliability, do not exceed the output current values given in table 38.7.

38.5 AC Characteristics

The inputs of this LSI are synchronous as a rule. The setup and hold time of each input signal must be satisfied unless otherwise noted.

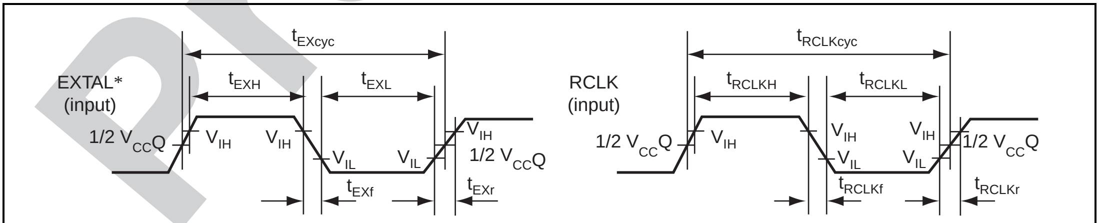
Table 38.8 Operating Frequency Range

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Operating frequency	CPU, FPU, cache (Iϕ)	f	10	—	400	MHz	
	CPU, FPU, cache (Uϕ)		10	—	133.4		
	SuperHyway bus (SHϕ)		10	—	133.4		
	BSC bus (Bϕ)		10	—	66.7		
	SBSC bus (B3ϕ)		10	—	133.4		
	Peripheral module (Pϕ)		2.5	—	33.4		
	SIU clock A (SIUCKA)		—	—	33.4		
	SIU clock B (SIUCKB)		—	—	33.4		
	IrDA clock (IrDACK)		—	—	33.4		
	Video clock (VIO_CKO)		—	—	66.7		

38.5.1 Clock Timing

Table 38.9 Clock Timing

Item	Symbol	Min.	Max.	Unit	Figure
EXTAL clock input frequency	f_{EX}	15	50	MHz	38.1
EXTAL clock input cycle time	t_{EXcyc}	20	66.7	ns	
EXTAL clock input low pulse width	t_{EXL}	4.5	—	ns	
EXTAL clock input high pulse width	t_{EXH}	4.5	—	ns	
EXTAL clock input rise time	t_{EXr}	—	3	ns	
EXTAL clock input fall time	t_{EXf}	—	3	ns	
RCLK clock input frequency	f_{RCLK}	32	33	kHz	
RCLK clock input cycle time	$t_{RCLKcyc}$	30.3	31.3	μs	
RCLK clock input low pulse width	t_{RCLKL}	10	—	μs	
RCLK clock input high pulse width	t_{RCLKH}	10	—	μs	
RCLK clock input rise time	t_{RCLKr}	—	200	ns	
RCLK clock input fall time	t_{RCLKf}	—	200	ns	
CKO clock output frequency	f_{CKO}	5	66.7	MHz	38.2
CKO clock output cycle time	t_{CKOcyc}	15	200	ns	
CKO clock output low pulse width	t_{CKOL}	3	—	ns	
CKO clock output high pulse width	t_{CKOH}	3	—	ns	
CKO clock output rise time	t_{CKOr}	—	3	ns	
CKO clock output fall time	t_{CKOf}	—	3	ns	
$\overline{\text{RESETP}}$ assert time	t_{RESPW}	4	—	$t_{RCLKcyc}$	38.3 to 38.5
$\overline{\text{RESETOUT}}$ assert time (clock modes 0 and 1)	$t_{RESOUTM0}$	—	300	μs	
$\overline{\text{RESETOUT}}$ assert time (clock mode 3)	$t_{RESOUTM3}$	—	2.3	ms	
Software standby return time (clock modes 0 and 1)	t_{SOSM0}	—	300	μs	38.6 to 38.8
Software standby return time (clock mode 3)	t_{SOSM3}	—	2.3	ms	



Note: * When the clock is input on the EXTAL pin.

Figure 38.1 Clock Input Timing of EXTAL and RCLK

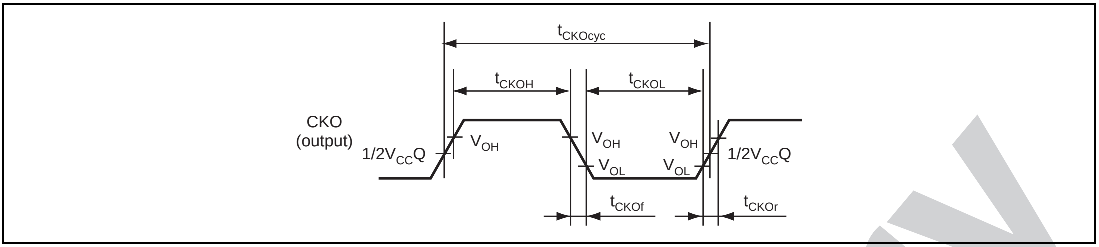


Figure 38.2 Clock Output Timing of CKO

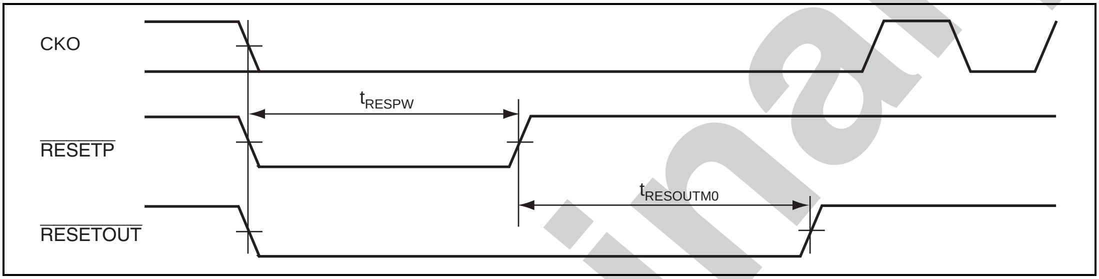


Figure 38.3 Power-On Oscillation Settling Time (Clock Mode 0)

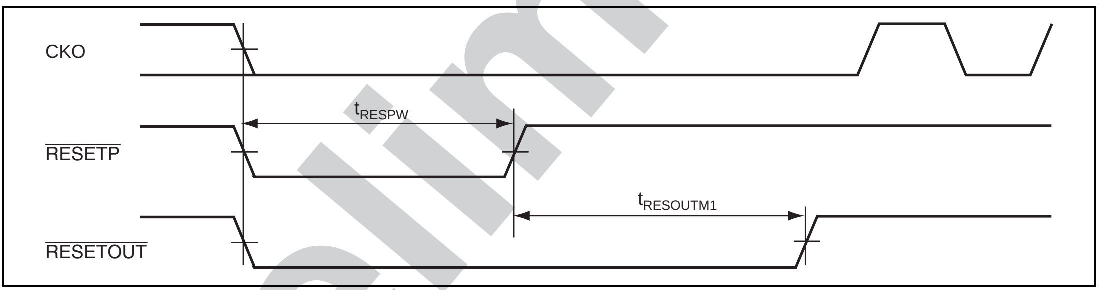


Figure 38.4 Power-On Oscillation Settling Time (Clock Mode 1)

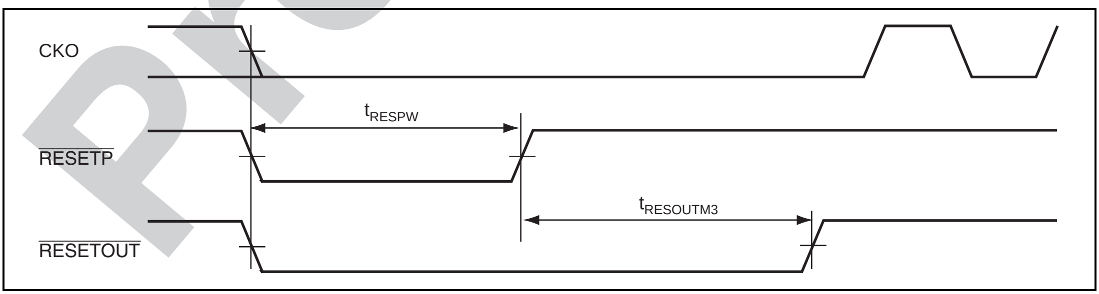


Figure 38.5 Power-On Oscillation Settling Time (Clock Mode 3)

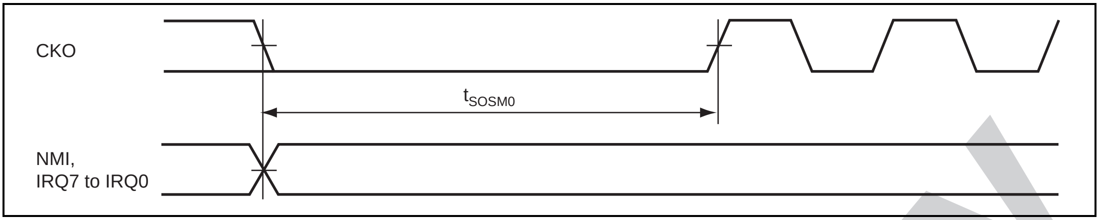


Figure 38.6 Oscillation Settling Time on Return from Software Standby by NMI or IRQ (Clock Mode 0)

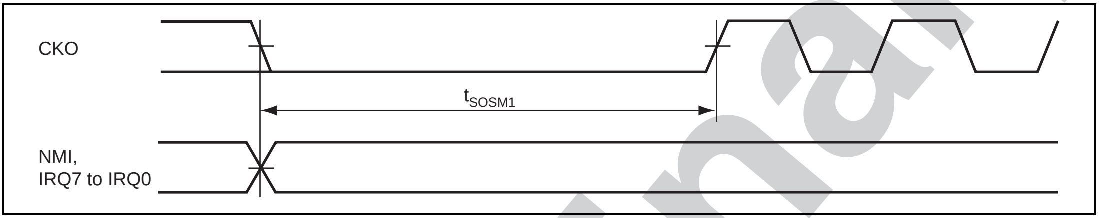


Figure 38.7 Oscillation Settling Time on Return from Software Standby by NMI or IRQ (Clock Mode 1)

Figure 38.8 Oscillation Settling Time on Return from Software Standby by NMI or IRQ (Clock Mode 3)

38.5.2 Interrupt Signal Timing

Table 38.10 Interrupt Signal Timing

Item	Symbol	Min.	Max.	Unit	Figure
NMI setup time*	t_{NMIS}	12	—	ns	38.9
NMI hold time	t_{NMIH}	6	—	ns	
IRQ7 to IRQ0 setup time*	t_{IRQS}	12	—	ns	
IRQ7 to IRQ0 hold time	t_{IRQH}	6	—	ns	

Note: * NMI and IRQ7 to IRQ0 are asynchronous signals. When the setup time in the table is satisfied, a change is detected at the rising edge of the clock. When the setup time is not satisfied, a change may not be detected until the next rising edge of the clock.

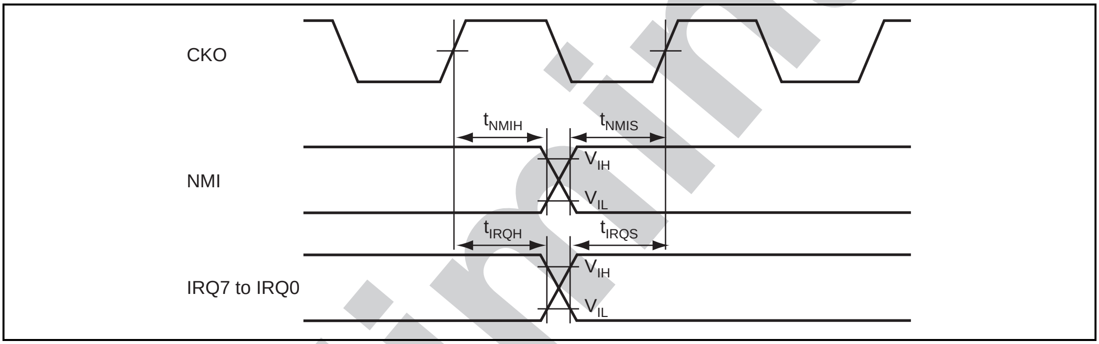


Figure 38.9 Interrupt Signal Input Timing

38.5.3 AC Bus Timing

Table 38.11 Bus Timing

Item	Symbol	Min.	Max.	Unit	Figure
Address delay time 1	t_{AD1}	1	15	ns	38.10 to 38.23
Address delay time 2	t_{AD2}	$1/2 \times t_{cyc}$	$1/2 \times t_{cyc} + 15$	ns	38.19
Address setup time	t_{AS}	0	—	ns	38.10 to 38.19
Address hold time	t_{AH}	0	—	ns	38.14
$\overline{\text{CS}}$ delay time 1	t_{CSD1}	1	15	ns	38.10 to 38.23
Read/write delay time 1	t_{RWD1}	1	15	ns	
Read/write delay time 2	t_{RWD2}	$1/2 \times t_{cyc}$	$1/2 \times t_{cyc} + 15$	ns	38.16
Read strobe delay time	t_{RSD}	$1/2 \times t_{cyc}$	$1/2 \times t_{cyc} + 15$	ns	38.10 to 38.21
Read data setup time 1	t_{RDS1}	$1/2t_{cyc} + 10$	—	ns	38.10 to 38.16, 38.20 to 38.23
Read data setup time 3	t_{RDS3}	$1/2t_{cyc} + 10$	—	ns	38.17 to 38.19
Read data hold time 1	t_{RDH1}	0	—	ns	38.10 to 38.16, 38.20 to 38.23
Read data hold time 3	t_{RDH3}	0	—	ns	38.17 to 38.19
Write enable delay time 1	t_{WED1}	$1/2 \times t_{cyc}$	$1/2 \times t_{cyc} + 15$	ns	38.10 to 38.18, 38.20, 38.21
Write enable delay time 2	t_{WED2}	0	15	ns	38.16, 38.17
Write data delay time 1	t_{WDD1}	—	15	ns	38.10 to 38.18, 38.20 to 38.23
Write data hold time 1	t_{WDH1}	1	—	ns	38.10 to 38.16, 38.20 to 38.23
$\overline{\text{WAIT}}$ setup time 1	t_{WTS1}	$1/2 \times t_{cyc} + 7$	—	ns	38.10 to 38.19
$\overline{\text{WAIT}}$ hold time 1	t_{WTH1}	$1/2 \times t_{cyc} + 6$	—	ns	
$\overline{\text{BS}}$ delay time	t_{BSD}	—	1.5	ns	38.10 to 38.19, 38.23

Item	Symbol	Min.	Max.	Unit	Figure
Write data hold time 5	t_{WDH5}	1	—	ns	38.20 to 38.23
$\overline{\text{ICIORD}}$ delay time	t_{ICRSD}	—	$1/2 \times t_{cyc} + 13$	ns	38.22, 38.23
$\overline{\text{ICIOWR}}$ delay time	t_{ICWSD}	—	$1/2 \times t_{cyc} + 13$	ns	
$\overline{\text{IOIS16}}$ setup time	t_{IO16S}	$1/2 \times t_{cyc} + 6$	—	ns	38.23
$\overline{\text{IOIS16}}$ hold time	t_{IO16H}	$1/2 \times t_{cyc} + 4$	—	ns	

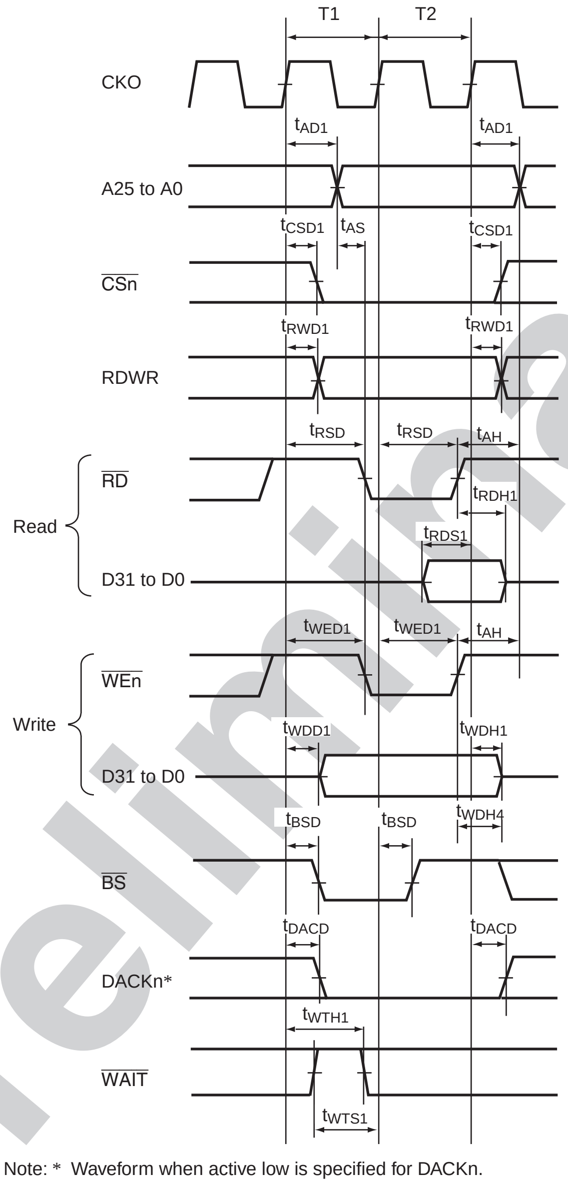


Figure 38.10 Basic Bus Cycle in Normal Space (No Wait)

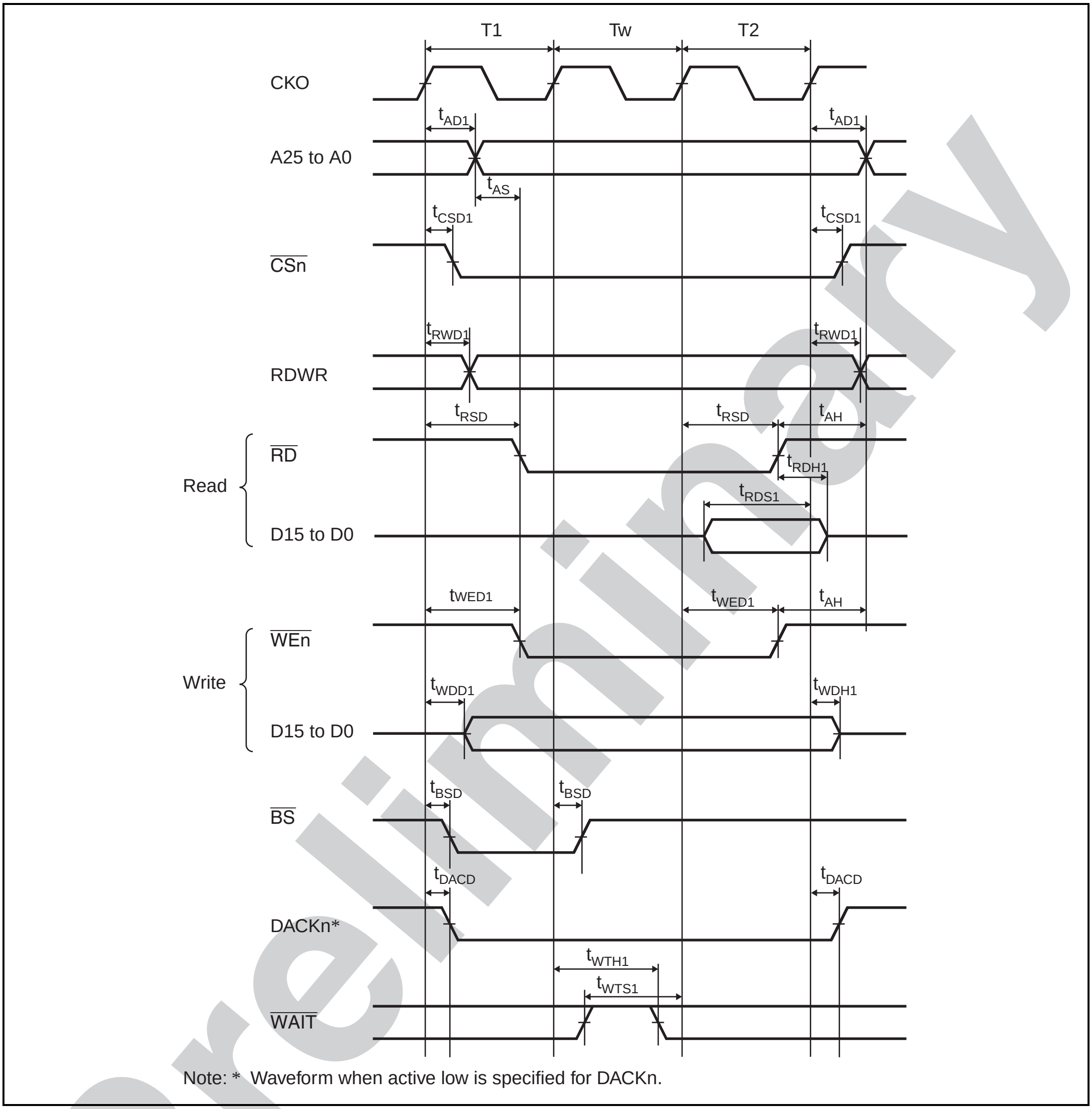


Figure 38.11 Basic Bus Cycle in Normal Space (Software Wait 1)

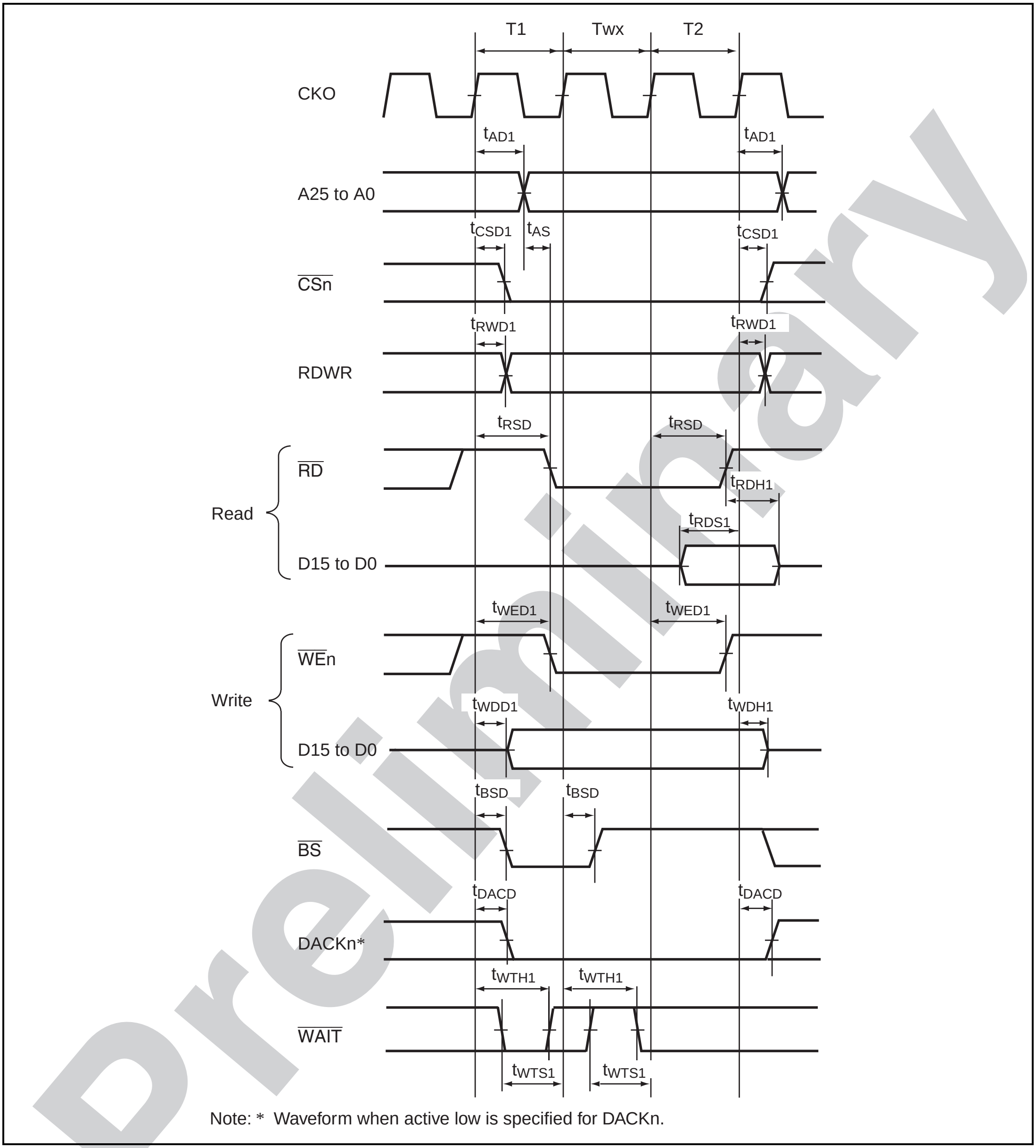
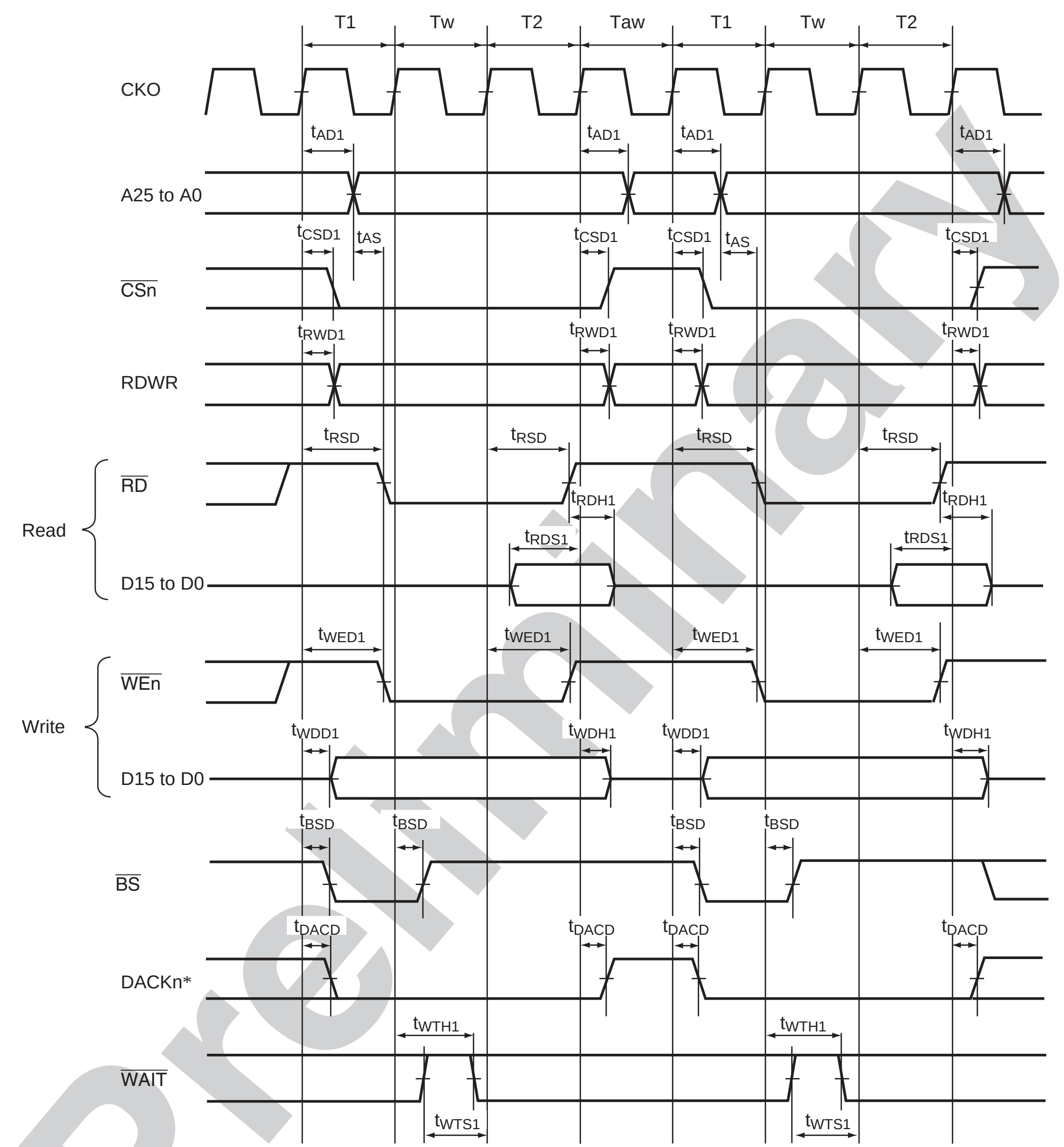


Figure 38.12 Basic Bus Cycle in Normal Space (Asynchronous External Wait 1)



Note: * Waveform when active low is specified for DACKn.

Figure 38.13 Basic Bus Cycle in Normal Space
(Software Wait 1, Asynchronous External Wait Valid (WM Bit = 0), No Idle Cycle)

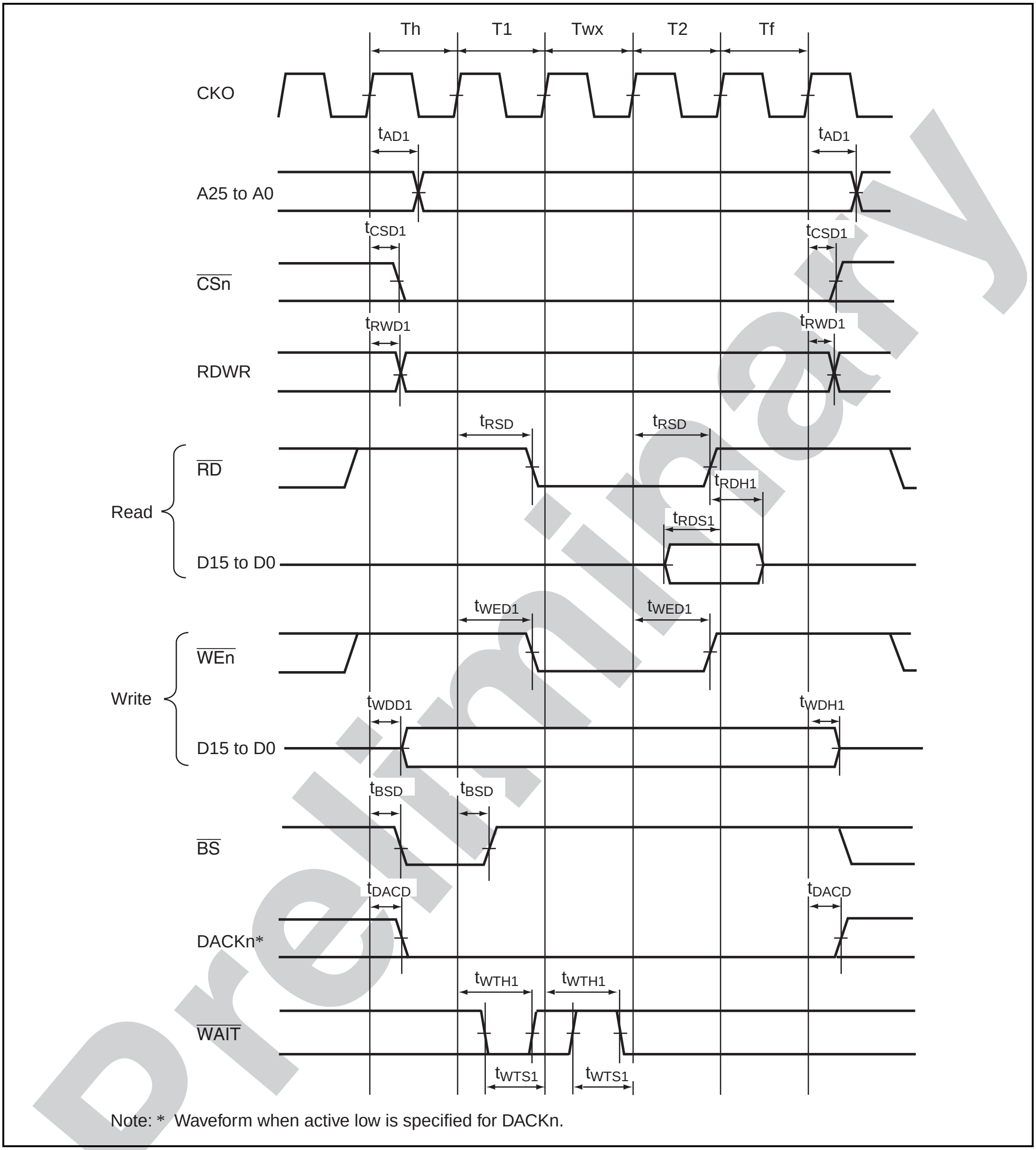
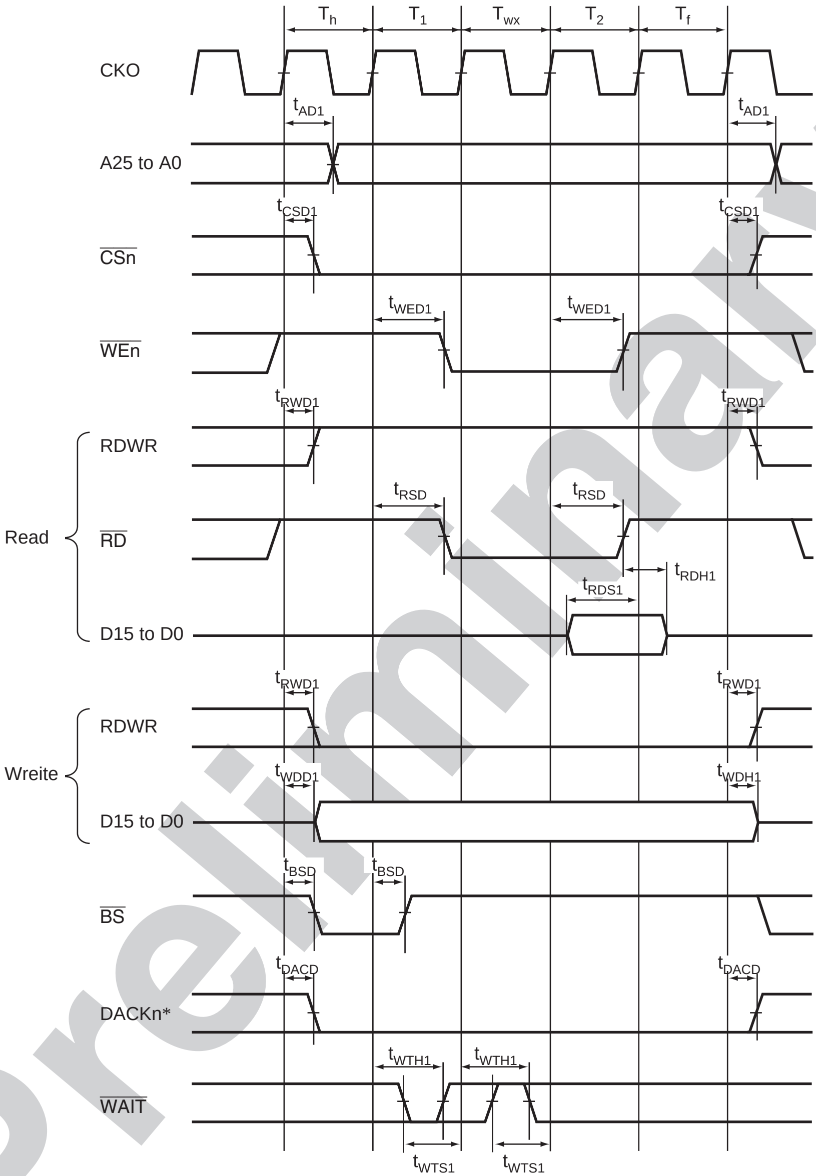


Figure 38.14 CS Extended Bus Cycle in Normal Space (SW = 1 Cycle, HW = 1 Cycle, Asynchronous External Wait 1)



Note: * Waveform when active low is specified for DACKn.

Figure 38.15 Bus Cycle of SRAM with Byte Selection (SW = 1 Cycle, HW = 1 Cycle, Asynchronous External Wait 1, BAS = 0 (UB and LB in Write Cycle Controlled))

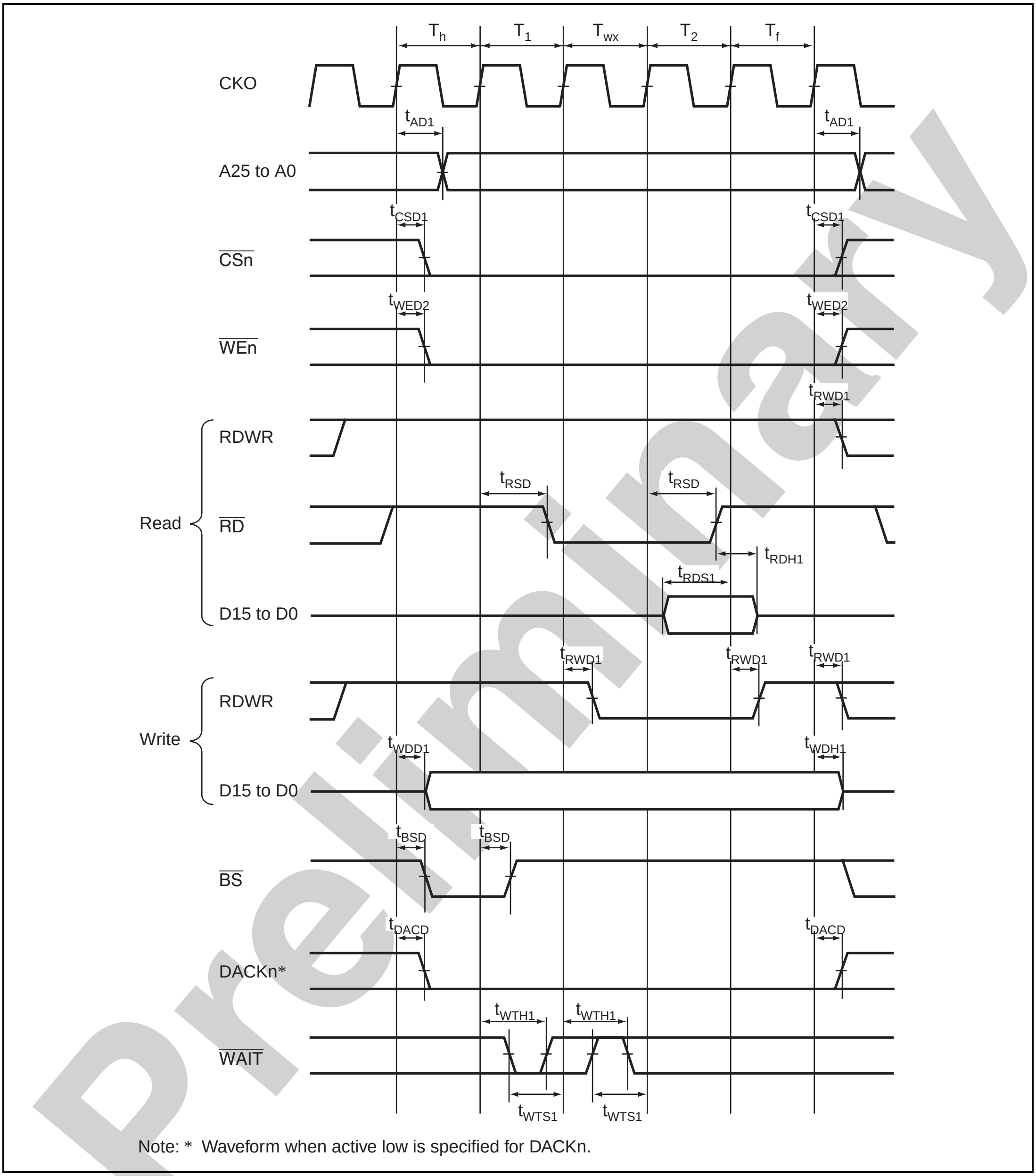


Figure 38.16 SRAM Bus Cycle with Byte Selection (SW = 1 Cycle, HW = 1 Cycle, Asynchronous External Wait 1, BAS = 1 (Write Cycle WE Control))

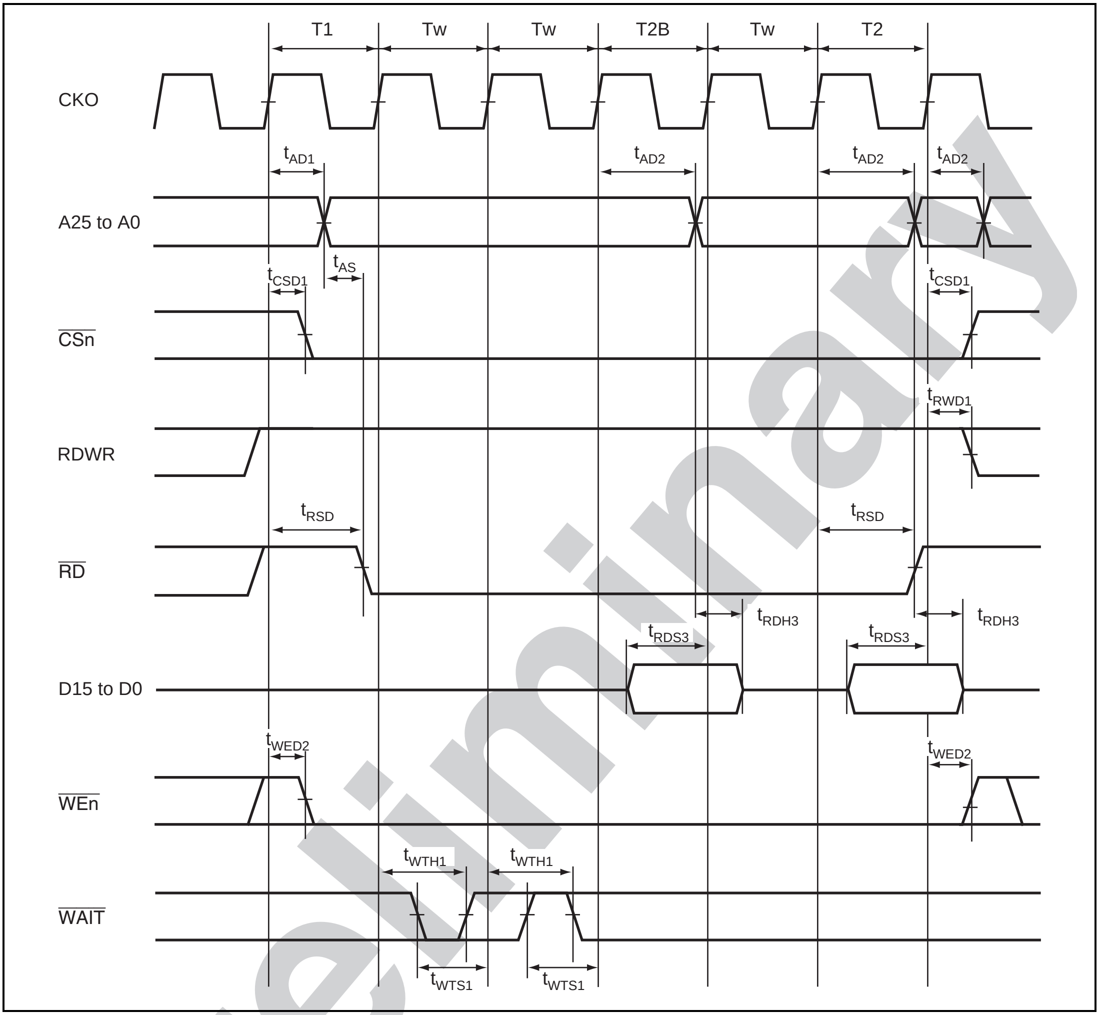


Figure 38.17 SRAM Page Mode Read Bus Cycle with Byte Selection PMD = 1, BAS = 1 (Software Wait 1, Asynchronous External Wait 1, Burst Wait 1, 2 Bursts)

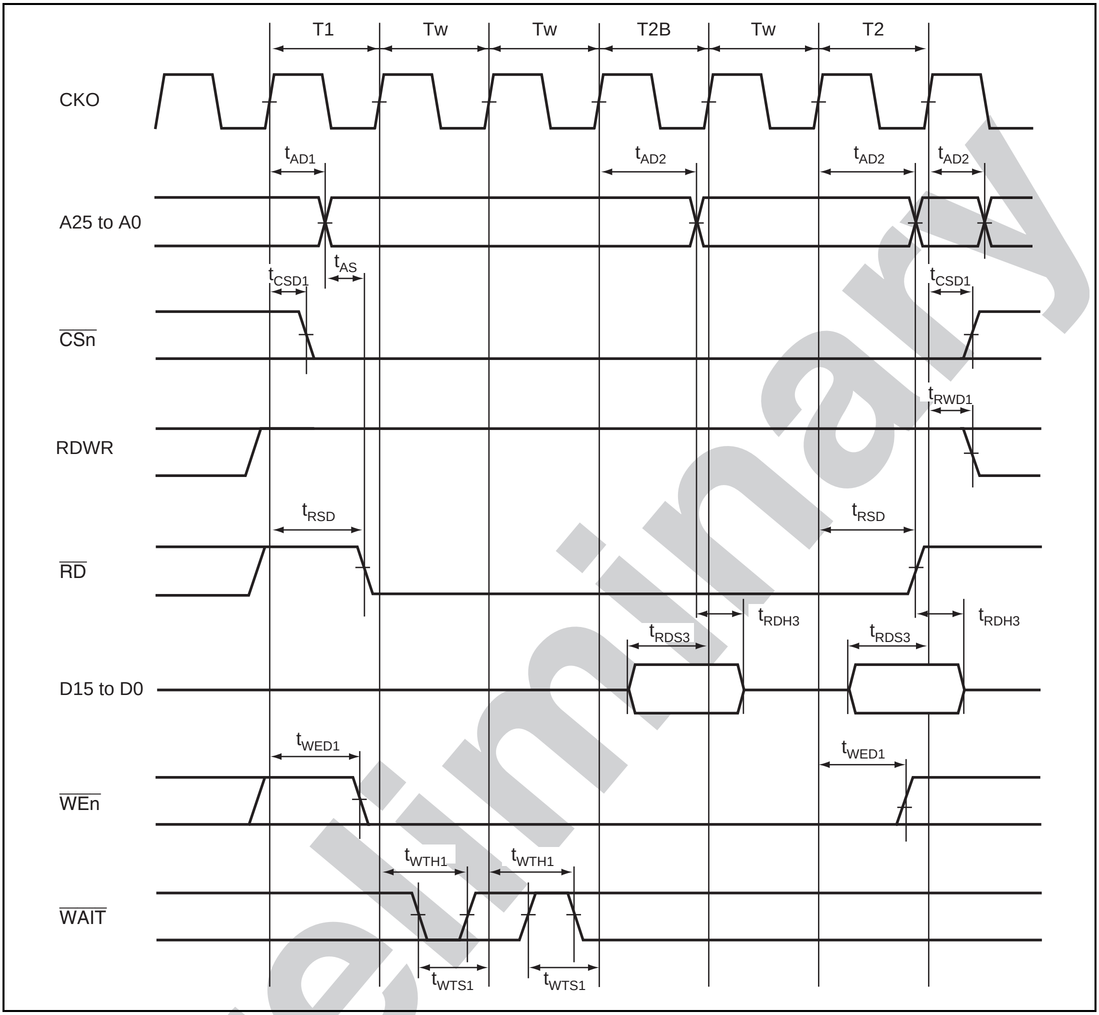


Figure 38.18 SRAM Page Mode Read Bus Cycle with Byte Selection PMD = 1, BAS = 0 (Software Wait 1, Asynchronous External Wait 1, Burst Wait 1, 2 Bursts)

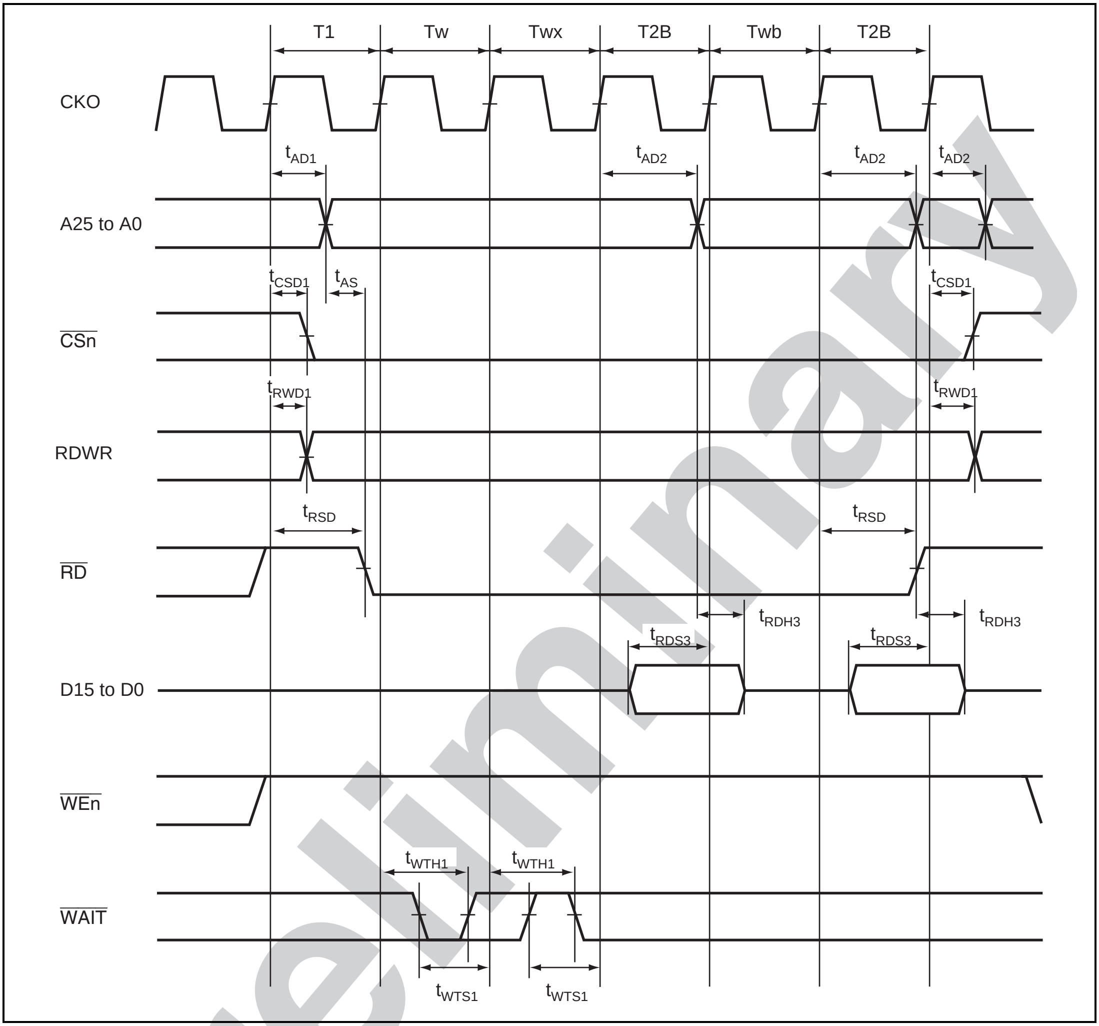


Figure 38.19 Read Bus Cycle of Burst ROM
(Software Wait 1, Asynchronous External Wait 1, Burst Wait 1, 2 Bursts)

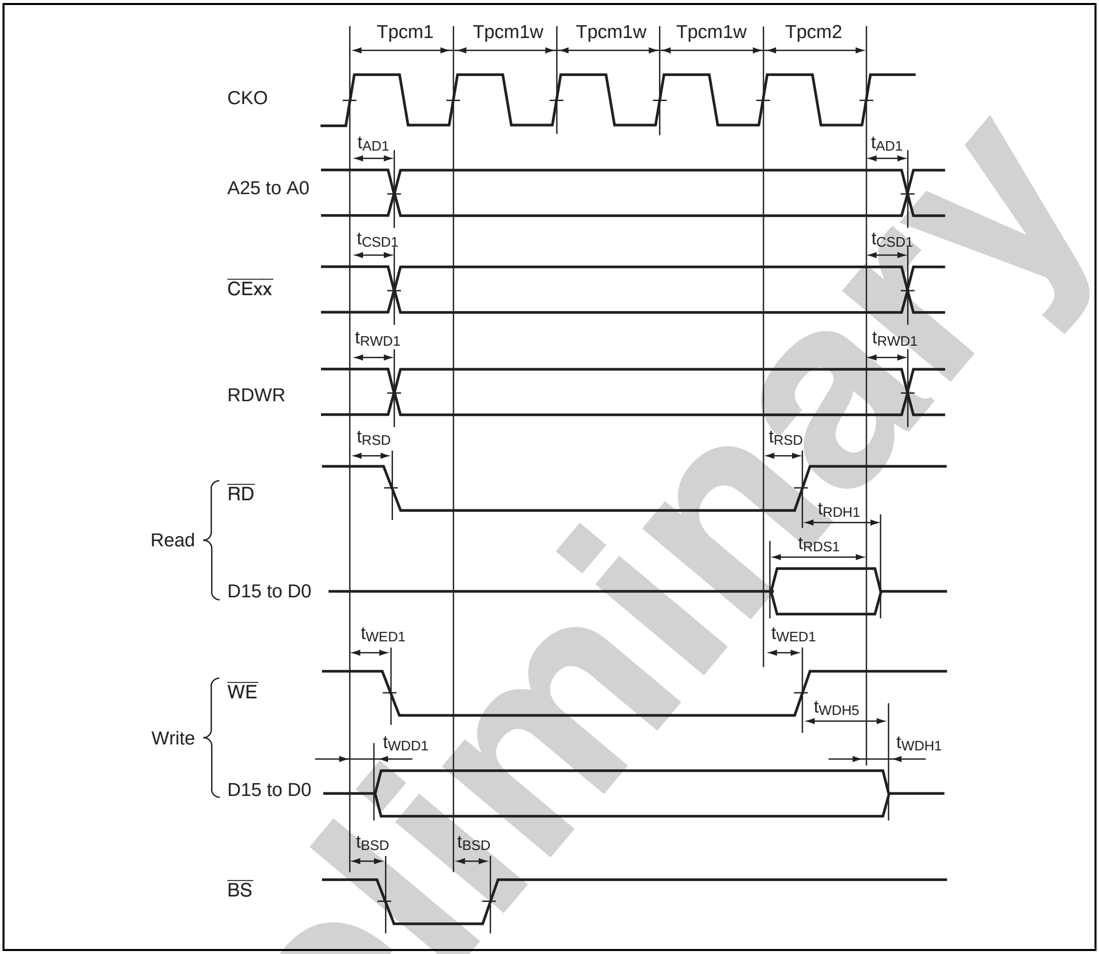


Figure 38.20 PCMCIA Memory Card Interface Bus Timing

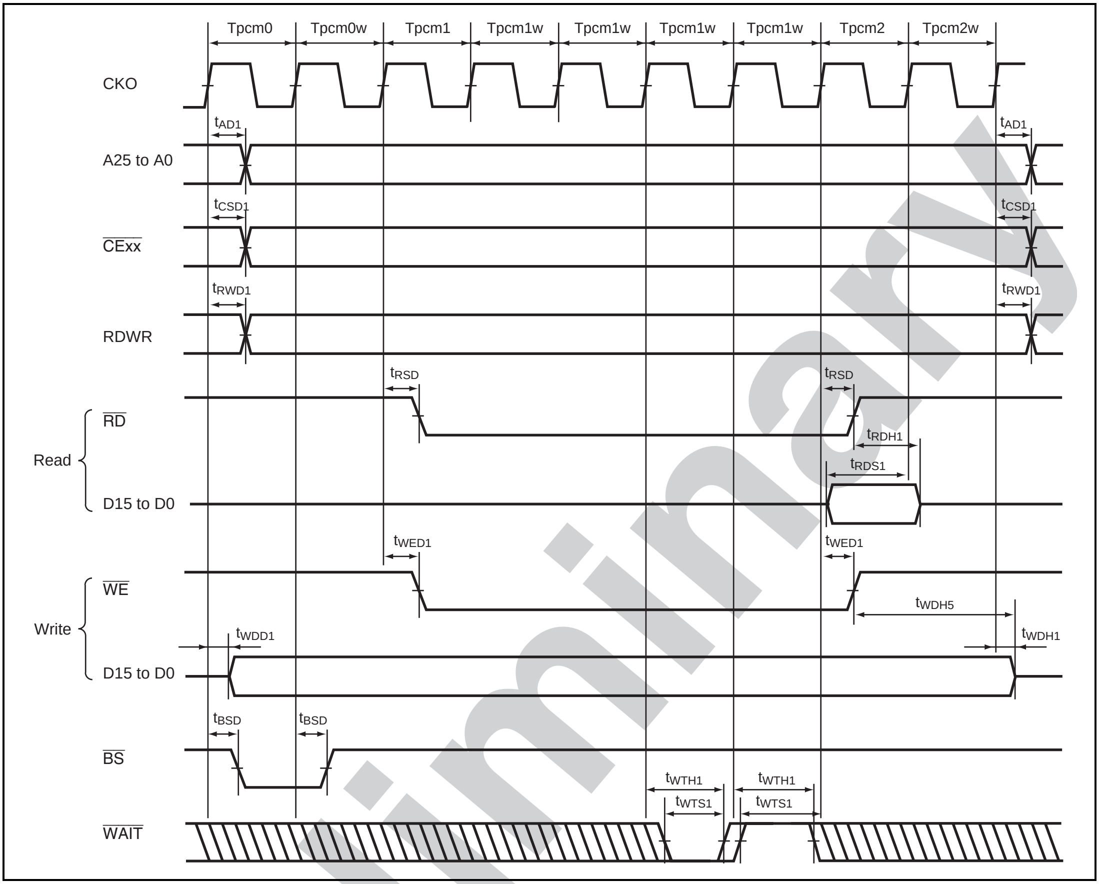


Figure 38.21 PCMCIA Memory Card Interface Bus Timing (TED[3:0] = B'0010, TEH[3:0] = B'0001, Software Wait 1, Hardware Wait 1)

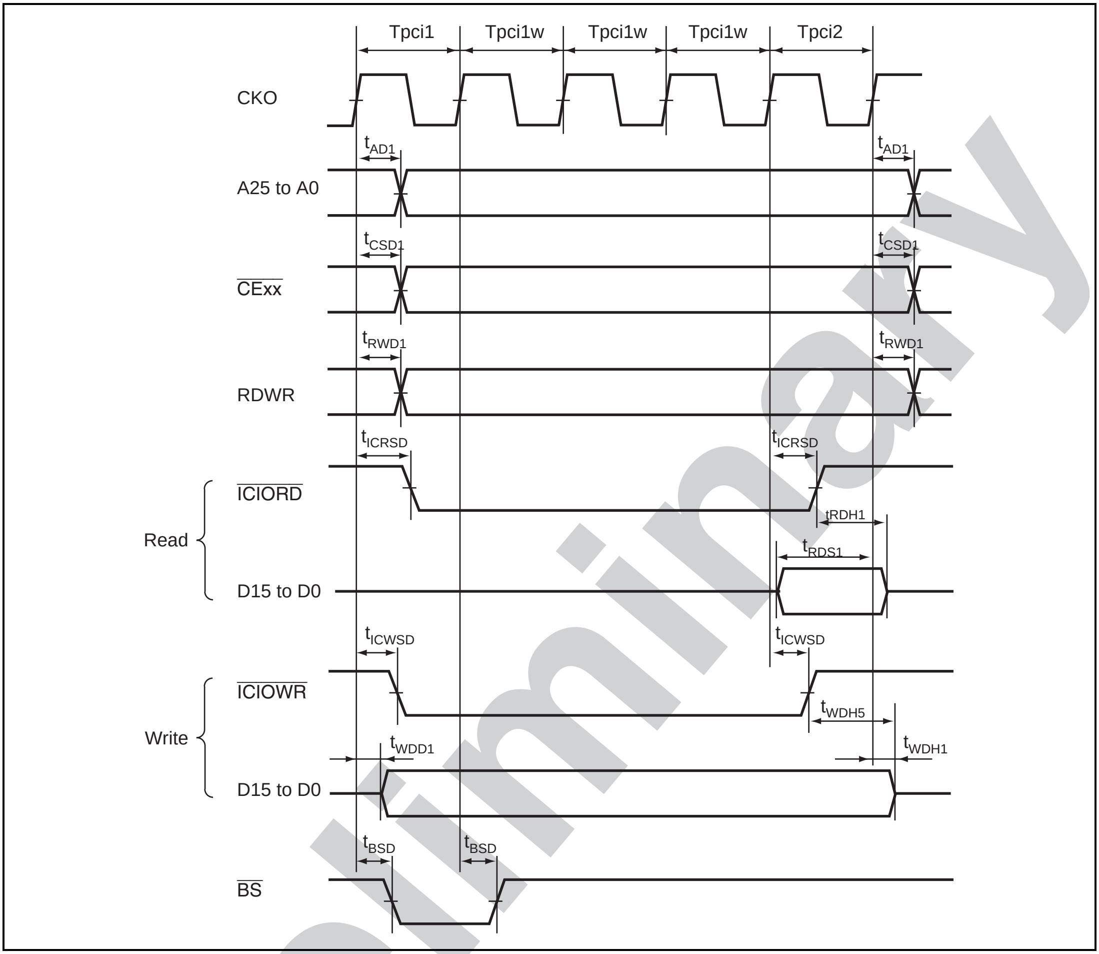


Figure 38.22 PCMCIA I/O Card Interface Bus Timing

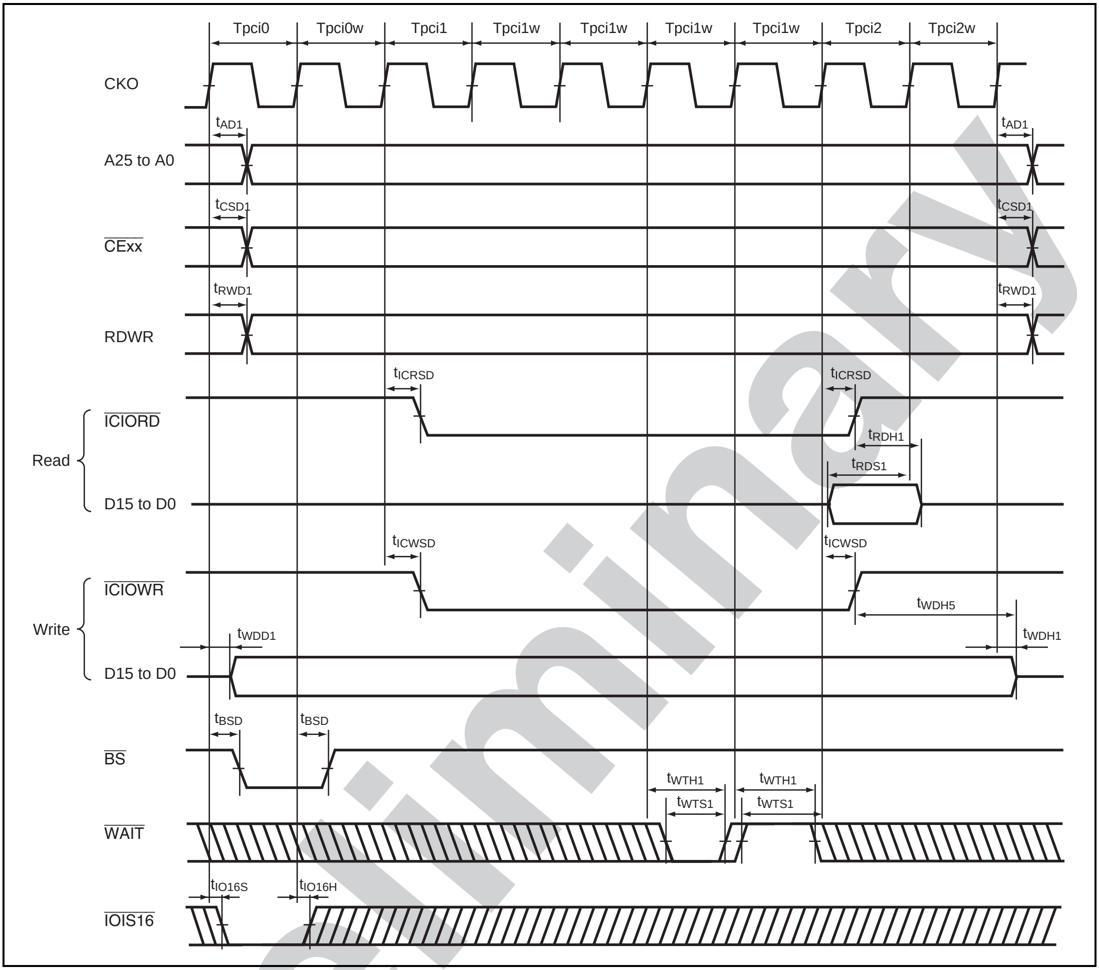


Figure 38.23 PCMCIA I/O Card Interface Bus Timing
(TED[3:0] = B'0010, TEH[3:0] = B'0001, Software Wait 1, Hardware Wait 1)

38.5.4 DDR-SDRAM Interface Timing

Table 38.12 DDR-SDRAM Interface Timing

Item	Symbol	Condition Min.	Condition Max.	Unit	Figure
Clock cycle time	t_{CK}	7.5	12	ns	38.24
CK high-level width	t_{CL}	$0.5 \times t_{CK} - 0.3$	$0.5 \times t_{CK} + 0.3$	ns	
CK low-level width	t_{CH}	$0.5 \times t_{CK} - 0.3$	$0.5 \times t_{CK} + 0.3$	ns	
Address and control input setup time	t_{IS}	1.2	—	ns	
Address and control input hold time	t_{IH}	1.2	—	ns	
First DQS latching transition to associated clock edge	t_{DQSS}	0.85	1.15	t_{CK}	
Write preamble setup time	t_{WPRES}	0	—	ns	
DQS write high pulse width	t_{DQSH}	0.38	—	t_{CK}	
DQS write low pulse width	t_{DQSL}	0.38	—	t_{CK}	
DQS falling edge to CK rising-setup time	t_{DSS}	0.3	—	t_{CK}	
DQS falling edge from CK rising-hold time	t_{DSH}	0.3	—	t_{CK}	
Write postamble	t_{WPST}	0.4	0.6	t_{CK}	
DQ and DM write setup time for DQS	t_{DS}	0.75	—	ns	
DQ and DM write hold time for DQS	t_{DH}	0.75	—	ns	
Read preamble	t_{RPRE}	0.9	1.1	t_{CK}	38.25
DQS read access time from HPCLK, HPCLK_	t_{DQSCK}	–0.75	1.75	ns	
Read postamble	t_{RPST}	0.4	0.6	t_{CK}	

Item	Symbol	Condition Min.	Condition Max.	Unit	Figure
DQ/DQS read hold time from DQS	t_{QH}	0.33	—	t_{CK}	38.25
DQS-DQ skew for DQS and associated DQ signals	t_{DQSQ}	—	0.7	ns	

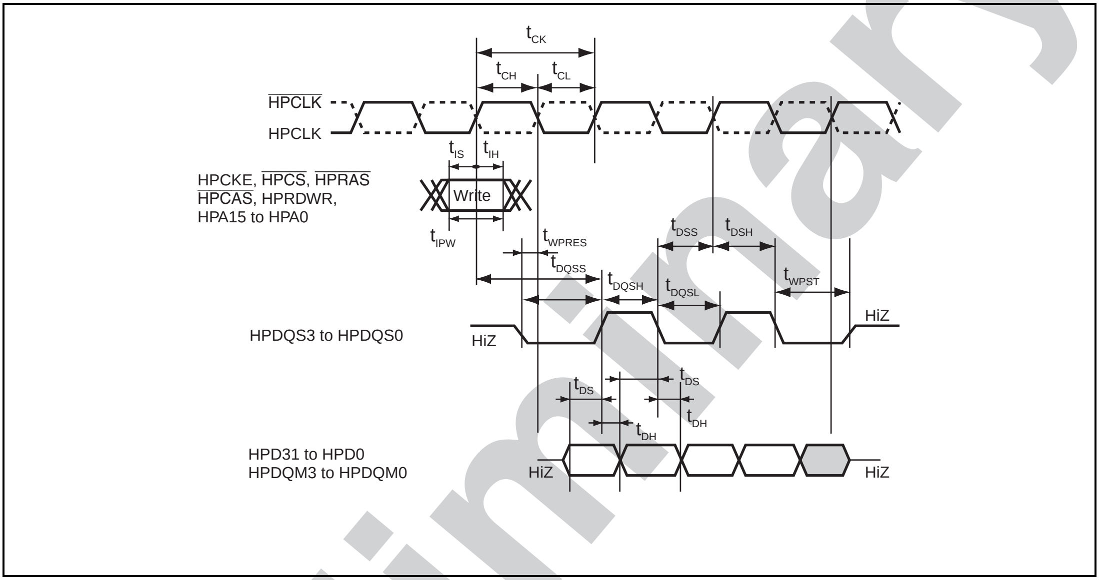


Figure 38.24 DDR-SDRAM Output Timing (Writing) [n: A/B]

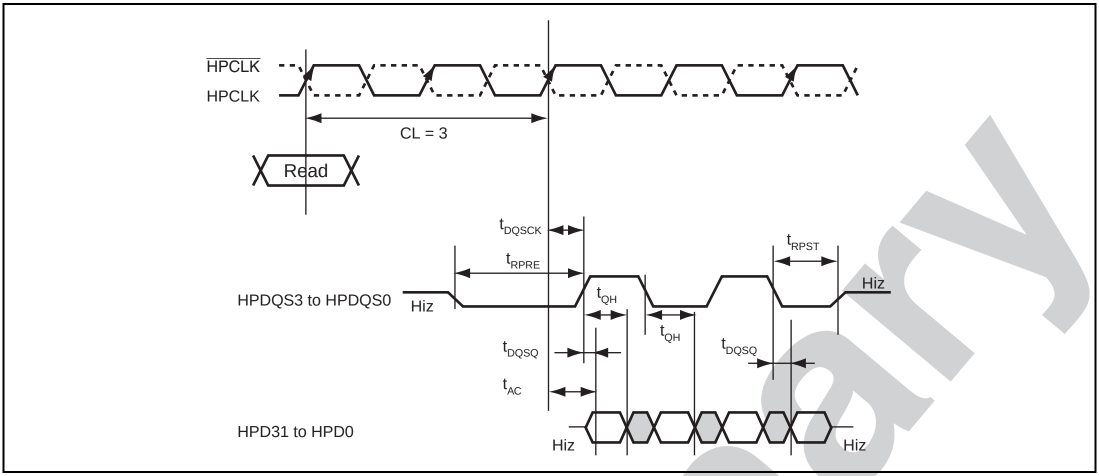


Figure 38.25 DDR-SDRAM Output Timing (Reading) [n: A/B]

38.5.5 I/O Port Signal Timing

Table 38.13 Peripheral Module Signal Timing

Item	Symbol	Min.	Max.	Unit	Figure
Output data delay time	t_{PORTD}	—	17	ns	38.26
Input data setup time	t_{PORTS}	17	—		
Input data hold time	t_{PORTH}	10	—		

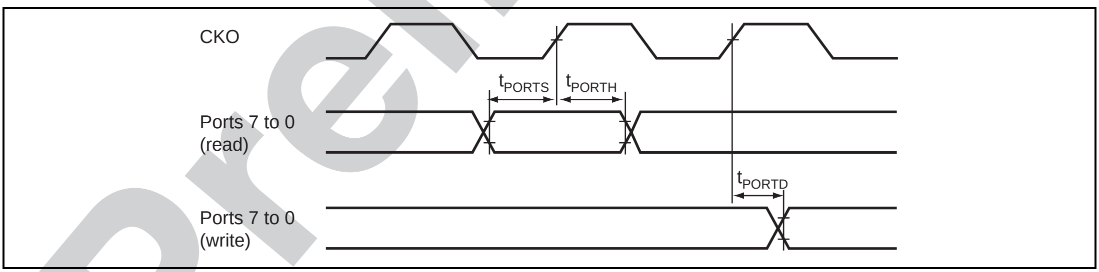


Figure 38.26 I/O Port Timing

38.5.6 DMAC Module Signal Timing

Table 38.14 DMAC Module Signal Timing

Item	Symbol	Min.	Max.	Unit	Figure
DREQ setup time	t_{DREQS}	8	—	ns	38.27
DREQ hold time	t_{DREQH}	8	—		
DACK delay time	t_{DACD}	—	15		38.28

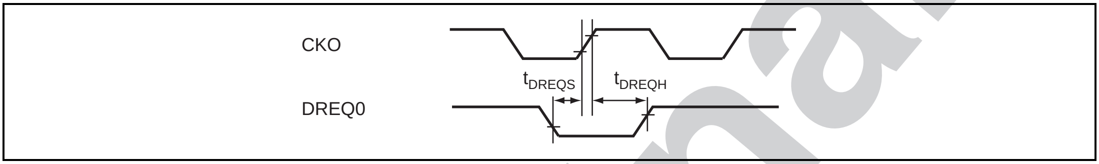


Figure 38.27 DREQ Input Timing (DREQ Low Level Detected)

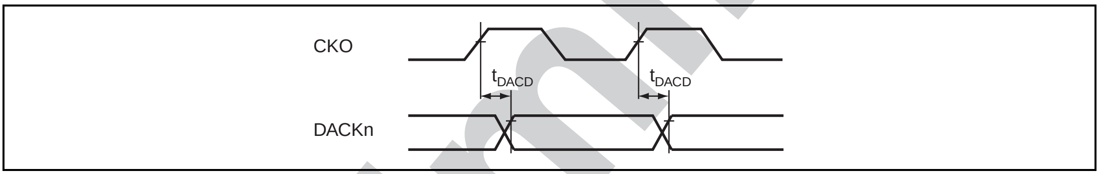


Figure 38.28 DACK Output Timing

38.5.7 TPU Module Signal Timing

Table 38.15 TPU Module Signal Timing

Item	Symbol	Min.	Max.	Unit	Figure
Output data delay time	t_{TOD}	—	15	ns	38.29

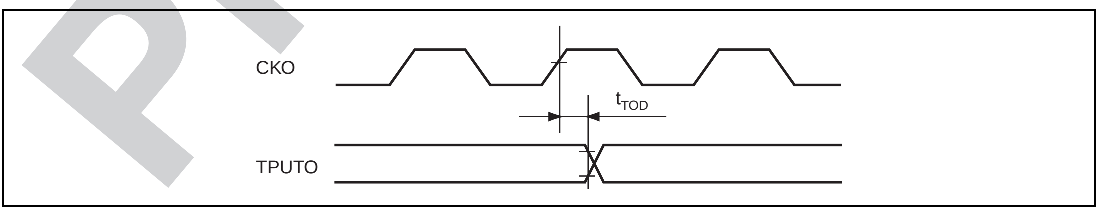


Figure 38.29 TPU Output Timing

38.5.8 MSIOF Module Signal Timing

Table 38.16 MSIOF Module Signal Timing

Item	Symbol	Min.	Max.	Unit	Figure
MSIOF_MCK0/1 clock cycle	t_{MCYC}	$2 \times t_{bcyc}$*	—	ns	38.30
MSIOF_MCK0/1 input high level width	t_{MWH}	$0.4 \times t_{MSCYC}$	—	ns	
MSIOF_MCK0/1 input low level width	t_{MWL}	$0.4 \times t_{MSCYC}$	—	ns	
MSIOF_TSCK (RSCK) clock cycle	t_{MSCYC}	$2 \times t_{bcyc}$*	—	ns	38.31, 38.32
MSIOF_TSCK (RSCK) output high level width	t_{MSWHO}	$0.4 \times t_{MSCYC}$	—	ns	38.31
MSIOF_TSCK (RSCK) output low level width	t_{MSWLO}	$0.4 \times t_{MSCYC}$	—	ns	
MSIOF_TSCK (RSCK) input high level width	t_{MSWHI}	$0.4 \times t_{MSCYC}$	—	ns	
MSIOF_TSCK (RSCK) input low level width	t_{MSWLI}	$0.4 \times t_{MSCYC}$	—	ns	38.32
MSIOF_TSYNC (RSYNC) output delay time	t_{FSD}	—	20	ns	38.31
MSIOF_TSYNC (RSYNC) input setup time	t_{FSS}	20	—	ns	38.32
MSIOF_TSYNC (RSYNC) input hold time	t_{FSH}	20	—	ns	
MSIOF_TXD output delay time	t_{TDD}	—	20	ns	38.31
MSIOF_RXD input setup time	t_{RDS}	20	—	ns	38.32
MSIOF_RXD input hold time	t_{RDH}	20	—	ns	

Note: t_{bcyc} is a cycle time of a peripheral clock (Bϕ).

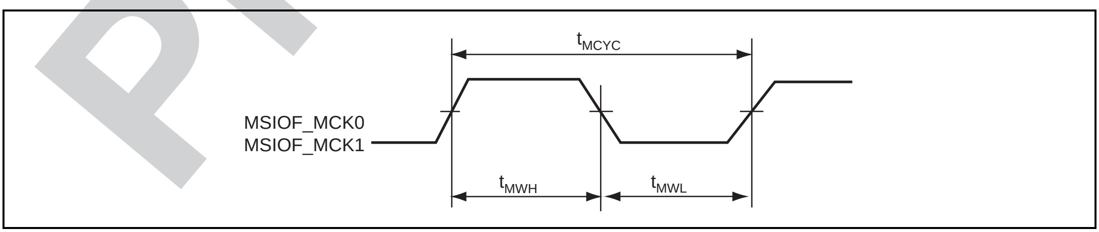


Figure 38.30 SIOFMCK Input Timing

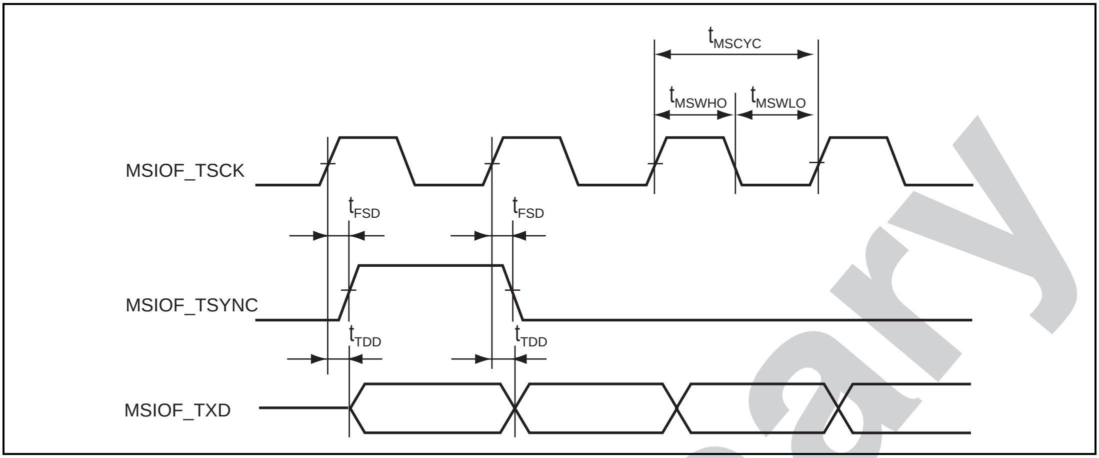


Figure 38.31 MSIOF Transmission/Reception Timing (Master Mode 1)

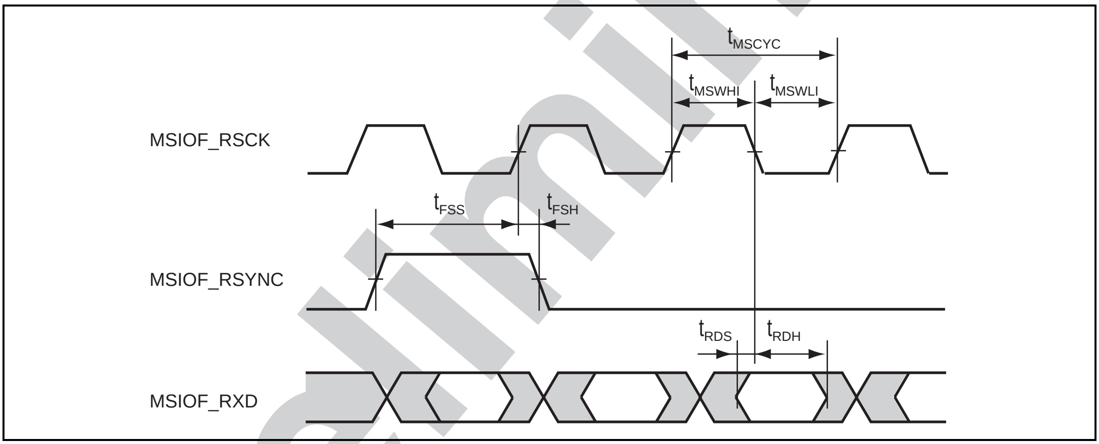


Figure 38.32 MSIOF Transmission/Reception Timing (Slave Mode)

38.5.9 SCIF Module Signal Timing

Table 38.17 SCIF Module Signal Timing (Asynchronous)

Item	Symbol	Min.	Max.	Unit	Figure
SCK input clock cycle	t_{SCYC}	4	—	t_{PCYC}	38.33
SCK input clock high level width	t_{SCWH}	0.4	—	t_{SCYC}	
SCK input clock low level width	t_{SCWL}	0.4	—	t_{SCYC}	
SCK input clock rise time	t_{SCKr}	—	1.5	t_{PCYC}	
SCK input clock fall time	t_{SCKf}	—	1.5	t_{PCYC}	
TXD transfer data delay time	t_{TXD}	—	$3 \times t_{PCYC} + 50$	ns	38.34
RXD input data setup time	t_{RXS}	$2 \times t_{PCYC}$	—	ns	
RTS input data hold time	t_{RXH}	$2 \times t_{PCYC}$	—	ns	
RTS delay time	t_{RTSD}	—	100	ns	
CTS setup time	t_{CTSS}	100	—	ns	
CTS hold time	t_{CTSH}	100	—	ns	

Note: In SCIF module, t_{pcyc} is a cycle time of a peripheral clock (Pϕ).
In SCIFA module, t_{pcyc} is a cycle time of a bus clock (Bϕ).

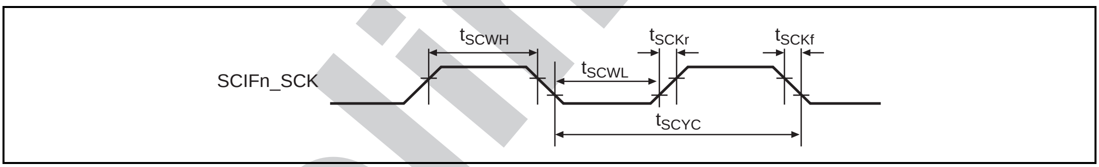


Figure 38.33 SCIF Module Signal Timing

Table 38.18 SCIF Module Signal Timing (Clocked Synchronous)

Item	Symbol	Min.	Max.	Unit	Figure
SCK input/output clock cycle	t_{SCYC}	12	—	t_{PCYC}	38.33
SCK input/output clock high level width	t_{SCWH}	0.4	—	t_{SCYC}	
SCK input/output clock low level width	t_{SCWL}	0.4	—	t_{SCYC}	
SCK input/output rise time (clocked synchronous)	t_{sSCKr}	—	1.5	t_{PCYC}	
SCK input/output fall time (clocked synchronous)	t_{sSCKf}	—	1.5	t_{PCYC}	
TXD output data delay time (SCK input)	t_{TXD}	—	$3 \times t_{pcyc} + 50$	ns	38.34
TXD output data delay time (SCK output)		—	50	ns	
RXD input data setup time (common to SCK input and output)	t_{RXS}	4	—	t_{PCYC}	
RXD input data hold time (common to SCK input and output)	t_{RXH}	4	—	t_{PCYC}	

Note: In SCIF module t_{pcyc} stands for a cycle time of a peripheral clock (Pϕ).
In SCIFA module t_{pcyc} stands for a cycle time of a bus clock (Bϕ).

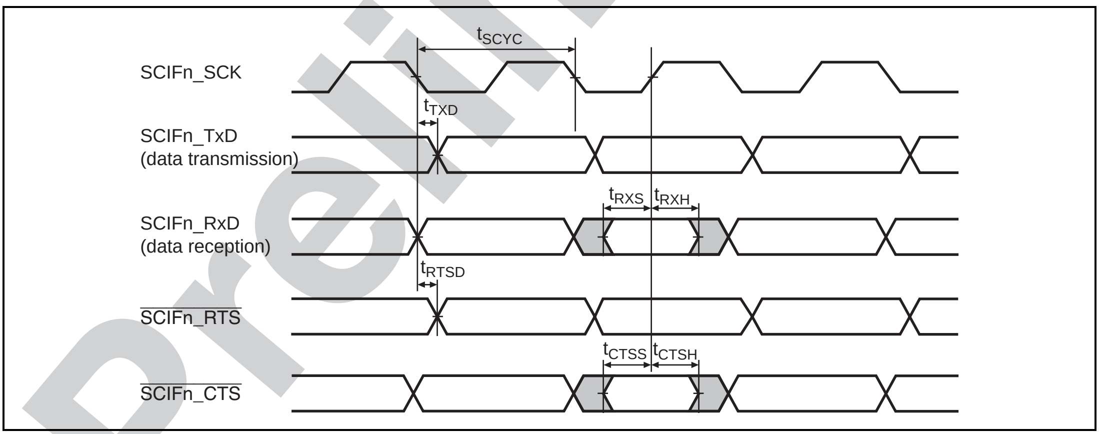


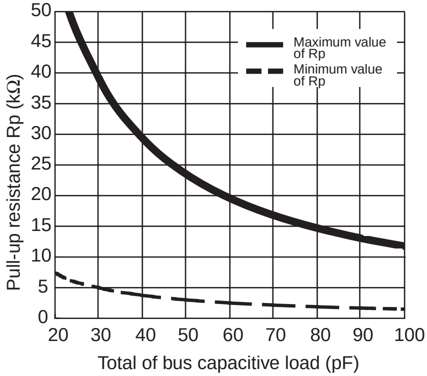
Figure 38.34 SCIF Module Signal Timing

38.5.10 I²C Module Signal Timing

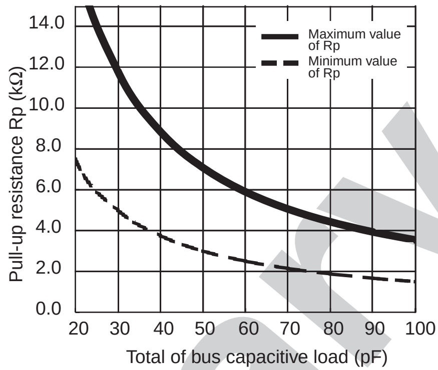
Table 38.19 SDA and SCL Bus Line Characteristics for I²C Bus Device

		Normal Mode		High-Speed Mode			
Item	**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**	**Figure**
SCL clock frequency	f_{SCL}	0	100	0	400	kHz	38.35
Hold time (after repeat START condition, first clock pulse is generated)	$t_{HD;STA}$	4.0	—	0.6	—	μs	
Low period in SCL clock	t_{LOW}	4.7	—	1.3	—	μs	
High period in SCL clock	t_{HIGH}	4.0	—	0.6	—	μs	
Setup time for repeat START condition	$t_{SU;STA}$	4.7	—	0.6	—	μs	
Data hold time: for I²C bus device	$t_{HD;DAT}$	—	3.45	—	0.9	μs	
Data setup time	$t_{SU;DAT}$	250	—	100	—	ns	
SDA and SCL signal rise time	t_r	—	1000	—	300	ns	
SDA and SCL signal fall time	t_f	—	300	—	300	ns	
Setup time for STOP condition	$t_{SU;STO}$	4.0	—	0.6	—	μs	
Bus free time between STOP and START conditions	t_{BUF}	4.7	—	1.3	—	μs	
Noise margin at low level of each connected device (including hysteresis)	V_{nL}	$0.1 \times V_{CC}Q$	—	$0.1 \times V_{CC}Q$	—	V	
Noise margin at high level of each connected device (including hysteresis)	V_{nH}	$0.2 \times V_{CC}Q$	—	$0.2 \times V_{CC}Q$	—	V	

Notes: 1. All values are referenced at $V_{CC}Q \times 0.3$ and $V_{CC}Q \times 0.7$ levels.
2. To satisfy the I²C-bus specification, pull-up resistors (Rp) with the appropriate resistance must be included depending on the total of bus capacitive load of each line.
3. Relationship between pull-up resistance and total capacitive load of the I²C bus.



(1) When SCL = 100 kHz



(2) When SCL = 400 kHz

* A hold time of at least 300 ns is internally assured for the SDA signal (relative to V_{IH}min of the SCL signal). The state of the SDA signal is stabilized on falling edges of the SCL signal.

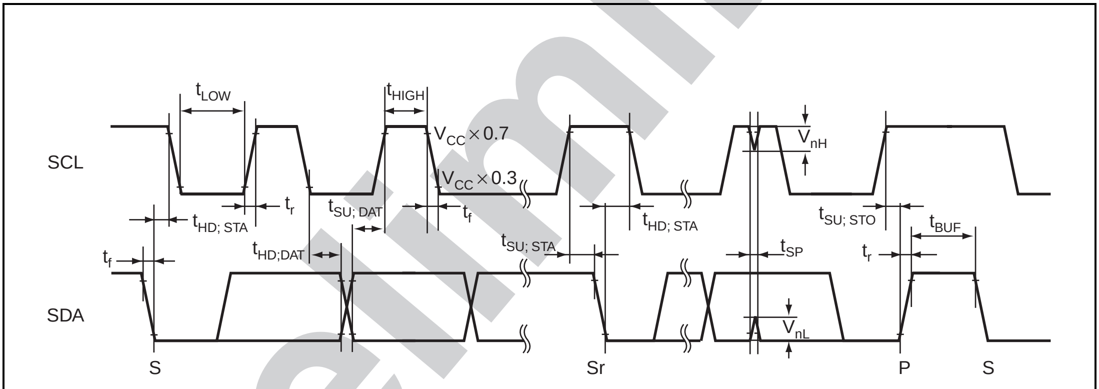


Figure 38.35 Device Timing Definition on I²C Bus

38.5.11 FLCTL Module Signal Timing

Table 38.20 NAND-Type Flash Memory Interface Timing

Item	Symbol	Min.	Max.	Unit	Figure
Command output setup time	t_{NCDS}	$2 \times t_{fcyc} - 10$	—	ns	38.36, 38.40
Command output hold time	t_{NCDH}	$1.5 \times t_{fcyc} - 5$	—	ns	
Data output setup time	t_{NDOS}	$0.5 \times t_{fcyc} - 5$	—	ns	38.36, 38.37, 38.39, 38.40
Data output hold time	t_{NDOH}	$0.5 \times t_{fcyc} - 10$	—	ns	
Command to address transition time 1	t_{NCDAD1}	$1.5 \times t_{fcyc} - 10$	—	ns	38.36, 38.37
Command to address transition time 2	t_{NCDAD2}	$2 \times t_{fcyc} - 10$	—	ns	38.37
$\overline{\text{FWE}}$ cycle time	t_{NWC}	$t_{fcyc} - 5$	—	ns	38.37, 38.39
$\overline{\text{FWE}}$ low pulse width	t_{NWP}	$0.5 \times t_{fcyc} - 5$	—	ns	38.36, 38.27, 38.39, 38.40
$\overline{\text{FWE}}$ high pulse width	t_{NWH}	$0.5 \times t_{fcyc} - 5$	—	ns	38.37, 38.39
Address to ready/busy transition time	t_{NADRB}	—	$32 \times t_{pcyc}$	ns	38.37, 38.38
Ready/busy to data read transition time 1	t_{NRBDR1}	$1.5 \times t_{fcyc}$	—	ns	38.38
Ready/busy to data read transition time 2	t_{NRBDR2}	$32 \times t_{pcyc}$	—	ns	
FSC cycle time	t_{NSCC}	$t_{fcyc} - 5$	—	ns	
FSC low pulse width	t_{NSP}	$0.5 \times t_{fcyc} - 5$	—	ns	38.38, 38.40
FSC high pulse width	t_{NSPH}	$0.5 \times t_{fcyc} - 5$	—	ns	38.38
Read data setup time	t_{NRDS}	24	—	ns	38.38, 38.40
Read data hold time	t_{NRDH}	5	—	ns	38.38, 38.40
Data write setup time	t_{NDWS}	$32 \times t_{pcyc}$	—	ns	38.39
Command to status read transition time	t_{NCDSR}	$4 \times t_{fcyc}$	—	ns	38.40
Command output off to status read transition time	t_{NCDFSR}	$3.5 \times t_{fcyc}$	—	ns	
Status read setup time	t_{NSTS}	$2.5 \times t_{fcyc}$	—	ns	

Note: t_{fcyc} indicates the period of one cycle of the FLCTL clock.
t_{pcyc} indicates the period of one cycle of the peripheral clock (Pϕ).

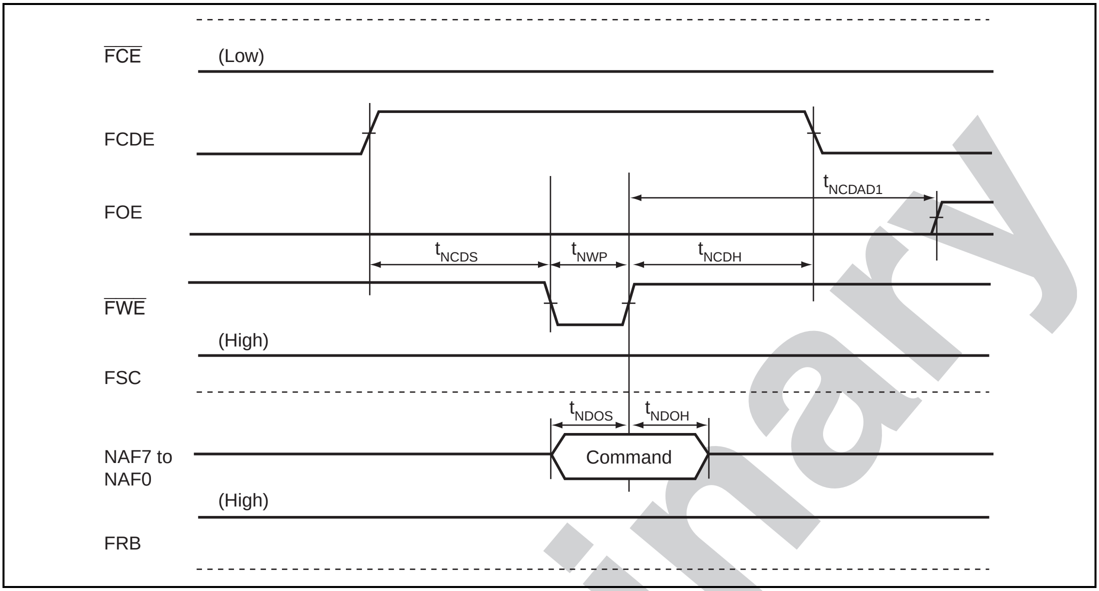


Figure 38.36 Command Issue Timing of NAND-Type Flash Memory

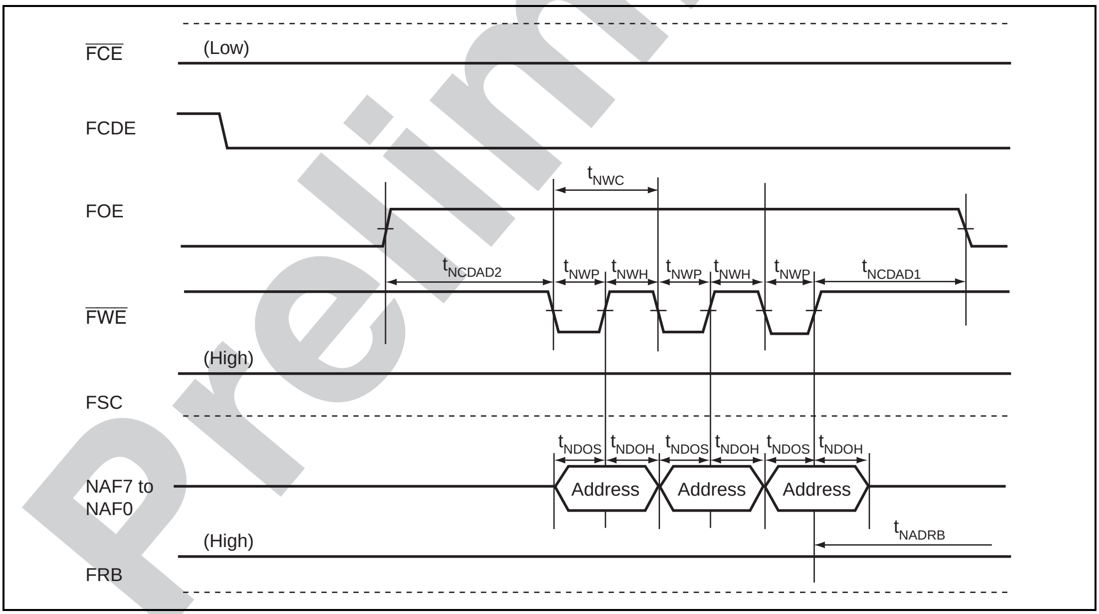


Figure 38.37 Address Issue Timing of NAND-Type Flash Memory

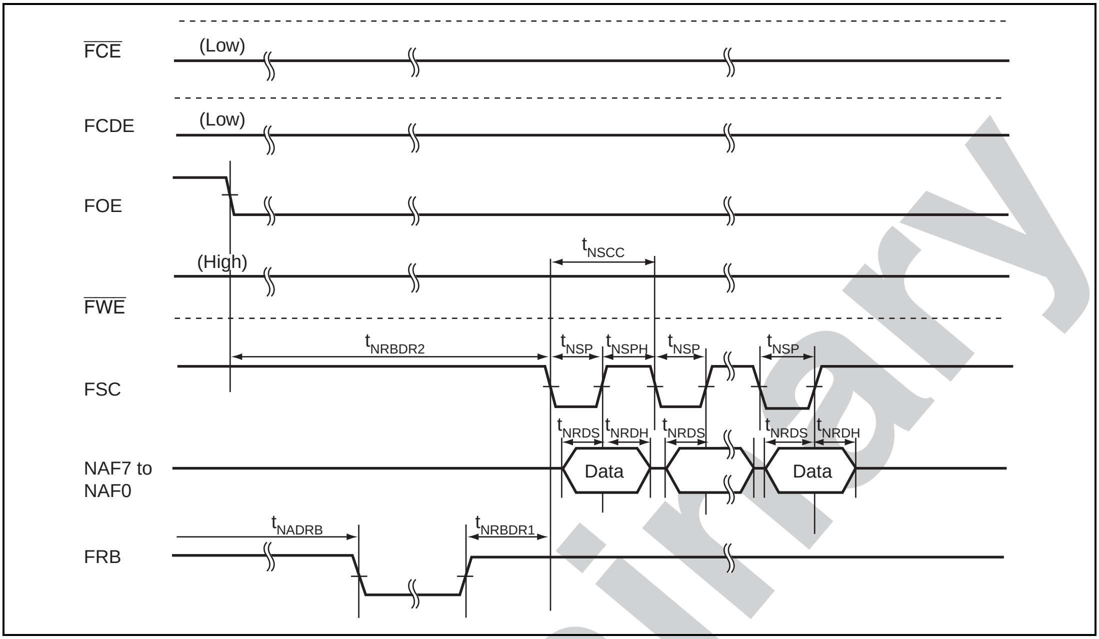


Figure 38.38 Data Read Timing of NAND-Type Flash Memory

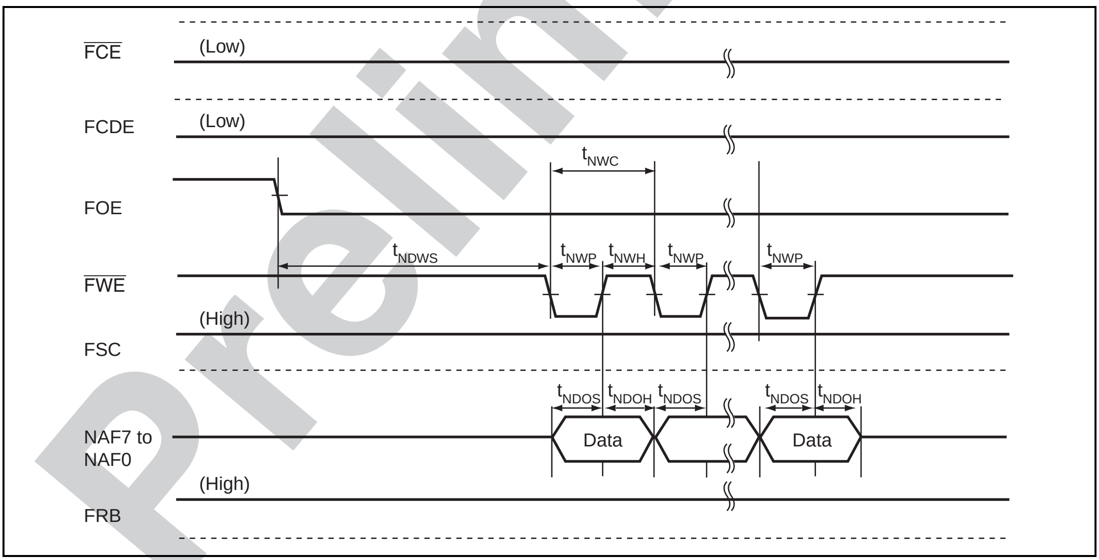


Figure 38.39 Data Write Timing of NAND-Type Flash Memory

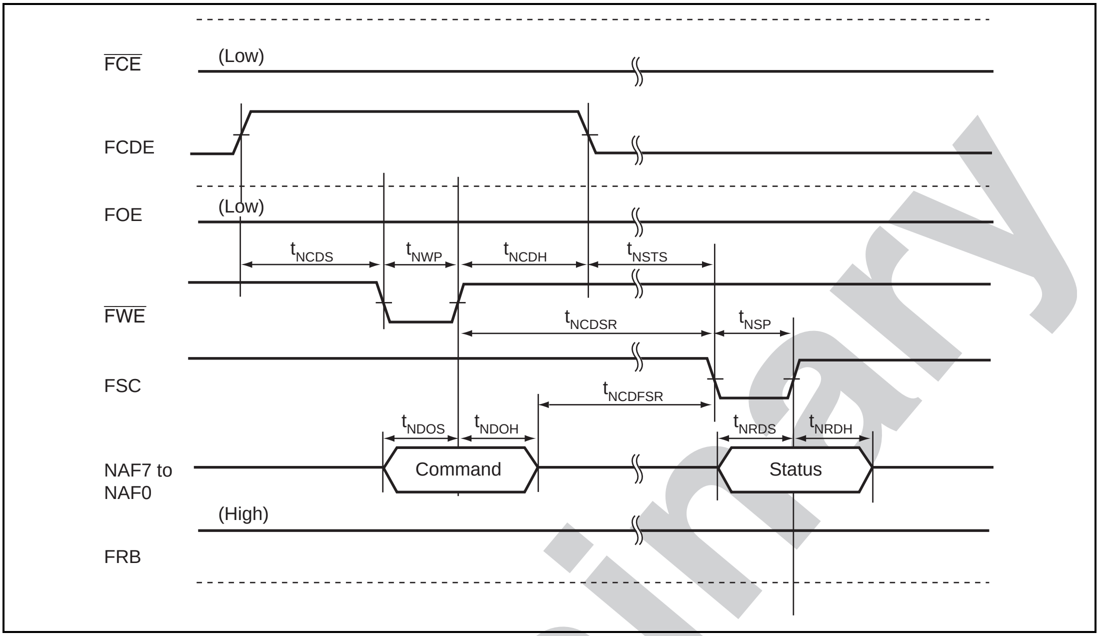


Figure 38.40 Status Read Timing of NAND-Type Flash Memory

38.5.12 VIO Module Signal Timing

Table 38.21 VIO Module Signal Timing

Item	Symbol	Min.	Max.	Unit	Figure
Vertical sync (VIO_VD) setup time	t_{VVDS}	10	—	ns	38.41
Vertical sync (VIO_VD) hold time	t_{VVDH}	10	—	ns	
Horizontal sync (VIO_HD) setup time	t_{VHDS}	10	—	ns	
Horizontal sync (VIO_HD) hold time	t_{VHDH}	10	—	ns	
Capture image data (VIO_D) setup time	t_{VDTS}	10	—	ns	
Capture image data (VIO_D) hold time	t_{VDTH}	10	—	ns	
Camera clock cycle	t_{VCYC}	t_{bcyc}*	—	ns	
Camera clock high width	t_{VHW}	$0.4 \times t_{Vcyc}$	—	ns	
Camera clock low width	t_{VLW}	$0.4 \times t_{Vcyc}$	—	ns	
Field identification signal (VIO_FLD) setup time	t_{VFDS}	10	—	ns	
Field identification signal (VIO_FLD) hold time	t_{VFDH}	10	—	ns	

Note: * t_{bcyc} is a cycle time of an internal bus clock (Bϕ).

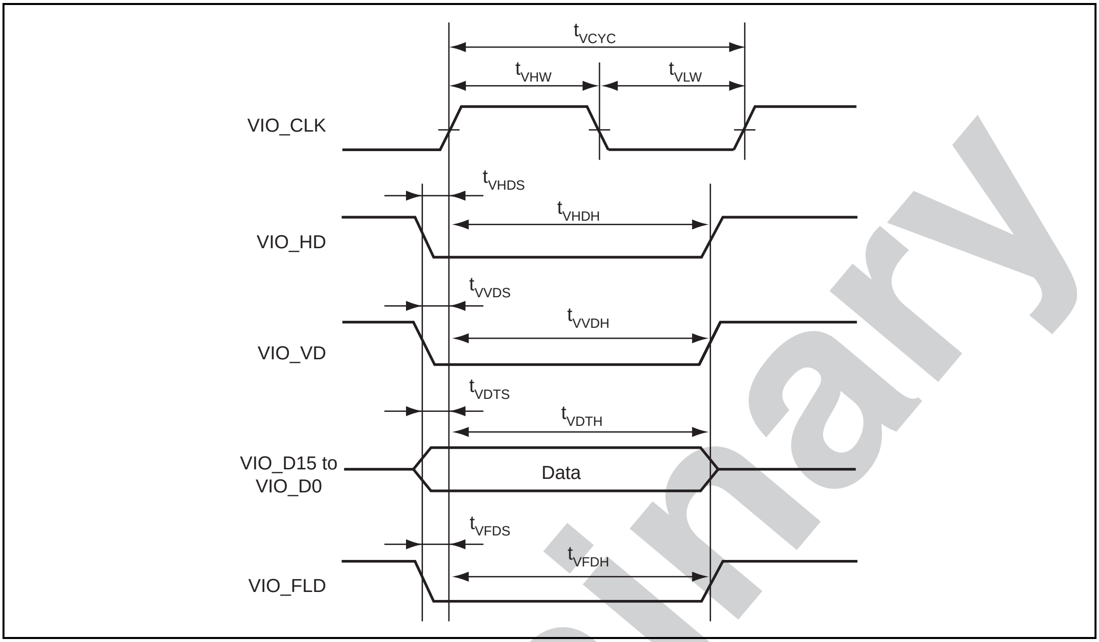


Figure 38.41 VIO Module Signal Timing

38.5.13 LCDC Module Signal Timing

Table 38.22 LCDC Module Signal Timing

Item	Symbol	Min.	Max.	Unit	Figure
Clock (LCDDCK) cycle time	t_{LCC}	30	—	ns	38.42
Clock (LCDDCK) high pulse time	t_{LCHW}	9	—	ns	
Clock (LCDDCK) low pulse time	t_{LCLW}	9	—	ns	
Data (LCDD) delay time	t_{LDD}	–12	12	ns	
Display enable (LCDDISP) delay time	t_{LID}	–12	12	ns	
Horizontal sync signal (LCDHSYN) delay time	t_{LHD}	–12	12	ns	
Vertical sync signal (LCDVSYN) delay time	t_{LVD}	–12	12	ns	
Chip select signal ($\overline{\text{LCDCS}}$) SYS interface command delay time	$t_{LSYSCSD}$	—	22	ns	38.43
Write strobe signal (LCDDCK) SYS interface command delay time	$t_{LSYSWRD}$	—	22	ns	
Register select signal (LCDDISP) SYS interface command delay time	$t_{LSYSRSD}$	—	22	ns	
Data (LCDD) SYS interface command write data delay time	t_{LSYSDD}	—	22	ns	
Read strobe signal ($\overline{\text{LCDRD}}$) SYS interface command delay time	$t_{LSYSRDD}$	—	22	ns	38.44
Data (LCDD) SYS interface read data setup time	$t_{LSYSRDS}$	10	—	ns	
Data (LCDD) SYS interface read data hold time	$t_{LSYSRDH}$	5	—	ns	
Read write signal (LCDVCPWC) SYS interface command delay time	$t_{LSYSRDWRD}$	–12	12	ns	
Write strobe signal ($\overline{\text{LCDWR}}$) SYS interface data cycle time	$t_{LSYSDWRC}$	30	—	ns	38.45
Write strobe signal ($\overline{\text{LCDWR}}$) SYS interface data high pulse time	$t_{LSYSDWRHW}$	9	—	ns	

Item	Symbol	Min.	Max.	Unit	Figure
Write strobe signal ($\overline{\text{LCDWR}}$) SYS interface data low pulse time	$t_{LSYSDWRLW}$	9	—	ns	38.45
Write strobe signal ($\overline{\text{LCDWR}}$) SYS interface data address setup time	$t_{LSYSDAS}$	$t_{LSYSDWRC}$ – 12	$t_{LSYSDWRC}$ + 12	ns	
Write strobe signal ($\overline{\text{LCDWR}}$) SYS interface data address hold time*	$t_{LSYSDAH}$	$t_{LSYSDWRHW}$ – 12	$1_{LSYSDWRHW}$ + 12	ns	
Data (LCDD) SYS interface data delay time	$t_{LSYSDDD}$	–12	12	ns	
Input vertical sync signal (LCDVSYN) setup time	t_{LVIS}	10	—	ns	38.46
Input vertical sync signal (LCDVSYN) hold time	t_{LVIH}	5	—	ns	

Note: * The minimum value of $t_{LSYSDAH}$ is one unit of $t_{LSYSDWRHW}$. $t_{LSYSDWRHW}$ can be arbitrarily set by LCDDCKPATxR (x = 1 to 4).

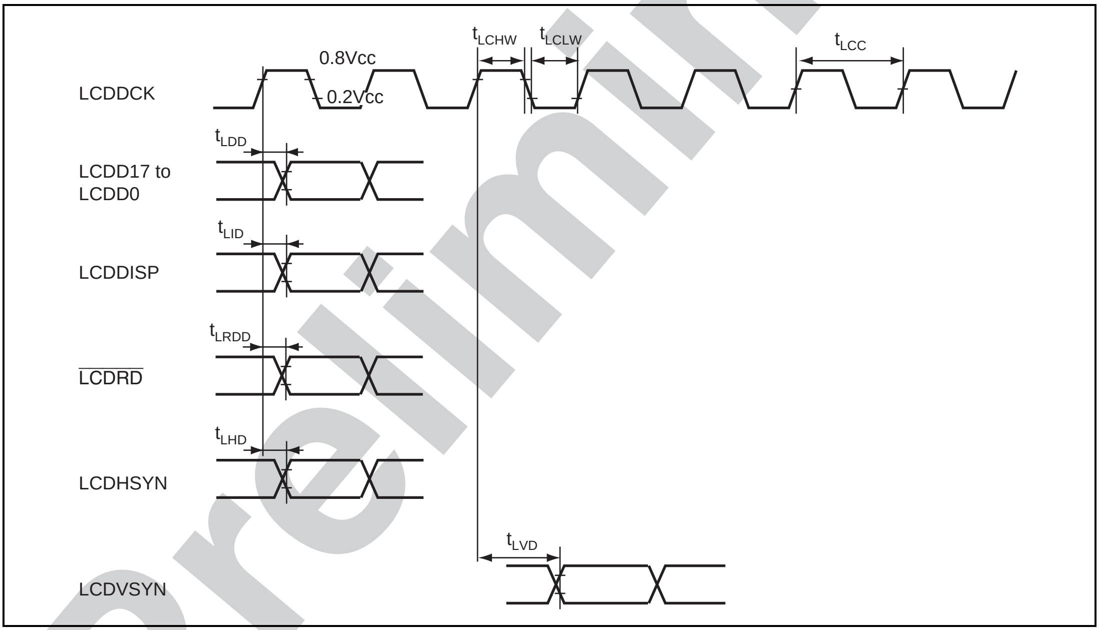


Figure 38.42 LCDC AC Characteristics

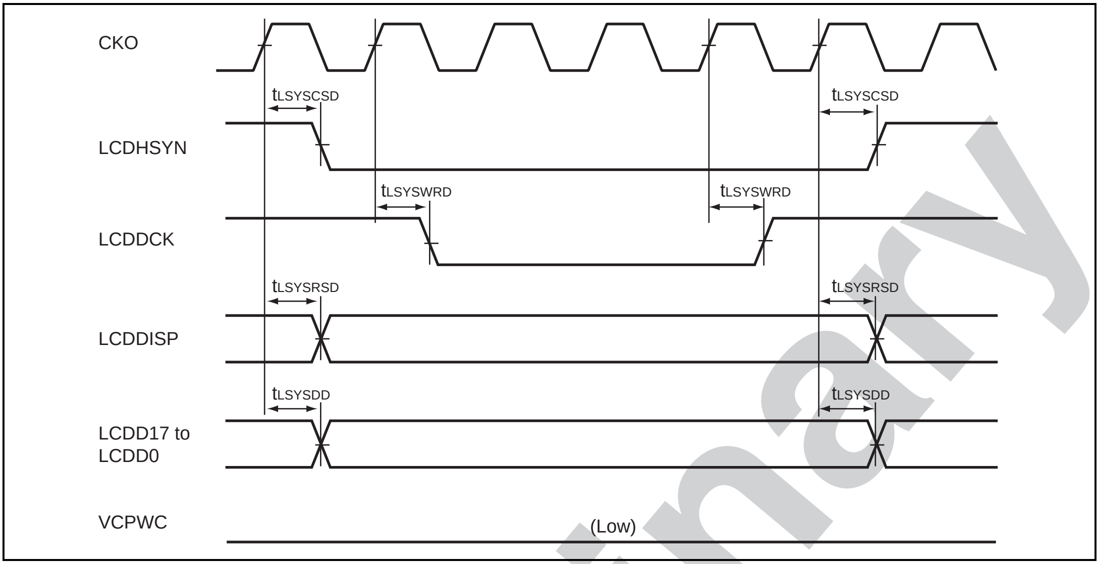


Figure 38.43 LCDC AC Characteristics SYS Interface, Command Write Bus Cycle (MLDMT2R.WCEC = 4, MLDMT2R.WCLW = 3, SLDMT2R.WCEC = 4, SLDMT2R.WCLW = 3)

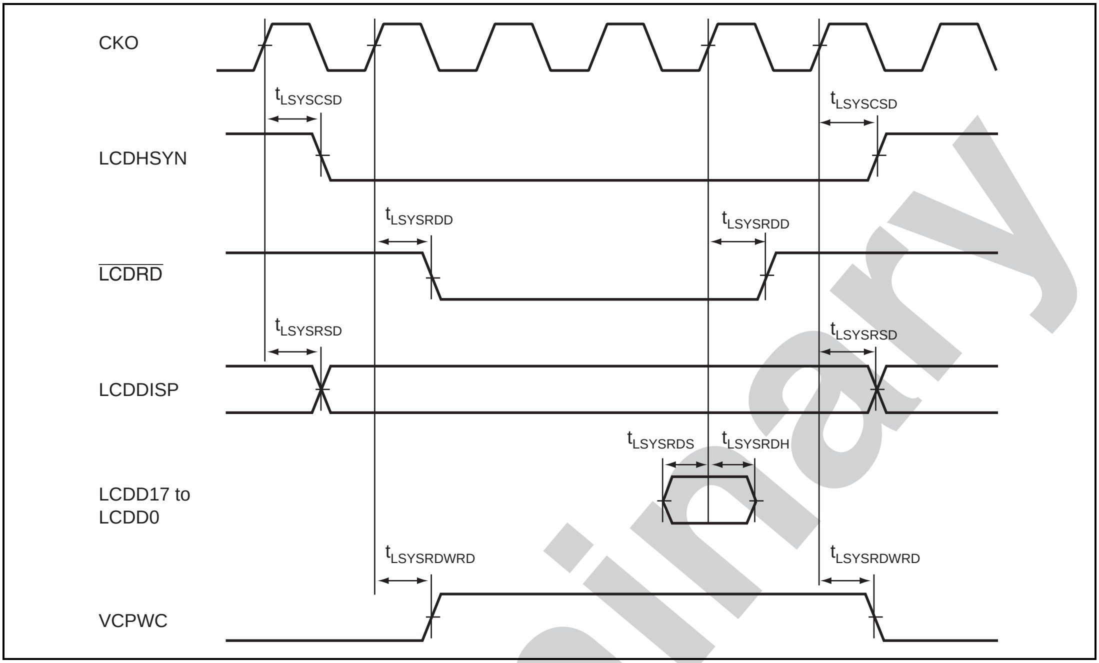


Figure 38.44 LCDC AC Characteristics SYS Interface, Command Read Bus Cycle (MLDMT3R.RDLC = 4, MLDMT3R.RCEC = 4, MLDMT3R.RCLW = 3, SLDMT3R.RDLC = 4, SLDMT3R.RDLC = 4, SLDMT3R.RCEC = 4, SLDMT3R.RCLW = 3)

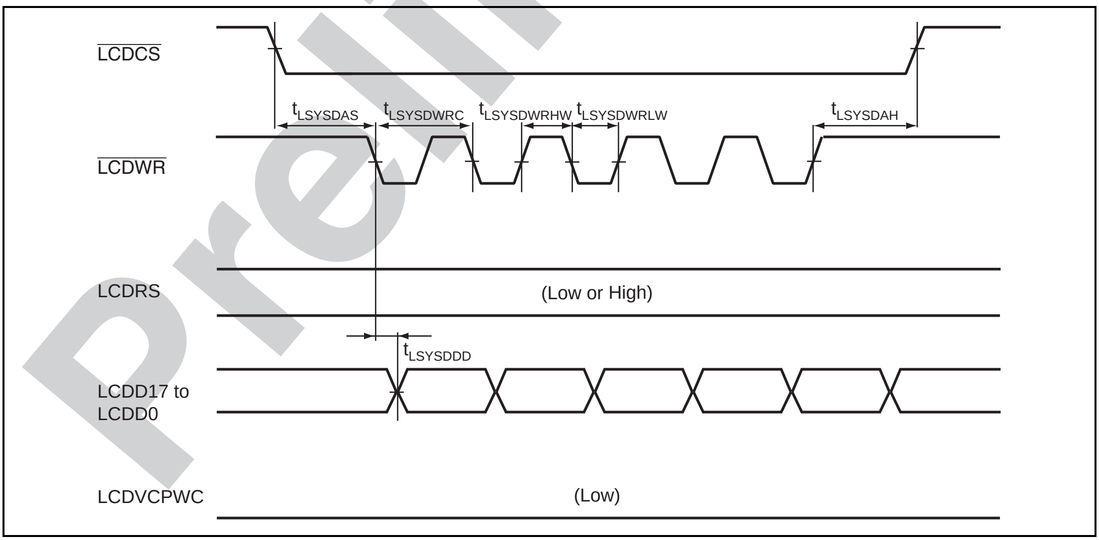


Figure 38.45 LCDC AC Characteristics (SYS Interface, Data Write Bus Cycle)

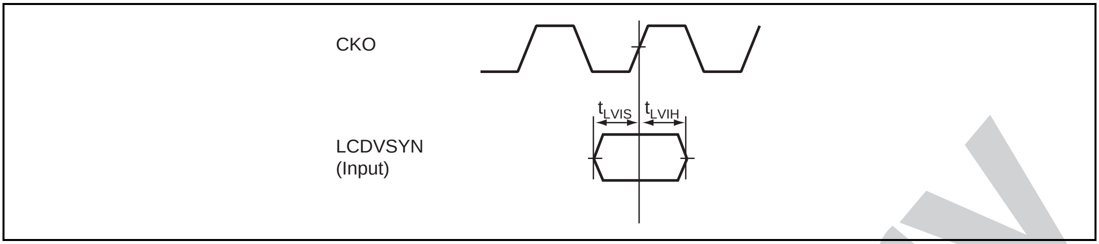


Figure 38.46 LCDC AC Characteristics (VSYNC Input Mode)

38.5.14 VOU Module Signal Timing

Table 38.23 VOU Module Signal Timing

Item	Symbol	Min.	Typ.	Max.	Unit	Figure
Output clock frequency	f_{px1}	13.5	—	27	MHz	38.47
Output clock cycle	t_{pxcyc1}	37	—	74.1	ns	
Output clock high width	t_{pxwH1}	14	—	—	ns	
Output clock low width	t_{pxwL1}	14	—	—	ns	
Output data delay time	t_{pxd1}	–4	—	4	ns	
Output clock frequency 2	f_{px2}	13.5	—	27	MHz	38.48
Output clock cycle 2	t_{pxcyc2}	37	—	74.1	ns	
Output clock high width 2	t_{pxwH2}	14	—	—	ns	
Output clock low width 2	t_{pxwL2}	14	—	—	ns	
Output data delay time 2	t_{pxd2}	–4	—	4	ns	

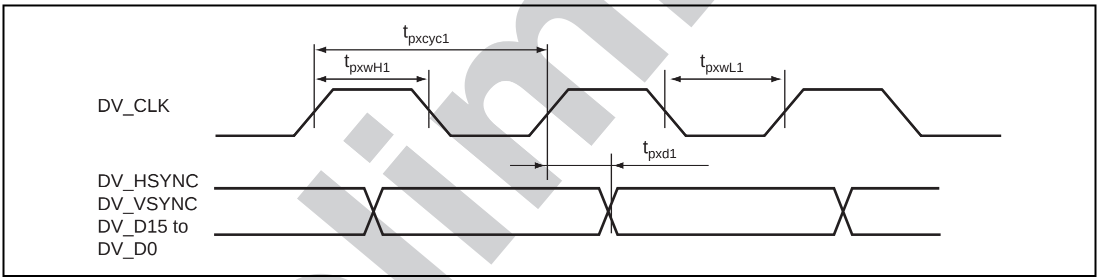


Figure 38.47 VOU AC Characteristics (VOUCR.CKPL = 0)

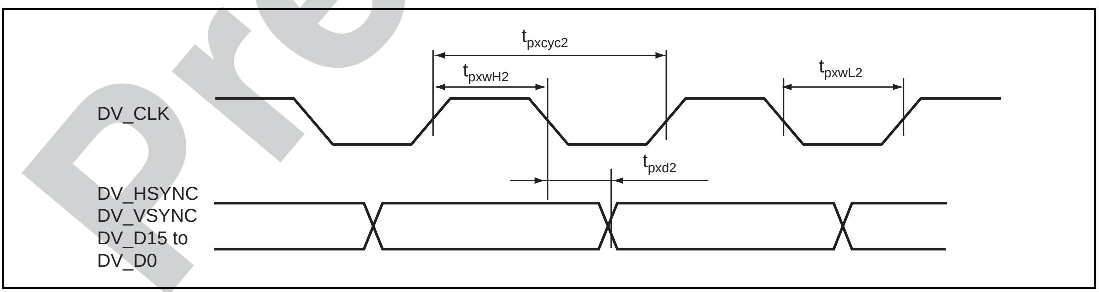


Figure 38.48 VOU AC Characteristics (VOUCR.CKPL = 1)

38.5.15 TSIF Module Signal Timing

Table 38.24 TSIF Module Signal Timing

Item		Symbol	Min.	Max.	Unit	Figure
TSIF input clock cycle	Bϕ ≥ 40 MHz	t_{TSCYC}	25	—	ns	38.49
	Bϕ < 40 MHz	t_{TSCYC}	t_{bcyc}*	—	ns	
TSIF input clock high width		t_{TSHW}	0.4 × t_{TSCYC}	—	ns	
TSIF input clock low width		t_{TSLW}	0.4 × t_{TSCYC}	—	ns	
TSIF input data setup time		t_{TSDTS}	5	—	ns	
TSIF input data hold time		t_{TSDTH}	5	—	ns	
TSIF input data enable signal setup time		t_{TSDES}	5	—	ns	
TSIF input data enable signal hold time		t_{TSDEH}	5	—	ns	
TSIF input data sync signal setup time		t_{TSSYS}	5	—	ns	
TSIF input data sync signal hold time		t_{TSSYH}	5	—	ns	

Note: * t_{bcyc} is a cycle time of an internal bus clock (Bϕ).

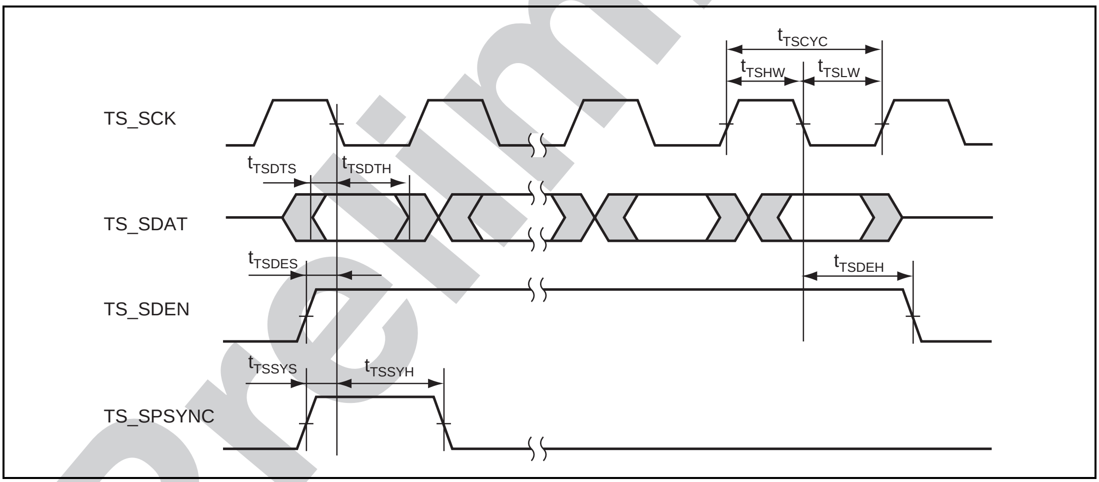


Figure 38.49 TSIF Module Signal Timing (TSCTLR.TSDATP = 0, TSCTLR.TSCLKP = 1, TSCTLR.TSVLDP = 0, TSCTLR.PSYCP = 0)

38.5.16 SIU Module Signal Timing

Table 38.25 SIU Module Signal Timing

Item	Symbol	Min.	Max.	Unit	Figure
SIUMCK clock input cycle time	$t_{SIUMCYC}$	40	—	ns	38.51
SIUMCK input high width	t_{SIUMWH}	$0.4 \times t_{SIUMCYC}$	—	ns	
SIUMCK input low width	t_{SIUMWL}	$0.4 \times t_{SIUMCYC}$	—	ns	
SIU_BT clock cycle time	$t_{SIUSICYC}$	300	—	ns	38.50
SIU_BT output high width	$t_{SIUSWHO}$	$0.4 \times t_{SIUSICYC}$	—	ns	
SIU_BT output low width	$t_{SIUSWLO}$	$0.4 \times t_{SIUSICYC}$	—	ns	
SIU_LR output delay time	t_{SIUFSD}	—	20	ns	
SIU_BT input high width	$t_{SIUSWHI}$	$0.4 \times t_{SIUSICYC}$	—	ns	
SIU_BT input low width	$t_{SIUSWLI}$	$0.4 \times t_{SIUSICYC}$	—	ns	
SIU_SLD output delay time	$t_{SIUSTDD}$	—	20	ns	
SIU_SLD input setup time	$t_{SIUSRDS}$	20	—	ns	
SIU_SLD input hold time	$t_{SIUSRDH}$	20	—	ns	

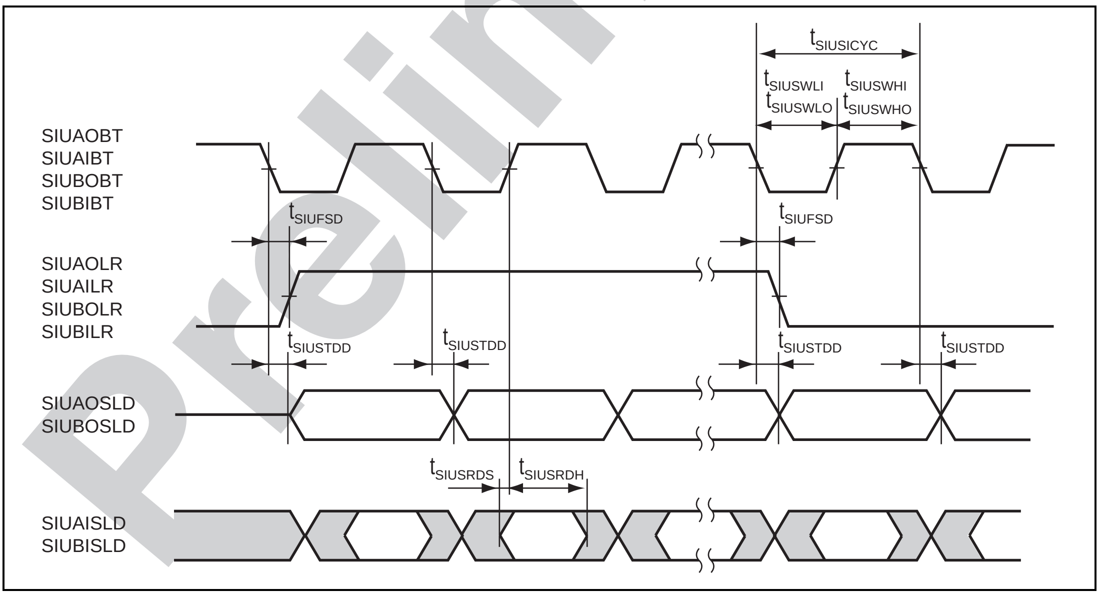


Figure 38.50 SIU Transmission Timing

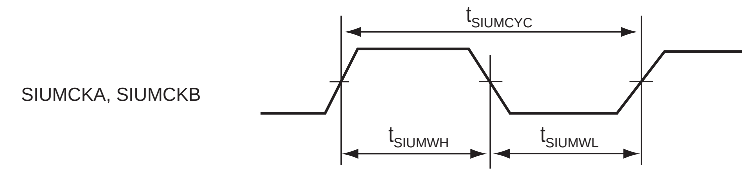
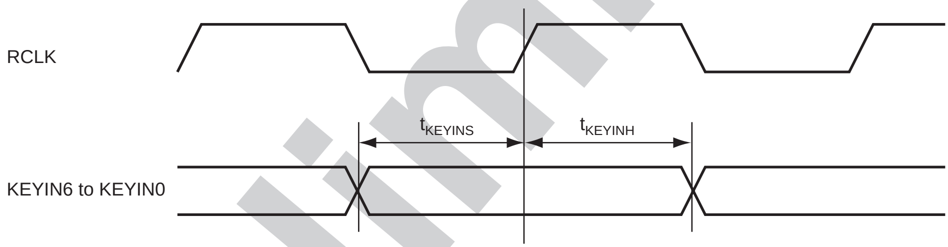


Figure 38.51 SIUMCK Input Timing

38.5.17 KEYSC Module Signal Timing

Table 38.26 KEYSC Module Signal Timing

Item	Symbol	Min.	Max.	Unit	Figure
KEYIN input setup time	t_{KEYINS}	15	—	ns	38.52
KEYIN input hold time	t_{KEYINH}	15	—	ns	
KEYOUT delay time	$t_{KEYOUTD}$	—	15	ns	38.53



Note: KEYIN is an asynchronous signal.
When the setup time in this figure is satisfied, a change is detected at the rising edge of the clock.
When the setup time is not satisfied, a change may not be detected until the next rising edge of the clock.

Figure 38.52 KEYIN Input Timing

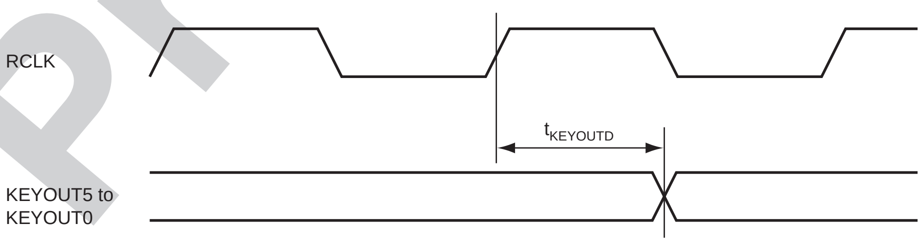


Figure 38.53 KEYOUT Output Timing

38.5.18 ATAPI Interface Module Signal Timing

Table 38.27 Symbols of PIO Transfer Timing of ATAPI Interface

Symbol	Item
t0	Cycle time
t1	Address setup time
t2	$\overline{\text{IDEIORD}}$/$\overline{\text{IDEIOWR}}$ pulse width 8 bits
t2i	$\overline{\text{IDEIORD}}$/$\overline{\text{IDEIOWR}}$ recovery time
t3	$\overline{\text{IDEIOWR}}$ data setup time
t4	$\overline{\text{IDEIOWR}}$ data hold time
t5	$\overline{\text{IDEIORD}}$ data setup time
t6	$\overline{\text{IDEIORD}}$ data hold time
t6z	$\overline{\text{IDEIORD3}}$ state delay time
t9	Address hold time
tRD	IDEIORDY read data valid time
tA	IDEIORDY setup time
tB	IDEIORDY pulse time
tC	Time from IDEIORDY negation to high impedance

Table 38.28 Register Access Timing using PIO Transfer of ATAPI Interface

	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4			
Symbol	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**	**Figure**
t0	600	—	383	—	330	—	180	—	120	—	ns	38.54
t1	70	—	50	—	30	—	30	—	25	—	ns	
t2	290	—	290	—	290	—	80	—	70	—	ns	
t2i	—	—	—	—	—	—	70	—	25	—	ns	
t3	60	—	45	—	30	—	30	—	20	—	ns	
t4	30	—	20	—	15	—	10	—	10	—	ns	
t5	50	—	35	—	20	—	20	—	20	—	ns	
t6	5	—	5	—	5	—	5	—	5	—	ns	
t6z	—	30	—	30	—	30	—	30	—	30	ns	
t9	20	—	15	—	10	—	10	—	10	—	ns	
tRD	0	—	0	—	0	—	0	—	0	—	ns	
tA	35	—	35	—	35	—	35	—	35	—	ns	
tB	—	1250	—	1250	—	1250	—	1250	—	1250	ns	
tC	5	—	5	—	5	—	5	—	5	—	ns	

Table 38.29 Data Transfer Timing using PIO Transfer of ATAPI Interface

	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4			
Symbol	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**	**Figure**
t0	600	—	383	—	240	—	180	—	120	—	ns	38.54
t1	70	—	50	—	30	—	30	—	25	—	ns	
t2	290	—	290	—	290	—	80	—	70	—	ns	
t2i	—	—	—	—	—	—	70	—	25	—	ns	
t3	60	—	45	—	30	—	30	—	20	—	ns	
t4	30	—	20	—	15	—	10	—	10	—	ns	
t5	50	—	35	—	20	—	20	—	20	—	ns	
t6	5	—	5	—	5	—	5	—	5	—	ns	
t6z	—	30	—	30	—	30	—	30	—	30	ns	
t9	20	—	15	—	10	—	10	—	10	—	ns	
tRD	0	—	0	—	0	—	0	—	0	—	ns	
tA	35	—	35	—	35	—	35	—	35	—	ns	
tB	—	1250	—	1250	—	1250	—	1250	—	1250	ns	
tC	5	—	5	—	5	—	5	—	5	—	ns	

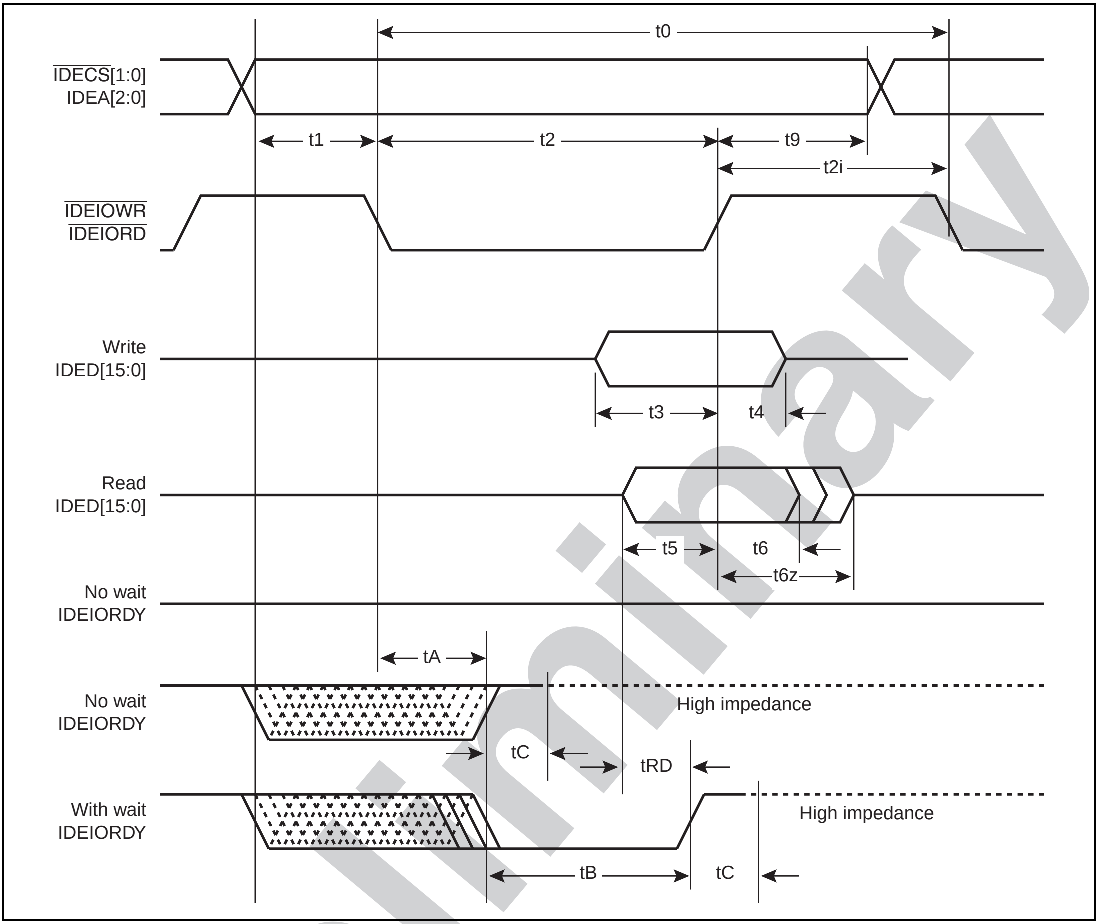


Figure 38.54 PIO Data Transfer and Register Transfer between Devices

Table 38.30 Symbols of Multiword Transfer Timing of ATAPI Interface

Symbol	Item
t0	Cycle time
tD	$\overline{\text{IDEIORD}}$/$\overline{\text{IDEIOWR}}$ pulse width
tE	$\overline{\text{IDEIORD}}$ data access time
tF	$\overline{\text{IDEIORD}}$ data hold time
tG	$\overline{\text{IDEIORD}}$/$\overline{\text{IDEIOWR}}$ data setup time
tH	$\overline{\text{IDEIOWR}}$ data hold time
tI	$\overline{\text{IODACK}}$ setup time
tJ	$\overline{\text{IODACK}}$ hold time
tKR	$\overline{\text{IDEIORD}}$ negate pulse width
tKW	$\overline{\text{IDEIOWR}}$ negate pulse width
tLR	$\overline{\text{IDEIORD}}$ · IODREQ delay time
tLW	$\overline{\text{IDEIOWR}}$ · IODREQ delay time
tM	$\overline{\text{IDECS}}$[1:0] setup time
tN	$\overline{\text{IDECS}}$[1:0] hold time
tZ	$\overline{\text{IODACK}}$3 state delay time

Table 38.31 Multiword Transfer Timing of ATAPI Interface

	Mode 0		Mode 1		Mode 2			
Symbol	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**	**Figure**
t0	480	—	150	—	120	—	ns	38.56 to 38.58
tD	215	—	80	—	70	—	ns	38.55 to 38.58
tE	—	150	—	60	—	50	ns	
tF	5	—	5	—	5	—	ns	
tG	100	—	30	—	20	—	ns	
tH	20	—	15	—	10	—	ns	
tI	0	—	0	—	0	—	ns	38.55
tJ	20	—	5	—	5	—	ns	38.55, 38.58
tKR	50	—	50	—	25	—	ns	38.56 to 38.58
tKW	215	—	50	—	25	—	ns	
tLR	—	120	—	40	—	35	ns	38.57
tLW	—	40	—	40	—	35	ns	
tM	50	—	30	—	25	—	ns	
tN	15	—	10	—	10	—	ns	38.57, 38.58
tZ	—	20	—	25	—	25	ns	

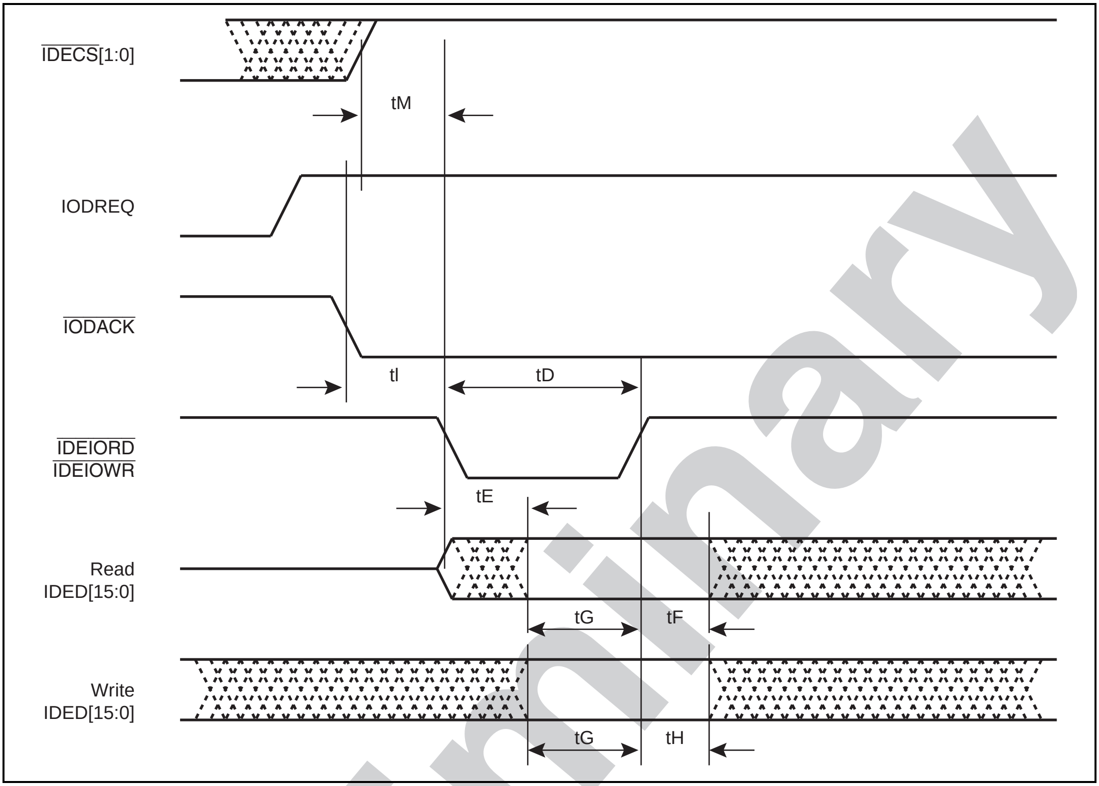


Figure 38.55 Start of Multiword DMA Data Transfer

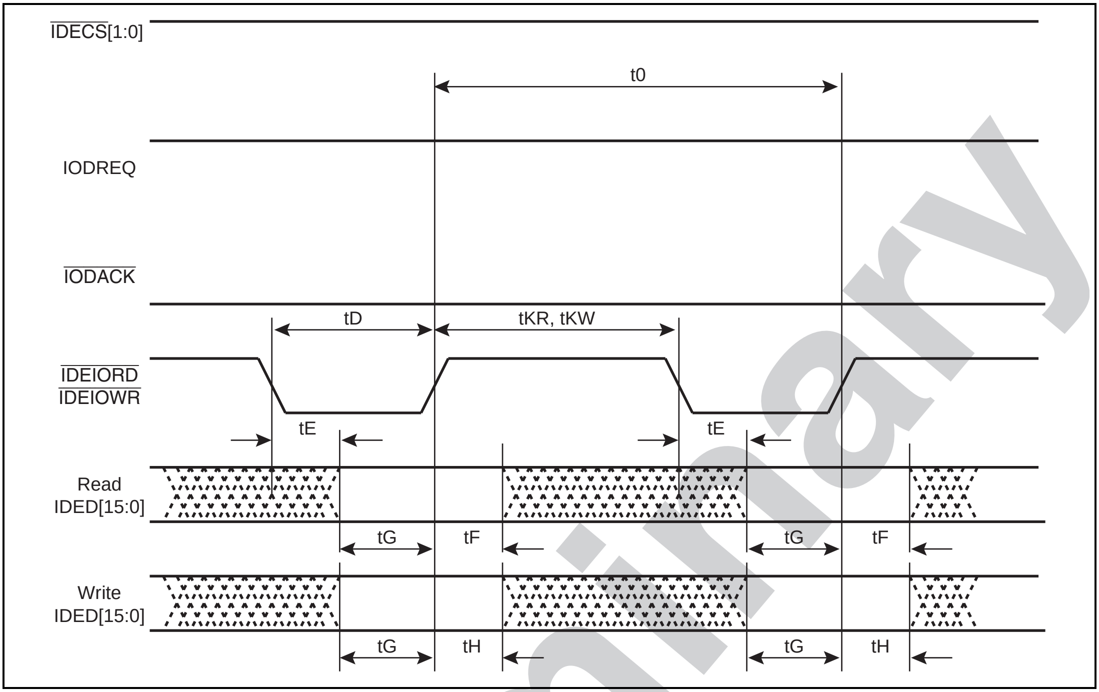


Figure 38.56 Multiword DMA Data Transfer

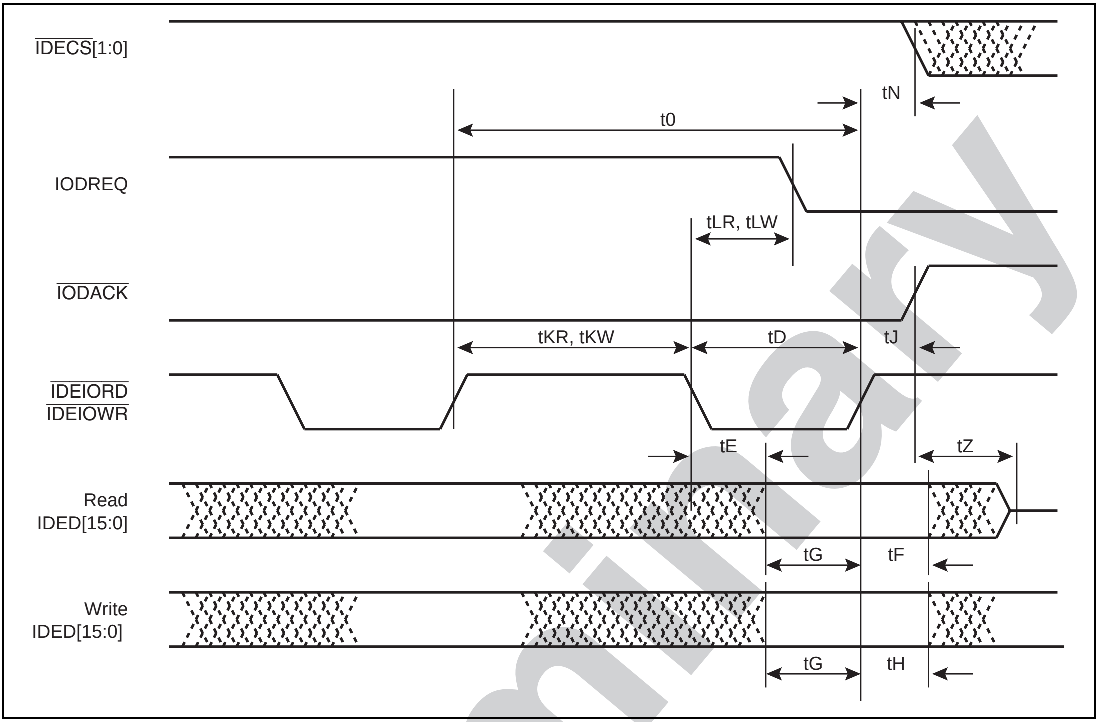


Figure 38.57 End of Multiword DMA Data Transfer from Device

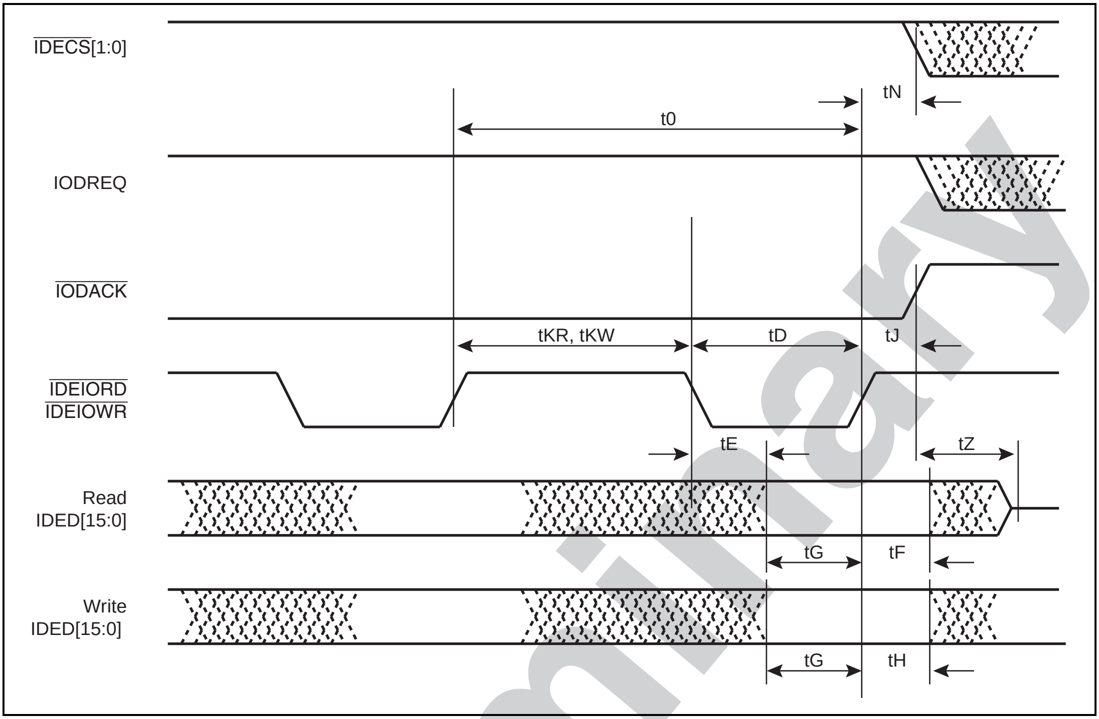


Figure 38.58 End of Multiword DMA Data Transfer from Host

Table 38.32 Symbols of Ultra DMA Transfer Timing of ATAPI Interface

Symbol	Item
t2CYCTYP	Average cycle time (two cycles)
tCYC	Cycle time
t2CYC	Minimum cycle time (two cycles)
tDS	Data setup time (receiver side)
tDH	Data hold time (receiver side)
tDVS	Data setup time (transmitter side)
tDVH	Data hold time (transmitter side)
tCS	CRC data setup time (receiver side)
tCH	CRC data hold time (receiver side)
tCVS	CRC data setup time (transmitter side)
tCVH	CRC data hold time (transmitter side)
tZFS	Setup time from drive of strobe to first STROBE (transmitter side)
tDZFS	Setup time from drive of data to first STROBE (transmitter side)
tFS	First STROBE time
tLI	Limited interlock time
tMLI	Minimum interlock time
tUI	Unlimited interlock time
tAZ	Output release time
tZAH	Output delay time
tZAD	Output determination time (from release)
tENV	Envelope time
tRFS	Last STROBE time
tRP	Time until STOP is asserted or DMARQ is negated
tIORDYZ	Time until IORDY is released
tZIORDY	Time until STROBE is driven
tACK	$\overline{\text{DMACK}}$ setup/hold time
tSS	Strobe stop time

Table 38.33 Ultra DMA Transfer Timing of ATAPI Interface

	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4			
Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Figure
t2CYCTYP	240	—	160	—	120	—	90	—	60	—	ns	38.60
tCYC	112	—	73	—	54	—	39	—	25	—	ns	38.60, 38.65
t2CYC	230	—	153	—	115	—	86	—	57	—	ns	
tDS	15	—	10	—	7	—	7	—	5	—	ns	
tDH	5	—	5	—	5	—	5	—	5	—	ns	
tDVS	70	—	48	—	31	—	20	—	6.7	—	ns	38.59, 38.60, 38.64, 38.65
tDVH	6.2	—	6.2	—	6.2	—	6.2	—	6.2	—	ns	
tCS	15	—	10	—	7	—	7	—	5	—	ns	
tCH	5	—	5	—	5	—	5	—	5	—	ns	
tCVS	70	—	48	—	31	—	20	—	6.7	—	ns	38.62, 38.63, 38.67, 38.68
tCVH	6.2	—	6.2	—	6.2	—	6.2	—	6.2	—	ns	
tZFS	0	—	0	—	0	—	0	—	0	—	ns	38.59
tDZFS	70	—	48	—	31	—	20	—	6.7	—	ns	38.59, 38.64
tFS	—	230	—	200	—	170	—	130	—	120	ns	38.59
tLI	0	150	0	150	0	150	0	100	0	100	ns	38.62 to 38.64, 38.67, 38.68
tMLI	20	—	20	—	20	—	20	—	20	—	ns	38.62, 38.63, 38.67, 38.68
tUI	0	—	0	—	0	—	0	—	0	—	ns	38.59, 38.64

	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4			
Symbol	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**	**Figure**
tAZ	—	10	—	10	—	10	—	10	—	10	ns	38.59, 38.62, 38.63
tZAH	20	—	20	—	20	—	20	—	20	—	ns	38.62, 38.63
tZAD	0	—	0	—	0	—	0	—	0	—	ns	38.59
tENV	20	70	20	70	20	70	20	55	20	55	ns	38.59, 38.64
tRFS	—	75	—	70	—	60	—	60	—	60	ns	38.61, 38.63, 38.66, 38.68
tRP	160	—	125	—	100	—	100	—	100	—	ns	
tIORDYZ	—	20	—	20	—	20	—	20	—	20	ns	38.62, 38.63, 38.66, 38.68
tZIORDY	0	—	0	—	0	—	0	—	0	—	ns	38.59, 38.64
tACK	20	—	20	—	20	—	20	—	20	—	ns	38.59, 38.62 to 38.64, 38.67, 38.68
tSS	50	—	50	—	50	—	50	—	50	—	ns	38.62, 38.67

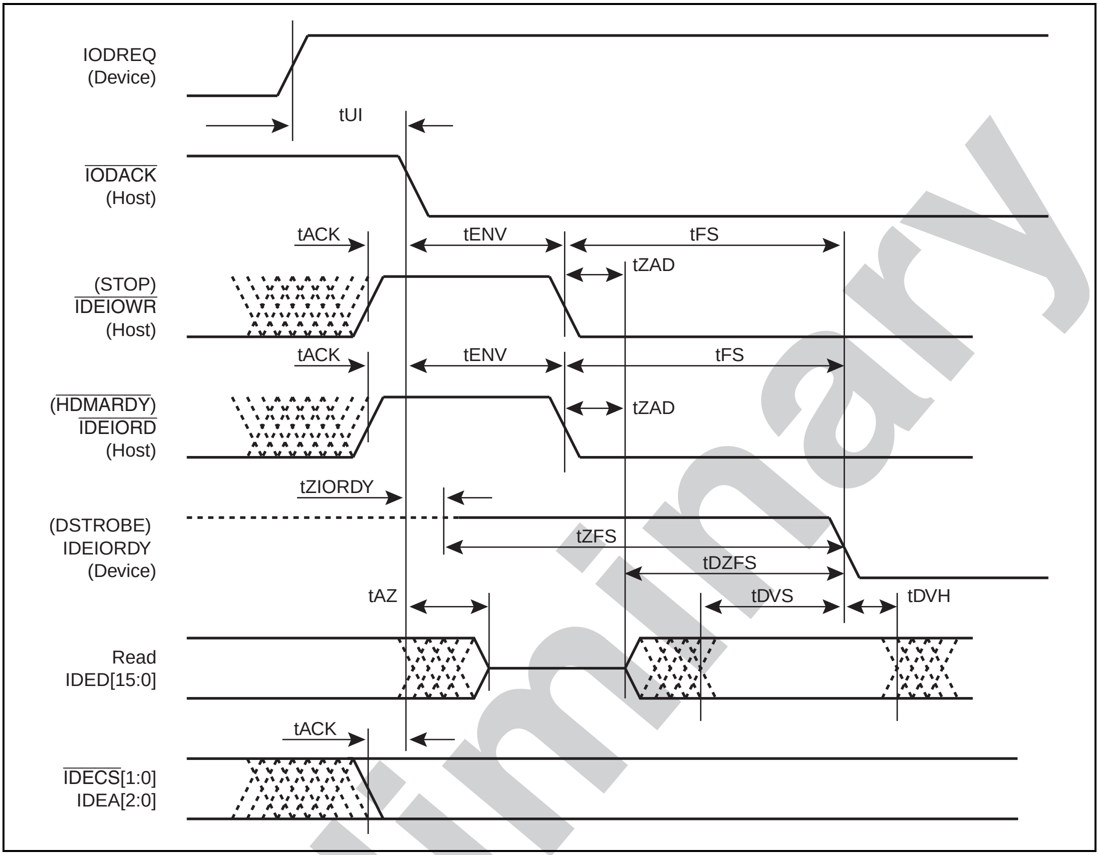


Figure 38.59 Start of Ultra DMA Transfer Data In Burst

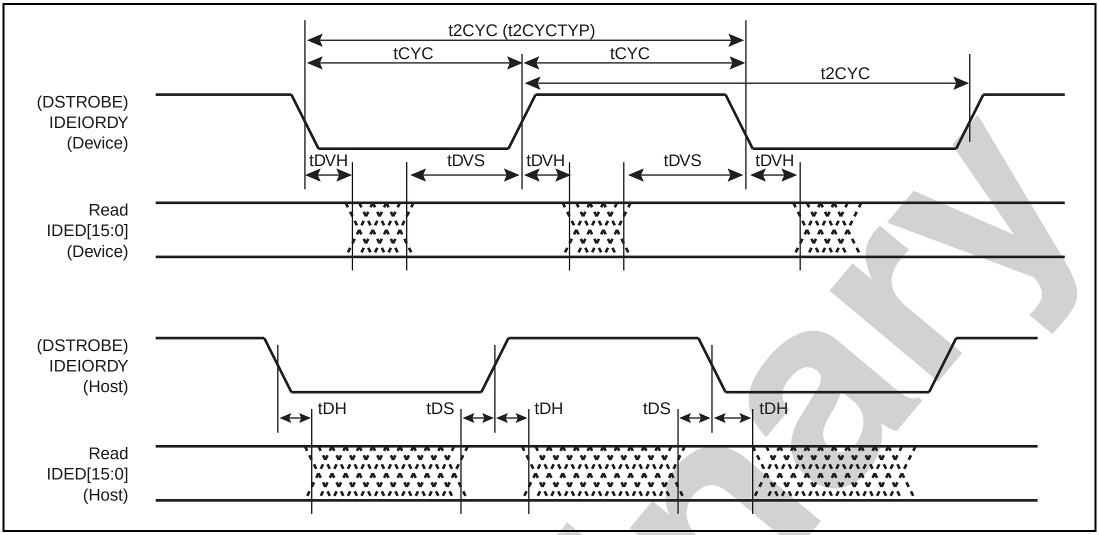


Figure 38.60 Ultra DMA Transfer Data In Burst

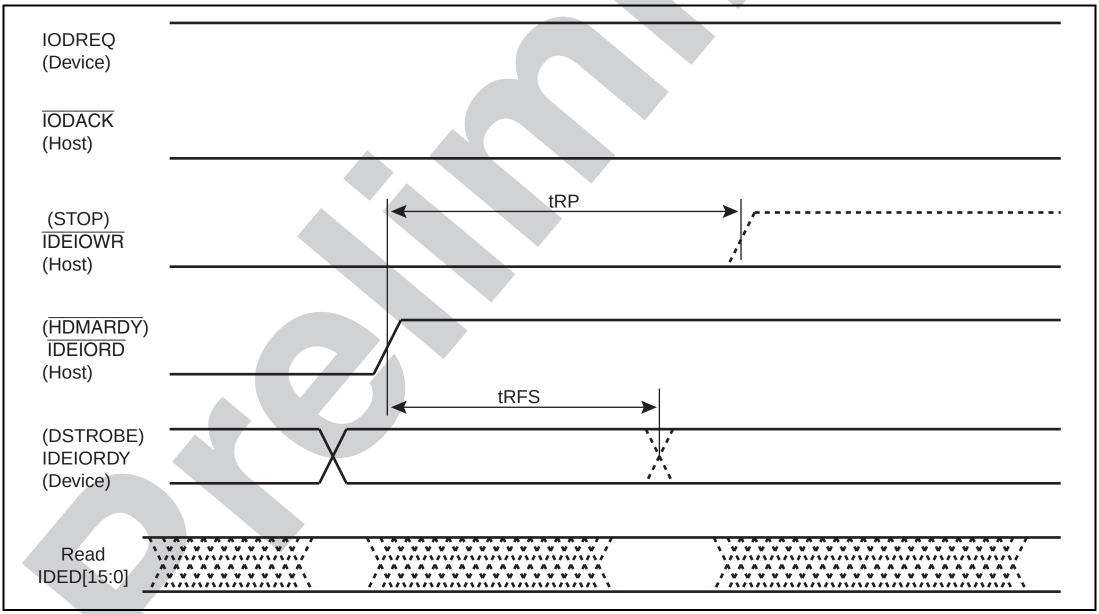


Figure 38.61 Pause of Ultra DMA Transfer Data In Burst from Host

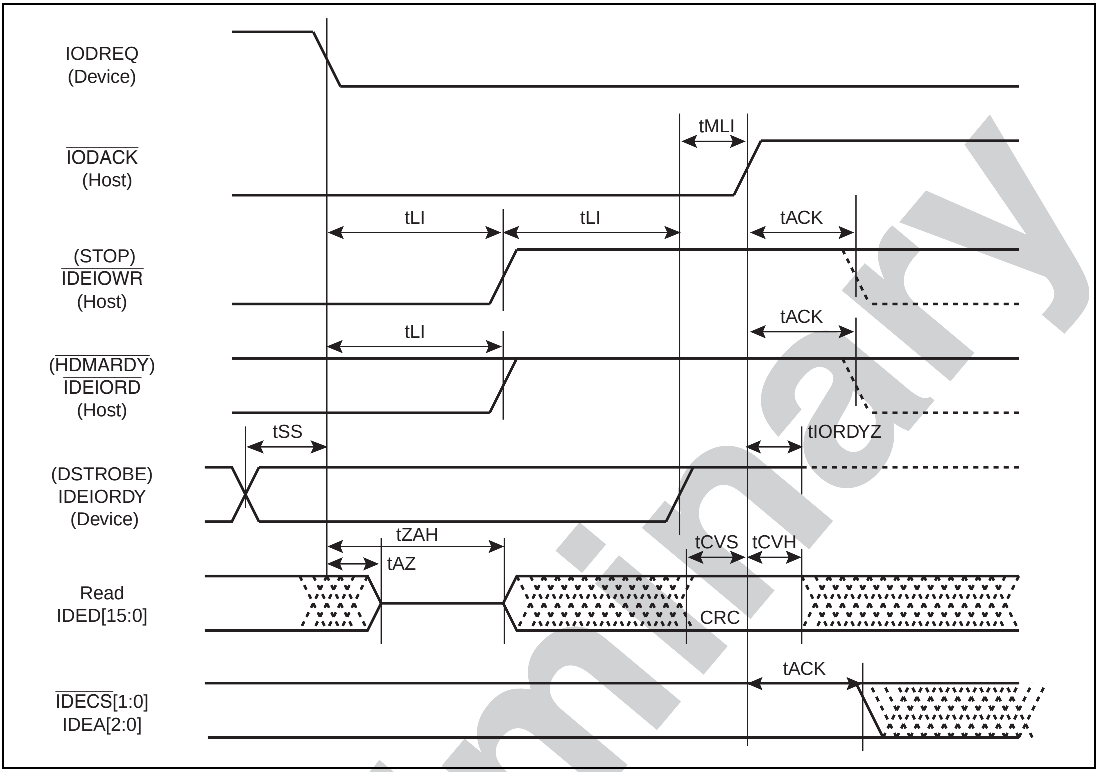


Figure 38.62 End of Ultra DMA Transfer Data In Burst from Device

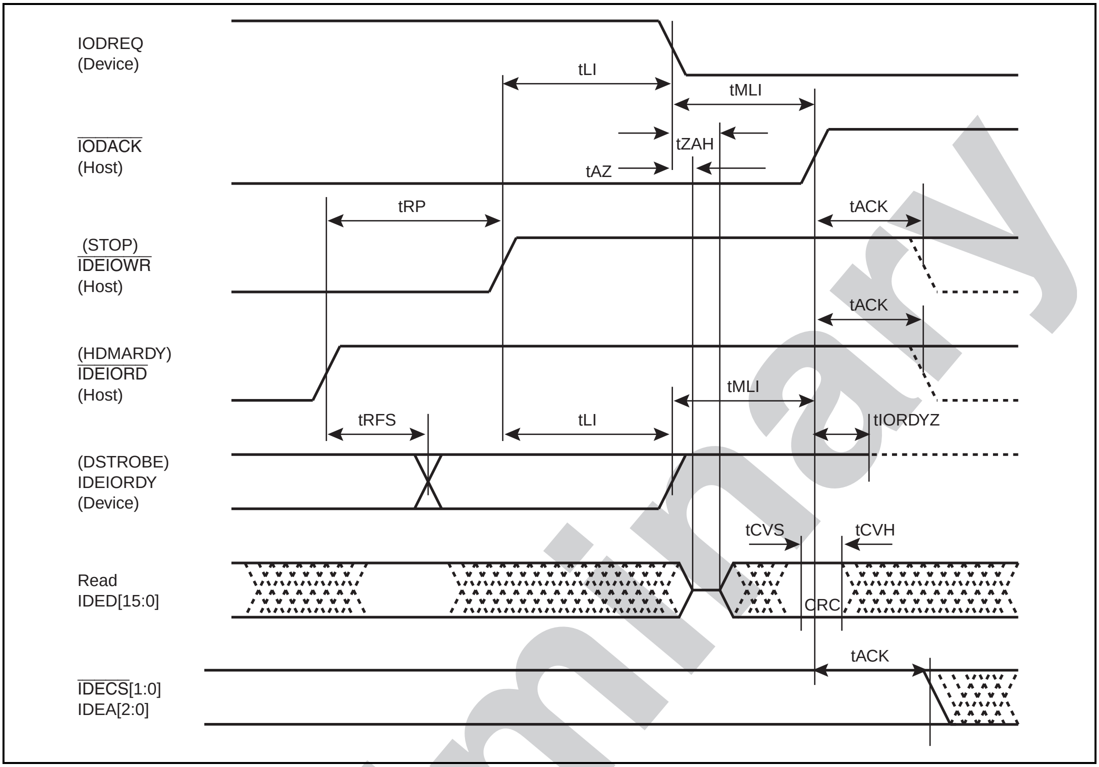


Figure 38.63 End of Ultra DMA Transfer Data In Burst from Host

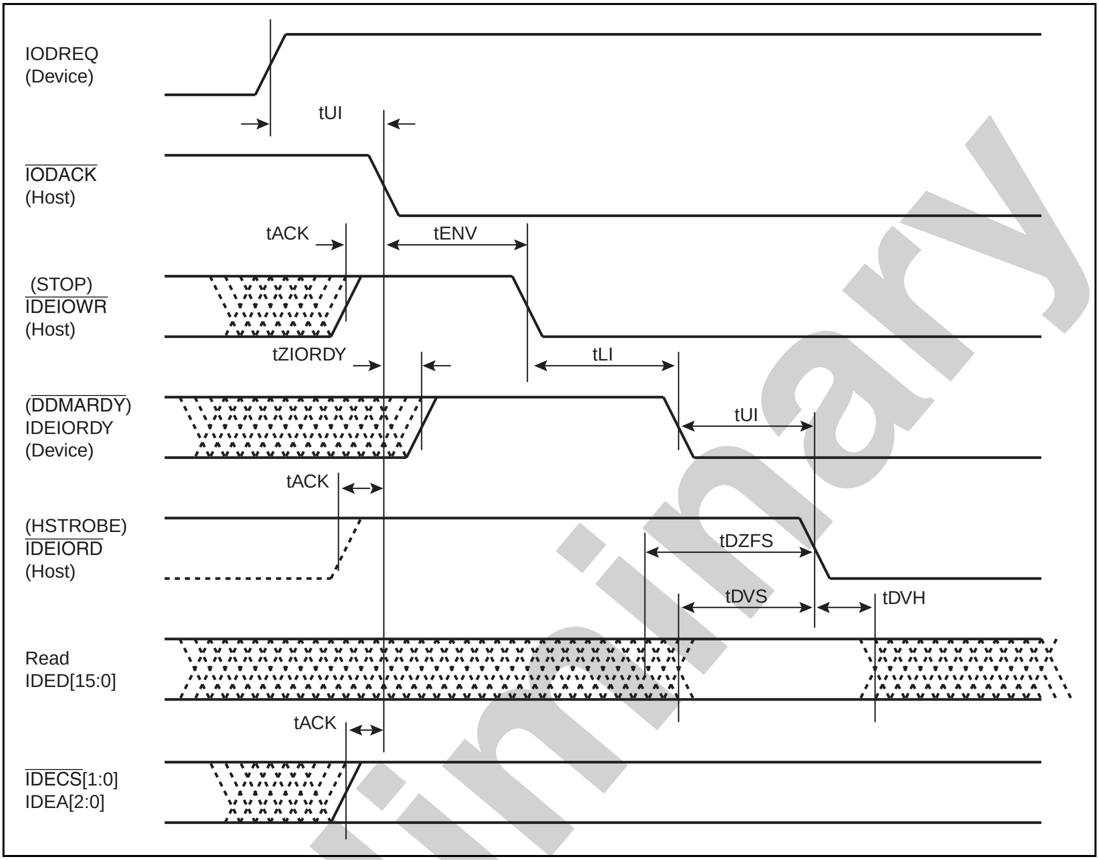


Figure 38.64 Start of Ultra DMA Transfer Data Out Burst

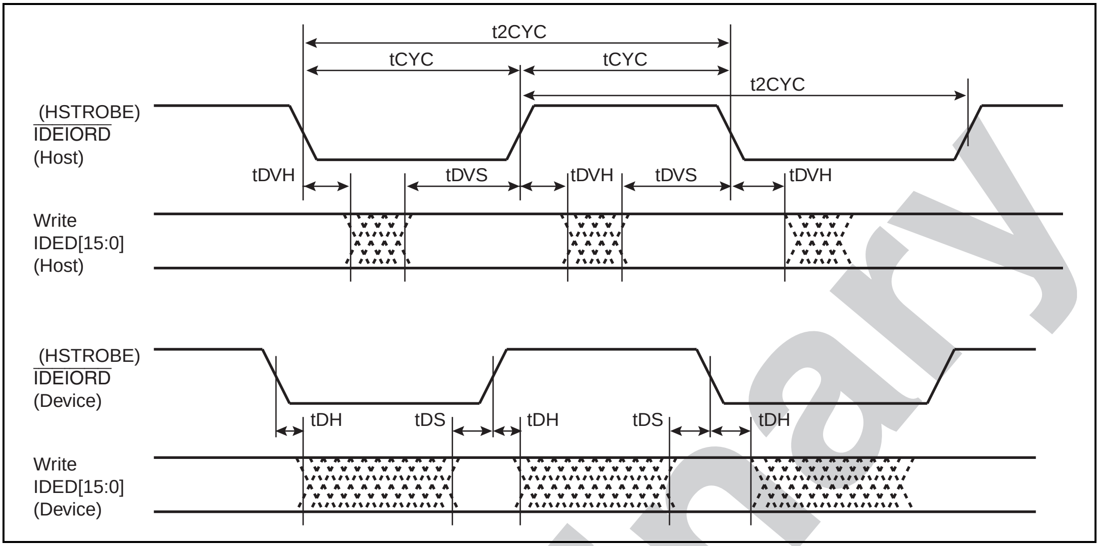


Figure 38.65 Ultra DMA Transfer Data Out Burst

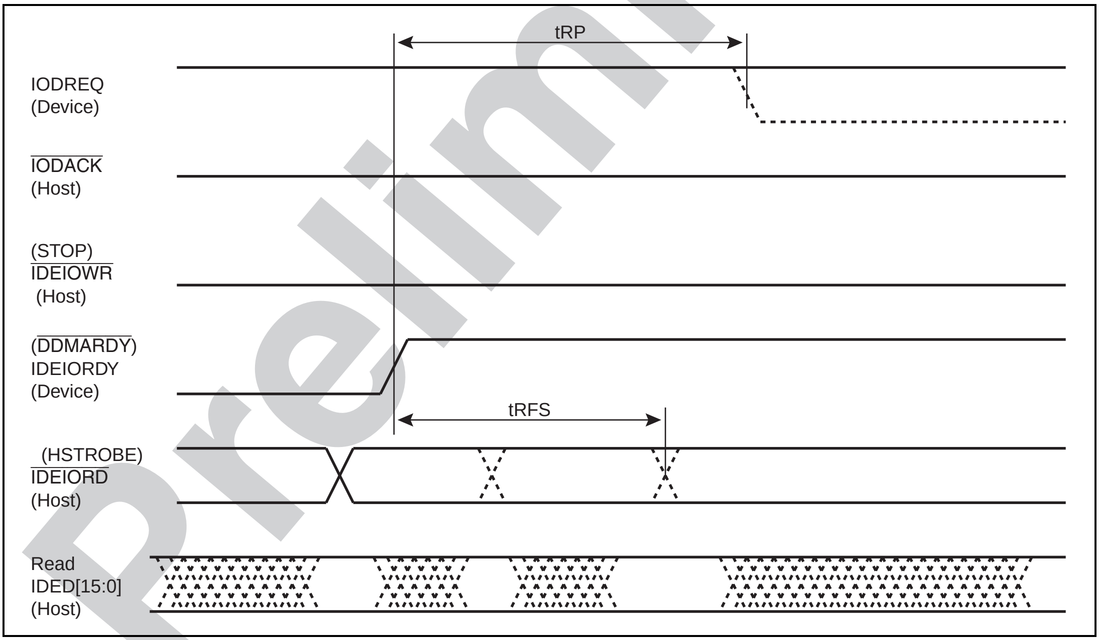


Figure 38.66 Pause of Ultra DMA Transfer Data Out Burst from Device

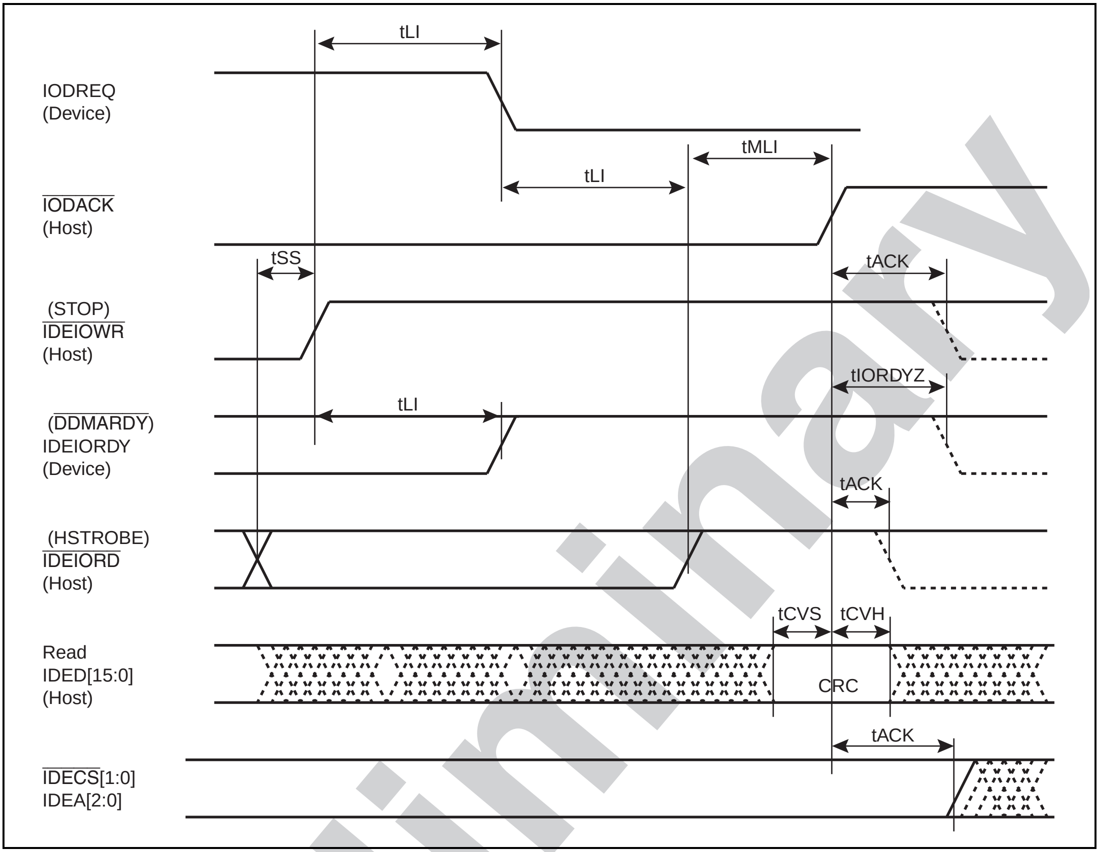


Figure 38.67 End of Ultra DMA Transfer Data Out Burst from Host

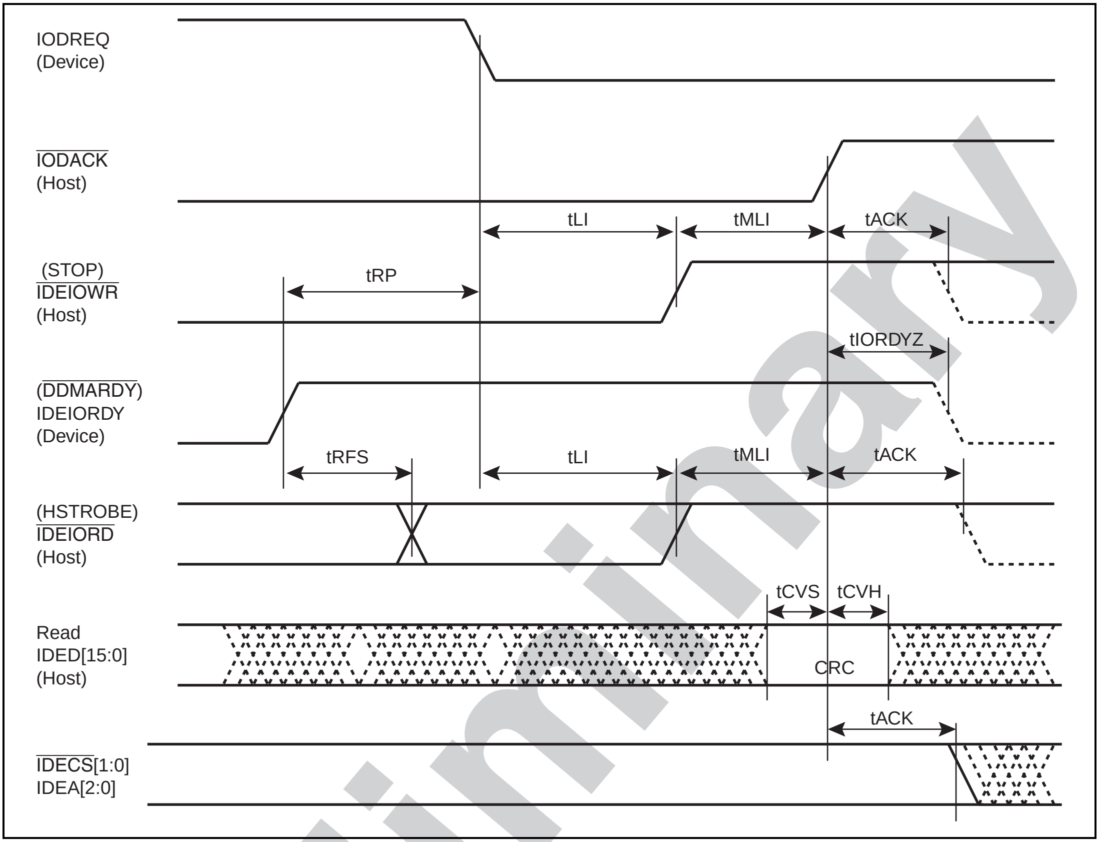


Figure 38.68 End of Ultra DMA Transfer Data Out Burst from Device

Table 38.34 Symbols of DIRECTION Timing of ATAPI Interface

Symbol	Item
tDIRECTION_WF	DIRECTION fall delay time on PIO writing
tDIRECTION_WR	DIRECTION rise delay time on PIO writing
tMDIRECTION_F	Multiword DMA data out DIRECTION fall delay time
tMDIRECTION_R	Multiword DMA data out DIRECTION rise delay time
tUDIRECTION_F(CRC)	DIRECTION fall delay time on ultra DMA data in CRC transmission
tUDIRECTION_R(CRC)	DIRECTION rise delay time on ultra DMA data in CRC transmission
tUDIRECTION_F	DIRECTION fall delay time on ultra DMA data out
tUDIRECTION_R	DIRECTION rise delay time on ultra DMA data out
tDON	Time from fall of DIRECTION to turning on IDED data bus
tDOFF	Time from turning off IDED data bus to rise of DIRECTION

Table 38.35 DIRECTION Timing of ATAPI Interface

Item and Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Figure
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
tDIRECTION_WF	79	87	56	65	34	42	34	42	34	42	ns	38.69
tDIRECTION_WR	63	71	63	71	33	41	33	41	33	41	ns	
tMDIRECTION_F	–19	–11	–19	–11	–19	–11	—	—	—	—	ns	38.71
tMDIRECTION_R	3	12	3	12	3	12	—	—	—	—	ns	
tUDIRECTION_F(CRC)	138	147	101	109	86	94	71	79	56	64	ns	38.73, 38.74
tUDIRECTION_R(CRC)	26	34	26	34	26	34	26	34	26	34	ns	
tUDIRECTION_F	48	57	48	57	48	57	48	57	48	57	ns	38.75
tUDIRECTION_R	56	64	56	64	56	64	56	64	56	64	ns	38.76, 38.77
tDON	9	15	9	15	9	15	9	15	18	22	ns	38.69, 38.71, 38.73 to 38.75
tDOFF	6	14	6	14	6	14	6	14	6	14	ns	38.69, 38.71, 38.73, 38.74, 38.76, 38.77

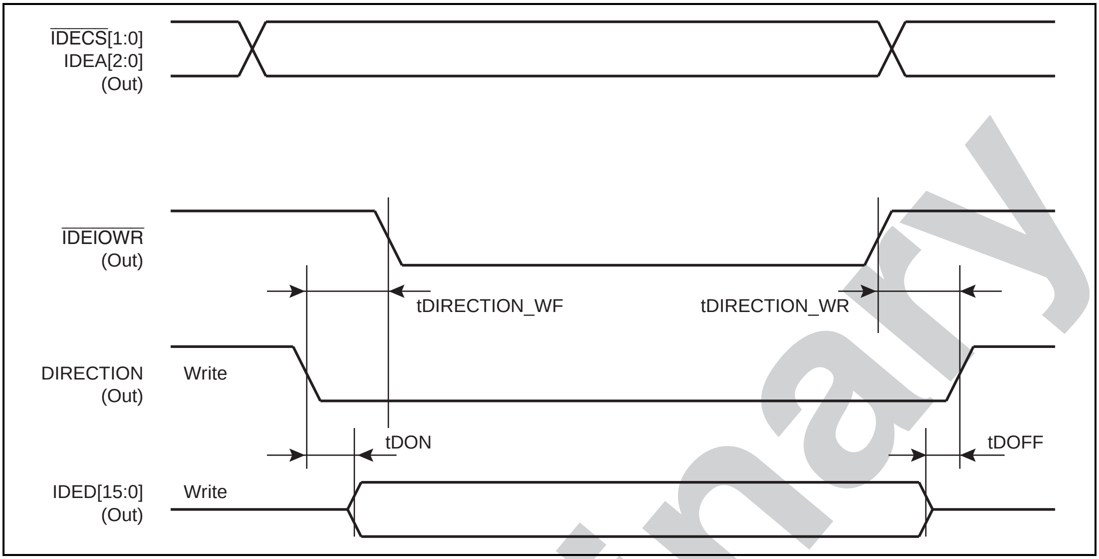


Figure 38.69 PIO Data Transfer to Device (DIRECTION)

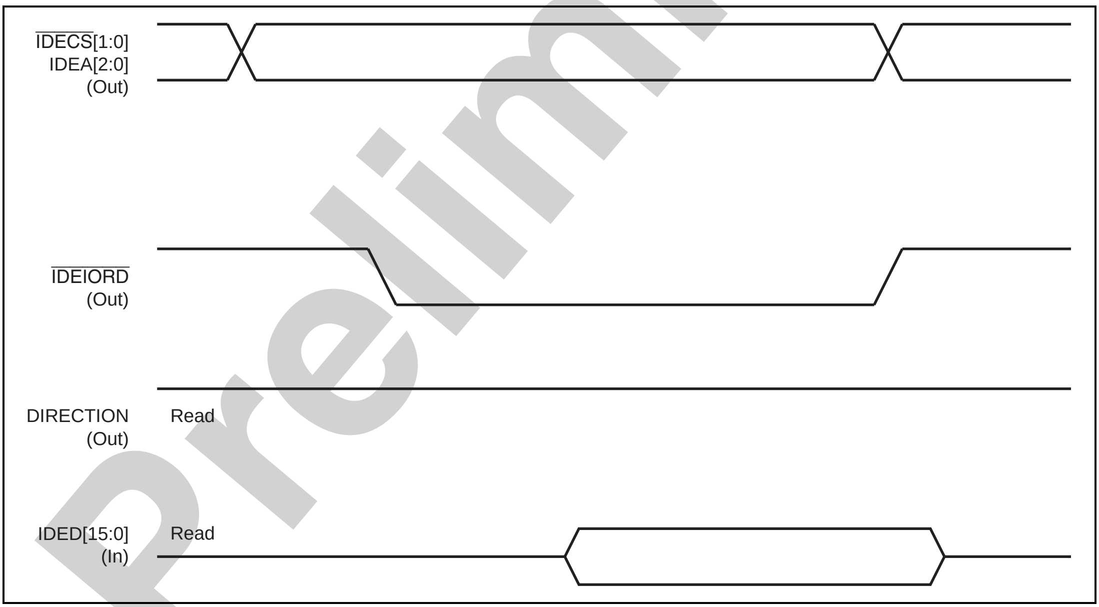


Figure 38.70 PIO Data Transfer from Device (DIRECTION)

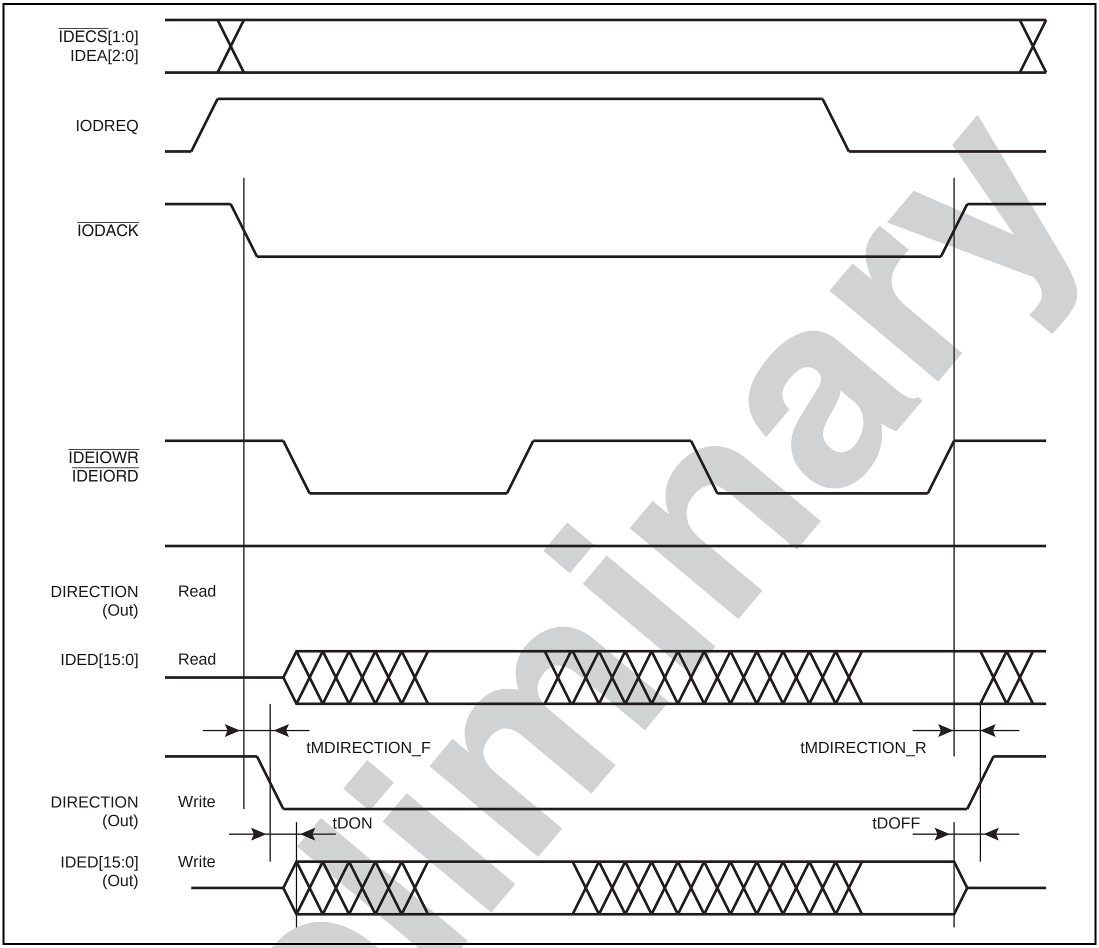


Figure 38.71 Multiword DMA Transfer (DIRECTION)

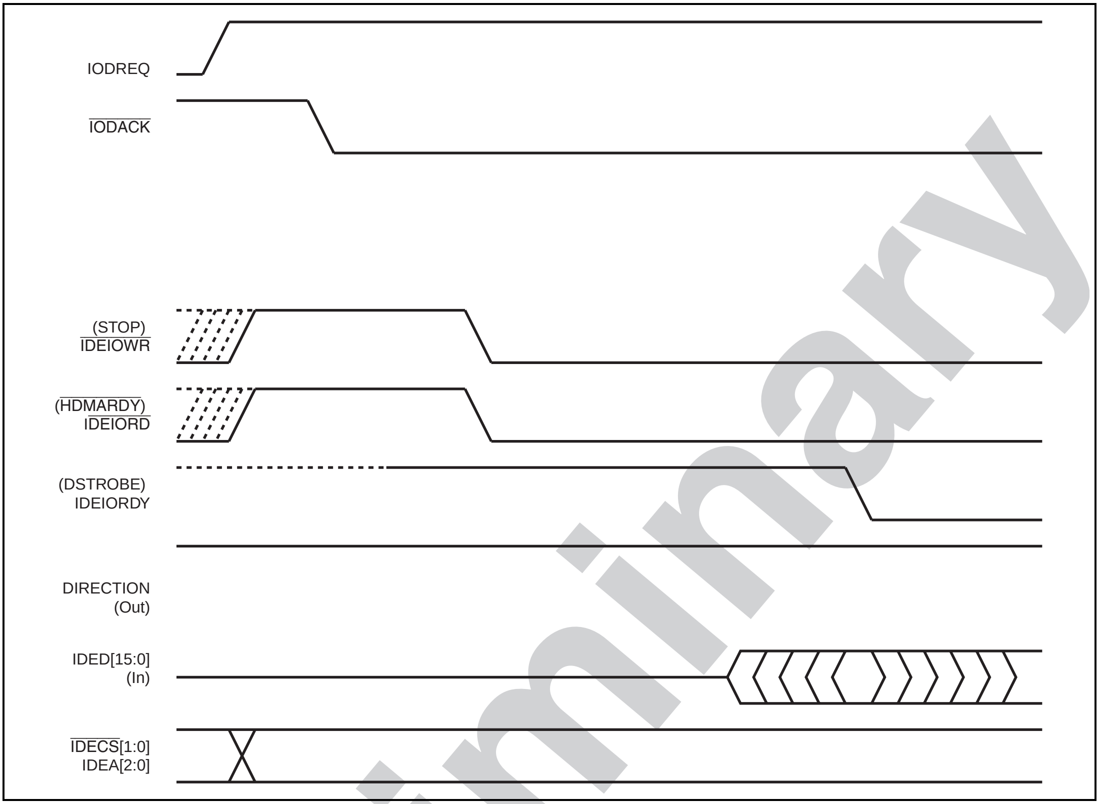


Figure 38.72 Start of Ultra DMA Transfer Data In Burst (DIRECTION)

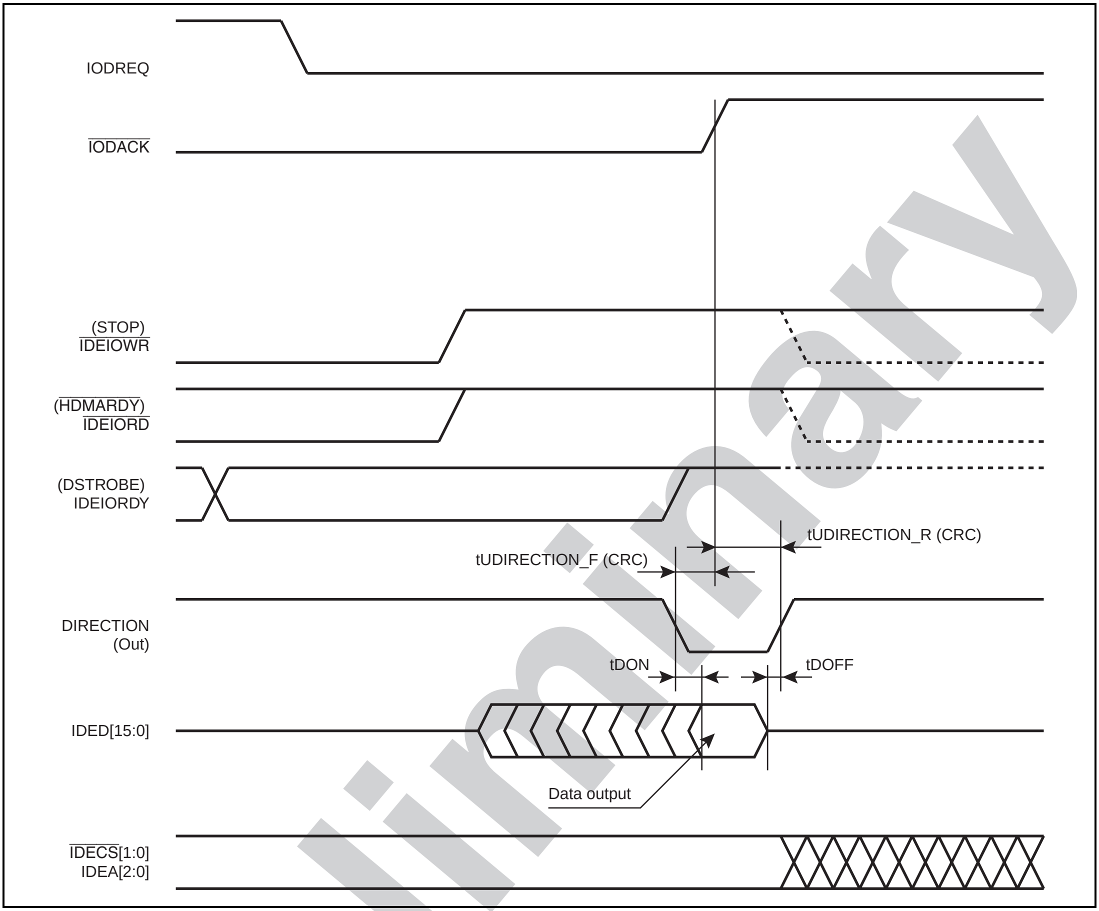


Figure 38.73 End of Ultra DMA Transfer Data In Burst from Device (DIRECTION)

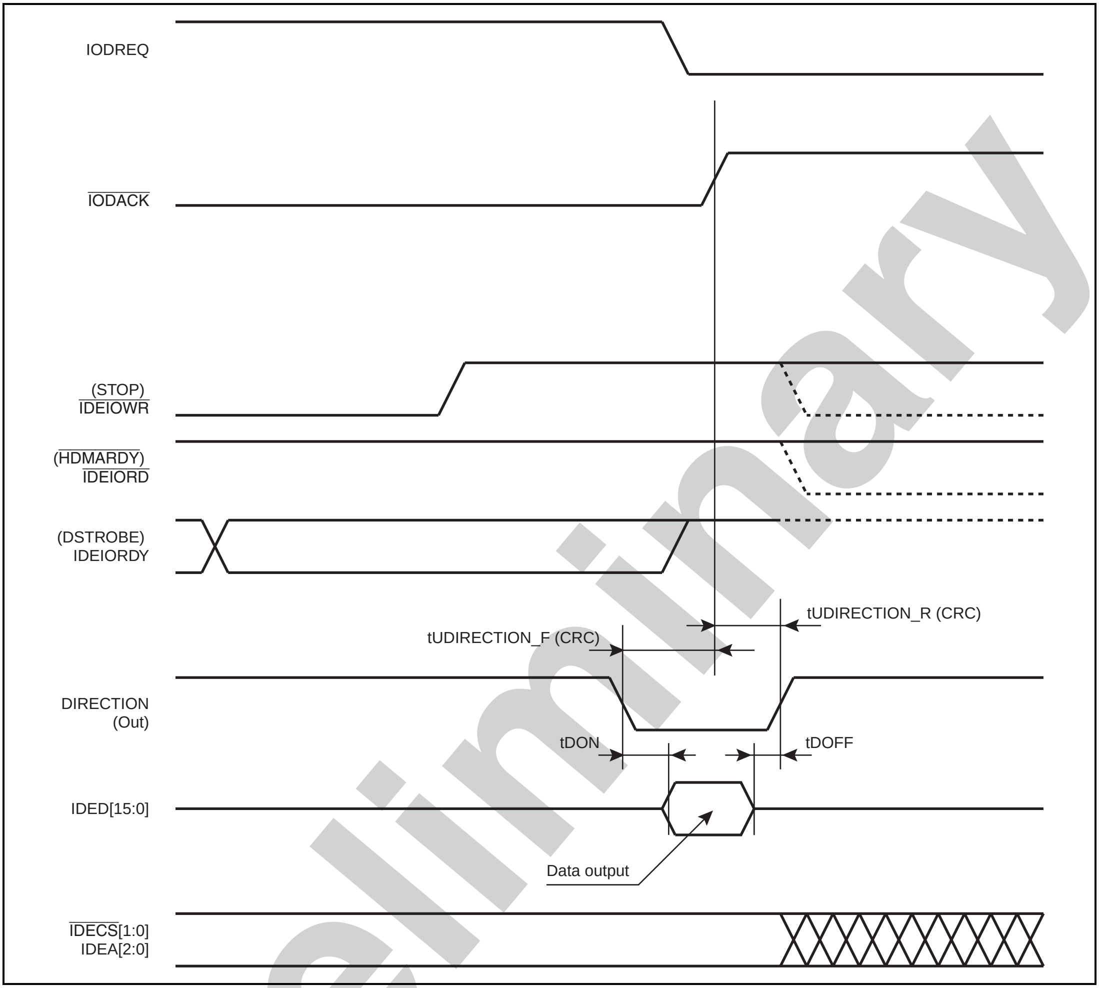


Figure 38.74 End of Ultra DMA Transfer Data In Burst from Host (DIRECTION)

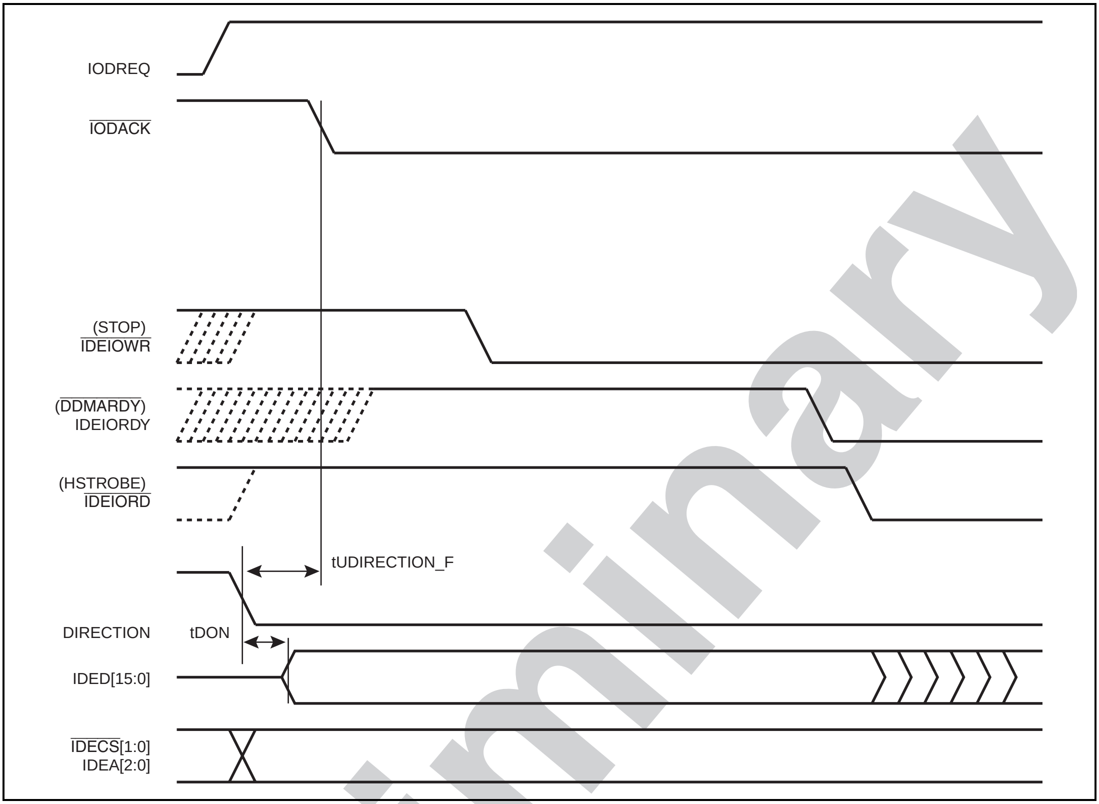


Figure 38.75 Start of Ultra DMA Transfer Data Out Burst (DIRECTION)

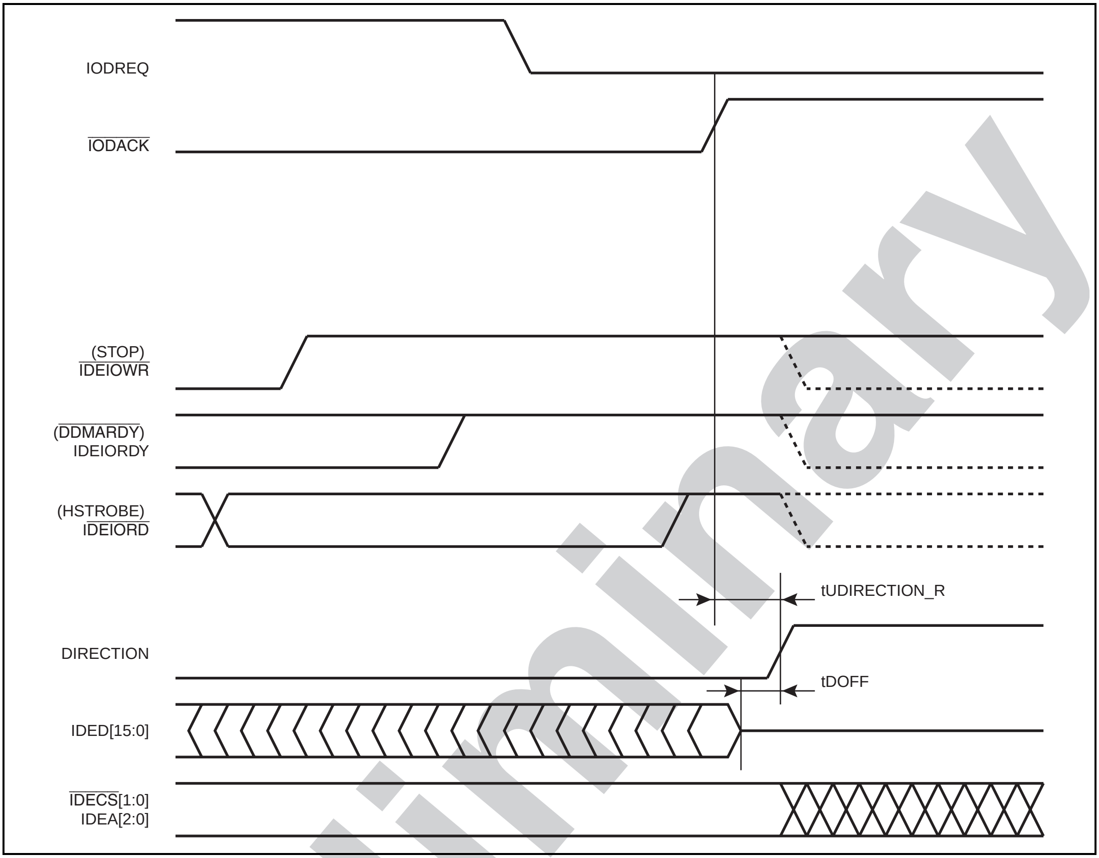


Figure 38.76 End of Ultra DMA Transfer Data Out Burst from Host (DIRECTION)

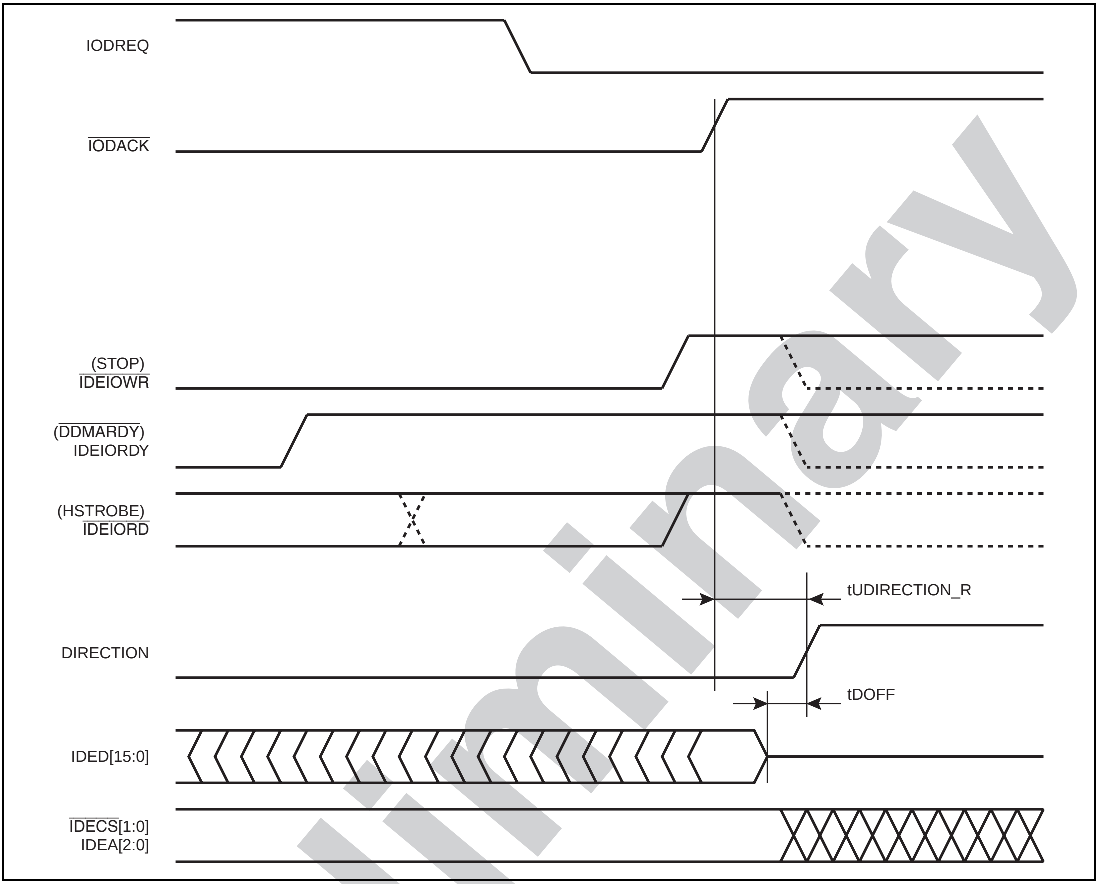


Figure 38.77 End of Ultra DMA Transfer Data Out Burst from Device (DIRECTION)

38.5.19 SDHI Module Signal Timing

Table 38.36 SDHI Module Signal Timing

Item	Symbol	Min.	Max.	Unit	Figure
SDCLK clock cycle	t_{SDDP}	20	—	ns	38.78
SDCLK clock high level width	t_{SDWH}	$0.4 \times t_{TSDPP}$	—	ns	
SDCLK clock low level width	t_{SDWL}	$0.4 \times t_{TSDPP}$	—	ns	
SDCMD, SDDAT3 to SDDAT0 output data delay (data transfer mode)	t_{SDODLY}	—	5	ns	
SDCMD, SDDAT3 to SDDAT0 input data setup	t_{SDISU}	5	—	ns	
SDCMD, SDDAT3 to SDDAT0 input data hold	t_{SDIH}	2	—	ns	

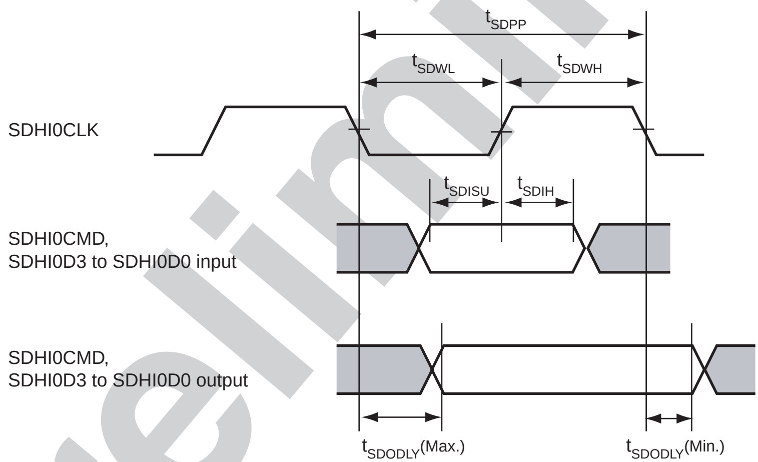


Figure 38.78 SDHI Module Signal Timing

38.6 USB Electrical Characteristics

Table 38.37 USB Electrical Characteristics

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Common	VBUS connection detecting voltage	V_{VBUSIH}	4.35	5.0	5.25	V	
	External reference resistance	R_{REF}	5.544	5.6	5.656	kΩ	±1%
	Driver output Hi-Z	R_{O}	40.5	45	49.5	Ω	
	DP Pull-up resistance (Function mode)	R_{PU}	900	—	1575	Ω	Be in the idle state
			1425	—	3090	Ω	Be in the transmission and reception state
	DP, DM pull-down resistance	R_{PD}	14250	—	24800	Ω	
	EXTAL_USB input clock frequency	f_{EXTAL_USB}	47.9952	48	48.0048	MHz	±100ppm
	Oscillation settling time	t_{UOSC}	10	—	—	ms	
	USB PLL settling time	t_{UPLL}	120	—	—	μs	
FS/LS input	Input high level voltage	V_{IH}	2.0	—	DV33 + 0.3	V	
	Input low level voltage	V_{IL}	–0.3	—	0.8	V	
	Differential input sensitivity	V_{DI}	0.2	—	—	V	│(DP) – (DM)│
	Common mode voltage range	V_{CM}	0.8	—	2.5	V	
	Single ended receiver threshold voltage	V_{SE}	0.8	—	2.0	V	
FS/LS output	Output high level voltage	V_{OH}	2.8	—	—	V	
	Output low level voltage	V_{OL}	—	—	0.3	V	
HS input	Squelch detection threshold voltage (differential)	V_{HSSQ}	100	—	150	mV	
	Differential input sensitivity	V_{HSDI}	150	—	—	mV	│(DP) – (DM)│
	Common mode voltage range	V_{HSCM}	–50	—	500	mV	
	Chirp input voltage	V_{CHIRP_RCV}	700	—	1100	mV	

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
HS output	Idle state	V_{HSOI}	–10	—	10	mV	
	Output high level voltage	V_{HSOH}	360	—	440	mV	
	Output low level voltage	V_{HSOL}	–10	—	10	mV	
	Chirp output voltage (DP pin)	$V_{HSCHIRP\_P}$	700	—	1100	mV	
	Chirp output voltage (DM pin)	$V_{HSCHIRP\_M}$	–900	—	–500	mV	
FS	Rising time (DP, DM)	t_{FDR}	4	—	20	ns	
	Falling time (DP, DM)	tFDF	4	—	20	ns	
	Rising / Rising time ratio	t_{FDR}/t_{FDF}	90	—	111.1	%	
	Output signal crossover voltage (DP, DM)	V_{FCRS}	1.3	—	2.0	V	
LS	Output rising time (DP, DM)	t_{LDR}	75	—	300	ns	
	Output falling time (DP, DM)	t_{LDF}	75	—	300	ns	
	Output rising / rising time ratio	t_{LDR}/t_{LDF}	80	—	125	%	
	Output signal crossover voltage (DP, DM)	V_{LCRS}	1.3	—	2.0	V	
HS	DISCONNECT detection voltage	$V_{DISCONNECT}$	525	—	625	mV	

38.7 A/D Converter Characteristics

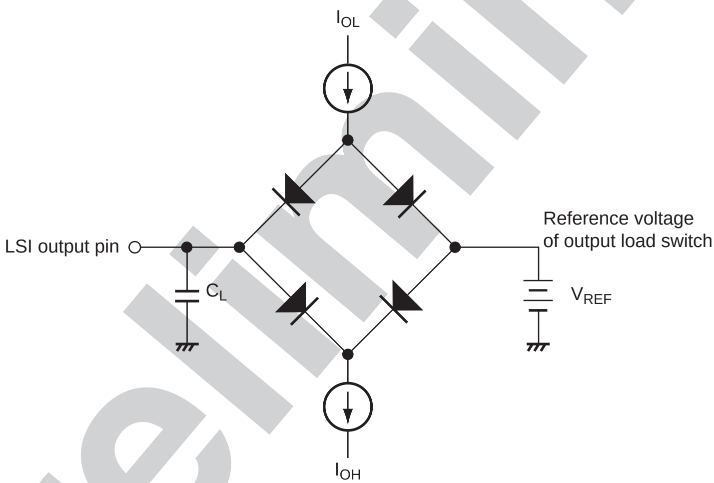
Table 38.36 A/D Converter Characteristics

Item	Min.	Typ.	Max.	Unit
Resolution	10	10	10	bits
Conversion time	15	—	—	μs
Analog input capacitance	—	—	20	pF
Permissible signal source (single source) impedance	—	—	5	kΩ
Nonlinearity error	—	—	±3.0	LSB
Offset error	—	—	±2.0	LSB
Full scale error	—	—	±2.0	LSB
Quantization error	—	—	±0.5	LSB
Absolute accuracy	—	—	±4.0	LSB

38.8 AC Characteristic Test Conditions

- I/O signal reference level: V_{CC}Q_DDR × 0.5 (DDR_SDRAM interface output)
  Dvref (DDR_SDRAM interface input)
  V_{CC}Q × 0.5 (other than DDR_SDRAM interface)
- Input pulse level: Vss to V_{CC}Q_DDR (DDR_SDRAM interface)
  Vss to V_{CC}Q (other than DDR_SDRAM interface)

- Input rise and fall times: 1 ns



Notes: 1. C_L is the total value that includes the capacitance of measurement instruments, and is set as follows for each pin:
30 pF: CKO, $\overline{\text{CS0}}$, $\overline{\text{CS2}}$ to $\overline{\text{CS6B}}$
50 pF: All other pins
2. I_{OL} = 0.2 mA, I_{OH} = –0.2 mA

Figure 38.79 Output Load Circuit (other than DDR-SDRAM Interface)

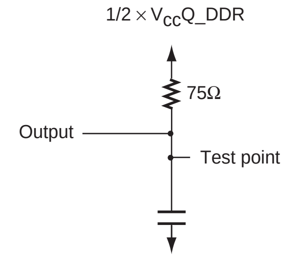


Figure 38.80 Output Load Circuit (DDR-SDRAM Interface)

Appendix

A. Pin States at Reset and in Power-Down Modes

Module	Pin Name	During Reset*[1]	After Reset*[2]	Sleep	Software Standby	U-Standby
Clock	EXTAL	I	I	I	I	I
	XTAL	O*[3]	O*[3]	O*[3]	O*[3]	O*[3]
	RCLK	I	I	I	I	I
Operating mode	MD0 to MD3	I	I	I	I	I
	MD5	I	I	I	I	I
	MD8	I	I	I	I	I
	$\overline{\text{TSTMD}}$	I	I	I	I	I
System control	BOOT	I	I	I	I	I
	$\overline{\text{RESETA}}$	I	I	I	I	I
	$\overline{\text{RESETP}}$	I	I	I	I	I
	$\overline{\text{RESETOUT}}$	L	H	O	O	O
	$\overline{\text{TST}}$	I	I	I	I	I
	STATUS0	L	O	L	H	H
	PDSTATUS	L	O	L	L	H
Interrupt	NMI	I	I	I	I	I
	IRQ0 to IRQ7	—	—	I	I	I
BSC	A0 to A25	L	O	O	O/Z*[4]	O/Z*[4]
	$\overline{\text{BS}}$	—	—	O	H/Z*[4]	H/Z*[4]
	CKO	O	O	O	O/Z*[4]	O/Z*[4]
	$\overline{\text{CS0}}$	H	O	O	H/Z*[4]	H/Z*[4]
	$\overline{\text{CS4}}$	H	O	O	H/Z*[4]	H/Z*[4]
	$\overline{\text{CS5B}}$/$\overline{\text{CE1A}}$	H	O	O	H/Z*[4]	H/Z*[4]
	$\overline{\text{CS5A}}$/$\overline{\text{CE2A}}$	H	O	O	H/Z*[4]	H/Z*[4]
	$\overline{\text{CS6A}}$/$\overline{\text{CE2B}}$	H	O	O	H/Z*[4]	H/Z*[4]
	$\overline{\text{CS6B}}$/$\overline{\text{CE1B}}$	H	O	O	H/Z*[4]	H/Z*[4]
	D0 to D31	Z	Z	Z/I/O	Z	Z
	$\overline{\text{IOIS16}}$	Z	I	I	Z	Z
	RDWR	H	O	O	H/Z*[4]	H/Z*[4]
	$\overline{\text{RD}}$	H	O	O	H/Z*[4]	H/Z*[4]

Module	Pin Name	During Reset*[1]	After Reset*[2]	Sleep	Software Standby	U-Standby
BSC	$\overline{\text{WAIT}}$	IU	IU	IU	IU	IU
	$\overline{\text{WE0}}$, $\overline{\text{WE1}}$	H	O	O	H/Z*[4]	H/Z*[4]
	$\overline{\text{WE2}}$/$\overline{\text{ICIORD}}$	H	O	O	H/Z*[4]	H/Z*[4]
	$\overline{\text{WE3}}$/$\overline{\text{ICIOWR}}$	H	O	O	H/Z*[4]	H/Z*[4]
SBSC	HPA0 to HPA15	L	O	O	O	O
	HPD0 to HPD31	Z	Z	Z/I/O	Z	Z
	HPDQM0 to HPDQM3	H	O	O	H	H
	HPDQS0 to HPDQS3	H	O	O	O	O
	$\overline{\text{HPCLK}}$	O	O	O	O	O
	HPCLK	O	O	O	O	O
	HPRDWR	H	O	O	O	O
	$\overline{\text{HPCS}}$	H	O	O	O	O
	$\overline{\text{HPCAS}}$	H	O	O	O	O
	$\overline{\text{HPRAS}}$	H	O	O	O	O
	HPCKE	O	O	O	O	O
DMAC	DACK0, DACK1	—	—	O	O	O
	DREQ0, DREQ1	—	—	I	Z	Z
SCIF	SCIF0_TXD	—	—	O/Z*[5]	Z	Z
	SCIF1_TXD					
	SCIF2_TXD					
	SCIF0_RXD	—	—	I/Z*[5]	Z	Z
	SCIF1_RXD					
	SCIF2_RXD					
	SCIF0_SCK	—	—	I/O/Z*[5]	Z/O*[5]	Z/O*[5]
	SCIF1_SCK					
	SCIF2_SCK					

Module	Pin Name	During Reset*1	After Reset*2	Sleep	Software Standby	U-Standby
SCIFA	SCIF3_SCK	—	—	I/O/Z*5	Z/O*5	Z/O*5
	SCIF4_SCK					
	SCIF5_SCK					
	SCIF3_RXD	—	—	I/Z*5	Z	Z
	SCIF4_RXD					
	SCIF5_RXD					
	SCIF3_TXD	—	—	O/Z*5	Z	Z
	SCIF4_TXD					
	SCIF5_TXD					
	$\overline{\text{SCIF3\_RTS}}$	—	—	O/Z*5	Z	Z
	$\overline{\text{SCIF3\_CTS}}$	—	—	I/Z*5	Z	Z
MSIOF0/ MSIOF1	MSIOF0_RXD	—	—	I	Z	Z
	MSIOF1_RXD					
	MSIOF0_ TSYNC	—	—	O	O/I*5	O/I*5
	MSIOF1_ TSYNC					
	MSIOF0_TSCK	—	—	O/I*5	O/I*5	O/I*5
	MSIOF1_TSCK					
	$\overline{\text{MSIOF0\_SS1}}$	—	—	O	O	O
	$\overline{\text{MSIOF1\_SS1}}$					
	$\overline{\text{MSIOF0\_SS2}}$	—	—	O	O	O
	$\overline{\text{MSIOF1\_SS2}}$					
	MSIOF0_RSCK	—	—	O/I*5	O/I*5	O/I*5
	MSIOF1_RSCK					

Module	Pin Name	During Reset*[1]	After Reset*[2]	Sleep	Software Standby	U-Standby
MSIOF0/ MSIOF1	MSIOF0_ RSYNC	—	—	O/I*[5]	O/I*[5]	O/I*[5]
	MSIOF1_ RSYNC					
TPU	TPUTO0 to TPUTO3	—	—	O	O	O
IrDA	IRDA_OUT	—	—	O	O	O
	$\overline{\text{IRDA\_IN}}$	—	—	I	Z	Z
IIC	SCL	Z	Z	I/O	Z	Z
	SDA	Z	Z	I/O	Z	Z
FLCTL	FCDE	—	—	O	O	O
	FSC	—	—	O	O	O
	$\overline{\text{FWE}}$	—	—	O	O	O
	FOE	—	—	O	O	O
	FRB	—	—	I	Z	Z
	$\overline{\text{FCE}}$	—	—	O	O	O
	NAF0 to NAF7	—	—	Z/I/O	Z	Z
VIO	VIO_D0 to VIO_D15	—	—	I	Z	Z
	VIO_FLD	—	—	I	Z	Z
	VIO_CKO	—	—	O	O	O
	VIO_VD1	—	—	I	Z	Z
	VIO_VD2	—	—	I	Z	Z
	VIO_CLK1	—	—	I	Z	Z
	VIO_CLK2	—	—	I	Z	Z
	VIO_HD1	—	—	I	Z	Z
	VIO_HD2	—	—	I	Z	Z
LCDC	LCDD0 to LCDD23	—	—	O/I	O/Z	O/Z
	LCDVCPWC	—	—	O	O	O
	$\overline{\text{LCDRD}}$	—	—	O	O	O
	LCDVSYN	—	—	O/I*[5]	O/Z*[5]	O/Z*[5]

Module	Pin Name	During Reset*[1]	After Reset*[2]	Sleep	Software Standby	U-Standby
LCDC	LCDDISP	—	—	O	O	O
	LCDHSYN	—	—	O	O	O
	LCDDON	—	—	O	O	O
	LCDDCK	—	—	O	O	O
	LCDVEPWC	—	—	O	O	O
	LCDRS	—	—	O	O	O
	$\overline{\text{LCDCS}}$	—	—	O	O	O
	$\overline{\text{LCDWR}}$	—	—	O	O	O
	LCDLCLK	—	—	I	Z	Z
VOU	DV_D0 to DV_D15	—	—	O	O	O
	DV_HSYNC	—	—	O	O	O
	DV_VSYNC	—	—	O	O	O
	DV_CLKI	—	—	I	Z	Z
	DV_CLK	—	—	O	O	O
TSIF	TS0_SDAT	—	—	I	Z	Z
	TS0_SCK	—	—	I	Z	Z
	TS0_SDEN	—	—	I	Z	Z
	TS0_SPSYNC	—	—	I	Z	Z
USB	DM	L	L	Z/I/O	Z	Z
	DP	H	H	Z/I/O	Z	Z
	VBUS	I	I	I	I	I
	REFRIN	—	—	—	—	—
	EXTALUSB	I	I	I	I	I
	XTALUSB	O	O	O	O	O
SIUA/ SIUB	SIUAFCK	—	—	O	O	O
	SIUBFCK	—	—	O	O	O
	SIUAILR	—	—	I/O*[5]	Z/O*[5]	Z/O*[5]
	SIUBILR	—	—	I/O*[5]	Z/O*[5]	Z/O*[5]
	SIUAIBT	—	—	I/O*[5]	Z/O*[5]	Z/O*[5]
	SIUBIBT	—	—	I/O*[5]	Z/O*[5]	Z/O*[5]

Module	Pin Name	During Reset*[1]	After Reset*[2]	Sleep	Software Standby	U-Standby
SIUA/ SIUB	SIUAISLD	—	—	I	Z	Z
	SIUBISLD	—	—	I	Z	Z
	SIUAOLR	—	—	I/O*[5]	Z/O*[5]	Z/O*[5]
	SIUBOLR	—	—	I/O	Z/O*[5]	Z/O*[5]
	SIUAOBT	—	—	I/O*[5]	Z/O*[5]	Z/O*[5]
	SIUBOBT	—	—	I/O	Z/O*[5]	Z/O*[5]
	SIUAOSLD	—	—	O	O	O
	SIUBOSLD	—	—	O	O	O
	SIUAISPD	—	—	I	Z	Z
	SIUAOSPD	—	—	O	O	O
	SIUAMCK	—	—	I	Z	Z
	SIUBMCK					
ATAPI	DIRECTION	—	—	O	H	H
	$\overline{\mathrm{EXBUF\_ENB}}$	—	—	O	H	H
	$\overline{\mathrm{IDERST}}$	—	—	O/Z*[5]	O/Z*[5]	O/Z*[5]
	$\overline{\mathrm{IODACK}}$	—	—	O/Z*[5]	O/Z*[5]	O/Z*[5]
	IODREQ	—	—	I	Z	Z
	IDEIORDY	—	—	I	Z	Z
	IDED0 to IDED15	—	—	Z/I/O	Z	Z
	IDEINT	—	—	I	Z	Z
	$\overline{\mathrm{IDEIOWR}}$	—	—	O/Z*[5]	O/Z*[5]	O/Z*[5]
	$\overline{\mathrm{IDEIORD}}$	—	—	O/Z*[5]	O/Z*[5]	O/Z*[5]
	$\overline{\mathrm{IDECS0}}$	—	—	O/Z*[5]	O/Z*[5]	O/Z*[5]
	$\overline{\mathrm{IDECS1}}$	—	—	O/Z*[5]	O/Z*[5]	O/Z*[5]
	IDEA0 to IDEA2	—	—	O/Z*[5]	O/Z*[5]	O/Z*[5]
KEYSC	KEYOUT0 to KEYOUT3	—	—	O/Z*[5]	O/Z*[5]	O/Z*[5]
	KEYIN0 to KEYIN4	—	—	IU	IU	IU
	KEYOUT5/ KEYIN5	—	—	O/Z/IU*[5]	O/Z/IU*[5]	O/Z/IU*[5]

Module	Pin Name	During Reset*[1]	After Reset*[2]	Sleep	Software Standby	U-Standby
KEYSC	KEYOUT4/ KEYIN6	—	—	O/Z/IU*[5]	O/Z/IU*[5]	O/Z/IU*[5]
SDHI0/ SDHI1	$\overline{\text{SDHI0CD}}$	—	—	I	Z	Z
	$\overline{\text{SDHI1CD}}$	—	—	I	Z	Z
	SDHI0WP	—	—	I	Z	Z
	SDHI1WP	—	—	I	Z	Z
	SDHI0D0 to SDHI0D3	—	—	I/O	Z	Z
	SDHI1D0 to SDHI1D3	—	—	I/O	Z	Z
	SDHI0CMD	—	—	I/O	Z	Z
	SDHI1CMD	—	—	I/O	Z	Z
	SDHI0CLK	—	—	O	L	L
	SDHI1CLK	—	—	O	L	L
ADC	AN0 to AN3	I	I	I	I	I
	ADTRG	—	—	I	Z	Z
I/O port	PTA	—	—	P	K	K
	PTB	—	—	P	K	K
	PTC	Z	Z	P	K	K
	PTD	Z	Z	P	K	K
	PTE	Z	Z	P	K	K
	PTF	Z	Z	P	K	K
	PTG	Z	Z	P	K	K
	PTH	Z	Z	P	K	K
	PTJ	—	—	P	K	K
	PTK	Z	Z	P	K	K
	PTL	Z	Z	P	K	K
	PTM	Z	Z	P	K	K
	PTN	Z	Z	P	K	K
	PTQ	—	—	P	K	K
	PTR	—	—	P	K	K
	PTS	Z	Z	P	K	K

Module	Pin Name	During Reset*[1]	After Reset*[2]	Sleep	Software Standby	U-Standby
I/O port	PTT	Z	Z	P	K	K
	PTU	Z	Z	P	K	K
	PTV	Z	Z	P	K	K
	PTW	Z	Z	P	K	K
	PTX	Z	Z	P	K	K
	PTY	Z	Z	P	K	K
	PTZ	Z	Z	P	K	K
H-UDI	TCK	IU	IU	IU	IU	IU
	TMS	IU	IU	IU	IU	IU
	TDI	IU	IU	IU	IU	IU
	TDO	Z/O	Z/O	Z/O*[6]	Z/O*[6]	Z/O*[6]
	$\overline{\text{TRST}}$	IU	IU	IU*[7]	IU*[7]	IU*[7]
	$\overline{\text{ASEBRK}}$/ BRKAK	IU/OU*[8]	IU/OU*[8]	IU/OU*[8]	IU/OU*[8]	IU/OU*[8]
	MPMD	IU	IU	IU	IU	IU
AUD	AUDCK	—	—	O	O	O
	AUDSYNC	—	—	O	O	O
	AUDATA0 to AUDATA3	—	—	O	O	O

[Legend]

I: Input (pull-up and pull-down MOS off)

IU: Input (pull-up MOS on)

ID: Input (pull-down MOS on)

H: High-level output

L: Low-level output

O: Output

OU: Output (pull-up MOS on)

P: Functions as a port. (Selection of input or output and state of pull-up and pull-down MOS depend on the register settings)

K: Port state is retained. (fixed to input; output buffer state retained; pull-up and pull-down state retained).

Z: High-impedance state. (fixed to input; output buffer off; pull-up and pull-down MOS off)

ZU: Pulled up. (fixed to input; output buffer off; pull-up MOS on)

ZD: Pulled down. (fixed to input; output buffer off; pull-down MOS on)

The state written on the left of a slash (/) indicates the default state.

—: Cannot be selected.

Notes: *1. Indicates the duration in which $\overline{\mathrm{RESETP}}$ is asserted and a maximum of two RCLK cycles after $\overline{\mathrm{RESETP}}$ is negated.

*2. Indicates the duration in which $\overline{\mathrm{RESETOUT}}$ is asserted after $\overline{\mathrm{RESETP}}$ is negated.

*3. Depends on the clock mode selected (MD0 to MD2).

*4. Z or [H/L] depending on the settings of the HIZMEM and HIZCNT bits in CMNCR register of the BSC.

*5. Depends on the register settings

*6. Depends on the state of the TAP controller when the MPMD pin = H. When the MPMD pin = L, the pin is placed in the state written on the right of a slash (/).

*7. The pull-up MOS can be turned on or off according to the PULCR register setting.

*8. With respect to I/O pins with a pull-up MOS, input or output is selected according to the register setting when the MPMD pin = L. When the $\overline{\mathrm{TRST}}$ pin = L, the pin provides input. When the $\overline{\mathrm{TRST}}$ pin = H, the pin always provides input.

B. Handling of Unused Pins

Pin No.	Pin Name	Default Function	Initial State	Handling	Group
B6	DV33	DV33	—	Use	USB
B5	DG33	DG33	—	Use	USB
A6	DM	DM	L	Open	USB
A5	DP	DP	H	Open	USB
C5	VBUS	VBUS	I	Pull down	USB
A4	DV12	DV12	—	Use	USB
B4	DG12	DG12	—	Use	USB
E6	REFRIN	REFRIN	—	Pull down	USB
B3	AV33	AV33	—	Use	USB
D5	AG33	AG33	—	Use	USB
A3	AV12	AV12	—	Use	USB
C4	AG12	AG12	—	Use	USB
A2	UV12	UV12	—	Use	USB
D6	UG12	UG12	—	Use	USB
B1	EXTALUSB	EXTALUSB	I	Pull down	USB
C1	XTALUSB	XTALUSB	O	Open	USB
C6	AV_{SS}	AV_{SS}	—	Use	ADC
B7	PTQ0 / AN0	AN0	I	Pull up	ADC
C7	PTQ1 / AN1	AN1	I	Pull up	ADC
A7	PTQ2 / AN2	AN2	I	Pull up	ADC
D7	PTQ3 / AN3	AN3	I	Pull up	ADC
E7	AV_{CC}	AV_{CC}	—	Use	ADC
W3	D0	D0	Z	Open	BSC
U4	D1	D1	Z	Open	BSC
V3	D2	D2	Z	Open	BSC
W1	D3	D3	Z	Open	BSC
T4	D4	D4	Z	Open	BSC
V1	D5	D5	Z	Open	BSC
T3	D6	D6	Z	Open	BSC

Pin No.	Pin Name	Default Function	Initial State	Handling	Group
T2	D7	D7	Z	Open	BSC
Y2	D8	D8	Z	Open	BSC
Y1	D9	D9	Z	Open	BSC
W2	D10	D10	Z	Open	BSC
U3	D11	D11	Z	Open	BSC
V2	D12	D12	Z	Open	BSC
U2	D13	D13	Z	Open	BSC
U1	D14	D14	Z	Open	BSC
T1	D15	D15	Z	Open	BSC
AE12	PTA0 / D16 / KEYIN0	D16	Z	Open	BSC
AC13	PTA1 / D17 / KEYIN1	D17	Z	Open	BSC
AB12	PTA2 / D18 / KEYIN2	D18	Z	Open	BSC
AE11	PTA3 / D19 / KEYIN3	D19	Z	Open	BSC
AE10	PTA4 / D20 / KEYIN4	D20	Z	Open	BSC
AC11	PTA5 / D21 / KEYOUT0	D21	Z	Open	BSC
AE9	PTA6 / D22 / KEYOUT1	D22	Z	Open	BSC
AC10	PTA7 / D23 / KEYOUT2	D23	Z	Open	BSC
AB13	PTB0 / D24 / KEYOUT3	D24	Z	Open	BSC
AD12	PTB1 / D25 / KEYOUT4/KEYIN6	D25	Z	Open	BSC
AC12	PTB2 / D26 / KEYOUT5/KEYIN5	D26	Z	Open	BSC
AD11	PTB3 / D27	D27	Z	Open	BSC
AB11	PTB4 / D28	D28	Z	Open	BSC
AD10	PTB5 / D29	D29	Z	Open	BSC
AD9	PTB6 / D30	D30	Z	Open	BSC
AE8	PTB7 / D31	D31	Z	Open	BSC
AC8	A0	A0	O	Open	BSC
AB10	A1	A1	O	Open	BSC
AD6	A2	A2	O	Open	BSC
AC7	A3	A3	O	Open	BSC

Pin No.	Pin Name	Default Function	Initial State	Handling	Group
AE5	A4	A4	O	Open	BSC
AC6	A5	A5	O	Open	BSC
AD5	A6	A6	O	Open	BSC
AB7	A7	A7	O	Open	BSC
AE4	A8	A8	O	Open	BSC
AB9	A9	A9	O	Open	BSC
AC5	A10	A10	O	Open	BSC
AB8	A11	A11	O	Open	BSC
AD4	A12	A12	O	Open	BSC
AB6	A13	A13	O	Open	BSC
AC4	A14	A14	O	Open	BSC
AE3	A15	A15	O	Open	BSC
AB5	A16	A16	O	Open	BSC
AD3	A17	A17	O	Open	BSC
AC3	A18	A18	O	Open	BSC
AE2	A19	A19	O	Open	BSC
AB4	A20	A20	O	Open	BSC
AD2	A21	A21	O	Open	BSC
AA4	PTJ0 / A22	A22	O	Open	BSC
AD1	PTJ1 / A23	A23	O	Open	BSC
AB3	PTJ2 / A24	A24	O	Open	BSC
AC2	PTJ3 / A25	A25	O	Open	BSC
AA1	$\overline{RD}$	$\overline{RD}$	O	Open	BSC
R3	RDWR	RDWR	O	Open	BSC
AA3	$\overline{WE0}$	$\overline{WE0}$	O	Open	BSC
AB1	$\overline{WE1}$	$\overline{WE1}$	O	Open	BSC
AB2	PTR0 / $\overline{WE2}$/$\overline{ICIORD}$	$\overline{WE2}$/$\overline{ICIORD}$	O	Open	BSC
AC1	PTR1 / $\overline{WE3}$/$\overline{ICIOWR}$	$\overline{WE3}$/$\overline{ICIOWR}$	O	Open	BSC
Y4	MD3	MD3	I	Use	BSC
AE6	CKO	CKO	O	Open	BSC
V4	$\overline{CS0}$	$\overline{CS0}$	O	Open	BSC

Pin No.	Pin Name	Default Function	Initial State	Handling	Group
AD7	$\overline{CS4}$	$\overline{CS4}$	O	Open	BSC
AC9	PTR7 / $\overline{CS6B}/\overline{CE1B}$	$\overline{CS6B}/\overline{CE1B}$	O	Open	BSC
AE7	PTR6 / $\overline{CS6A}/\overline{CE2B}$	$\overline{CS6A}/\overline{CE2B}$	O	Open	BSC
Y3	PTR5 / $\overline{CS5B}/\overline{CE1A}$	$\overline{CS5B}/\overline{CE1A}$	O	Open	BSC
AA2	PTR4 / $\overline{CS5A}/\overline{CE2A}$	$\overline{CS5A}/\overline{CE2A}$	O	Open	BSC
W4	PTR3 / $\overline{IOIS16}$ / LCDLCLK	$\overline{IOIS16}$	I	Pull up	BSC
AD8	PTR2 / $\overline{WAIT}$	$\overline{WAIT}$	IU	Pull up	BSC
M25	PTC0 / IDED8 / SDHI1CLK	PTC0	Z	Open	ATAPI
N23	PTC1 / IDED9 / SDHI1CMD	PTC1	Z	Open	ATAPI
N24	PTC2 / IDED10 / SDHI1D0	PTC2	Z	Open	ATAPI
N25	PTC3 / IDED11 / SDHI1D1	PTC3	Z	Open	ATAPI
P22	PTC4 / IDED12 / SDHI1D2	PTC4	Z	Open	ATAPI
P23	PTC5 / IDED13 / SDHI1D3	PTC5	Z	Open	ATAPI
P24	PTC6 / IDED14 / SDHI1WP	PTC6	Z	Open	ATAPI
P25	PTC7 / IDED15 / $\overline{SDHI1CD}$	PTC7	Z	Open	ATAPI
K24	PTD0 / IDED0 / SDHI0CLK	PTD0	Z	Open	ATAPI
K25	PTD1 / IDED1 / SDHI0CMD	PTD1	Z	Open	ATAPI
M22	PTD2 / IDED2 / SDHI0D0	PTD2	Z	Open	ATAPI
L24	PTD3 / IDED3 / SDHI0D1	PTD3	Z	Open	ATAPI
M23	PTD4 / IDED4 / SDHI0D2	PTD4	Z	Open	ATAPI

Pin No.	Pin Name	Default Function	Initial State	Handling	Group
L25	PTD5 / IDED5 / SDHI0D3	PTD5	Z	Open	ATAPI
M24	PTD6 / IDED6 / SDHI0WP	PTD6	Z	Open	ATAPI
N22	PTD7 / IDED7 / $\overline{\text{SDHI0CD}}$	PTD7	Z	Open	ATAPI
R23	PTE0 / IDEIORDY / SCIF4_TXD	PTE0	Z	Open	ATAPI
R24	PTE1 / IODREQ / SCIF4_RXD	PTE1	Z	Open	ATAPI
R25	PTE2 / $\overline{\text{IODACK}}$ / SCIF4_SCK	PTE2	Z	Open	ATAPI
T23	PTE3 / $\overline{\text{IDERST}}$ / SCIF5_TXD	PTE3	Z	Open	ATAPI
R22	PTE4 / $\overline{\text{EXBUF\_ENB}}$ / SCIF5_RXD	PTE4	Z	Open	ATAPI
T22	PTE5 / DIRECTION / SCIF5_SCK	PTE5	Z	Open	ATAPI
J23	PTF0 / IDEA0 / MSIOF0_MCK	PTF0	Z	Open	ATAPI
H24	PTF1 / IDEA1 / MSIOF0_TXD	PTF1	Z	Open	ATAPI
H25	PTF2 / IDEA2 / MSIOF0_RXD	PTF2	Z	Open	ATAPI
K23	PTF3 / $\overline{\text{IDECS0}}$ / MSIOF0_TSCK	PTF3	Z	Open	ATAPI
J24	PTF4 / $\overline{\text{IDECS1}}$ / MSIOF0_TSYNC	PTF4	Z	Open	ATAPI
J25	PTF5 / $\overline{\text{IDEIORD}}$ / $\overline{\text{MSIOF0\_SS1}}$ / MSIOF0_RSCK	PTF5	Z	Open	ATAPI
L22	PTF6 / $\overline{\text{IDEIOWR}}$ / $\overline{\text{MSIOF0\_SS2}}$ / MSIOF0_RSYNC	PTF6	Z	Open	ATAPI
L23	PTF7 / IDEINT	PTF7	Z	Open	ATAPI
U23	HPA1	HPA1	O	Open	SBSC

Pin No.	Pin Name	Default Function	Initial State	Handling	Group
U24	HPA2	HPA2	O	Open	SBSC
U25	HPA3	HPA3	O	Open	SBSC
V25	HPA4	HPA4	O	Open	SBSC
V24	HPA5	HPA5	O	Open	SBSC
W25	HPA6	HPA6	O	Open	SBSC
W24	HPA7	HPA7	O	Open	SBSC
Y25	HPA8	HPA8	O	Open	SBSC
Y24	HPA9	HPA9	O	Open	SBSC
V23	HPA10	HPA10	O	Open	SBSC
AA25	HPA11	HPA11	O	Open	SBSC
AB25	HPA12	HPA12	O	Open	SBSC
AB23	HPA13	HPA13	O	Open	SBSC
W23	HPA14	HPA14	O	Open	SBSC
W22	HPA15	HPA15	O	Open	SBSC
V22	HPA0	HPA0	O	Open	SBSC
AD19	HPD0	HPD0	Z	Open	SBSC
AB19	HPD1	HPD1	Z	Open	SBSC
AC19	HPD2	HPD2	Z	Open	SBSC
AE20	HPD3	HPD3	Z	Open	SBSC
AD20	HPD4	HPD4	Z	Open	SBSC
AC20	HPD5	HPD5	Z	Open	SBSC
AB20	HPD6	HPD6	Z	Open	SBSC
AE21	HPD7	HPD7	Z	Open	SBSC
AB21	HPD8	HPD8	Z	Open	SBSC
AC22	HPD9	HPD9	Z	Open	SBSC
AB22	HPD10	HPD10	Z	Open	SBSC
AE23	HPD11	HPD11	Z	Open	SBSC
AD23	HPD12	HPD12	Z	Open	SBSC
AC23	HPD13	HPD13	Z	Open	SBSC
AE24	HPD14	HPD14	Z	Open	SBSC
AD24	HPD15	HPD15	Z	Open	SBSC

Pin No.	Pin Name	Default Function	Initial State	Handling	Group
AE14	HPD16	HPD16	Z	Open	SBSC
AD14	HPD17	HPD17	Z	Open	SBSC
AC14	HPD18	HPD18	Z	Open	SBSC
AE15	HPD19	HPD19	Z	Open	SBSC
AD15	HPD20	HPD20	Z	Open	SBSC
AB15	HPD21	HPD21	Z	Open	SBSC
AC15	HPD22	HPD22	Z	Open	SBSC
AE16	HPD23	HPD23	Z	Open	SBSC
AD17	HPD24	HPD24	Z	Open	SBSC
AC17	HPD25	HPD25	Z	Open	SBSC
AB17	HPD26	HPD26	Z	Open	SBSC
AE18	HPD27	HPD27	Z	Open	SBSC
AD18	HPD28	HPD28	Z	Open	SBSC
AB18	HPD29	HPD29	Z	Open	SBSC
AC18	HPD30	HPD30	Z	Open	SBSC
AE19	HPD31	HPD31	Z	Open	SBSC
AA24	$\overline{\text{HPCAS}}$	$\overline{\text{HPCAS}}$	O	Open	SBSC
AB24	HPCKE	HPCKE	O	Open	SBSC
AC24	HPCLK	HPCLK	O	Open	SBSC
AC25	$\overline{\text{HPCLK}}$	$\overline{\text{HPCLK}}$	O	Open	SBSC
Y23	$\overline{\text{HPCS}}$	$\overline{\text{HPCS}}$	O	Open	SBSC
AC21	HPDQM0	HPDQM0	O	Open	SBSC
AE22	HPDQM1	HPDQM1	O	Open	SBSC
AB16	HPDQM2	HPDQM2	O	Open	SBSC
AC16	HPDQM3	HPDQM3	O	Open	SBSC
AD21	HPDQS0	HPDQS0	O	Open	SBSC
AD22	HPDQS1	HPDQS1	O	Open	SBSC
AD16	HPDQS2	HPDQS2	O	Open	SBSC
AE17	HPDQS3	HPDQS3	O	Open	SBSC
Y22	$\overline{\text{HPRAS}}$	$\overline{\text{HPRAS}}$	O	Open	SBSC
AA23	HPRDWR	HPRDWR	O	Open	SBSC

Pin No.	Pin Name	Default Function	Initial State	Handling	Group
G25	PTM0 / LCDD0 / DV_D0	PTM0	Z	Open	LCDC
G24	PTM1 / LCDD1 / DV_D1	PTM1	Z	Open	LCDC
H23	PTM2 / LCDD2 / DV_D2	PTM2	Z	Open	LCDC
J22	PTM3 / LCDD3 / DV_D3	PTM3	Z	Open	LCDC
F25	PTM4 / LCDD4 / DV_D4	PTM4	Z	Open	LCDC
F24	PTM5 / LCDD5 / DV_D5	PTM5	Z	Open	LCDC
K22	PTM6 / LCDD6 / DV_D6	PTM6	Z	Open	LCDC
G23	PTM7 / LCDD7 / DV_D7	PTM7	Z	Open	LCDC
H22	PTL0 / LCDD8 / DV_D8	PTL0	Z	Open	LCDC
E25	PTL1 / LCDD9 / DV_D9	PTL1	Z	Open	LCDC
E24	PTL2 / LCDD10 / DV_D10	PTL2	Z	Open	LCDC
F23	PTL3 / LCDD11 / DV_D11	PTL3	Z	Open	LCDC
G22	PTL4 / LCDD12 / DV_D12	PTL4	Z	Open	LCDC
D24	PTL5 / LCDD13 / DV_D13	PTL5	Z	Open	LCDC
D25	PTL6 / LCDD14 / DV_D14	PTL6	Z	Open	LCDC
F22	PTL7 / LCDD15 / DV_D15	PTL7	Z	Open	LCDC
E23	PTN0 / LCDD16 / DV_HSYNC	PTN0	Z	Open	LCDC
D23	PTN1 / LCDD17 / DV_VSYNC	PTN1	Z	Open	LCDC
C25	PTN2 / LCDD18 / SCIF4_TXD	PTN2	Z	Open	LCDC
C24	PTN3 / LCDD19 / SCIF4_RXD	PTN3	Z	Open	LCDC
E22	PTN4 / LCDD20 / SCIF4_SCK	PTN4	Z	Open	LCDC
B25	PTN5 / LCDD21 / SCIF5_TXD	PTN5	Z	Open	LCDC

Pin No.	Pin Name	Default Function	Initial State	Handling	Group
B23	PTN6 / LCDD22 / SCIF5_RXD	PTN6	Z	Open	LCDC
A23	PTN7 / LCDD23 / SCIF5_SCK	PTN7	Z	Open	LCDC
A21	PTH0 / LCDVEPWC	PTH0	Z	Open	LCDC
B21	PTH1 / LCDDCK / $\overline{\text{LCDWR}}$	PTH1	Z	Open	LCDC
C21	PTH2 / LCDDON	PTH2	Z	Open	LCDC
D20	PTH3 / LCDHSYN / $\overline{\text{LCDCS}}$	PTH3	Z	Open	LCDC
D21	PTH4 / LCDDISP / LCDRS	PTH4	Z	Open	LCDC
A22	PTH5 / LCDVSYN / DV_CLK	PTH5	Z	Open	LCDC
B22	PTH6 / $\overline{\text{LCDRD}}$ / DV_CLKI	PTH6	Z	Open	LCDC
C22	PTH7 / LCDVCPWC	PTH7	Z	Open	LCDC
L3	PTK0 / SIUAMCK / MSIOF1_MCK	PTK0	Z	Open	SIU
K2	PTK1 / SIUAOSLD / MSIOF1_TXD	PTK1	Z	Open	SIU
J1	PTK2 / SIUAOBT / MSIOF1_TSCK	PTK2	Z	Open	SIU
J2	PTK3 / SIUAOLR / MSIOF1_TSYNC	PTK3	Z	Open	SIU
K3	PTK4 / SIUAISLD / MSIOF1_RXD	PTK4	Z	Open	SIU
H1	PTK5 / SIUAIBT / $\overline{\text{MSIOF1\_SS1}}$ / MSIOF1_RSCK	PTK5	Z	Open	SIU
H2	PTK6 / SIUAILR / $\overline{\text{MSIOF1\_SS2}}$ / MSIOF1_RSYNC	PTK6	Z	Open	SIU
J3	PTK7 / SIUAFCK	PTK7	Z	Open	SIU
G1	PTS0 / SCIF3_TXD / SDHI0CLK	PTS0	Z	Open	SCIF3

Pin No.	Pin Name	Default Function	Initial State	Handling	Group
G2	PTS1 / SCIF3_RXD / SDHI0CMD	PTS1	Z	Open	SCIF3
H3	PTS2 / SCIF3_SCK / SDHI0D0	PTS2	Z	Open	SCIF3
J4	PTS3 / $\overline{\text{SCIF3\_RTS}}$ / SDHI0D1	PTS3	Z	Open	SCIF3
F2	PTS4 / $\overline{\text{SCIF3\_CTS}}$ / SDHI0D2	PTS4	Z	Open	SCIF3
L4	PTS5 / SCIF1_TXD / SDHI0D3	PTS5	Z	Open	SCIF1
G3	PTS6 / SCIF1_RXD / SDHI0WP	PTS6	Z	Open	SCIF1
H4	PTS7 / SCIF1_SCK / $\overline{\text{SDHI0CD}}$	PTS7	Z	Open	SCIF1
F4	PTT0 / SCIF2_TXD / $\overline{\text{MSIOF0\_SS2}}$ / MSIOF0_RSYNC	PTT0	Z	Open	SCIF2
D1	PTT1 / SCIF2_RXD / $\overline{\text{MSIOF0\_SS1}}$ / MSIOF0_RSCK	PTT1	Z	Open	SCIF2
F3	PTT2 / SCIF2_SCK / MSIOF0_TSYNC	PTT2	Z	Open	SCIF2
G4	PTT3 / SCIF0_TXD / MSIOF0_TXD	PTT3	Z	Open	SCIF0
E2	PTT4 / SCIF0_RXD / MSIOF0_RXD	PTT4	Z	Open	SCIF0
K4	PTT5 / SCIF0_SCK / MSIOF0_TSCK	PTT5	Z	Open	SCIF0
N2	PTU0 / $\overline{\text{FCE}}$ / SCIF2_TXD / VIO_HD2	PTU0	Z	Open	FLCTL
N3	PTU1 / FRB / SCIF2_RXD / VIO_CLK2	PTU1	Z	Open	FLCTL
M1	PTU2 / FOE / SCIF2_SCK / VIO_VD2	PTU2	Z	Open	FLCTL
M2	PTU3 / $\overline{\text{FWE}}$ / SCIF0_TXD	PTU3	Z	Open	FLCTL

Pin No.	Pin Name	Default Function	Initial State	Handling	Group
M3	PTU4 / FSC / SCIF0_RXD	PTU4	Z	Open	FLCTL
N4	PTU5 / FCDE / SCIF0_SCK	PTU5	Z	Open	FLCTL
N1	PTV0 / NAF0 / SCIF3_TXD / VIO_D8	PTV0	Z	Open	FLCTL
P2	PTV1 / NAF1 / SCIF3_RXD / VIO_D9	PTV1	Z	Open	FLCTL
P3	PTV2 / NAF2 / SCIF3_SCK / VIO_D10	PTV2	Z	Open	FLCTL
P1	PTV3 / NAF3 / $\overline{\mathrm{SCIF3\_RTS}}$ / VIO_D11	PTV3	Z	Open	FLCTL
P4	PTV4 / NAF4 / $\overline{\mathrm{SCIF3\_CTS}}$ / VIO_D12	PTV4	Z	Open	FLCTL
R1	PTV5 / NAF5 / SCIF1_TXD / VIO_D13	PTV5	Z	Open	FLCTL
R4	PTV6 / NAF6 / SCIF1_RXD / VIO_D14	PTV6	Z	Open	FLCTL
R2	PTV7 / NAF7 / SCIF1_SCK / VIO_D15	PTV7	Z	Open	FLCTL
E1	SCL	SCL	Z	Pull up	IIC
F1	SDA	SDA	Z	Pull up	IIC
D3	PTW0 / IRQ0 / SIUAOSPD	PTW0	Z	Open	Interrupt
C3	PTW1 / IRQ1 / SIUAISPD	PTW1	Z	Open	Interrupt
B2	PTW2 / IRQ2 / $\overline{\mathrm{BS}}$ / VIO_CKO	PTW2	Z	Open	Interrupt
D4	PTW3 / IRQ3 / ADTRG	PTW3	Z	Open	Interrupt
B20	PTW4 / IRQ4 / LCDLCLK	PTW4	Z	Open	Interrupt
A20	PTW5 / IRQ5	PTW5	Z	Open	Interrupt
D19	PTW6 / IRQ6	PTW6	Z	Open	Interrupt
C20	PTW7 / IRQ7	PTW7	Z	Open	Interrupt
D2	PTX0 / TS0_SPSYNC	PTX0	Z	Open	TS-DMUX0

Pin No.	Pin Name	Default Function	Initial State	Handling	Group
E3	PTX1 / TS0_SDEN	PTX1	Z	Open	TS-DMUX0
C2	PTX2 / TS0_SCK	PTX2	Z	Open	TS-DMUX0
E4	PTX3 / TS0_SDAT	PTX3	Z	Open	TS-DMUX0
C8	PTX4 / DREQ0 / $\overline{\text{IRDA\_IN}}$	PTX4	Z	Open	DMAC
C9	PTX5 / DACK0 / IRDA_OUT	PTX5	Z	Open	DMAC
B8	PTX6 / DREQ1 / MSIOF0_MCK	PTX6	Z	Open	DMAC
D9	PTX7 / DACK1	PTX7	Z	Open	DMAC
A8	PTY0 / VIO_D0	PTY0	Z	Open	VIO
D11	PTY1 / VIO_D1	PTY1	Z	Open	VIO
C10	PTY2 / VIO_D2	PTY2	Z	Open	VIO
B9	PTY3 / VIO_D3	PTY3	Z	Open	VIO
D10	PTY4 / VIO_D4	PTY4	Z	Open	VIO
A9	PTY5 / VIO_D5	PTY5	Z	Open	VIO
C11	PTY6 / VIO_D6	PTY6	Z	Open	VIO
B10	PTY7 / VIO_D7	PTY7	Z	Open	VIO
A10	PTZ0 / VIO_CLK1 / SIUBISLD	PTZ0	Z	Open	VIO
B11	PTZ1 / VIO_VD1 / SIUBIBT	PTZ1	Z	Open	VIO
C12	PTZ2 / VIO_HD1 / SIUBILR	PTZ2	Z	Open	VIO
A11	PTZ3 / VIO_FLD / SIUBFCK	PTZ3	Z	Open	VIO
L1	PTZ4 / SIUBMCK	PTZ4	Z	Open	SIUB
M4	PTZ5 / SIUBOSLD	PTZ5	Z	Open	SIUB
L2	PTZ6 / SIUBOBT	PTZ6	Z	Open	SIUB
K1	PTZ7 / SIUBOLR	PTZ7	Z	Open	SIUB
D18	MD0	MD0	I	Use	Mode
C19	MD1	MD1	I	Use	Mode
D17	MD2	MD2	I	Use	Mode

Pin No.	Pin Name	Default Function	Initial State	Handling	Group
B19	$\overline{\text{TSTMD}}$	$\overline{\text{TSTMD}}$	I	Pull up	Mode
D15	MD5	MD5	I	Use	Mode
C18	MD8	MD8	I	Pull up or pull down	Mode
B18	$\overline{\text{RESETA}}$	$\overline{\text{RESETA}}$	I	Pull up	System
A18	RCLK	RCLK	I	Use	Clock
B17	$\overline{\text{RESETP}}$	$\overline{\text{RESETP}}$	I	Use	System
C16	$\overline{\text{RESETOUT}}$	$\overline{\text{RESETOUT}}$	H	Open	System
A19	PTJ7 / STATUS0	STATUS0	O	Open	System
C17	BOOT	BOOT	I	Pull down	System
D16	PTJ5 / PDSTATUS	PDSTATUS	O	Open	System
A17	$\overline{\text{TST}}$	$\overline{\text{TST}}$	I	Pull up	Mode
B16	TCK	TCK	IU	Open	H-UDI
C15	TMS	TMS	IU	Open	H-UDI
A16	TDI	TDI	IU	Open	H-UDI
B15	TDO	TDO	Z/O	Open	H-UDI
A15	$\overline{\text{TRST}}$	$\overline{\text{TRST}}$	IU	Use	H-UDI
C13	PTG0 / AUDATA0 / TPUTO0	PTG0	Z	Open	AUD
D13	PTG1 / AUDATA1 / TPUTO1	PTG1	Z	Open	AUD
A14	PTG2 / AUDATA2 / TPUTO2	PTG2	Z	Open	AUD
B14	PTG3 / AUDATA3 / TPUTO3	PTG3	Z	Open	AUD
C14	PTG4 / AUDSYNC	PTG4	Z	Open	AUD
D14	PTG5 / AUDCK	PTG5	Z	Open	AUD
D12	$\overline{\text{ASEBRK}}$/BRKAK	$\overline{\text{ASEBRK}}$/ BRKAK	IU	Open	H-UDI
B13	MPMD	MPMD	IU	Pull up	H-UDI
A13	EXTAL	EXTAL	I	Pull down	Clock
A12	XTAL	XTAL	O	Open	Clock

Pin No.	Pin Name	Default Function	Initial State	Handling	Group
B12	NMI	NMI	I	Pull up	Interrupt
AA7	$V_{cc}Q$	$V_{cc}Q$	—	Use	Power
AA8	$V_{cc}Q$	$V_{cc}Q$	—	Use	Power
AA11	$V_{cc}Q$	$V_{cc}Q$	—	Use	Power
AA12	$V_{cc}Q$	$V_{cc}Q$	—	Use	Power
AD13	$V_{cc}Q$	$V_{cc}Q$	—	Use	Power
E10	$V_{cc}Q$	$V_{cc}Q$	—	Use	Power
E11	$V_{cc}Q$	$V_{cc}Q$	—	Use	Power
E14	$V_{cc}Q$	$V_{cc}Q$	—	Use	Power
E15	$V_{cc}Q$	$V_{cc}Q$	—	Use	Power
E18	$V_{cc}Q$	$V_{cc}Q$	—	Use	Power
E19	$V_{cc}Q$	$V_{cc}Q$	—	Use	Power
G5	$V_{cc}Q$	$V_{cc}Q$	—	Use	Power
G21	$V_{cc}Q$	$V_{cc}Q$	—	Use	Power
H5	$V_{cc}Q$	$V_{cc}Q$	—	Use	Power
H21	$V_{cc}Q$	$V_{cc}Q$	—	Use	Power
K21	$V_{cc}Q$	$V_{cc}Q$	—	Use	Power
L5	$V_{cc}Q$	$V_{cc}Q$	—	Use	Power
L21	$V_{cc}Q$	$V_{cc}Q$	—	Use	Power
M5	$V_{cc}Q$	$V_{cc}Q$	—	Use	Power
P21	$V_{cc}Q$	$V_{cc}Q$	—	Use	Power
R5	$V_{cc}Q$	$V_{cc}Q$	—	Use	Power
R21	$V_{cc}Q$	$V_{cc}Q$	—	Use	Power
T5	$V_{cc}Q$	$V_{cc}Q$	—	Use	Power
T24	$V_{cc}Q$	$V_{cc}Q$	—	Use	Power
W5	$V_{cc}Q$	$V_{cc}Q$	—	Use	Power
Y5	$V_{cc}Q$	$V_{cc}Q$	—	Use	Power
AA15	$V_{cc}Q$_DDR	$V_{cc}Q$_DDR	—	Use	Power
AA16	$V_{cc}Q$_DDR	$V_{cc}Q$_DDR	—	Use	Power
AA19	$V_{cc}Q$_DDR	$V_{cc}Q$_DDR	—	Use	Power
AA20	$V_{cc}Q$_DDR	$V_{cc}Q$_DDR	—	Use	Power

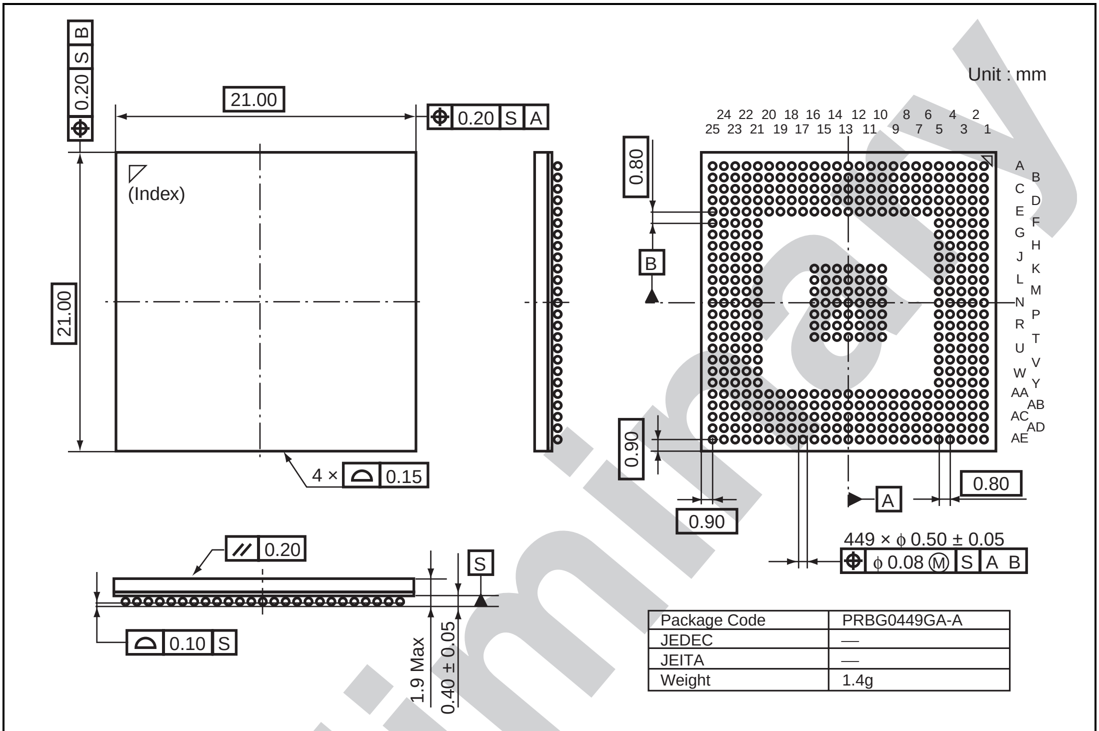
Pin No.	Pin Name	Default Function	Initial State	Handling	Group
AB14	V_{CC}Q_DDR	V_{CC}Q_DDR	—	Use	Power
AD25	V_{CC}Q_DDR	V_{CC}Q_DDR	—	Use	Power
AE13	V_{CC}Q_DDR	V_{CC}Q_DDR	—	Use	Power
T25	V_{CC}Q_DDR	V_{CC}Q_DDR	—	Use	Power
U22	V_{CC}Q_DDR	V_{CC}Q_DDR	—	Use	Power
V21	V_{CC}Q_DDR	V_{CC}Q_DDR	—	Use	Power
W21	V_{CC}Q_DDR	V_{CC}Q_DDR	—	Use	Power
K10	V_{DD}	V_{DD}	—	Use	Power
K11	V_{DD}	V_{DD}	—	Use	Power
K12	V_{DD}	V_{DD}	—	Use	Power
K13	V_{DD}	V_{DD}	—	Use	Power
K14	V_{DD}	V_{DD}	—	Use	Power
K15	V_{DD}	V_{DD}	—	Use	Power
K16	V_{DD}	V_{DD}	—	Use	Power
L10	V_{DD}	V_{DD}	—	Use	Power
L11	V_{DD}	V_{DD}	—	Use	Power
L15	V_{DD}	V_{DD}	—	Use	Power
L16	V_{DD}	V_{DD}	—	Use	Power
M10	V_{DD}	V_{DD}	—	Use	Power
M16	V_{DD}	V_{DD}	—	Use	Power
N10	V_{DD}	V_{DD}	—	Use	Power
N16	V_{DD}	V_{DD}	—	Use	Power
P10	V_{DD}	V_{DD}	—	Use	Power
P16	V_{DD}	V_{DD}	—	Use	Power
R10	V_{DD}	V_{DD}	—	Use	Power
R11	V_{DD}	V_{DD}	—	Use	Power
R15	V_{DD}	V_{DD}	—	Use	Power
R16	V_{DD}	V_{DD}	—	Use	Power
T10	V_{DD}	V_{DD}	—	Use	Power
T11	V_{DD}	V_{DD}	—	Use	Power
T12	V_{DD}	V_{DD}	—	Use	Power

Pin No.	Pin Name	Default Function	Initial State	Handling	Group
T13	V_{DD}	V_{DD}	—	Use	Power
T14	V_{DD}	V_{DD}	—	Use	Power
T15	V_{DD}	V_{DD}	—	Use	Power
T16	V_{DD}	V_{DD}	—	Use	Power
B24	V_{DD}_DLL	V_{DD}_DLL	—	Use	Power
E20	V_{DD}_PLL1	V_{DD}_PLL1	—	Use	Power
AA22	VREF	VREF	—	Use	Power
A1	V_{SS}	V_{SS}	—	Use	Power
A25	V_{SS}	V_{SS}	—	Use	Power
AA5	V_{SS}	V_{SS}	—	Use	Power
AA6	V_{SS}	V_{SS}	—	Use	Power
AA9	V_{SS}	V_{SS}	—	Use	Power
AA10	V_{SS}	V_{SS}	—	Use	Power
AA13	V_{SS}	V_{SS}	—	Use	Power
AA14	V_{SS}	V_{SS}	—	Use	Power
AA17	V_{SS}	V_{SS}	—	Use	Power
AA18	V_{SS}	V_{SS}	—	Use	Power
AA21	V_{SS}	V_{SS}	—	Use	Power
AE1	V_{SS}	V_{SS}	—	Use	Power
AE25	V_{SS}	V_{SS}	—	Use	Power
C23	V_{SS}	V_{SS}	—	Use	Power
D8	V_{SS}	V_{SS}	—	Use	Power
D22	V_{SS}	V_{SS}	—	Use	Power
E5	V_{SS}	V_{SS}	—	Use	Power
E8	V_{SS}	V_{SS}	—	Use	Power
E9	V_{SS}	V_{SS}	—	Use	Power
E12	V_{SS}	V_{SS}	—	Use	Power
E13	V_{SS}	V_{SS}	—	Use	Power
E16	V_{SS}	V_{SS}	—	Use	Power
E17	V_{SS}	V_{SS}	—	Use	Power
F5	V_{SS}	V_{SS}	—	Use	Power

Pin No.	Pin Name	Default Function	Initial State	Handling	Group
F21	V_{SS}	V_{SS}	—	Use	Power
J5	V_{SS}	V_{SS}	—	Use	Power
J21	V_{SS}	V_{SS}	—	Use	Power
K5	V_{SS}	V_{SS}	—	Use	Power
L12	V_{SS}	V_{SS}	—	Use	Power
L13	V_{SS}	V_{SS}	—	Use	Power
L14	V_{SS}	V_{SS}	—	Use	Power
M11	V_{SS}	V_{SS}	—	Use	Power
M12	V_{SS}	V_{SS}	—	Use	Power
M13	V_{SS}	V_{SS}	—	Use	Power
M14	V_{SS}	V_{SS}	—	Use	Power
M15	V_{SS}	V_{SS}	—	Use	Power
M21	V_{SS}	V_{SS}	—	Use	Power
N5	V_{SS}	V_{SS}	—	Use	Power
N11	V_{SS}	V_{SS}	—	Use	Power
N12	V_{SS}	V_{SS}	—	Use	Power
N13	V_{SS}	V_{SS}	—	Use	Power
N14	V_{SS}	V_{SS}	—	Use	Power
N15	V_{SS}	V_{SS}	—	Use	Power
N21	V_{SS}	V_{SS}	—	Use	Power
P5	V_{SS}	V_{SS}	—	Use	Power
P11	V_{SS}	V_{SS}	—	Use	Power
P12	V_{SS}	V_{SS}	—	Use	Power
P13	V_{SS}	V_{SS}	—	Use	Power
P14	V_{SS}	V_{SS}	—	Use	Power
P15	V_{SS}	V_{SS}	—	Use	Power
R12	V_{SS}	V_{SS}	—	Use	Power
R13	V_{SS}	V_{SS}	—	Use	Power
R14	V_{SS}	V_{SS}	—	Use	Power
T21	V_{SS}	V_{SS}	—	Use	Power
U5	V_{SS}	V_{SS}	—	Use	Power

Pin No.	Pin Name	Default Function	Initial State	Handling	Group
U21	V_{SS}	V_{SS}	—	Use	Power
V5	V_{SS}	V_{SS}	—	Use	Power
Y21	V_{SS}	V_{SS}	—	Use	Power
A24	V_{SS}_DLL	V_{SS}_DLL	—	Use	Power
E21	V_{SS}_PLL1	V_{SS}_PLL1	—	Use	Power

C. Package Dimension



Package Code	PRBG0449GA-A
JEDEC	—
JEITA	—
Weight	1.4g

Figure C.1 Package Dimension

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

RENESAS SALES OFFICES

http://www.renesas.com

Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

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Colophon 6.2

SH7723
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