User's Manual

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R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group

User's Manual: Hardware

RENESAS MCU
R8C Family / R8C/3x Series

Renesas Electronics
www.renesas.com

Rev.1.10 Jun 2013

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(2012.4)

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.
The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
Datasheet	Hardware overview and electrical characteristics	R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group Datasheet	R01DS0014EJ0100
User's Manual: Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description Note: Refer to the application notes for details on using peripheral functions.	R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group User's Manual: Hardware	This User's Manual
User's Manuall: Software	Description of CPU instruction set	R8C/Tiny Series Software Manual	REJ09B0001
Application note	Information on using peripheral functions and application examples Sample programs Information on writing programs in assembly language and C	Available from Renesas Electronics Web site.	
Renesas technical update	Product specifications, updates on documents, etc.		

2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

(1) Register Names, Bit Names, and Pin Names
Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word “register,” “bit,” or “pin” to distinguish the three categories.
Examples the PM03 bit in the PM0 register
P3_5 pin, VCC pin

(2) Notation of Numbers
The indication “b” is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication “h” is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.
Examples Binary: 11b
Hexadecimal: EFA0h
Decimal: 1234

3. Register Notation

The symbols and terms used in register diagrams are described below.

x.x.x XXX Register (Symbol)

Address XXXXh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	XXX7	XXX6	XXX5	XXX4	—	—	XXX1	XXX0
After Reset	0	0	0	0	0	0	0	0

*1

Bit	Symbol	Bit Name	Function	R/W
b0	XXX0	XXX bit	b1 b0 0 0: XXX 0 1: XXX 1 0: Do not set. 1 1: XXX	R/W
b1	XXX1			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b3	—	Reserved bit	Set to 0.	R/W
b4	XXX4	XXX bit	Function varies according to the operating mode.	R/W
b5	XXX5			W
b6	XXX6			R/W
b7	XXX7	XXX bit	0: XXX 1: XXX	R

*2

*3

*1

R/W: Read and write.
R: Read only.
W: Write only.
–: Nothing is assigned.

*2

- Reserved bit

  Reserved bit. Set to specified value.

*3

- Nothing is assigned.

  Nothing is assigned to the bit. As the bit may be used for future functions, if necessary, set to 0.
- Do not set to a value.

  Operation is not guaranteed when a value is set.
- Function varies according to the operating mode.

  The function of the bit varies with the peripheral function mode. Refer to the register diagram for information on the individual modes.

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input / Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver / Transmitter
VCO	Voltage Controlled Oscillator

Table of Contents

SFR Page Reference

Address	Register	Symbol	Page
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	46
0005h	Processor Mode Register 1	PM1	209
0006h	System Clock Control Register 0	CM0	142
0007h	System Clock Control Register 1	CM1	143
0008h	Module Standby Control Register	MSTCR	279, 335, 350, 370, 385, 399, 415, 563
0009h	System Clock Control Register 3	CM3	144
000Ah	Protect Register	PRCR	170
000Bh	Reset Source Determination Register	RSTFR	46
000Ch	Oscillation Stop Detection Register	OCD	145
000Dh	Watchdog Timer Reset Register	WDTR	209
000Eh	Watchdog Timer Start Register	WDTS	209
000Fh	Watchdog Timer Control Register	WDTC	210
0010h			
0011h			
0012h			
0013h			
0014h			
0015h	High-Speed On-Chip Oscillator Control Register 7	FRA7	145
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	210
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	146
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	146
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	147
0026h	On-Chip Reference Voltage Control Register	OCVREFCR	666
0027h			
0028h			
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	148
002Ah	High-Speed On-Chip Oscillator Control Register 5	FRA5	148
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	148
002Ch			
002Dh			
002Eh			
002Fh	High-Speed On-Chip Oscillator Control Register 3	FRA3	148
0030h	Voltage Monitor Circuit Control Register	CMPA	59
0031h	Voltage Monitor Circuit Edge Select Register	VCAC	60
0032h			
0033h	Voltage Detect Register 1	VCA1	60
0034h	Voltage Detect Register 2	VCA2	61, 149
0035h			
0036h	Voltage Detection 1 Level Select Register	VD1LS	62
0037h			
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	63
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	64
003Ah	Voltage Monitor 2 Circuit Control Register	VW2C	65
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			

Note:
1. The blank regions are reserved. Do not access locations in these regions.

Address	Register	Symbol	Page
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	177
0042h	Timer RA1 Interrupt Control Register	TRA1IC	176
0043h			
0044h			
0045h			
0046h	INT4 Interrupt Control Register	INT4IC	178
0047h	Timer RC Interrupt Control Register	TRCIC	177
0048h	Timer RD0 Interrupt Control Register	TRD0IC	177
0049h	Timer RD1 Interrupt Control Register	TRD1IC	177
004Ah	Timer RE Interrupt Control Register	TREIC	176
004Bh	UART2 Transmit Interrupt Control Register	S2TIC	176
004Ch	UART2 Receive Interrupt Control Register	S2RIC	176
004Dh	Key Input Interrupt Control Register	KUPIC	176
004Eh	A/D Conversion Interrupt Control Register	ADIC	176
004Fh	SSU Interrupt Control Register	SSUIC	177
0050h	Timer RF Compare 1 Interrupt Control Register	CMP1IC	176
0051h	UART0 Transmit Interrupt Control Register	S0TIC	176
0052h	UART0 Receive Interrupt Control Register	S0RIC	176
0053h	UART1 Transmit Interrupt Control Register	S1TIC	176
0054h	UART1 Receive Interrupt Control Register	S1RIC	176
0055h	INT2 Interrupt Control Register	INT2IC	178
0056h	Timer RA0 Interrupt Control Register	TRA0IC	176
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	176
0059h	INT1 Interrupt Control Register	INT1IC	178
005Ah	INT3 Interrupt Control Register	INT3IC	178
005Bh	Timer RF Interrupt Control Register	TRFIC	176
005Ch	Timer RF Compare 0 Interrupt Control Register	CMP0IC	176
005Dh	INT0 Interrupt Control Register	INT0IC	178
005Eh	UART2 Bus Collision Detection Interrupt Control Register	U2BCNIC	176
005Fh	Timer RF Capture Interrupt Control Register	CAPIC	176
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh	Timer RG Interrupt Control Register	TRGIC	177
006Ch	CAN0 Reception Complete Interrupt Control Register	C0RIC	176
006Dh	CAN0 Transmission Complete Interrupt Control Register	C0TIC	176
006Eh	CAN0 Receive FIFO Interrupt Control Register	C0FRIC	176
006Fh	CAN0 Transmit FIFO Interrupt Control Register	C0FTIC	176
0070h	CAN0 Error Interrupt Control Register	C0EIC	176
0071h	CAN0 Wake-up Interrupt Control Register	C0WIC	176
0072h	Voltage Monitor 1 Interrupt Control Register	VCMP1IC	176
0073h	Voltage Monitor 2 Interrupt Control Register	VCMP2IC	176
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

Address	Register	Symbol	Page
0080h	DTC Activation Control Register	DTCTL	221
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DTC Activation Enable Register 0	DTCEN0	220
0089h	DTC Activation Enable Register 1	DTCEN1	220
008Ah	DTC Activation Enable Register 2	DTCEN2	220
008Bh	DTC Activation Enable Register 3	DTCEN3	220
008Ch	DTC Activation Enable Register 4	DTCEN4	220
008Dh	DTC Activation Enable Register 5	DTCEN5	220
008Eh	DTC Activation Enable Register 6	DTCEN6	220
008Fh			
0090h	Timer RF Register	TRF	447
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah	Timer RF Control Register 0	TRFCR0	448
009Bh	Timer RF Control Register 1	TRFCR1	449
009Ch	Capture and Compare 0 Register	TRFM0	447
009Dh			
009Eh	Compare 1 Register	TRFM1	448
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	493
00A1h	UART0 Bit Rate Register	U0BRG	493
00A2h	UART0 Transmit Buffer Register	U0TB	494
00A3h			
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	495
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	495
00A6h	UART0 Receive Buffer Register	U0RB	496
00A7h			
00A8h	UART2 Transmit/Receive Mode Register	U2MR	515
00A9h	UART2 Bit Rate Register	U2BRG	515
00AAh	UART2 Transmit Buffer Register	U2TB	516
00ABh			
00ACh	UART2 Transmit/Receive Control Register 0	U2C0	517
00ADh	UART2 Transmit/Receive Control Register 1	U2C1	518
00AEh	UART2 Receive Buffer Register	U2RB	519
00AFh			
00B0h	UART2 Digital Filter Function Select Register	URXDF	520
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	520
00BCh	UART2 Special Mode Register 4	U2SMR4	521
00BDh	UART2 Special Mode Register 3	U2SMR3	521
00BEh	UART2 Special Mode Register 2	U2SMR2	522
00BFh	UART2 Special Mode Register	U2SMR	522

Address	Register	Symbol	Page
00C0h	A/D Register 0	AD0	667
00C1h			
00C2h	A/D Register 1	AD1	667
00C3h			
00C4h	A/D Register 2	AD2	667
00C5h			
00C6h	A/D Register 3	AD3	667
00C7h			
00C8h	A/D Register 4	AD4	667
00C9h			
00CAh	A/D Register 5	AD5	667
00CBh			
00CCh	A/D Register 6	AD6	667
00CDh			
00CEh	A/D Register 7	AD7	667
00CFh			
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Mode Register	ADMOD	668
00D5h	A/D Input Select Register	ADINSEL	669
00D6h	A/D Control Register 0	ADCON0	670
00D7h	A/D Control Register 1	ADCON1	671
00D8h			
00D9h			
00DAh			
00DBh			
00DCh			
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	97
00E1h	Port P1 Register	P1	97
00E2h	Port P0 Direction Register	PD0	96
00E3h	Port P1 Direction Register	PD1	96
00E4h	Port P2 Register	P2	97
00E5h	Port P3 Register	P3	97
00E6h	Port P2 Direction Register	PD2	96
00E7h	Port P3 Direction Register	PD3	96
00E8h	Port P4 Register	P4	97
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00EAh	Port P4 Direction Register	PD4	96
00EBh	Port P5 Direction Register	PD5	96
00ECh	Port P6 Register	P6	97
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00F1h	Port P9 Register	P9	97
00F2h	Port P8 Direction Register	PD8	96
00F3h	Port P9 Direction Register	PD9	96
00F4h			
00F5h			
00F6h			
00F7h			
00F8h			
00F9h			
00FAh			
00FBh			
00FCh			
00FDh			
00FEh			
00FFh			

Note:
1. The blank regions are reserved. Do not access locations in these regions.

Address	Register	Symbol	Page
0100h	Timer RA0 Control Register	TRA0CR	240
0101h	Timer RA0 I/O Control Register	TRA0IOC	240, 243, 246, 248, 250, 253
0102h	Timer RA0 Mode Register	TRA0MR	241
0103h	Timer RA0 Prescaler Register	TRA0PRE	241
0104h	Timer RA0 Register	TRA0	242
0105h	LIN0 Control Register 2	LIN0CR2	594
0106h	LIN0 Control Register	LIN0CR	595
0107h	LIN0 Status Register	LIN0ST	595
0108h	Timer RB Control Register	TRBCR	257
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010Bh	Timer RB Mode Register	TRBMR	258
010Ch	Timer RB Prescaler Register	TRBPRE	259
010Dh	Timer RB Secondary Register	TRBSC	259
010Eh	Timer RB Primary Register	TRBPR	260
010Fh			
0110h	Timer RA1 Control Register	TRA1CR	240
0111h	Timer RA1 I/O Control Register	TRA1IOC	240, 243, 246, 248, 250, 253
0112h	Timer RA1 Mode Register	TRA1MR	241
0113h	Timer RA1 Prescaler Register	TRA1PRE	241
0114h	Timer RA1 Register	TRA1	242
0115h	LIN1 Control Register 2	LIN1CR2	594
0116h	LIN1 Control Register	LIN1CR	595
0117h	LIN1 Status Register	LIN1ST	595
0118h	Timer RE Counter Data Register	TRESEC	440
0119h	Timer RE Compare Data Register	TREMIN	440
011Ah			
011Bh			
011Ch	Timer RE Control Register 1	TRECR1	441
011Dh	Timer RE Control Register 2	TRECR2	441
011Eh	Timer RE Count Source Select Register	TRECSR	442
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0124h	Timer RC I/O Control Register 0	TRCIOR0	282, 296, 302
0125h	Timer RC I/O Control Register 1	TRCIOR1	282, 297, 303
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012Ch	Timer RC General Register C	TRCGRC	283
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012Fh			

Note:
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0131h	Timer RC Digital Filter Function Select Register	TRCDF	284, 317
0132h	Timer RC Output Master Enable Register	TRCOER	285
0133h	Timer RC Trigger Control Register	TRCADCR	285
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0136h	Timer RD Trigger Control Register	TRDADCR	351, 371, 386, 400, 416
0137h	Timer RD Start Register	TRDSTR	336, 352, 372, 387, 401, 417
0138h	Timer RD Mode Register	TRDMR	336, 353, 372, 388, 401, 417
0139h	Timer RD PWM Mode Register	TRDPMR	337, 354, 373
013Ah	Timer RD Function Control Register	TRDFCR	337, 354, 373, 388, 402, 418
013Bh	Timer RD Output Master Enable Register 1	TRDOER1	355, 374, 389, 403, 419
013Ch	Timer RD Output Master Enable Register 2	TRDOER2	355, 374, 389, 403, 419
013Dh	Timer RD Output Control Register	TRDOCR	356, 375, 420
013Eh	Timer RD Digital Filter Function Select Register 0	TRDDF0	338
013Fh	Timer RD Digital Filter Function Select Register 1	TRDDF1	338
0140h	Timer RD Control Register 0	TRDCR0	339, 357, 375, 390, 404, 421
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0149h			
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014Bh			
014Ch	Timer RD General Register C0	TRDGRC0	344, 362, 378, 393, 424
014Dh			
014Eh	Timer RD General Register D0	TRDGRD0	344, 362, 378, 393, 407, 424
014Fh			
0150h	Timer RD Control Register 1	TRDCR1	339, 357, 375, 404
0151h	Timer RD I/O Control Register A1	TRDIORA1	340, 358
0152h	Timer RD I/O Control Register C1	TRDIORC1	341, 359
0153h	Timer RD Status Register 1	TRDSR1	342, 360, 376, 391, 405, 422
0154h	Timer RD Interrupt Enable Register 1	TRDIER1	343, 361, 377, 392, 406, 423
0155h	Timer RD PWM Mode Output Level Control Register 1	TRDPOCR1	377
0156h	Timer RD Counter 1	TRD1	343, 361, 378, 407
0157h			
0158h	Timer RD General Register A1	TRDGRA1	344, 362, 378, 393, 407, 424
0159h			
015Ah	Timer RD General Register B1	TRDGRB1	344, 362, 378, 393, 407, 424
015Bh			
015Ch	Timer RD General Register C1	TRDGRC1	344, 362, 378, 393, 407, 424
015Dh			
015Eh	Timer RD General Register D1	TRDGRD1	344, 362, 378, 393, 407, 424
015Fh			

Address	Register	Symbol	Page
0160h	UART1 Transmit/Receive Mode Register	U1MR	493
0161h	UART1 Bit Rate Register	U1BRG	493
0162h	UART1 Transmit Buffer Register	U1TB	494
0163h			
0164h	UART1 Transmit/Receive Control Register 0	U1C0	495
0165h	UART1 Transmit/Receive Control Register 1	U1C1	495
0166h	UART1 Receive Buffer Register	U1RB	496
0167h			
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h	Timer RG Mode Register	TRGMR	460
0171h	Timer RG Count Control Register	TRGCNTC	461
0172h	Timer RG Control Register	TRGCR	462, 486
0173h	Timer RG Interrupt Enable Register	TRGIER	463
0174h	Timer RG Status Register	TRGSR	464
0175h	Timer RG I/O Control Register	TRGIOR	465, 474, 478
0176h	Timer RG Counter	TRG	466
0177h			
0178h	Timer RG General Register A	TRGGRA	467
0179h			
017Ah	Timer RG General Register B	TRGGRB	467
017Bh			
017Ch	Timer RG General Register C	TRGGRC	467
017Dh			
017Eh	Timer RG General Register D	TRGGRD	467
017Fh			
0180h	Timer RA Pin Select Register	TRASR	97, 242
0181h	Timer RB/RC Pin Select Register	TRBRCSR	98, 260, 286
0182h	Timer RC Pin Select Register 0	TRCPSR0	98, 286
0183h	Timer RC Pin Select Register 1	TRCPSR1	99, 287
0184h	Timer RD Pin Select Register 0	TRDPSR0	99, 345, 363, 379, 394, 409, 426
0185h	Timer RD Pin Select Register 1	TRDPSR1	100, 345, 363, 379, 394, 409, 426
0186h	Timer Pin Select Register	TIMSR	100, 442, 450, 467
0187h	Timer RF Output Control Register	TRFOUT	101, 449
0188h	UART0 Pin Select Register	U0SR	101, 497
0189h	UART1 Pin Select Register	U1SR	102, 497
018Ah	UART2 Pin Select Register 0	U2SR0	102, 523
018Bh	UART2 Pin Select Register 1	U2SR1	103, 523
018Ch	SSU Pin Select Register	SSUIICSR	103, 564
018Dh			
018Eh	INT Interrupt Input Pin Select Register	INTSR	104, 186
018Fh	I/O Function Pin Select Register	PINSR	105

Note:
1. The blank regions are reserved. Do not access locations in these regions.

Address	Register	Symbol	Page
0190h			
0191h			
0192h			
0193h	SS Bit Counter Register	SSBR	565
0194h	SS Transmit Data Register	SSTDR	565
0195h			
0196h	SS Receive Data Register	SSRDR	566
0197h			
0198h	SS Control Register H	SSCRH	566
0199h	SS Control Register L	SSCRL	567
019Ah	SS Mode Register	SSMR	568
019Bh	SS Enable Register	SSER	569
019Ch	SS Status Register	SSSR	570
019Dh	SS Mode Register 2	SSMR2	571
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	694
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	696
01B5h	Flash Memory Control Register 1	FMR1	699, 701
01B6h	Flash Memory Control Register 2	FMR2	702, 704
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			
01C0h	Address Match Interrupt Register 0	RMAD0	193
01C1h			
01C2h			
01C3h	Address Match Interrupt Enable Register 0	AIER0	193
01C4h	Address Match Interrupt Register 1	RMAD1	193
01C5h			
01C6h			
01C7h	Address Match Interrupt Enable Register 1	AIER1	193
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			

Address	Register	Symbol	Page
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	Pull-Up Control Register 0	PUR0	106
01E1h	Pull-Up Control Register 1	PUR1	107
01E2h	Pull-Up Control Register 2	PUR2	107
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h			
01F1h			
01F2h			
01F3h			
01F4h			
01F5h	Input Threshold Control Register 0	VLT0	108
01F6h	Input Threshold Control Register 1	VLT1	109
01F7h	Input Threshold Control Register 2	VLT2	110
01F8h			
01F9h			
01FAh	External Input Enable Register 0	INTEN	187
01FBh	External Input Enable Register 1	INTEN1	187
01FCh	INT Input Filter Select Register 0	INTF	188
01FDh	INT Input Filter Select Register 1	INTF1	188
01FEh	Key Input Enable Register 0	KIEN	191
01FFh			

Note:

1. The blank regions are reserved. Do not access locations in these regions.

Address	Register	Symbol	Page
2C00h	DTC Transfer Vector Area		
2C01h	DTC Transfer Vector Area		
2C02h	DTC Transfer Vector Area		
2C03h	DTC Transfer Vector Area		
2C04h	DTC Transfer Vector Area		
2C05h			
2C06h			
2C07h			
2C08h	DTC Transfer Vector Area		
2C09h	DTC Transfer Vector Area		
2C0Ah	DTC Transfer Vector Area		
:	DTC Transfer Vector Area		
:	DTC Transfer Vector Area		
2C3Ah			
2C3Bh			
2C3Ch			
2C3Dh			
2C3Eh			
2C3Fh			
2C40h	DTC Control Data 0	DTCD0	
2C41h			
2C42h			
2C43h			
2C44h			
2C45h			
2C46h			
2C47h			
2C48h	DTC Control Data 1	DTCD1	
2C49h			
2C4Ah			
2C4Bh			
2C4Ch			
2C4Dh			
2C4Eh			
2C4Fh			
2C50h	DTC Control Data 2	DTCD2	
2C51h			
2C52h			
2C53h			
2C54h			
2C55h			
2C56h			
2C57h			
2C58h	DTC Control Data 3	DTCD3	
2C59h			
2C5Ah			
2C5Bh			
2C5Ch			
2C5Dh			
2C5Eh			
2C5Fh			
2C60h	DTC Control Data 4	DTCD4	
2C61h			
2C62h			
2C63h			
2C64h			
2C65h			
2C66h			
2C67h			
2C68h	DTC Control Data 5	DTCD5	
2C69h			
2C6Ah			
2C6Bh			
2C6Ch			
2C6Dh			
2C6Eh			
2C6Fh			

Address	Register	Symbol	Page
2C70h	DTC Control Data 6	DTCD6	
2C71h			
2C72h			
2C73h			
2C74h			
2C75h			
2C76h			
2C77h			
2C78h	DTC Control Data 7	DTCD7	
2C79h			
2C7Ah			
2C7Bh			
2C7Ch			
2C7Dh			
2C7Eh			
2C7Fh			
2C80h	DTC Control Data 8	DTCD8	
2C81h			
2C82h			
2C83h			
2C84h			
2C85h			
2C86h			
2C87h			
2C88h	DTC Control Data 9	DTCD9	
2C89h			
2C8Ah			
2C8Bh			
2C8Ch			
2C8Dh			
2C8Eh			
2C8Fh			
2C90h	DTC Control Data 10	DTCD10	
2C91h			
2C92h			
2C93h			
2C94h			
2C95h			
2C96h			
2C97h			
2C98h	DTC Control Data 11	DTCD11	
2C99h			
2C9Ah			
2C9Bh			
2C9Ch			
2C9Dh			
2C9Eh			
2C9Fh			
2CA0h	DTC Control Data 12	DTCD12	
2CA1h			
2CA2h			
2CA3h			
2CA4h			
2CA5h			
2CA6h			
2CA7h			
2CA8h	DTC Control Data 13	DTCD13	
2CA9h			
2CAAh			
2CABh			
2CACh			
2CADh			
2CAEh			
2CAFh			

Address	Register	Symbol	Page
2CB0h	DTC Control Data 14	DTCD14	
2CB1h			
2CB2h			
2CB3h			
2CB4h			
2CB5h			
2CB6h			
2CB7h			
2CB8h	DTC Control Data 15	DTCD15	
2CB9h			
2CBAh			
2CBBh			
2CBCh			
2CBDh			
2CBEh			
2CBFh			
2CC0h	DTC Control Data 16	DTCD16	
2CC1h			
2CC2h			
2CC3h			
2CC4h			
2CC5h			
2CC6h			
2CC7h			
2CC8h	DTC Control Data 17	DTCD17	
2CC9h			
2CCAh			
2CCBh			
2CCCh			
2CCDh			
2CCEh			
2CCFh			
2CD0h	DTC Control Data 18	DTCD18	
2CD1h			
2CD2h			
2CD3h			
2CD4h			
2CD5h			
2CD6h			
2CD7h			
2CD8h	DTC Control Data 19	DTCD19	
2CD9h			
2CDAh			
2CDBh			
2CDCh			
2CDDh			
2CDEh			
2CDFh			
2CE0h	DTC Control Data 20	DTCD20	
2CE1h			
2CE2h			
2CE3h			
2CE4h			
2CE5h			
2CE6h			
2CE7h			
2CE8h	DTC Control Data 21	DTCD21	
2CE9h			
2CEAh			
2CEBh			
2CECh			
2CEDh			
2CEEh			
2CEFh			

Note:
1. The blank regions are reserved. Do not access locations in these regions.

Address	Register	Symbol	Page
2CF0h	DTC Control Data 22	DTCD22	
2CF1h			
2CF2h			
2CF3h			
2CF4h			
2CF5h			
2CF6h			
2CF7h			
2CF8h	DTC Control Data 23	DTCD23	
2CF9h			
2CFAh			
2CFBh			
2CFCh			
2CFDh			
2CFEh			
2CFFh			
2D00h			
2D01h			
:			
2E00h	CAN0 Mailbox 0: Message ID	C0MB0	619
2E01h			
2E02h			
2E03h			
2E04h			
2E05h	CAN0 Mailbox 0: Data length		
2E06h	CAN0 Mailbox 0: Data field		
2E07h			
2E08h			
2E09h			
2E0Ah			
2E0Bh			
2E0Ch			
2E0Dh			
2E0Eh	CAN0 Mailbox 0: Time stamp		
2E0Fh			
2E10h	CAN0 Mailbox 1: Message ID	C0MB1	619
2E11h			
2E12h			
2E13h			
2E14h			
2E15h	CAN0 Mailbox 1: Data length		
2E16h	CAN0 Mailbox 1: Data field		
2E17h			
2E18h			
2E19h			
2E1Ah			
2E1Bh			
2E1Ch			
2E1Dh			
2E1Eh	CAN0 Mailbox 0: Time stamp		
2E1Fh			
2E20h	CAN0 Mailbox 2: Message ID	C0MB2	619
2E21h			
2E22h			
2E23h			
2E24h			
2E25h	CAN0 Mailbox 2: Data length		
2E26h	CAN0 Mailbox 2: Data field		
2E27h			
2E28h			
2E29h			
2E2Ah			
2E2Bh			
2E2Ch			
2E2Dh			
2E2Eh	CAN0 Mailbox 2: Time stamp		
2E2Fh			

Address	Register	Symbol	Page
2E30h	CAN0 Mailbox 3: Message ID	C0MB3	619
2E31h			
2E32h			
2E33h			
2E34h			
2E35h	CAN0 Mailbox 3: Data length		
2E36h	CAN0 Mailbox 3: Data field		
2E37h			
2E38h			
2E39h			
2E3Ah			
2E3Bh			
2E3Ch			
2E3Dh			
2E3Eh	CAN0 Mailbox 3: Time stamp		
2E3Fh			
2E40h	CAN0 Mailbox 4: Message ID	C0MB4	619
2E41h			
2E42h			
2E43h			
2E44h			
2E45h	CAN0 Mailbox 4: Data length		
2E46h	CAN0 Mailbox 4: Data field		
2E47h			
2E48h			
2E49h			
2E4Ah			
2E4Bh			
2E4Ch			
2E4Dh			
2E4Eh	CAN0 Mailbox 4: Time stamp		
2E4Fh			
2E50h	CAN0 Mailbox 5: Message ID	C0MB5	619
2E51h			
2E52h			
2E53h			
2E54h			
2E55h	CAN0 Mailbox 5: Data length		
2E56h	CAN0 Mailbox 5: Data field		
2E57h			
2E58h			
2E59h			
2E5Ah			
2E5Bh			
2E5Ch			
2E5Dh			
2E5Eh	CAN0 Mailbox 5: Time stamp		
2E5Fh			
2E60h	CAN0 Mailbox 6: Message ID	C0MB6	619
2E61h			
2E62h			
2E63h			
2E64h			
2E65h	CAN0 Mailbox 6: Data length		
2E66h	CAN0 Mailbox 6: Data field		
2E67h			
2E68h			
2E69h			
2E6Ah			
2E6Bh			
2E6Ch			
2E6Dh			
2E6Eh	CAN0 Mailbox 6: Time stamp		
2E6Fh			

Note:
1. The blank regions are reserved. Do not access locations in these regions.

Address	Register	Symbol	Page
2E70h	CAN0 Mailbox 7: Message ID	C0MB7	619
2E71h			
2E72h			
2E73h			
2E74h			
2E75h	CAN0 Mailbox 7: Data length		
2E76h	CAN0 Mailbox 7: Data field		
2E77h			
2E78h			
2E79h			
2E7Ah			
2E7Bh			
2E7Ch			
2E7Dh			
2E7Eh	CAN0 Mailbox 7: Time stamp		
2E7Fh			
2E80h	CAN0 Mailbox 8: Message ID	C0MB8	619
2E81h			
2E82h			
2E83h			
2E84h			
2E85h	CAN0 Mailbox 8: Data length		
2E86h	CAN0 Mailbox 8: Data field		
2E87h			
2E88h			
2E89h			
2E8Ah			
2E8Bh			
2E8Ch			
2E8Dh			
2E8Eh	CAN0 Mailbox 8: Time stamp		
2E8Fh			
2E90h	CAN0 Mailbox 9: Message ID	C0MB9	619
2E91h			
2E92h			
2E93h			
2E94h			
2E95h	CAN0 Mailbox 9: Data length		
2E96h	CAN0 Mailbox 9: Data field		
2E97h			
2E98h			
2E99h			
2E9Ah			
2E9Bh			
2E9Ch			
2E9Dh			
2E9Eh	CAN0 Mailbox 9: Time stamp		
2E9Fh			
2EA0h	CAN0 Mailbox 10: Message ID	C0MB10	619
2EA1h			
2EA2h			
2EA3h			
2EA4h			
2EA5h	CAN0 Mailbox 10: Data length		
2EA6h	CAN0 Mailbox 10: Data field		
2EA7h			
2EA8h			
2EA9h			
2EAAh			
2EABh			
2EACh			
2EADh			
2EAEh	CAN0 Mailbox 10: Time stamp		
2EAFh			

Address	Register	Symbol	Page
2EB0h	CAN0 Mailbox 11: Message ID	C0MB11	619
2EB1h			
2EB2h			
2EB3h			
2EB4h			
2EB5h	CAN0 Mailbox 11: Data length		
2EB6h	CAN0 Mailbox 11: Data field		
2EB7h			
2EB8h			
2EB9h			
2EBAh			
2EBBh			
2EBCh			
2EBDh			
2EBEh	CAN0 Mailbox 11: Time stamp		
2EBFh			
2EC0h	CAN0 Mailbox 12: Message ID	C0MB12	619
2EC1h			
2EC2h			
2EC3h			
2EC4h			
2EC5h	CAN0 Mailbox 12: Data length		
2EC6h	CAN0 Mailbox 12: Data field		
2EC7h			
2EC8h			
2EC9h			
2ECAh			
2ECBh			
2ECCh			
2ECDh			
2ECEh	CAN0 Mailbox 12: Time stamp		
2ECFh			
2ED0h	CAN0 Mailbox 13: Message ID	C0MB13	619
2ED1h			
2ED2h			
2ED3h			
2ED4h			
2ED5h	CAN0 Mailbox 13: Data length		
2ED6h	CAN0 Mailbox 13: Data field		
2ED7h			
2ED8h			
2ED9h			
2EDAh			
2EDBh			
2EDCh			
2EDDh			
2EDEh	CAN0 Mailbox 13: Time stamp		
2EDFh			
2EE0h	CAN0 Mailbox 14: Message ID	C0MB14	619
2EE1h			
2EE2h			
2EE3h			
2EE4h			
2EE5h	CAN0 Mailbox 14: Data length		
2EE6h	CAN0 Mailbox 14: Data field		
2EE7h			
2EE8h			
2EE9h			
2EEAh			
2EEBh			
2EECh			
2EEDh			
2EEEh	CAN0 Mailbox 14: Time stamp		
2EEFh			

Note:

1. The blank regions are reserved. Do not access locations in these regions.

Address	Register	Symbol	Page
2EF0h	CAN0 Mailbox 15: Message ID	C0MB15	619
2EF1h			
2EF2h			
2EF3h			
2EF4h			
2EF5h	CAN0 Mailbox 15: Data length		
2EF6h	CAN0 Mailbox 15: Data field		
2EF7h			
2EF8h			
2EF9h			
2EFAh			
2EFBh			
2EFCh			
2EFDh			
2EFEh	CAN0 Mailbox 15: Time stamp		
2EFFh			
2F00h			
2F01h			
2F02h			
2F03h			
2F04h			
2F05h			
2F06h			
2F07h			
2F08h			
2F09h			
2F0Ah			
2F0Bh			
2F0Ch			
2F0Dh			
2F0Eh			
2F0Fh			
2F10h	CAN0 Mask Register 0	C0MKR0	616
2F11h			
2F12h			
2F13h			
2F14h	CAN0 Mask Register 1	C0MKR1	616
2F15h			
2F16h			
2F17h			
2F18h	CAN0 Mask Register 2	C0MKR2	616
2F19h			
2F1Ah			
2F1Bh			
2F1Ch	CAN0 Mask Register 3	C0MKR3	616
2F1Dh			
2F1Eh			
2F1Fh			
2F20h	CAN0 FIFO Received ID Compare Register 0	C0FIDCR0	617
2F21h			
2F22h			
2F23h			
2F24h	CAN0 FIFO Received ID Compare Register 1	C0FIDCR1	617
2F25h			
2F26h			
2F27h			
2F28h			
2F29h			
2F2Ah	CAN0 Mask Invalid Register	C0MKIVLR	618
2F2Bh			
2F2Ch			
2F2Dh			
2F2Eh	CAN0 Mailbox Interrupt Enable Register	C0MIER	623
2F2Fh			

Note:
1. The blank regions are reserved. Do not access locations in these regions.

Address	Register	Symbol	Page
2F30h	CAN0 Message Control Register 0	C0MCTL0	624
2F31h	CAN0 Message Control Register 1	C0MCTL1	624
2F32h	CAN0 Message Control Register 2	C0MCTL2	624
2F33h	CAN0 Message Control Register 3	C0MCTL3	624
2F34h	CAN0 Message Control Register 4	C0MCTL4	624
2F35h	CAN0 Message Control Register 5	C0MCTL5	624
2F36h	CAN0 Message Control Register 6	C0MCTL6	624
2F37h	CAN0 Message Control Register 7	C0MCTL7	624
2F38h	CAN0 Message Control Register 8	C0MCTL8	624
2F39h	CAN0 Message Control Register 9	C0MCTL9	624
2F3Ah	CAN0 Message Control Register 10	C0MCTL10	624
2F3Bh	CAN0 Message Control Register 11	C0MCTL11	624
2F3Ch	CAN0 Message Control Register 12	C0MCTL12	624
2F3Dh	CAN0 Message Control Register 13	C0MCTL13	624
2F3Eh	CAN0 Message Control Register 14	C0MCTL14	624
2F3Fh	CAN0 Message Control Register 15	C0MCTL15	624
2F40h	CAN0 Control Register	C0CTLR	610
2F41h			
2F42h	CAN0 Status Register	C0STR	632
2F43h			
2F44h	CAN0 Bit Configuration Register	C0BCR	614
2F45h			
2F46h			
2F47h			
2F48h	CAN0 Receive FIFO Control Register	C0RFCR	627
2F49h	CAN0 Receive FIFO Pointer Control Register	C0RFPCR	629
2F4Ah	CAN0 Transmit FIFO Control Register	C0TFCR	630
2F4Bh	CAN0 Transmit FIFO Pointer Control Register	C0TFPCR	631
2F4Ch	CAN0 Error Interrupt Enable Register	C0EIER	639
2F4Dh	CAN0 Error Interrupt Factor Judge Register	C0EIFR	641
2F4Eh	CAN0 Reception Error Count Register	C0RECR	643
2F4Fh	CAN0 Transmission Error Count Register	C0TECR	643
2F50h	CAN0 Error Code Store Register	C0ECSR	644
2F51h	CAN0 Channel Search Support Register	C0CSSR	637
2F52h	CAN0 Mailbox Search Status Register	C0MSSR	636
2F53h	CAN0 Mailbox Search Mode Register	C0MSMR	635
2F54h	CAN0 Time Stamp Register	C0TSR	646
2F55h			
2F56h	CAN0 Acceptance Filter Support Register	C0AFSR	638
2F57h			
2F58h	CAN0 Test Control Register	C0TCR	647
:			
FFDBh	Option Function Select Register 2	OFS2	48, 205, 212
:			
FFFFh	Option Function Select Register	OFS	47, 66, 204, 211, 692

1. Overview

1.1 Features

The R8C/38W Group, R8C/38X Group, R8C/38Y Group, and R8C/38Z Group of single-chip MCUs incorporate the R8C CPU core, employing sophisticated instructions for a high level of efficiency. With 1 Mbyte of address space, and it is capable of executing instructions at high speed. In addition, the CPU core boasts a multiplier for high-speed operation processing.
Power consumption is low, and the supported operating modes allow additional power control. These MCUs are designed to maximize EMI/EMS performance.
Integration of many peripheral functions, including multifunction timer and serial interface, reduces the number of system components.
The R8C/38W Group and R8C/38X Group have a single channel CAN module and are suitable for LAN systems in vehicles and for FA.
The R8C/38Y Group and R8C/38Z Group do not have CAN modules.
The R8C/38W Group and R8C/38Y Group have data flash (1 KB × 4 blocks) with the background operation (BGO) function.

1.1.1 Applications

Automobiles and others

1.1.2 Specifications

Tables 1.1 and 1.2 outline the Specifications for R8C/38W Group, tables 1.3 and 1.4 outline the Specifications for R8C/38X Group, tables 1.5 and 1.6 outline the Specifications for R8C/38Y Group, and tables 1.7 and 1.8 outline the Specifications for R8C/38Z Group.

Table 1.1 Specifications for R8C/38W Group (1)

Item	Function	Specification
CPU	Central processing unit	R8C CPU core • Number of fundamental instructions: 89 • Minimum instruction execution time: 50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operating mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM, Data flash	Refer to **Table 1.9 Product List for R8C/38W Group**.
Power Supply Voltage Detection	Voltage detection circuit	• Power-on reset • Voltage detection 3 (detection level of voltage detection 1 selectable)
I/O Ports	Programmable I/O ports	• Input-only: 1 pin • CMOS I/O ports: 75, selectable pull-up resistor
Clock	Clock generation circuits	3 circuits: XIN clock oscillation circuit (with on-chip feedback resistor), High-speed on-chip oscillator (with frequency adjustment function), Low-speed on-chip oscillator • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: Standard operating mode (high-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
Interrupts		• Interrupt vectors: 69 • External: 9 sources ($\overline{\text{INT}}$ × 5, key input × 4) • Priority levels: 7 levels
Watchdog Timer		• 14 bits × 1 (with prescaler) • Reset start selectable • Low-speed on-chip oscillator for watchdog timer selectable
DTC (Data Transfer Controller)		• 1 channel • Activation sources: 40 • Transfer modes: 2 (normal mode, repeat mode)

Table 1.2 Specifications for R8C/38W Group (2)

Item	Function	Specification
Timer	Timer RA0	8 bits (with 8-bit prescaler) × 1 Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RA1	8 bits (with 8-bit prescaler) × 1 Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits (with 8-bit prescaler) × 1 Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits (with 4 capture/compare registers) × 1 Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
	Timer RD	16 bits (with 4 capture/compare registers) × 2 Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period)
	Timer RE	8 bits × 1 Output compare mode
	Timer RF	16 bits × 1 Input capture mode (input capture circuit), output compare mode (output compare circuit)
	Timer RG	16 bits × 1 Timer mode (input capture function, output compare function), PWM mode (output 1 pin), phase counting mode (available automatic measurement for the counts of 2-phase encoder)
Serial Interface	UART0, 1	2 channels Clock synchronous serial I/O, UART
	UART2	1 channel Clock synchronous serial I/O, UART, I^2C mode (I^2C-bus), IE mode (IEbus), multiprocessor communication function
Synchronous Serial Communication Unit (SSU)		1 channel
LIN Module		Hardware LIN: 2 (timer RA0, timer RA1, UART0, UART1)
CAN Module		1 channel, 16 Mailboxes (conforms to the ISO 11898-1)
A/D Converter		10-bit resolution × 20 channels, includes sample and hold function, with sweep mode
Flash Memory		• Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function • Background operation (BGO) function (data flash)
Operating Frequency/Supply Voltage		f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V)
Current Consumption		Typ. 7 mA (VCC = 5.0 V, f(XIN) = 20 MHz)
Operating Ambient Temperature		-40 to 85°C (J version) -40 to 125°C (K version) (1)
Package		80-pin LQFP Package code: PLQP0080KB-A (previous code: 80P6Q-A)

Note:
1. Specify the K version if K version functions are to be used.

Table 1.3 Specifications for R8C/38X Group (1)

Item	Function	Specification
CPU	Central processing unit	R8C CPU core • Number of fundamental instructions: 89 • Minimum instruction execution time: 50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operating mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM, Data flash	Refer to **Table 1.10 Product List for R8C/38X Group**.
Power Supply Voltage Detection	Voltage detection circuit	• Power-on reset • Voltage detection 3 (detection level of voltage detection 1 selectable)
I/O Ports	Programmable I/O ports	• Input-only: 1 pin • CMOS I/O ports: 75, selectable pull-up resistor
Clock	Clock generation circuits	3 circuits: XIN clock oscillation circuit (with on-chip feedback resistor), High-speed on-chip oscillator (with frequency adjustment function), Low-speed on-chip oscillator • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: Standard operating mode (high-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
Interrupts		• Interrupt vectors: 69 • External: 9 sources ($\overline{\text{INT}}$ × 5, key input × 4) • Priority levels: 7 levels
Watchdog Timer		• 14 bits × 1 (with prescaler) • Reset start selectable • Low-speed on-chip oscillator for watchdog timer selectable
DTC (Data Transfer Controller)		• 1 channel • Activation sources: 40 • Transfer modes: 2 (normal mode, repeat mode)

Table 1.4 Specifications for R8C/38X Group (2)

Item	Function	Specification
Timer	Timer RA0	8 bits (with 8-bit prescaler) × 1 Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RA1	8 bits (with 8-bit prescaler) × 1 Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits (with 8-bit prescaler) × 1 Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits (with 4 capture/compare registers) × 1 Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
	Timer RD	16 bits (with 4 capture/compare registers) × 2 Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period)
	Timer RE	8 bits × 1 Output compare mode
	Timer RF	16 bits × 1 Input capture mode (input capture circuit), output compare mode (output compare circuit)
	Timer RG	16 bits × 1 Timer mode (input capture function, output compare function), PWM mode (output 1 pin), phase counting mode (available automatic measurement for the counts of 2-phase encoder)
Serial Interface	UART0, 1	2 channels Clock synchronous serial I/O, UART
	UART2	1 channel Clock synchronous serial I/O, UART, I^2C mode (I^2C-bus), IE mode (IEbus), multiprocessor communication function
Synchronous Serial Communication Unit (SSU)		1 channel
LIN Module		Hardware LIN: 2 (timer RA0, timer RA1, UART0, UART1)
CAN Module		1 channel, 16 Mailboxes (conforms to the ISO 11898-1)
A/D Converter		10-bit resolution × 20 channels, includes sample and hold function, with sweep mode
Flash Memory		• Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 100 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function
Operating Frequency/Supply Voltage		f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V)
Current Consumption		Typ. 7 mA (VCC = 5.0 V, f(XIN) = 20 MHz)
Operating Ambient Temperature		-40 to 85°C (J version) -40 to 125°C (K version) (1)
Package		80-pin LQFP Package code: PLQP0080KB-A (previous code: 80P6Q-A)

Note:
1. Specify the K version if K version functions are to be used.

Table 1.5 Specifications for R8C/38Y Group (1)

Item	Function	Specification
CPU	Central processing unit	R8C CPU core • Number of fundamental instructions: 89 • Minimum instruction execution time: 50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operating mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM, Data flash	Refer to **Table 1.11 Product List for R8C/38Y Group**.
Power Supply Voltage Detection	Voltage detection circuit	• Power-on reset • Voltage detection 3 (detection level of voltage detection 1 selectable)
I/O Ports	Programmable I/O ports	• Input-only: 1 pin • CMOS I/O ports: 75, selectable pull-up resistor
Clock	Clock generation circuits	3 circuits: XIN clock oscillation circuit (with on-chip feedback resistor), High-speed on-chip oscillator (with frequency adjustment function), Low-speed on-chip oscillator • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: Standard operating mode (high-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
Interrupts		• Interrupt vectors: 69 • External: 9 sources ($\overline{\text{INT}}$ × 5, key input × 4) • Priority levels: 7 levels
Watchdog Timer		• 14 bits × 1 (with prescaler) • Reset start selectable • Low-speed on-chip oscillator for watchdog timer selectable
DTC (Data Transfer Controller)		• 1 channel • Activation sources: 40 • Transfer modes: 2 (normal mode, repeat mode)

Table 1.6 Specifications for R8C/38Y Group (2)

Item	Function	Specification
Timer	Timer RA0	8 bits (with 8-bit prescaler) × 1 Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RA1	8 bits (with 8-bit prescaler) × 1 Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits (with 8-bit prescaler) × 1 Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits (with 4 capture/compare registers) × 1 Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
	Timer RD	16 bits (with 4 capture/compare registers) × 2 Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period)
	Timer RE	8 bits × 1 Output compare mode
	Timer RF	16 bits × 1 Input capture mode (input capture circuit), output compare mode (output compare circuit)
	Timer RG	16 bits × 1 Timer mode (input capture function, output compare function), PWM mode (output 1 pin), phase counting mode (available automatic measurement for the counts of 2-phase encoder)
Serial Interface	UART0, 1	2 channels Clock synchronous serial I/O, UART
	UART2	1 channel Clock synchronous serial I/O, UART, I^2C mode (I^2C-bus), IE mode (IEbus), multiprocessor communication function
Synchronous Serial Communication Unit (SSU)		1 channel
LIN Module		Hardware LIN: 2 (timer RA0, timer RA1, UART0, UART1)
A/D Converter		10-bit resolution × 20 channels, includes sample and hold function, with sweep mode
Flash Memory		• Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function • Background operation (BGO) function (data flash)
Operating Frequency/Supply Voltage		f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V)
Current Consumption		Typ. 7 mA (VCC = 5.0 V, f(XIN) = 20 MHz)
Operating Ambient Temperature		-40 to 85°C (J version) -40 to 125°C (K version) (1)
Package		80-pin LQFP Package code: PLQP0080KB-A (previous code: 80P6Q-A)

Note:
1. Specify the K version if K version functions are to be used.

Table 1.7 Specifications for R8C/38Z Group (1)

Item	Function	Specification
CPU	Central processing unit	R8C CPU core • Number of fundamental instructions: 89 • Minimum instruction execution time: 50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operating mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM, Data flash	Refer to **Table 1.12 Product List for R8C/38Z Group**.
Power Supply Voltage Detection	Voltage detection circuit	• Power-on reset • Voltage detection 3 (detection level of voltage detection 1 selectable)
I/O Ports	Programmable I/O ports	• Input-only: 1 pin • CMOS I/O ports: 75, selectable pull-up resistor
Clock	Clock generation circuits	3 circuits: XIN clock oscillation circuit (with on-chip feedback resistor), High-speed on-chip oscillator (with frequency adjustment function), Low-speed on-chip oscillator • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: Standard operating mode (high-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
Interrupts		• Interrupt vectors: 69 • External: 9 sources ($\overline{\text{INT}}$ × 5, key input × 4) • Priority levels: 7 levels
Watchdog Timer		• 14 bits × 1 (with prescaler) • Reset start selectable • Low-speed on-chip oscillator for watchdog timer selectable
DTC (Data Transfer Controller)		• 1 channel • Activation sources: 40 • Transfer modes: 2 (normal mode, repeat mode)

Table 1.8 Specifications for R8C/38Z Group (2)

Item	Function	Specification
Timer	Timer RA0	8 bits (with 8-bit prescaler) × 1 Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RA1	8 bits (with 8-bit prescaler) × 1 Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits (with 8-bit prescaler) × 1 Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits (with 4 capture/compare registers) × 1 Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
	Timer RD	16 bits (with 4 capture/compare registers) × 2 Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period)
	Timer RE	8 bits × 1 Output compare mode
	Timer RF	16 bits × 1 Input capture mode (input capture circuit), output compare mode (output compare circuit)
	Timer RG	16 bits × 1 Timer mode (input capture function, output compare function), PWM mode (output 1 pin), phase counting mode (available automatic measurement for the counts of 2-phase encoder)
Serial Interface	UART0, 1	2 channels Clock synchronous serial I/O, UART
	UART2	1 channel Clock synchronous serial I/O, UART, I^2C mode (I^2C-bus), IE mode (IEbus), multiprocessor communication function
Synchronous Serial Communication Unit (SSU)		1 channel
LIN Module		Hardware LIN: 2 (timer RA0, timer RA1, UART0, UART1)
A/D Converter		10-bit resolution × 20 channels, includes sample and hold function, with sweep mode
Flash Memory		• Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 100 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function
Operating Frequency/Supply Voltage		f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V)
Current Consumption		Typ. 7 mA (VCC = 5.0 V, f(XIN) = 20 MHz)
Operating Ambient Temperature		-40 to 85°C (J version) -40 to 125°C (K version) (1)
Package		80-pin LQFP Package code: PLQP0080KB-A (previous code: 80P6Q-A)

Note:
1. Specify the K version if K version functions are to be used.

1.2 Product List

Table 1.9 lists Product List for R8C/38W Group, Table 1.10 lists Product List for R8C/38X Group, Table 1.11 lists Product List for R8C/38Y Group, and Table 1.12 lists Product List for R8C/38Z Group.

Table 1.9 Product List for R8C/38W Group **Current of Jun 2013**

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data flash			
R5F21388WJFP	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0080KB-A	J version
R5F2138AWJFP	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0080KB-A	
R5F2138CWJFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080KB-A	
R5F21388WKFP	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0080KB-A	K version
R5F2138AWKFP	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0080KB-A	
R5F2138CWKFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080KB-A	

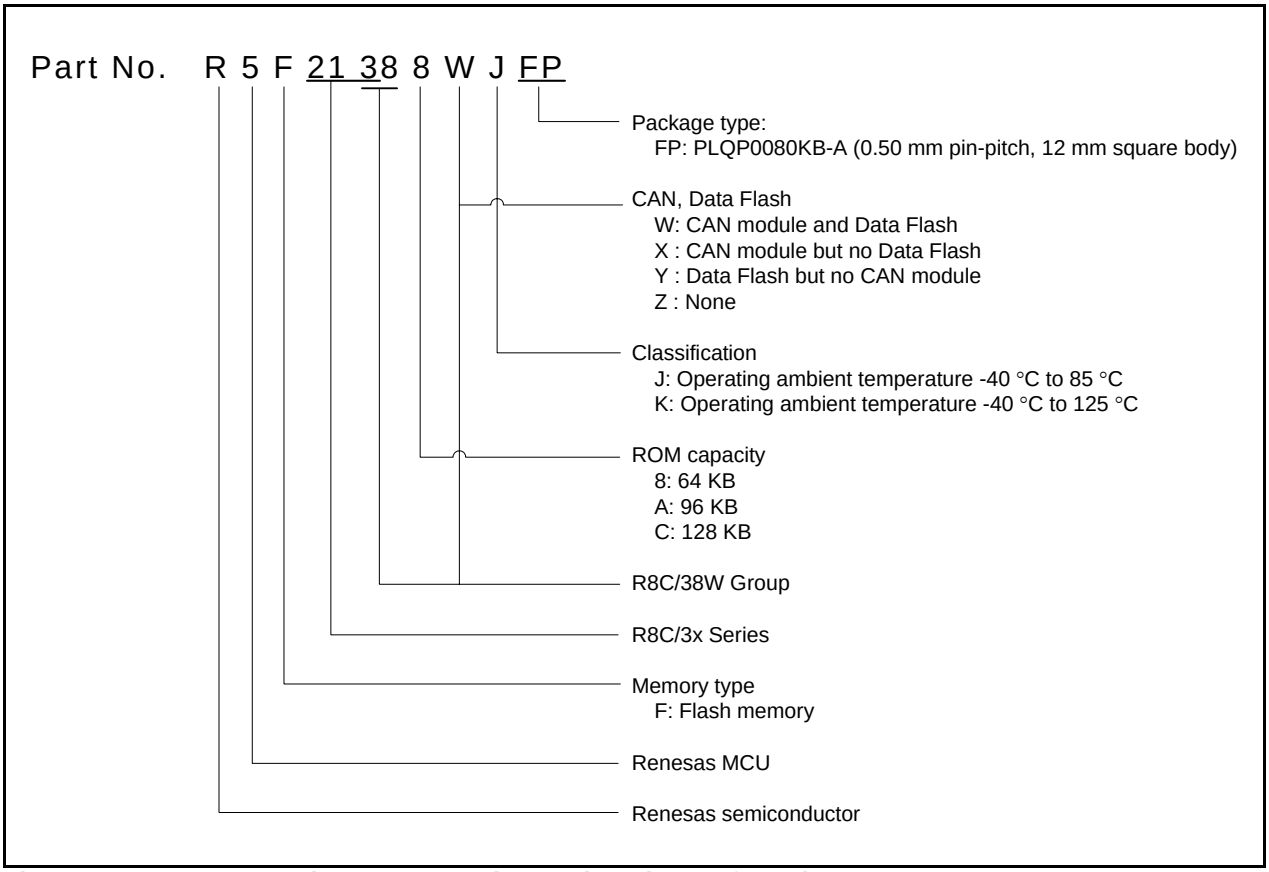


Figure 1.1 Part Number, Memory Size, and Package of R8C/38W Group

Table 1.10 Product List for R8C/38X Group **Current of Jun 2013**

Part No.	ROM Capacity Program ROM	RAM Capacity	Package Type	Remarks
R5F21388XJFP	64 Kbytes	6 Kbytes	PLQP0080KB-A	J version
R5F2138AXJFP	96 Kbytes	8 Kbytes	PLQP0080KB-A	
R5F2138CXJFP	128 Kbytes	10 Kbytes	PLQP0080KB-A	
R5F21388XKFP	64 Kbytes	6 Kbytes	PLQP0080KB-A	K version
R5F2138AXKFP	96 Kbytes	8 Kbytes	PLQP0080KB-A	
R5F2138CXKFP	128 Kbytes	10 Kbytes	PLQP0080KB-A	

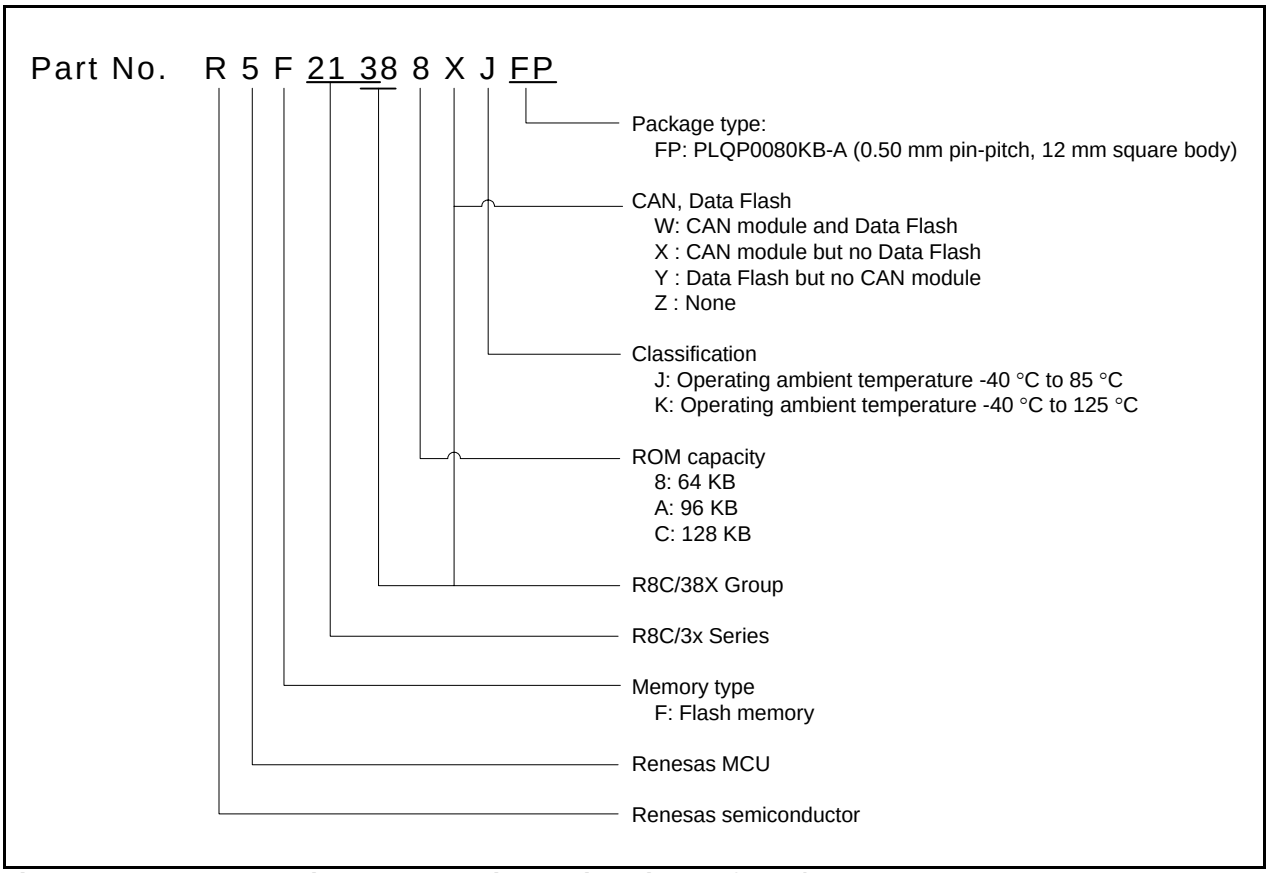


Figure 1.2 Part Number, Memory Size, and Package of R8C/38X Group

Table 1.11 Product List for R8C/38Y Group **Current of Jun 2013**

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data flash			
R5F21388YJFP	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0080KB-A	J version
R5F2138AYJFP	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0080KB-A	
R5F2138CYJFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080KB-A	
R5F21388YKFP	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0080KB-A	K version
R5F2138AYKFP	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0080KB-A	
R5F2138CYKFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080KB-A	

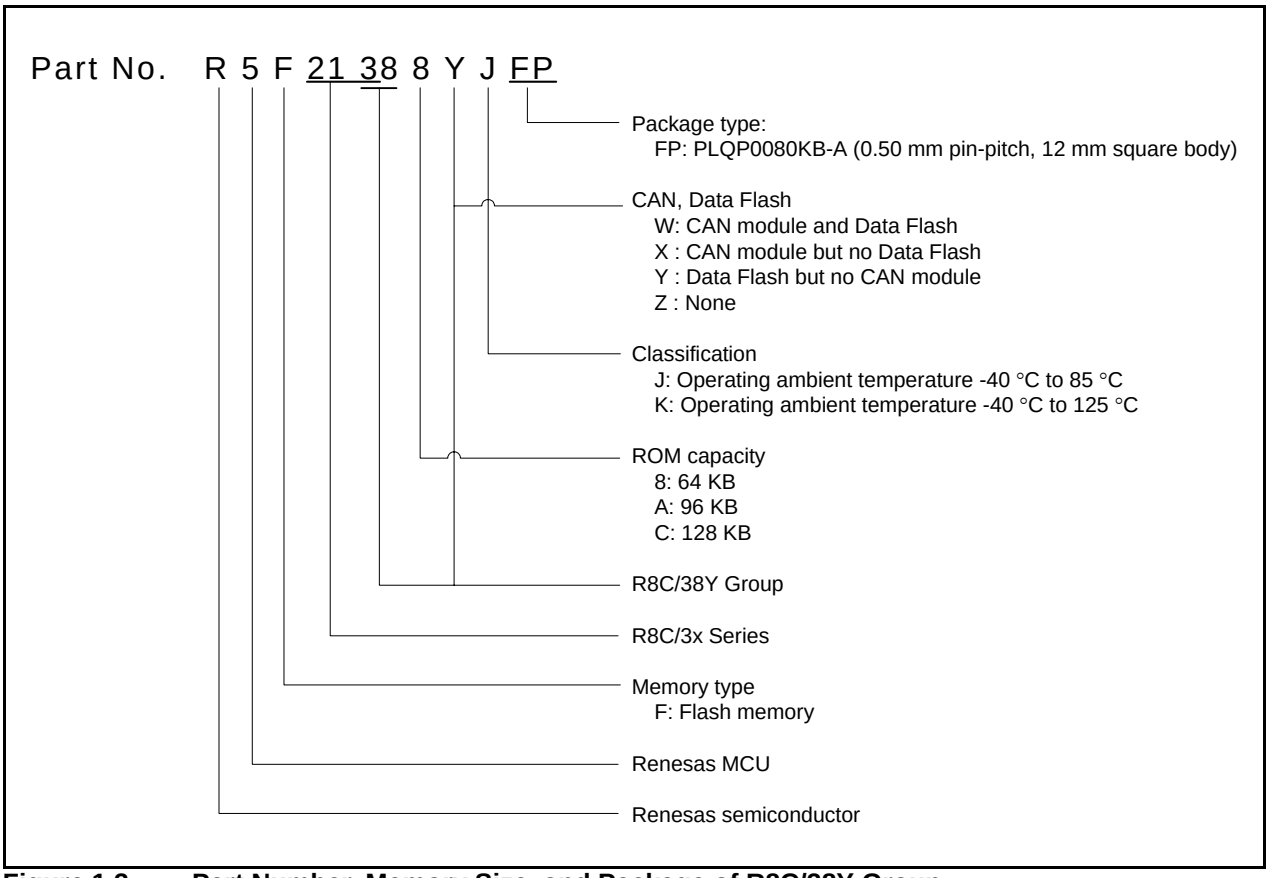


Figure 1.3 Part Number, Memory Size, and Package of R8C/38Y Group

Table 1.12 Product List for R8C/38Z Group **Current of Jun 2013**

Part No.	ROM Capacity Program ROM	RAM Capacity	Package Type	Remarks
R5F21388ZJFP	64 Kbytes	6 Kbytes	PLQP0080KB-A	J version
R5F2138AZJFP	96 Kbytes	8 Kbytes	PLQP0080KB-A	
R5F2138CZJFP	128 Kbytes	10 Kbytes	PLQP0080KB-A	
R5F21388ZKFP	64 Kbytes	6 Kbytes	PLQP0080KB-A	K version
R5F2138AZKFP	96 Kbytes	8 Kbytes	PLQP0080KB-A	
R5F2138CZKFP	128 Kbytes	10 Kbytes	PLQP0080KB-A	

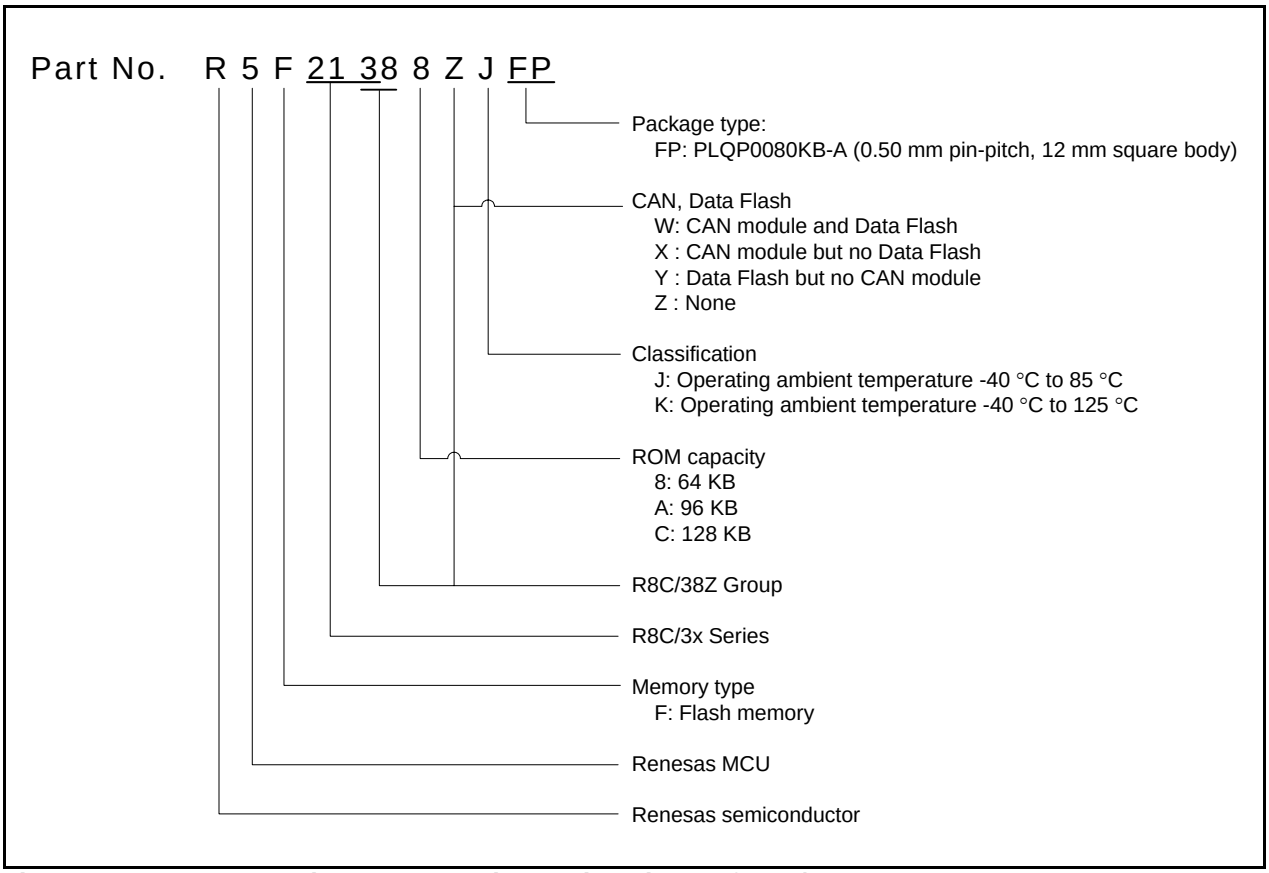


Figure 1.4 Part Number, Memory Size, and Package of R8C/38Z Group

1.3 Block Diagram

Figure 1.5 shows a Block Diagram.

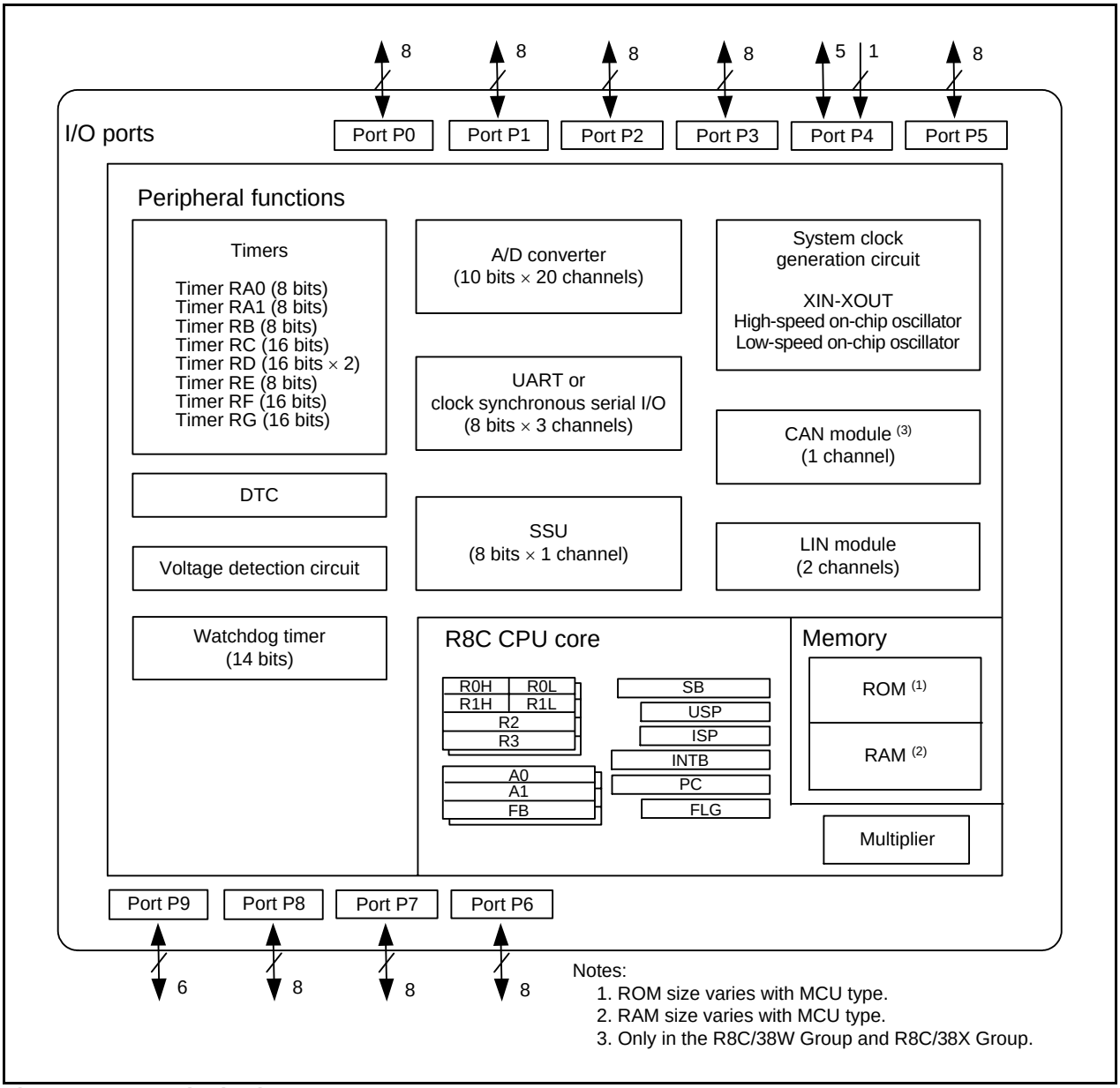
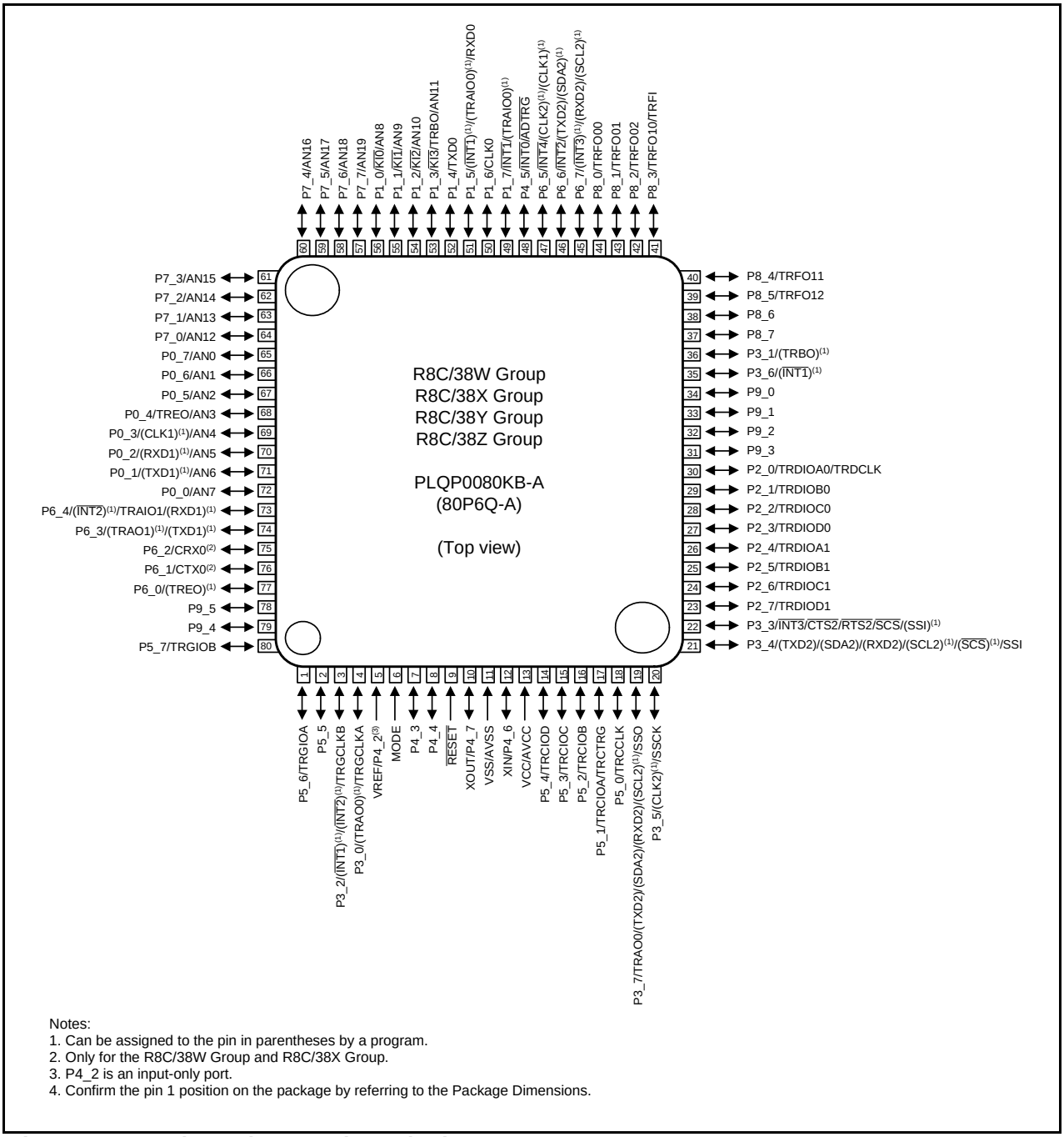


Figure 1.5 Block Diagram

1.4 Pin Assignment

Figure 1.6 shows Pin Assignment (Top View). Tables 1.13 and 1.14 outline the Pin Name Information by Pin Number.



Notes:
1. Can be assigned to the pin in parentheses by a program.
2. Only for the R8C/38W Group and R8C/38X Group.
3. P4_2 is an input-only port.
4. Confirm the pin 1 position on the package by referring to the Package Dimensions.

Figure 1.6 Pin Assignment (Top View)

Table 1.13 Pin Name Information by Pin Number (1)

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules					
			Interrupt	Timer	Serial Interface	SSU	CAN Module (2)	A/D Converter, Voltage Detection Circuit
1		P5_6		TRGIOA				
2		P5_5						
3		P3_2	(INT1) (1)/ (INT2) (1)	TRGCLKB				
4		P3_0		(TRAO0) (1)/ TRGCLKA				
5		P4_2						VREF
6	MODE							
7		P4_3						
8		P4_4						
9	RESET							
10	XOUT	P4_7						
11	VSS/AVSS							
12	XIN	P4_6						
13	VCC/ AVCC							
14		P5_4		TRCIOD				
15		P5_3		TRCIOC				
16		P5_2		TRCIOB				
17		P5_1		TRCIOA/ TRCTRG				
18		P5_0		TRCCLK				
19		P3_7		TRAO0	(TXD2)/(SDA2)/ (RXD2)/(SCL2) (1)	SSO		
20		P3_5			(CLK2) (1)	SSCK		
21		P3_4			(TXD2)/(SDA2)/ (RXD2)/(SCL2) (1)	(SCS) (1)/SSI		
22		P3_3	INT3		CTS2/RTS2	SCS/(SSI) (1)		
23		P2_7		TRDIOD1				
24		P2_6		TRDIOC1				
25		P2_5		TRDIOB1				
26		P2_4		TRDIOA1				
27		P2_3		TRDIOD0				
28		P2_2		TRDIOC0				
29		P2_1		TRDIOB0				
30		P2_0		TRDIOA0/ TRDCLK				
31		P9_3						
32		P9_2						
33		P9_1						
34		P9_0						
35		P3_6	(INT1) (1)					
36		P3_1		(TRBO) (1)				
37		P8_7						
38		P8_6						
39		P8_5		TRFO12				
40		P8_4		TRFO11				

Notes:
1. This can be assigned to the pin in parentheses by a program.
2. Only for the R8C/38W Group and R8C/38X Group.

Table 1.14 Pin Name Information by Pin Number (2)

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules					
			Interrupt	Timer	Serial Interface	SSU	CAN Module (2)	A/D Converter, Voltage Detection Circuit
41		P8_3		TRFO10/TRFI				
42		P8_2		TRFO02				
43		P8_1		TRFO01				
44		P8_0		TRFO00				
45		P6_7	(INT3) (1)		(RXD2)/ (SCL2) (1)			
46		P6_6	INT2		(TXD2)/ (SDA2) (1)			
47		P6_5	INT4		(CLK2) (1)/ (CLK1) (1)			
48		P4_5	INT0					ADTRG
49		P1_7	INT1	(TRAIO0) (1)				
50		P1_6			CLK0			
51		P1_5	(INT1) (1)	(TRAIO0) (1)	RXD0			
52		P1_4			TXD0			
53		P1_3	KI3	TRBO				AN11
54		P1_2	KI2					AN10
55		P1_1	KI1					AN9
56		P1_0	KI0					AN8
57		P7_7						AN19
58		P7_6						AN18
59		P7_5						AN17
60		P7_4						AN16
61		P7_3						AN15
62		P7_2						AN14
63		P7_1						AN13
64		P7_0						AN12
65		P0_7						AN0
66		P0_6						AN1
67		P0_5						AN2
68		P0_4		TREO				AN3
69		P0_3			(CLK1) (1)			AN4
70		P0_2			(RXD1) (1)			AN5
71		P0_1			(TXD1) (1)			AN6
72		P0_0						AN7
73		P6_4	(INT2) (1)	TRAIO1	(RXD1) (1)			
74		P6_3		(TRAO1) (1)	(TXD1) (1)			
75		P6_2					CRX0 (2)	
76		P6_1					CTX0 (2)	
77		P6_0		(TREO) (1)				
78		P9_5						
79		P9_4						
80		P5_7		TRGIOB				

Notes:
1. This can be assigned to the pin in parentheses by a program.
2. Only for the R8C/38W Group and R8C/38X Group.

1.5 Pin Functions

Tables 1.15 and 1.16 list Pin Functions.

Table 1.15 Pin Functions (1)

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS	I	Apply 2.7 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	I	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Input “L” on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins (1). To use an external clock, input it to the XOUT pin and leave the XIN pin open.
XIN clock output	XOUT	I/O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT4}}$	I	$\overline{\text{INT}}$ interrupt input pins.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input pins
Timer RA0 Timer RA1	TRAIO0, TRAIO1	I/O	Timer RA I/O pin
	TRAO0, TRAO1	O	Timer RA output pin
Timer RB	TRBO	O	Timer RB output pin
Timer RC	TRCCLK	I	External clock input pin
	TRCTRG	I	External trigger input pin
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins
Timer RD	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1	I/O	Timer RD I/O pins
	TRDCLK	I	External clock input pin
Timer RE	TREO	O	Divided clock output pin
Timer RF	TRFO00, TRFO10, TRFO01, TRFO11, TRFO02, TRFO12	O	Timer RF output pins.
	TRFI	I	Timer RF input pin.
Timer RG	TRGIOA, TRGIOB	I/O	Timer RG I/O ports.
	TRGCLKA, TRGCLKB	I	External clock input pins.
Serial interface	CLK0, CLK1, CLK2	I/O	Transfer clock I/O pins
	RXD0, RXD1, RXD2	I	Serial data input pins
	TXD0, TXD1, TXD2	O	Serial data output pins
	$\overline{\text{CTS2}}$	I	Transmission control input pin
	$\overline{\text{RTS2}}$	O	Reception control output pin
	SCL2	I/O	I^2C mode clock I/O pin
	SDA2	I/O	I^2C mode data I/O pin
SSU	SSI	I/O	Data I/O pin
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin
	SSCK	I/O	Clock I/O pin
	SSO	I/O	Data I/O pin

I: Input O: Output I/O: Input and output

Note:

1. Refer to the oscillator manufacturer for oscillation characteristics.

Table 1.16 Pin Functions (2)

Item	Pin Name	I/O Type	Description
CAN module	CRX0 (1)	I	CAN data input pin
	CTX0 (1)	O	CAN data output pin
Reference voltage input	VREF	I	Reference voltage input pin to A/D converter
A/D converter	AN0 to AN19	I	Analog input pins to A/D converter
	$\overline{\text{ADTRG}}$	I	AD external trigger input pin
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_3 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7 P8_0 to P8_7 P9_0 to P9_5	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program.
Input port	P4_2	I	Input-only port

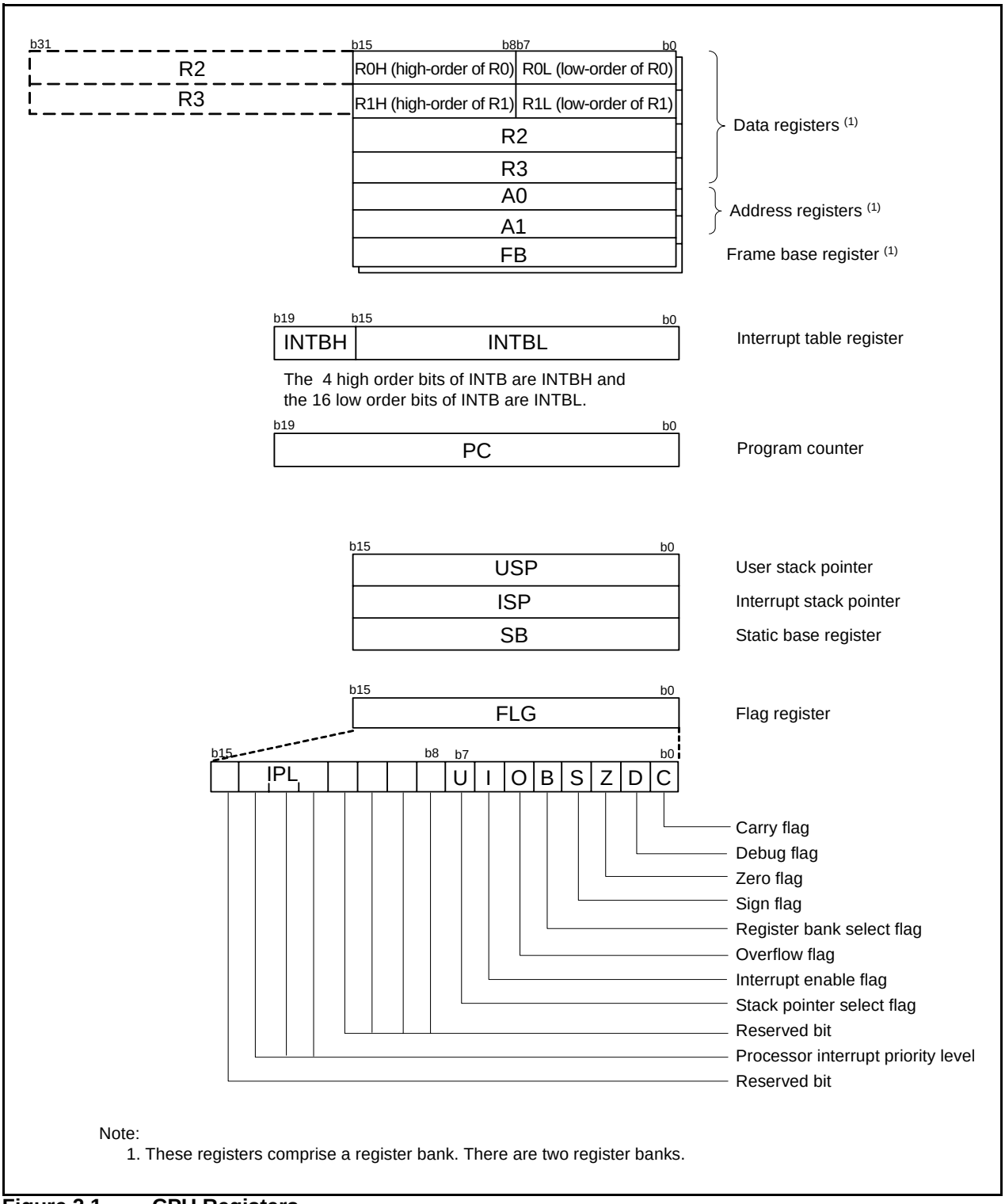
I: Input O: Output I/O: Input and output

Note:

1. Only in the R8C/38W Group and R8C/38X Group.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.



Note:
1. These registers comprise a register bank. There are two register banks.

Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

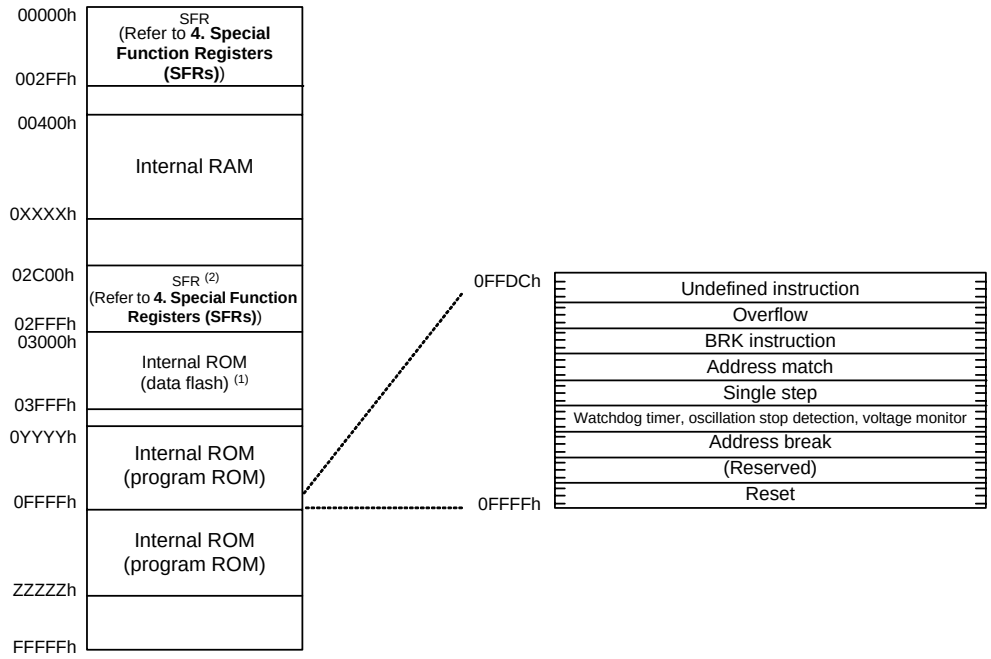
2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3. Memory

3.1 R8C/38W Group

Figure 3.1 is a Memory Map of R8C/38W Group. The R8C/38W Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 64-Kbyte internal ROM area is allocated addresses 04000h to 13FFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM area is allocated addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh (the SFR areas for the CAN, DTC, and other modules). Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



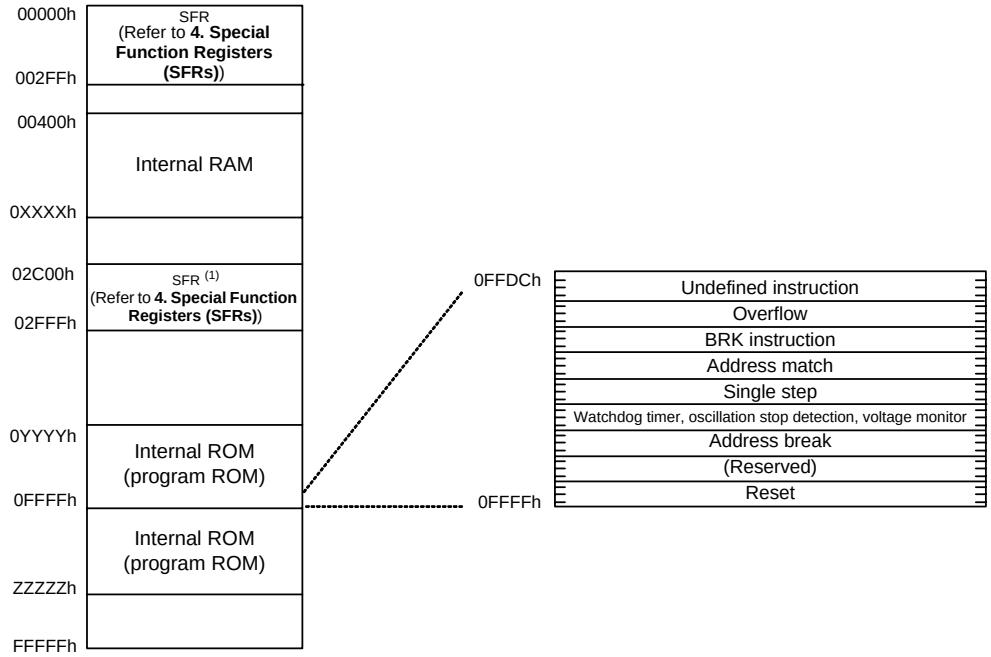
Notes:
1. The Data Flash memory indicates blocks A (1 Kbyte), B (1 Kbyte), C (1 Kbyte), and D (1 Kbyte).
2. The SFR areas for the CAN, DTC and other modules are allocated to addresses 02C00h to 02FFFh.
3. The blank areas are reserved and cannot be accessed by users.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh
R5F21388WJFP, R5F21388WKFP	64 Kbytes	04000h	13FFFh	6 Kbytes	01BFFh
R5F2138AWJFP, R5F2138AWKFP	96 Kbytes	04000h	1BFFFh	8 Kbytes	023FFh
R5F2138CWJFP, R5F2138CWKFP	128 Kbytes	04000h	23FFFh	10 Kbytes	02BFFh

Figure 3.1 Memory Map of R8C/38W Group

3.2 R8C/38X Group

Figure 3.2 is a Memory Map of R8C/38X Group. The R8C/38X Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 64-Kbyte internal ROM area is allocated addresses 04000h to 13FFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM area is allocated addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh (the SFR areas for the CAN, DTC, and other modules). Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



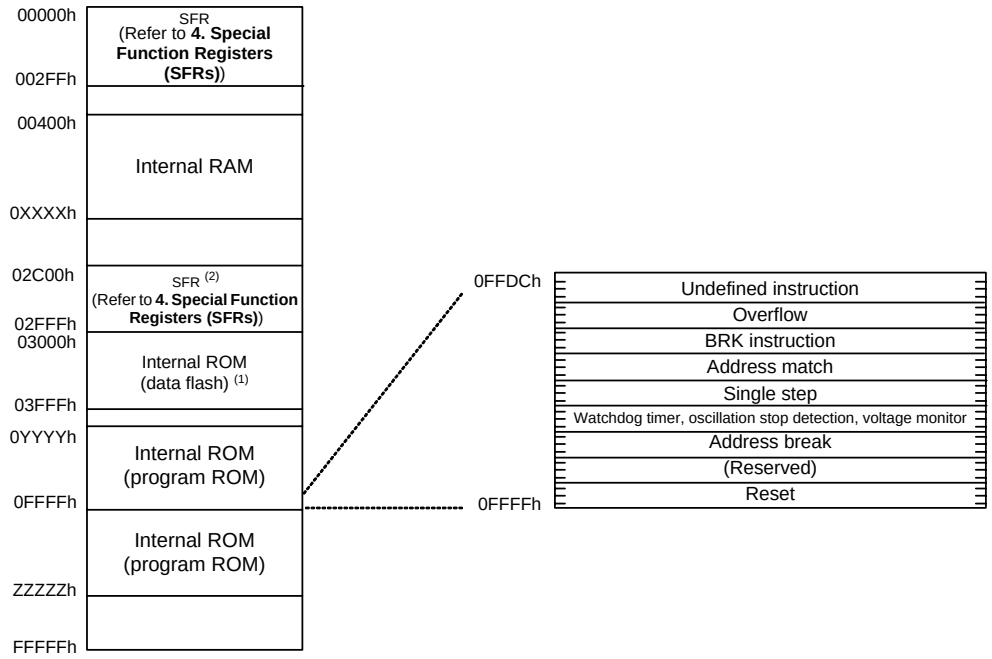
Notes:
1. The SFR areas for the CAN, DTC and other modules are allocated to addresses 02C00h to 02FFFh.
2. The blank areas are reserved and cannot be accessed by users.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh
R5F21388XJFP, R5F21388XKFP	64 Kbytes	04000h	13FFFh	6 Kbytes	01BFFh
R5F2138AXJFP, R5F2138AXKFP	96 Kbytes	04000h	1BFFFh	8 Kbytes	023FFh
R5F2138CXJFP, R5F2138CXKFP	128 Kbytes	04000h	23FFFh	10 Kbytes	02BFFh

Figure 3.2 Memory Map of R8C/38X Group

3.3 R8C/38Y Group

Figure 3.3 is a Memory Map of R8C/38Y Group. The R8C/38Y Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 64-Kbyte internal ROM area is allocated addresses 04000h to 13FFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM area is allocated addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh (the SFR areas for the DTC and other modules). Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



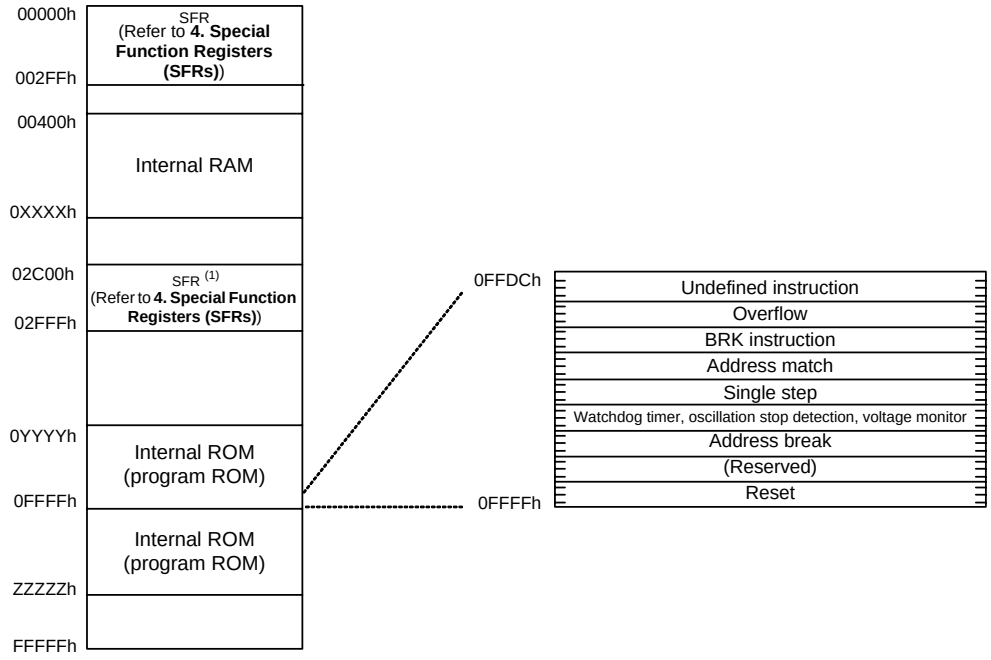
Notes:
1. The Data Flash memory indicates blocks A (1 Kbyte), B (1 Kbyte), C (1 Kbyte), and D (1 Kbyte).
2. The SFR areas for the DTC and other modules are allocated to addresses 02C00h to 02FFFh.
3. The blank areas are reserved and cannot be accessed by users.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh
R5F21388YJFP, R5F21388YKFP	64 Kbytes	04000h	13FFFh	6 Kbytes	01BFFh
R5F2138AYJFP, R5F2138AYKFP	96 Kbytes	04000h	1BFFFh	8 Kbytes	023FFh
R5F2138CYJFP, R5F2138CYKFP	128 Kbytes	04000h	23FFFh	10 Kbytes	02BFFh

Figure 3.3 Memory Map of R8C/38Y Group

3.4 R8C/38Z Group

Figure 3.4 is a Memory Map of R8C/38Z Group. The R8C/38Z Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 64-Kbyte internal ROM area is allocated addresses 04000h to 13FFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM area is allocated addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh (the SFR areas for the DTC and other modules). Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



Notes:
1. The SFR areas for the DTC and other modules are allocated to addresses 02C00h to 02FFFh.
2. The blank areas are reserved and cannot be accessed by users.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh
R5F21388ZJFP, R5F21388ZKFP	64 Kbytes	04000h	13FFFh	6 Kbytes	01BFFh
R5F2138AZJFP, R5F2138AZKFP	96 Kbytes	04000h	1BFFFh	8 Kbytes	023FFh
R5F2138CZJFP, R5F2138CZKFP	128 Kbytes	04000h	23FFFh	10 Kbytes	02BFFh

Figure 3.4 Memory Map of R8C/38Z Group

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.17 list the special function registers and Table 4.18 lists the ID Code Areas and Option Function Select Area.

Table 4.1 SFR Information (1) (1)

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	00101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h	Module Standby Control Register	MSTCR	00h
0009h	System Clock Control Register 3	CM3	00h
000Ah	Protect Register	PRCR	00h
000Bh	Reset Source Determination Register	RSTFR	0XXXXXXXb (2)
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDTC	00111111b
0010h			
0011h			
0012h			
0013h			
0014h			
0015h	High-Speed On-Chip Oscillator Control Register 7	FRA7	When shipping
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b (3)
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h	On-Chip Reference Voltage Control Register	OCVREFCR	00h
0027h			
0028h			
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	When shipping
002Ah	High-Speed On-Chip Oscillator Control Register 5	FRA5	When shipping
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	When shipping
002Ch			
002Dh			
002Eh			
002Fh	High-Speed On-Chip Oscillator Control Register 3	FRA3	When shipping
0030h	Voltage Monitor Circuit Control Register	CMPA	00h
0031h	Voltage Monitor Circuit Edge Select Register	VCAC	00h
0032h			
0033h	Voltage Detect Register 1	VCA1	00001000b
0034h	Voltage Detect Register 2	VCA2	00h (4) 00100000b (5)
0035h			
0036h	Voltage Detection 1 Level Select Register	VD1LS	00000111b
0037h			
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	1100X010b (4) 1100X011b (5)
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	10001010b

X: Undefined

Notes:
1. The blank areas are reserved and cannot be accessed by users.
2. The CWR bit in the RSTFR register is set to 0 after power-on and voltage monitor 0 reset. Hardware reset, software reset or watchdog timer reset does not affect this bit.
3. The CSPROINI bit in the OFS register is set to 0.
4. The LVDAS bit in the OFS register is set to 1.
5. The LVDAS bit in the OFS register is set to 0.

Table 4.2 SFR Information (2) (1)

Address	Register	Symbol	After reset
003Ah	Voltage Monitor 2 Circuit Control Register	VW2C	10000010b
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0042h	Timer RA1 Interrupt Control Register	TRA1IC	XXXXX000b
0043h			
0044h			
0045h			
0046h	INT4 Interrupt Control Register	INT4IC	XX00X000b
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h	Timer RD0 Interrupt Control Register	TRD0IC	XXXXX000b
0049h	Timer RD1 Interrupt Control Register	TRD1IC	XXXXX000b
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
004Ch	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU Interrupt Control Register	SSUIC	XXXXX000b
0050h	Timer RF Compare 1 Interrupt Control Register	CMP1IC	XXXXX000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h	INT2 Interrupt Control Register	INT2IC	XX00X000b
0056h	Timer RA0 Interrupt Control Register	TRA0IC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh	Timer RF Interrupt Control Register	TRFIC	XXXXX000b
005Ch	Timer RF Compare 0 Interrupt Control Register	CMP0IC	XXXXX000b
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh	UART2 Bus Collision Detection Interrupt Control Register	U2BCNIC	XXXXX000b
005Fh	Timer RF Capture Interrupt Control Register	CAPIC	XXXXX000b
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh	Timer RG Interrupt Control Register	TRGIC	XXXXX000b
006Ch	CAN0 Reception Complete Interrupt Control Register	C0RIC	XXXXX000b
006Dh	CAN0 Transmission Complete Interrupt Control Register	C0TIC	XXXXX000b
006Eh	CAN0 Receive FIFO Interrupt Control Register	C0FRIC	XXXXX000b
006Fh	CAN0 Transmit FIFO Interrupt Control Register	C0FTIC	XXXXX000b
0070h	CAN0 Error Interrupt Control Register	C0EIC	XXXXX000b
0071h	CAN0 Wake-up Interrupt Control Register	C0WIC	XXXXX000b
0072h	Voltage Monitor 1 Interrupt Control Register	VCMP1IC	XXXXX000b
0073h	Voltage Monitor 2 Interrupt Control Register	VCMP2IC	XXXXX000b
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.3 SFR Information (3) (1)

Address	Register	Symbol	After reset
0080h	DTC Activation Control Register	DTCTL	00h
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DTC Activation Enable Register 0	DTCEN0	00h
0089h	DTC Activation Enable Register 1	DTCEN1	00h
008Ah	DTC Activation Enable Register 2	DTCEN2	00h
008Bh	DTC Activation Enable Register 3	DTCEN3	00h
008Ch	DTC Activation Enable Register 4	DTCEN4	00h
008Dh	DTC Activation Enable Register 5	DTCEN5	00h
008Eh	DTC Activation Enable Register 6	DTCEN6	00h
008Fh			
0090h	Timer RF Register	TRF	00h
0091h			00h
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah	Timer RF Control Register 0	TRFCR0	00h
009Bh	Timer RF Control Register 1	TRFCR1	00h
009Ch	Capture and Compare 0 Register	TRFM0	00h
009Dh			00h
009Eh	Compare 1 Register	TRFM1	FFh
009Fh			FFh
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART2 Transmit/Receive Mode Register	U2MR	00h
00A9h	UART2 Bit Rate Register	U2BRG	XXh
00AAh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh			XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
00BCh	UART2 Special Mode Register 4	U2SMR4	00h
00BDh	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
00BEh	UART2 Special Mode Register 2	U2SMR2	X0000000b
00BFh	UART2 Special Mode Register	U2SMR	X0000000b

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.4 SFR Information (4) (1)

Address	Register	Symbol	After reset
00C0h	A/D Register 0	AD0	XXh
00C1h			000000XXb
00C2h	A/D Register 1	AD1	XXh
00C3h			000000XXb
00C4h	A/D Register 2	AD2	XXh
00C5h			000000XXb
00C6h	A/D Register 3	AD3	XXh
00C7h			000000XXb
00C8h	A/D Register 4	AD4	XXh
00C9h			000000XXb
00CAh	A/D Register 5	AD5	XXh
00CBh			000000XXb
00CCh	A/D Register 6	AD6	XXh
00CDh			000000XXb
00CEh	A/D Register 7	AD7	XXh
00CFh			000000XXb
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Mode Register	ADMOD	00h
00D5h	A/D Input Select Register	ADINSEL	11000000b
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h			
00D9h			
00DAh			
00DBh			
00DCh			
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h	Port P5 Register	P5	XXh
00EAh	Port P4 Direction Register	PD4	00h
00EBh	Port P5 Direction Register	PD5	00h
00ECh	Port P6 Register	P6	XXh
00EDh	Port P7 Register	P7	XXh
00EEh	Port P6 Direction Register	PD6	00h
00EFh	Port P7 Direction Register	PD7	00h
00F0h	Port P8 Register	P8	XXh
00F1h	Port P9 Register	P9	XXh
00F2h	Port P8 Direction Register	PD8	00h
00F3h	Port P9 Direction Register	PD9	00h
00F4h			
00F5h			
00F6h			
00F7h			
00F8h			
00F9h			
00FAh			
00FBh			
00FCh			
00FDh			
00FEh			
00FFh			

X: Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.5 SFR Information (5) (1)

Address	Register	Symbol	After reset
0100h	Timer RA0 Control Register	TRA0CR	00h
0101h	Timer RA0 I/O Control Register	TRA0IOC	00h
0102h	Timer RA0 Mode Register	TRA0MR	00h
0103h	Timer RA0 Prescaler Register	TRA0PRE	FFh
0104h	Timer RA0 Register	TRA0	FFh
0105h	LIN0 Control Register 2	LIN0CR2	00h
0106h	LIN0 Control Register	LIN0CR	00h
0107h	LIN0 Status Register	LIN0ST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h	Timer RA1 Control Register	TRA1CR	00h
0111h	Timer RA1 I/O Control Register	TRA1IOC	00h
0112h	Timer RA1 Mode Register	TRA1MR	00h
0113h	Timer RA1 Prescaler Register	TRA1PRE	FFh
0114h	Timer RA1 Register	TRA1	FFh
0115h	LIN1 Control Register 2	LIN1CR2	00h
0116h	LIN1 Control Register	LIN1CR	00h
0117h	LIN1 Status Register	LIN1ST	00h
0118h	Timer RE Counter Data Register	TRESEC	00h
0119h	Timer RE Compare Data Register	TREMIN	00h
011Ah			
011Bh			
011Ch	Timer RE Control Register 1	TRECR1	00h
011Dh	Timer RE Control Register 2	TRECR2	00h
011Eh	Timer RE Count Source Select Register	TRECSR	00001000b
011Fh			
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011000b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h	Timer RC Trigger Control Register	TRCADCR	00h
0134h			
0135h			
0136h	Timer RD Trigger Control Register	TRDADCR	00h
0137h	Timer RD Start Register	TRDSTR	11111100b
0138h	Timer RD Mode Register	TRDMR	00001110b
0139h	Timer RD PWM Mode Register	TRDPMR	10001000b
013Ah	Timer RD Function Control Register	TRDFCR	10000000b
013Bh	Timer RD Output Master Enable Register 1	TRDOER1	FFh
013Ch	Timer RD Output Master Enable Register 2	TRDOER2	01111111b
013Dh	Timer RD Output Control Register	TRDOCR	00h
013Eh	Timer RD Digital Filter Function Select Register 0	TRDDF0	00h
013Fh	Timer RD Digital Filter Function Select Register 1	TRDDF1	00h

Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.6 SFR Information (6) (1)

Address	Register	Symbol	After reset
0140h	Timer RD Control Register 0	TRDCR0	00h
0141h	Timer RD I/O Control Register A0	TRDIORA0	10001000b
0142h	Timer RD I/O Control Register C0	TRDIORC0	10001000b
0143h	Timer RD Status Register 0	TRDSR0	11100000b
0144h	Timer RD Interrupt Enable Register 0	TRDIER0	11100000b
0145h	Timer RD PWM Mode Output Level Control Register 0	TRDPOCR0	11111000b
0146h	Timer RD Counter 0	TRD0	00h
0147h			00h
0148h	Timer RD General Register A0	TRDGRA0	FFh
0149h			FFh
014Ah	Timer RD General Register B0	TRDGRB0	FFh
014Bh			FFh
014Ch	Timer RD General Register C0	TRDGRC0	FFh
014Dh			FFh
014Eh	Timer RD General Register D0	TRDGRD0	FFh
014Fh			FFh
0150h	Timer RD Control Register 1	TRDCR1	00h
0151h	Timer RD I/O Control Register A1	TRDIORA1	10001000b
0152h	Timer RD I/O Control Register C1	TRDIORC1	10001000b
0153h	Timer RD Status Register 1	TRDSR1	11000000b
0154h	Timer RD Interrupt Enable Register 1	TRDIER1	11100000b
0155h	Timer RD PWM Mode Output Level Control Register 1	TRDPOCR1	11111000b
0156h	Timer RD Counter 1	TRD1	00h
0157h			00h
0158h	Timer RD General Register A1	TRDGRA1	FFh
0159h			FFh
015Ah	Timer RD General Register B1	TRDGRB1	FFh
015Bh			FFh
015Ch	Timer RD General Register C1	TRDGRC1	FFh
015Dh			FFh
015Eh	Timer RD General Register D1	TRDGRD1	FFh
015Fh			FFh
0160h	UART1 Transmit/Receive Mode Register	U1MR	00h
0161h	UART1 Bit Rate Register	U1BRG	XXh
0162h	UART1 Transmit Buffer Register	U1TB	XXh
0163h			XXh
0164h	UART1 Transmit/Receive Control Register 0	U1C0	00001000b
0165h	UART1 Transmit/Receive Control Register 1	U1C1	00000010b
0166h	UART1 Receive Buffer Register	U1RB	XXh
0167h			XXh
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h	Timer RG Mode Register	TRGMR	01000000b
0171h	Timer RG Count Control Register	TRGCNTC	00h
0172h	Timer RG Control Register	TRGCR	10000000b
0173h	Timer RG Interrupt Enable Register	TRGIER	11110000b
0174h	Timer RG Status Register	TRGSR	11100000b
0175h	Timer RG I/O Control Register	TRGIOR	00h
0176h	Timer RG Counter	TRG	00h
0177h			00h
0178h	Timer RG General Register A	TRGGRA	FFh
0179h			FFh
017Ah	Timer RG General Register B	TRGGRB	FFh
017Bh			FFh
017Ch	Timer RG General Register C	TRGGRC	FFh
017Dh			FFh
017Eh	Timer RG General Register D	TRGGRD	FFh
017Fh			FFh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.7 SFR Information (7) (1)

Address	Register	Symbol	After reset
0180h	Timer RA Pin Select Register	TRASR	00h
0181h	Timer RB/RC Pin Select Register	TRBRCSR	00h
0182h	Timer RC Pin Select Register 0	TRCPSR0	00h
0183h	Timer RC Pin Select Register 1	TRCPSR1	00h
0184h	Timer RD Pin Select Register 0	TRDPSR0	00h
0185h	Timer RD Pin Select Register 1	TRDPSR1	00h
0186h	Timer Pin Select Register	TIMSR	00h
0187h	Timer RF Output Control Register	TRFOUT	00h
0188h	UART0 Pin Select Register	U0SR	00h
0189h	UART1 Pin Select Register	U1SR	00h
018Ah	UART2 Pin Select Register 0	U2SR0	00h
018Bh	UART2 Pin Select Register 1	U2SR1	00h
018Ch	SSU Pin Select Register	SSUIICSR	00h
018Dh			
018Eh	INT Interrupt Input Pin Select Register	INTSR	00h
018Fh	I/O Function Pin Select Register	PINSR	00h
0190h			
0191h			
0192h			
0193h	SS Bit Counter Register	SSBR	11111000b
0194h	SS Transmit Data Register	SSTDR	FFh
0195h			FFh
0196h	SS Receive Data Register	SSRDR	FFh
0197h			FFh
0198h	SS Control Register H	SSCRH	00h
0199h	SS Control Register L	SSCRL	01111101b
019Ah	SS Mode Register	SSMR	00010000b
019Bh	SS Enable Register	SSER	00h
019Ch	SS Status Register	SSSR	00h
019Dh	SS Mode Register 2	SSMR2	00h
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	10000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	00h
01B6h	Flash Memory Control Register 2	FMR2	00h
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

X: Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.8 SFR Information (8) (1)

Address	Register	Symbol	After reset
01C0h	Address Match Interrupt Register 0	RMAD0	XXh
01C1h			XXh
01C2h			0000XXXXb
01C3h	Address Match Interrupt Enable Register 0	AIER0	00h
01C4h	Address Match Interrupt Register 1	RMAD1	XXh
01C5h			XXh
01C6h			0000XXXXb
01C7h	Address Match Interrupt Enable Register 1	AIER1	00h
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	Pull-Up Control Register 0	PUR0	00h
01E1h	Pull-Up Control Register 1	PUR1	00h
01E2h	Pull-Up Control Register 2	PUR2	00h
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h			
01F1h			
01F2h			
01F3h			
01F4h			
01F5h	Input Threshold Control Register 0	VLT0	00h
01F6h	Input Threshold Control Register 1	VLT1	00h
01F7h	Input Threshold Control Register 2	VLT2	00h
01F8h			
01F9h			
01FAh	External Input Enable Register 0	INTEN	00h
01FBh	External Input Enable Register 1	INTEN1	00h
01FCh	INT Input Filter Select Register 0	INTF	00h
01FDh	INT Input Filter Select Register 1	INTF1	00h
01FEh	Key Input Enable Register 0	KIEN	00h
01FFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.9 SFR Information (9) (1)

Address	Register	Symbol	After reset
2C00h	DTC Transfer Vector Area		XXh
2C01h	DTC Transfer Vector Area		XXh
2C02h	DTC Transfer Vector Area		XXh
2C03h	DTC Transfer Vector Area		XXh
2C04h	DTC Transfer Vector Area		XXh
2C05h			
2C06h			
2C07h			
2C08h	DTC Transfer Vector Area		XXh
2C09h	DTC Transfer Vector Area		XXh
2C0Ah	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
2C3Ah			
2C3Bh			
2C3Ch			
2C3Dh			
2C3Eh			
2C3Fh			
2C40h	DTC Control Data 0	DTCD0	XXh
2C41h			XXh
2C42h			XXh
2C43h			XXh
2C44h			XXh
2C45h			XXh
2C46h			XXh
2C47h			XXh
2C48h	DTC Control Data 1	DTCD1	XXh
2C49h			XXh
2C4Ah			XXh
2C4Bh			XXh
2C4Ch			XXh
2C4Dh			XXh
2C4Eh			XXh
2C4Fh			XXh
2C50h	DTC Control Data 2	DTCD2	XXh
2C51h			XXh
2C52h			XXh
2C53h			XXh
2C54h			XXh
2C55h			XXh
2C56h			XXh
2C57h			XXh
2C58h	DTC Control Data 3	DTCD3	XXh
2C59h			XXh
2C5Ah			XXh
2C5Bh			XXh
2C5Ch			XXh
2C5Dh			XXh
2C5Eh			XXh
2C5Fh			XXh
2C60h	DTC Control Data 4	DTCD4	XXh
2C61h			XXh
2C62h			XXh
2C63h			XXh
2C64h			XXh
2C65h			XXh
2C66h			XXh
2C67h			XXh
2C68h	DTC Control Data 5	DTCD5	XXh
2C69h			XXh
2C6Ah			XXh
2C6Bh			XXh
2C6Ch			XXh
2C6Dh			XXh
2C6Eh			XXh
2C6Fh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.10 SFR Information (10) (1)

Address	Register	Symbol	After reset
2C70h	DTC Control Data 6	DTCD6	XXh
2C71h			XXh
2C72h			XXh
2C73h			XXh
2C74h			XXh
2C75h			XXh
2C76h			XXh
2C77h			XXh
2C78h	DTC Control Data 7	DTCD7	XXh
2C79h			XXh
2C7Ah			XXh
2C7Bh			XXh
2C7Ch			XXh
2C7Dh			XXh
2C7Eh			XXh
2C7Fh			XXh
2C80h	DTC Control Data 8	DTCD8	XXh
2C81h			XXh
2C82h			XXh
2C83h			XXh
2C84h			XXh
2C85h			XXh
2C86h			XXh
2C87h			XXh
2C88h	DTC Control Data 9	DTCD9	XXh
2C89h			XXh
2C8Ah			XXh
2C8Bh			XXh
2C8Ch			XXh
2C8Dh			XXh
2C8Eh			XXh
2C8Fh			XXh
2C90h	DTC Control Data 10	DTCD10	XXh
2C91h			XXh
2C92h			XXh
2C93h			XXh
2C94h			XXh
2C95h			XXh
2C96h			XXh
2C97h			XXh
2C98h	DTC Control Data 11	DTCD11	XXh
2C99h			XXh
2C9Ah			XXh
2C9Bh			XXh
2C9Ch			XXh
2C9Dh			XXh
2C9Eh			XXh
2C9Fh			XXh
2CA0h	DTC Control Data 12	DTCD12	XXh
2CA1h			XXh
2CA2h			XXh
2CA3h			XXh
2CA4h			XXh
2CA5h			XXh
2CA6h			XXh
2CA7h			XXh
2CA8h	DTC Control Data 13	DTCD13	XXh
2CA9h			XXh
2CAAh			XXh
2CABh			XXh
2CACh			XXh
2CADh			XXh
2CAEh			XXh
2CAFh			XXh

X: Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.11 SFR Information (11) (1)

Address	Register	Symbol	After reset
2CB0h	DTC Control Data 14	DTCD14	XXh
2CB1h			XXh
2CB2h			XXh
2CB3h			XXh
2CB4h			XXh
2CB5h			XXh
2CB6h			XXh
2CB7h			XXh
2CB8h	DTC Control Data 15	DTCD15	XXh
2CB9h			XXh
2CBAh			XXh
2CBBh			XXh
2CBCh			XXh
2CBDh			XXh
2CBEh			XXh
2CBFh			XXh
2CC0h	DTC Control Data 16	DTCD16	XXh
2CC1h			XXh
2CC2h			XXh
2CC3h			XXh
2CC4h			XXh
2CC5h			XXh
2CC6h			XXh
2CC7h			XXh
2CC8h	DTC Control Data 17	DTCD17	XXh
2CC9h			XXh
2CCAh			XXh
2CCBh			XXh
2CCCh			XXh
2CCDh			XXh
2CCEh			XXh
2CCFh			XXh
2CD0h	DTC Control Data 18	DTCD18	XXh
2CD1h			XXh
2CD2h			XXh
2CD3h			XXh
2CD4h			XXh
2CD5h			XXh
2CD6h			XXh
2CD7h			XXh
2CD8h	DTC Control Data 19	DTCD19	XXh
2CD9h			XXh
2CDAh			XXh
2CDBh			XXh
2CDCh			XXh
2CDDh			XXh
2CDEh			XXh
2CDFh			XXh
2CE0h	DTC Control Data 20	DTCD20	XXh
2CE1h			XXh
2CE2h			XXh
2CE3h			XXh
2CE4h			XXh
2CE5h			XXh
2CE6h			XXh
2CE7h			XXh
2CE8h	DTC Control Data 21	DTCD21	XXh
2CE9h			XXh
2CEAh			XXh
2CEBh			XXh
2CECh			XXh
2CEDh			XXh
2CEEh			XXh
2CEFh			XXh

X: Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.12 SFR Information (12) (1)

Address	Register	Symbol	After reset
2CF0h	DTC Control Data 22	DTCD22	XXh
2CF1h			XXh
2CF2h			XXh
2CF3h			XXh
2CF4h			XXh
2CF5h			XXh
2CF6h			XXh
2CF7h			XXh
2CF8h	DTC Control Data 23	DTCD23	XXh
2CF9h			XXh
2CFAh			XXh
2CFBh			XXh
2CFCh			XXh
2CFDh			XXh
2CFEh			XXh
2CFFh			XXh
2D00h			
2D01h			
:			
2E00h	CAN0 Mailbox 0: Message ID	C0MB0	XXh
2E01h			XXh
2E02h			XXh
2E03h			XXh
2E04h			
2E05h	CAN0 Mailbox 0: Data length		XXh
2E06h	CAN0 Mailbox 0: Data field		XXh
2E07h			XXh
2E08h			XXh
2E09h			XXh
2E0Ah			XXh
2E0Bh			XXh
2E0Ch			XXh
2E0Dh			XXh
2E0Eh	CAN0 Mailbox 0: Time stamp		XXh
2E0Fh			XXh
2E10h	CAN0 Mailbox 1: Message ID	C0MB1	XXh
2E11h			XXh
2E12h			XXh
2E13h			XXh
2E14h			
2E15h	CAN0 Mailbox 1: Data length		XXh
2E16h	CAN0 Mailbox 1: Data field		XXh
2E17h			XXh
2E18h			XXh
2E19h			XXh
2E1Ah			XXh
2E1Bh			XXh
2E1Ch			XXh
2E1Dh			XXh
2E1Eh	CAN0 Mailbox 1: Time stamp		XXh
2E1Fh			XXh
2E20h	CAN0 Mailbox 2: Message ID	C0MB2	XXh
2E21h			XXh
2E22h			XXh
2E23h			XXh
2E24h			
2E25h	CAN0 Mailbox 2: Data length		XXh
2E26h	CAN0 Mailbox 2: Data field		XXh
2E27h			XXh
2E28h			XXh
2E29h			XXh
2E2Ah			XXh
2E2Bh			XXh
2E2Ch			XXh
2E2Dh			XXh
2E2Eh	CAN0 Mailbox 2: Time stamp		XXh
2E2Fh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.13 SFR Information (13) (1)

Address	Register	Symbol	After reset
2E30h	CAN0 Mailbox 3: Message ID	C0MB3	XXh
2E31h			XXh
2E32h			XXh
2E33h			XXh
2E34h			
2E35h	CAN0 Mailbox 3: Data length		XXh
2E36h	CAN0 Mailbox 3: Data field		XXh
2E37h			XXh
2E38h			XXh
2E39h			XXh
2E3Ah			XXh
2E3Bh			XXh
2E3Ch			XXh
2E3Dh			XXh
2E3Eh	CAN0 Mailbox 3: Time stamp		XXh
2E3Fh			XXh
2E40h	CAN0 Mailbox 4: Message ID	C0MB4	XXh
2E41h			XXh
2E42h			XXh
2E43h			XXh
2E44h			
2E45h	CAN0 Mailbox 4: Data length		XXh
2E46h	CAN0 Mailbox 4: Data field		XXh
2E47h			XXh
2E48h			XXh
2E49h			XXh
2E4Ah			XXh
2E4Bh			XXh
2E4Ch			XXh
2E4Dh			XXh
2E4Eh	CAN0 Mailbox 4: Time stamp		XXh
2E4Fh			XXh
2E50h	CAN0 Mailbox 5: Message ID	C0MB5	XXh
2E51h			XXh
2E52h			XXh
2E53h			XXh
2E54h			
2E55h	CAN0 Mailbox 5: Data length		XXh
2E56h	CAN0 Mailbox 5: Data field		XXh
2E57h			XXh
2E58h			XXh
2E59h			XXh
2E5Ah			XXh
2E5Bh			XXh
2E5Ch			XXh
2E5Dh			XXh
2E5Eh	CAN0 Mailbox 5: Time stamp		XXh
2E5Fh			XXh
2E60h	CAN0 Mailbox 6: Message ID	C0MB6	XXh
2E61h			XXh
2E62h			XXh
2E63h			XXh
2E64h			
2E65h	CAN0 Mailbox 6: Data length		XXh
2E66h	CAN0 Mailbox 6: Data field		XXh
2E67h			XXh
2E68h			XXh
2E69h			XXh
2E6Ah			XXh
2E6Bh			XXh
2E6Ch			XXh
2E6Dh			XXh
2E6Eh	CAN0 Mailbox 6: Time stamp		XXh
2E6Fh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.14 SFR Information (14) (1)

Address	Register	Symbol	After reset
2E70h	CAN0 Mailbox 7: Message ID	C0MB7	XXh
2E71h			XXh
2E72h			XXh
2E73h			XXh
2E74h			
2E75h	CAN0 Mailbox 7: Data length		XXh
2E76h	CAN0 Mailbox 7: Data field		XXh
2E77h			XXh
2E78h			XXh
2E79h			XXh
2E7Ah			XXh
2E7Bh			XXh
2E7Ch			XXh
2E7Dh			XXh
2E7Eh	CAN0 Mailbox 7: Time stamp		XXh
2E7Fh			XXh
2E80h	CAN0 Mailbox 8: Message ID	C0MB8	XXh
2E81h			XXh
2E82h			XXh
2E83h			XXh
2E84h			
2E85h	CAN0 Mailbox 8: Data length		XXh
2E86h	CAN0 Mailbox 8: Data field		XXh
2E87h			XXh
2E88h			XXh
2E89h			XXh
2E8Ah			XXh
2E8Bh			XXh
2E8Ch			XXh
2E8Dh			XXh
2E8Eh	CAN0 Mailbox 8: Time stamp		XXh
2E8Fh			XXh
2E90h	CAN0 Mailbox 9: Message ID	C0MB9	XXh
2E91h			XXh
2E92h			XXh
2E93h			XXh
2E94h			
2E95h	CAN0 Mailbox 9: Data length		XXh
2E96h	CAN0 Mailbox 9: Data field		XXh
2E97h			XXh
2E98h			XXh
2E99h			XXh
2E9Ah			XXh
2E9Bh			XXh
2E9Ch			XXh
2E9Dh			XXh
2E9Eh	CAN0 Mailbox 9: Time stamp		XXh
2E9Fh			XXh
2EA0h	CAN0 Mailbox 10: Message ID	C0MB10	XXh
2EA1h			XXh
2EA2h			XXh
2EA3h			XXh
2EA4h			
2EA5h	CAN0 Mailbox 10: Data length		XXh
2EA6h	CAN0 Mailbox 10: Data field		XXh
2EA7h			XXh
2EA8h			XXh
2EA9h			XXh
2EAAh			XXh
2EABh			XXh
2EACh			XXh
2EADh			XXh
2EAEh	CAN0 Mailbox 10: Time stamp		XXh
2EAFh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.15 SFR Information (15) (1)

Address	Register	Symbol	After reset
2EB0h	CAN0 Mailbox 11: Message ID	C0MB11	XXh
2EB1h			XXh
2EB2h			XXh
2EB3h			XXh
2EB4h			
2EB5h	CAN0 Mailbox 11: Data length		XXh
2EB6h	CAN0 Mailbox 11: Data field		XXh
2EB7h			XXh
2EB8h			XXh
2EB9h			XXh
2EBAh			XXh
2EBBh			XXh
2EBCh			XXh
2EBDh			XXh
2EBEh	CAN0 Mailbox 11: Time stamp		XXh
2EBFh			XXh
2EC0h	CAN0 Mailbox 12: Message ID	C0MB12	XXh
2EC1h			XXh
2EC2h			XXh
2EC3h			XXh
2EC4h			
2EC5h	CAN0 Mailbox 12: Data length		XXh
2EC6h	CAN0 Mailbox 12: Data field		XXh
2EC7h			XXh
2EC8h			XXh
2EC9h			XXh
2ECAh			XXh
2ECBh			XXh
2ECCh			XXh
2ECDh			XXh
2ECEh	CAN0 Mailbox 12: Time stamp		XXh
2ECFh			XXh
2ED0h	CAN0 Mailbox 13: Message ID	C0MB13	XXh
2ED1h			XXh
2ED2h			XXh
2ED3h			XXh
2ED4h			
2ED5h	CAN0 Mailbox 13: Data length		XXh
2ED6h	CAN0 Mailbox 13: Data field		XXh
2ED7h			XXh
2ED8h			XXh
2ED9h			XXh
2EDAh			XXh
2EDBh			XXh
2EDCh			XXh
2EDDh			XXh
2EDEh	CAN0 Mailbox 13: Time stamp		XXh
2EDFh			XXh
2EE0h	CAN0 Mailbox 14: Message ID	C0MB14	XXh
2EE1h			XXh
2EE2h			XXh
2EE3h			XXh
2EE4h			
2EE5h	CAN0 Mailbox 14: Data length		XXh
2EE6h	CAN0 Mailbox 14: Data field		XXh
2EE7h			XXh
2EE8h			XXh
2EE9h			XXh
2EEAh			XXh
2EEBh			XXh
2EECh			XXh
2EEDh			XXh
2EEEh	CAN0 Mailbox 14: Time stamp		XXh
2EEFh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.16 SFR Information (16) (1)

Address	Register	Symbol	After reset
2EF0h	CAN0 Mailbox 15: Message ID	C0MB15	XXh
2EF1h			XXh
2EF2h			XXh
2EF3h			XXh
2EF4h			
2EF5h	CAN0 Mailbox 15: Data length		XXh
2EF6h	CAN0 Mailbox 15: Data field		XXh
2EF7h			XXh
2EF8h			XXh
2EF9h			XXh
2EFAh			XXh
2EFBh			XXh
2EFCh			XXh
2EFDh			XXh
2EFEh	CAN0 Mailbox 15: Time stamp		XXh
2EFFh			XXh
2F00h			
2F01h			
2F02h			
2F03h			
2F04h			
2F05h			
2F06h			
2F07h			
2F08h			
2F09h			
2F0Ah			
2F0Bh			
2F0Ch			
2F0Dh			
2F0Eh			
2F0Fh			
2F10h	CAN0 Mask Register 0	C0MKR0	XXh
2F11h			XXh
2F12h			XXh
2F13h			XXh
2F14h	CAN0 Mask Register 1	C0MKR1	XXh
2F15h			XXh
2F16h			XXh
2F17h			XXh
2F18h	CAN0 Mask Register 2	C0MKR2	XXh
2F19h			XXh
2F1Ah			XXh
2F1Bh			XXh
2F1Ch	CAN0 Mask Register 3	C0MKR3	XXh
2F1Dh			XXh
2F1Eh			XXh
2F1Fh			XXh
2F20h	CAN0 FIFO Received ID Compare Register 0	C0FIDCR0	XXh
2F21h			XXh
2F22h			XXh
2F23h			XXh
2F24h	CAN0 FIFO Received ID Compare Register 1	C0FIDCR1	XXh
2F25h			XXh
2F26h			XXh
2F27h			XXh
2F28h			
2F29h			
2F2Ah	CAN0 Mask Invalid Register	C0MKIVLR	XXh
2F2Bh			XXh
2F2Ch			
2F2Dh			
2F2Eh	CAN0 Mailbox Interrupt Enable Register	C0MIER	XXh
2F2Fh			XXh
2F30h	CAN0 Message Control Register 0	C0MCTL0	00h
2F31h	CAN0 Message Control Register 1	C0MCTL1	00h
2F32h	CAN0 Message Control Register 2	C0MCTL2	00h
2F33h	CAN0 Message Control Register 3	C0MCTL3	00h
2F34h	CAN0 Message Control Register 4	C0MCTL4	00h
2F35h	CAN0 Message Control Register 5	C0MCTL5	00h
2F36h	CAN0 Message Control Register 6	C0MCTL6	00h
2F37h	CAN0 Message Control Register 7	C0MCTL7	00h
2F38h	CAN0 Message Control Register 8	C0MCTL8	00h
2F39h	CAN0 Message Control Register 9	C0MCTL9	00h
2F3Ah	CAN0 Message Control Register 10	C0MCTL10	00h

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.17 SFR Information (17) (1)

Address	Register	Symbol	After reset
2F3Bh	CAN0 Message Control Register 11	C0MCTL11	00h
2F3Ch	CAN0 Message Control Register 12	C0MCTL12	00h
2F3Dh	CAN0 Message Control Register 13	C0MCTL13	00h
2F3Eh	CAN0 Message Control Register 14	C0MCTL14	00h
2F3Fh	CAN0 Message Control Register 15	C0MCTL15	00h
2F40h	CAN0 Control Register	C0CTLR	00000101b
2F41h			00h
2F42h	CAN0 Status Register	C0STR	00000101b
2F43h			00h
2F44h	CAN0 Bit Configuration Register	C0BCR	00h
2F45h			00h
2F46h			00h
2F47h			
2F48h	CAN0 Receive FIFO Control Register	C0RFCR	10000000b
2F49h	CAN0 Receive FIFO Pointer Control Register	C0RFPCR	XXh
2F4Ah	CAN0 Transmit FIFO Control Register	C0TFCR	10000000b
2F4Bh	CAN0 Transmit FIFO Pointer Control Register	C0TFPCR	XXh
2F4Ch	CAN0 Error Interrupt Enable Register	C0EIER	00h
2F4Dh	CAN0 Error Interrupt Factor Judge Register	C0EIFR	00h
2F4Eh	CAN0 Reception Error Count Register	C0RECR	00h
2F4Fh	CAN0 Transmission Error Count Register	C0TECR	00h
2F50h	CAN0 Error Code Store Register	C0ECSR	00h
2F51h	CAN0 Channel Search Support Register	C0CSSR	XXh
2F52h	CAN0 Mailbox Search Status Register	C0MSSR	10000000b
2F53h	CAN0 Mailbox Search Mode Register	C0MSMR	00h
2F54h	CAN0 Time Stamp Register	C0TSR	00h
2F55h			00h
2F56h	CAN0 Acceptance Filter Support Register	C0AFSR	XXh
2F57h			XXh
2F58h	CAN0 Test Control Register	C0TCR	00h
:			
2FFFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.18 ID Code Areas and Option Function Select Area

Address	Area Name	Symbol	After Reset
:			
FFDBh	Option Function Select Register 2	OFS2	(Note 1)
:			
FFDFh	ID1		(Note 2)
:			
FFE3h	ID2		(Note 2)
:			
FFEBh	ID3		(Note 2)
:			
FFEFh	ID4		(Note 2)
:			
FFF3h	ID5		(Note 2)
:			
FFF7h	ID6		(Note 2)
:			
FFFBh	ID7		(Note 2)
:			
FFFFh	Option Function Select Register	OFS	(Note 1)

Notes:

1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh.
   When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
2. The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh.
   When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user.
   When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

5. Resets

The following resets are implemented: hardware reset, power-on reset, voltage monitor 0 reset, watchdog timer reset, and software reset.
Table 5.1 lists the Reset Names and Sources.

Table 5.1 Reset Names and Sources

Reset Name	Source
Hardware reset	Input voltage of $\overline{\text{RESET}}$ pin is held “L”
Power-on reset	VCC rises
Voltage monitor 0 reset	VCC falls (monitor voltage: Vdet0)
Watchdog timer reset	Underflow of watchdog timer
Software reset	Write 1 to PM03 bit in PM0 register

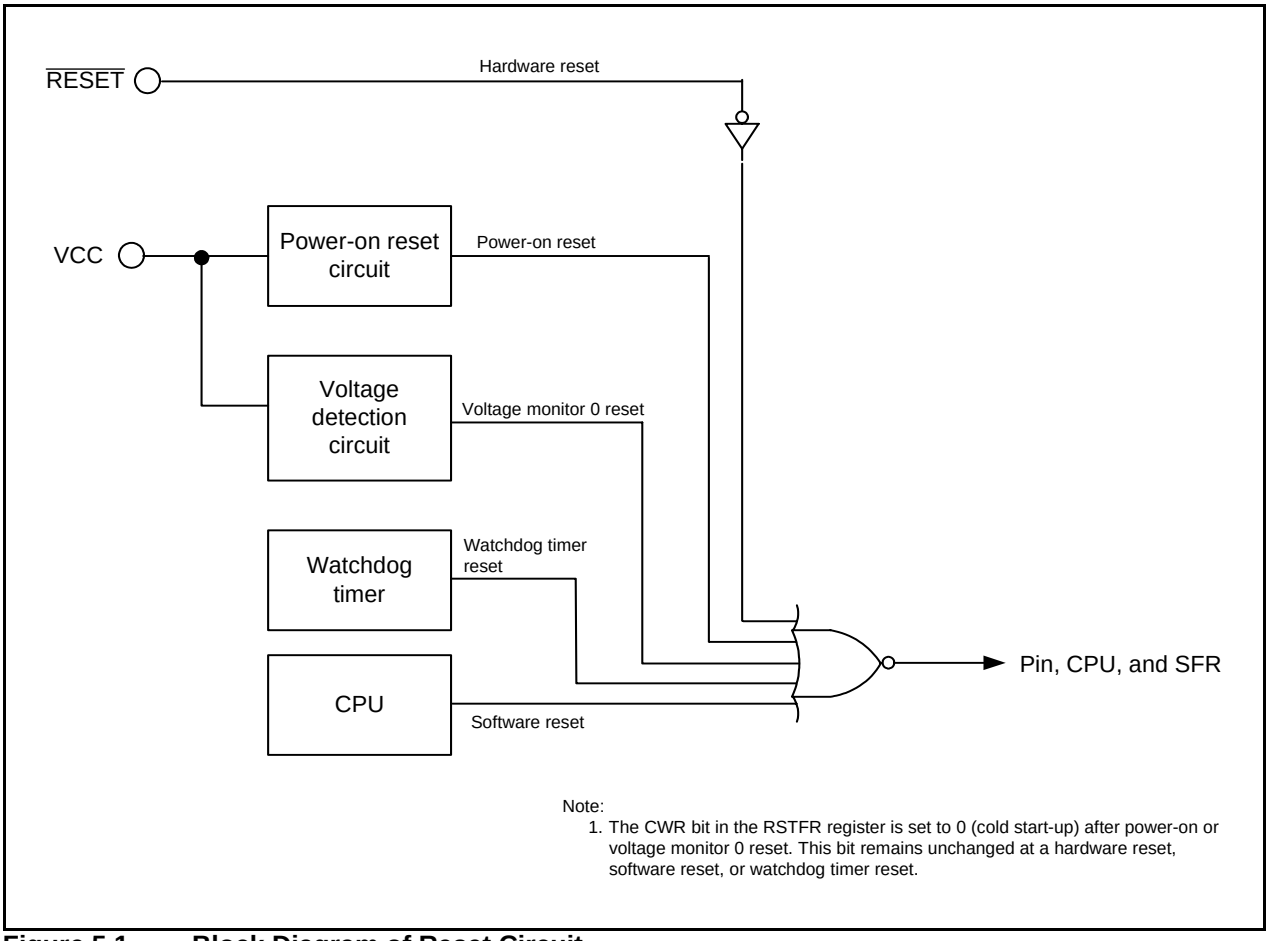


Figure 5.1 Block Diagram of Reset Circuit

Table 5.2 shows the Pin Functions while $\overline{\text{RESET}}$ Pin Level is “L”, Figure 5.2 shows the CPU Register Status after Reset, Figure 5.3 shows the Reset Sequence.

Table 5.2 Pin Functions while $\overline{\text{RESET}}$ Pin Level is “L”

Pin Name	Pin Function
P0 to P3, P5 to P8	Input port
P4_2 to P4_7	Input port
P9_0 to P9_5	Input port

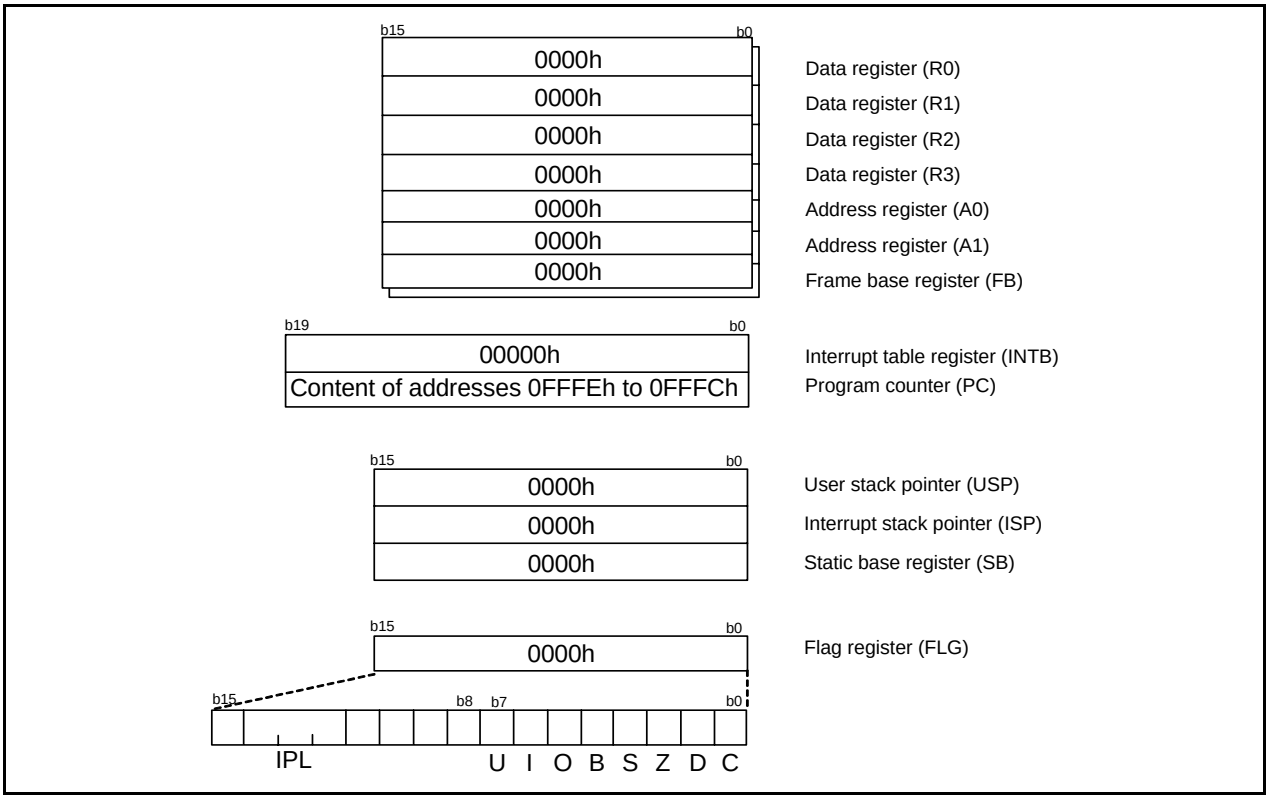
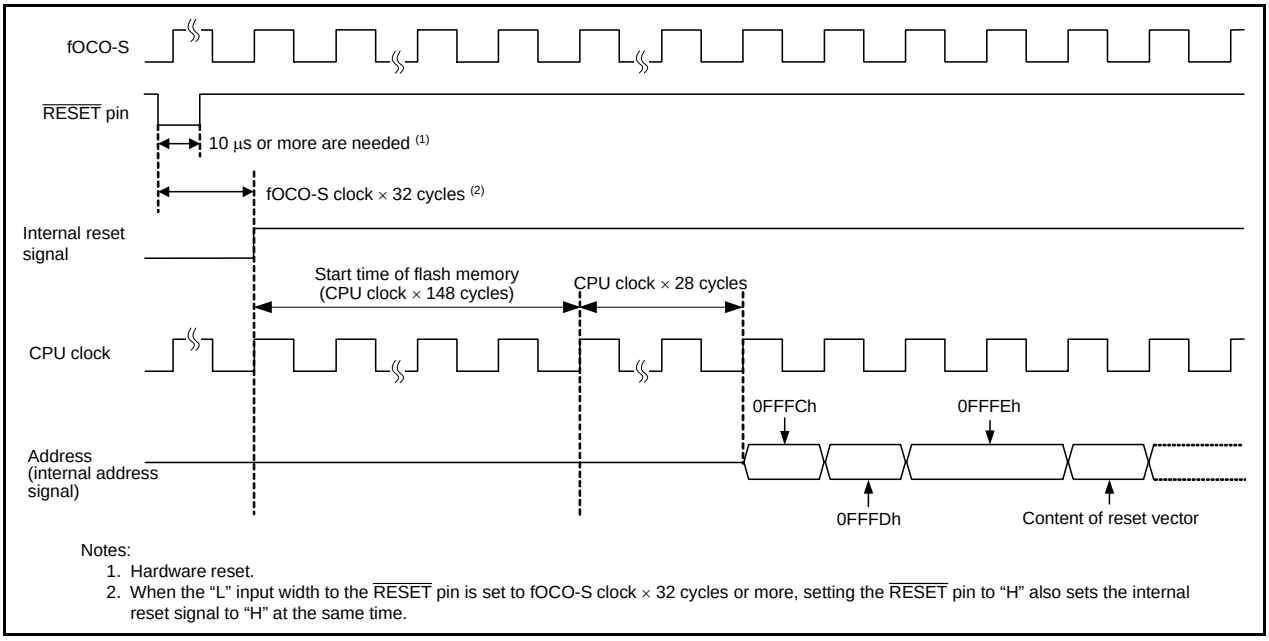


Figure 5.2 CPU Register Status after Reset



Notes:
1. Hardware reset.
2. When the “L” input width to the $\overline{\text{RESET}}$ pin is set to fOCO-S clock × 32 cycles or more, setting the $\overline{\text{RESET}}$ pin to “H” also sets the internal reset signal to “H” at the same time.

Figure 5.3 Reset Sequence

5.1 Registers

5.1.1 Processor Mode Register 0 (PM0)

Address 0004h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	PM03	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	PM03	Software reset bit	The MCU is reset when this bit is set to 1. When read, the content is 0.	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting the PM0 register.

5.1.2 Reset Source Determination Register (RSTFR)

Address 000Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	—	—	WDR	SWR	HWR	CWR	
After Reset	0	X	X	X	X	X	X	X	(Note 1)

Bit	Symbol	Bit Name	Function	R/W
b0	CWR	Cold start-up/warm start-up determine flag (2, 3)	0: Cold start-up 1: Warm start-up	R/W
b1	HWR	Hardware reset detect flag	0: Not detected 1: Detected	R
b2	SWR	Software reset detect flag	0: Not detected 1: Detected	R
b3	WDR	Watchdog timer reset detect flag	0: Not detected 1: Detected	R
b4	—	Reserved bits	When read, the content is undefined.	R
b5	—			
b6	—			
b7	—	Reserved bit	Set to 0.	R/W

Notes:
1. The CWR bit is set to 0 (cold start-up) after power-on or voltage monitor 0 reset. This bit remains unchanged at a hardware reset, software reset, or watchdog timer reset.
2. If 1 is written to the CWR bit by a program, it is set to 1. (Writing 0 does not affect this bit.)
3. When the VW0C0 bit in the VW0C register is set to 0 (voltage monitor 0 reset disabled), the CWR bit value is undefined.

5.1.3 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	—	—	ROMCP1	ROMCR	—	WDTON
After Reset	User Setting Value (Note 1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset. 1: Watchdog timer is stopped after reset.	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	—	Reserved bits	Set to 1.	R/W
b5	—			
b6	LVDAS	Voltage detection 0 circuit start bit (2)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protect mode enabled after reset 1: Count source protect mode disabled after reset	R/W

Notes:

1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS register. If the block including the OFS register is erased, the OFS register is set to FFh.
   When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.
2. To use power-on reset and voltage monitor 0 reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

For a setting example of the OFS register, refer to **13.3.1 Setting Example of Option Function Select Area**.

5.1.4 Option Function Select Register 2 (OFS2)

Address 0FFDBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	WDTRCS1	WDTRCS0	WDTUFS1	WDTUFS0
After Reset	User Setting Value (Note 1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTUFS0	Watchdog timer underflow period set bit	b1 b0 0 0: 03FFh 0 1: 0FFFh 1 0: 1FFFh 1 1: 3FFFh	R/W
b1	WDTUFS1			R/W
b2	WDTRCS0	Watchdog timer refresh acknowledgement period set bit	b3 b2 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100%	R/W
b3	WDTRCS1			R/W
b4	—	Reserved bits	Set to 1.	R/W
b5	—			
b6	—			
b7	—			

Note:

1. The OFS2 register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS2 register. If the block including the OFS2 register is erased, the OFS2 register is set to FFh.
   When blank products are shipped, the OFS2 register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS2 register is the value programmed by the user.

   For a setting example of the OFS2 register, refer to **13.3.1 Setting Example of Option Function Select Area**.

Bits WDTRCS0 and WDTRCS1 (Watchdog Timer Refresh Acknowledgement Period Set Bit)

Assuming that the period from when the watchdog timer starts counting until it underflows is 100%, the refresh acknowledgement period for the watchdog timer can be selected.
For details, refer to **14.3.1.1 Refresh Acknowledgment Period**.

5.2 Hardware Reset

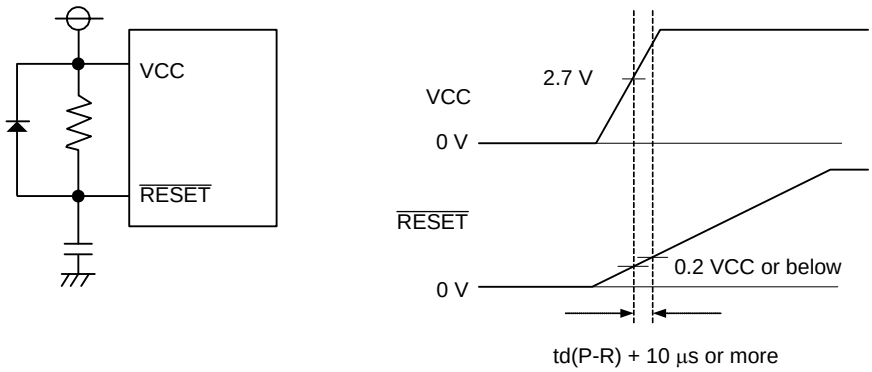
A reset is applied using the $\overline{\text{RESET}}$ pin. When an “L” signal is applied to the $\overline{\text{RESET}}$ pin while the supply voltage meets the recommended operating conditions, pins, CPU, and SFRs are all reset (refer to **Table 5.2 Pin Functions while $\overline{\text{RESET}}$ Pin Level is “L”, Figure 5.2 CPU Register Status after Reset, and Table 4.1 to Table 4.17 SFR Information**). When the input level applied to the $\overline{\text{RESET}}$ pin changes from “L” to “H”, a program is executed beginning with the address indicated by the reset vector. After reset, the low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock.
Refer to **4. Special Function Registers (SFRs)** for the states of the SFRs after reset.
The internal RAM is not reset. If the $\overline{\text{RESET}}$ pin is pulled “L” while writing to the internal RAM is in progress, the contents of internal RAM will be undefined.
Figure 5.4 shows an Example of Hardware Reset Circuit and Operation and Figure 5.5 shows an Example of Hardware Reset Circuit (Usage Example of External Supply Voltage Detection Circuit) and Operation.

5.2.1 When Power Supply is Stable

(1) Apply “L” to the $\overline{\text{RESET}}$ pin.
(2) Wait for 10 µs.
(3) Apply “H” to the $\overline{\text{RESET}}$ pin.

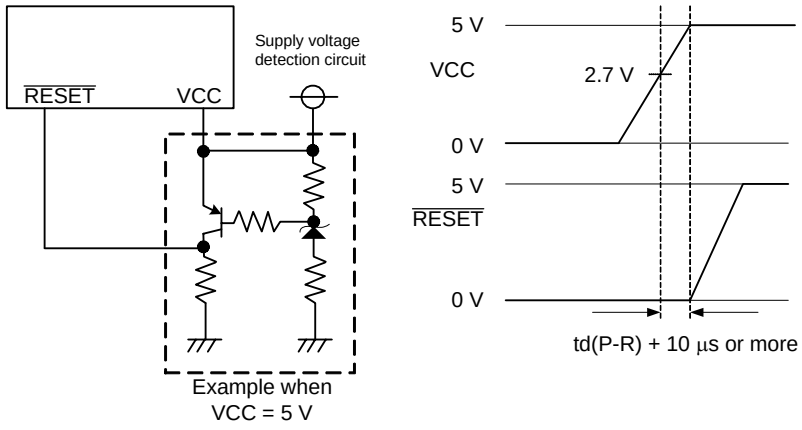
5.2.2 Power On

(1) Apply “L” to the $\overline{\text{RESET}}$ pin.
(2) Let the supply voltage increase until it meets the recommended operating conditions.
(3) Wait for td(P-R) or more to allow the internal power supply to stabilize (refer to **32. Electrical Characteristics**).
(4) Wait for 10 µs.
(5) Apply “H” to the $\overline{\text{RESET}}$ pin.



Note:
1. Refer to **32. Electrical Characteristics**.

Figure 5.4 Example of Hardware Reset Circuit and Operation

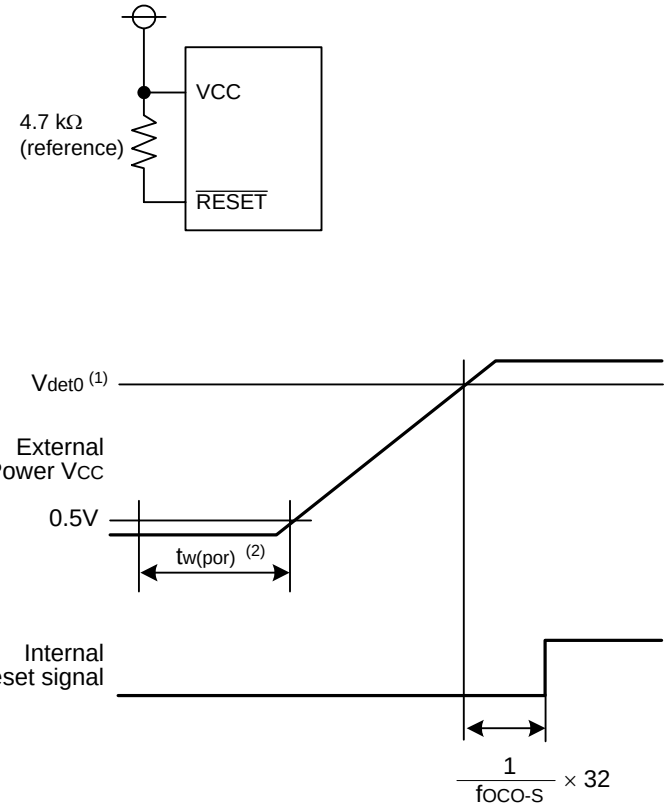


Note:
1. Refer to **32. Electrical Characteristics**.

Figure 5.5 Example of Hardware Reset Circuit (Usage Example of External Supply Voltage Detection Circuit) and Operation

5.3 Power-On Reset Function

When the $\overline{\text{RESET}}$ pin is connected to the VCC pin via a pull-up resistor, and the VCC pin voltage level rises while the rise gradient is trth or more, the power-on reset function is enabled and the MCU resets its pins, CPU, and SFR. When a capacitor is connected to the $\overline{\text{RESET}}$ pin, too, always keep the voltage to the $\overline{\text{RESET}}$ pin 0.8VCC or more. When the input voltage to the VCC pin reaches the Vdet0 level or above, the low-speed on-chip oscillator clock starts counting. When the low-speed on-chip oscillator clock count reaches 32, the internal reset signal is held "H" and the MCU enters the reset sequence (refer to **Figure 5.3**). The low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock after reset.
Refer to **4. Special Function Registers (SFRs)** for the states of the SFR after power-on reset.
After power-on reset, voltage monitor 0 reset is enabled when the LVDAS bit in the OFS register is set to 0 (voltage monitor 0 reset enabled after reset).
Figure 5.6 shows an Example of Power-On Reset Circuit and Operation.



Notes:
1. Vdet0 indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** for details.
2. tw(por) indicates the duration the external power VCC must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain tw(por) for 1 ms or more.
3. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

Figure 5.6 Example of Power-On Reset Circuit and Operation

5.4 Voltage Monitor 0 Reset

A reset is applied using the voltage detection 0 circuit. The voltage detection 0 circuit monitors the input voltage to the VCC pin. The voltage to be monitored is Vdet0.

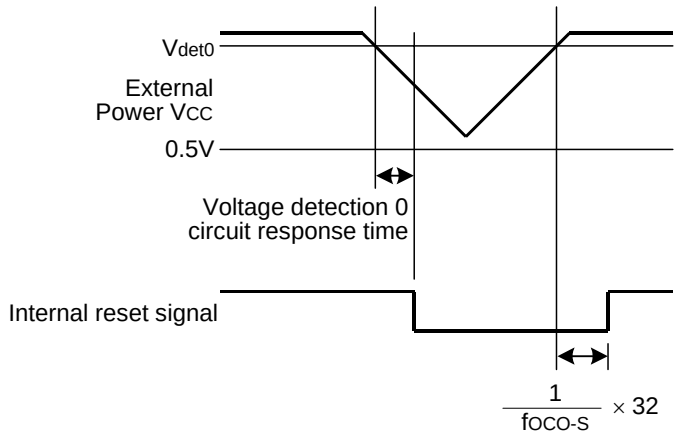
To use voltage monitor 0 reset, set the LVDAS bit in the OFS register to 0.

When the VCC pin voltage reaches the Vdet0 level or below, the internal reset signal is held low. When the VCC pin voltage then reaches the Vdet0 level or above, the MCU enters the reset sequence (refer to **Figure 5.3**) and the low-speed on-chip oscillator clock starts counting. When the low-speed on-chip oscillator clock count reaches 32, the internal reset signal is held high.

After 176 cycles of the CPU clock has elapsed, a program is executed by reading the reset vector. The low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock.

Refer to **3. Memory** for the status of internal RAM after reset and **4. Special Function Registers (SFRs)** for the status of the SFR.

If a voltage monitor 0 reset occurs while writing to internal RAM is in progress, the contents of the internal RAM are undefined. Refer to **6. Voltage Detection Circuit** for details of voltage monitor 0 reset. Refer to **5.1.3 Option Function Select Register (OFS)** for details of the OFS register.



Notes:
1. Vdet0 indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** for details.
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

Figure 5.7 Example of Voltage Monitor 0 Reset Circuit and Operation

5.5 Watchdog Timer Reset

When the PM12 bit in the PM1 register is set to 1 (reset when watchdog timer underflows), the MCU resets its pins, CPU, and SFR if the watchdog timer underflows. Then the program beginning with the address indicated by the reset vector is executed. After reset, the low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock.
Refer to **4. Special Function Registers (SFRs)** for the states of the SFRs after watchdog timer reset.
The internal RAM is not reset. When the watchdog timer underflows, while writing to the internal RAM is in progress the contents of internal RAM are undefined.
The underflow period and refresh acknowledge period for the watchdog timer can be set by bits WDTUFS0 to WDTUFS1 and bits WDTRCS0 to WDTRCS1 in the OFS2 register, respectively.
Refer to **14. Watchdog Timer** for details of the watchdog timer.

5.6 Software Reset

When the PM03 bit in the PM0 register is set to 1 (MCU reset), the MCU resets its pins, CPU, and SFR. The program beginning with the address indicated by the reset vector is executed. After reset, the low-speed on-chip oscillator clock with no division is automatically selected for the CPU clock.
Refer to **4. Special Function Registers (SFRs)** for the states of the SFRs after software reset.
The internal RAM is not reset.

5.7 Cold Start-Up/Warm Start-Up Determination Function

The cold start-up/warm start-up determination function uses the CWR bit in the RSTFR register to determine cold start-up (reset process) at power-on and warm start-up (reset process) when a reset occurred during operation.
The CWR bit is set to 0 (cold start-up) at power-on and also set to 0 at a voltage monitor 0 reset. If 1 is written to the CWR bit by a program, it is set to 1. This bit remains unchanged at a hardware reset, software reset, or watchdog timer reset.
The cold start-up/warm start-up determination function uses voltage monitor 0 reset.
Figure 5.8 shows an Operating Example of Cold Start-Up/Warm Start-Up Function

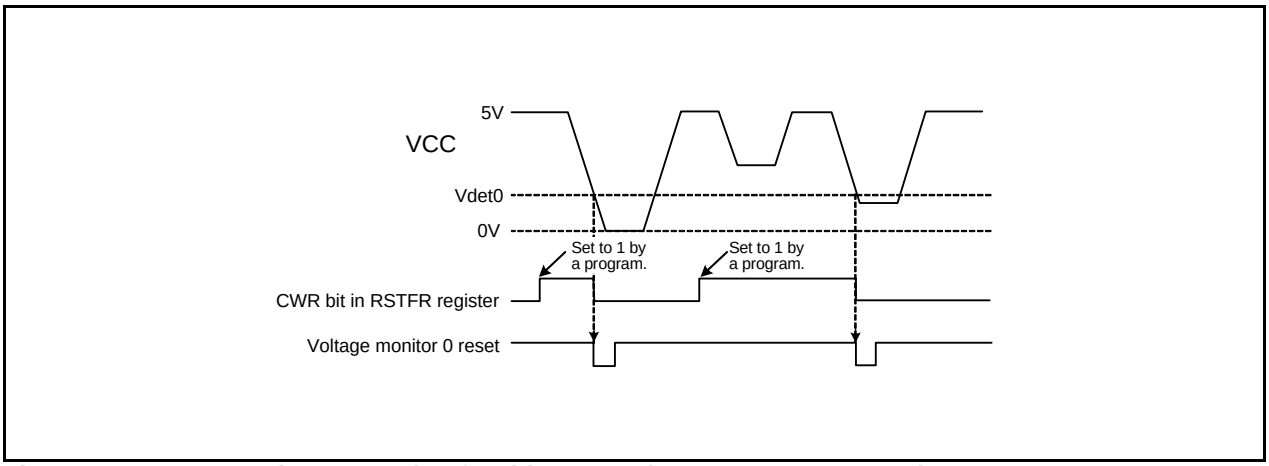


Figure 5.8 Operating Example of Cold Start-Up/Warm Start-Up Function

5.8 Reset Source Determination Function

The RSTFR register can be used to detect whether a hardware reset, software reset, or watchdog timer reset has occurred.
If a hardware reset occurs, the HWR bit is set to 1 (detected). If a software reset occurs, the SWR bit is set to 1 (detected). If a watchdog timer reset occurs, the WDR bit is set to 1 (detected).

6. Voltage Detection Circuit

The voltage detection circuit monitors the voltage input to the VCC pin. This circuit can be used to monitor the VCC input voltage by a program.

6.1 Overview

The detection voltage of voltage detection 0 is fixed level (typical 2.85V).
The detection voltage of voltage detection 1 can be selected among 8 levels using the VD1LS register.
The detection voltage of voltage detection 2 is fixed level (typical 4.00 V).
The voltage monitor 0 reset, and voltage monitor 1 interrupt and voltage monitor 2 interrupt can also be used.

Table 6.1 Voltage Detection Circuit Specifications

Item		Voltage Monitor 0	Voltage Monitor 1	Voltage Monitor 2
VCC monitor	Voltage to monitor	Vdet0	Vdet1	Vdet2
	Detection target	Whether passing through Vdet0 by falling	Whether passing through Vdet1 by rising or falling	Whether passing through Vdet2 by rising or falling
	Detection voltage	fixed level	Selectable among 8 levels using the VD1LS register.	fixed level
	Monitor	None	The VW1C3 bit in the VW1C register	The VCA13 bit in the VCA1 register
			Whether VCC is higher or lower than Vdet1	Whether VCC is higher or lower than Vdet2
Process at voltage detection	Reset	Voltage monitor 0 reset	None	None
		Reset at Vdet0 > VCC; CPU operation restarts at VCC > Vdet0		
	Interrupts	None	Voltage monitor 1 interrupt	Voltage monitor 2 interrupt
			Non-maskable or maskable selectable	Non-maskable or maskable selectable
			Interrupt request at: Vdet1 > VCC and/or VCC > Vdet1	Interrupt request at: Vdet2 > VCC and/or VCC > Vdet2
Digital filter	Switching enable/disable	No digital filter function	Supported	Supported
	Sampling time	—	(fOCO-S divided by n) × 2 n: 1, 2, 4, and 8	(fOCO-S divided by n) × 2 n: 1, 2, 4, and 8

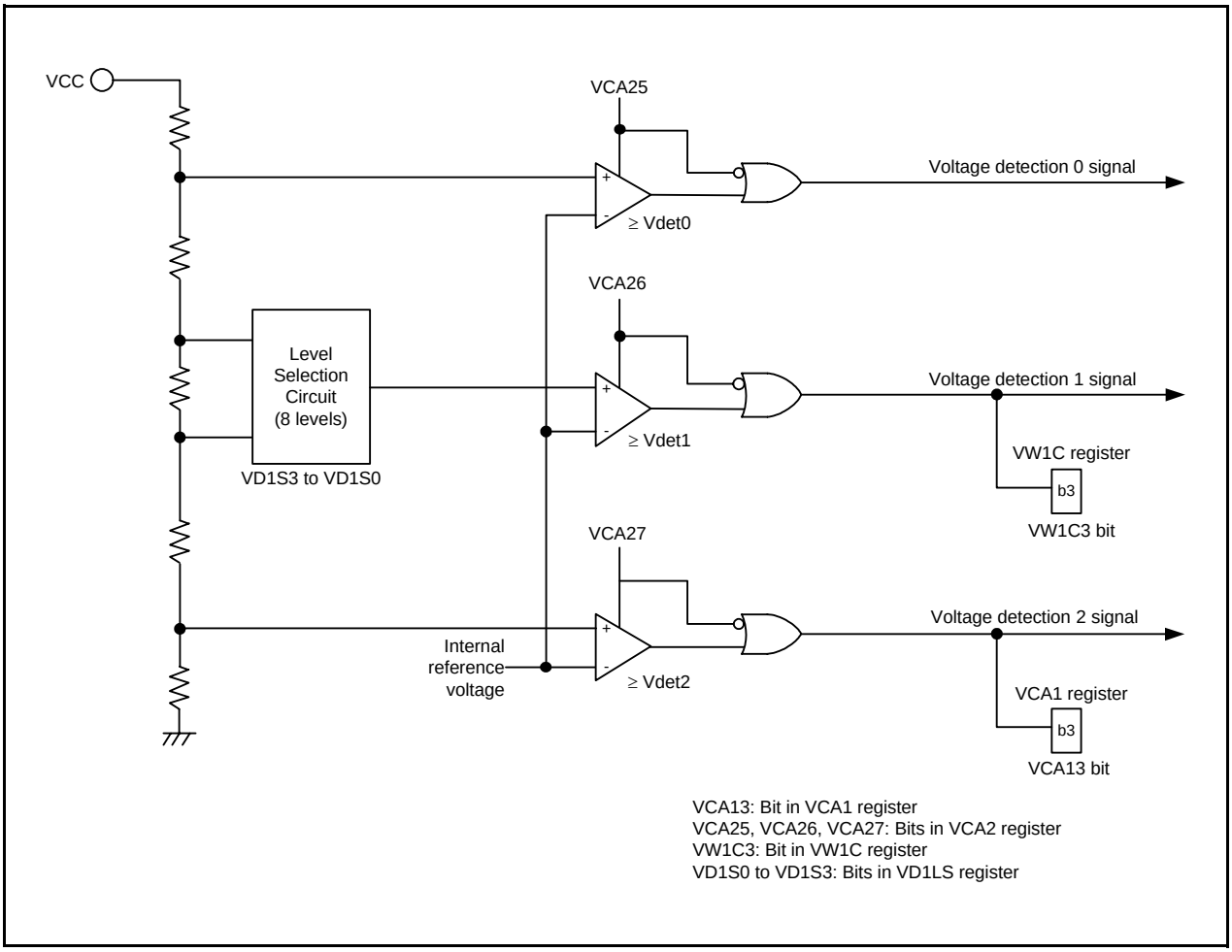


Figure 6.1 Voltage Detection Circuit Block Diagram

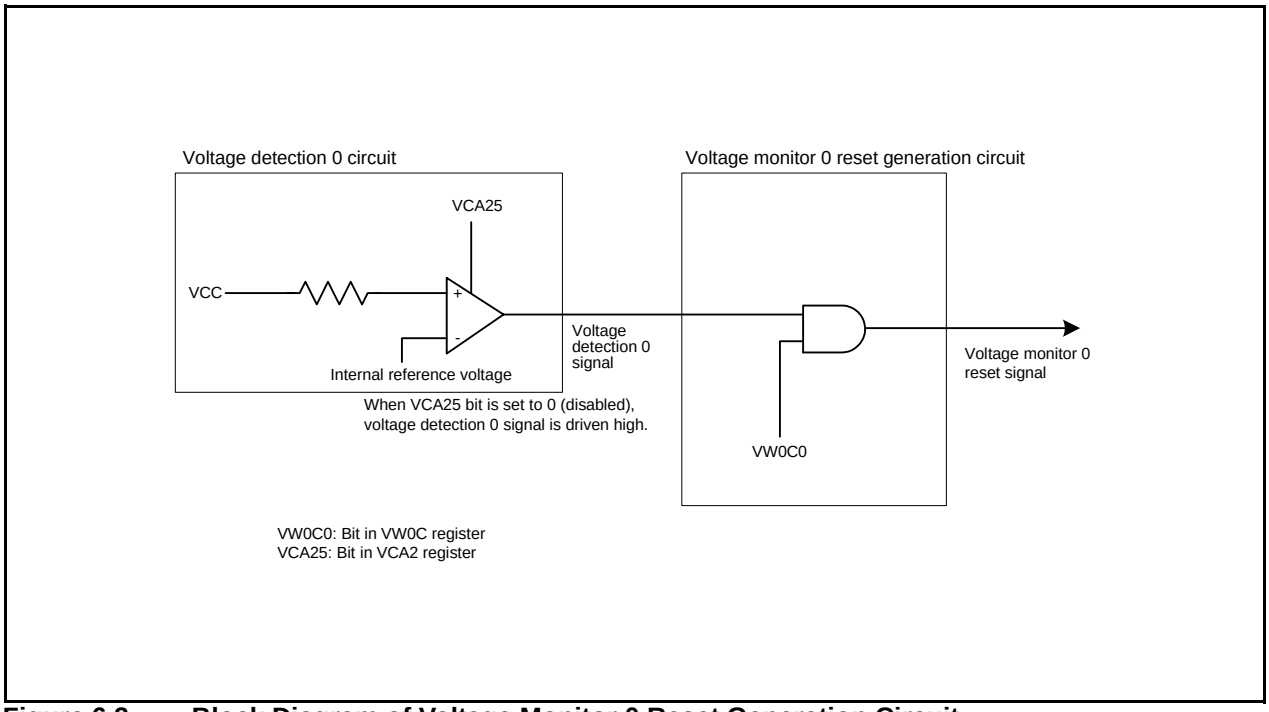


Figure 6.2 Block Diagram of Voltage Monitor 0 Reset Generation Circuit

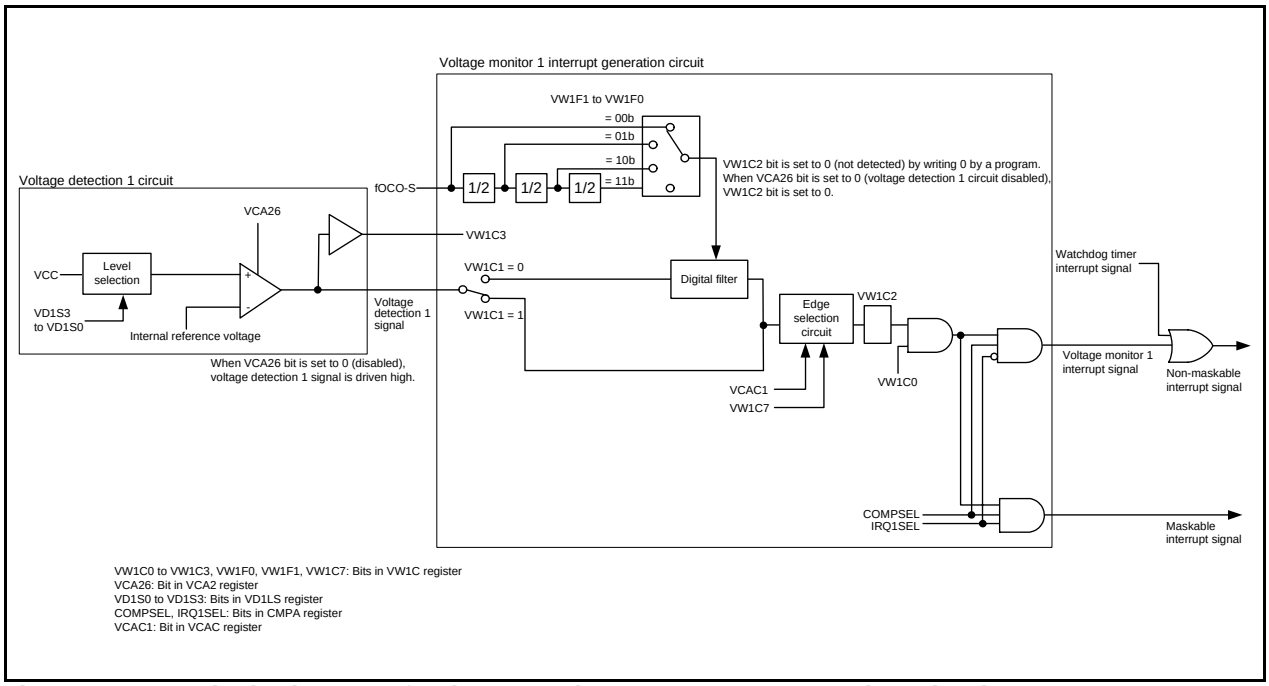


Figure 6.3 Block Diagram of Voltage Monitor 1 Interrupt Generation Circuit

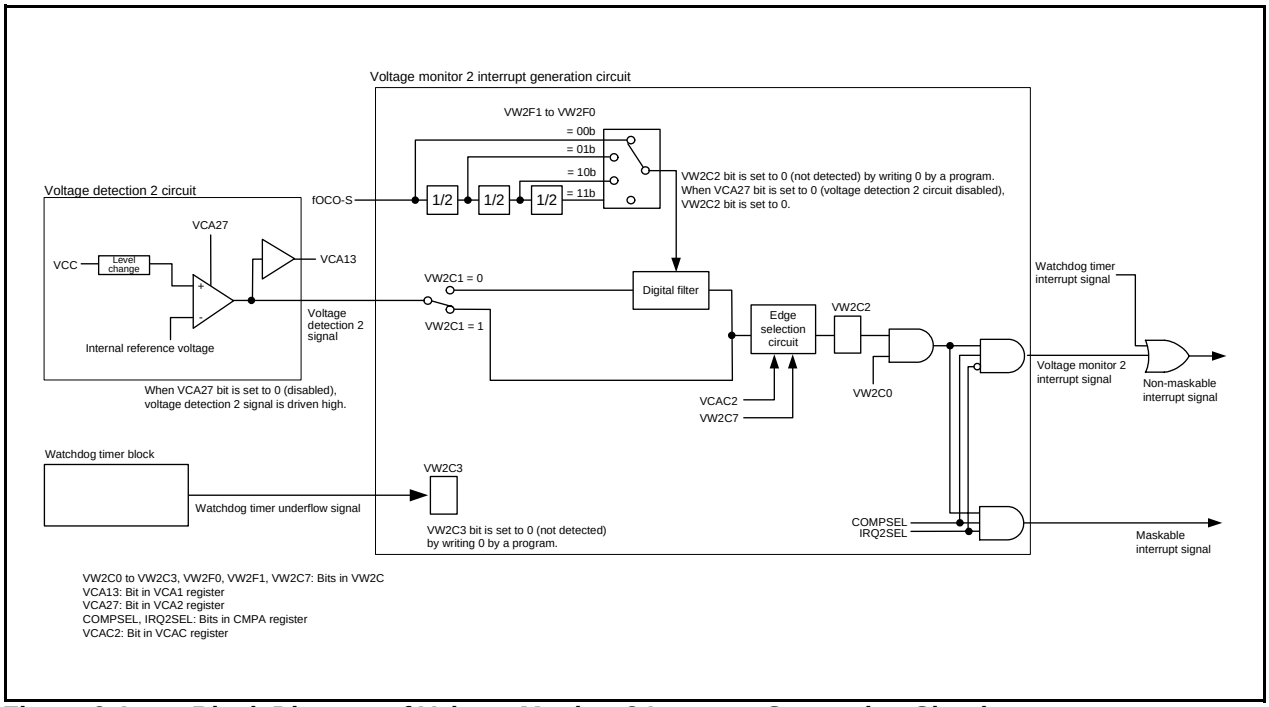


Figure 6.4 Block Diagram of Voltage Monitor 2 Interrupt Generation Circuit

6.2 Registers

6.2.1 Voltage Monitor Circuit Control Register (CMPA)

Address 0030h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	COMPSEL	—	IRQ2SEL	IRQ1SEL	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	—			
b4	IRQ1SEL	Voltage monitor 1 interrupt type select bit (1)	0: Non-maskable interrupt 1: Maskable interrupt	R/W
b5	IRQ2SEL	Voltage monitor 2 interrupt type select bit (2)	0: Non-maskable interrupt 1: Maskable interrupt	R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	COMPSEL	Voltage monitor interrupt type selection enable bit (1, 2)	0: Bits IRQ1SEL and IRQ2SEL disabled 1: Bits IRQ1SEL and IRQ2SEL enabled	R/W

Notes:
1. When the VW1C0 bit in the VW1C register is set to 1 (enabled), do not set bits IRQ1SEL and COMPSEL simultaneously (with one instruction).
2. When the VW2C0 bit in the VW2C register is set to 1 (enabled), do not set bits IRQ2SEL and COMPSEL simultaneously (with one instruction).

6.2.2 Voltage Monitor Circuit Edge Select Register (VCAC)

Address 0031h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	VCAC2	VCAC1	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	VCAC1	Voltage monitor 1 circuit edge select bit (1)	0: One edge 1: Both edges	R/W
b2	VCAC2	Voltage monitor 2 circuit edge select bit (2)	0: One edge 1: Both edges	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Notes:
1. When the VCAC1 bit is set to 0 (one edge), the VW1C7 bit in the VW1C register is enabled. Set the VW1C7 bit after setting the VCAC1 bit to 0.
2. When the VCAC2 bit is set to 0 (one edge), the VW2C7 bit in the VW2C register is enabled. Set the VW2C7 bit after setting the VCAC2 bit to 0.

6.2.3 Voltage Detect Register 1 (VCA1)

Address 0033h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	VCA13	—	—	—
After Reset	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	VCA13	Voltage detection 2 signal monitor flag (1)	0: VCC < Vdet2 1: VCC ≥ Vdet2 or voltage detection 2 circuit disabled	R
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

Note:
1. When the VCA27 bit in the VCA2 register is set to 1 (voltage detection 2 circuit enabled), the VCA13 bit is enabled.
   When the VCA27 bit in the VCA2 register is set to 0 (voltage detection 2 circuit disabled), the VCA13 bit is set to 1 (VCC ≥ Vdet2).

6.2.4 Voltage Detect Register 2 (VCA2)

Address 0034h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VCA27	VCA26	VCA25	—	—	—	—	VCA20
After Reset	0	0	0	0	0	0	0	0

The above applies when the LVDAS bit in the OFS register is set to 1.

After Reset	0	0	1	0	0	0	0	0

The above applies when the LVDAS bit in the OFS register is set to 0.

Bit	Symbol	Bit Name	Function	R/W
b0	VCA20	Internal power low consumption enable bit (1)	0: Low consumption disabled 1: Low consumption enabled (2)	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	—			
b5	VCA25	Voltage detection 0 enable bit (3)	0: Voltage detection 0 circuit disabled 1: Voltage detection 0 circuit enabled	R/W
b6	VCA26	Voltage detection 1 enable bit (4)	0: Voltage detection 1 circuit disabled 1: Voltage detection 1 circuit enabled	R/W
b7	VCA27	Voltage detection 2 enable bit (5)	0: Voltage detection 2 circuit disabled 1: Voltage detection 2 circuit enabled	R/W

Notes:
1. Use the VCA20 bit only when the MCU enters wait mode. To set the VCA20 bit, follow the procedure shown in **Figure 9.3 Procedure for Reducing Internal Power Consumption Using VCA20 bit**.
2. When the VCA20 bit is set to 1 (low consumption enabled), do not set the CM10 bit in the CM1 register to 1 (stop mode).
3. When writing to the VCA25 bit, set a value after reset.
4. To use the voltage detection 1 interrupt or the VW1C3 bit in the VW1C register, set the VCA26 bit to 1. After the VCA26 bit is set to 1 from 0, allow td(E-A) to elapse before the voltage detection 1 circuit starts operation.
5. To use the voltage detection 2 interrupt or the VCA13 bit in the VCA1 register, set the VCA27 bit to 1. After the VCA27 bit is set to 1 from 0, allow td(E-A) to elapse before the voltage detection 2 circuit starts operation.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VCA2 register.

6.2.5 Voltage Detection 1 Level Select Register (VD1LS)

Address 0036h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	VD1S3	VD1S2	VD1S1	VD1S0
After Reset	0	0	0	0	0	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	VD1S0	Voltage detection 1 level select bit (Reference voltage when the voltage falls)	b3 b2 b1 b0 0 0 0 0: Do not set. 0 0 0 1: Do not set. 0 0 1 0: Do not set. 0 0 1 1: Do not set. 0 1 0 0: Do not set. 0 1 0 1: Do not set. 0 1 1 0: Do not set. 0 1 1 1: 3.25 V (Vdet1_7) 1 0 0 0: 3.40 V (Vdet1_8) 1 0 0 1: 3.55 V (Vdet1_9) 1 0 1 0: 3.70 V (Vdet1_A) 1 0 1 1: 3.85 V (Vdet1_B) 1 1 0 0: 4.00 V (Vdet1_C) 1 1 0 1: 4.15 V (Vdet1_D) 1 1 1 0: 4.30 V (Vdet1_E) 1 1 1 1: Do not set.	R/W
b1	VD1S1			R/W
b2	VD1S2			R/W
b3	VD1S3			R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VD1LS register.

6.2.6 Voltage Monitor 0 Circuit Control Register (VW0C)

Address 0038h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	VW0C0
After Reset	1	1	0	0	X	0	1	0

The above applies when the LVDAS bit in the OFS register is set to 1.

After Reset	1	1	0	0	X	0	1	1

The above applies when the LVDAS bit in the OFS register is set to 0.

Bit	Symbol	Bit Name	Function	R/W
b0	VW0C0	Voltage monitor 0 reset enable bit (1)	0: Disabled 1: Enabled	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	—	Reserved bit	When read, the content is undefined.	R
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—	Reserved bits	Set to 1.	R/W
b7	—			

Note:
1. The VW0C0 bit is enabled when the VCA25 bit in the VCA2 register is set to 1 (voltage detection 0 circuit enabled). When writing to the VW0C0 bit, set a value after reset.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before writing the VW0C register.

6.2.7 Voltage Monitor 1 Circuit Control Register (VW1C)

Address 0039h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VW1C7	—	VW1F1	VW1F0	VW1C3	VW1C2	VW1C1	VW1C0
After Reset	1	0	0	0	1	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	VW1C0	Voltage monitor 1 interrupt enable bit (1)	0: Disabled 1: Enabled	R/W
b1	VW1C1	Voltage monitor 1 digital filter disable mode select bit (2, 6)	0: Digital filter enabled mode (digital filter circuit enabled) 1: Digital filter disable mode (digital filter circuit disabled)	R/W
b2	VW1C2	Voltage change detection flag (3, 4)	0: Not detected 1: Vdet1 passing detected	R/W
b3	VW1C3	Voltage detection 1 signal monitor flag (3)	0: VCC < Vdet1 1: VCC ≥ Vdet1 or voltage detection 1 circuit disabled	R
b4	VW1F0	Sampling clock select bit (6)	b5 b4 0 0: fOCO-S divided by 1 0 1: fOCO-S divided by 2 1 0: fOCO-S divided by 4 1 1: fOCO-S divided by 8	R/W
b5	VW1F1			R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	VW1C7	Voltage monitor 1 interrupt generation condition select bit (5)	0: When VCC reaches Vdet1 or above. 1: When VCC reaches Vdet1 or below.	R/W

Notes:

1. The VW1C0 is enabled when the VCA26 bit in the VCA2 register is set to 1 (voltage detection 1 circuit enabled). Set the VW1C0 bit to 0 (disabled) when the VCA26 bit is set to 0 (voltage detection 1 circuit disabled).
   To set the VW0C0 bit to 1 (enabled), follow the procedure shown in **Table 6.2 Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt**.
2. When using the digital filter (while the VW1C1 bit is 0), set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on).
   To use the voltage monitor 1 interrupt to exit stop mode, set the VW1C1 bit in the VW1C register to 1 (digital filter disabled).
3. Bits VW1C2 and VW1C3 are enabled when the VCA26 bit in the VCA2 register is set to 1(voltage detection 1 circuit enabled).
4. Set the VW1C2 bit to 0 by a program. When 0 is written by a program, this bit is set to 0 (and remains unchanged even if 1 is written to it).
5. The VW1C7 bit is enabled when the VCAC1 bit in the VCAC register is set to 0 (one edge). After setting the VCAC1 bit to 0, set the VW1C7 bit.
6. When the VW1C0 bit is set to 1 (enabled), do not set the VW1C1 bit and bits VW1F1 and VW1F0 simultaneously (with one instruction).

Set the PRC3 bit in the PRCR register to 1 (write enabled) before writing the VW1C register.
Rewriting the VW1C register may set the VW1C2 bit to 1. Set the VW1C2 bit to 0 after rewriting the VW1C register.

6.2.8 Voltage Monitor 2 Circuit Control Register (VW2C)

Address 003Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VW2C7	—	VW2F1	VW2F0	VW2C3	VW2C2	VW2C1	VW2C0
After Reset	1	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	VW2C0	Voltage monitor 2 interrupt enable bit (1)	0: Disabled 1: Enabled	R/W
b1	VW2C1	Voltage monitor 2 digital filter disable mode select bit (2, 6)	0: Digital filter enable mode (digital filter circuit enabled) 1: Digital filter disable mode (digital filter circuit disabled)	R/W
b2	VW2C2	Voltage change detection flag (3, 4)	0: Not detected 1: Vdet2 passing detected	R/W
b3	VW2C3	WDT detection monitor flag (4)	0: Not detected 1: Detected	R/W
b4	VW2F0	Sampling clock select bit (6)	b5 b4	R/W
b5	VW2F1		0 0: fOCO-S divided by 1 0 1: fOCO-S divided by 2 1 0: fOCO-S divided by 4 1 1: fOCO-S divided by 8	R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	VW2C7	Voltage monitor 2 interrupt generation condition select bit (5)	0: When VCC reaches Vdet2 or above. 1: When VCC reaches Vdet2 or below.	R/W

Notes:

1. The VW2C0 is enabled when the VCA27 bit in the VCA2 register is set to 1 (voltage detection 2 circuit enabled). Set the VW2C0 bit to 0 (disabled) when the VCA27 bit is set to 0 (voltage detection 2 circuit disabled).
   To set the VW2C0 bit to 1 (enabled), follow the procedure shown in **Table 6.3 Procedure for Setting Bits Associated with Voltage Monitor 2 Interrupt**.
2. When using the digital filter (while the VW2C1 bit is 0), set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on).
   To use the voltage monitor 2 interrupt to exit stop mode, set the VW2C1 bit in the VW2C register to 1 (digital filter disabled).
3. The VW2C2 bit is enabled when the VCA27 bit in the VCA2 register is set to 1 (voltage detection 2 circuit enabled).
4. Set this bit to 0 by a program. When 0 is written by a program, this bit is set to 0 (and remains unchanged even if 1 is written to it).
5. The VW2C7 bit is enabled when the VCAC2 bit in the VCAC register is set to 0 (one edge). After setting the VCAC2 bit to 0, set the VW2C7 bit.
6. When the VW2C0 bit is set to 1 (enabled), do not set the VW2C1 bit and bits VW2F1 and VW2F0 simultaneously (with one instruction).

   Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VW2C register.
   Rewriting the VW2C register may set the VW2C2 bit to 1. After rewriting this register, set the VW2C2 bit to 0.

6.2.9 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	—	—	ROMCP1	ROMCR	—	WDTON
After Reset	User Setting Value (Note 1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset. 1: Watchdog timer is stopped after reset.	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	—	Reserved bits	Set to 1.	R/W
b5	—			
b6	LVDAS	Voltage detection 0 circuit start bit (2)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protect mode enabled after reset 1: Count source protect mode disabled after reset	R/W

Notes:

1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS register. If the block including the OFS register is erased, the OFS register is set to FFh.
   When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.
2. To use power-on reset and voltage monitor 0 reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

For a setting example of the OFS register, refer to **13.3.1 Setting Example of Option Function Select Area**.

6.3 VCC Input Voltage

6.3.1 Monitoring Vdet0

Vdet0 cannot be monitored.

6.3.2 Monitoring Vdet1

Once the following settings are made, the comparison result of voltage monitor 1 can be monitored by the VW1C3 bit in the VW1C register after td(E-A) has elapsed (refer to **32. Electrical Characteristics**).

(1) Set bits VD1S3 to VD1S0 in the VD1LS register (voltage detection 1 detection voltage).
(2) Set the VCA26 bit in the VCA2 register to 1 (voltage detection 1 circuit enabled).

6.3.3 Monitoring Vdet2

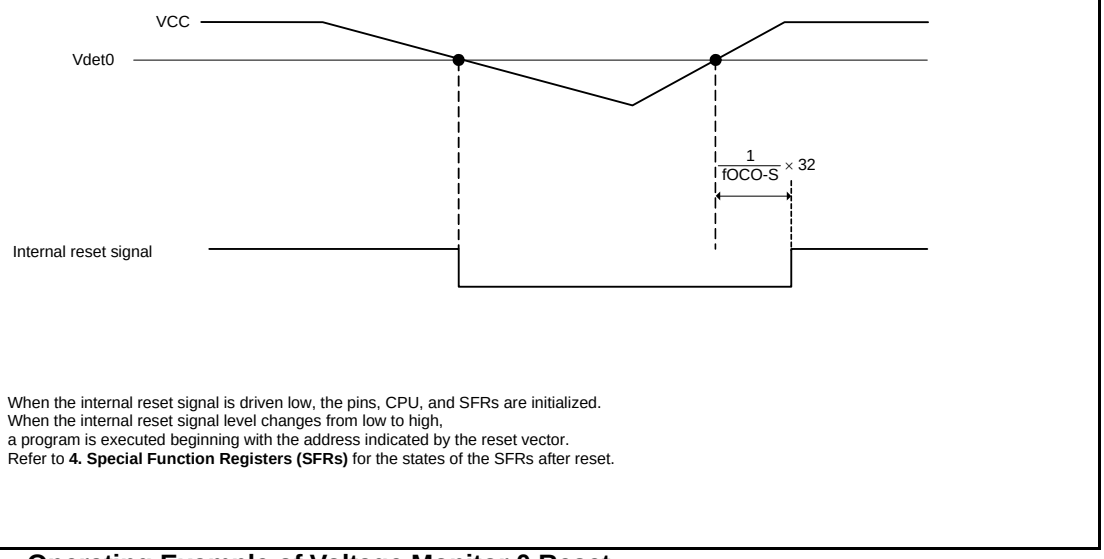
Once the following settings are made, the comparison result of voltage monitor 2 can be monitored by the VCA13 bit in the VCA1 register after td(E-A) has elapsed (refer to **32. Electrical Characteristics**).

- Set the VCA27 bit in the VCA2 register to 1 (voltage detection 2 circuit enabled).

6.4 Voltage Monitor 0 Reset

To use voltage monitor 0 reset, set the LVDAS bit in the OFS register to 0 (voltage monitor 0 reset enabled after reset).

Figure 6.5 shows an Operating Example of Voltage Monitor 0 Reset.



When the internal reset signal is driven low, the pins, CPU, and SFRs are initialized.
When the internal reset signal level changes from low to high,
a program is executed beginning with the address indicated by the reset vector.
Refer to **4. Special Function Registers (SFRs)** for the states of the SFRs after reset.

Figure 6.5 Operating Example of Voltage Monitor 0 Reset

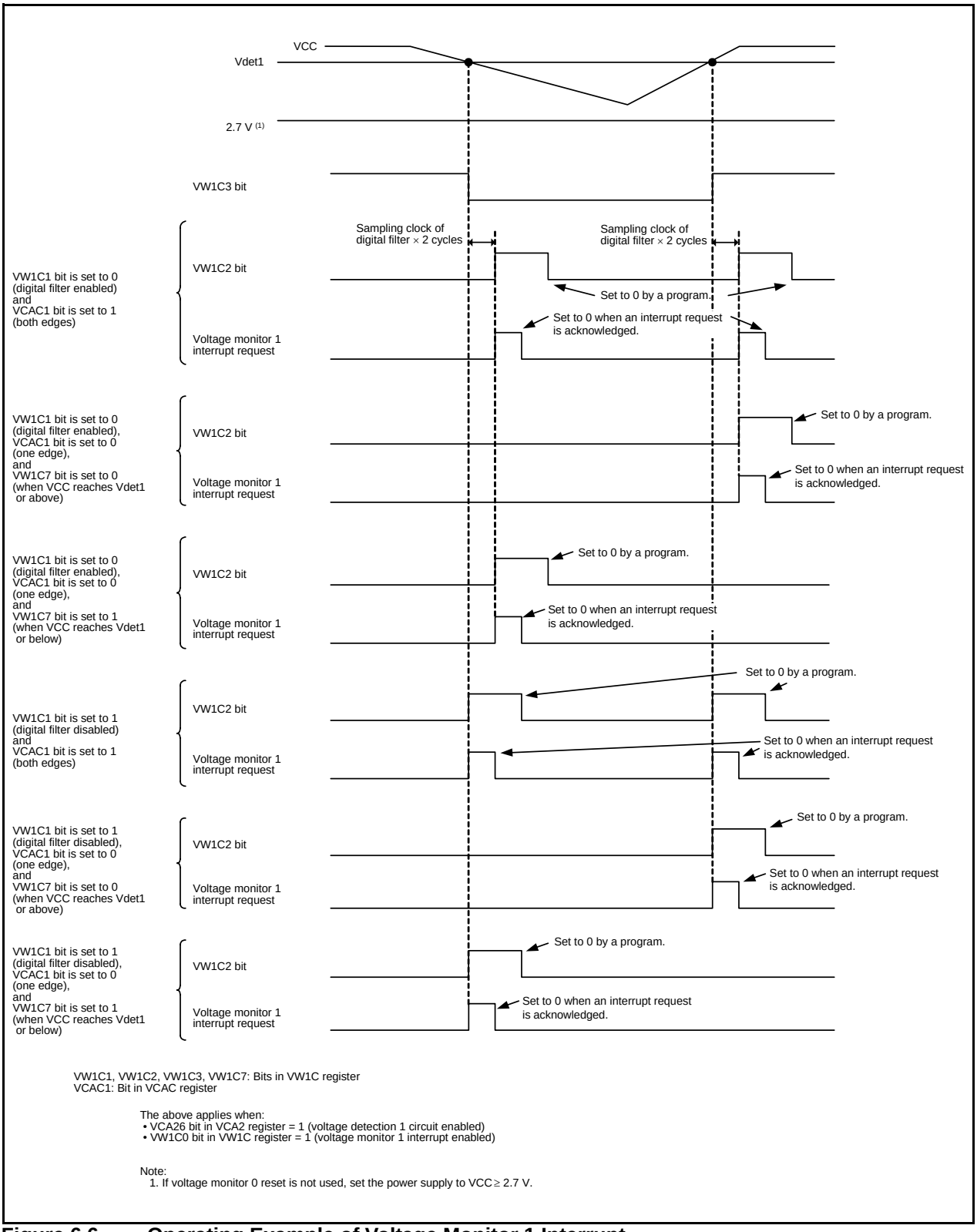
6.5 Voltage Monitor 1 Interrupt

Table 6.2 lists the Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt. Figure 6.6 shows an Operating Example of Voltage Monitor 1 Interrupt.
To use the voltage monitor 1 interrupt to exit stop mode, set the VW1C1 bit in the VW1C register to 1 (digital filter disabled).

Table 6.2 Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt

Step	When Using Digital Filter	When Using No Digital Filter
1	Select the voltage detection 1 detection voltage by bits VD1S3 to VD1S0 in the VD1LS register.	
2	Set the VCA26 bit in the VCA2 register to 1 (voltage detection 1 circuit enabled).	
3	Wait for td(E-A).	
4	Set the COMPSEL bit in the CMPA register to 1.	
5 (1)	Select the interrupt type by the IRQ1SEL in the CMPA register.	
6	Select the sampling clock of the digital filter by bits VW1F0 and VW1F1 in the VW1C register.	Set the VW1C1 bit in the VW1C register to 1 (digital filter disabled).
7 (2)	Set the VW1C1 bit in the VW1C register to 0 (digital filter enabled).	–
8	Select the interrupt request timing by the VCAC1 bit in the VCAC register and the VW1C7 bit in the VW1C register.	
9	Set the VW1C2 bit in the VW1C register to 0.	
10	Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on)	–
11	Wait for 2 cycles of the sampling clock of the digital filter	– (No wait time required)
12 (3)	Set the VW1C0 bit in the VW1C register to 1 (voltage monitor 1 interrupt enabled)	

Notes:
1. When the VW1C0 bit is set to 0, steps 4 and 5 can be executed simultaneously (with one instruction).
2. When the VW1C0 bit is set to 0, steps 6 and 7 can be executed simultaneously (with one instruction).
3. When the voltage detection 1 circuit is enabled while the voltage monitor 1 interrupt is disabled, low voltage is detected and the VW1C2 bit becomes 1.
   When low voltage is detected after the voltage detection 1 circuit is enabled until an interrupt is enabled for the setting procedure of bits associated with voltage monitor 1 interrupt, an interrupt is not generated. After an interrupt is enabled, read the VW1C2 bit. When the bit is read as 1, perform the process that occurs when low voltage is detected.



VW1C1, VW1C2, VW1C3, VW1C7: Bits in VW1C register
VCAC1: Bit in VCAC register

The above applies when:
- VCA26 bit in VCA2 register = 1 (voltage detection 1 circuit enabled)
- VW1C0 bit in VW1C register = 1 (voltage monitor 1 interrupt enabled)

Note:
1. If voltage monitor 0 reset is not used, set the power supply to VCC ≥ 2.7 V.

Figure 6.6 Operating Example of Voltage Monitor 1 Interrupt

6.6 Voltage Monitor 2 Interrupt

Table 6.3 lists the Procedure for Setting Bits Associated with Voltage Monitor 2 Interrupt. Figure 6.7 shows an Operating Example of Voltage Monitor 2 Interrupt.
To use the voltage monitor 2 interrupt to exit stop mode, set the VW2C1 bit in the VW2C register to 1 (digital filter disabled).

Table 6.3 Procedure for Setting Bits Associated with Voltage Monitor 2 Interrupt

Step	When Using Digital Filter	When Using No Digital Filter
1	Set the VCA27 bit in the VCA2 register to 1 (voltage detection 2 circuit enabled).	
2	Wait for td(E-A).	
3	Set the COMPSEL bit in the CMPA register to 1.	
4 (1)	Select the interrupt type by the IRQ2SEL in the CMPA register.	
5	Select the sampling clock of the digital filter by bits VW2F0 and VW2F1 in the VW2C register.	Set the VW2C1 bit in the VW2C register to 1 (digital filter disabled).
6 (2)	Set the VW2C1 bit in the VW2C register to 0 (digital filter enabled).	–
7	Select the interrupt request timing by the VCAC2 bit in the VCAC register and the VW2C7 bit in the VW2C register.	
8	Set the VW2C2 bit in the VW2C register to 0.	
9	Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on).	–
10	Wait for 2 cycles of the sampling clock of the digital filter.	– (No wait time required)
11 (3)	Set the VW2C0 bit in the VW2C register to 1 (voltage monitor 2 interrupt enabled).	

Notes:
1. When the VW2C0 bit is set to 0, steps 3 and 4 can be executed simultaneously (with one instruction).
2. When the VW2C0 bit is set to 0, steps 5 and 6 can be executed simultaneously (with one instruction).
3. When the voltage detection 2 circuit is enabled while the voltage monitor 2 interrupt is disabled, low voltage is detected and the VW2C2 bit becomes 1.
   When low voltage is detected after the voltage detection 2 circuit is enabled until an interrupt is enabled for the setting procedure of bits associated with voltage monitor 2 interrupt, an interrupt is not generated. After an interrupt is enabled, read the VW2C2 bit. When the bit is read as 1, perform the process that occurs when low voltage is detected.

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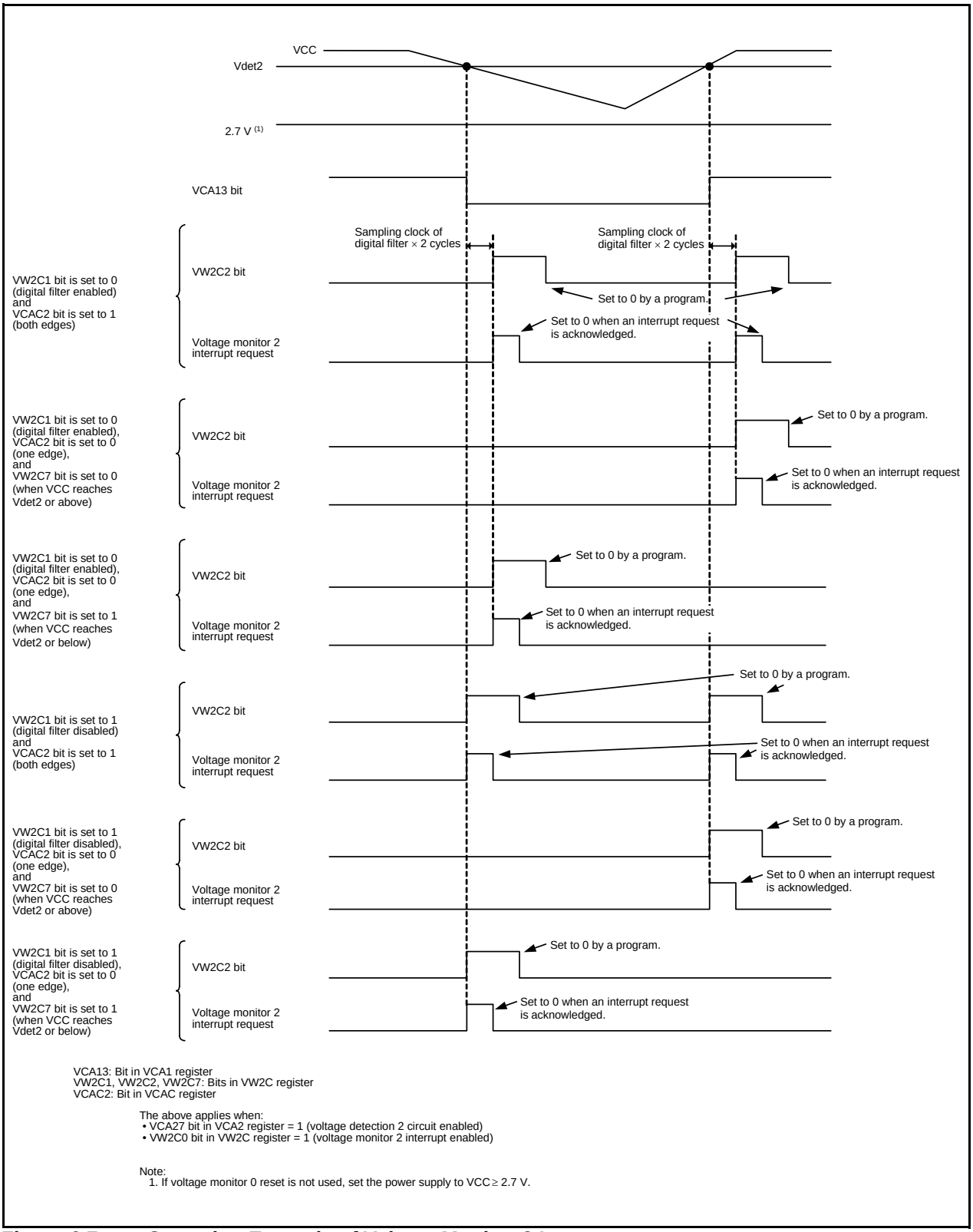


VCA13: Bit in VCA1 register
VW2C1, VW2C2, VW2C7: Bits in VW2C register
VCAC2: Bit in VCAC register

The above applies when:
- VCA27 bit in VCA2 register = 1 (voltage detection 2 circuit enabled)
- VW2C0 bit in VW2C register = 1 (voltage monitor 2 interrupt enabled)

Note:
1. If voltage monitor 0 reset is not used, set the power supply to VCC ≥ 2.7 V.

Figure 6.7 Operating Example of Voltage Monitor 2 Interrupt

7. I/O Ports

There are 75 I/O ports P0 to P3, P4_3 to P4_7, P5 to P8, and P9_0 to P9_5 (P4_6 and P4_7 can be used as I/O ports if the XIN clock oscillation circuit is not used.).
If the A/D converter is not used, P4_2 can be used as an input-only port.
Table 7.1 lists an Overview of I/O Ports.

Table 7.1 Overview of I/O Ports

Ports	I/O	Type of Output	I/O Setting	Internal Pull-Up Resister	Input Level Switch
P0 to P3, P5 to P8	I/O	CMOS3 state	Set in 1-bit units	Set in 4-bit units (1)	Set in 8-bit units (2)
P9_0 to P9_3	I/O	CMOS3 state	Set in 1-bit units	Set in 4-bit units (1)	Set in 6-bit units (2)
P9_4, P9_5	I/O	CMOS3 state	Set in 1-bit units	Set in 2-bit units (1)	
P4_3	I/O	CMOS3 state	Set in 1-bit units	Set in 1-bit units (1)	
P4_4, P4_5, P4_6 (3), P4_7 (3)	I/O	CMOS3 state	Set in 1-bit units	Set in 4-bit units (1)	
P4_2 (4)	I	(No output function)	None	None	

Notes:
1. In input mode, whether an internal pull-up resistor is connected or not can be selected by registers PUR0, PUR1, and PUR2.
2. The input threshold value can be selected among three voltage levels (0.35 VCC, 0.50 VCC, and 0.70 VCC) by registers VLT0, VLT1, and VLT2.
3. When the XIN clock oscillation circuit is not used, these ports can be used as I/O ports.
4. When the A/D converter is not used, this port can be used as an input-only ports.

7.1 Functions of I/O Ports

The PDi_j (j = 0 to 7) bit in the PDi (i = 0 to 9) register controls I/O of the ports P0 to P3, P4_3 to P4_7, P5 to P8, and P9_0 to P9_5. The Pi register consists of a port latch to hold output data and a circuit to read pin states.
Figures 7.1 to 7.21 show the Configurations of I/O Ports. Table 7.2 lists the Functions of I/O Ports.

Table 7.2 Functions of I/O Ports

Operation When Accessing Pi Register	Value of PDi_j Bit in PDi Register (1)	
	When PDi_j Bit is Set to 0 (Input Mode)	When PDi_j Bit is Set to 1 (Output Mode)
Read	Read the pin input level.	Read the port latch.
Write	Write to the port latch.	Write to the port latch. The value written to the port latch is output from the pin.

i = 0 to 9, j = 0 to 7
Note:
1. Nothing is assigned to bits PD4_0 to PD4_2, PD9_6, and PD9_7

7.2 Effect on Peripheral Functions

I/O ports function as I/O ports for peripheral functions (Refer to **Table 1.13 Pin Name Information by Pin Number (1)** and **Table 1.14 Pin Name Information by Pin Number (2)**).
Table 7.3 lists the Setting of PDi_j Bit when Functioning as I/O Ports for Peripheral Functions (i = 0 to 9, j = 0 to 7).
Refer to the description of each function for information on how to set peripheral functions.

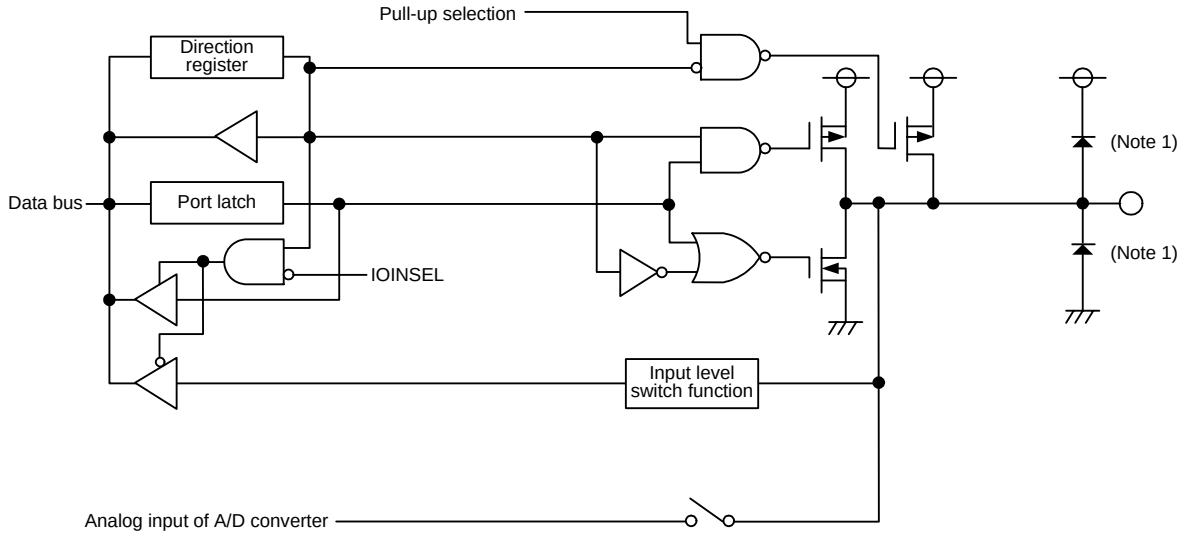
Table 7.3 Setting of PDi_j Bit when Functioning as I/O Ports for Peripheral Functions (i = 0 to 9, j = 0 to 7)

I/O of Peripheral Function	PDi_j Bit Settings for Shared Pin Function
Input	Set this bit to 0 (input mode).
Output	This bit can be set to either 0 or 1 (output regardless of the port setting).

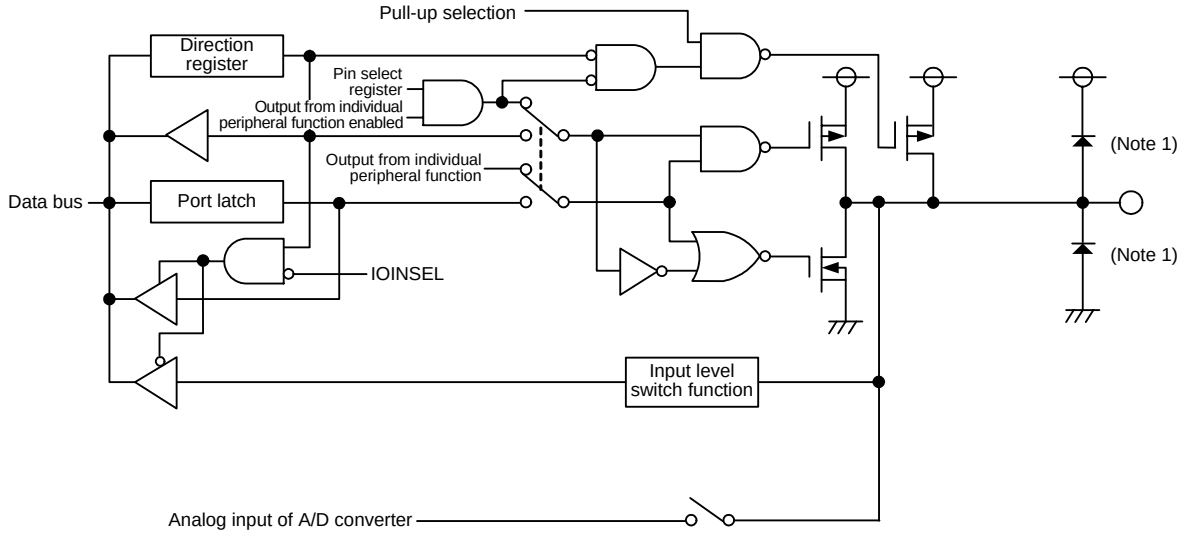
7.3 Pins Other than I/O Ports

Figure 7.22 shows the Configuration of I/O Pins.

P0_0, P0_5 to P0_7



P0_1, P0_4

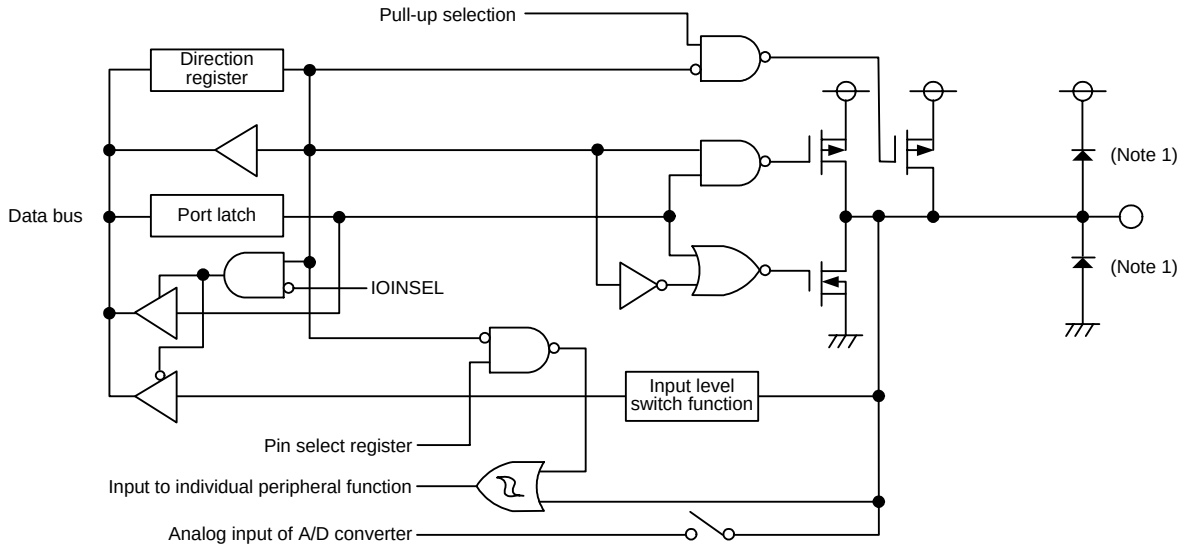


Note:
1. ⊣◀⊢ symbolizes a parasitic diode.
Ensure the input voltage to each port does not exceed VCC.

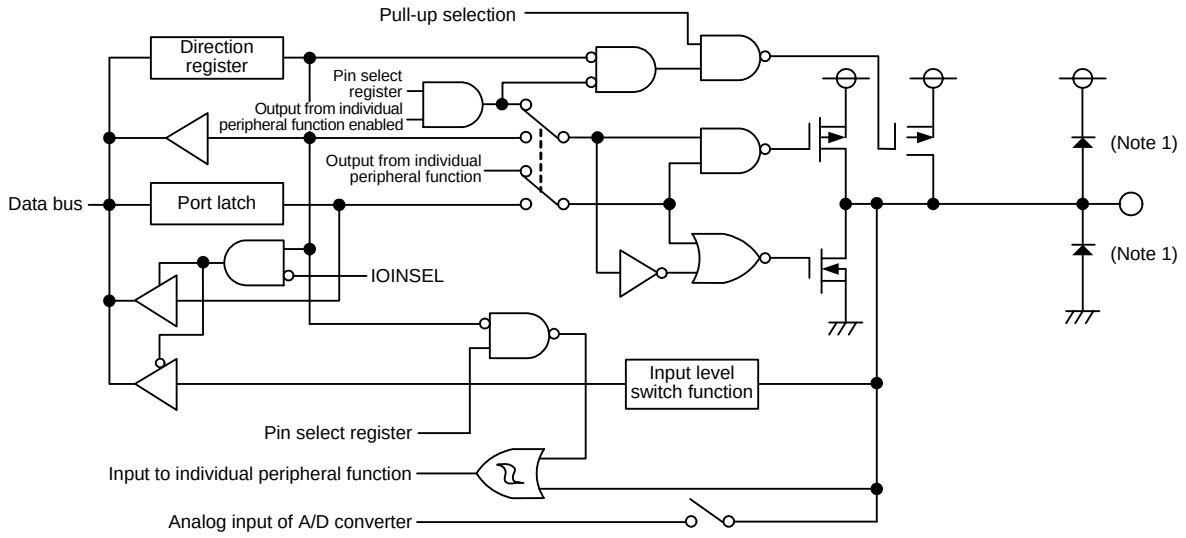
IOINSEL: Bit in PINSR register

Figure 7.1 Configuration of I/O Ports (1)

P0_2



P0_3



Note:
1. ⟵| symbolizes a parasitic diode.
Ensure the input voltage to each port does not exceed VCC.

IOINSEL: Bit in PINSR register

Figure 7.2 Configuration of I/O Ports (2)

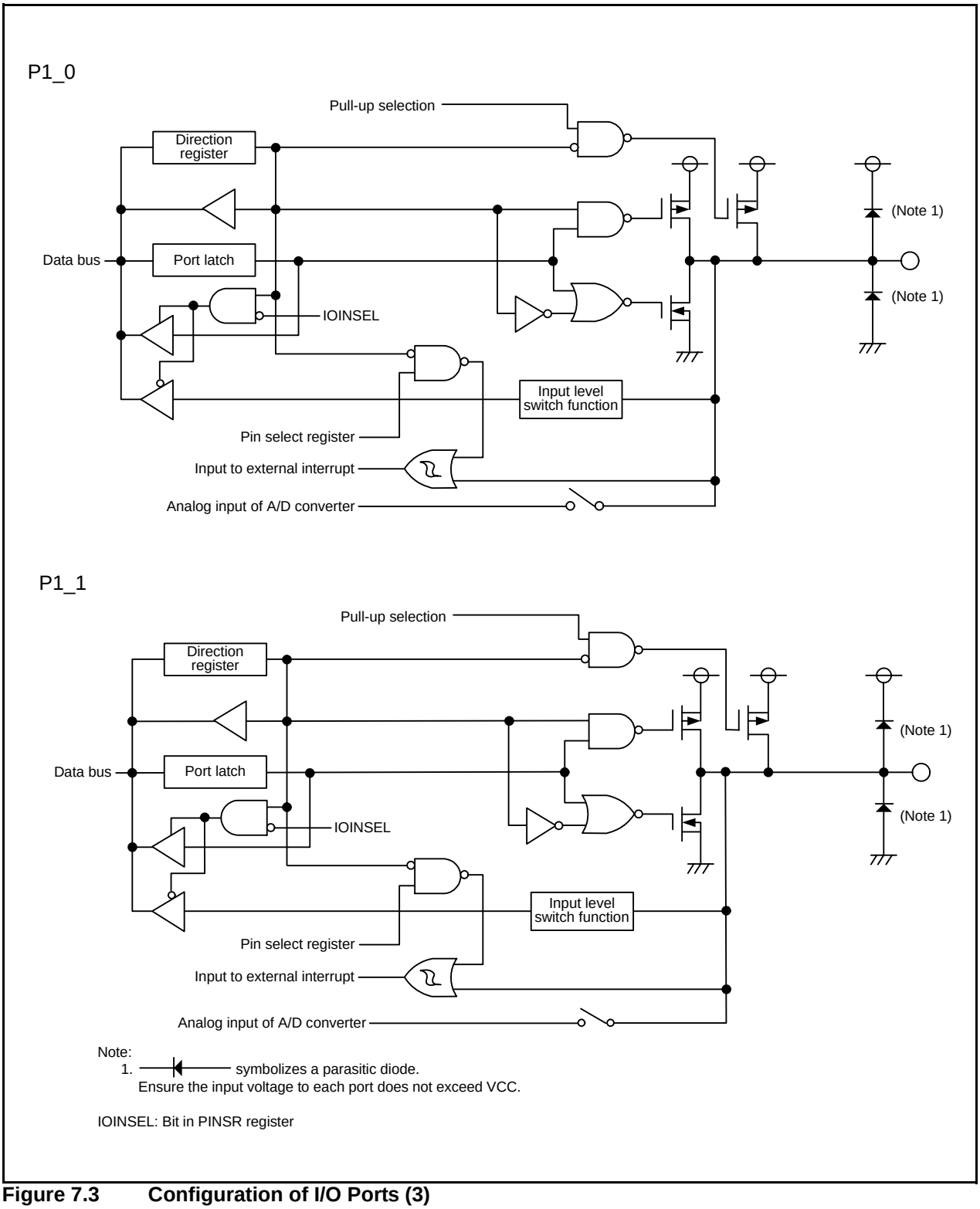
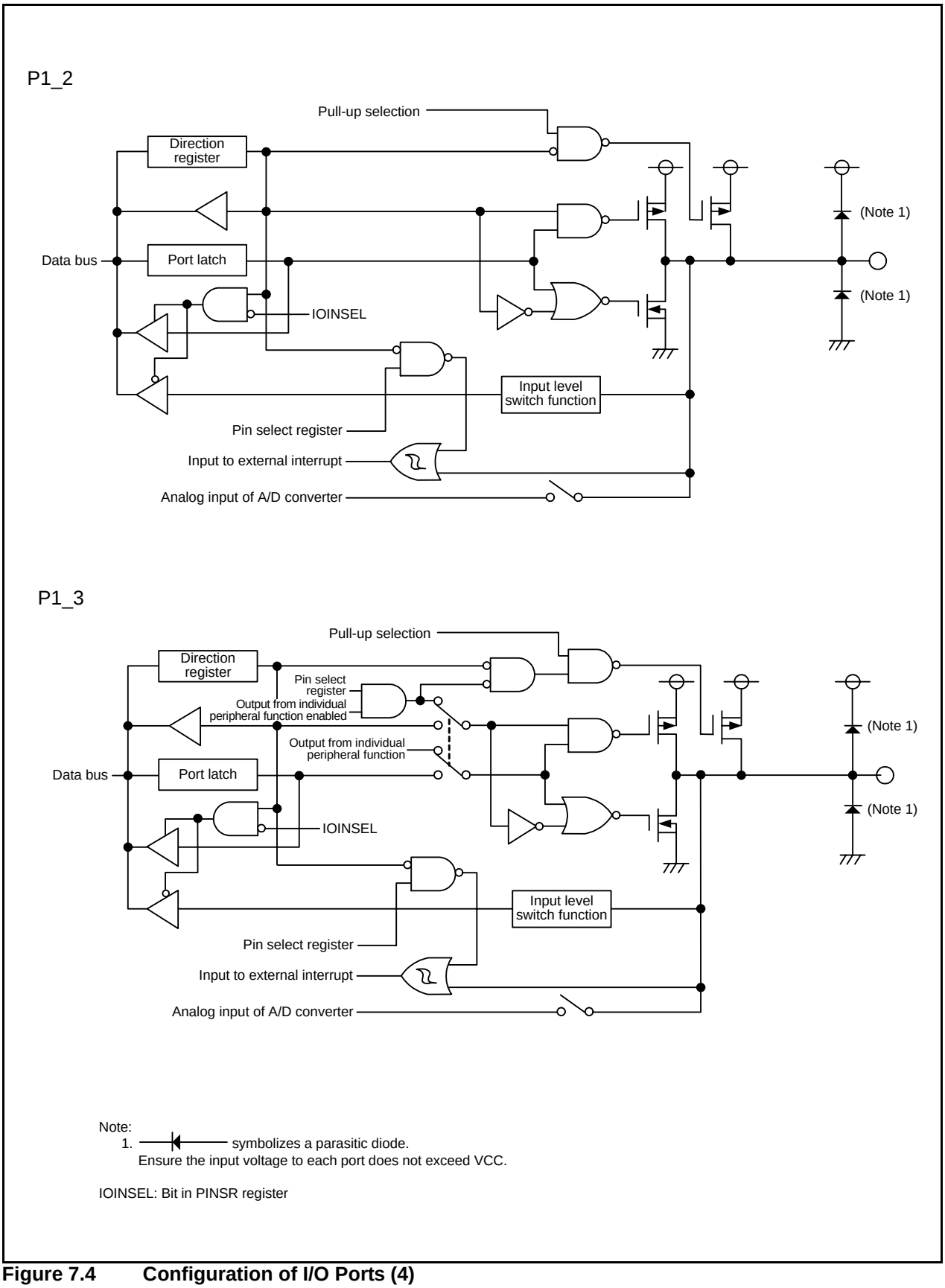


Figure 7.3 Configuration of I/O Ports (3)

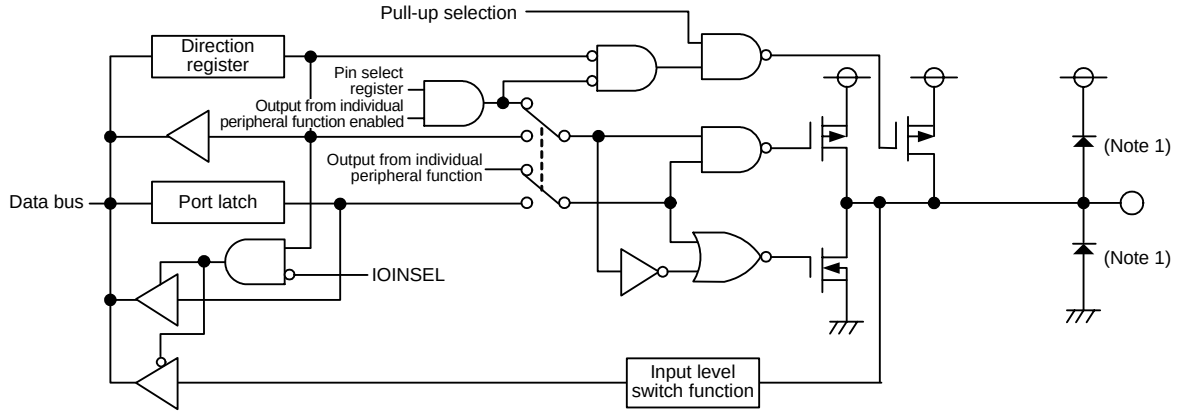


Note:
1. ⟵| symbolizes a parasitic diode.
Ensure the input voltage to each port does not exceed VCC.

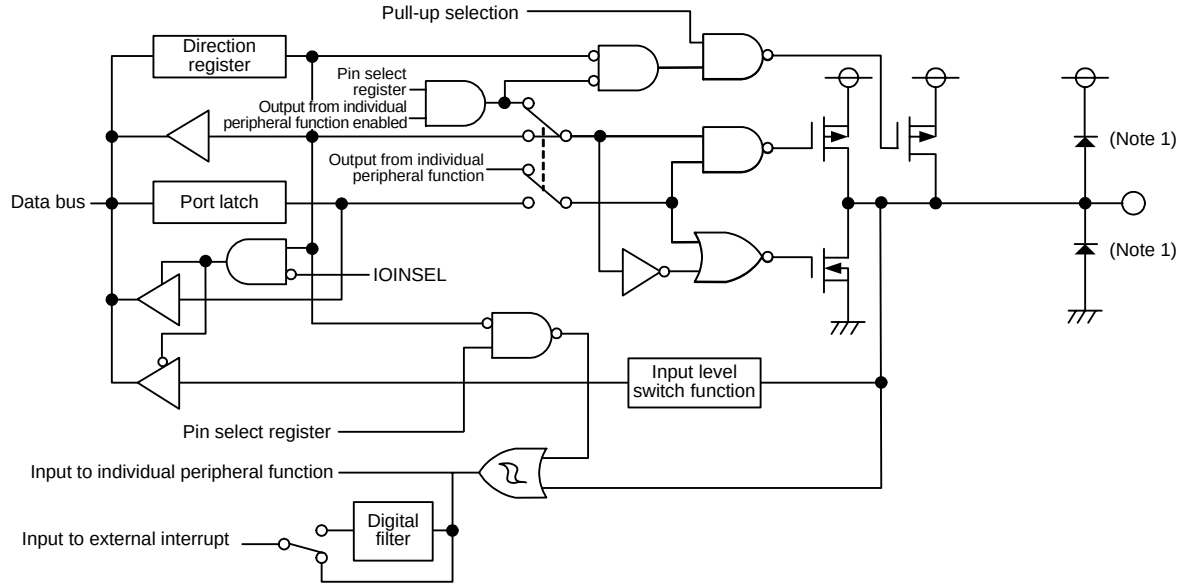
IOINSEL: Bit in PINSR register

Figure 7.4 Configuration of I/O Ports (4)

P1_4



P1_5, P1_7



Note:
1. ⟵| symbolizes a parasitic diode.
Ensure the input voltage to each port does not exceed VCC.

IOINSEL: Bit in PINSR register

Figure 7.5 Configuration of I/O Ports (5)

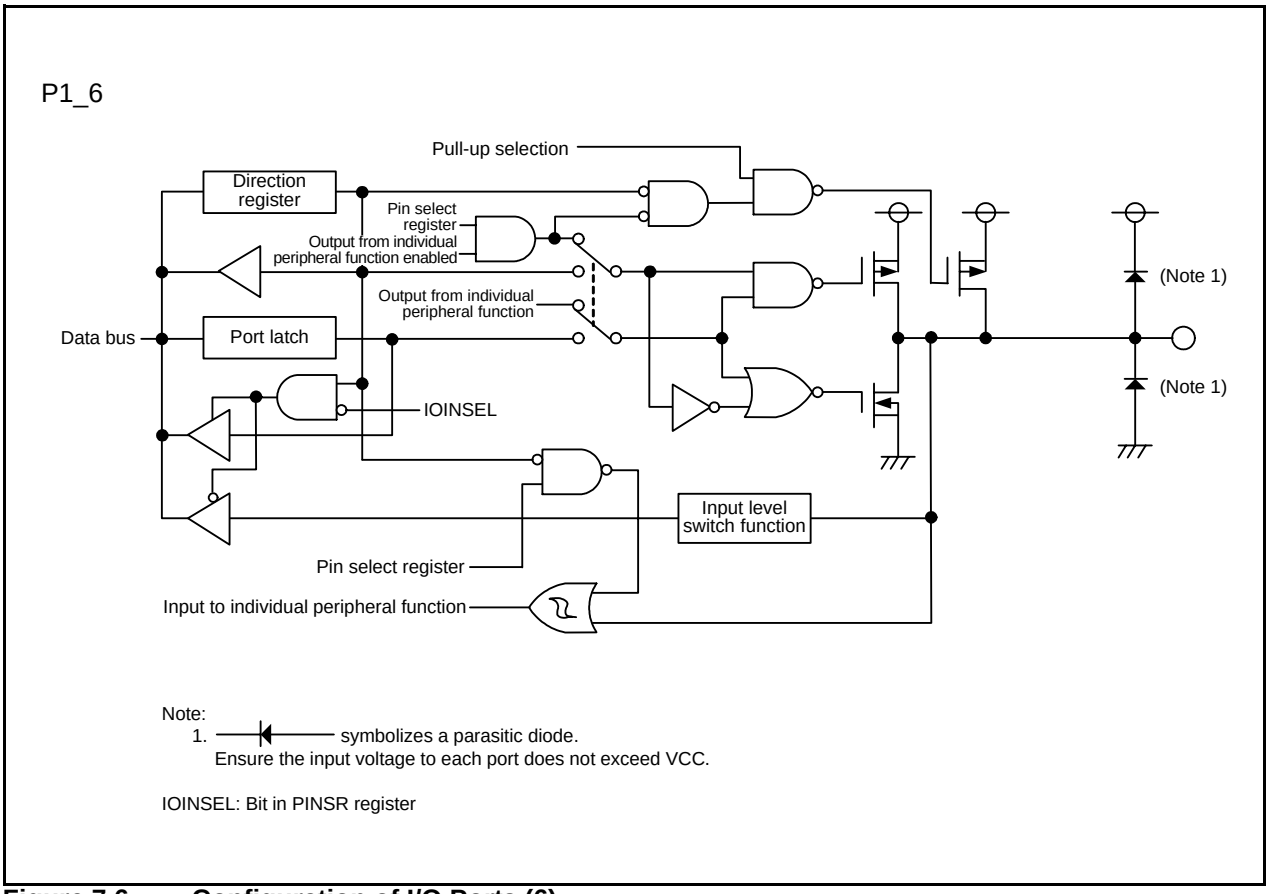


Figure 7.6 Configuration of I/O Ports (6)

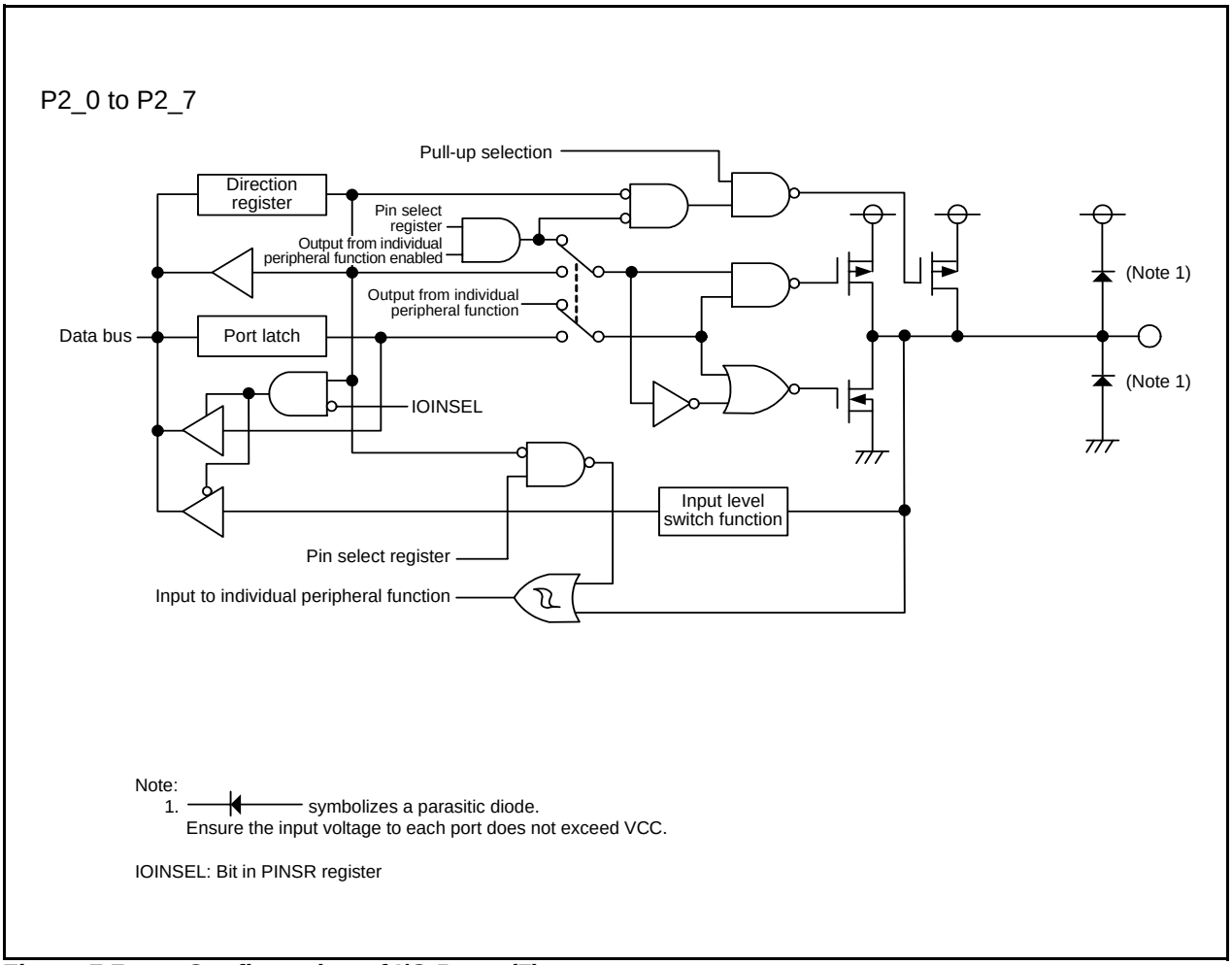


Figure 7.7 Configuration of I/O Ports (7)

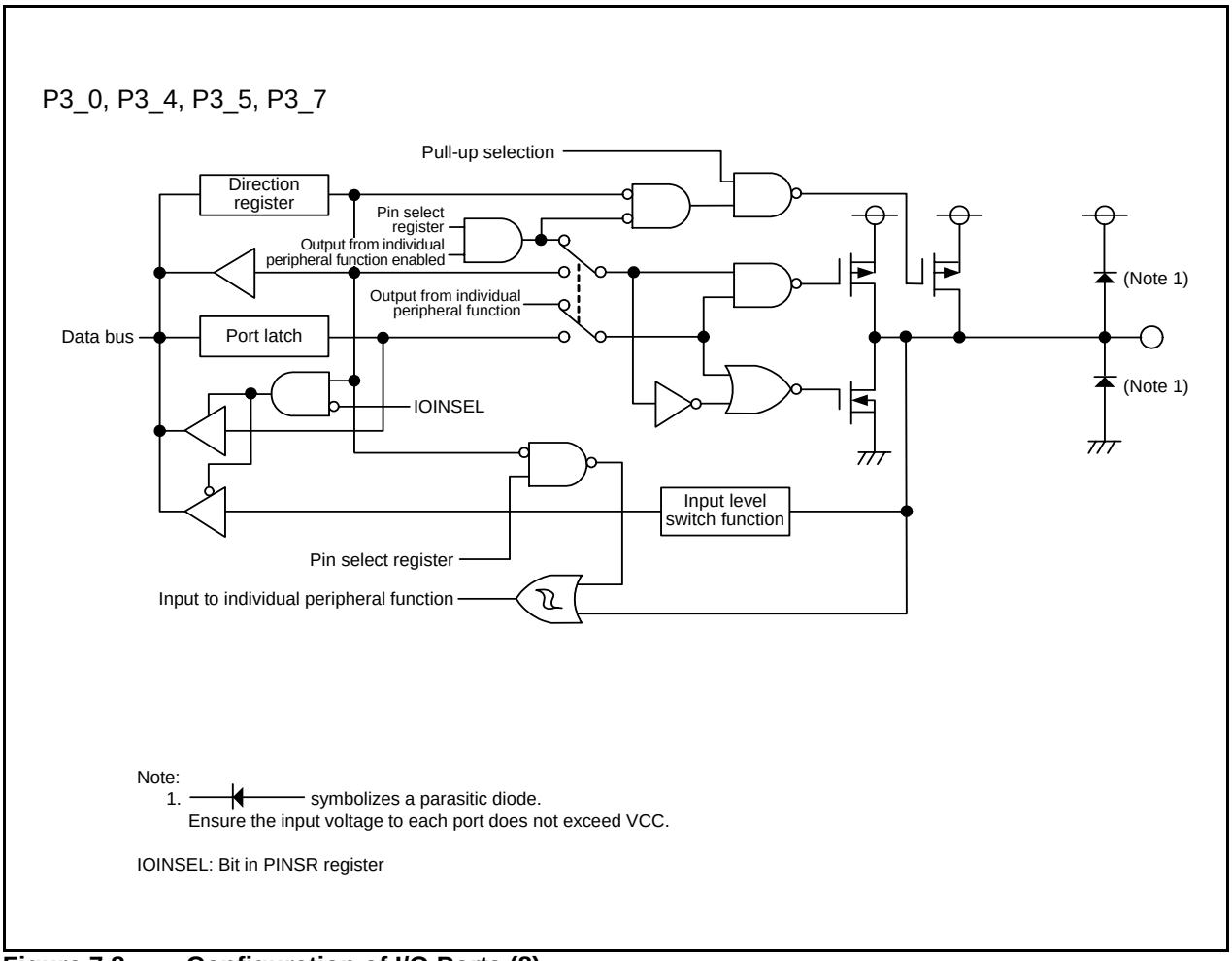
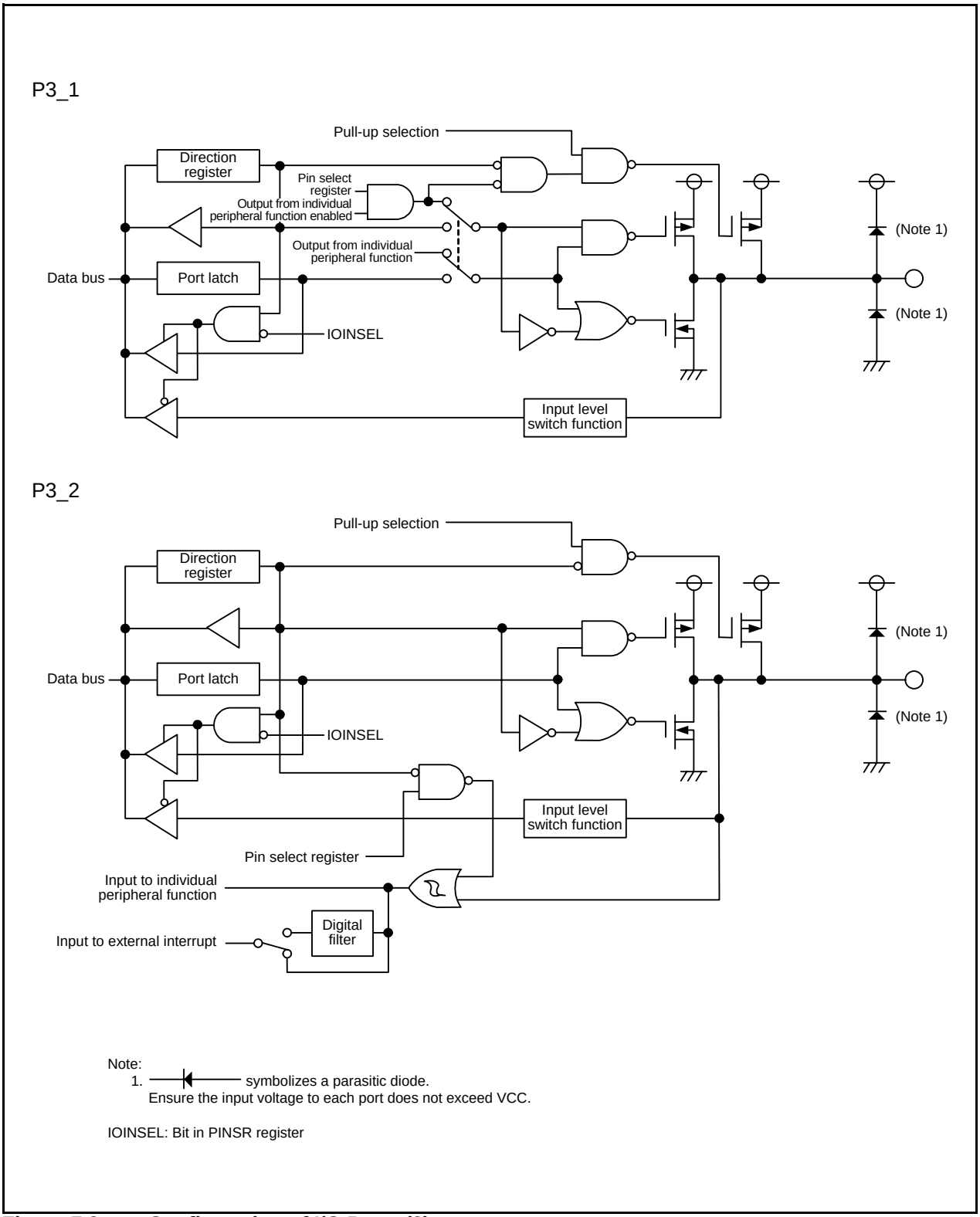


Figure 7.8 Configuration of I/O Ports (8)

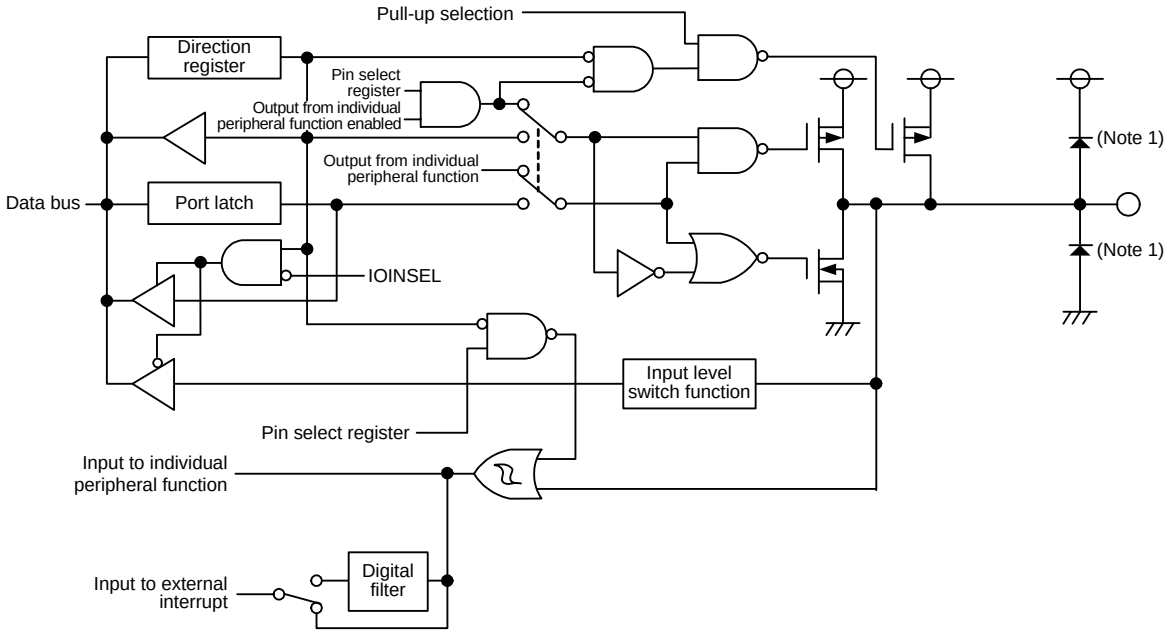


Note:
1. ⟵ symbolizes a parasitic diode.
Ensure the input voltage to each port does not exceed VCC.

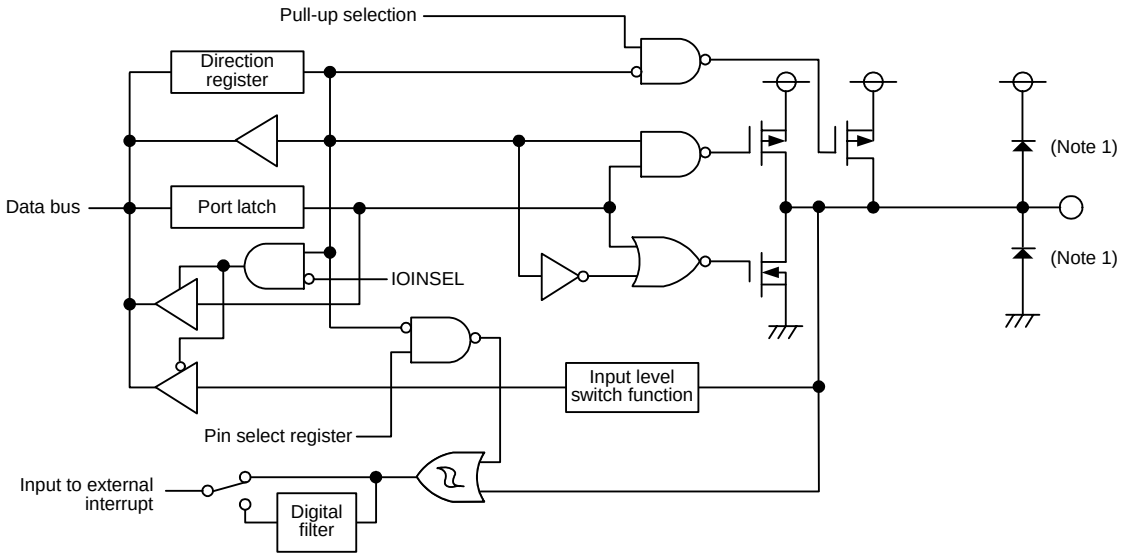
IOINSEL: Bit in PINSR register

Figure 7.9 Configuration of I/O Ports (9)

P3_3



P3_6



Note:
1. ⟵ symbolizes a parasitic diode.
Ensure the input voltage to each port does not exceed VCC.

IOINSEL: Bit in PINSR register

Figure 7.10 Configuration of I/O Ports (10)

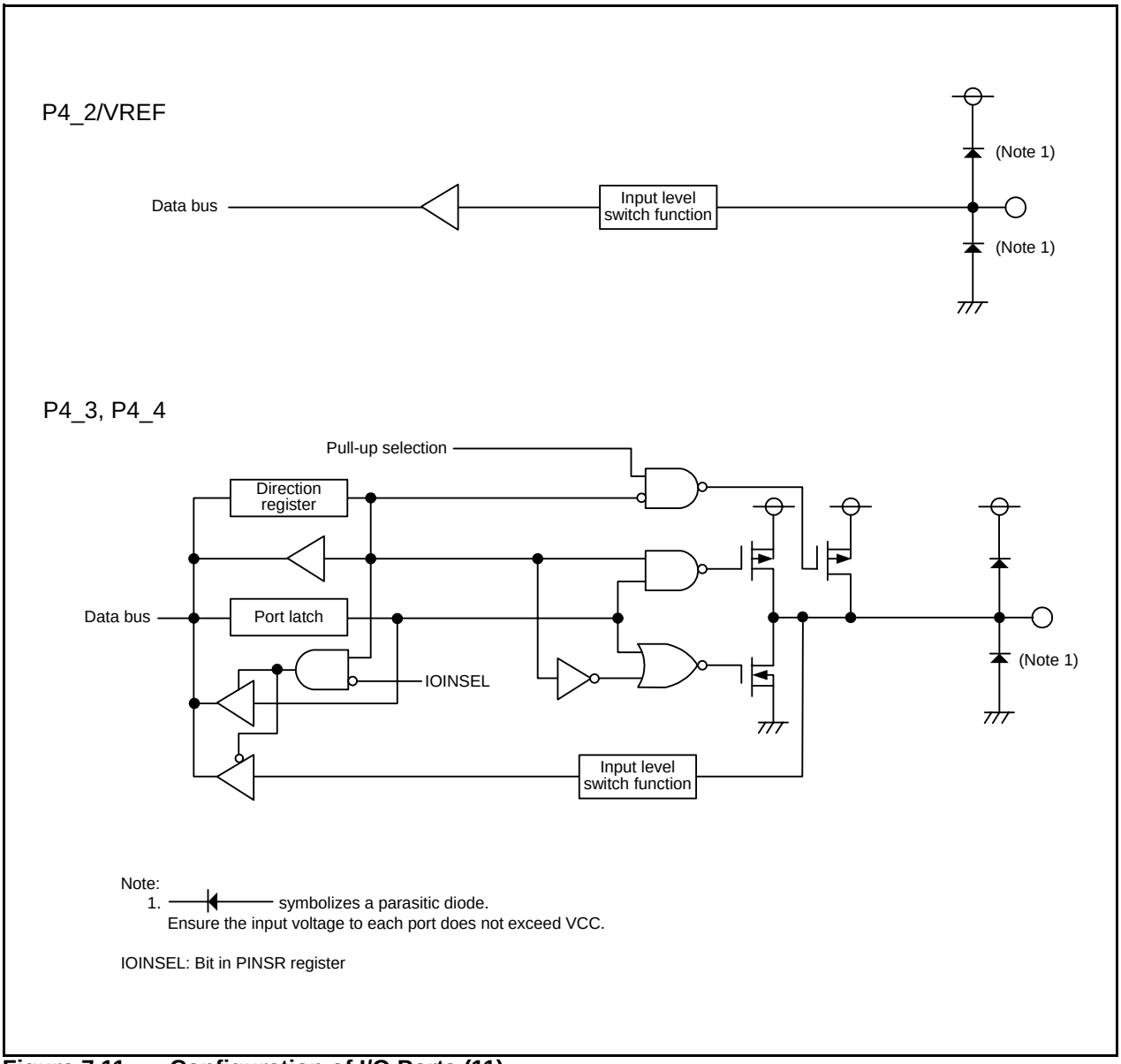


Figure 7.11 Configuration of I/O Ports (11)

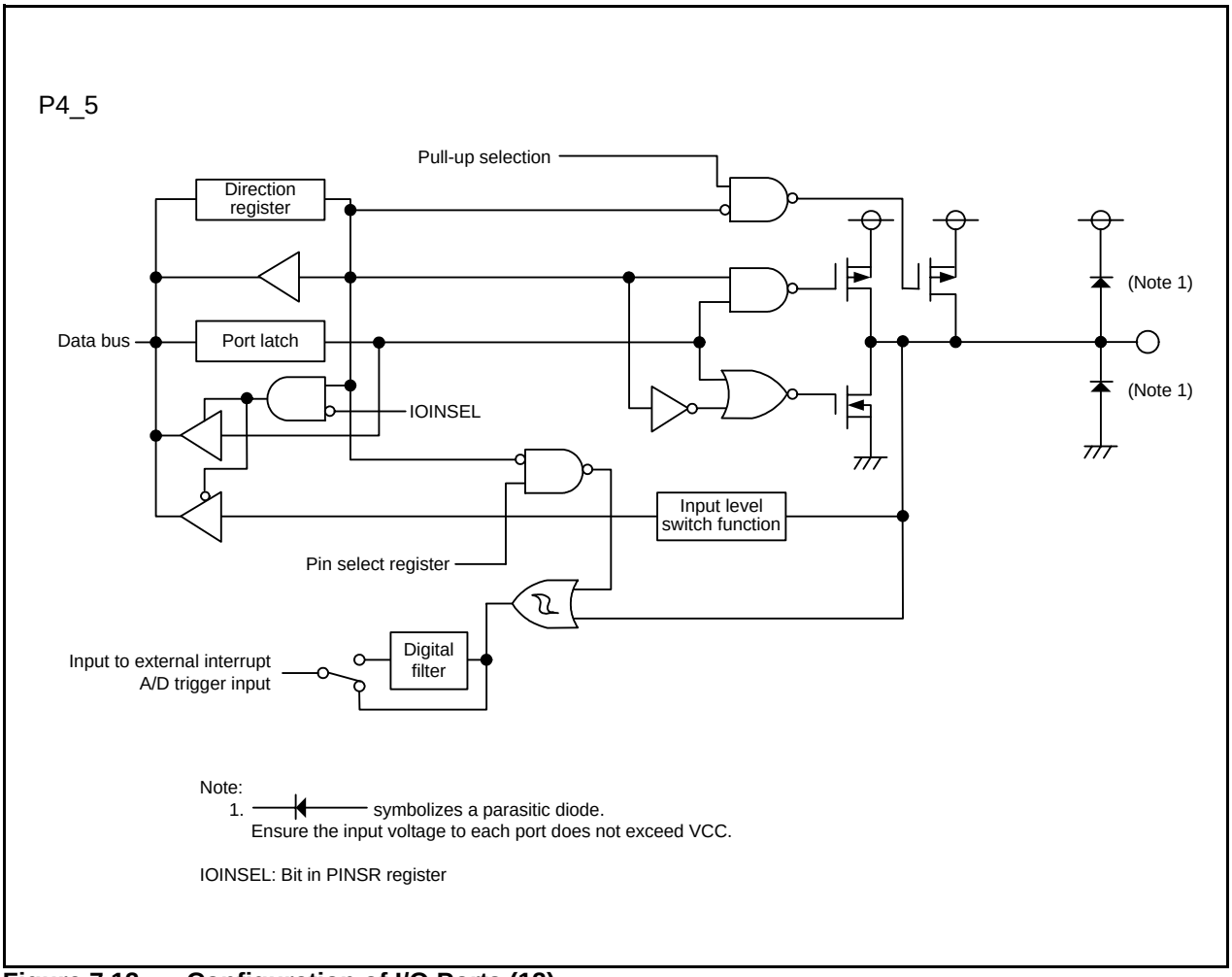


Figure 7.12 Configuration of I/O Ports (12)

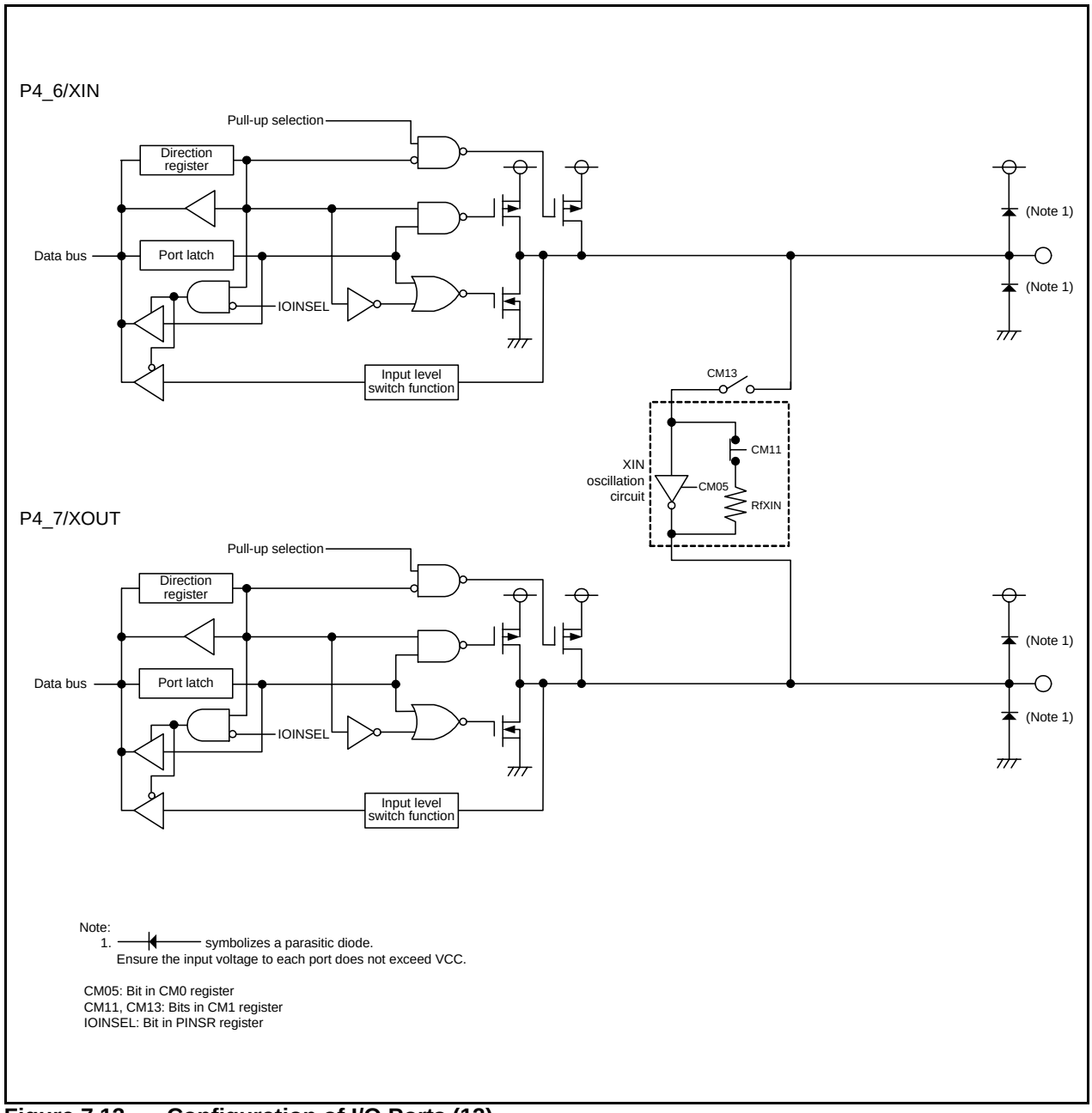
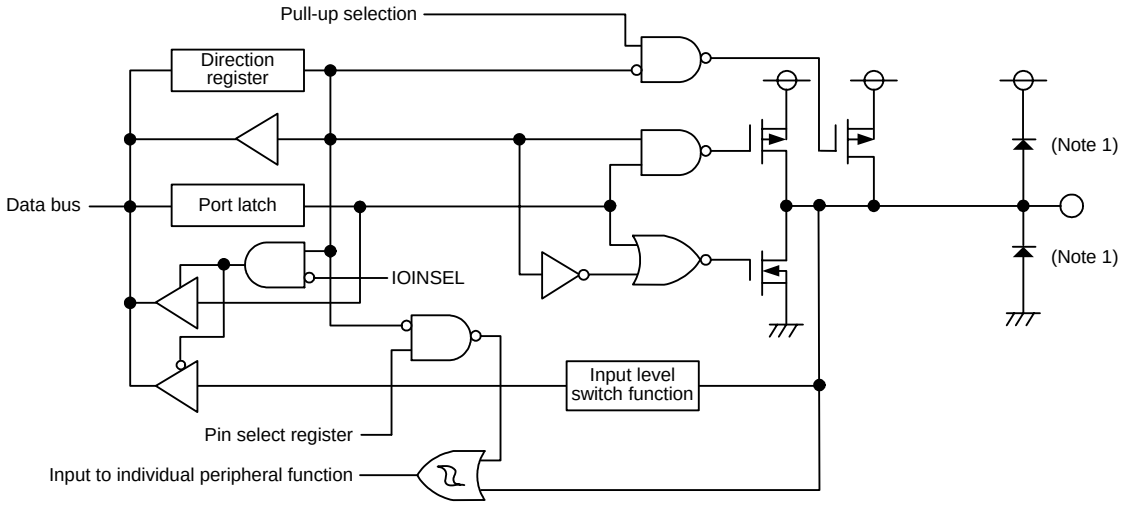
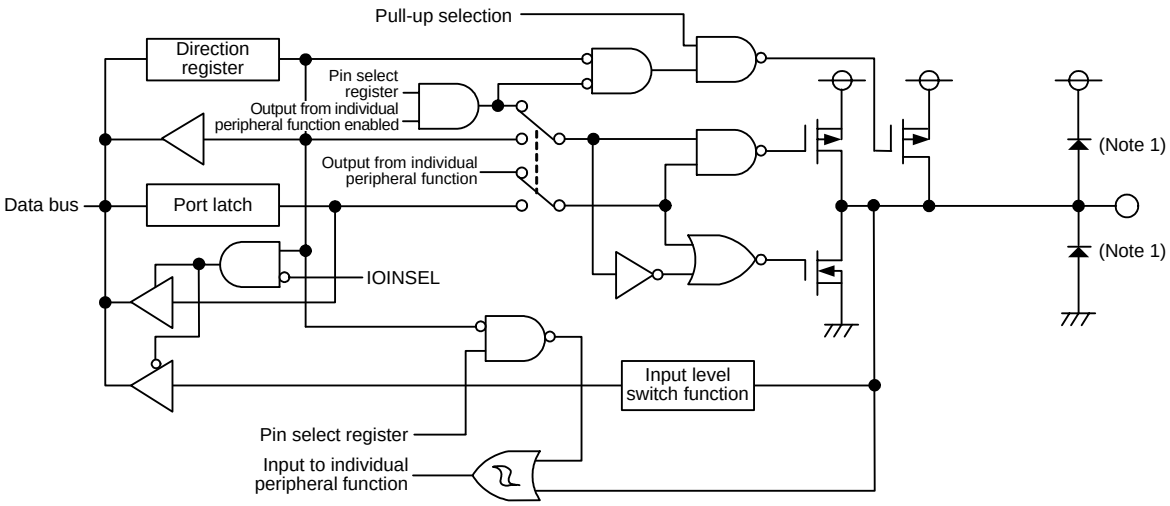


Figure 7.13 Configuration of I/O Ports (13)

P5_0



P5_1 to P5_4, P5_6, P5_7



Note:
1. symbolizes a parasitic diode.
Ensure the input voltage to each port does not exceed VCC.

IOINSEL: Bit in PINSR register

Figure 7.14 Configuration of I/O Ports (14)

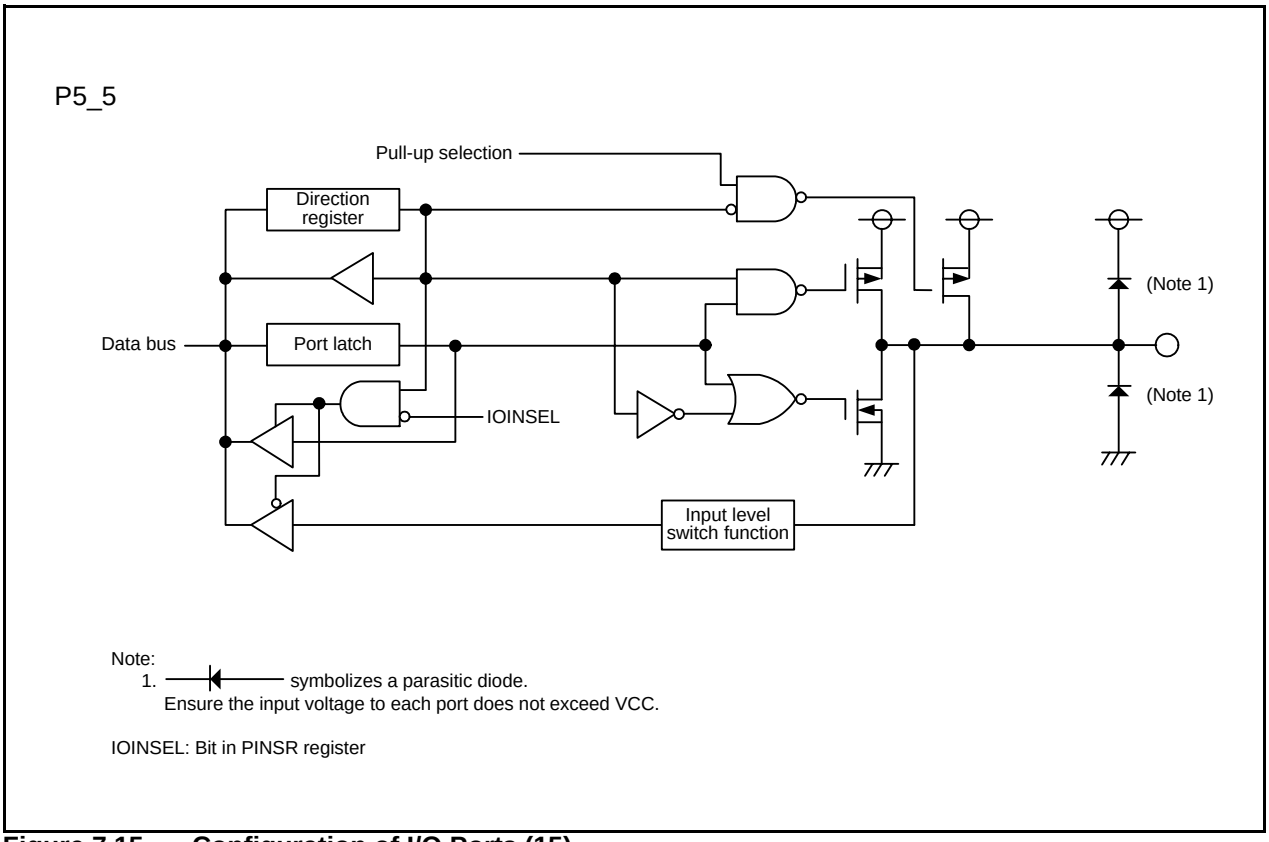
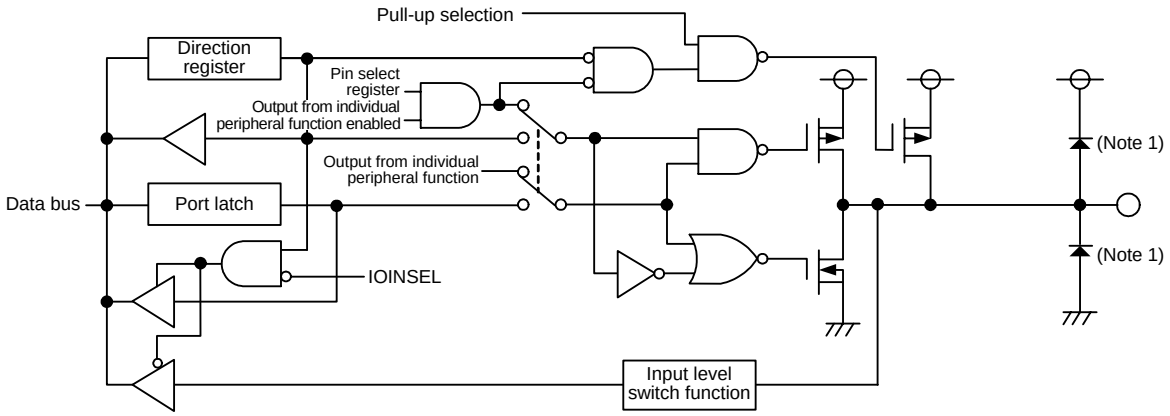
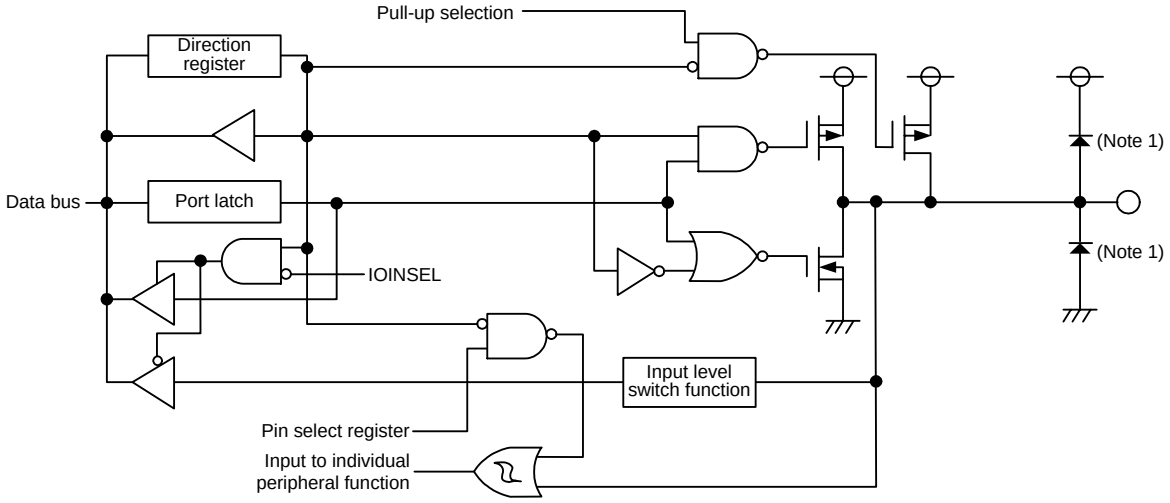


Figure 7.15 Configuration of I/O Ports (15)

P6_0, P6_1



P6_2

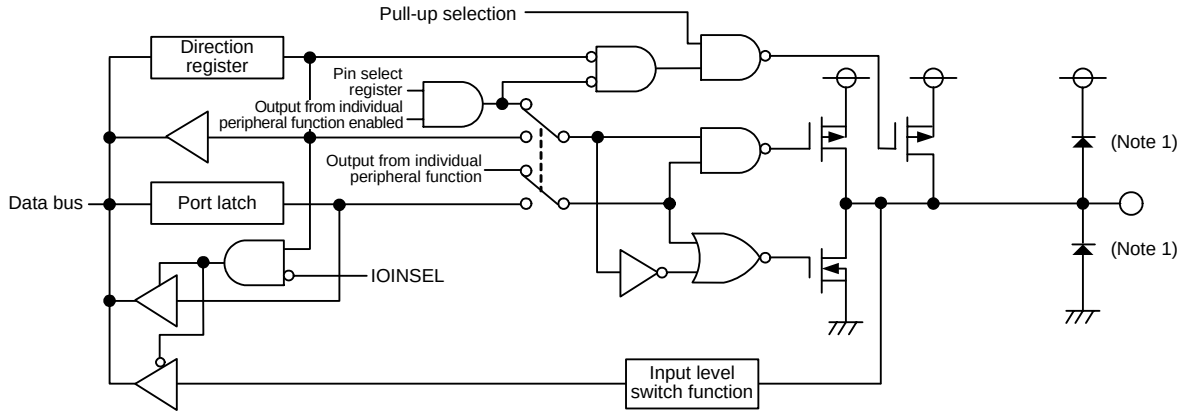


Note:
1. ⟵ symbolizes a parasitic diode.
Ensure the input voltage to each port does not exceed VCC.

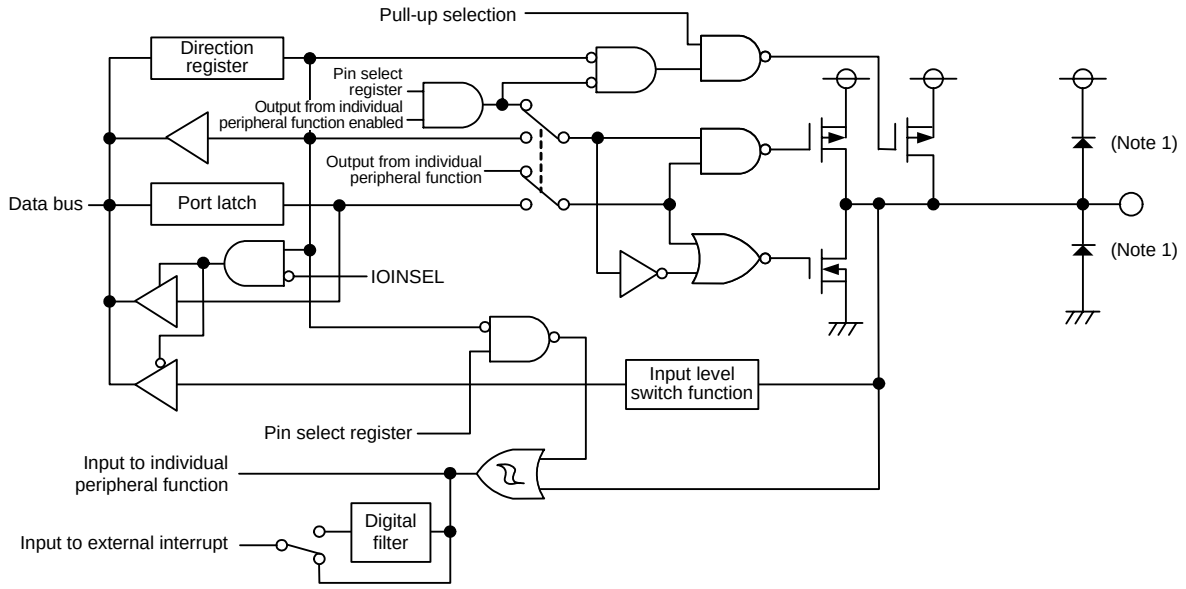
IOINSEL: Bit in PINSR register

Figure 7.16 Configuration of I/O Ports (16)

P6_3



P6_4 to P6_7



Note:
1. ⟵ symbolizes a parasitic diode.
Ensure the input voltage to each port does not exceed VCC.

IOINSEL: Bit in PINSR register

Figure 7.17 Configuration of I/O Ports (17)

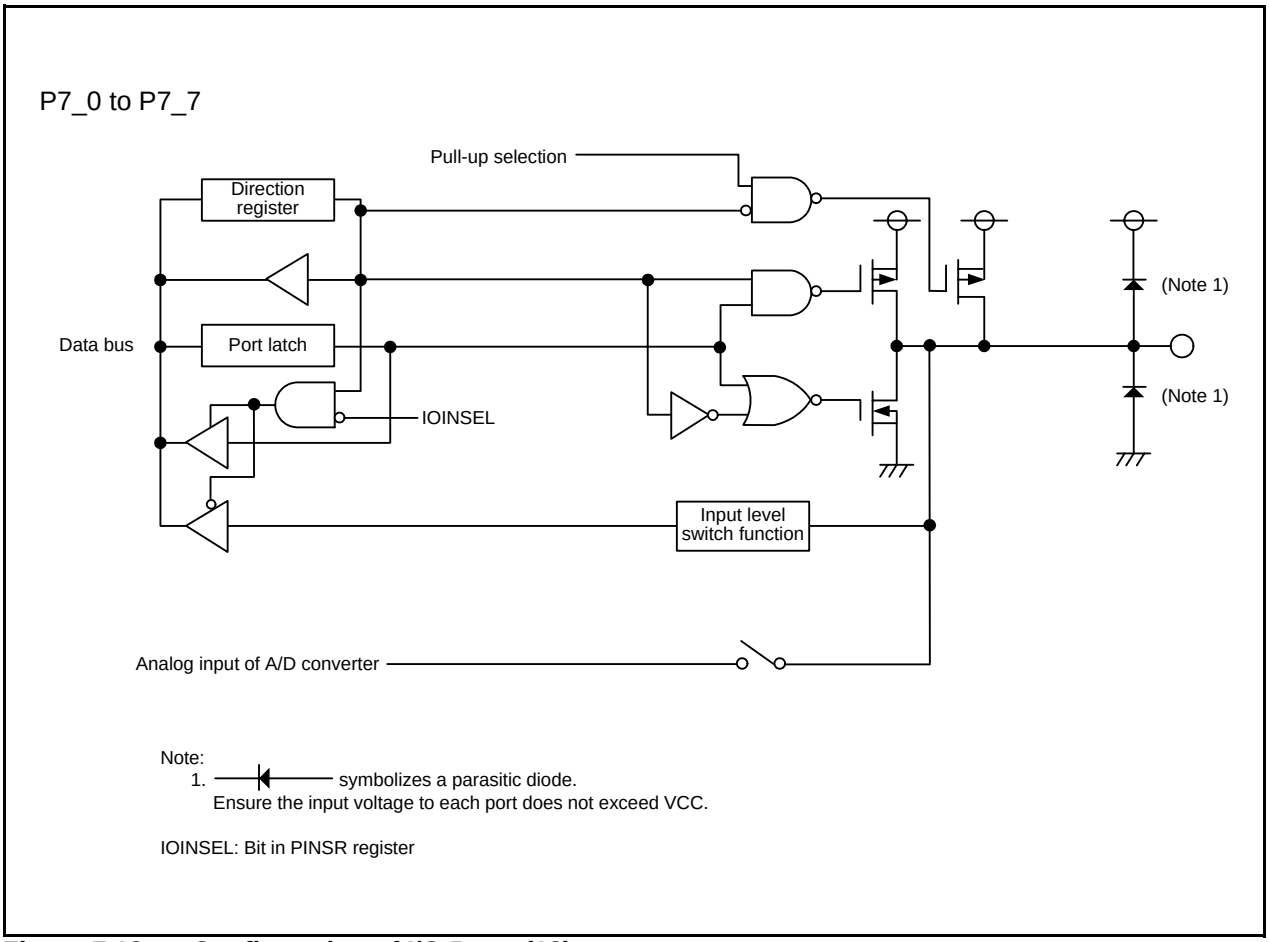
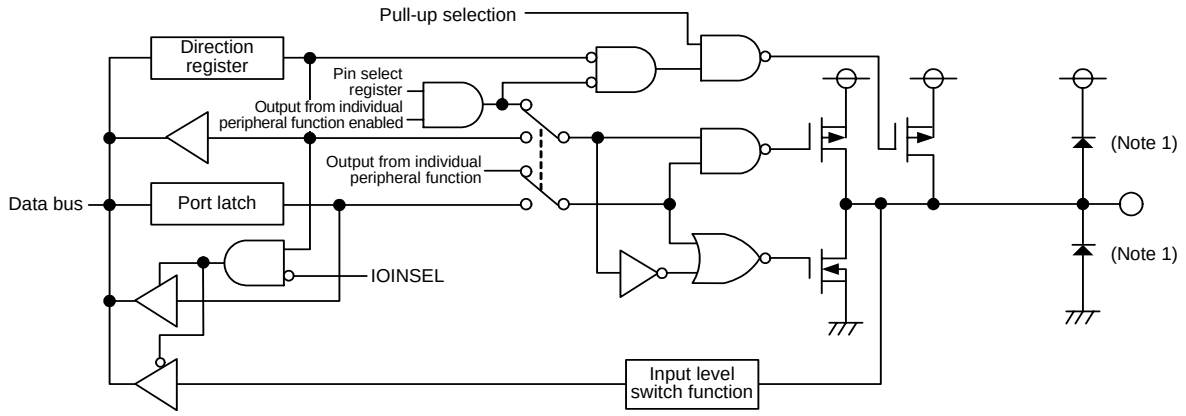
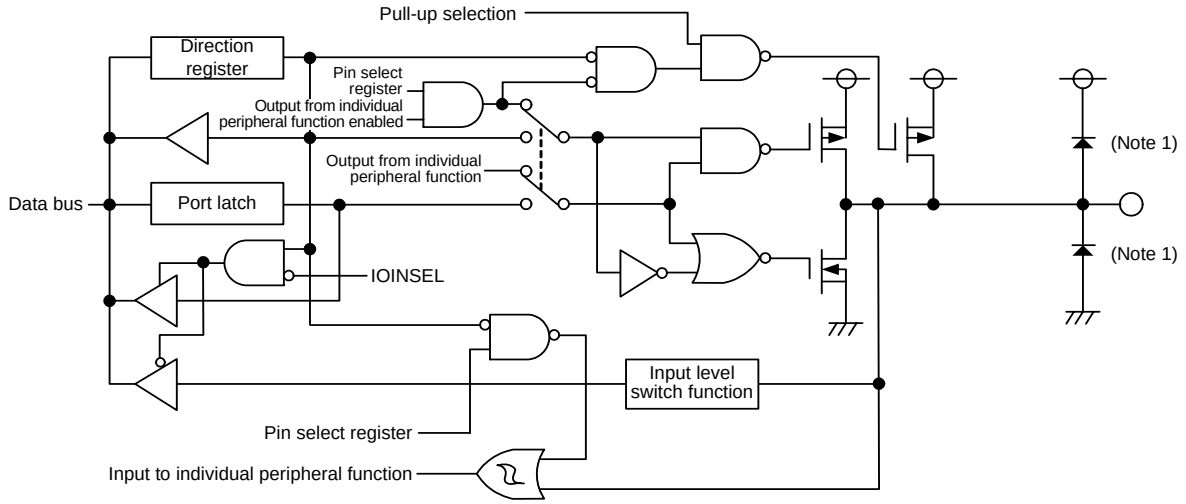


Figure 7.18 Configuration of I/O Ports (18)

P8_0 to P8_2, P8_4, P8_5



P8_3

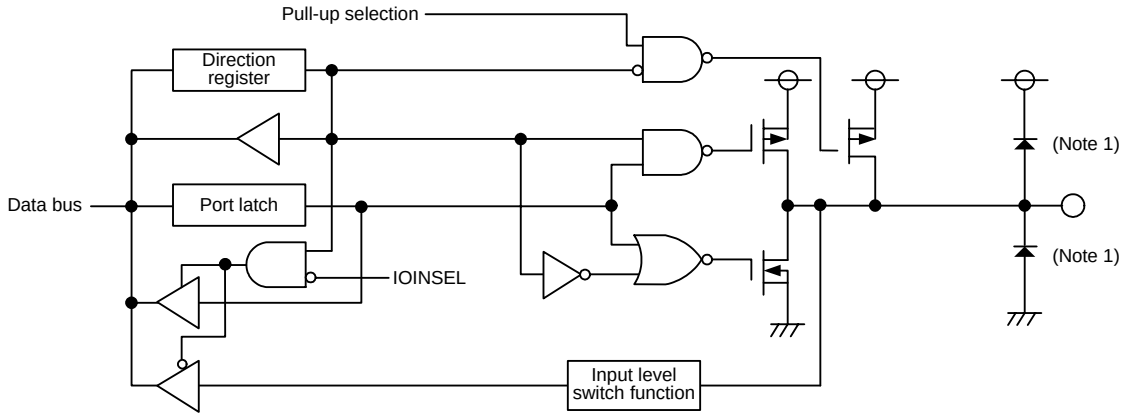


Note:
1. ⟵ symbolizes a parasitic diode.
Ensure the input voltage to each port does not exceed VCC.

IOINSEL: Bit in PINSR register

Figure 7.19 Configuration of I/O Ports (19)

P8_6, P8_7

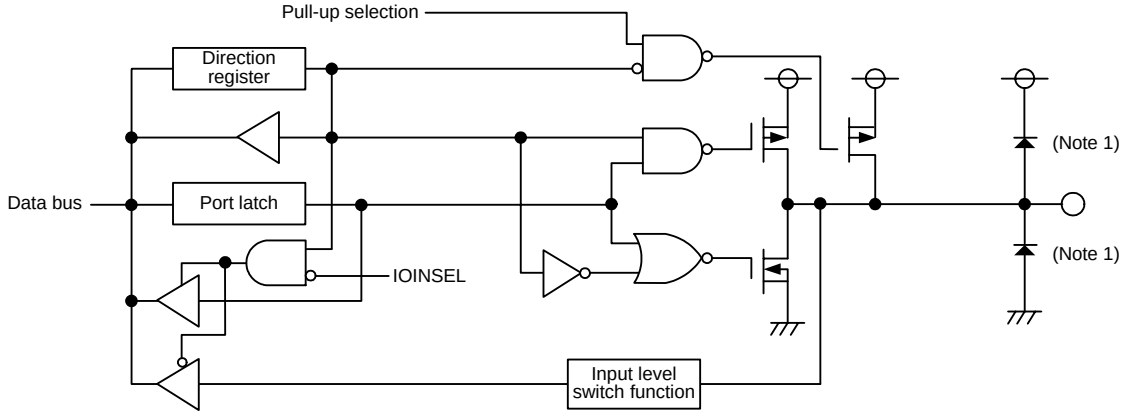


Note:
1. ⟵ symbolizes a parasitic diode.
Ensure the input voltage to each port does not exceed VCC.

IOINSEL: Bit in PINSR register

Figure 7.20 Configuration of I/O Ports (20)

P9_0 to P9_5



Note:
1. ⟵ symbolizes a parasitic diode.
Ensure the input voltage to each port does not exceed VCC.

IOINSEL: Bit in PINSR register

Figure 7.21 Configuration of I/O Ports (21)

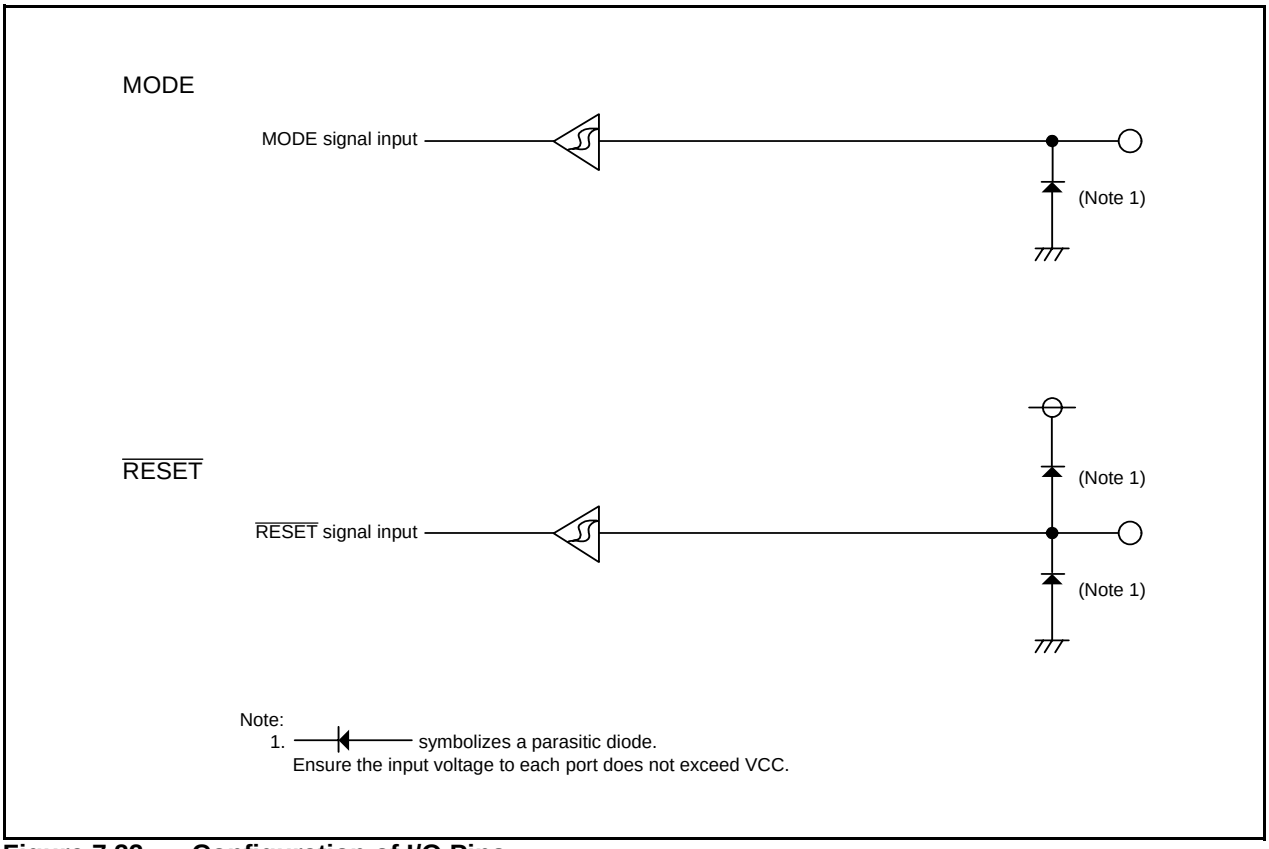


Figure 7.22 Configuration of I/O Pins

7.4 Registers

7.4.1 Port Pi Direction Register (PDi) (i = 0 to 9)

Address 00E2h (PD0 (1)), 00E3h (PD1), 00E6h (PD2), 00E7h (PD3), 00EAh (PD4 (2)), 00EBh (PD5), 00EEh (PD6), 00EFh (PD7), 00F2h (PD8), 00F3h (PD9 (2))

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PDi_7	PDi_6	PDi_5	PDi_4	PDi_3	PDi_2	PDi_1	PDi_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PDi_0	Port Pi_0 direction bit	0: Input mode (functions as an input port) 1: Output mode (functions as an output port)	R/W
b1	PDi_1	Port Pi_1 direction bit		R/W
b2	PDi_2	Port Pi_2 direction bit		R/W
b3	PDi_3	Port Pi_3 direction bit		R/W
b4	PDi_4	Port Pi_4 direction bit		R/W
b5	PDi_5	Port Pi_5 direction bit		R/W
b6	PDi_6	Port Pi_6 direction bit		R/W
b7	PDi_7	Port Pi_7 direction bit		R/W

Notes:
1. Write to the PD0 register with the next instruction after that used to set the PRC2 bit in the PRCR register to 1 (write enabled).
2. Bits PD4_0 to PD4_2 in the PD4 and bits PD9_6, PD9_7 in the PD9 register are unavailable on this MCU. If it is necessary to set bits PD4_0 to PD4_2 and PD9_6, PD9_7, set to 0. When read, the content is 0.

The PDi register selects whether I/O ports are used for input or output. Each bit in the PDi register corresponds to one port.

7.4.2 Port Pi Register (Pi) (i = 0 to 9)

Address 00E0h(P0), 00E1h(P1), 00E4h(P2), 00E5h(P3), 00E8h(P4 (1)), 00E9h(P5 (1)), 00ECh(P6), 00EDh (P7), 00F0h (P8), 00F1h (P9)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	Pi_7	Pi_6	Pi_5	Pi_4	Pi_3	Pi_2	Pi_1	Pi_0
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	Pi_0	Port Pi_0 bit	0: “L” level 1: “H” level	R/W
b1	Pi_1	Port Pi_1 bit		R/W
b2	Pi_2	Port Pi_2 bit		R/W
b3	Pi_3	Port Pi_3 bit		R/W
b4	Pi_4	Port Pi_4 bit		R/W
b5	Pi_5	Port Pi_5 bit		R/W
b6	Pi_6	Port Pi_6 bit		R/W
b7	Pi_7	Port Pi_7 bit		R/W

Note:
1. Bits P4_0 to P4_1 in the P4 and bits P9_6, P9_7 in the P9 register are unavailable on this MCU. If it is necessary to set bits P4_0 to P4_1 and P9_6, P9_7, set to 0. When read, the content is 0.

Data input and output to and from external devices are accomplished by reading and writing to the Pi register. The Pi register consists of a port latch to retain output data and a circuit to read the pin status. The value written in the port latch is output from the pin. Each bit in the Pi register corresponds to one port.

Pi_j Bit (i = 0 to 9, j = 0 to 7) (Port Pi_j Bit)

The pin level of any I/O port which is set to input mode can be read by reading the corresponding bit in this register. The pin level of any I/O port which is set to output mode can be controlled by writing to the corresponding bit in this register.

7.4.3 Timer RA Pin Select Register (TRASR)

Address 0180h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	TRAIO1SEL0	—	TRAOSEL0	—	TRAIOSEL1	TRAIOSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRAIOSEL0	TRAIO0 pin select bit	b1 b0 0 0: TRAIO0 pin not used 0 1: P1_7 assigned 1 0: P1_5 assigned 1 1: Do not set.	R/W
b1	TRAIOSEL1			R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	TRAOSEL0	TRAO0 pin select bit	0: P3_7 assigned 1: P3_0 assigned	R/W
b4	—	Reserved bit	Set to 0.	R/W
b5	TRAIO1SEL0	TRAIO1 pin select bit	0: TRAIO1 pin not used 1: P6_4 assigned	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

The TRASR register selects which pin is assigned to the timer RA I/O. To use the I/O pin for timer RA, set this register.
Set the TRASR register before setting the timer RA associated registers. Also, do not change the setting value in this register during timer RA operation.

7.4.4 Timer RB/RC Pin Select Register (TRBRCSR)

Address 0181h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	TRCCLKSEL2	TRCCLKSEL1	TRCCLKSEL0	—	—	TRBOSEL1	TRBOSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRBOSEL0	TRBO pin select bit	b1 b0 0 0: P1_3 assigned 0 1: P3_1 assigned 1 0: Do not set. 1 1: TRBO pin not used	R/W
b1	TRBOSEL1			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	TRCCLKSEL0	TRCCLK pin select bit	b6 b5 b4 0 0 0: TRCCLK pin not used 1 0 0: P5_0 assigned Other than above: Do not set.	R/W
b5	TRCCLKSEL1			R/W
b6	TRCCLKSEL2			R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

The TRBRCSR register selects which pin is assigned to the timer RB and timer RC I/O. To use the I/O pin for timer RB and timer RC, set this register.
Set bits TRBOSEL0 and TRBOSEL1 before setting the timer RB associated registers. Set bits TRCCLKSEL0 to TRCCLKSEL2 before setting the timer RC associated registers. Also, do not change the setting values of bits TRBOSEL0 and TRBOSEL1 during timer RB operation. Do not change the setting values of bits TRCCLKSEL0 to TRCCLKSEL2 during timer RC operation.

7.4.5 Timer RC Pin Select Register 0 (TRCPSR0)

Address 0182h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	TRCIOBSEL2	TRCIOBSEL1	TRCIOBSEL0	—	TRCIOASEL2	TRCIOASEL1	TRCIOASEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRCIOASEL0	TRCIOA/TRCTRG pin select bit	b2 b1 b0 0 0 0: TRCIOA/TRCTRG pin not used 1 0 1: P5_1 assigned Other than above: Do not set.	R/W
b1	TRCIOASEL1			R/W
b2	TRCIOASEL2			R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TRCIOBSEL0	TRCIOB pin select bit	b6 b5 b4 0 0 0: TRCIOB pin not used 1 1 1: P5_2 assigned Other than above: Do not set.	R/W
b5	TRCIOBSEL1			R/W
b6	TRCIOBSEL2			R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

The TRCPSR0 register selects which pin is assigned to the timer RC I/O. To use the I/O pin for timer RC, set this register.
Set the TRCPSR0 register before setting the timer RC associated registers. Also, do not change the setting value in this register during timer RC operation.

7.4.6 Timer RC Pin Select Register 1 (TRCPSR1)

Address 0183h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	TRCIODSEL2	TRCIODSEL1	TRCIODSEL0	—	TRCIOCSEL2	TRCIOCSEL1	TRCIOCSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRCIOCSEL0	TRCIOC pin select bit	b2 b1 b0 0 0 0: TRCIOC pin not used 1 1 0: P5_3 assigned Other than above: Do not set.	R/W
b1	TRCIOCSEL1			R/W
b2	TRCIOCSEL2			R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TRCIODSEL0	TRCIOD pin select bit	b6 b5 b4 0 0 0: TRCIOD pin not used 1 1 0: P5_4 assigned Other than above: Do not set.	R/W
b5	TRCIODSEL1			R/W
b6	TRCIODSEL2			R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

The TRCPSR1 register selects which pin is assigned to the timer RC I/O. To use the I/O pin for timer RC, set this register.
Set the TRCPSR1 register before setting the timer RC associated registers. Also, do not change the setting value in this register during timer RC operation.

7.4.7 Timer RD Pin Select Register 0 (TRDPSR0)

Address 0184h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	TRDIOD0SEL0	—	TRDIOC0SEL0	—	TRDIOB0SEL0	—	TRDIOA0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRDIOA0SEL0	TRDIOA0/TRDCLK pin select bit	0: TRDIOA0/TRDCLK pin not used 1: P2_0 assigned	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	TRDIOB0SEL0	TRDIOB0 pin select bit	0: TRDIOB0 pin not used 1: P2_1 assigned	R/W
b3	—	Reserved bit	Set to 0.	R/W
b4	TRDIOC0SEL0	TRDIOC0 pin select bit	0: TRDIOC0 pin not used 1: P2_2 assigned	R/W
b5	—	Reserved bit	Set to 0.	R/W
b6	TRDIOD0SEL0	TRDIOD0 pin select bit	0: TRDIOD0 pin not used 1: P2_3 assigned	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

The TRDPSR0 register selects which pin is assigned to the timer RD I/O. To use the I/O pin for timer RD, set this register.
Set the TRDPSR0 register before setting the timer RD associated registers. Also, do not change the setting value in this register during timer RD operation.

7.4.8 Timer RD Pin Select Register 1 (TRDPSR1)

Address 0185h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	TRDIOD1SEL0	—	TRDIOC1SEL0	—	TRDIOB1SEL0	—	TRDIOA1SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRDIOA1SEL0	TRDIOA1 pin select bit	0: TRDIOA1 pin not used 1: P2_4 assigned	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	TRDIOB1SEL0	TRDIOB1 pin select bit	0: TRDIOB1 pin not used 1: P2_5 assigned	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TRDIOC1SEL0	TRDIOC1 pin select bit	0: TRDIOC1 pin not used 1: P2_6 assigned	R/W
b5	—	Reserved bit	Set to 0.	R/W
b6	TRDIOD1SEL0	TRDIOD1 pin select bit	0: TRDIOD1 pin not used 1: P2_7 assigned	R/W
b7	—	Reserved bit	Set to 0.	R/W

The TRDPSR1 register selects which pin is assigned to the timer RD I/O. To use the I/O pin for timer RD, set this register.
Set the TRDPSR1 register before setting the timer RD associated registers. Also, do not change the setting value in this register during timer RD operation.

7.4.9 Timer Pin Select Register (TIMSR)

Address 0186h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRGCLKBSEL	TRGCLKASEL	TRGIOBSEL	TRGIOASEL	—	TRFISEL0	—	TREOSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TREOSEL0	TREO pin select bit	0: P0_4 pin assigned 1: P6_0 pin assigned	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	TRFISEL0	TRFI pin select bit	0: TRFI pin not used 1: P8_3 pin assigned	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TRGIOASEL	TRGIOA pin select bit	0: TRGIOA pin not used 1: P5_6 pin assigned	R/W
b5	TRGIOBSEL	TRGIOB pin select bit	0: TRGIOB pin not used 1: P5_7 pin assigned	R/W
b6	TRGCLKASEL	TRGCLKA pin select bit	0: TRGCLKA pin not used 1: P3_0 pin assigned	R/W
b7	TRGCLKBSEL	TRGCLKB pin select bit	0: TRGCLKB pin not used 1: P3_2 pin assigned	R/W

The TIMSR register selects which pin is assigned as the timers RE, RF, and RG I/O. To use the I/O pin for timers RE, RF, and RG, set this register.
Set the TIMSR register before setting the registers associated with timers RE, RF, and RG. Also, do not change the setting value in this register during the operation of timers RE, RF, and RG.

7.4.10 Timer RF Output Control Register (TRFOUT)

Address 0187h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRFOUT7	TRFOUT6	TRFOUT5	TRFOUT4	TRFOUT3	TRFOUT2	TRFOUT1	TRFOUT0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRFOUT0	TRFO00 output enable bit	0: Output disabled 1: Output enabled	R/W
b1	TRFOUT1	TRFO01 output enable bit		R/W
b2	TRFOUT2	TRFO02 output enable bit		R/W
b3	TRFOUT3	TRFO10 output enable bit		R/W
b4	TRFOUT4	TRFO11 output enable bit		R/W
b5	TRFOUT5	TRFO12 output enable bit		R/W
b6	TRFOUT6	TRFO00 to TRFO02 output invert bit	0: Output not inverted 1: Output inverted	R/W
b7	TRFOUT7	TRFO10 to TRFO12 output invert bit		R/W

7.4.11 UART0 Pin Select Register (U0SR)

Address 0188h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	CLK0SEL0	—	RXD0SEL0	—	TXD0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TXD0SEL0	TXD0 pin select bit	0: TXD0 pin not used 1: P1_4 assigned	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	RXD0SEL0	RXD0 pin select bit	0: RXD0 pin not used 1: P1_5 assigned	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	CLK0SEL0	CLK0 pin select bit	0: CLK0 pin not used 1: P1_6 assigned	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	—			
b7	—			

The U0SR register selects which pin is assigned to the UART0 I/O. To use the I/O pin for UART0, set this register.
Set the U0SR register before setting the UART0 associated registers. Also, do not change the setting value in this register during UART0 operation.

7.4.12 UART1 Pin Select Register (U1SR)

Address 0189h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	CLK1SEL1	CLK1SEL0	RXD1SEL1	RXD1SEL0	TXD1SEL1	TXD1SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TXD1SEL0	TXD1 pin select bit	b1 b0 0 0: TXD1 pin not used 0 1: P0_1 assigned 1 0: P6_3 assigned 1 1: Do not set.	R/W
b1	TXD1SEL1			R/W
b2	RXD1SEL0	RXD1 pin select bit	b3 b2 0 0: RXD1 pin not used 0 1: P0_2 assigned 1 0: P6_4 assigned 1 1: Do not set.	R/W
b3	RXD1SEL1			R/W
b4	CLK1SEL0	CLK1 pin select bit	b5 b4 0 0: CLK1 pin not used 0 1: P0_3 assigned 1 0: Do not set. 1 1: P6_5 assigned	R/W
b5	CLK1SEL1			R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

The U1SR register selects which pin is assigned to the UART1 I/O. To use the I/O pin for UART1, set this register.
Set the U1SR register before setting the UART1 associated registers. Also, do not change the setting value in this register during UART1 operation.

7.4.13 UART2 Pin Select Register 0 (U2SR0)

Address 018Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	RXD2SEL2	RXD2SEL1	RXD2SEL0	—	TXD2SEL2	TXD2SEL1	TXD2SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TXD2SEL0	TXD2/SDA2 pin select bit	b2 b1 b0 0 0 0: TXD2/SDA2 pin not used 0 0 1: P3_7 assigned 0 1 0: P3_4 assigned 1 0 1: P6_6 assigned Other than above: Do not set.	R/W
b1	TXD2SEL1			R/W
b2	TXD2SEL2			R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	RXD2SEL0	RXD2/SCL2 pin select bit	b6 b5 b4 0 0 0: RXD2/SCL2 pin not used 0 0 1: P3_4 assigned 0 1 0: P3_7 assigned 1 0 1: P6_7 assigned Other than above: Do not set.	R/W
b5	RXD2SEL1			R/W
b6	RXD2SEL2			R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

The U2SR0 register selects which pin is assigned to the UART2 I/O. To use the I/O pin for UART2, set this register.
Set the U2SR0 register before setting the UART2 associated registers. Also, do not change the setting value in this register during UART2 operation.

7.4.14 UART2 Pin Select Register 1 (U2SR1)

Address 018Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	CTS2SEL0	—	—	CLK2SEL1	CLK2SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CLK2SEL0	CLK2 pin select bit	b1 b0 0 0: CLK2 pin not used 0 1: P3_5 assigned 1 0: Do not set. 1 1: P6_5 assigned	R/W
b1	CLK2SEL1			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	CTS2SEL0	$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$ pin select bit	0: $\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$ pin not used 1: P3_3 assigned	R/W
b5	—	Reserved bit	Set to 0.	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

The U2SR1 register selects which pin is assigned to the UART2 I/O. To use the I/O pin for UART2, set this register.
Set the U2SR1 register before setting the UART2 associated registers. Also, do not change the setting value in this register during UART2 operation.

7.4.15 SSU Pin Select Register (SSUIICSR)

Address 018Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	SCSSEL0	—	SSISEL0	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	SSISEL0	SSI pin select bit	0: P3_4 assigned 1: P3_3 assigned	R/W
b5	—	Reserved bit	Set to 0.	R/W
b6	SCSSEL0	$\overline{\text{SCS}}$ pin select bit	0: P3_3 assigned 1: P3_4 assigned	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

SSISEL0 Bit (SSI pin select bit)

The SSISEL0 bit select which pin is assigned to the SSU I/O. To use the I/O pin for SSU, set this bit.
Set the SSUIICSR register setting the SSU associated registers. Also, do not change the setting value in this register during SSU operation.

SCSSEL0 Bit ($\overline{\text{SCS}}$ pin select bit)

The SCSSEL0 bit select which pin is assigned to the SSU I/O. To use the I/O pin for SSU, set this bit.
Set the SSUIICSR register setting the SSU associated registers. Also, do not change the setting value in this register during SSU operation.

7.4.16 INT Interrupt Input Pin Select Register (INTSR)

Address 018Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3SEL1	INT3SEL0	INT2SEL1	INT2SEL0	INT1SEL2	INT1SEL1	INT1SEL0	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	INT1SEL0	$\overline{\text{INT1}}$ pin select bit	b3 b2 b1 0 0 0: P1_7 assigned 0 0 1: P1_5 assigned 0 1 1: P3_6 assigned 1 0 0: P3_2 assigned Other than above: Do not set.	R/W
b2	INT1SEL1			R/W
b3	INT1SEL2			R/W
b4	INT2SEL0	$\overline{\text{INT2}}$ pin select bit	b5 b4 0 0: P6_6 assigned 0 1: P3_2 assigned 1 0: P6_4 assigned 1 1: Do not set.	R/W
b5	INT2SEL1			R/W
b6	INT3SEL0	$\overline{\text{INT3}}$ pin select bit	b7 b6 0 0: P3_3 assigned 0 1: Do not set. 1 0: P6_7 assigned 1 1: Do not set.	R/W
b7	INT3SEL1			R/W

The INTSR register selects which pin is assigned to the $\overline{\text{INTi}}$ (i = 1 to 3) input. To use $\overline{\text{INTi}}$, set this register. Set the INTSR register before setting the $\overline{\text{INTi}}$ associated registers. Also, do not change the setting values in this register during $\overline{\text{INTi}}$ operation.

7.4.17 I/O Function Pin Select Register (PINSR)

Address 018Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	IOINSEL	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	IOINSEL	I/O port input function select bit	0: The I/O port input function depends on the PDi (i = 0 to 9) register. When the PDi_j (j = 0 to 7) bit in the PDi register is set to 0 (input mode), the pin input level is read. When the PDi_j bit in the PDi register is set to 1 (output mode), the port latch is read. 1: The I/O port input function reads the pin input level regardless of the PDi register.	R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

IOINSEL Bit (I/O port input function select bit)

The IOINSEL bit is used to select the pin level of an I/O port when the PDi_j (j = 0 to 7) bit in the PDi (i = 0 to 9) register is set to 1 (output mode). When this bit is set to 1, the I/O port input function reads the pin input level regardless of the PDi register.

Table 7.4 lists I/O Port Values Read by Using IOINSEL Bit. The IOINSEL bit can be used to change the input function of all I/O ports except P4_2.

Table 7.4 I/O Port Values Read by Using IOINSEL Bit

PDi_j bit in PDi register	0 (input mode)		1 (output mode)	
IOINSEL bit	0	1	0	1
I/O port values read	Pin input level		Port latch value	Pin input level

7.4.18 Pull-Up Control Register 0 (PUR0)

Address 01E0h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PU07	PU06	PU05	PU04	PU03	PU02	PU01	PU00
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PU00	P0_0 to P0_3 pull-up	0: Not pulled up 1: Pulled up (1)	R/W
b1	PU01	P0_4 to P0_7 pull-up		R/W
b2	PU02	P1_0 to P1_3 pull-up		R/W
b3	PU03	P1_4 to P1_7 pull-up		R/W
b4	PU04	P2_0 to P2_3 pull-up		R/W
b5	PU05	P2_4 to P2_7 pull-up		R/W
b6	PU06	P3_0 to P3_3 pull-up		R/W
b7	PU07	P3_4 to P3_7 pull-up		R/W

Note:
1. When this bit is set to 1 (pulled up), the pin whose port direction bit is set to 0 (input mode) is pulled up.

   For pins used as input, the setting values in the PUR0 register are valid.

7.4.19 Pull-Up Control Register 1 (PUR1)

Address 01E1h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PU17	PU16	PU15	PU14	PU13	PU12	PU11	PU10
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PU10	P4_3 pull-up	0: Not pulled up	R/W
b1	PU11	P4_4 to P4_7 pull-up	1: Pulled up (1)	R/W
b2	PU12	P5_0 to P5_3 pull-up		R/W
b3	PU13	P5_4 to P5_7 pull-up		R/W
b4	PU14	P6_0 to P6_3 pull-up		R/W
b5	PU15	P6_4 to P6_7 pull-up		R/W
b6	PU16	P7_0 to P7_3 pull-up		R/W
b7	PU17	P7_4 to P7_7 pull-up		R/W

Note:
1. When this bit is set to 1 (pulled up), the pin whose port direction bit is set to 0 (input mode) is pulled up.

   For pins used as input, the setting values in the PUR1 register are valid.

7.4.20 Pull-Up Control Register 2 (PUR2)

Address 01E2h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	PU23	PU22	PU21	PU20
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PU20	P8_0 to P8_3 pull-up	0: Not pulled up	R/W
b1	PU21	P8_4 to P8_7 pull-up	1: Pulled up (1)	R/W
b2	PU22	P9_0 to P9_3 pull-up		R/W
b3	PU23	P9_4 and P9_5 pull-up		R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

Note:
1. When this bit is set to 1 (pulled up), the pin whose port direction bit is set to 0 (input mode) is pulled up.

   For pins used as input, the setting values in the PUR2 register are valid.

7.4.21 Input Threshold Control Register 0 (VLT0)

Address 01F5h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VLT07	VLT06	VLT05	VLT04	VLT03	VLT02	VLT01	VLT00
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	VLT00	P0 input level select bit	b1 b0 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b1	VLT01			R/W
b2	VLT02	P1 input level select bit	b3 b2 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b3	VLT03			R/W
b4	VLT04	P2 input level select bit	b5 b4 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b5	VLT05			R/W
b6	VLT06	P3 input level select bit	b7 b6 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b7	VLT07			R/W

The VLT0 register selects the voltage level of the input threshold values for ports P0 to P3. Bits VLT00 to VLT07 are used to select the input threshold values among three voltage levels (0.35 VCC, 0.50 VCC, and 0.70 VCC) for every eight pins.

7.4.22 Input Threshold Control Register 1 (VLT1)

Address 01F6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VLT17	VLT16	VLT15	VLT14	VLT13	VLT12	VLT11	VLT10
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	VLT10	P4_2 to P4_7 input level select bit	b1 b0 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b1	VLT11			R/W
b2	VLT12	P5 input level select bit	b3 b2 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b3	VLT13			R/W
b4	VLT14	P6 input level select bit	b5 b4 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b5	VLT15			R/W
b6	VLT16	P7 input level select bit	b7 b6 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b7	VLT17			R/W

The VLT1 register selects the voltage level of the input threshold values for ports P4_2 to P4_7, P5, P6, and P7. Bits VLT10 to VLT17 are used to select the input threshold values among three voltage levels (0.35 VCC, 0.50 VCC, and 0.70 VCC).

7.4.23 Input Threshold Control Register 2 (VLT2)

Address 01F7h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	VLT23	VLT22	VLT21	VLT20
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	VLT20	P8 input level select bit	b1 b0 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b1	VLT21			R/W
b2	VLT22	P9_0 to P9_5 input level select bit	b3 b2 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b3	VLT23			R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

The VLT2 register selects the voltage level of the input threshold values for ports P8 and P9_0 to P9_5. Bits VLT20 to VLT23 are used to select the input threshold values among three voltage levels (0.35 VCC, 0.50 VCC, and 0.70 VCC).

7.5 Port Settings

Tables 7.5 to 7.95 list the port settings.

Table 7.5 Port P0_0/AN7

Register	PD0	ADINSEL					Function
Bit	PD0_0	CH			ADGSEL		
		2	1	0	1	0	
Setting Value	0	X	X	X	X	X	Input port (1)
	1	X	X	X	X	X	Output port
	0	1	1	1	0	0	A/D converter input (AN7) (1)

X: 0 or 1

Note:

1. Pulled up by setting the PU00 bit in the PUR0 register to 1.

Table 7.6 Port P0_1/AN6/TXD1

Register	PD0	ADINSEL					U1SR		U1MR			Function
Bit	PD0_1	CH			ADGSEL		TXD1SEL		SMD			
		2	1	0	1	0	1	0	2	1	0	
Setting Value	0	X	X	X	X	X	Other than 01b		X	X	X	Input port (1)
	1	X	X	X	X	X	Other than 01b		X	X	X	Output port
	0	1	1	0	0	0	Other than 01b		X	X	X	A/D converter input (AN6) (1)
	X	X	X	X	X	X	0	1	0	0	1	TXD1 output (2)
									1		0	
										1	1	
											0	

X: 0 or 1

Notes:

1. Pulled up by setting the PU00 bit in the PUR0 register to 1.
2. N-channel open-drain output by setting the NCH bit in the U1C0 register to 1.

Table 7.7 Port P0_2/AN5/RXD1

Register	PD0	ADINSEL					U1SR		Function
Bit	PD0_2	CH			ADGSEL		RXD1SEL		
		2	1	0	1	0	1	0	
Setting Value	0	X	X	X	X	X	X	X	Input port (1)
	1	X	X	X	X	X	X	X	Output port
	0	1	0	1	0	0	Other than 01b		A/D converter input (AN5) (1)
	0	X	X	X	X	X	0	1	RXD1 input (1)

X: 0 or 1

Note:

1. Pulled up by setting the PU00 bit in the PUR0 register to 1.

Table 7.8 Port P0_3/AN4/CLK1

Register	PD0	ADINSEL					U1SR		U1MR				Function
Bit	PD0_3	CH			ADGSEL		CLK1SEL		SMD			CKDIR	
		2	1	0	1	0	1	0	2	1	0		
Setting Value	0	X	X	X	X	X	Other than 01b		X	X	X	X	Input port (1)
	1	X	X	X	X	X	Other than 01b		X	X	X	X	Output port
	0	1	0	0	0	0	Other than 01b		X	X	X	X	A/D converter input (AN4) (1)
	0	X	X	X	X	X	0	1	X	X	X	1	CLK1 (external clock) input (1)
	X	X	X	X	X	X	0	1	0	0	1	0	CLK1 (internal clock) output

X: 0 or 1

Note:

1. Pulled up by setting the PU00 bit in the PUR0 register to 1.

Table 7.9 Port P0_4/AN3/TREO

Register	PD0	ADINSEL					TIMSR	TRECR1	Function
Bit	PD0_4	CH			ADGSEL		TREOSEL0	TOENA	
		2	1	0	1	0			
Setting Value	0	X	X	X	X	X	Other than 01b		Input port (1)
	1	X	X	X	X	X	Other than 01b		Output port
	0	0	1	1	0	0	Other than 01b		A/D converter input (AN3) (1)
	X	X	X	X	X	X	0	1	TREO output

X: 0 or 1

Note:

1. Pulled up by setting the PU01 bit in the PUR0 register to 1.

Table 7.10 Port P0_5/AN2

Register	PD0	ADINSEL					Function
Bit	PD0_5	CH			ADGSEL		
		2	1	0	1	0	
Setting Value	0	X	X	X	X	X	Input port (1)
	1	X	X	X	X	X	Output port
	0	0	1	0	0	0	A/D converter input (AN2) (1)

X: 0 or 1

Note:

1. Pulled up by setting the PU01 bit in the PUR0 register to 1.

Table 7.11 Port P0_6/AN1

Register	PD0	ADINSEL					Function
Bit	PD0_6	CH			ADGSEL		
		2	1	0	1	0	
Setting Value	0	X	X	X	X	X	Input port (1)
	1	X	X	X	X	X	Output port
	0	0	0	1	0	0	A/D converter input (AN1) (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU01 bit in the PUR0 register to 1.

Table 7.12 Port P0_7/AN0

Register	PD0	ADINSEL					Function
Bit	PD0_7	CH			ADGSEL		
		2	1	0	1	0	
Setting Value	0	X	X	X	X	X	Input port (1)
	1	X	X	X	X	X	Output port
	0	0	0	0	0	0	A/D converter input (AN0) (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU01 bit in the PUR0 register to 1.

Table 7.13 Port P1_0/$\overline{\text{KI0}}$/AN8

Register	PD1	KIEN	ADINSEL					Function
Bit	PD1_0	KI0EN	CH			ADGSEL		
			2	1	0	1	0	
Setting Value	0	X	X	X	X	X	X	Input port (1)
	1	X	X	X	X	X	X	Output port
	0	1	X	X	X	X	X	$\overline{\text{KI0}}$ input (1)
	0	0	0	0	0	0	1	A/D converter input (AN8) (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU02 bit in the PUR0 register to 1.

Table 7.14 Port P1_1/$\overline{KI1}$/AN9

Register	PD1	KIEN	ADINSEL					Function
Bit	PD1_1	KI1EN	CH			ADGSEL		
			2	1	0	1	0	
Setting Value	0	X	X	X	X	X	X	Input port (1)
	1	X	X	X	X	X	X	Output port
	0	1	X	X	X	X	X	$\overline{KI1}$ input (1)
	0	0	0	0	1	0	1	A/D converter input (AN9) (1)

X: 0 or 1

Note:

1. Pulled up by setting the PU02 bit in the PUR0 register to 1.

Table 7.15 Port P1_2/$\overline{KI2}$/AN10

Register	PD1	KIEN	ADINSEL					Function
Bit	PD1_2	KI2EN	CH			ADGSEL		
			2	1	0	1	0	
Setting Value	0	X	X	X	X	X	X	Input port (1)
	1	X	X	X	X	X	X	Output port
	0	1	X	X	X	X	X	$\overline{KI2}$ input (1)
	0	0	0	1	0	0	1	A/D converter input (AN10) (1)

X: 0 or 1

Note:

1. Pulled up by setting the PU02 bit in the PUR0 register to 1.

Table 7.16 Port P1_3/$\overline{KI3}$/AN11/TRBO

Register	PD1	KIEN	ADINSEL					TRBRCSR		Timer RB Setting	Function
Bit	PD1_3	KI3EN	CH			ADGSEL		TRBOSEL		—	
			2	1	0	1	0	1	0		
Setting Value	0	X	X	X	X	X	X	1	1	X	Input port (1, 2)
								0	1		
								0	0	Other than TRBO usage conditions	
	1	X	X	X	X	X	X	1	X	X	Output port
								0	1		
								0	0	Other than TRBO usage conditions	
	0	1	X	X	X	X	X	1	X	X	$\overline{KI3}$ input (1)
								0	1		
								0	0	Other than TRBO usage conditions	
	0	0	0	1	1	0	1	1	X	X	A/D converter input (AN11) (1)
								0	1		
								0	0	Other than TRBO usage conditions	
	X	X	X	X	X	X	X	0	0	Refer to **Table 7.81 TRBO Pin Setting**	TRBO output

X: 0 or 1

Notes:

1. Pulled up by setting the PU02 bit in the PUR0 register to 1.
2. Do not set bits TRBOSEL1 to TRBOSEL0 in the TRBRCSR register to 10b.

Table 7.17 Port P1_4/TXD0

Register	PD1	U0SR	U0MR			Function
Bit	PD1_4	TXD0SEL0	SMD			
			2	1	0	
Setting Value	0	0	X	X	X	Input port (1)
	1	0	X	X	X	Output port
	X	1	0	0	1	TXD0 output (2)
			1		0	
					1	
				1	0	

X: 0 or 1

Notes:
1. Pulled up by setting the PU03 bit in the PUR0 register to 1.
2. N-channel open-drain output by setting the NCH bit in the U0C0 register to 1.

Table 7.18 Port P1_5/RXD0/TRAIO0/$\overline{\text{INT1}}$

Register	PD1	U0SR	TRASR		TRA0IOC	TRA0MR			INTSR			INTEN	Function
Bit	PD1_5	RXD0SEL0	TRAIOSEL		TOPCR	TMOD			INT1SEL			INT1EN	
			1	0		2	1	0	2	1	0		
Setting Value	0	X	Other than 10b		X	X	X	X	X	X	X	X	Input port (1)
	1	X	Other than 10b		X	X	X	X	X	X	X	X	Output port
	0	1	Other than 10b		X	X	X	X	X	X	X	X	RXD0 input (1)
	0	X	1	0	0	Other than 000b, 001b			X	X	X	X	TRAIO0 input (1)
	0	X	Other than 10b		X	X	X	X	0	0	1	1	$\overline{\text{INT1}}$ input (1)
	0	X	1	0	0	Other than 000b, 001b			0	0	1	1	TRAIO0/$\overline{\text{INT1}}$ input (1)
	X	X	1	0	0	0	0	1	X	X	X	X	TRAIO0 pulse output
	0	1	1	0	0	Master mode: 000b Slave mode: 011b			X	X	X	X	TRAIO0/RXD0 input (Hardware LIN0)
	0	1	1	0	0				0	0	1	1	TRAIO0/RXD0/$\overline{\text{INT1}}$ input (Hardware LIN0)

X: 0 or 1

Note:
1. Pulled up by setting the PU03 bit in the PUR0 register to 1.

Table 7.19 Port P1_6/CLK0

Register	PD1	U0SR	U0MR				Function
Bit	PD1_6	CLK0SEL0	SMD			CKDIR	
			2	1	0		
Setting Value	0	0	X	X	X	X	Input port (1)
	1	0	X	X	X	X	Output port
	0	1	X	X	X	1	CLK0 (external clock) input (1)
	X	1	0	0	1	0	CLK0 (internal clock) output

X: 0 or 1

Note:
1. Pulled up by setting the PU03 bit in the PUR0 register to 1.

Table 7.20 Port P1_7/$\overline{\text{INT1}}$/TRAIO0

Register	PD1	TRASR		TRA0IOC	TRA0MR			INTSR			INTEN	Function
Bit	PD1_7	TRAIOSEL		TOPCR	TMOD			INT1SEL			INT1EN	
		1	0		2	1	0	2	1	0		
Setting Value	0	Other than 01b		X	X	X	X	X	X	X	X	Input port (1)
	1	Other than 01b		X	X	X	X	X	X	X	X	Output port
	0	0	1	0	Other than 000b, 001b			X	X	X	X	TRAIO0 input (1)
	0	Other than 01b		X	X	X	X	0	0	0	1	$\overline{\text{INT1}}$ input (1)
	0	0	1	0	Other than 000b, 001b			0	0	0	1	TRAIO0/$\overline{\text{INT1}}$ input (1)
	X	0	1	0	0	0	1	X	X	X	X	TRAIO0 pulse output

X: 0 or 1

Note:

1. Pulled up by setting the PU03 bit in the PUR0 register to 1.

Table 7.21 Port P2_0/TRDIOA0/TRDCLK

Register	PD2	TRDPSR0	Timer RD Setting	Function
Bit	PD2_0	TRDIOA0SEL0	—	
Setting Value	0	0	X	Input port (1)
	1	0	X	Output port
	0	1	Refer to **Table 7.86 TRDIOA0 Pin Setting**	TRDIOA0 input (1)
	X	1	Refer to **Table 7.86 TRDIOA0 Pin Setting**	TRDIOA0 output

X: 0 or 1

Note:

1. Pulled up by setting the PU04 bit in the PUR0 register to 1.

Table 7.22 Port P2_1/TRDIOB0

Register	PD2	TRDPSR0	Timer RD Setting	Function
Bit	PD2_1	TRDIOB0SEL0	—	
Setting Value	0	0	X	Input port (1)
	1	0	X	Output port
	0	1	Refer to **Table 7.87 TRDIOB0 Pin Setting**	TRDIOB0 input (1)
	X	1	Refer to **Table 7.87 TRDIOB0 Pin Setting**	TRDIOB0 output

X: 0 or 1

Note:

1. Pulled up by setting the PU04 bit in the PUR0 register to 1.

Table 7.23 Port P2_2/TRDIOC0

Register	PD2	TRDPSR0	Timer RD Setting	Function
Bit	PD2_2	TRDIOC0SEL0	—	
Setting Value	0	0	X	Input port (1)
	1	0	X	Output port
	0	1	Refer to **Table 7.88 TRDIOC0 Pin Setting**	TRDIOC0 input (1)
	X	1	Refer to **Table 7.88 TRDIOC0 Pin Setting**	TRDIOC0 output

X: 0 or 1
Note:
1. Pulled up by setting the PU04 bit in the PUR0 register to 1.

Table 7.24 Port P2_3/TRDIOD0

Register	PD2	TRDPSR0	Timer RD Setting	Function
Bit	PD2_3	TRDIOD0SEL0	—	
Setting Value	0	0	X	Input port (1)
	1	0	X	Output port
	0	1	Refer to **Table 7.89 TRDIOD0 Pin Setting**	TRDIOD0 input (1)
	X	1	Refer to **Table 7.89 TRDIOD0 Pin Setting**	TRDIOD0 output

X: 0 or 1
Note:
1. Pulled up by setting the PU04 bit in the PUR0 register to 1.

Table 7.25 Port P2_4/TRDIOA1

Register	PD2	TRDPSR1	Timer RD Setting	Function
Bit	PD2_4	TRDIOA1SEL0	—	
Setting Value	0	0	X	Input port (1)
	1	0	X	Output port
	0	1	Refer to **Table 7.90 TRDIOA1 Pin Setting**	TRDIOA1 input (1)
	X	1	Refer to **Table 7.90 TRDIOA1 Pin Setting**	TRDIOA1 output

X: 0 or 1
Note:
1. Pulled up by setting the PU05 bit in the PUR0 register to 1.

Table 7.26 Port P2_5/TRDIOB1

Register	PD2	TRDPSR1	Timer RD Setting	Function
Bit	PD2_5	TRDIOB1SEL0	—	
Setting Value	0	0	X	Input port (1)
	1	0	X	Output port
	0	1	Refer to **Table 7.91 TRDIOB1 Pin Setting**	TRDIOB1 input (1)
	X	1	Refer to **Table 7.91 TRDIOB1 Pin Setting**	TRDIOB1 output

X: 0 or 1
Note:
1. Pulled up by setting the PU05 bit in the PUR0 register to 1.

Table 7.27 Port P2_6/TRDIOC1

Register	PD2	TRDPSR1	Timer RD Setting	Function
Bit	PD2_6	TRDIOC1SEL0	—	
Setting Value	0	0	X	Input port (1)
	1	0	X	Output port
	0	1	Refer to **Table 7.92 TRDIOC1 Pin Setting**	TRDIOC1 input (1)
	X	1	Refer to **Table 7.92 TRDIOC1 Pin Setting**	TRDIOC1 output

X: 0 or 1

Note:

1. Pulled up by setting the PU05 bit in the PUR0 register to 1.

Table 7.28 Port P2_7/TRDIOD1

Register	PD2	TRDPSR1	Timer RD Setting	Function
Bit	PD2_7	TRDIOD1SEL0	—	
Setting Value	0	0	X	Input port (1)
	1	0	X	Output port
	0	1	Refer to **Table 7.93 TRDIOD1 Pin Setting**	TRDIOD1 input (1)
	X	1	Refer to **Table 7.93 TRDIOD1 Pin Setting**	TRDIOD1 output

X: 0 or 1

Note:

1. Pulled up by setting the PU05 bit in the PUR0 register to 1.

Table 7.29 Port P3_0/TRAO0/TRGCLKA

Register	PD3	TRASR	TRA0IOC	TIMSR	TRGCR			Function
Bit	PD3_0	TRAOSEL0	TOENA	TRGCLKASEL	TCK			
					2	1	0	
Setting Value	0	0	X	X	X	X	X	Input port (1)
	1	0	X	X	X	X	X	Output port
	X	1	1	X	X	X	X	TRAO0 output
	0	0	X	1	1	0	1	TRGCLKA input (1)

X: 0 or 1

Note:

1. Pulled up by setting the PU06 bit in the PUR0 register to 1.

Table 7.30 Port P3_1/TRBO

Register	PD3	TRBRCSR		Timer RB Setting	Function
Bit	PD3_1	TRBOSEL			
		1	0		
Setting Value	0	1	1	X	Input port (1, 2)
		0	0		
		0	1	Other than TRBO usage conditions	
	1	1	X	X	Output port
		0	0		
		0	1	Other than TRBO usage conditions	
	X	0	1	Refer to **"Table 7.81 TRBO Pin Setting"**	TRBO output

X: 0 or 1

Notes:

1. Pulled up by setting the PU06 bit in the PUR0 register to 1.
2. Do not set bits TRBOSEL1 to TRBOSEL0 in the TRBRCSR register to 10b.

Table 7.31 Port P3_2 /INT1/INT2/TRGCLKB

Register	PD3	INTSR					INTEN		TIMSR	TRGCR			Function
Bit	PD3_2	INT1SEL			INT2SEL		INT1EN	INT2EN	TRGCLKBSEL	TCK			
		2	1	0	1	0				2	1	0	
Setting Value	0	X	X	X	X	X	X	X	X	X	X	X	Input port (1)
	1	X	X	X	X	X	X	X	X	X	X	X	Output port
	0	1	0	0	X	X	1	X	X	X	X	X	$\overline{\text{INT1}}$ input (1)
	0	X	X	X	0	1	X	1	X	X	X	X	$\overline{\text{INT2}}$ input (1)
	0	X	X	X	X	X	X	X	1	1	1	1	TRGCLKB input (1)

X: 0 or 1

Note:

1. Pulled up by setting the PU06 bit in the PUR0 register to 1.

Table 7.32 Port P3_3/INT3/CTS2/RTS2/SSI/SCS

Register	PD3	SSUIICSR		Synchronous Serial Communication Unit (Refer to **Table 26.4 Association between Communication Modes and I/O Pins**.)		SSMR2		INTSR		INTEN	U2SR1	U2MR			U2CO		Function
Bit	PD3_3	SSI SEL0	SCS SEL0	SSI output control	SSI input control	CSS		INT3SEL		INT3EN	CTS2SEL0	SMD			CRS	CRD	
						1	0	1	0			2	1	0			
Setting Value	0	0	1	X	X	X	X	X	X	X	0	X	X	X	X	X	Input port (1)
			X			0	0										
	1	0	1	X	X	X	X	X	X	X	0	X	X	X	X	X	Output port
			X			0	0										
	X	1	X	0	1	X	X	X	X	X	X	X	X	X	X	X	SSI input (1)
				1	0												SSI output (2)
	0	0	1	X	X	X	X	0	0	1	0	X	X	X	X	X	$\overline{\text{INT3}}$ input (1)
			X			0	0										
	X	0	0	X	X	0	1	X	X	X	X	X	X	X	X	X	$\overline{\text{SCS}}$ input (1)
						1	0										$\overline{\text{SCS}}$ output (3)
						1	1										
	0	0	1	X	X	X	X	X	X	X	1	Other than 000			0	0	$\overline{\text{CTS2}}$ input (1)
			0			0	0										
	X	0	1	X	X	X	X	X	X	X	1	Other than 000b			1	0	$\overline{\text{RTS2}}$ output
			0			0	0										

X: 0 or 1

Notes:

1. Pulled up by setting the PU06 bit in the PUR0 register to 1.
2. N-channel open-drain output by setting the SOOS bit in the SSMR2 register to 1 (N-channel open-drain output) and setting the BIDE bit in the SSMR2 register to 0 (standard mode).
3. N-channel open-drain output by setting the CSOS bit in the SSMR2 register to 1 (N-channel open-drain output).

Table 7.33 Port P3_4/TXD2/SDA2/RXD2/SCL2/SSI/$\overline{SCS}$

Register	PD3	SSUIICSR		SSMR2		Synchronous Serial Communication Unit (Refer to **Table 26.4 Association between Communication Modes and I/O Pins**.)		U2SR0						U2MR			U2SMR	Function
Bit	PD3_4	SCS SEL0	SSI SEL0	CSS		SSI output control	SSI input control	RXD2 SEL			TXD2 SEL			SMD			IICM	
				1	0			2	1	0	2	1	0	2	1	0		
Setting Value	0	0	1	X	X	X	X	Other than 001b			Other than 010b			X	X	X	X	Input port (1)
			0			0	0											
	1	0	1	X	X	X	X	Other than 001b			Other than 010b			X	X	X	X	Output port
			0			0	0											
	X	1	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	$\overline{SCS}$ input (1)
			0			0	0											
			1	10b or 11b		X	X											$\overline{SCS}$ output (2)
			0			0	0											
	X	X	0	X	X	0	1	X	X	X	X	X	X	X	X	X	X	SSI input (1)
						1	0											SSI output (3)
	0	0	1	X	X	X	X	0	0	1	Other than 010b			X	X	X	0	RXD2 input (1)
			0			0	0											
	0	0	1	X	X	X	X	0	0	1	Other than 010b			0	1	0	1	SCL2 input/output (4)
			0			0	0											
	X	0	1	X	X	X	X	X	X	X	0	1	0	0	0	1	X	TXD2 output (4)
														1	0	0		
			0			0	0							1	0	1		
														1	1	0		
	0	0	1	X	X	X	X	X	X	X	0	1	0	0	1	0	1	SDA2 output (4)
			0			0	0											

X: 0 or 1

Notes:
1. Pulled up by setting the PU07 bit in the PUR0 register to 1.
2. N-channel open-drain output by setting the CSOS bit in the SSMR2 register to 1 (N-channel open-drain output).
3. N-channel open-drain output by setting the SOOS bit in the SSMR2 register to 1 (N-channel open-drain output) and setting the BIDE bit in the SSMR2 register to 0 (standard mode).
4. N-channel open-drain output by setting the NCH bit in the U2C0 register to 1.

Table 7.34 Port P3_5/SSCK/CLK2

Register	PD3	Synchronous Serial Communication Unit (Refer to **Table 26.4 Association between Communication Modes and I/O Pins**.)		U2SR1		U2MR				Function
Bit	PD3_5	SSCK output control	SSCK input control	CLK2SEL		SMD			CKDIR	
				1	0	2	1	0		
Setting Value	0	0	0	Other than 01b		X	X	X	X	Input port (1)
	1	0	0	Other than 01b		X	X	X	X	Output port
	X	0	1	X	X	X	X	X	X	SSCK input (1)
	X	1	0	X	X	X	X	X	X	SSCK output (2)
	0	0	0	0	1	X	X	X	1	CLK2 input
	X	0	0	0	1	0	0	1	0	CLK2 output (3)

X: 0 or 1

Notes:
1. Pulled up by setting the PU07 bit in the PUR0 register to 1.
2. N-channel open-drain output by setting the SCKOS bit in the SSMR2 register to 1 (N-channel open-drain output).
3. N-channel open-drain output by setting the NODC bit in the U2SMR3 register to 1.

Table 7.35 Port P3_6/$\overline{\text{INT1}}$

Register	PD3	INTSR			INTEN	Function
Bit	PD3_6	INT1SEL			INT1EN	
		2	1	0		
Setting Value	0	X	X	X	X	Input port (1)
	1	X	X	X	X	Output port
	0	0	1	1	1	$\overline{\text{INT1}}$ input (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU07 bit in the PUR0 register to 1.

Table 7.36 Port P3_7/SSO/TXD2/SDA2/RXD2/SCL2/TRAO0

Register	PD3	Synchronous Serial Communication Unit (Refer to **Table 26.4 Association between Communication Modes and I/O Pins**.)		U2SR0						U2MR			U2SMR	TRASR	TRA0IOC	Function
Bit	PD3_7	SSO output control	SSO input control	RXD2SEL			TXD2SEL			SMD			IICM	TRAOSEL0	TOENA	
				2	1	0	2	1	0	2	1	0				
Setting Value	0	0	0	Other than 010b			Other than 001b			X	X	X	X	Other than 01b		Input port (1)
	1	0	0	Other than 010b			Other than 001b			X	X	X	X	Other than 01b		Output port
	X	0	1	X	X	X	X	X	X	X	X	X	X	X	X	SSO input (1)
	X	1	0	X	X	X	X	X	X	X	X	X	X	X	X	SSO output (2)
	0	0	0	0	1	0	Other than 001b			X	X	X	0	Other than 01b		RXD2 input (1)
	0	X 0	X 0	0	1	0	Other than 001b			0	1	0	1	X	X	SCL2 input/ output (3)
	X	0	0	X	X	X	0	0	1	0 1	0	1 0 1 0	X	X	X	TXD2 output (3)
	0	0	0	X	X	X	0	0	1	0	1	0	1	X	X	SDA2 input/ output (3)
	X	0	0	Other than 010b			Other than 001b			X	X	X	X	0	1	TRAO0 output (2)

X: 0 or 1
Notes:
1. Pulled up by setting the PU07 bit in the PUR0 register to 1.
2. N-channel open-drain output by setting the SOOS bit in the SSMR2 register to 1 (N-channel open-drain output).
3. N-channel open-drain output by setting the NCH bit in the U2C0 register to 1.

Table 7.37 Port P4_2/VREF

Register	ADCON1	Function
Bit	ADSTBY	
Setting Value	0	Input port
	1	Input port/VREF input

Table 7.38 Port P4_3

Register	PD4	Function
Bit	PD4_3	
Setting Value	0	Input port (1)
	1	Output port

Note:
1. Pulled up by setting the PU10 bit in the PUR1 register to 1.

Table 7.39 Port P4_4

Register	PD4	Function
Bit	PD4_4	
Setting Value	0	Input port (1)
	1	Output port

Note:
1. Pulled up by setting the PU11 bit in the PUR1 register to 1.

Table 7.40 Port P4_5/$\overline{\text{INT0}}$/$\overline{\text{ADTRG}}$

Register	PD4	INTEN	ADMOD		Function
Bit	PD4_5	INT0EN	ADCAP		
			1	0	
Setting Value	0	X	X	X	Input port (1)
	1	X	X	X	Output port
	0	1	X	X	$\overline{\text{INT0}}$ input (1)
	0	1	1	1	$\overline{\text{ADTRG}}$ input (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU11 bit in the PUR1 register to 1.

Table 7.41 Port P4_6/XIN

Register	PD4	CM0	CM1			Circuit specifications		Function
Bit	PD4_6	CM05	CM10	CM11	CM13	Oscillation buffer	Feedback resistor	
Setting Value	0	X	0	X	0	OFF	OFF	Input port (1)
	1	X	0	X	0	OFF	OFF	Output port
	X	0	0	0	1	ON	ON	XIN-XOUT oscillation (on-chip feedback resistor enabled)
				1		ON	OFF	XIN-XOUT oscillation (on-chip feedback resistor disabled)
		1		0		OFF	ON	XIN-XOUT oscillation stop (on-chip feedback resistor enabled)
				1		OFF	OFF	XIN-XOUT oscillation stop (on-chip feedback resistor disabled)
	X	X	1	X	X	OFF	OFF	Oscillation stop (STOP mode)

X: 0 or 1
Note:
1. Pulled up by setting the PU11 bit in the PUR1 register to 1.

Table 7.42 Port P4_7/XOUT

Register	PD4	CM0	CM1			Circuit specifications		Function
Bit	PD4_7	CM05	CM10	CM11	CM13	Oscillation buffer	Feedback resistor	
Setting Value	0	X	0	X	0	OFF	OFF	Input port (1)
	1	X	0	X	0	OFF	OFF	Output port
	X	0	0	0	1	ON	ON	XIN-XOUT oscillation (on-chip feedback resistor enabled)
				1		ON	OFF	XIN-XOUT oscillation (on-chip feedback resistor disabled)
		1		0		OFF	ON	XIN-XOUT oscillation stop (on-chip feedback resistor enabled)
				1		OFF	OFF	XIN-XOUT oscillation stop (on-chip feedback resistor disabled)
	X	X	1	X	X	OFF	OFF	Oscillation stop (STOP mode)

X: 0 or 1
Note:
1. Pulled up by setting the PU11 bit in the PUR1 register to 1.

Table 7.43 Port P5_0/TRCCLK

Register	PD5	TRBRCSR			TRCCR1			Function
Bit	PD5_0	TRCCLKSEL			TCK			
		2	1	0	2	1	0	
Setting Value	0	X	X	X	X	X	X	Input port (1)
	1	X	X	X	X	X	X	Output port
	0	1	0	0	1	0	1	TRCCLK input (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU12 bit in the PUR1 register to 1.

Table 7.44 Port P5_1/TRCIOA/TRCTRG

Register	PD5	TRCPSR0			Timer RC Setting			Function
Bit	PD5_1	TRCIOASEL						
		2	1	0				
Setting Value	0	Other than 101b			X	X	X	Input port (1)
	1	Other than 101b			X	X	X	Output port
	0	1	0	1	Refer to **Table 7.82 TRCIOA Pin Setting**			TRCIOA input(1)
	X							TRCIOA output

X: 0 or 1
Note:
1. Pulled up by setting the PU12 bit in the PUR1 register to 1.

Table 7.45 Port P5_2/TRCIOB

Register	PD5	TRCPSR0			Timer RC Setting			Function
Bit	PD5_2	TRCIOBSEL						
		2	1	0				
Setting Value	0	Other than 111b			X	X	X	Input port (1)
	1	Other than 111b			X	X	X	Output port
	0	1	1	1	Refer to **Table 7.83 TRCIOB Pin Setting**			TRCIOB input(1)
	X							TRCIOB output

X: 0 or 1
Note:
1. Pulled up by setting the PU12 bit in the PUR1 register to 1.

Table 7.46 Port P5_3/TRCIOC

Register	PD5	TRCPSR1			Timer RC Setting			Function
Bit	PD5_3	TRCIOCSEL						
		2	1	0				
Setting Value	0	Other than 110b			X	X	X	Input port (1)
	1	Other than 110b			X	X	X	Output port
	0	1	1	0	Refer to **Table 7.84 TRCIOC Pin Setting**			TRCIOC input(1)
	X							TRCIOC output

X: 0 or 1
Note:
1. Pulled up by setting the PU12 bit in the PUR1 register to 1.

Table 7.47 Port P5_4/TRCIOD

Register	PD5	TRCPSR1			Timer RC Setting			Function
Bit	PD5_4	TRCIODSEL						
		2	1	0				
Setting Value	0	Other than 110b			X	X	X	Input port (1)
	1	Other than 110b			X	X	X	Output port
	0	1	1	0	Refer to **Table 7.85 TRCIOD Pin Setting**			TRCIOD input(1)
	X							TRCIOD output

X: 0 or 1
Note:
1. Pulled up by setting the PU13 bit in the PUR1 register to 1.

Table 7.48 Port P5_5

Register	PD5	Function
Bit	PD5_5	
Setting Value	0	Input port (1)
	1	Output port

X: 0 or 1
Note:
1. Pulled up by setting the PU13 bit in the PUR1 register to 1.

Table 7.49 Port P5_6/TRGIOA

Register	PD5	TIMSR	Timer RG Setting			Function
Bit	PD5_6	TRGIOASEL				
Setting Value	0	0	X	X	X	Input port (1)
	1	0	X	X	X	Output port
	0	1	Refer to **Table 7.94 TRGIOA Pin Setting**			TRGIOA input (1)
	X					TRGIOA output

X: 0 or 1
Note:
1. Pulled up by setting the PU13 bit in the PUR1 register to 1.

Table 7.50 Port P5_7/TRGIOB

Register	PD5	TIMSR	Timer RG Setting			Function
Bit	PD5_7	TRGIOBSEL				
Setting Value	0	0	X	X	X	Input port (1)
	1	0	X	X	X	Output port
	0	1	Refer to **Table 7.95 TRGIOB Pin Setting**			TRGIOB input (1)
	X					TRGIOB output

X: 0 or 1
Note:
1. Pulled up by setting the PU13 bit in the PUR1 register to 1.

Table 7.51 Port P6_0/TREO

Register	PD6	TIMSR	TRECR1	Function
Bit	PD6_0	TREOSEL0	TOENA	
Setting Value	0	Other than 11b		Input port (1)
	1	Other than 11b		Output port
	X	1	1	TREO output

X: 0 or 1
Note:
1. Pulled up by setting the PU14 bit in the PUR1 register to 1.

Table 7.52 Port P6_1/CTX0

Register	PD6	C0CTL	Function
Bit	PD6_1	CPE	
Setting Value	0	0	Input port (1)
	1	0	Output port
	X	1	CTX0 output

Note:
1. Pulled up by setting the PU14 bit in the PUR1 register to 1.

Table 7.53 Port P6_2/CRX0

Register	PD6	C0CTL	Function
Bit	PD6_2	CPE	
Setting Value	0	0	Input port (1)
	1	0	Output port
	X	1	CRX0 input (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU14 bit in the PUR1 register to 1.

Table 7.54 Port P6_3/TRAO1/TXD1

Register	PD6	U1SR		U1MR			TRA1IOC	Function
Bit	PD6_3	TXD1SEL		SMD			TOENA	
		1	0	2	1	0		
Setting Value	0	Other than 10b		X	X	X	0	Input port (1)
	1	Other than 10b		X	X	X	0	Output port
	X	1	0	0	0	1	X	TXD1 output (2)
				1	0	0		
				1	0	1		
				1	1	0		
	X	Other than 10b		X	X	X	1	TRAO1 output

X: 0 or 1
Notes:
1. Pulled up by setting the PU14 bit in the PUR1 register to 1.
2. N-channel open-drain output by setting the NCH bit in the U1C0 register to 1.

Table 7.55 Port P6_4/$\overline{\text{INT2}}$/TRAIO1/RXD1

Register	PD6	U1SR		TRASR	TRA1IOC	TRA1MR			INTSR		INTEN	Function
Bit	PD6_4	RXD1SEL		TRAIO1SEL0	TOPCR	TMOD			INT2SEL		INT2EN	
		1	0			2	1	0	1	0		
Setting Value	0	X	X	0	X	X	X	X	X	X	X	Input port (1)
	1	X	X	0	X	X	X	X	X	X	X	Output port
	0	1	0	0	X	X	X	X	X	X	X	RXD1 input (1)
	0	X	X	1	0	Other than 000b and 001b			X	X	X	TRAIO1 input (1)
	0	X	X	0	X	X	X	X	1	0	1	$\overline{\text{INT2}}$ input (1)
	0	X	X	1	0	Other than 000b and 001b			1	0	1	TRAIO1/$\overline{\text{INT2}}$ input (1)
	X	X	X	1	0	0	0	1	X	X	X	TRAIO1 pulse output
	0	1	0	1	0	Master mode: 000b Slave mode: 011b			X	X	X	TRAIO1/RXD1 input (Hardware LIN1)
	0	1	0	1	0				1	0	1	TRAIO1/RXD1/$\overline{\text{INT2}}$ input (Hardware LIN1)

X: 0 or 1

Note:

1. Pulled up by setting the PU15 bit in the PUR1 register to 1.

Table 7.56 Port P6_5/$\overline{\text{INT4}}$/CLK2/CLK1

Register	PD6	INTEN1	U2SR1		U2MR				U1SR		U1MR				Function
Bit	PD6_5	INT4EN	CLK2SEL		SMD			CKDIR	CLK1SEL		SMD			CKDIR	
			1	0	2	1	0		1	0	2	1	0		
Setting Value	0	X	Other than 11b		X	X	X	X	Other than 11b		X	X	X	X	Input port (1)
	1	X	Other than 11b		X	X	X	X	Other than 11b		X	X	X	X	Output port
	0	1	Other than 11b		X	X	X	X	Other than 11b		X	X	X	X	$\overline{\text{INT4}}$ input (1)
	0	X	1	1	X	X	X	1	Other than 11b		X	X	X	X	CLK2 (external clock) input (1)
	X	X	1	1	0	0	1	0	Other than 11b		X	X	X	X	CLK2 (internal clock) output (2)
	0	X	X	X	X	X	X	X	1	1	X	X	X	1	CLK1 (external clock) input (1)
	X	X	X	X	X	X	X	X	1	1	0	0	1	0	CLK1 (internal clock) output

X: 0 or 1

Notes:

1. Pulled up by setting the PU15 bit in the PUR1 register to 1.
2. N-channel open-drain output by setting the NODC bit in the U2SMR3 register to 1.

Table 7.57 Port P6_6/$\overline{\text{INT2}}$/TXD2/SDA2

Register	PD6	INTSR		INTEN	U2SR0			U2MR			U2SMR	Function
Bit	PD6_6	INT2SEL		INT2EN	TXD2SEL			SMD			IICM	
		1	0		2	1	0	2	1	0		
Setting Value	0	X	X	X	Other than 101b			X	X	X	X	Input port (1)
	1	X	X	X	Other than 101b			X	X	X	X	Output port
	0	0	0	1	Other than 101b			X	X	X	X	$\overline{\text{INT2}}$ input (1)
	X	X	X	X	1	0	1	0	0	1	X	TXD2 output (2)
								1		0		
								0	1	1		
								1		0		
	0	X	X	X	1	0	1	0	1	0	1	SDA2 input/output (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU15 bit in the PUR1 register to 1.
2. N-channel open-drain output by setting the NCH bit in the U2C0 register to 1.

Table 7.58 Port P6_7/$\overline{\text{INT3}}$/RXD2/SCL2

Register	PD6	INTSR		INTEN	U2SR0			U2MR			U2SMR	Function
Bit	PD6_7	INT3SEL		INT3EN	RXD2SEL			SMD			IICM	
		1	0		2	1	0	2	1	0		
Setting Value	0	X	X	X	Other than 101b			X	X	X	X	Input port (1)
	1	X	X	X	Other than 101b			X	X	X	X	Output port
	0	1	0	1	Other than 101b			X	X	X	X	$\overline{\text{INT3}}$ input (1)
	0	X	X	X	1	0	1	X	X	X	0	RXD2 input (1)
	0	X	X	X	1	0	1	0	1	0	1	SCL2 input/output (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU15 bit in the PUR1 register to 1.
2. N-channel open-drain output by setting the NCH bit in the U2C0 register to 1.

Table 7.59 Port P7_0/AN12

Register	PD7	ADINSEL					Function
Bit	PD7_0	CH			ADGSEL		
		2	1	0	1	0	
Setting Value	0	X	X	X	X	X	Input port (1)
	1	X	X	X	X	X	Output port
	0	0	0	0	1	0	A/D converter input (AN12) (1)

X: 0 or 1

Note:
1. Pulled up by setting the PU16 bit in the PUR1 register to 1.

Table 7.60 Port P7_1/AN13

Register	PD7	ADINSEL					Function
Bit	PD7_1	CH			ADGSEL		
		2	1	0	1	0	
Setting Value	0	X	X	X	X	X	Input port (1)
	1	X	X	X	X	X	Output port
	0	0	0	1	1	0	A/D converter input (AN13) (1)

X: 0 or 1

Note:
1. Pulled up by setting the PU16 bit in the PUR1 register to 1.

Table 7.61 Port P7_2/AN14

Register	PD7	ADINSEL					Function
Bit	PD7_2	CH			ADGSEL		
		2	1	0	1	0	
Setting Value	0	X	X	X	X	X	Input port (1)
	1	X	X	X	X	X	Output port
	0	0	1	0	1	0	A/D converter input (AN14) (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU16 bit in the PUR1 register to 1.

Table 7.62 Port P7_3/AN15

Register	PD7	ADINSEL					Function
Bit	PD7_3	CH			ADGSEL		
		2	1	0	1	0	
Setting Value	0	X	X	X	X	X	Input port (1)
	1	X	X	X	X	X	Output port
	0	0	1	1	1	0	A/D converter input (AN15) (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU16 bit in the PUR1 register to 1.

Table 7.63 Port P7_4/AN16

Register	PD7	ADINSEL					Function
Bit	PD7_4	CH			ADGSEL		
		2	1	0	1	0	
Setting Value	0	X	X	X	X	X	Input port (1)
	1	X	X	X	X	X	Output port
	0	1	0	0	1	0	A/D converter input (AN16) (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU17 bit in the PUR1 register to 1.

Table 7.64 Port P7_5/AN17

Register	PD7	ADINSEL					Function
Bit	PD7_5	CH			ADGSEL		
		2	1	0	1	0	
Setting Value	0	X	X	X	X	X	Input port (1)
	1	X	X	X	X	X	Output port
	0	1	0	1	1	0	A/D converter input (AN17) (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU17 bit in the PUR1 register to 1.

Table 7.65 Port P7_6/AN18

Register	PD7	ADINSEL					Function
Bit	PD7_6	CH			ADGSEL		
		2	1	0	1	0	
Setting Value	0	X	X	X	X	X	Input port (1)
	1	X	X	X	X	X	Output port
	0	1	1	0	1	0	A/D converter input (AN18) (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU17 bit in the PUR1 register to 1.

Table 7.66 Port P7_7/AN19

Register	PD7	ADINSEL					Function
Bit	PD7_7	CH			ADGSEL		
		2	1	0	1	0	
Setting Value	0	X	X	X	X	X	Input port (1)
	1	X	X	X	X	X	Output port
	0	1	1	1	1	0	A/D converter input (AN19) (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU17 bit in the PUR1 register to 1.

Table 7.67 Port P8_0/TRFO00

Register	PD8	TRFOU	P8	Function
Bit	PD8_0	TRFOUT0	P8_0	
Setting Value	0	0	X	Input port (1)
	1	0	X	Output port
	X	1	1	TRFO00 output

X: 0 or 1
Note:
1. Pulled up by setting the PU20 bit in the PUR2 register to 1.

Table 7.68 Port P8_1/TRFO01

Register	PD8	TRFOU	P8	Function
Bit	PD8_1	TRFOUT1	P8_1	
Setting Value	0	0	X	Input port (1)
	1	0	X	Output port
	X	1	1	TRFO01 output

X: 0 or 1
Note:
1. Pulled up by setting the PU20 bit in the PUR2 register to 1.

Table 7.69 Port P8_2/TRFO02

Register	PD8	TRFOU	P8	Function
Bit	PD8_2	TRFOUT2	P8_2	
Setting Value	0	0	X	Input port (1)
	1	0	X	Output port
	X	1	1	TRFO02 output

X: 0 or 1
Note:
1. Pulled up by setting the PU20 bit in the PUR2 register to 1.

Table 7.70 Port P8_3/TRFO10/TRFI

Register	PD8	TRFOU	P8	TIMSR	Function
Bit	PD8_3	TRFOUT3	P8_3	TRFISEL0	
Setting Value	0	0	X	X	Input port (1)
	1	0	X	X	Output port
	X	1	1	X	TRFO10 output
	0	0	X	1	TRFI input (1)

X: 0 or 1
Note:
1. Pulled up by setting the PU20 bit in the PUR2 register to 1.

Table 7.71 Port P8_4/TRFO11

Register	PD8	TRFOU	P8	Function
Bit	PD8_4	TRFOUT4	P8_4	
Setting Value	0	0	X	Input port (1)
	1	0	X	Output port
	X	1	1	TRFO11 output

X: 0 or 1
Note:
1. Pulled up by setting the PU21 bit in the PUR2 register to 1.

Table 7.72 Port P8_5/TRFO12

Register	PD8	TRFOU	P8	Function
Bit	PD8_5	TRFOUT5	P8_5	
Setting Value	0	0	X	Input port (1)
	1	0	X	Output port
	X	1	1	TRFO12 output

X: 0 or 1
Note:
1. Pulled up by setting the PU21 bit in the PUR2 register to 1.

Table 7.73 Port P8_6

Register	PD8	Function
Bit	PD8_6	
Setting Value	0	Input port (1)
	1	Output port

X: 0 or 1
Note:
1. Pulled up by setting the PU21 bit in the PUR2 register to 1.

Table 7.74 Port P8_7

Register	PD8	Function
Bit	PD8_7	
Setting Value	0	Input port (1)
	1	Output port

X: 0 or 1
Note:
1. Pulled up by setting the PU21 bit in the PUR2 register to 1.

Table 7.75 Port P9_0

Register	PD9	Function
Bit	PD9_0	
Setting Value	0	Input port (1)
	1	Output port

X: 0 or 1
Note:
1. Pulled up by setting the PU22 bit in the PUR2 register to 1.

Table 7.76 Port P9_1

Register	PD9	Function
Bit	PD9_1	
Setting Value	0	Input port (1)
	1	Output port

X: 0 or 1
Note:
1. Pulled up by setting the PU22 bit in the PUR2 register to 1.

Table 7.77 Port P9_2

Register	PD9	Function
Bit	PD9_2	
Setting Value	0	Input port (1)
	1	Output port

X: 0 or 1
Note:
1. Pulled up by setting the PU22 bit in the PUR2 register to 1.

Table 7.78 Port P9_3

Register	PD9	Function
Bit	PD9_3	
Setting Value	0	Input port (1)
	1	Output port

X: 0 or 1
Note:
1. Pulled up by setting the PU22 bit in the PUR2 register to 1.

Table 7.79 Port P9_4

Register	PD9	Function
Bit	PD9_4	
Setting Value	0	Input port (1)
	1	Output port

X: 0 or 1
Note:
1. Pulled up by setting the PU23 bit in the PUR2 register to 1.

Table 7.80 Port P9_5

Register	PD9	Function
Bit	PD9_5	
Setting Value	0	Input port (1)
	1	Output port

X: 0 or 1
Note:
1. Pulled up by setting the PU23 bit in the PUR2 register to 1.

Table 7.81 TRBO Pin Setting

Register	TRBIOC	TRBMR		Function
Bit	TOCNT	TMOD1	TMOD0	
Setting value	0	0	1	Programmable waveform generation mode (pulse output)
	1	0	1	Programmable waveform generation mode (programmable output)
	0	1	0	Programmable one-shot generation mode
	0	1	1	Programmable wait one-shot generation mode

Table 7.82 TRCIOA Pin Setting

Register	TRCOER	TRCMR	TRCIOR0			TRCCR2		Function
Bit	EA	PWM2	IOA2	IOA1	IOA0	TCEG1	TCEG0	
Setting Value	0	1	0	0	1	X	X	Timer waveform output (output compare function)
				1	X			
	0	1	1	X	X	X	X	Timer mode (input capture function)
	1							
	1	0	X	X	X	0	1	PWM2 mode TRCTRG input
						1	X	

X: 0 or 1

Table 7.83 TRCIOB Pin Setting

Register	TRCOER	TRCMR		TRCIOR0			Function
Bit	EB	PWM2	PWMB	IOB2	IOB1	IOB0	
Setting Value	0	0	X	X	X	X	PWM2 mode waveform output
	0	1	1	X	X	X	PWM mode waveform output
	0	1	0	0	0	1	Timer waveform output (output compare function)
					1	X	
	0	1	0	1	X	X	Timer mode (input capture function)
	1						

X: 0 or 1

Table 7.84 TRCIOC Pin Setting

Register	TRCOER	TRCMR		TRCIOR1			Function
Bit	EC	PWM2	PWMC	IOC2	IOC1	IOC0	
Setting Value	0	1	1	X	X	X	PWM mode waveform output
	0	1	0	0	0	1	Timer waveform output (output compare function)
					1	X	
	0	1	0	1	X	X	Timer mode (input capture function)
	1						

X: 0 or 1

Table 7.85 TRCIOD Pin Setting

Register	TRCOER	TRCMR		TRCIOR1			Function
Bit	ED	PWM2	PWMD	IOD2	IOD1	IOD0	
Setting Value	0	1	1	X	X	X	PWM mode waveform output
	0	1	0	0	0	1	Timer waveform output (output compare function)
					1	X	
	0	1	0	1	X	X	Timer mode (input capture function)
	1						

X: 0 or 1

Table 7.86 TRDIOA0 Pin Setting

Register	TRDOER1	TRDFCR				TRDIORA0			Function
Bit	EA0	CMD1	CMD0	STCLK	PWM3	IOA2	IOA1	IOA0	
Setting Value	X	0	0	0	1	1	X	X	Timer mode (input capture function)
	X	X	X	1	1	0	0	0	External clock input (TRDCLK)
	0	0	0	0	0	X	X	X	PWM3 mode waveform output
	0	0	0	0	1	0	0	1	Timer mode waveform output (output compare function)
							1	X	

X: 0 or 1

Table 7.87 TRDIOB0 Pin Setting

Register	TRDOER1	TRDFCR			TRDPMR	TRDIORA0			Function
Bit	EB0	CMD1	CMD0	PWM3	PWMB0	IOB2	IOB1	IOB0	
Setting Value	X	0	0	1	0	1	X	X	Timer mode (input capture function)
	0	1	0	X	X	X	X	X	Complementary PWM mode waveform output
			1						
	0	0	1	X	X	X	X	X	Reset synchronous PWM mode waveform output
	0	0	0	0	X	X	X	X	PWM3 mode waveform output
	0	0	0	1	1	X	X	X	PWM mode waveform output
	0	0	0	1	0	0	0	1	Timer mode waveform output (output compare function)
							1	X	

X: 0 or 1

Table 7.88 TRDIOC0 Pin Setting

Register	TRDOER1	TRDFCR			TRDPMR	TRDIORC0			Function
Bit	EC0	CMD1	CMD0	PWM3	PWMC0	IOC2	IOC1	IOC0	
Setting Value	X	0	0	1	0	1	X	X	Timer mode (input capture function)
	0	1	0	X	X	X	X	X	Complementary PWM mode waveform output
			1						
	0	0	1	X	X	X	X	X	Reset synchronous PWM mode waveform output
	0	0	0	1	1	X	X	X	PWM mode waveform output
	0	0	0	1	0	0	0	1	Timer mode waveform output (output compare function)
							1	X	

X: 0 or 1

Table 7.89 TRDIOD0 Pin Setting

Register	TRDOER1	TRDFCR			TRDPMR	TRDIORC0			Function
Bit	ED0	CMD1	CMD0	PWM3	PWMD0	IOD2	IOD1	IOD0	
Setting Value	X	0	0	1	0	1	X	X	Timer mode (input capture function)
	0	1	0	X	X	X	X	X	Complementary PWM mode waveform output
			1						
	0	0	1	X	X	X	X	X	Reset synchronous PWM mode waveform output
	0	0	0	1	1	X	X	X	PWM mode waveform output
	0	0	0	1	0	0	0	1	Timer mode waveform output (output compare function)
							1	X	

X: 0 or 1

Table 7.90 TRDIOA1 Pin Setting

Register	TRDOER1	TRDFCR			TRDIORA1			Function
Bit	EA1	CMD1	CMD0	PWM3	IOA2	IOA1	IOA0	
Setting Value	X	0	0	1	1	X	X	Timer mode (input capture function)
	0	1	0	X	X	X	X	Complementary PWM mode waveform output
			1					
	0	0	1	X	X	X	X	Reset synchronous PWM mode waveform output
	0	0	0	1	0	0	1	Timer mode waveform output (output compare function)
						1	X	

X: 0 or 1

Table 7.91 TRDIOB1 Pin Setting

Register	TRDOER1	TRDFCR			TRDPMR	TRDIORA1			Function
Bit	EB1	CMD1	CMD0	PWM3	PWMB1	IOB2	IOB1	IOB0	
Setting Value	X	0	0	1	0	1	X	X	Timer mode (input capture function)
	0	1	0	X	X	X	X	X	Complementary PWM mode waveform output
			1						
	0	0	1	X	X	X	X	X	Reset synchronous PWM mode waveform output
	0	0	0	1	1	X	X	X	PWM mode waveform output
	0	0	0	1	0	0	0	1	Timer mode waveform output (output compare function)
							1	X	

X: 0 or 1

Table 7.92 TRDIOC1 Pin Setting

Register	TRDOER1	TRDFCR			TRDPMR	TRDIORC1			Function
Bit	EC1	CMD1	CMD0	PWM3	PWMC1	IOC2	IOC1	IOC0	
Setting Value	X	0	0	1	0	1	X	X	Timer mode (input capture function)
	0	1	0	X	X	X	X	X	Complementary PWM mode waveform output
			1						
	0	0	1	X	X	X	X	X	Reset synchronous PWM mode waveform output
	0	0	0	1	1	X	X	X	PWM mode waveform output
	0	0	0	1	0	0	0	1	Timer mode waveform output (output compare function)
							1	X	

X: 0 or 1

Table 7.93 TRDIOD1 Pin Setting

Register	TRDOER1	TRDFCR			TRDPMR	TRDIORC1			Function
Bit	ED1	CMD1	CMD0	PWM3	PWMD1	IOD2	IOD1	IOD0	
Setting Value	X	0	0	1	0	1	X	X	Timer mode (input capture function)
	0	1	0	X	X	X	X	X	Complementary PWM mode waveform output
			1						
	0	0	1	X	X	X	X	X	Reset synchronous PWM mode waveform output
	0	0	0	1	1	X	X	X	PWM mode waveform output
	0	0	0	1	0	0	0	1	Timer mode waveform output (output compare function)
							1	X	

X: 0 or 1

Table 7.94 TRGIOA Pin Setting

Register	TRGMR	TRGIOR			Function
Bit	PWM	IOA2	IOA1	IOA0	
Setting Value	1	X	X	X	PWM mode waveform output
	0	0	0	1	Timer waveform output (output compare function)
			1	0	
			1	1	
	0	1	X	X	Timer mode (input capture function)

X: 0 or 1

Table 7.95 TRGIOB Pin Setting

Register	TRGMR	TRGIOR			Function
Bit	PWM	IOB2	IOB1	IOB0	
Setting Value	0	0	0	1	Timer waveform output (output compare function)
			1	0	
			1	1	
	0	1	X	X	Timer mode (input capture function)

X: 0 or 1

7.6 Unassigned Pin Handling

Table 7.96 lists Unassigned Pin Handling.

Table 7.96 Unassigned Pin Handling

Pin Name	Connection
Ports P0, P1, P2, P3, P4_3 to P4_7, P5, P6, P7, P8, P9_0 to P9_5	• After setting to input mode, connect each pin to VSS via a resistor (pull-down) or connect each pin to VCC via a resistor (pull-up). (2) • After setting to output mode, leave these pins open. (1, 2)
Port P4_2/VREF	Connect to VCC
$\overline{\text{RESET}}$ (3)	Connect to VCC via a pull-up resistor (2)

Notes:
1. If these ports are set to output mode and left open, they remain in input mode until they are switched to output mode by a program. The voltage level of these pins may be undefined and the power current may increase while the ports remain in input mode.
   The content of the direction registers may change due to noise or program runaway caused by noise. In order to enhance program reliability, the program should periodically repeat the setting of the direction registers.
2. Connect these unassigned pins to the MCU using the shortest wire length (2 cm or less) possible.
3. When the power-on reset function is in use.

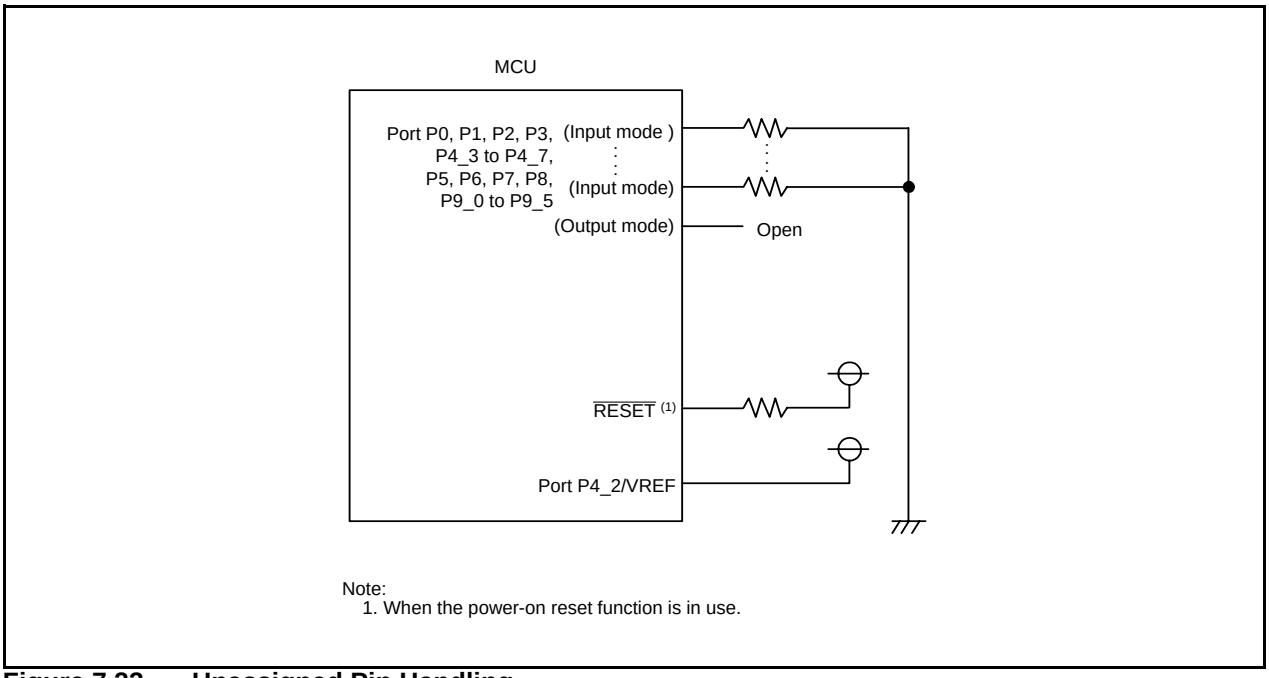


Figure 7.23 Unassigned Pin Handling

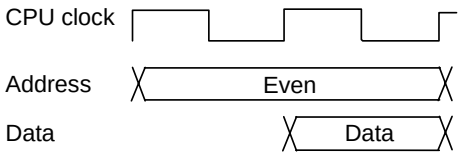
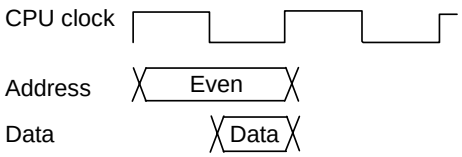
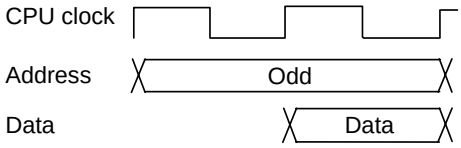
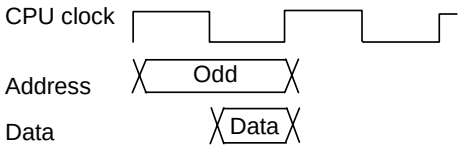
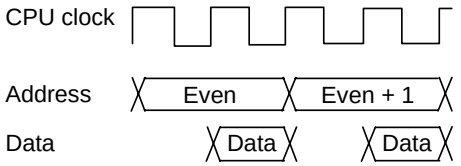
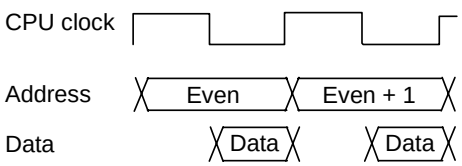
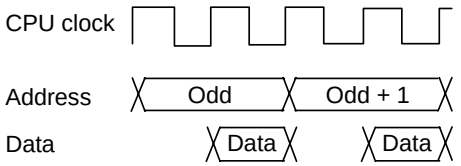
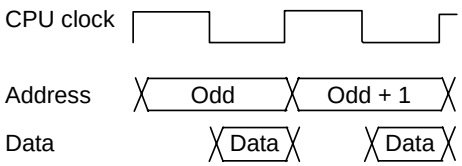
8. Bus

The bus cycles differ when accessing ROM, RAM, DTC vector area, DTC control data and when accessing SFR. Table 8.1 lists Bus Cycles by Access Area of This MCU (with Data Flash).
ROM, RAM, DTC vector area, DTC control data and SFR are connected to the CPU by an 8-bit bus. When accessing in word (16-bit) units, these areas are accessed twice in 8-bit units.
Table 8.2 shows Access Units and Bus Operations.

Table 8.1 Bus Cycles by Access Area of This MCU (with Data Flash)

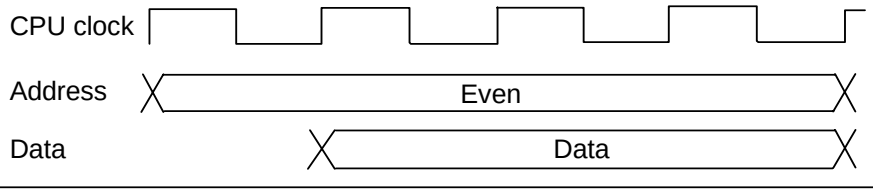
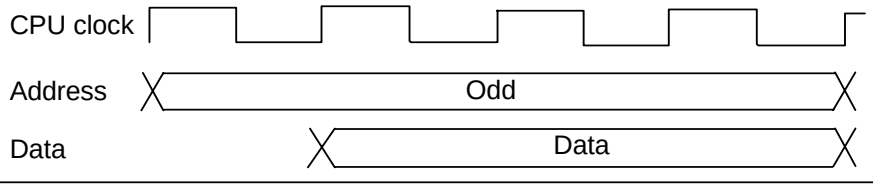
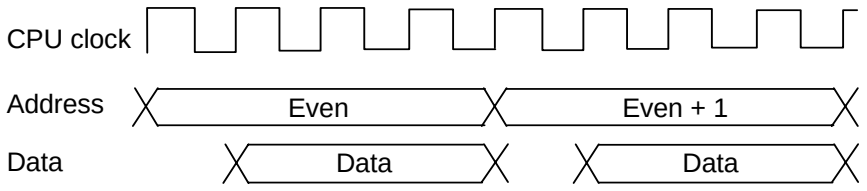
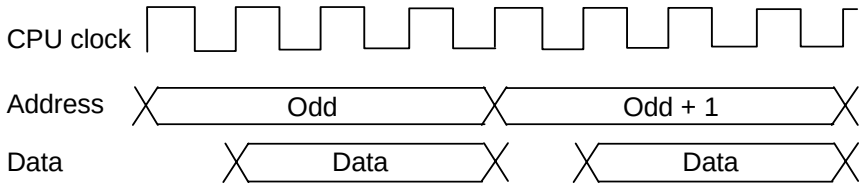
Access Area	Bus Cycle
SFR/Data flash	2 cycles of CPU clock
Program ROM/RAM	1 cycle of CPU clock

Table 8.2 Access Units and Bus Operations

Area	SFR, Data flash	ROM (program ROM), RAM, DTC vector area, DTC control data
Even address Byte access		
Odd address Byte access		
Even address Word access		
Odd address Word access		

To use the data flash with more than 16 MHz CPU clock, set the FMR23 bit in the FMR2 register (data flash access cycle selection bit) to 1 (4 cycles of the CPU clock). Table 8.3 shows the Access Unit and Bus Operations for accessing the data flash area.

Table 8.3 Access Units and Bus Operations for Accessing Data Flash Area (FMR23 = 1)

Even address Byte access	
Odd address Byte access	
Even address Word access	
Odd address Word access	

However, only the following SFRs are connected with the 16-bit bus:

Interrupts: Interrupt Control Register
Timer RC: Registers TRC, TRCGRA, TRCGRB, TRCGRC, and TRCGRD
Timer RD: Registers TRDi (i = 0, 1), TRDGRAi, TRDGRBi, TRDGRCi, and TRDGRDi
Timer RG: Registers TRG, TRGGRA, TRGGRB, TRGGRC, and TRGGRD
SSU: Registers SSTDR and SSRDR.
UART2: Registers U2MR, U2BRG, U2TB, U2C0, U2C1, U2RB, U2SMR5, U2SMR4, U2SMR3, U2SMR2, and U2SMR
A/D converter: Registers AD0, AD1, AD2, AD3, AD4, AD5, AD6, AD7, ADMOD, ADINSEL, ADCON0, and ADCON1
Address match interrupt: Registers RMAD0, AIER0, RMAD1, and AIER1
CAN module: All registers
Therefore, when the even address is accessed in 16-bit unit, the bus operation is the same as “Area: SFR, Data flash, Even address Byte Access” in Table 8.2 Access Units and Bus Operations, and 16-bit data is accessed at a time.

9. Clock Generation Circuit

The following four circuits are incorporated in the clock generation circuit:
- XIN clock oscillation circuit
- Low-speed on-chip oscillator
- High-speed on-chip oscillator
- Low-speed on-chip oscillator for watchdog timer

9.1 Overview

Table 9.1 lists the Specification Overview of Clock Generation Circuit. Figure 9.1 shows a Clock Generation Circuit. Figure 9.2 shows a Peripheral Function Clock and Figure 9.3 shows a Procedure for Reducing Internal Power Consumption Using VCA20 bit.

Table 9.1 Specification Overview of Clock Generation Circuit

Item	XIN Clock Oscillation Circuit	On-Chip Oscillator		Low-Speed On-Chip Oscillator for Watchdog Timer
		High-Speed On-Chip Oscillator	Low-Speed On-Chip Oscillator	
Applications	• CPU clock source • Peripheral function clock source	• CPU clock source • Peripheral function clock source • CPU and peripheral function clock source when XIN clock stops oscillating	• CPU clock source • Peripheral function clock source • CPU and peripheral function clock source when XIN clock stops oscillating	• Watchdog timer clock source
Clock frequency	0 to 20 MHz	Approx. 40 MHz (3)	Approx. 125 kHz	Approx. 125 kHz
Connectable oscillator	• Ceramic resonator • Crystal oscillator	–	–	–
Oscillator connect pins	XIN, XOUT (1)	– (1)	– (1)	–
Oscillation stop, restart function	Usable	Usable	Usable	Usable
Oscillator status after reset	Stop	Stop	Oscillate	Stop (4) Oscillate (5)
Others	Externally generated clock can be input (2)	–	–	–

Notes:
1. These pins can be used as P4_6 or P4_7 when using the on-chip oscillator clock as the CPU clock while the XIN clock oscillation circuit is not used.
2. To input an external clock, set the CM05 bit in the CM0 register to 1 (XIN clock stops), the CM11 bit in the CM1 register to 1 (internal feedback resistor disabled), and the CM13 bit to 1 (XIN-XOUT pin).
3. The clock frequency is automatically set to up to approximately 20 MHz by a divider when using the high-speed on-chip oscillator as the CPU clock source.
4. This applies when the CSPROINI bit in the OFS register is set to 1 (count source protection mode disabled after reset).
5. This applies when the CSPROINI bit in the OFS register is set to 0 (count source protection mode enabled after reset).

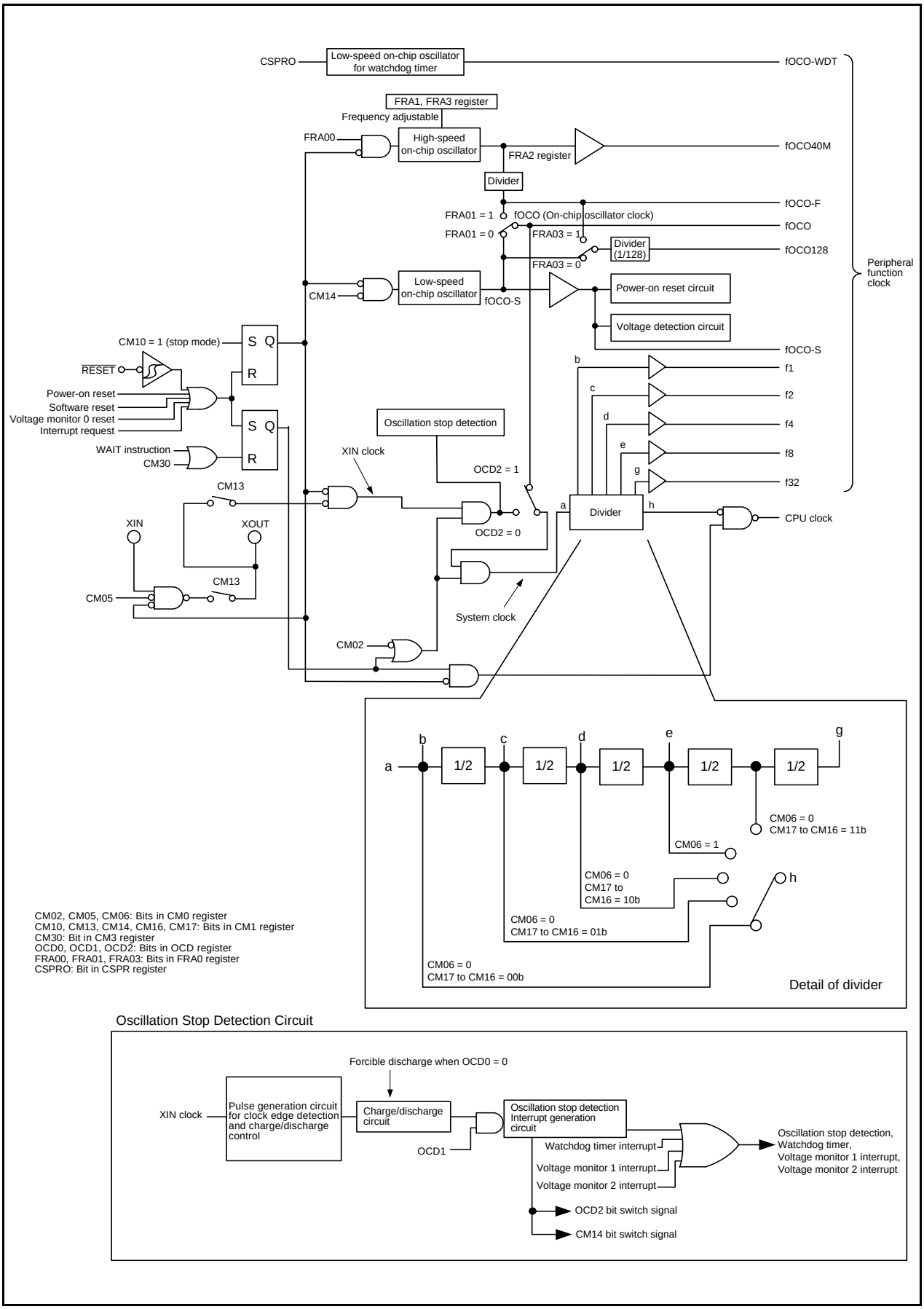


Figure 9.1 Clock Generation Circuit

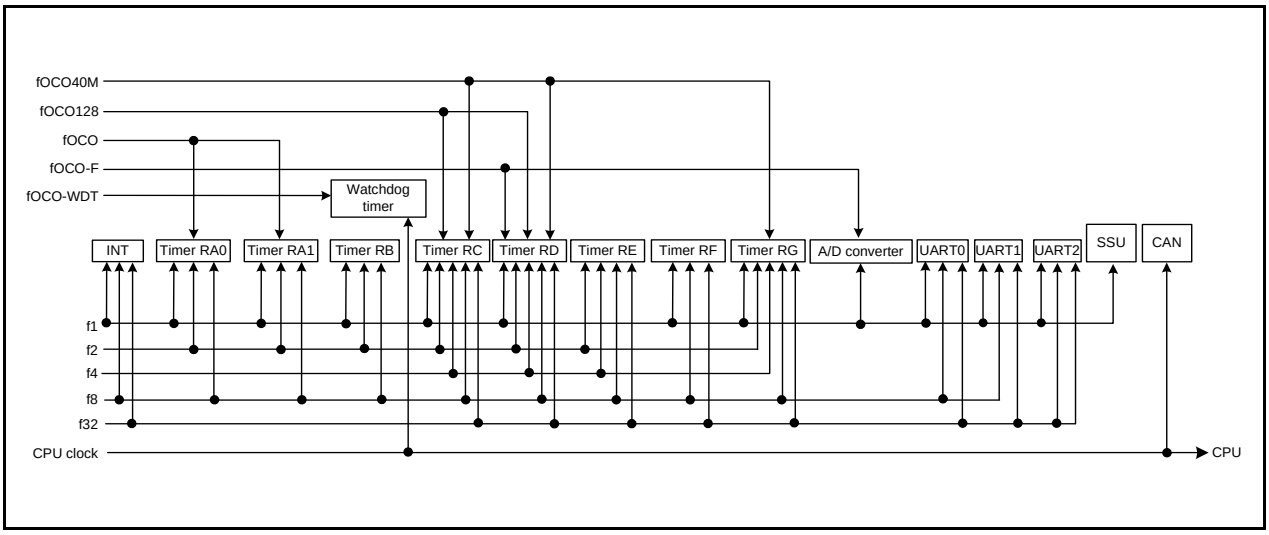


Figure 9.2 Peripheral Function Clock

9.2 Registers

9.2.1 System Clock Control Register 0 (CM0)

Address 0006h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	CM06	CM05	—	—	CM02	—	—
After Reset	0	0	1	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	CM02	Wait mode peripheral function clock stop bit	0: Peripheral function clock does not stop in wait mode 1: Peripheral function clock stops in wait mode	R/W
b3	—	Reserved bit	Set to 1.	R/W
b4	—	Reserved bit	Set to 0.	R/W
b5	CM05	XIN clock (XIN-XOUT) stop bit (1, 3)	0: XIN clock oscillates 1: XIN clock stops (2)	R/W
b6	CM06	CPU clock division select bit 0 (4)	0: Bits CM16 and CM17 in CM1 register enabled 1: Divide-by-8 mode	R/W
b7	—	Reserved bit	Set to 0.	R/W

Notes:
1. The CM05 bit stops the XIN clock when the high-speed on-chip oscillator mode or low-speed on-chip oscillator mode is selected. This bit cannot be used to detect whether the XIN clock has stopped. To stop the XIN clock, set the bits in the following order:
   (a) Set bits OCD1 to OCD0 in the OCD register to 00b.
   (b) Set the OCD2 bit to 1 (on-chip oscillator clock selected).
2. During external clock input, only the clock oscillation buffer stops and clock input is acknowledged.
3. Only when the CM05 bit is set to 1 (XIN clock stops) and the CM13 bit in the CM1 register is set to 0 (P4_6 and P4_7), P4_6 and P4_7 can be used as I/O ports.
4. When the MCU enters stop mode, the CM06 bit is set to 1 (divide-by-8 mode).

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM0 register.

9.2.2 System Clock Control Register 1 (CM1)

Address 0007h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM17	CM16	—	CM14	CM13	—	CM11	CM10
After Reset	0	0	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CM10	All clock stop control bit (2, 6)	0: Clock oscillates 1: All clocks stop (stop mode)	R/W
b1	CM11	XIN-XOUT on-chip feedback resistor select bit	0: On-chip feedback resistor enabled 1: On-chip feedback resistor disabled	R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	CM13	Port/XIN-XOUT switch bit (5)	0: I/O ports P4_6 and P4_7 1: XIN-XOUT pin	R/W
b4	CM14	Low-speed on-chip oscillator stop bit (3, 4)	0: Low-speed on-chip oscillator on 1: Low-speed on-chip oscillator off	R/W
b5	—	Reserved bit	Set to 1.	R/W
b6	CM16	CPU clock division select bit 1 (1)	b7 b6 0 0: No division mode 0 1: Divide-by-2 mode 1 0: Divide-by-4 mode 1 1: Divide-by-16 mode	R/W
b7	CM17			R/W

Notes:
1. When the CM06 bit is set to 0 (bits CM16 and CM17 enabled), bits CM16 and CM17 are enabled.
2. If the CM10 bit is set to 1 (stop mode), the on-chip feedback resistor is disabled.
3. When the OCD2 bit is set to 0 (XIN clock selected), the CM14 bit can be set to 1 (low-speed on-chip oscillator off). When the OCD2 bit is set to 1 (on-chip oscillator clock selected), the CM14 bit is set to 0 (low-speed on-chip oscillator on). It remains unchanged even if 1 is written to it.
4. To use the voltage monitor 1 interrupt or voltage monitor 2 interrupt (when the digital filter is used), set the CM14 bit to 0 (low-speed on-chip oscillator on).
5. Once the CM13 bit is set to 1 by a program, it cannot be set to 0.
6. Do not set the CM10 bit to 1 (stop mode) when the VCA20 bit in the VCA2 register to 1 (low consumption enabled).

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM1 register.

9.2.3 System Clock Control Register 3 (CM3)

Address 0009h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM37	CM36	CM35	—	—	—	—	CM30
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CM30	Wait control bit (1)	0: Other than wait mode 1: MCU enters wait mode	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	—	Reserved bits	Set to 0.	R/W
b4	—			
b5	CM35	CPU clock division when exiting wait mode select bit (2)	0: Following settings are enabled: CM06 bit in CM0 register Bits CM16 and CM17 in CM1 register 1: No division	R/W
b6	CM36	System clock when exiting wait mode or stop mode select bit	b7 b6 0 0: MCU exits with the CPU clock immediately before entering wait or stop mode. 0 1: Do not set. 1 0: High-speed on-chip oscillator clock selected (3) 1 1: XIN clock selected (4)	R/W
b7	CM37			R/W

Notes:
1. When the MCU exits wait mode by a peripheral function interrupt, the CM30 bit is set to 0 (other than wait mode).
2. Set the CM35 bit to 0 in stop mode. When the MCU enters wait mode, if the CM35 bit is set to 1 (no division), the CM06 bit in the CM0 register is set to 0 (bits CM16 and CM17 enabled) and bits CM17 and CM16 in the CM1 register is set to 00b (no division mode).
3. When bits CM37 and CM36 are set to 10b (high-speed on-chip oscillator clock selected), the following will be set when the MCU exits wait mode or stop mode.
   • OCD2 bit in OCD register = 1 (on-chip oscillator selected)
   • FRA00 bit in FRA0 register = 1 (high-speed on-chip oscillator on)
   • FRA01 bit in FRA0 register = 1 (high-speed on-chip oscillator selected)
4. When bits CM37 and CM36 are set to 11b (XIN clock selected), the following will be set when the MCU exits wait mode or stop mode.
   • OM05 bit in OM0 register = 0 (XIN clock oscillates)
   • OM13 bit in OM1 register = 1 (XIN-XOUT pin)
   • OCD2 bit in OCD register = 0 (XIN clock selected)
   When the MCU enters wait mode while the CM05 bit in the CM0 register is 1 (XIN clock stops), if the XIN clock is selected as the CPU clock when exiting wait mode, set the CM06 bit to 1 (divide-by-8 mode) and the CM35 bit to 0. However, if an externally generated clock is used as the XIN clock, do not set bits CM37 to CM36 to 11b (XIN clock selected).

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM3 register.

CM30 bit (Wait Control Bit)

When the CM30 bit is set to 1 (MCU enters wait mode), the CPU clock stops (wait mode). Since the XIN clock and the on-chip oscillator clock do not stop, the peripheral functions using these clocks continue operating. To set the CM30 bit to 1, set the I flag to 0 (maskable interrupt disabled).

The MCU exits wait mode by a reset or peripheral function interrupt. When the MCU exits wait mode by a peripheral function interrupt, it resumes executing the instruction immediately after the instruction to set the CM30 bit to 1.

When the MCU enters wait mode with the WAIT instruction, make sure to set the I flag to 1 (maskable interrupt enabled). With this setting, interrupt handling is performed by the CPU when the MCU exits wait mode.

9.2.4 Oscillation Stop Detection Register (OCD)

Address 000Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	OCD3	OCD2	OCD1	OCD0
After Reset	0	0	0	0	0	1	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	OCD0	Oscillation stop detection enable bit (6)	0: Oscillation stop detection function disabled (1) 1: Oscillation stop detection function enabled	R/W
b1	OCD1	Oscillation stop detection interrupt enable bit	0: Disabled (1) 1: Enabled	R/W
b2	OCD2	System clock select bit (3)	0: XIN clock selected (6) 1: On-chip oscillator clock selected (2)	R/W
b3	OCD3	Clock monitor bit (4, 5)	0: XIN clock oscillates 1: XIN clock stops	R
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

Notes:
1. Set bits OCD1 to OCD0 to 00b before the MCU enters stop mode, high-speed on-chip oscillator mode, or low-speed on-chip oscillator mode (XIN clock stops).
2. If the OCD2 bit is set to 1 (on-chip oscillator clock selected), the CM14 bit is set to 0 (low-speed on-chip oscillator on).
3. The OCD2 bit is automatically set to 1 (on-chip oscillator clock selected) if XIN clock oscillation stop is detected while bits OCD1 to OCD0 are set to 11b. If the OCD3 bit is set to 1 (XIN clock stops), the OCD2 bit remains unchanged even when set to 0 (XIN clock selected).
4. The OCD3 bit is enabled when the OCD0 bit is set to 1 (oscillation stop detection function enabled).
5. The OCD3 bit remains 0 (XIN clock oscillates) if bits OCD1 to OCD0 are set to 00b.
6. Refer to **Figure 9.9 Procedure for Switching Clock Source from Low-Speed On-Chip Oscillator to XIN Clock** for the switching procedure when the XIN clock re-oscillates after detecting oscillation stop.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the OCD register.

9.2.5 High-Speed On-Chip Oscillator Control Register 7 (FRA7)

Address 0015h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	When shipping							

Bit	Function	R/W
b7-b0	32 MHz frequency correction data is stored. The frequency can be adjusted by transferring this value to the FRA3 register and by transferring the correction value in the FRA6 register to the FRA1 register.	R

9.2.6 High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Address 0023h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	FRA03	—	FRA01	FRA00
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FRA00	High-speed on-chip oscillator enable bit	0: High-speed on-chip oscillator off 1: High-speed on-chip oscillator on	R/W
b1	FRA01	High-speed on-chip oscillator select bit (1)	0: Low-speed on-chip oscillator selected (2) 1: High-speed on-chip oscillator selected (3)	R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	FRA03	fOCO128 clock select bit	0: fOCO-S divided by 128 selected 1: fOCO-F divided by 128 selected	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

Notes:
1. Change the FRA01 bit in the following conditions.
   • FRA00 = 1 (high-speed on-chip oscillator on)
   • The CM14 bit in the CM1 register = 0 (low-speed on-chip oscillator on)
2. When setting the FRA01 bit to 0 (low-speed on-chip oscillator selected), do not set the FRA00 bit to 0 (high-speed on-chip oscillator off) at the same time. Set the FRA00 bit to 0 after setting the FRA01 bit to 0.
3. When setting the FRA01 bit to 1 (high-speed on-chip oscillator selected) and stopping the low-speed on-chip oscillator, wait for one or more cycles of the low-speed on-chip oscillator and then set the CM14 bit in the CM1 register to 1 (low-speed on-chip oscillator off)

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRA0 register.

9.2.7 High-Speed On-Chip Oscillator Control Register 1 (FRA1)

Address 0024h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	When shipping							

Bit	Function	R/W
b7-b0	The frequency of the high-speed on-chip oscillator can be changed by the following settings. 40MHz : FRA1 = value after reset, FRA3 = value after reset 36.864MHz : Transfer the data of the FRA4 register to the FRA1 register, and transfer the data of the FRA5 register to the FRA3 register. 32MHz : Transfer the data of the FRA6 register to the FRA1 register, and transfer the data of the FRA7 register to the FRA3 register.	R/W

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRA1 register.

9.2.8 High-Speed On-Chip Oscillator Control Register 2 (FRA2)

Address 0025h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	FRA22	FRA21	FRA20
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FRA20	High-speed on-chip oscillator frequency switching bit	Division selection These bits select the division ratio for the high-speed on-chip oscillator clock. b2 b1 b0 0 0 0: Divide-by-2 mode 0 0 1: Divide-by-3 mode 0 1 0: Divide-by-4 mode 0 1 1: Divide-by-5 mode 1 0 0: Divide-by-6 mode 1 0 1: Divide-by-7 mode 1 1 0: Divide-by-8 mode 1 1 1: Divide-by-9 mode	R/W
b1	FRA21			R/W
b2	FRA22			R/W
b3	—	Reserved bits	Set to 0.	R/W
b4	—			
b5	—			
b6	—			
b7	—			

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRA2 register.

9.2.9 High-Speed On-Chip Oscillator Control Register 4 (FRA4)

Address 0029h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	When shipping							

Bit	Function	R/W
b7-b0	36.864 MHz frequency correction data is stored. The frequency can be adjusted by transferring this value to the FRA1 register and by transferring the correction value in the FRA5 register to the FRA3 register.	R

9.2.10 High-Speed On-Chip Oscillator Control Register 5 (FRA5)

Address 002Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	When shipping							

Bit	Function	R/W
b7-b0	36.864 MHz frequency correction data is stored. The frequency can be adjusted by transferring this value to the FRA3 register and by transferring the correction value in the FRA4 register to the FRA1 register.	R

9.2.11 High-Speed On-Chip Oscillator Control Register 6 (FRA6)

Address 002Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	When shipping							

Bit	Function	R/W
b7-b0	32 MHz frequency correction data is stored. The frequency can be adjusted by transferring this value to the FRA1 register and by transferring the correction value in the FRA7 register to the FRA3 register.	R

9.2.12 High-Speed On-Chip Oscillator Control Register 3 (FRA3)

Address 002Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	When shipping							

Bit	Function	R/W
b7-b0	The frequency of the high-speed on-chip oscillator can be changed by the following settings. 40MHz : FRA1 = value after reset, FRA3 = value after reset 36.864MHz : Transfer the data of the FRA4 register to the FRA1 register, and transfer the data of the FRA5 register to the FRA3 register. 32MHz : Transfer the data of the FRA6 register to the FRA1 register, and transfer the data of the FRA7 register to the FRA3 register.	R/W

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRA3 register.
Also, rewrite the FRA3 register when the FRA00 bit in the FRA0 register is set 0 (high-speed on-chip oscillator off).

9.2.13 Voltage Detect Register 2 (VCA2)

Address 0034h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VCA27	VCA26	VCA25	—	—	—	—	VCA20
After Reset	0	0	0	0	0	0	0	0

The above applies when the LVDAS bit in the OFS register is set to 1.

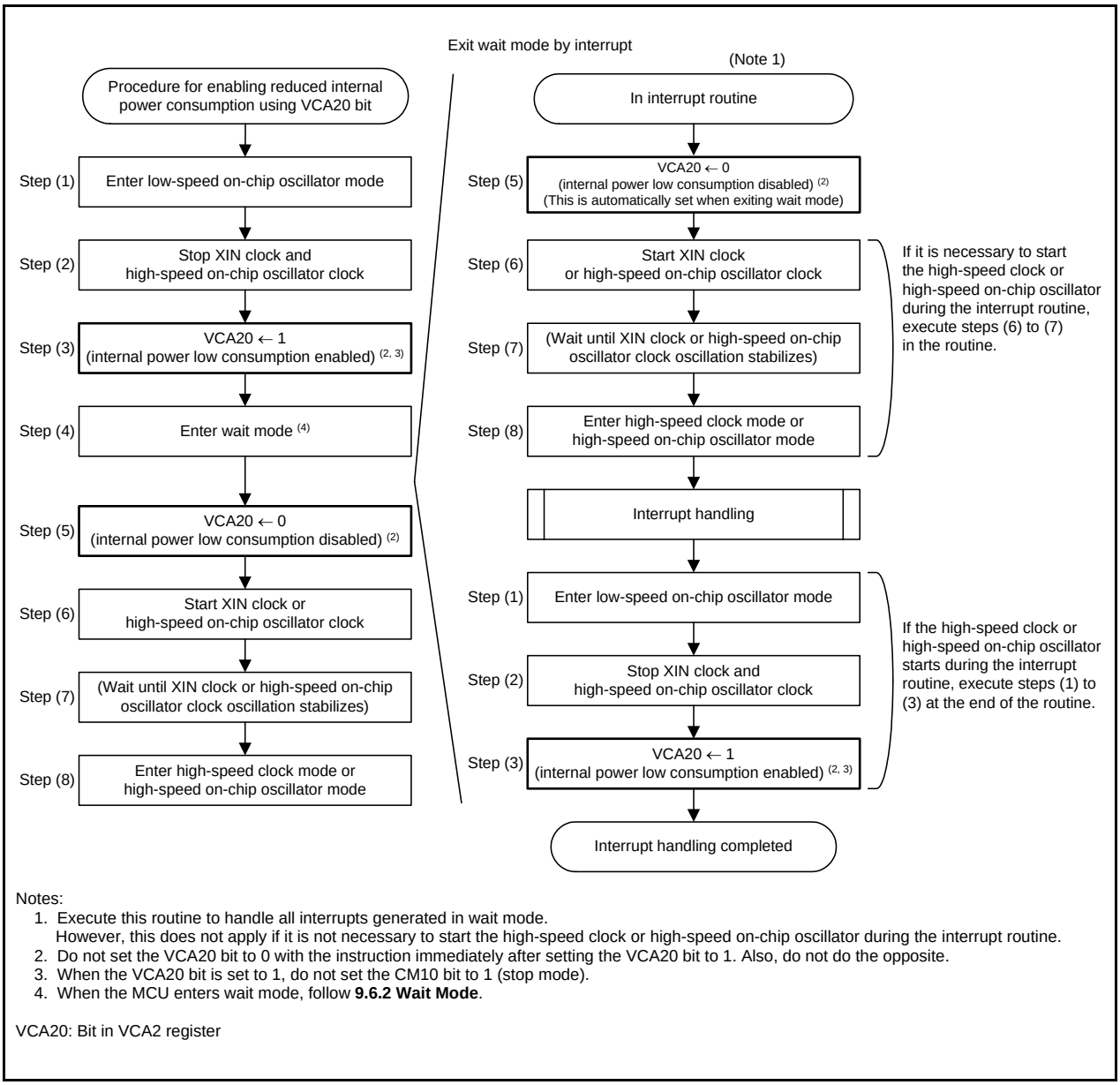
After Reset	0	0	1	0	0	0	0	0

The above applies when the LVDAS bit in the OFS register is set to 0.

Bit	Symbol	Bit Name	Function	R/W
b0	VCA20	Internal power low consumption enable bit (1)	0: Low consumption disabled 1: Low consumption enabled (2)	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	—			
b5	VCA25	Voltage detection 0 enable bit (3)	0: Voltage detection 0 circuit disabled 1: Voltage detection 0 circuit enabled	R/W
b6	VCA26	Voltage detection 1 enable bit (4)	0: Voltage detection 1 circuit disabled 1: Voltage detection 1 circuit enabled	R/W
b7	VCA27	Voltage detection 2 enable bit (5)	0: Voltage detection 2 circuit disabled 1: Voltage detection 2 circuit enabled	R/W

Notes:
1. Use the VCA20 bit only when the MCU enters wait mode. To set the VCA20 bit, follow the procedure shown in **Figure 9.3 Procedure for Reducing Internal Power Consumption Using VCA20 bit**.
2. When the VCA20 bit is set to 1 (low consumption enabled), do not set the CM10 bit in the CM1 register to 1 (stop mode).
3. When writing to the VCA25 bit, set a value after reset.
4. To use the voltage detection 1 interrupt or the VW1C3 bit in the VW1C register, set the VCA26 bit to 1. After the VCA26 bit is set to 1 from 0, allow td(E-A) to elapse before the voltage detection 1 circuit starts operation.
5. To use the voltage detection 2 interrupt or the VCA13 bit in the VCA1 register, set the VCA27 bit to 1. After the VCA27 bit is set to 1 from 0, allow td(E-A) to elapse before the voltage detection 2 circuit starts operation.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VCA2 register.



Notes:
1. Execute this routine to handle all interrupts generated in wait mode.
   However, this does not apply if it is not necessary to start the high-speed clock or high-speed on-chip oscillator during the interrupt routine.
2. Do not set the VCA20 bit to 0 with the instruction immediately after setting the VCA20 bit to 1. Also, do not do the opposite.
3. When the VCA20 bit is set to 1, do not set the CM10 bit to 1 (stop mode).
4. When the MCU enters wait mode, follow **9.6.2 Wait Mode**.

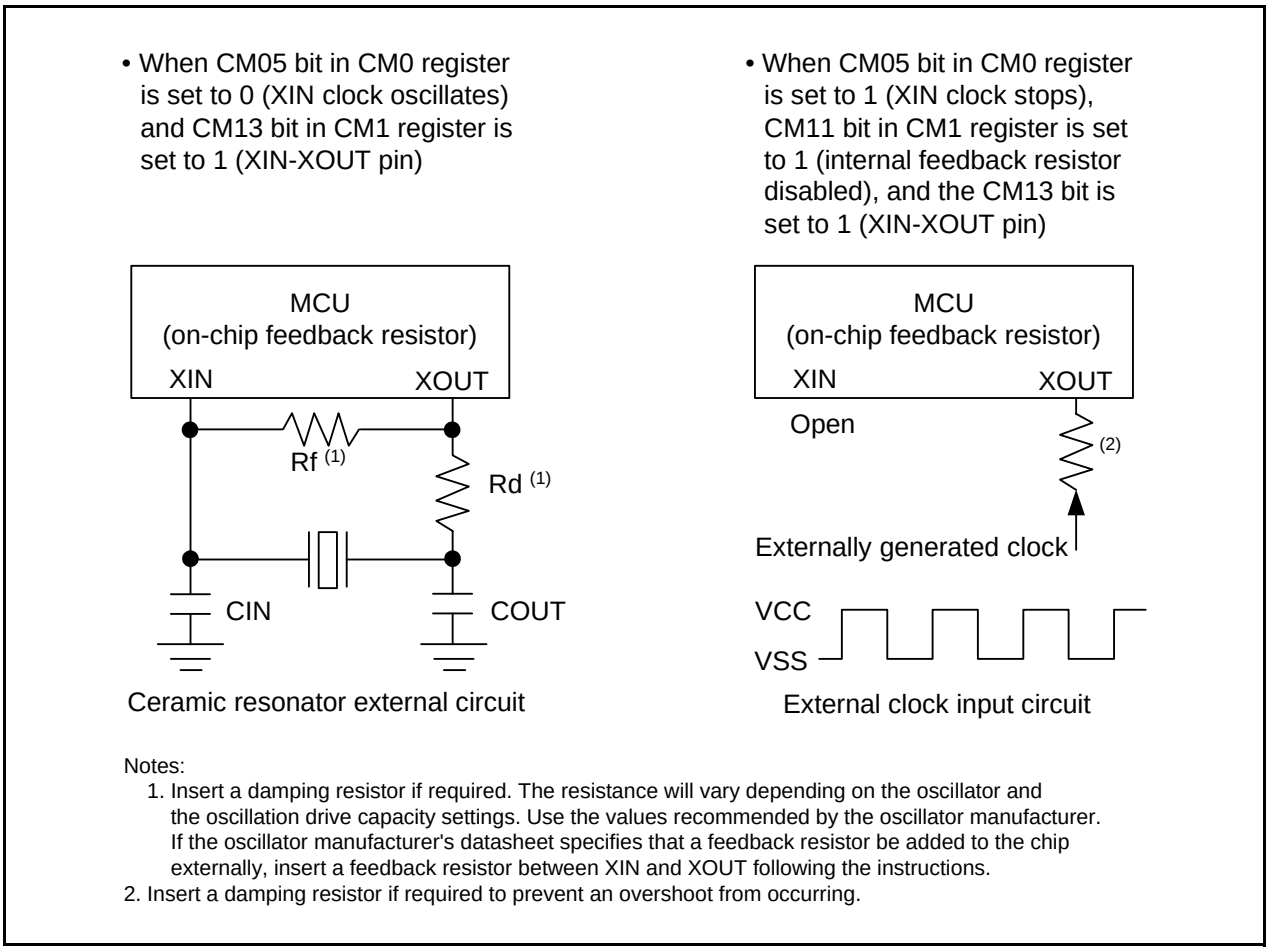
VCA20: Bit in VCA2 register

Figure 9.3 Procedure for Reducing Internal Power Consumption Using VCA20 bit

The clocks generated by the clock generation circuits are described below.

9.3 XIN Clock

The XIN clock is supplied by the XIN clock oscillation circuit. This clock is used as the clock source for the CPU and peripheral function clocks. The XIN clock oscillation circuit is configured by connecting a resonator between pins XIN and XOUT. The XIN clock oscillation circuit includes an on-chip feedback resistor, which is disconnected from the oscillation circuit in stop mode in order to reduce the amount of power consumed by the chip. The XIN clock oscillation circuit may also be configured by feeding an externally generated clock to the XOUT pin.
Figure 9.4 shows Examples of XIN Clock Connection Circuit.
During and after a reset, the XIN clock stops.
After setting the CM13 bit in the CM1 register to 1 (XIN-XOUT pin), the XIN clock starts oscillating when the CM05 bit in the CM0 register is set to 0 (XIN clock oscillates). After the XIN clock oscillation stabilizes, the XIN clock is used as the CPU clock source when the OCD2 bit in the OCD register is set to 0 (XIN clock selected).
The power consumption can be reduced by setting the CM05 bit in the CM0 register to 1 (XIN clock stops) if the OCD2 bit is set to 1 (on-chip oscillator clock selected).
When an externally generated clock is input to the XOUT pin, the XIN clock does not stop even if the CM05 bit is set to 1. If necessary, use an external circuit to stop the clock.
In stop mode, all clocks including the XIN clock stop. Refer to **9.6 Power Control** for details.



Notes:
1. Insert a damping resistor if required. The resistance will vary depending on the oscillator and the oscillation drive capacity settings. Use the values recommended by the oscillator manufacturer. If the oscillator manufacturer's datasheet specifies that a feedback resistor be added to the chip externally, insert a feedback resistor between XIN and XOUT following the instructions.
2. Insert a damping resistor if required to prevent an overshoot from occurring.

Figure 9.4 Examples of XIN Clock Connection Circuit

9.4 On-Chip Oscillator Clock

The on-chip oscillator clock is supplied by the on-chip oscillator (high-speed on-chip oscillator or low-speed on-chip oscillator). This clock is selected by the FRA01 bit in the FRA0 register.

9.4.1 Low-Speed On-Chip Oscillator Clock

The clock generated by the low-speed on-chip oscillator is used as the clock source for the CPU clock, peripheral function clock, fOCO, fOCO-S, and fOCO128.
After a reset, the on-chip oscillator clock generated by the low-speed on-chip oscillator divided by 1 (no division) is selected as the CPU clock.
If the XIN clock stops oscillating when bits OCD1 to OCD0 in the OCD register are set to 11b, the low-speed on-chip oscillator automatically starts operating and supplies the necessary clock for the MCU.
The frequency of the low-speed on-chip oscillator varies depending on the supply voltage and the operating ambient temperature. Application products must be designed with sufficient margin to allow for frequency changes.

9.4.2 High-Speed On-Chip Oscillator Clock

The clock generated by the high-speed on-chip oscillator is used as the clock source for the CPU clock, peripheral function clock, fOCO, fOCO-F, fOCO40M, and fOCO128.

After a reset, the on-chip oscillator clock generated by the high-speed on-chip oscillator stops. Oscillation is started by setting the FRA00 bit in the FRA0 register to 1 (high-speed on-chip oscillator on).

Frequency correction data is stored in registers FRA4 to FRA7.
To adjust the frequency of the high-speed on-chip oscillator clock to 36.864 MHz, first transfer the correction value in the FRA4 register to the FRA1 register and the correction value in the FRA5 register to the FRA3 register before using the values. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode (refer to **Table 24.8** and **Table 25.8 Bit Rate Setting Example in UART Mode**).
To adjust the frequency of the high-speed on-chip oscillator clock to 32 MHz, first transfer the correction value in the FRA6 register to the FRA1 register and the correction value in the FRA7 register to the FRA3 register before using the values.

9.5 CPU Clock and Peripheral Function Clock

There are a CPU clock to operate the CPU and a peripheral function clock to operate the peripheral functions. Refer to **Figure 9.1 Clock Generation Circuit**.

9.5.1 System Clock

The system clock is the clock source for the CPU and peripheral function clocks. The XIN clock or the on-chip oscillator clock can be selected.

9.5.2 CPU Clock

The CPU clock is an operating clock for the CPU and the watchdog timer.
The system clock divided by 1 (no division), 2, 4, 8, or 16 is used as the CPU clock. Use the CM06 bit in the CM0 register and bits CM16 and CM17 in the CM1 register to select the value of the division.
After a reset, the low-speed on-chip oscillator clock divided by 1 (no division) is used as the CPU clock.
When the MCU enters stop mode, the CM06 bit is set to 1 (divide-by-8 mode). To enter stop mode, set the CM35 bit in the CM3 register to 0 (settings of CM06 in CM0 register and bits CM16 and CM17 in CM1 register enabled).

9.5.3 Peripheral Function Clock (f1, f2, f4, f8, and f32)

The peripheral function clock is an operating clock for the peripheral functions.
The fi (i = 1, 2, 4, 8, and 32) clock is generated by the system clock divided by i. It is used for timers RA0, RA1, RB, RC, RD, RE, RF, RG, the serial interface, and the A/D converter.
If the MCU enters wait mode after the CM02 bit in the CM0 register is set to 1 (peripheral function clock stops in wait mode), the fi clock stops.

9.5.4 fOCO

fOCO is an operating clock for the peripheral functions.
This clock runs at the same frequency as the on-chip oscillator clock and can be used as the source for timer RA0, RA1.
In wait mode, the fOCO clock does not stop.

9.5.5 fOCO40M

fOCO40M is used as the count source for timers RC, RD, and RG.
This clock is generated by the high-speed on-chip oscillator and supplied by setting the FRA00 bit to 1.
In wait mode, the fOCO40M clock does not stop.

9.5.6 fOCO-F

fOCO-F is used as the count source for timers RC, RD and the A/D converter.
fOCO-F is a clock generated by the high-speed on-chip oscillator and divided by i (i = 2, 3, 4, 5, 6, 7, 8, and 9; divide ratio selected by the FRA2 register). This clock is supplied by setting the FRA00 bit to 1.
In wait mode, the fOCO-F clock does not stop.

9.5.7 fOCO-S

fOCO-S is an operating clock for the voltage detection circuit.
This clock is generated by the low-speed on-chip oscillator and supplied by setting the CM14 bit to 0 (low-speed on-chip oscillator on).
In wait mode, the fOCO-S clock does not stop.

9.5.8 fOCO128

fOCO128 is a clock generated by dividing fOCO-S or fOCO-F by 128. When the FRA03 bit is set to 0, fOCO-S divided by 128 is selected. When this bit is set to 1, fOCO-F divided by 128 is selected.
fOCO128 is configured as the capture signal used in the TRCGRA register for timer RC and timer RD0 for timer RD.

9.5.9 fOCO-WDT

fOCO-WDT is an operating clock for the watchdog timer.
This clock is generated by the low-speed on-chip oscillator for the watchdog timer and supplied by setting the CSPRO bit in the CSPR register to 1 (count source protect mode enabled).
In count source protection mode for the watchdog timer, the fOCO-WDT clock does not stop.

9.6 Power Control

There are three power control modes. All modes other than wait mode and stop mode are referred to as standard operating mode.

9.6.1 Standard Operating Mode

Standard operating mode is further separated into three modes.
In standard operating mode, the CPU and peripheral function clocks are supplied to operate the CPU and the peripheral functions. Power consumption control is enabled by controlling the CPU clock frequency. The higher the CPU clock frequency, the more processing power increases. The lower the CPU clock frequency, the more power consumption decreases. If unnecessary oscillator circuits stop, power consumption is further reduced.
Before the clock sources for the CPU clock can be switched over, the new clock source needs to be oscillating and stable. Allow sufficient wait time in a program until oscillation stabilizes before switching the clock.

Table 9.2 Settings and Modes of Clock Associated Bits

Modes		OCD Register	CM1 Register			CM0 Register		FRA0 Register	
		OCD2	CM17, CM16	CM14	CM13	CM06	CM05	FRA01	FRA00
High-speed clock mode	No division	0	00b	–	1	0	0	–	–
	Divide-by-2	0	01b	–	1	0	0	–	–
	Divide-by-4	0	10b	–	1	0	0	–	–
	Divide-by-8	0	–	–	1	1	0	–	–
	Divide-by-16	0	11b	–	1	0	0	–	–
High-speed on-chip oscillator mode	No division	1	00b	–	–	0	–	1	1
	Divide-by-2	1	01b	–	–	0	–	1	1
	Divide-by-4	1	10b	–	–	0	–	1	1
	Divide-by-8	1	–	–	–	1	–	1	1
	Divide-by-16	1	11b	–	–	0	–	1	1
Low-speed on-chip oscillator mode	No division	1	00b	0	–	0	–	0	–
	Divide-by-2	1	01b	0	–	0	–	0	–
	Divide-by-4	1	10b	0	–	0	–	0	–
	Divide-by-8	1	–	0	–	1	–	0	–
	Divide-by-16	1	11b	0	–	0	–	0	–

–: Indicates that either 0 or 1 can be set.

9.6.1.1 High-Speed Clock Mode

The XIN clock divided by 1 (no division), 2, 4, 8, or 16 is used as the CPU clock. If the CM14 bit is set to 0 (low-speed on-chip oscillator on) or the FRA00 bit in the FRA0 register is set to 1 (high-speed on-chip oscillator on), fOCO can be used for timer RA0 and timer RA1.
Also, if the FRA00 bit is set to 1, fOCO40M can be used for timer RC, timer RD, and timer RG.
If the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO-S can be used for the voltage detection circuit.

9.6.1.2 High-Speed On-Chip Oscillator Mode

The high-speed on-chip oscillator is used as the on-chip oscillator clock when the FRA00 bit in the FRA0 register is set to 1 (high-speed on-chip oscillator on) and the FRA01 bit in the FRA0 register is set to 1. The on-chip oscillator divided by 1 (no division), 2, 4, 8, or 16 is used as the CPU clock. If the FRA00 bit is set to 1, fOCO40M can be used for timer RC, timer RD, and timer RG.
Also, if the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO-S can be used for the voltage detection circuit.

9.6.1.3 Low-Speed On-Chip Oscillator Mode

If the CM14 bit in the CM1 register is set to 0 (low-speed on-chip oscillator on) and the FRA01 bit in the FRA0 register is set to 0, the low-speed on-chip oscillator is used as the on-chip oscillator clock. At this time, the on-chip oscillator clock divided by 1 (no division), 2, 4, 8 or 16 is used as the CPU clock. The on-chip oscillator clock is also the clock source for the peripheral function clocks. If the FRA00 bit is set to 1, fOCO40M can be used for timer RC, timer RD, and timer RG.
Also, if the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO-S can be used for the voltage detection circuit.
In this mode, low consumption operation is enabled by stopping the XIN clock and the high-speed on-chip oscillator, and by setting the FMR27 bit in the FMR2 register to 1 (low-consumption-current read mode enabled). When the CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16, low-consumption-current read mode can be used. When divided by 1 (no division) or divided by 2 is set, do not use low-consumption-current read mode. After setting the divide ratio of the CPU clock, set the FMR27 bit to 1.
To enter wait mode from low-speed clock mode, lower consumption current in wait mode is enabled by setting the VCA20 bit in the VCA2 register to 1 (internal power low consumption enabled).
To reduce the power consumption, refer to **31. Reducing Power Consumption**.

9.6.2 Wait Mode

Since the CPU clock stops in wait mode, the CPU operating with the CPU clock, the watchdog timer and the CAN when count source protection mode is disabled stop. Since the XIN clock and on-chip oscillator clock do not stop, the peripheral functions using these clocks continue operating.

9.6.2.1 Peripheral Function Clock Stop Function

If the CM02 bit is set to 1 (peripheral function clock stops in wait mode), the f1, f2, f4, f8, and f32 clocks stop in wait mode. This reduces power consumption.

9.6.2.2 Entering Wait Mode

The MCU enters wait mode by executing the WAIT instruction or setting the CM30 bit in the CM3 register to 1 (MCU enters wait mode).
When the OCD2 bit in the OCD register is set to 1 (on-chip oscillator selected as system clock), set the OCD1 bit in the OCD register to 0 (oscillation stop detection interrupt disabled) before executing the WAIT instruction or setting the CM30 bit in the CM3 register to 1(MCU enters wait mode).
If the MCU enters wait mode while the OCD1 bit is set to 1 (oscillation stop detection interrupt enabled), current consumption is not reduced because the CPU clock does not stop.
Enter wait mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled). Do not enter wait mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

9.6.2.3 Pin Status in Wait Mode

The I/O port retains the status immediately before the MCU enters wait mode.

9.6.2.4 Exiting Wait Mode

The MCU exits wait mode by a reset or peripheral function interrupt.
The peripheral function interrupts are affected by the CM02 bit. When the CM02 bit is set to 0 (peripheral function clock does not stop in wait mode), the peripheral function interrupts other than A/D conversion interrupts can be used to exit wait mode. When the CM02 bit is set to 1 (peripheral function clock stops in wait mode), the peripheral functions using the peripheral function clock stop and the peripheral functions operating with external signals or the on-chip oscillator clock can be used to exit wait mode.
Table 9.3 lists Interrupts to Exit Wait Mode and Usage Conditions.

Table 9.3 Interrupts to Exit Wait Mode and Usage Conditions

Interrupt	CM02 = 0	CM02 = 1
Serial interface interrupt	Usable when operating with internal or external clock	Usable when operating with external clock
Synchronous serial communication unit interrupt	Usable in all modes	(Do not use)
Key input interrupt	Usable	Usable
A/D conversion interrupt	(Do not use)	(Do not use)
Timer RA0 interrupt, Timer RA1 interrupt	Usable in all modes	Usable if there is no filter in event counter mode. Usable by selecting fOCO as count source.
Timer RB interrupt	Usable in all modes	Usable by selecting fOCO as timer RA count source and timer RA underflow as timer RB count source
Timer RC interrupt	Usable in all modes	Usable by selecting fOCO40M or fOCO-F as count source
Timer RD interrupt	Usable in all modes	Usable by selecting fOCO40M or fOCO-F as count source
Timer RE interrupt	Usable in all modes	(Do not use)
Timer RF interrupt	Usable in all modes	(Do not use)
Timer RG interrupt	Usable in all modes	Usable by selecting fOCO40M as count source
$\overline{\text{INT}}$ interrupt	Usable	Usable ($\overline{\text{INT0}}$ to $\overline{\text{INT4}}$ can be used if there is no filter.)
Voltage monitor 1 interrupt	Usable	Usable
Voltage monitor 2 interrupt	Usable	Usable
Oscillation stop detection interrupt	Usable	(Do not use)
CAN0 wakeup interrupt	Usable	Usable

Figure 9.5 shows the Time from Wait Mode to First Instruction Execution following Exit after CM30 Bit in CM3 Register is Set to 1 (MCU Enters Wait Mode).
To use a peripheral function interrupt to exit wait mode, set up the following before setting the CM30 bit to 1.
(1) Set the I flag to 0 (maskable interrupt disabled).
(2) Set the interrupt priority level in bits ILVL2 to ILVL0 in the interrupt control registers of the peripheral function interrupts to be used for exiting wait mode. Set bits ILVL2 to ILVL0 of the peripheral function interrupts that are not to be used for exiting wait mode to 000b (interrupt disabled).
(3) Operate the peripheral function to be used for exiting wait mode.

When the MCU exits by a peripheral function interrupt, the time (number of cycles) between interrupt request generation and interrupt routine execution is determined by the settings of the FMSTP bit in the FMR0 register and the VCA20 bit in the VCA2 register, as shown in Figure 9.5.
The clock set by bits CM35, CM36, and CM37 in the CM3 register is used as the CPU clock when the MCU exits wait mode by a peripheral function interrupt. At this time, the CM06 bit in the CM0 register and bits CM16 and CM17 in the CM1 register automatically change.

FMR0 Register	VCA2 Register	Internal Power Stabilization Time (T0)	Time until Flash Memory Activation (T1)	Time until CPU Clock Supply (T2)	Remarks
FMSTP Bit	VCA20 Bit				
0 (flash memory operates)	0 (internal power low consumption disabled)	0 μs	Period of system clock × 1 cycle + 60 μs (max.)	Period of CPU clock × 2 cycles	The total of T0 to T2 is the time from wait mode to first instruction execution following exit.
	1 (internal power low consumption enabled)	100 μs (max.)			
1 (flash memory stops)	0 (internal power low consumption disabled	0 μs	Period of system clock × 1 cycle	Same as above	
	1 (internal power low consumption enabled)	100 μs (max.)			

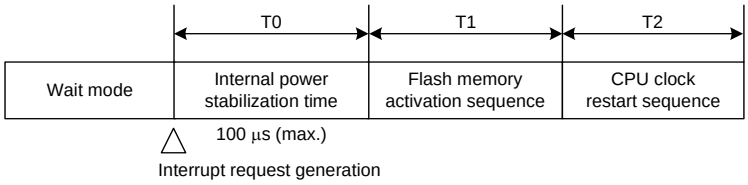


Figure 9.5 Time from Wait Mode to First Instruction Execution following Exit after CM30 Bit in CM3 Register is Set to 1 (MCU Enters Wait Mode)

Figure 9.6 shows the Time from Wait Mode to Interrupt Routine Execution after WAIT instruction is Executed. To use a peripheral function interrupt to exit wait mode, set up the following before executing the WAIT instruction.

(1) Set the interrupt priority level in bits ILVL2 to ILVL0 of the peripheral function interrupts to be used for exiting stop mode. Set bits ILVL2 to ILVL0 of the peripheral function interrupts that are not to be used for exiting stop mode to 000b (interrupt disabled).
(2) Set the I flag to 1.
(3) Operate the peripheral function to be used for exiting stop mode.

When the MCU exits by a peripheral function interrupt, the time (number of cycles) between interrupt request generation and interrupt routine execution is determined by the settings of the FMSTP bit in the FMR0 register and the VCA20 bit in the VCA2 register, as shown in Figure 9.6.
The clock set by bits CM35, CM36, and CM37 in the CM3 register is used as the CPU clock when the MCU exits wait mode by a peripheral function interrupt. At this time, the CM06 bit in the CM0 register and bits CM16 and CM17 in the CM1 register automatically change.

FMR0 Register FMSTP Bit	VCA2 Register VCA20 Bit	Internal Power Stabilization Time (T0)	Time until Flash Memory Activation (T1)	Time until CPU Clock Supply (T2)	Time for Interrupt Sequence (T3)	Remarks
0 (flash memory operates)	0 (internal power low consumption disabled)	0 μs	Period of system clock × 1 cycle + 60 μs (max.)	Period of CPU clock × 2 cycles	Period of CPU clock × 20 cycles	The total of T0 to T3 is the time from wait mode to interrupt routine execution.
	1 (internal power low consumption enabled)	100 μs (max.)				
1 (flash memory stops)	0 (internal power low consumption disabled	0 μs	Period of system clock × 1 cycle	Same as above	Same as above	
	1 (internal power low consumption enabled)	100 μs (max.)				

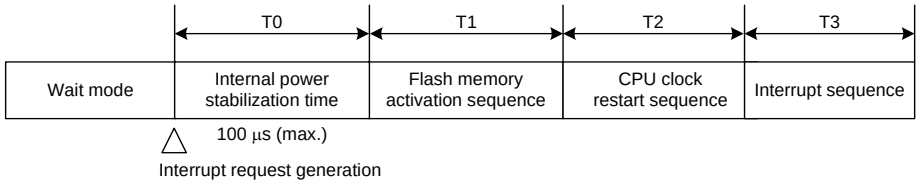


Figure 9.6 Time from Wait Mode to Interrupt Routine Execution after WAIT instruction is Executed

9.6.3 Stop Mode

Since all oscillator circuits except fOCO-WDT stop in stop mode, the CPU and peripheral function clocks stop and the CPU and the peripheral functions operating with these clocks also stop. The least power required to operate the MCU is in stop mode. If the voltage applied to the VCC pin is VRAM or more, the contents of internal RAM is retained.
The peripheral functions clocked by external signals continue operating.
Table 9.4 lists Interrupts to Exit Stop Mode and Usage Conditions.

Table 9.4 Interrupts to Exit Stop Mode and Usage Conditions

Interrupt	Usage Conditions
Key input interrupt	Usable
$\overline{\text{INT0}}$ to $\overline{\text{INT4}}$ interrupt	Usable if there is no filter
Timer RA0 interrupt, Timer RA1 interrupt	Usable if there is no filter when external pulse is counted in event counter mode
Serial interface interrupt	When external clock selected
Voltage monitor 1 interrupt	Usable in digital filter disabled mode (VW1C1 bit in VW1C register is set to 1)
Voltage monitor 2 interrupt	Usable in digital filter disabled mode (VW2C1 bit in VW2C register is set to 1)
CAN0 wakeup interrupt	Usable

9.6.3.1 Entering Stop Mode

The MCU enters stop mode when the CM10 bit in the CM1 register is set to 1 (all clocks stop). At the same time, the CM06 bit in the CM0 register is set to 1 (divide-by-8 mode).
To use stop mode, set the following before the MCU enters stop mode:

- Bits OCD1 to OCD0 in the OCD register = 00b
- CM35 bit in CM3 register = 0 (settings of CM06 bit in CM0 register and bits CM16 and CM17 in CM1 register enabled)

Enter stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled). Do not enter stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

9.6.3.2 Pin Status in Stop Mode

The I/O port retains the status before the MCU enters stop mode.
However, when the CM13 bit in the CM1 register is 1 (XIN-XOUT pin), pins XIN (P4_6) and XOUT (P4_7) are set to high impedance.

9.6.3.3 Exiting Stop Mode

The MCU exits stop mode by a reset or peripheral function interrupt.
Figure 9.7 shows the Time from Stop Mode to Interrupt Routine Execution.
To use a peripheral function interrupt to exit stop mode, set up the following before setting the CM10 bit to 1.

(1) Set the interrupt priority level in bits ILVL2 to ILVL0 of the peripheral function interrupts to be used for exiting stop mode. Set bits ILVL2 to ILVL0 of the peripheral function interrupts that are not to be used for exiting stop mode to 000b (interrupt disabled).
(2) Set the I flag to 1.
(3) Operate the peripheral function to be used for exiting stop mode.
When the MCU exits stop mode by a peripheral function interrupt, the interrupt sequence is executed when an interrupt request is generated and the CPU clock supply starts.

The clock divided by 8 specified by bits CM36 and CM37 in the CM3 register is used as the CPU clock when the MCU exits stop mode by a peripheral function interrupt. To enter stop mode, set the CM35 bit in the CM3 register to 0 (settings of CM06 bit in CM0 register and bits CM16 and CM17 in CM1 register enabled)

FMR0 Register FMSTP Bit	Internal Power Stabilization Time (T0)	Time until Flash Memory Activation (T2)	Time until CPU Clock Supply (T3)	Time for Interrupt Sequence (T4)	Remarks
0 (flash memory operates)	100 μs (max.)	Period of system clock × 1 cycle + 60 μs (max.)	Period of CPU clock × 2 cycles	Period of CPU clock × 20 cycles	The total of T0 to T4 is the time from wait mode to interrupt routine execution.
1 (flash memory stops)	100 μs (max.)	Period of system clock × 1 cycle	Same as above	Same as above	

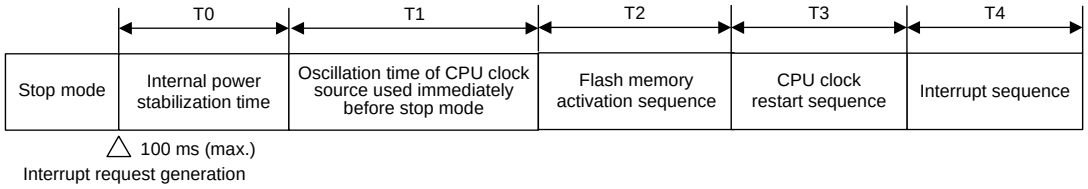


Figure 9.7 Time from Stop Mode to Interrupt Routine Execution

Figure 9.8 shows the State Transitions in Power Control Mode.

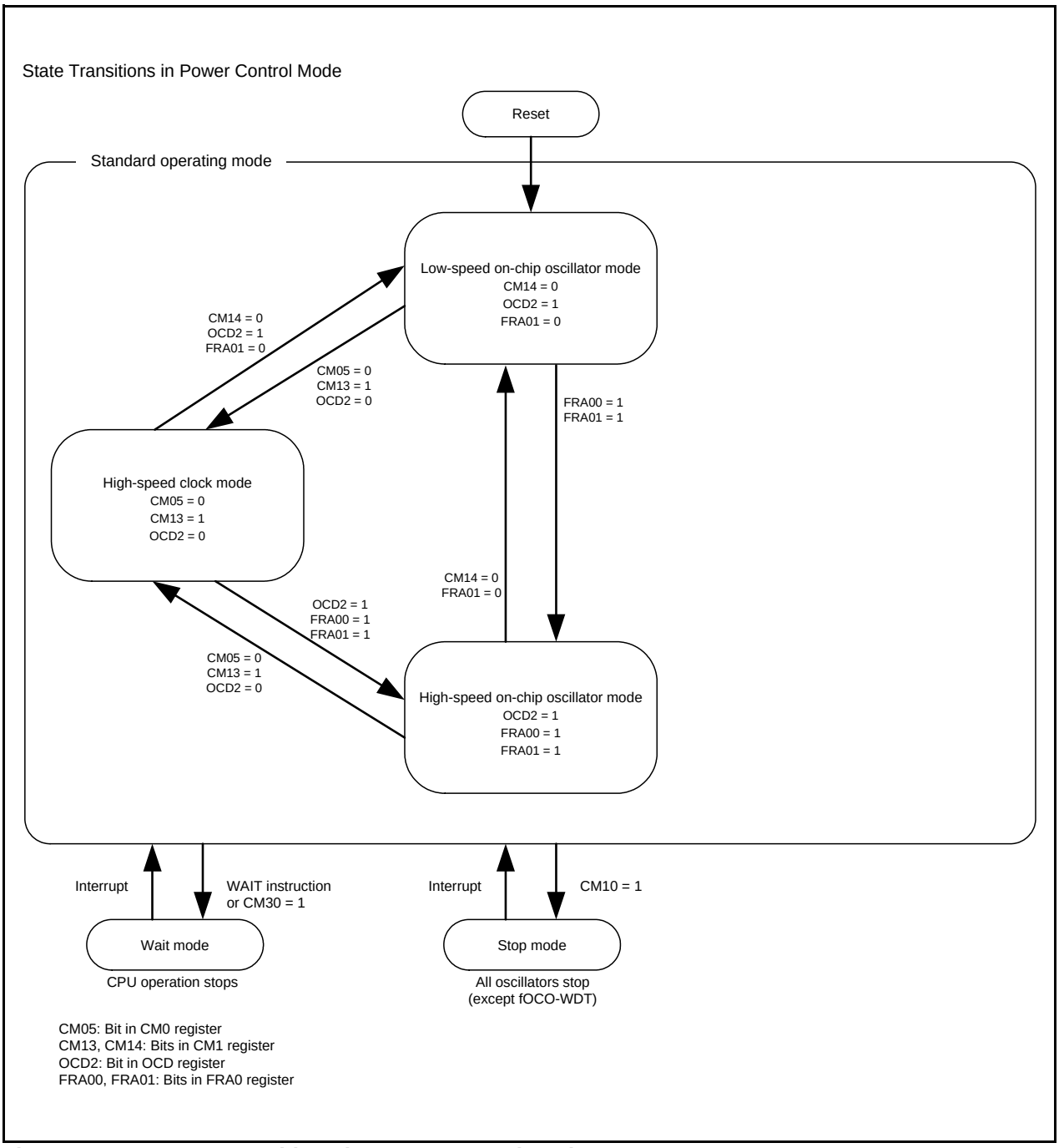


Figure 9.8 State Transitions in Power Control Mode

9.7 Oscillation Stop Detection Function

The oscillation stop detection function detects the stop of the XIN clock oscillating circuit.
The oscillation stop detection function can be enabled and disabled by the OCD0 bit in the OCD register.
Table 9.5 lists the Specifications of Oscillation Stop Detection Function.

When the XIN clock is the CPU clock source and bits OCD1 to OCD0 are set to 11b, the MCU is placed in the following state if the XIN clock stops.

- OCD2 bit in OCD register = 1 (on-chip oscillator clock selected)
- OCD3 bit in OCD register = 1 (XIN clock stops)
- CM14 bit in CM1 register = 0 (low-speed on-chip oscillator oscillates)
- Oscillation stop detection interrupt request is generated

Table 9.5 Specifications of Oscillation Stop Detection Function

Item	Specification
Oscillation stop detection clock and frequency bandwidth	f(XIN) ≥ 2 MHz
Enabled condition for oscillation stop detection function	Bits OCD1 to OCD0 set to 11b
Operation at oscillation stop detection	Oscillation stop detection interrupt generated

9.7.1 How to Use Oscillation Stop Detection Function

- The oscillation stop detection interrupt shares a vector with the voltage monitor 1 interrupt, the voltage monitor 2 interrupt, and the watchdog timer interrupt. To use the oscillation stop detection interrupt and watchdog timer interrupt, the interrupt source needs to be determined.
  Table 9.6 lists the Determination of Interrupt Sources for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, or Voltage Monitor 2 Interrupt. Figure 9.10 shows an Example of Determining Interrupt Sources for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, or Voltage Monitor 2 Interrupt.
- When the XIN clock restarts after oscillation stop, switch the XIN clock to the clock source for the CPU clock and the peripheral functions by a program.
  Figure 9.9 shows the Procedure for Switching Clock Source from Low-Speed On-Chip Oscillator to XIN Clock.
- To enter wait mode while the oscillation stop detection function is used, set the CM02 bit to 0 (peripheral function clock does not stop in wait mode).
- Since the oscillation stop detection function is a function for cases where the XIN clock is stopped by an external cause, set bits OCD1 to OCD0 to 00b to stop or start the XIN clock by a program (select stop mode or change the CM05 bit).
- This function cannot be used when the XIN clock frequency is below 2 MHz. In this case, set bits OCD1 to OCD0 to 00b.
- To use the low-speed on-chip oscillator clock as the clock source for the CPU clock and the peripheral functions after detecting the oscillation stop, set the FRA01 bit in the FRA0 register to 0 (low-speed on-chip oscillator selected) and bits OCD1 to OCD0 to 11b.
  To use the high-speed on-chip oscillator clock as the clock source for the CPU clock and the peripheral functions after detecting the oscillation stop, first set the FRA00 bit to 1 (high-speed on-chip oscillator oscillates) and the FRA01 bit to 1 (high-speed on-chip oscillator selected). Then set bits OCD1 to OCD0 to 11b.

Table 9.6 Determination of Interrupt Sources for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, or Voltage Monitor 2 Interrupt

Generated Interrupt Source	Bit Indicating Interrupt Source
Oscillation stop detection ((a) or (b))	(a) OCD3 bit in OCD register = 1
	(b) OCD1 to OCD0 bits in OCD register = 11b and OCD2 bit = 1
Watchdog timer	VW2C3 bit in VW2C register = 1
Voltage monitor 1	VW1C2 bit in VW1C register = 1
Voltage monitor 2	VW2C2 bit in VW2C register = 1

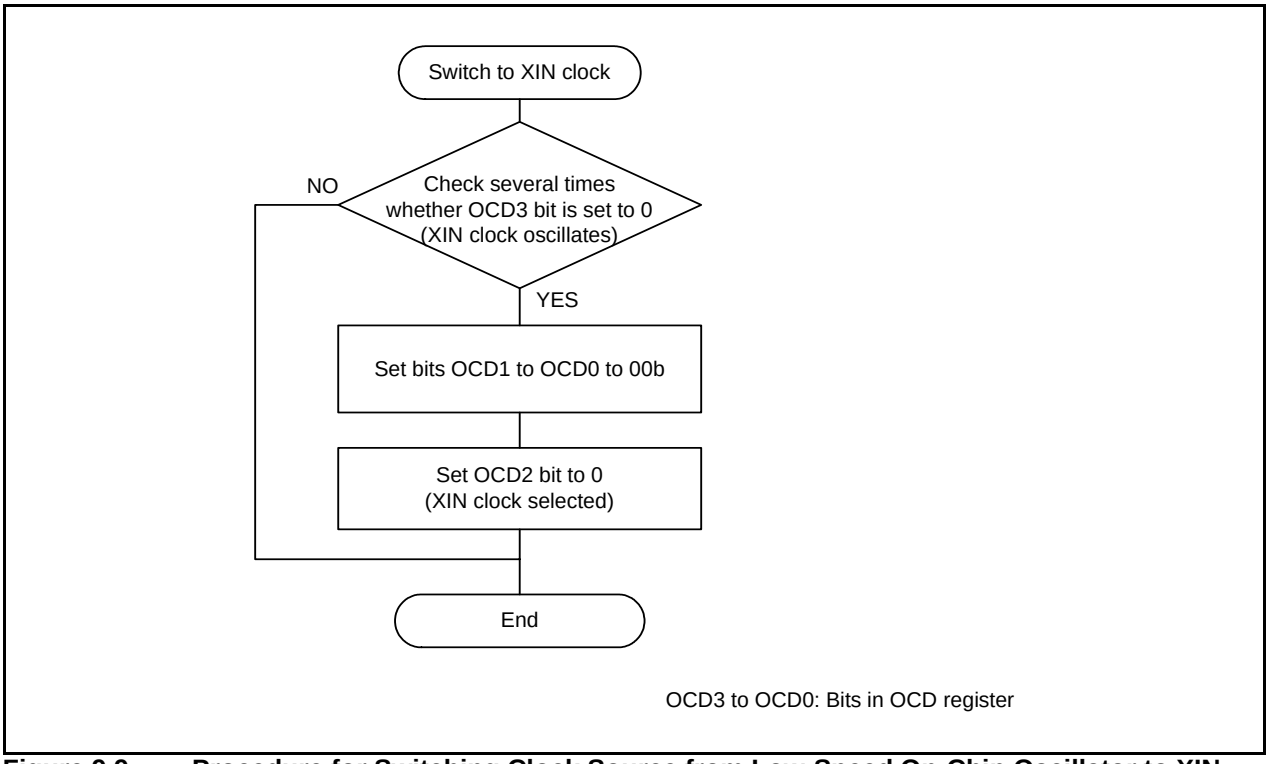
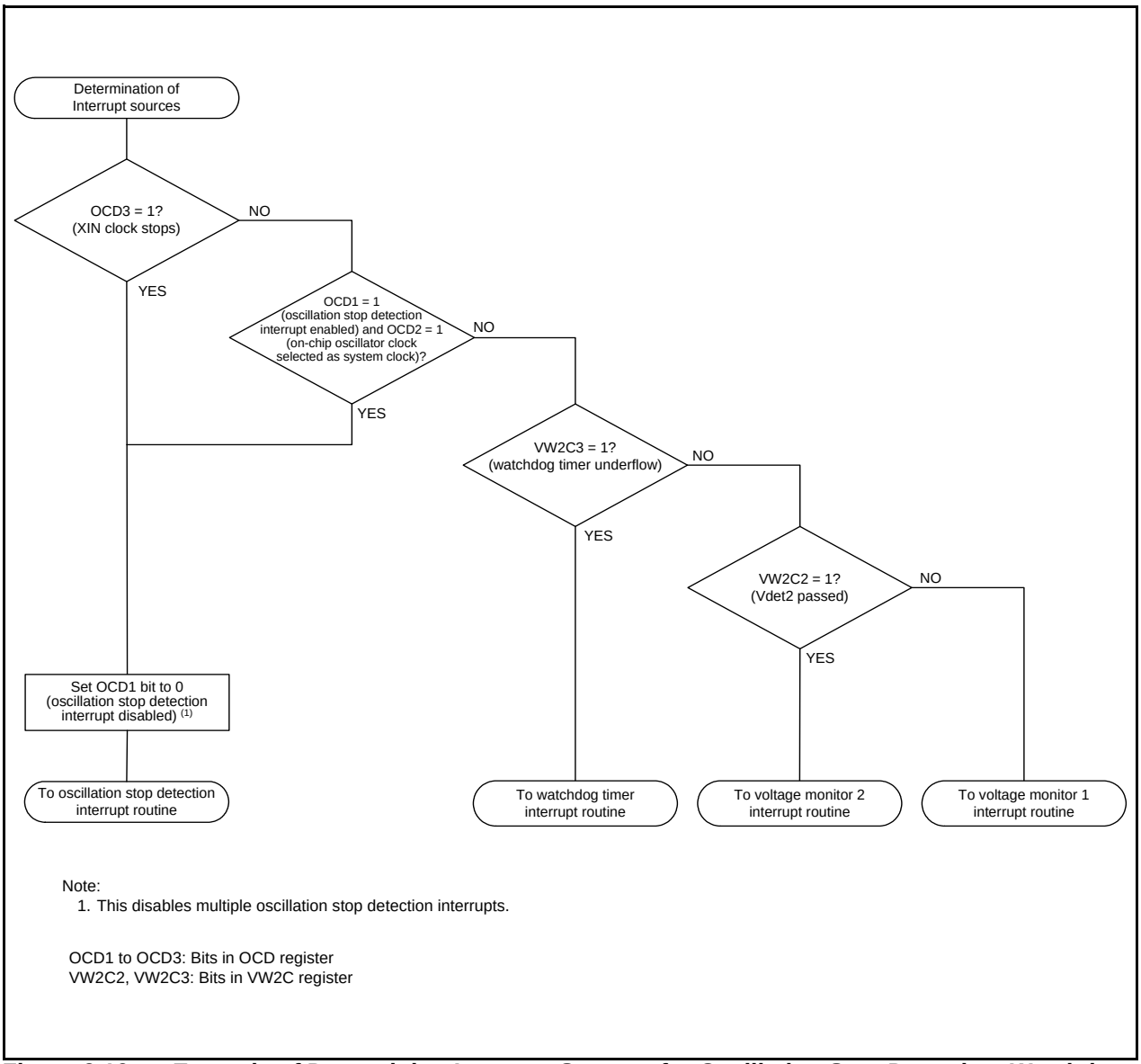


Figure 9.9 Procedure for Switching Clock Source from Low-Speed On-Chip Oscillator to XIN Clock



Note:
1. This disables multiple oscillation stop detection interrupts.

OCD1 to OCD3: Bits in OCD register
VW2C2, VW2C3: Bits in VW2C register

Figure 9.10 Example of Determining Interrupt Sources for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, or Voltage Monitor 2 Interrupt

9.8 Notes on Clock Generation Circuit

9.8.1 Stop Mode

To enter stop mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and then the CM10 bit in the CM1 register to 1 (stop mode). An instruction queue pre-reads 4 bytes from the instruction which sets the CM10 bit to 1 (stop mode) and the program stops.
Insert at least four NOP instructions following the JMP.B instruction after the instruction which sets the CM10 bit to 1.

• Program example to enter stop mode

```
        BCLR    1,FMR0      ; CPU rewrite mode disabled
        BCLR    7,FMR2      ; Low-current-consumption read mode disabled
        BSET    0,PRCR      ; Writing to CM1 register enabled
        FSET    I           ; Enable interrupt
        BSET    0,CM1       ; Stop mode
        JMP.B   LABEL_001
LABEL_001:
        NOP
        NOP
        NOP
        NOP
```

9.8.2 Wait Mode

When setting bits CM37 and CM36 to values other than 00b to enter wait mode from high-speed clock mode, set the XIN clock frequency to 28 kHz or more.
To enter wait mode by setting the CM30 bit to 1, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) before setting the CM30 bit to 1.
To enter wait mode with the WAIT instruction, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and then execute the WAIT instruction. An instruction queue pre-reads 4 bytes from the instruction to set the CM30 bit to 1 (MCU enters wait mode) or the WAIT instruction, and then the program stops. Insert at least four NOP instructions after the instruction to set the CM30 bit to 1 (MCU enters wait mode) or these instructions.

• Program example to execute the WAIT instruction

```
        BCLR    1,FMR0      ; CPU rewrite mode disabled
        BCLR    7,FMR2      ; Low-current-consumption read mode disabled
        FSET    I           ; Enable interrupt
        WAIT                ; Wait mode
        NOP
        NOP
        NOP
        NOP
```

• Program example to execute the instruction to set the CM30 bit to 1

```
        BCLR    1, FMR0     ; CPU rewrite mode disabled
        BCLR    7,FMR2      ; Low-current-consumption read mode disabled
        BSET    0, PRCR     ; Writing to CM3 register enabled
        FCLR    I           ; Interrupt disabled
        BSET    0, CM3      ; Wait mode
        NOP
        NOP
        NOP
        NOP
        BCLR    0, PRCR     ; Writing to CM3 register enabled
        FSET    I           ; Interrupt enabled
```

9.8.3 Oscillation Stop Detection Function

Since the oscillation stop detection function cannot be used if the XIN clock frequency is below 2 MHz, set bits OCD1 to OCD0 to 00b.

9.8.4 Oscillation Circuit Constants

Consult the oscillator manufacturer to determine the optimal oscillation circuit constants for the user system.

10. Protection

The protection function protects important registers from being easily overwritten if a program runs out of control. The registers protected by the PRCR register are as follows:

- Registers protected by PRC0 bit: Registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3
- Registers protected by PRC1 bit: Registers PM0 and PM1
- Registers protected by PRC2 bit: PD0 register
- Registers protected by PRC3 bit: Registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C

10.1 Register

10.1.1 Protect Register (PRCR)

Address 000Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	PRC3	PRC2	PRC1	PRC0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 0: Write disabled 1: Write enabled (2)	R/W
b1	PRC1	Protect bit 1	Enables writing to registers PM0 and PM1. 0: Write disabled 1: Write enabled (2)	R/W
b2	PRC2	Protect bit 2	Enables writing to the PD0 register. 0: Write disabled 1: Write enabled (1)	R/W
b3	PRC3	Protect bit 3	Enables writing to registers OCVREFCR, VCA2, VD1LS, VW0C, VW1C, and VW2C. 0: Write disabled 1: Write enabled (2)	R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			R/W
b6	—			R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:

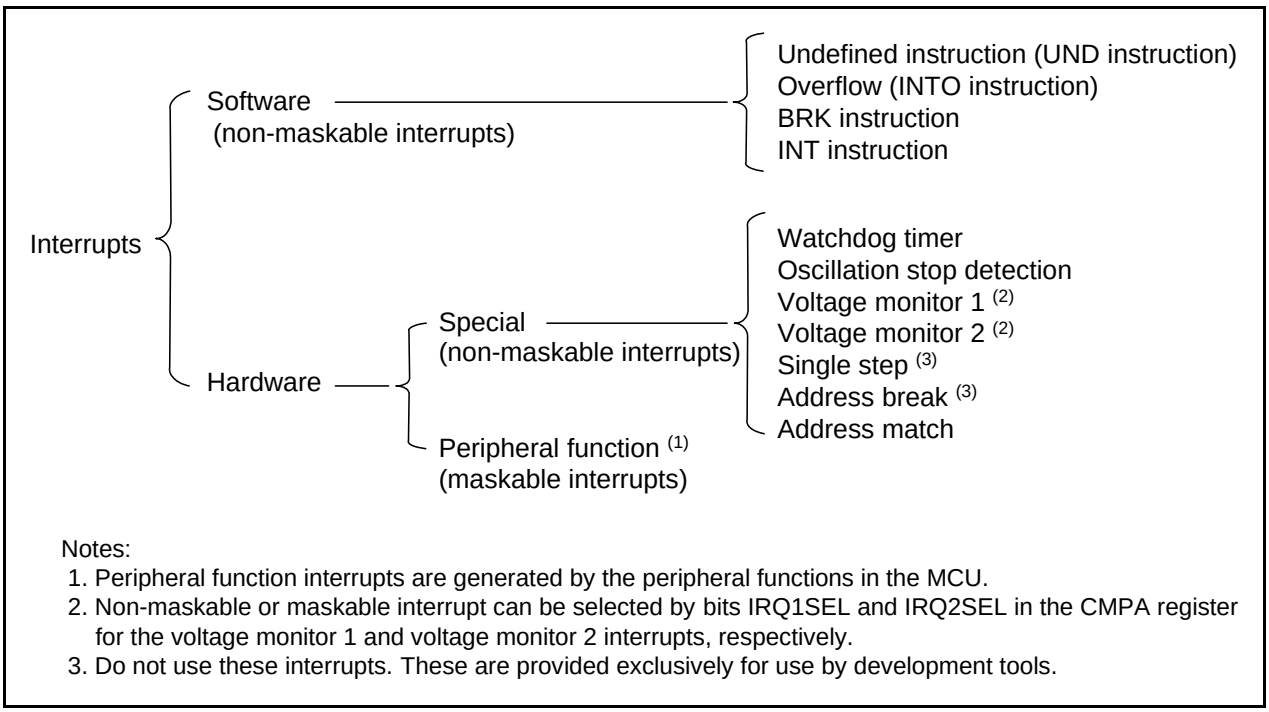
1. The PRC2 bit is set to 0 after setting it to 1 (write enabled) and writing to the SFR area. Change the register protected by the PRC2 bit with the next instruction after that used to set the PRC2 bit to 1. Do not allow interrupts or DTC activation between the instruction to set to the PRC2 bit to 1 and the next instruction.
2. Bits PRC0, PRC1, and PRC3 are not set to 0 even after setting them to 1 (write enabled) and writing to the SFR areas. Set these bits to 0 by a program.

11. Interrupts

11.1 Overview

11.1.1 Types of Interrupts

Figure 11.1 shows the Types of Interrupts.



Notes:
1. Peripheral function interrupts are generated by the peripheral functions in the MCU.
2. Non-maskable or maskable interrupt can be selected by bits IRQ1SEL and IRQ2SEL in the CMPA register for the voltage monitor 1 and voltage monitor 2 interrupts, respectively.
3. Do not use these interrupts. These are provided exclusively for use by development tools.

Figure 11.1 Types of Interrupts

- Maskable interrupts: These interrupts are enabled or disabled by the interrupt enable flag (I flag). The interrupt priority **can be changed** based on the interrupt priority level.
- Non-maskable interrupts: These interrupts are not enabled or disabled by the interrupt enable flag (I flag). The interrupt priority **cannot be changed** based on the interrupt priority level.

11.1.2 Software Interrupts

A software interrupt is generated when an instruction is executed. Software interrupts are non-maskable.

11.1.2.1 Undefined Instruction Interrupt

An undefined instruction interrupt is generated when the UND instruction is executed.

11.1.2.2 Overflow Interrupt

An overflow interrupt is generated when the O flag is set to 1 (arithmetic operation overflow) and the INTO instruction is executed. Instructions that set the O flag are as follows:
ABS, ADC, ADCF, ADD, CMP, DIV, DIVU, DIVX, NEG, RMPA, SBB, SHA, and SUB.

11.1.2.3 BRK Interrupt

A BRK interrupt is generated when the BRK instruction is executed.

11.1.2.4 INT Instruction Interrupt

An INT instruction interrupt is generated when the INT instruction is executed. Software interrupt numbers 0 to 63 can be specified with the INT instruction. Because some software interrupt numbers are assigned to peripheral function interrupts, the same interrupt routine as for peripheral function interrupts can be executed by executing the INT instruction.
For software interrupt numbers 0 to 31, the U flag is saved on the stack during instruction execution and the U flag is set to 0 (ISP selected) before the interrupt sequence is executed. The U flag is restored from the stack when returning from the interrupt routine. For software interrupt numbers 32 to 63, the U flag does not change state during instruction execution, and the selected SP is used.

11.1.3 Special Interrupts

Special interrupts are non-maskable.

11.1.3.1 Watchdog Timer Interrupt

A watchdog timer interrupt is generated by the watchdog timer. For details, refer to **14. Watchdog Timer**.

11.1.3.2 Oscillation Stop Detection Interrupt

An oscillation stop detection interrupt is generated by the oscillation stop detection function. For details of the oscillation stop detection function, refer to **9. Clock Generation Circuit**.

11.1.3.3 Voltage Monitor 1 Interrupt

A voltage monitor 1 interrupt is generated by the voltage detection circuit. For details of the voltage detection circuit, refer to **6. Voltage Detection Circuit**. Non-maskable or maskable interrupt can be selected by the IRQ1SEL bit in the CMPA register for the voltage monitor 1 interrupt.

11.1.3.4 Voltage Monitor 2 Interrupt

A voltage monitor 2 interrupt is generated by the voltage detection circuit. For details of the voltage detection circuit, refer to **6. Voltage Detection Circuit**. Non-maskable or maskable interrupt can be selected by the IRQ2SEL bit in the CMPA register for the voltage monitor 2 interrupt.

11.1.3.5 Single-Step Interrupt, and Address Break Interrupt

Do not use these interrupts. They are provided exclusively for use by development tools.

11.1.3.6 Address Match Interrupt

An address match interrupt is generated immediately before executing an instruction that is stored at an address indicated by registers RMAD0 to RMAD1 if the AIER00 bit in the AIER0 register or AIER10 bit in the AIER1 register is set to 1 (address match interrupt enabled).
For details of the address match interrupt, refer to **11.6 Address Match Interrupt**.

11.1.4 Peripheral Function Interrupts

A peripheral function interrupt is generated by a peripheral function in the MCU. Peripheral function interrupts are maskable. Refer to **Table 11.2 Relocatable Vector Tables (1), Table 11.3 Relocatable Vector Tables (2)** for sources of the corresponding peripheral function interrupt. For details of peripheral functions, refer to the descriptions of individual peripheral functions.

11.1.5 Interrupts and Interrupt Vectors

There are 4 bytes in each vector. Set the starting address of an interrupt routine in each interrupt vector. When an interrupt request is acknowledged, the CPU branches to the address set in the corresponding interrupt vector. Figure 11.2 shows an Interrupt Vector.

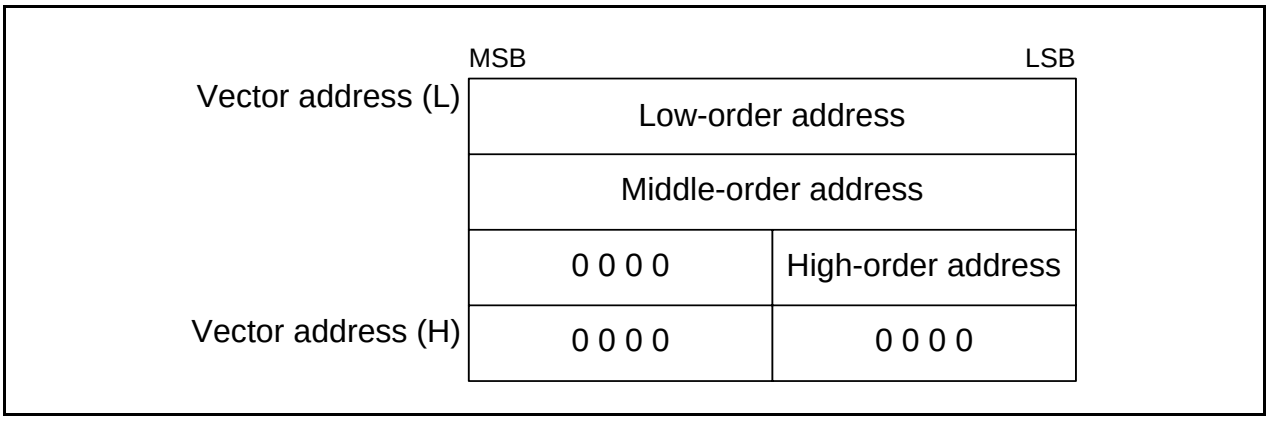


Figure 11.2 Interrupt Vector

11.1.5.1 Fixed Vector Tables

The fixed vector tables are allocated addresses 0FFDCh to 0FFFFh.
Table 11.1 lists the Fixed Vector Tables. The vector addresses (H) of fixed vectors are used by the ID code check function. For details, refer to **30.3 Functions to Prevent Flash Memory from being Rewritten**.

Table 11.1 Fixed Vector Tables

Interrupt Source	Vector Addresses Address (L) to (H)	Remarks	Reference
Undefined instruction	0FFDCh to 0FFDFh	Interrupt with UND instruction	R8C/Tiny Series Software Manual
Overflow	0FFE0h to 0FFE3h	Interrupt with INTO instruction	
BRK instruction	0FFE4h to 0FFE7h	If the content of address 0FFE6h is FFh, program execution starts from the address shown by the vector in the relocatable vector table.	
Address match	0FFE8h to 0FFEBh		11.6 Address Match Interrupt
Single step (1)	0FFECh to 0FFEFh		
Watchdog timer, Oscillation stop detection, Voltage monitor 1, Voltage monitor 2 (2)	0FFF0h to 0FFF3h		14. Watchdog Timer 9. Clock Generation Circuit 6. Voltage Detection Circuit
Address break (1)	0FFF4h to 0FFF7h		
(Reserved)	0FFF8h to 0FFFBh		
Reset	0FFFCh to 0FFFFh		5. Resets

Notes:
1. Do not use these interrupts. These are provided exclusively for use by development tools.
2. Non-maskable or maskable interrupt can be selected by bits IRQ1SEL and IRQ2SEL in the CMPA register for the voltage monitor 1 and voltage monitor 2 interrupts, respectively.

11.1.5.2 Relocatable Vector Tables

The relocatable vector tables occupy 256 bytes beginning from the starting address set in the INTB register. Table 11.2 lists the Relocatable Vector Tables (1), Table 11.3 lists the Relocatable Vector Tables (2).

Table 11.2 Relocatable Vector Tables (1)

Interrupt Source	Vector Addresses (1) Address (L) to Address (H)	Software Interrupt Number	Interrupt Control Register	Reference
BRK instruction (2)	+0 to +3 (0000h to 0003h)	0	–	R8C/Tiny Series Software Manual
Flash memory ready	+4 to +7 (0004h to 0007h)	1	FMRDYIC	30. Flash Memory
Timer RA1	+8 to +11 (0008h to 000Bh)	2	TRA1IC	17. Timer RA
(Reserved)		3 to 5	–	–
$\overline{\text{INT4}}$	+24 to +27 (0018h to 001Bh)	6	INT4IC	11.4 $\overline{\text{INT}}$ Interrupt
Timer RC	+28 to +31 (001Ch to 001Fh)	7	TRCIC	19. Timer RC
Timer RD0	+32 to +35 (0020h to 0023h)	8	TRD0IC	20. Timer RD
Timer RD1	+36 to +39 (0024h to 0027h)	9	TRD1IC	
Timer RE	+40 to +43 (0028h to 002Bh)	10	TREIC	21. Timer RE
UART2 transmit/NACK2	+44 to +47 (002Ch to 002Fh)	11	S2TIC	25. Serial Interface (UART2)
UART2 receive/ACK2	+48 to +51 (0030h to 0033h)	12	S2RIC	
Key input	+52 to +55 (0034h to 0037h)	13	KUPIC	11.5 Key Input Interrupt
A/D conversion	+56 to +59 (0038h to 003Bh)	14	ADIC	29. A/D Converter
Synchronous serial communication unit	+60 to +63 (003Ch to 003Fh)	15	SSUIC	26. Synchronous Serial Communication Unit (SSU)
Timer RF compare 1	+64 to +67 (0040h to 0043h)	16	CMP1IC	22. Timer RF
UART0 transmit	+68 to +71 (0044h to 0047h)	17	S0TIC	24. Serial Interface (UARTi (i = 0 or 1))
UART0 receive	+72 to +75 (0048h to 004Bh)	18	S0RIC	
UART1 transmit	+76 to +79 (004Ch to 004Fh)	19	S1TIC	
UART1 receive	+80 to +83 (0050h to 0053h)	20	S1RIC	
$\overline{\text{INT2}}$	+84 to +87 (0054h to 0057h)	21	INT2IC	11.4 $\overline{\text{INT}}$ Interrupt
Timer RA0	+88 to +91 (0058h to 005Bh)	22	TRA0IC	17. Timer RA
(Reserved)		23	–	–
Timer RB	+96 to +99 (0060h to 0063h)	24	TRBIC	18. Timer RB
$\overline{\text{INT1}}$	+100 to +103 (0064h to 0067h)	25	INT1IC	11.4 $\overline{\text{INT}}$ Interrupt
$\overline{\text{INT3}}$	+104 to +107 (0068h to 006Bh)	26	INT3IC	
Timer RF	+108 to +111 (006Ch to 006Fh)	27	TRFIC	22. Timer RF
Timer RF compare 0	+112 to +115 (0070h to 0073h)	28	CMP0IC	
$\overline{\text{INT0}}$	+116 to +119 (0074h to 0077h)	29	INT0IC	11.4 $\overline{\text{INT}}$ Interrupt
UART2 bus collision detection	+120 to +123 (0078h to 007Bh)	30	U2BCNIC	25. Serial Interface (UART2)
Timer RF capture	+124 to +127 (007Ch to 007Fh)	31	CAPIC	22. Timer RF
Software (2)	+128 to +131 (0080h to 0083h) to +164 to +167 (00A4h to 00A7h)	32 to 41	–	R8C/Tiny Series Software Manual
(Reserved)		42	–	–
Timer RG	+172 to +175 (00ACh to 00AFh)	43	TRGIC	23. Timer RG
CAN0 reception complete	+176 to +179 (00B0h to 00B3h)	44	C0RIC	28. CAN Module
CAN0 transmission complete	+180 to +183 (00B4h to 00B7h)	45	C0TIC	
CAN0 receive FIFO	+184 to +187 (00B8h to 00BBh)	46	C0FRIC	
CAN0 transmit FIFO	+188 to +191 (00BCh to 00BFh)	47	C0FTIC	
CAN0 error	+192 to +195 (00C0h to 00C3h)	48	C0EIC	
CAN0 wake-up	+196 to +199 (00C4h to 00C7h)	49	C0WIC	

Notes:
1. These addresses are relative to those in the INTB register.
2. These interrupts are not disabled by the I flag.

Table 11.3 Relocatable Vector Tables (2)

Interrupt Source	Vector Addresses (1) Address (L) to Address (H)	Software Interrupt Number	Interrupt Control Register	Reference
Voltage monitor 1 (2)	+200 to +203 (00C8h to 00CBh)	50	VCMP1IC	6. Voltage Detection Circuit
Voltage monitor 2 (2)	+204 to +207 (00CCh to 00CFh)	51	VCMP2IC	
(Reserved)		52 to 55	—	—
Software (3)	+224 to +227 (00E0h to 00E3h) to +252 to +255 (00FCh to 00FFh)	56 to 63		R8C/Tiny Series Software Manual

Notes:
1. These addresses are relative to those in the INTB register.
2. Non-maskable or maskable interrupt can be selected by bits IRQ1SEL and IRQ2SEL in the CMPA register for the voltage monitor 1 and voltage monitor 2 interrupts, respectively.
3. These interrupts are not disabled by the I flag.

11.2 Registers

11.2.1 Interrupt Control Register (TRA1IC, TREIC, S2TIC, S2RIC, KUPIC, ADIC, CMP1IC, S0TIC, S0RIC, S1TIC, S1RIC, TRA0IC, TRBIC, TRFIC, CMP0IC, U2BCNIC, CAPIC, C0RIC, C0TIC, C0FRIC, C0FTIC, C0EIC, C0WIC, VCMP1IC, VCMP2IC)

Address 0042h (TRA1IC), 004Ah (TREIC), 004Bh (S2TIC), 004Ch (S2RIC), 004Dh (KUPIC), 004Eh (ADIC), 0050h (CMP1IC), 0051h (S0TIC), 0052h (S0RIC), 0053h (S1TIC), 0054h (S1RIC), 0056h (TRA0IC), 0058h (TRBIC), 005Bh (TRFIC), 005Ch (CMP0IC), 005Eh (U2BCNIC), 005Fh (CAPIC), 006Ch (C0RIC), 006Dh (C0TIC), 006Eh (C0FRIC), 006Fh (C0FTIC), 0070h (C0EIC), 0071h (C0WIC), 0072h (VCMP1IC), 0073h (VCMP2IC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	IR	ILVL2	ILVL1	ILVL0
After Reset	X	X	X	X	X	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled) 0 0 1: Level 1 0 1 0: Level 2 0 1 1: Level 3 1 0 0: Level 4 1 0 1: Level 5 1 1 0: Level 6 1 1 1: Level 7	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R/W (1)
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b5	—			
b6	—			
b7	—			

Note:
1. Only 0 can be written to the IR bit. Do not write 1 to this bit.

Rewrite the interrupt control register when an interrupt request corresponding to the register is not generated. Refer to **11.8.5 Rewriting Interrupt Control Register**.

11.2.2 Interrupt Control Register (FMRDYIC, TRCIC, TRD0IC, TRD1IC, SSUIC, TRGIC)

Address 0041h (FMRDYIC), 0047h (TRCIC), 0048h (TRD0IC), 0049h (TRD1IC), 004Fh (SSUIC), 006Bh (TRGIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	IR	ILVL2	ILVL1	ILVL0
After Reset	X	X	X	X	X	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled) 0 0 1: Level 1 0 1 0: Level 2 0 1 1: Level 3 1 0 0: Level 4 1 0 1: Level 5 1 1 0: Level 6 1 1 1: Level 7	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b5	—			
b6	—			
b7	—			

Rewrite the interrupt control register when an interrupt request corresponding to the register is not generated. Refer to **11.8.5 Rewriting Interrupt Control Register**.

11.2.3 INTi Interrupt Control Register (INTiIC) (i = 0 to 4)

Address 0046h (INT4IC), 0055h (INT2IC), 0059h (INT1IC), 005Ah (INT3IC), 005Dh (INT0IC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	POL	IR	ILVL2	ILVL1	ILVL0
After Reset	X	X	0	0	X	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled) 0 0 1: Level 1 0 1 0: Level 2 0 1 1: Level 3 1 0 0: Level 4 1 0 1: Level 5 1 1 0: Level 6 1 1 1: Level 7	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R/W (1)
b4	POL	Polarity switch bit (3)	0: Falling edge selected 1: Rising edge selected (2)	R/W
b5	—	Reserved bit	Set to 0.	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b7	—			

Notes:
1. Only 0 can be written to the IR bit. Do not write 1 to this bit.
2. If the INTiPL bit in the INTEN register is set to 1 (both edges), set the POL bit to 0 (falling edge selected).
3. The IR bit may be set to 1 (interrupt requested) when the POL bit is rewritten. Refer to **11.8.4 Changing Interrupt Sources**.

Rewrite the interrupt control register when an interrupt request corresponding to the register is not generated. Refer to **11.8.5 Rewriting Interrupt Control Register**.

11.3 Interrupt Control

The following describes enabling and disabling maskable interrupts and setting the acknowledgement priority. This description does not apply to non-maskable interrupts.
Use the I flag in the FLG register, IPL, and bits ILVL2 to ILVL0 in the corresponding interrupt control register to enable or disable a maskable interrupt. Whether an interrupt is requested or not is indicated by the IR bit in the corresponding interrupt control register.

11.3.1 I Flag

The I flag enables or disables maskable interrupts. Setting the I flag to 1 (enabled) enables maskable interrupts. Setting the I flag to 0 (disabled) disables all maskable interrupts.

11.3.2 IR Bit

The IR bit is set to 1 (interrupt requested) when an interrupt request is generated. After the interrupt request is acknowledged and the CPU branches to the corresponding interrupt vector, the IR bit is set to 0 (no interrupt requested).
The IR bit can be set to 0 by a program. Do not write 1 to this bit.
However, the IR bit operations of the timer RC interrupt, the timer RD interrupt, the synchronous serial communication unit interrupt the I^2C bus interface interrupt, and the flash memory interrupt are different. Refer to **11.7 Timer RC Interrupt, Timer RD Interrupt, Timer RG Interrupt, Synchronous Serial Communication Unit Interrupt, and Flash Memory Interrupt (Interrupts with Multiple Interrupt Request Sources)**.

11.3.3 Bits ILVL2 to ILVL0, IPL

Interrupt priority levels can be set using bits ILVL2 to ILVL0.
Table 11.4 lists the Settings of Interrupt Priority Levels and Table 11.5 lists the Interrupt Priority Levels Enabled by IPL.

The following are the conditions when an interrupt is acknowledged:

- I flag = 1
- IR bit = 1
- Interrupt priority level > IPL

The I flag, IR bit, bits ILVL2 to ILVL0, and IPL are independent of each other. They do not affect one another.

Table 11.4 Settings of Interrupt Priority Levels

Bits ILVL2 to ILVL0	Interrupt Priority Level	Priority
000b	Level 0 (interrupt disabled)	–
001b	Level 1	Low ↓ High
010b	Level 2	
011b	Level 3	
100b	Level 4	
101b	Level 5	
110b	Level 6	
111b	Level 7	

Table 11.5 Interrupt Priority Levels Enabled by IPL

IPL	Enabled Interrupt Priority Level
000b	Interrupt level 1 and above
001b	Interrupt level 2 and above
010b	Interrupt level 3 and above
011b	Interrupt level 4 and above
100b	Interrupt level 5 and above
101b	Interrupt level 6 and above
110b	Interrupt level 7 and above
111b	All maskable interrupts are disabled

11.3.4 Interrupt Sequence

The following describes an interrupt sequence which is performed from when an interrupt request is acknowledged until the interrupt routine is executed.
When an interrupt request is generated while an instruction is being executed, the CPU determines its interrupt priority level after the instruction is completed. The CPU starts the interrupt sequence from the following cycle. However, for the SMOVB, SMOVF, SSTR, or RMPA instruction, if an interrupt request is generated while the instruction is being executed, the MCU suspends the instruction to start the interrupt sequence. The interrupt sequence is performed as indicated below.
Figure 11.3 shows the Time Required for Executing Interrupt Sequence.

(1) The CPU obtains interrupt information (interrupt number and interrupt request level) by reading address 00000h. The IR bit for the corresponding interrupt is set to 0 (no interrupt requested). (2)
(2) The FLG register is saved to a temporary register (1) in the CPU immediately before entering the interrupt sequence.
(3) The I, D and U flags in the FLG register are set as follows:
The I flag is set to 0 (interrupts disabled).
The D flag is set to 0 (single-step interrupt disabled).
The U flag is set to 0 (ISP selected).
However, the U flag does not change state if an INT instruction for software interrupt number 32 to 63 is executed.
(4) The CPU internal temporary register (1) is saved on the stack.
(5) The PC is saved on the stack.
(6) The interrupt priority level of the acknowledged interrupt is set in the IPL.
(7) The starting address of the interrupt routine set in the interrupt vector is stored in the PC.

After the interrupt sequence is completed, instructions are executed from the starting address of the interrupt routine.

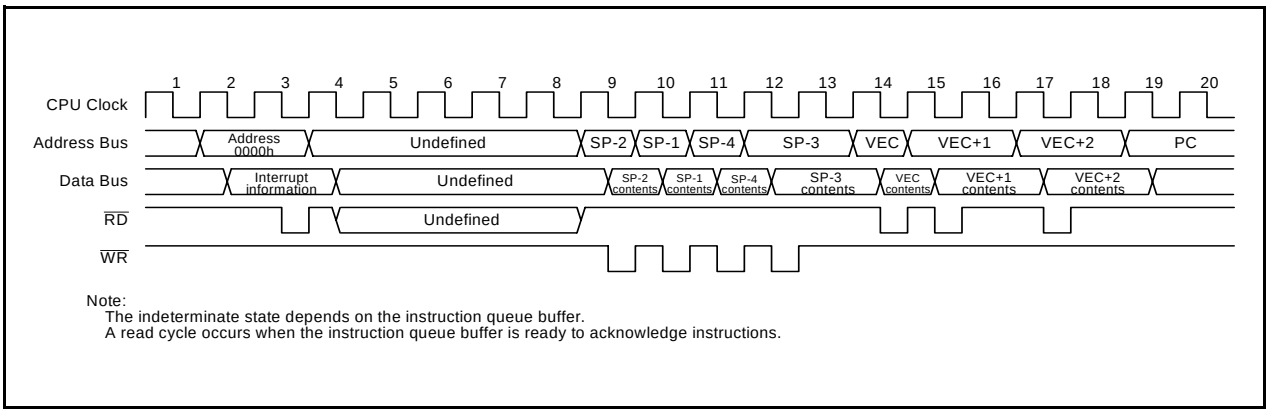
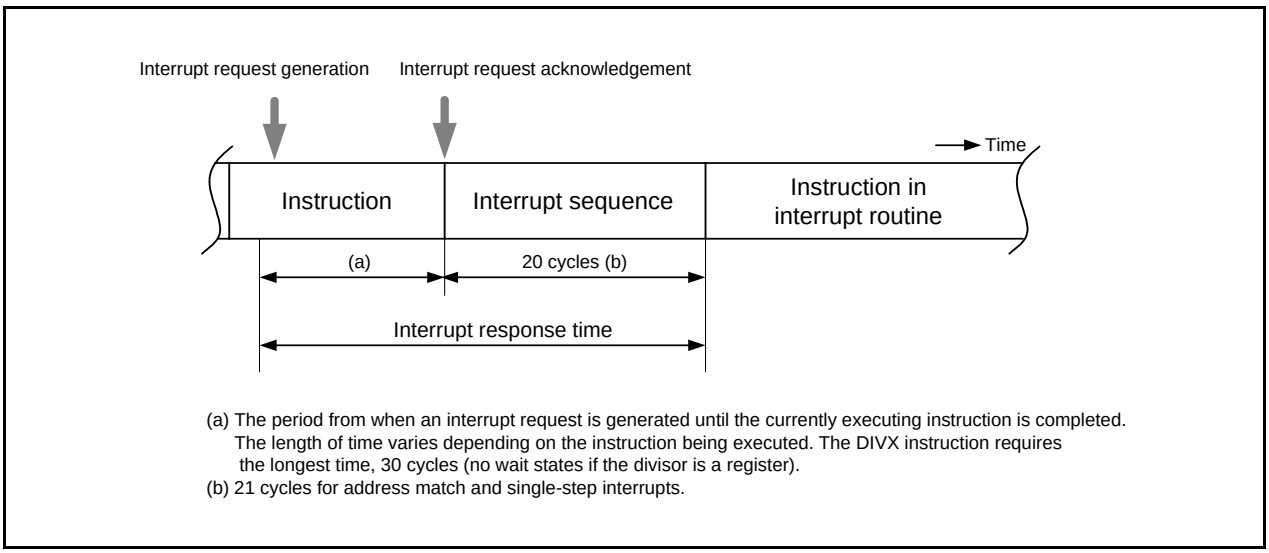


Figure 11.3 Time Required for Executing Interrupt Sequence

Notes:
1. These registers cannot be accessed by the user.
2. Refer to **11.7 Timer RC Interrupt, Timer RD Interrupt, Timer RG Interrupt, Synchronous Serial Communication Unit Interrupt, and Flash Memory Interrupt (Interrupts with Multiple Interrupt Request Sources)** for the IR bit operations of the timer RC Interrupt, timer RD Interrupt, timer RG Interrupt, Synchronous Serial Communication unit Interrupt.

11.3.5 Interrupt Response Time

Figure 11.4 shows the Interrupt Response Time. The interrupt response time is the period from when an interrupt request is generated until the first instruction in the interrupt routine is executed. The interrupt response time includes the period from when an interrupt request is generated until the currently executing instruction is completed (refer to (a) in Figure 11.4) and the period required for executing the interrupt sequence (20 cycles, refer to (b) in Figure 11.4).



(a) The period from when an interrupt request is generated until the currently executing instruction is completed. The length of time varies depending on the instruction being executed. The DIVX instruction requires the longest time, 30 cycles (no wait states if the divisor is a register).
(b) 21 cycles for address match and single-step interrupts.

Figure 11.4 Interrupt Response Time

11.3.6 IPL Change when Interrupt Request is Acknowledged

When a maskable interrupt request is acknowledged, the interrupt priority level of the acknowledged interrupt is set in the IPL.
When a software interrupt or special interrupt request is acknowledged, the level listed in Table 11.6 is set in the IPL.
Table 11.6 lists the IPL Value When Software or Special Interrupt is Acknowledged.

Table 11.6 IPL Value When Software or Special Interrupt is Acknowledged

Interrupt Source without Interrupt Priority Level	Value Set in IPL
Watchdog timer, oscillation stop detection, voltage monitor 1, voltage monitor 2, address break	7
Software, address match, single-step	Not changed

11.3.7 Saving Registers

In the interrupt sequence, the FLG register and PC are saved on the stack.
After an extended 16 bits, 4 high-order bits in the PC and 4 high-order (IPL) and 8 low-order bits in the FLG register, are saved on the stack, the 16 low-order bits in the PC are saved.
Figure 11.5 shows the Stack State Before and After Acknowledgement of Interrupt Request.
The other necessary registers should be saved by a program at the beginning of the interrupt routine. The PUSHM instruction can save several registers in the register bank being currently used (1) with a single instruction.

Note:
1. Selectable from registers R0, R1, R2, R3, A0, A1, SB, and FB.

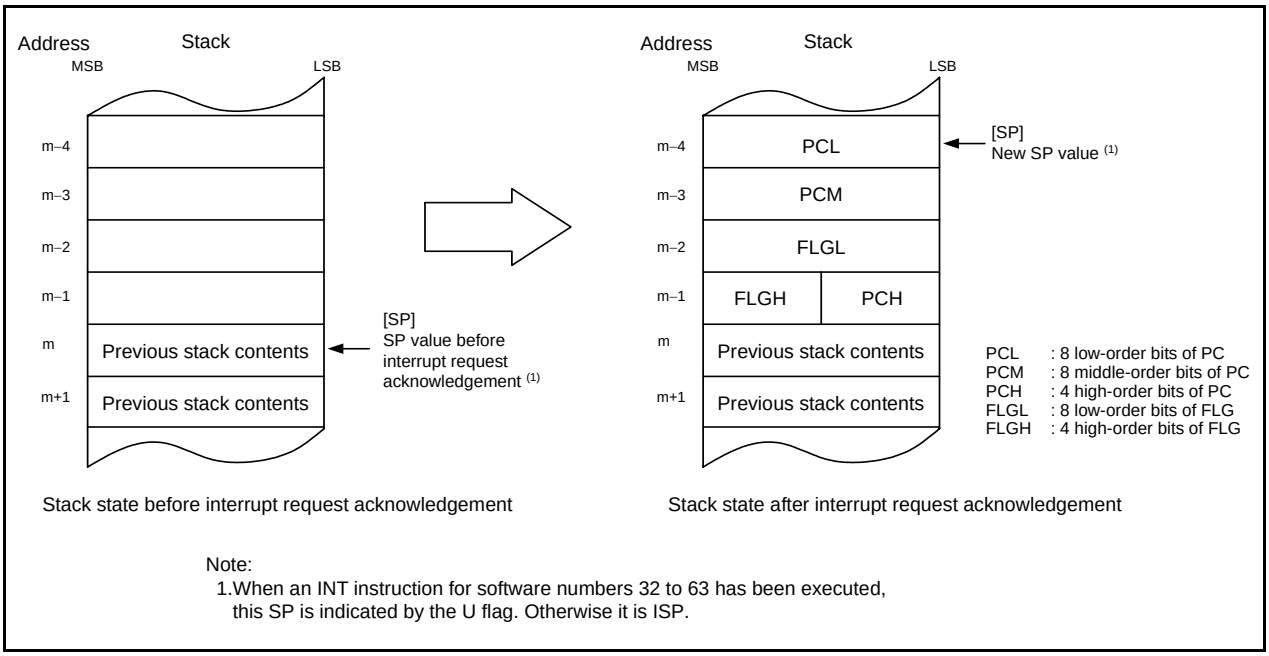
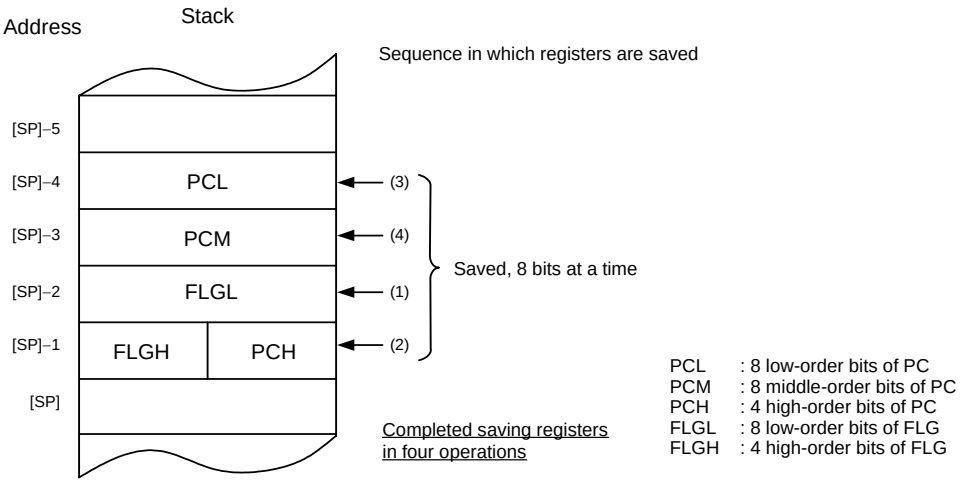


Figure 11.5 Stack State Before and After Acknowledgement of Interrupt Request

The register saving operation, which is performed as part of the interrupt sequence, saved in 8 bits at a time in four steps.
Figure 11.6 shows the Register Saving Operation.



Note:
1. [SP] indicates the SP initial value when an interrupt request is acknowledged.
After registers are saved, the SP content is [SP] minus 4.
When an INT instruction for software numbers 32 to 63 has been executed, this SP is indicated by the U flag. Otherwise it is ISP.

Figure 11.6 Register Saving Operation

11.3.8 Returning from Interrupt Routine

When the REIT instruction is executed at the end of an interrupt routine, the FLG register and PC, which have been saved on the stack, are automatically restored. The program, that was running before the interrupt request was acknowledged, starts running again.

Registers saved by a program in an interrupt routine should be saved using the POPM instruction or a similar instruction before executing the REIT instruction.

11.3.9 Interrupt Priority

If two or more interrupt requests are generated while a single instruction is being executed, the interrupt with the higher priority is acknowledged.

Set bits ILVL2 to ILVL0 to select any priority level for maskable interrupts (peripheral function). However, if two or more maskable interrupts have the same priority level, their interrupt priority is resolved by hardware, with the higher priority interrupts acknowledged.

The priority of watchdog timer and other special interrupts is set by hardware.

Figure 11.7 shows the Hardware Interrupt Priority.

Software interrupts are not affected by the interrupt priority. If an instruction is executed, the MCU executes the interrupt routine.

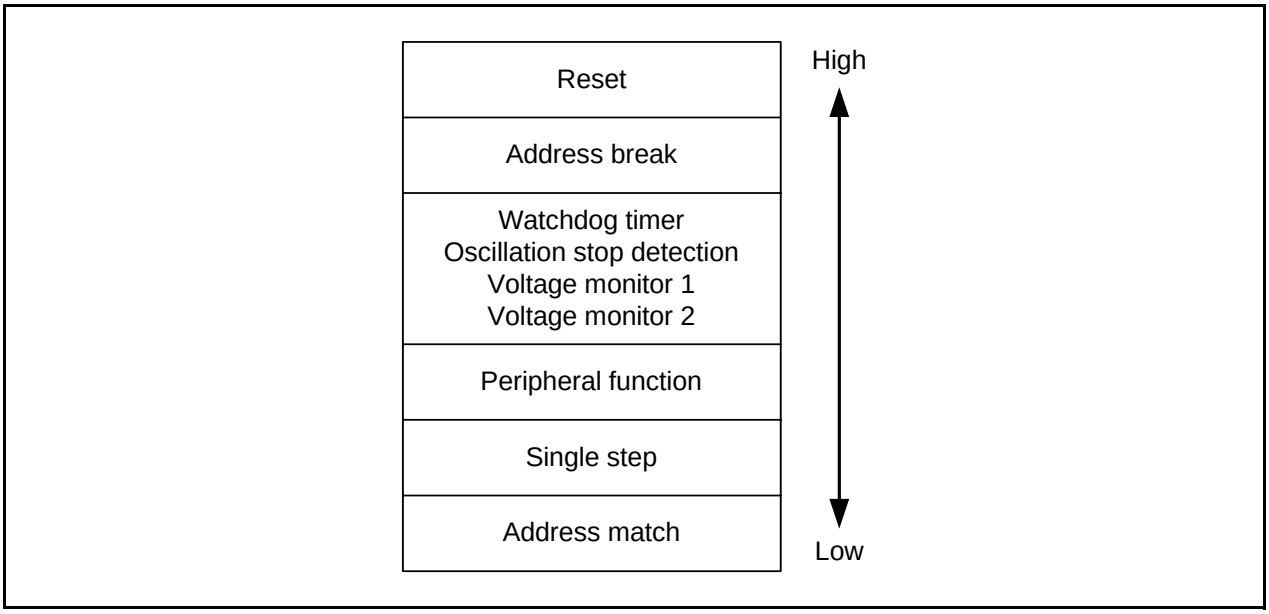


Figure 11.7 Hardware Interrupt Priority

11.3.10 Interrupt Priority Level Selection Circuit

The interrupt priority level selection circuit is used to select the highest priority interrupt. Figure 11.8 shows the Interrupt Priority Level Selection Circuit.

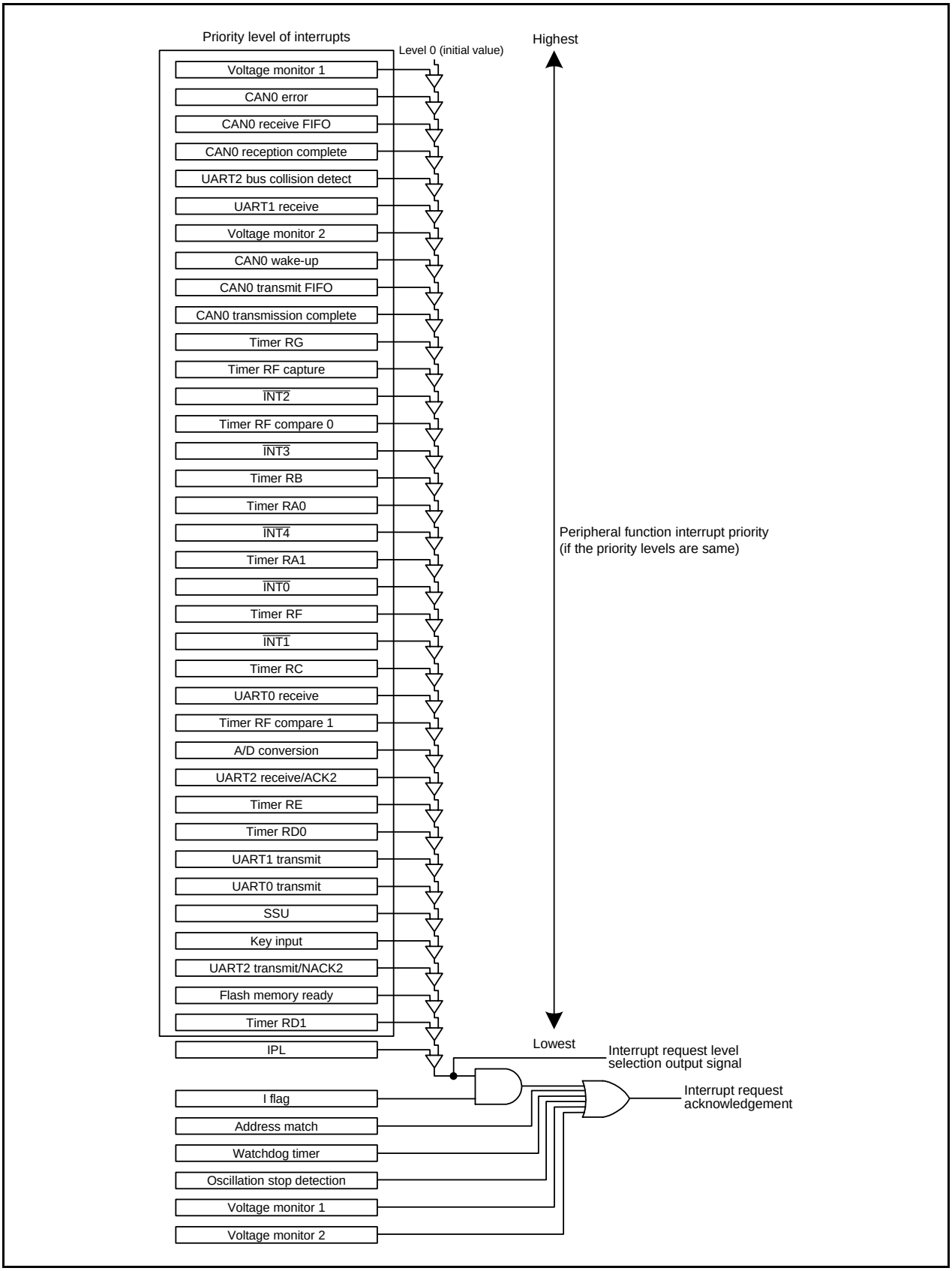


Figure 11.8 Interrupt Priority Level Selection Circuit

11.4 $\overline{\text{INT}}$ Interrupt

11.4.1 $\overline{\text{INTi}}$ Interrupt (i = 0 to 4)

The $\overline{\text{INTi}}$ interrupt is generated by an $\overline{\text{INTi}}$ input. To use the $\overline{\text{INTi}}$ interrupt, set the INTiEN bit in the INTEN register is to 1 (enabled). The edge polarity is selected using the INTiPL bit in the INTEN register and the POL bit in the INTiIC register. The input pins used as the $\overline{\text{INT1}}$ to $\overline{\text{INT3}}$ input can be selected.
Also, inputs can be passed through a digital filter with three different sampling clocks.
The $\overline{\text{INT0}}$ pin is shared with the pulse output forced cutoff input of timer RC and timer RD, and the external trigger input of timer RB, the $\overline{\text{INT2}}$ pin is shared with the event input enabled of timer RA.
Table 11.7 lists the Pin Configuration of $\overline{\text{INT}}$ Interrupt.

Table 11.7 Pin Configuration of $\overline{\text{INT}}$ Interrupt

Pin Name	Assigned Pin	I/O	Function
$\overline{\text{INT0}}$	P4_5	Input	$\overline{\text{INT0}}$ interrupt input, timer RB external trigger input, timer RC and timer RD pulse output forced cutoff input
$\overline{\text{INT1}}$	P1_5, P1_7, P3_2, or P3_6	Input	$\overline{\text{INT1}}$ interrupt input
$\overline{\text{INT2}}$	P3_2, P6_4, or P6_6	Input	$\overline{\text{INT2}}$ interrupt input, timer RA event input enabled
$\overline{\text{INT3}}$	P3_3 or P6_7	Input	$\overline{\text{INT3}}$ interrupt input
$\overline{\text{INT4}}$	P6_5	Input	$\overline{\text{INT4}}$ interrupt input

11.4.2 INT Interrupt Input Pin Select Register (INTSR)

Address 018Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3SEL1	INT3SEL0	INT2SEL1	INT2SEL0	INT1SEL2	INT1SEL1	INT1SEL0	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	INT1SEL0	$\overline{\text{INT1}}$ pin select bit	b3 b2 b1 0 0 0: P1_7 assigned 0 0 1: P1_5 assigned 0 1 1: P3_6 assigned 1 0 0: P3_2 assigned Other than above: Do not set.	R/W
b2	INT1SEL1			R/W
b3	INT1SEL2			R/W
b4	INT2SEL0	$\overline{\text{INT2}}$ pin select bit	b5 b4 0 0: P6_6 assigned 0 1: P3_2 assigned 1 0: P6_4 assigned 1 1: Do not set.	R/W
b5	INT2SEL1			R/W
b6	INT3SEL0	$\overline{\text{INT3}}$ pin select bit	b7 b6 0 0: P3_3 assigned 0 1: Do not set. 1 0: P6_7 assigned 1 1: Do not set.	R/W
b7	INT3SEL1			R/W

The INTSR register selects which pin is assigned to the $\overline{\text{INTi}}$ (i = 1 to 3) input. To use $\overline{\text{INTi}}$, set this register. Set the INTSR register before setting the $\overline{\text{INTi}}$ associated registers. Also, do not change the setting values in this register during $\overline{\text{INTi}}$ operation.

11.4.3 External Input Enable Register 0 (INTEN)

Address 01FAh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3PL	INT3EN	INT2PL	INT2EN	INT1PL	INT1EN	INT0PL	INT0EN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0EN	$\overline{\text{INT0}}$ input enable bit	0: Disabled 1: Enabled	R/W
b1	INT0PL	$\overline{\text{INT0}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b2	INT1EN	$\overline{\text{INT1}}$ input enable bit	0: Disabled 1: Enabled	R/W
b3	INT1PL	$\overline{\text{INT1}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b4	INT2EN	$\overline{\text{INT2}}$ input enable bit	0: Disabled 1: Enabled	R/W
b5	INT2PL	$\overline{\text{INT2}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b6	INT3EN	$\overline{\text{INT3}}$ input enable bit	0: Disabled 1: Enabled	R/W
b7	INT3PL	$\overline{\text{INT3}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W

Notes:
1. To set the INTiPL bit (i = 0 to 3) to 1 (both edges), set the POL bit in the INTiIC register to 0 (falling edge selected).
2. The IR bit in the INTiIC register may be set to 1 (interrupt requested) if the INTEN register is rewritten. Refer to **11.8.4 Changing Interrupt Sources**.

11.4.4 External Input Enable Register 1 (INTEN1)

Address 01FBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	INT4PL	INT4EN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT4EN	$\overline{\text{INT4}}$ input enable bit	0: Disabled 1: Enabled	R/W
b1	INT4PL	$\overline{\text{INT4}}$ input polarity select bit(1, 2)	0: One edge 1: Both edges	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

Notes:
1. To set the INT4PL bit to 1 (both edges), set the POL bit in the INT4IC register to 0 (falling edge selected).
2. The IR bit in the INT4IC register may be set to 1 (interrupt requested) if the INTEN1 register is rewritten. Refer to **11.8.4 Changing Interrupt Sources**.

11.4.5 INT Input Filter Select Register 0 (INTF)

Address 01FCh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3F1	INT3F0	INT2F1	INT2F0	INT1F1	INT1F0	INT0F1	INT0F0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0F0	$\overline{\text{INT0}}$ input filter select bit	b1 b0 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b1	INT0F1			R/W
b2	INT1F0	$\overline{\text{INT1}}$ input filter select bit	b3 b2 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b3	INT1F1			R/W
b4	INT2F0	$\overline{\text{INT2}}$ input filter select bit	b5 b4 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b5	INT2F1			R/W
b6	INT3F0	$\overline{\text{INT3}}$ input filter select bit	b7 b6 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b7	INT3F1			R/W

11.4.6 INT Input Filter Select Register 1 (INTF1)

Address 01FDh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	INT4F1	INT4F0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT4F0	$\overline{\text{INT4}}$ input filter select bit	b1 b0 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b1	INT4F1			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

11.4.7 $\overline{\text{INTi}}$ Input Filter (i = 0 to 4)

The $\overline{\text{INTi}}$ input contains a digital filter. The sampling clock is selected using bits INTiF1 and INTiF0 in registers INTF, INTF1. The $\overline{\text{INTi}}$ level is sampled every sampling clock cycle and if the sampled input level matches three times, the IR bit in the INTiIC register is set to 1 (interrupt requested).

Figure 11.9 shows the $\overline{\text{INTi}}$ Input Filter Configuration. Figure 11.10 shows an Operating Example of $\overline{\text{INTi}}$ Input Filter.

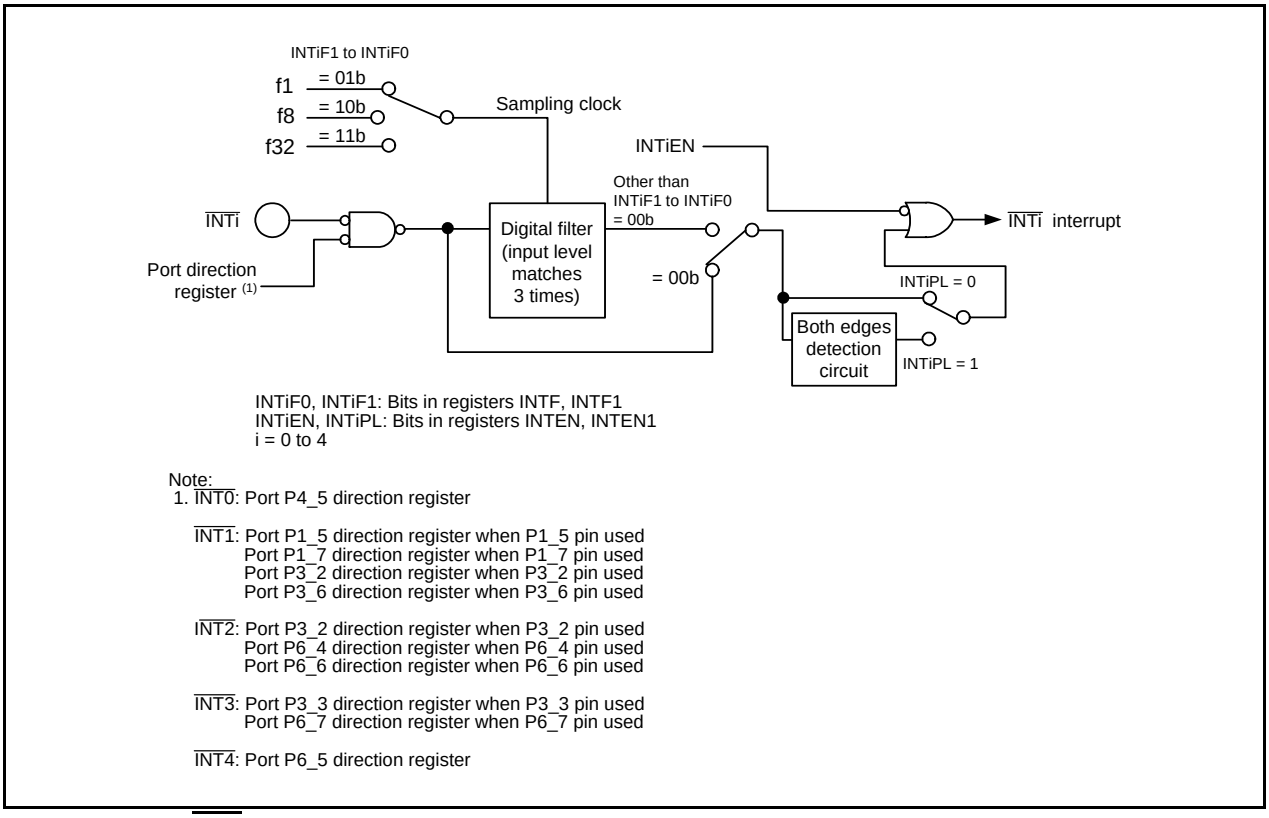


Figure 11.9 $\overline{\text{INTi}}$ Input Filter Configuration

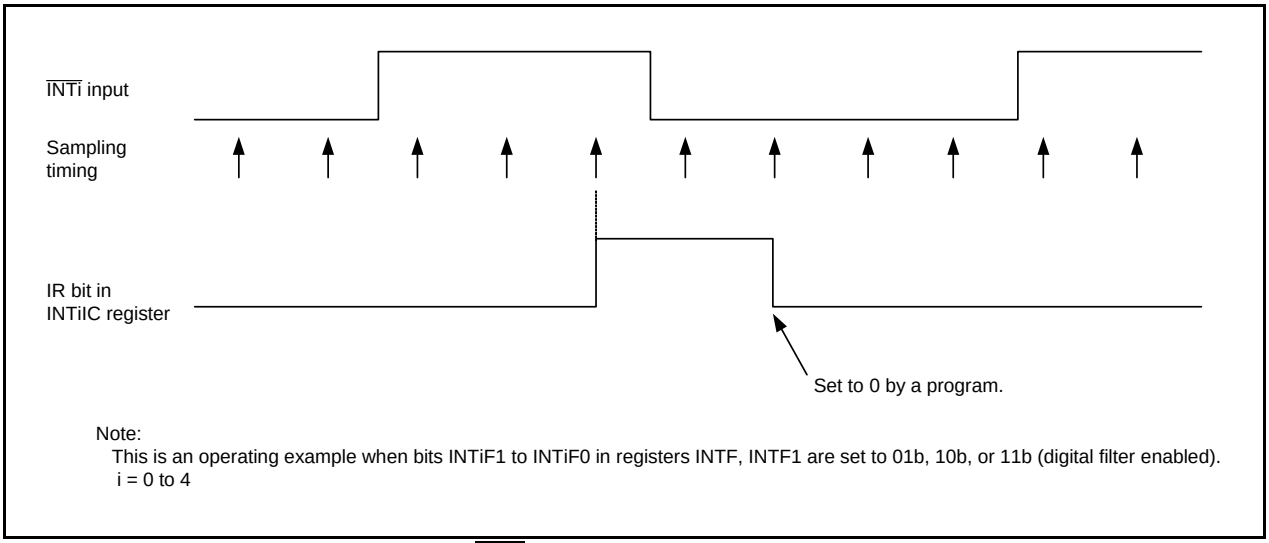


Figure 11.10 Operating Example of $\overline{\text{INTi}}$ Input Filter

11.5 Key Input Interrupt

A key input interrupt request is generated by one of the input edges of pins $\overline{K10}$ to $\overline{K13}$. The key input interrupt can be used as a key-on wake-up function to exit wait or stop mode.

The KIiEN (i = 0 to 3) bit in the KIEN register is be used to select whether or not the pins are used as the $\overline{KIi}$ input. The KIiPL bit in the KIEN register is also be used to select the input polarity.

When inputting "L" to the $\overline{KIi}$ pin, which sets the KIiPL bit to 0 (falling edge), the input to the other pins $\overline{K10}$ to $\overline{K13}$ is not detected as interrupts. When inputting "H" to the $\overline{KIi}$ pin, which sets the KIiPL bit to 1 (rising edge), the input to the other pins $\overline{K10}$ to $\overline{K13}$ is not also detected as interrupts.

Figure 11.11 shows a Block Diagram of Key Input Interrupt. Table 11.8 lists the Pin Configuration of Key Input Interrupt.

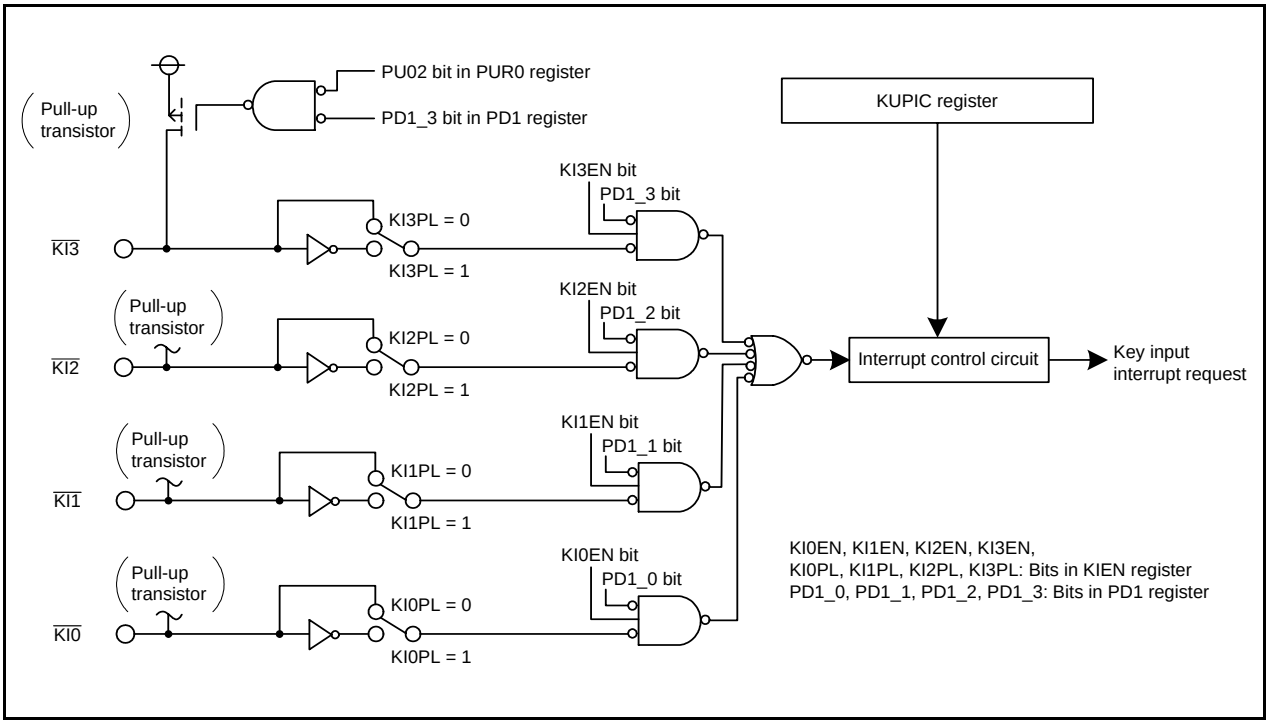


Figure 11.11 Block Diagram of Key Input Interrupt

Table 11.8 Pin Configuration of Key Input Interrupt

Pin Name	I/O	Function
$\overline{KI0}$	Input	$\overline{KI0}$ interrupt input
$\overline{KI1}$	Input	$\overline{KI1}$ interrupt input
$\overline{KI2}$	Input	$\overline{KI2}$ interrupt input
$\overline{KI3}$	Input	$\overline{KI3}$ interrupt input

11.5.1 Key Input Enable Register 0 (KIEN)

Address 01FEh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	KI3PL	KI3EN	KI2PL	KI2EN	KI1PL	KI1EN	KI0PL	KI0EN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	KI0EN	KI0 input enable bit	0: Disabled 1: Enabled	R/W
b1	KI0PL	KI0 input polarity select bit	0: Falling edge 1: Rising edge	R/W
b2	KI1EN	KI1 input enable bit	0: Disabled 1: Enabled	R/W
b3	KI1PL	KI1 input polarity select bit	0: Falling edge 1: Rising edge	R/W
b4	KI2EN	KI2 input enable bit	0: Disabled 1: Enabled	R/W
b5	KI2PL	KI2 input polarity select bit	0: Falling edge 1: Rising edge	R/W
b6	KI3EN	KI3 input enable bit	0: Disabled 1: Enabled	R/W
b7	KI3PL	KI3 input polarity select bit	0: Falling edge 1: Rising edge	R/W

The IR bit in the KUPIC register may be set to 1 (interrupt requested) when the KIEN register is rewritten. Refer to **11.8.4 Changing Interrupt Sources**.

11.6 Address Match Interrupt

An address match interrupt request is generated immediately before execution of the instruction at the address indicated by the RMADi register (i = 0 or 1). This interrupt is used as a break function by the debugger. When the on-chip debugging emulator is used, do not set an address match interrupt (registers AIER0, AIER1, RMAD0, and RMAD1, and fixed vector tables) in the user system.

Set the starting address of any instruction in the RMADi register (i = 0 or 1). The AIERi0 bit in the AIERi register can be used to select enable or disable the interrupt. The address match interrupt is not affected by the I flag and IPL.

The PC value (Refer to **11.3.7 Saving Registers**) which is saved on the stack when an address match interrupt request is acknowledged varies depending on the instruction at the address indicated by the RMADi register. (The appropriate return address is not saved on the stack.) When returning from the address match interrupt, follow one of the following means:

- Rewrite the contents of the stack and use the REIT instruction to return.
- Use an instruction such as POP to restore the stack to its previous state before the interrupt request was acknowledged. Then use a jump instruction to return.

Table 11.9 lists the PC Value Saved on Stack When Address Match Interrupt Request is Acknowledged.

Table 11.9 PC Value Saved on Stack When Address Match Interrupt Request is Acknowledged

Address Indicated by RMADi Register (i = 0 or 1)	PC Value Saved (1)
• Instruction with 2-byte operation code (2) • Instruction with 1-byte operation code (2) ADD.B:S #IMM8,dest SUB.B:S #IMM8,dest AND.B:S #IMM8,dest OR.B:S #IMM8,dest MOV.B:S #IMM8,dest STZ #IMM8,dest STNZ #IMM8,dest STZX #IMM81,#IMM82,dest CMP.B:S #IMM8,dest PUSHM src POPM dest JMPS #IMM8 JSRS #IMM8 MOV.B:S #IMM,dest (however, dest = A0 or A1)	Address indicated by RMADi register + 2
• Instructions other than above	Address indicated by RMADi register + 1

Notes:
1. Refer to the **11.3.7 Saving Registers**.
2. Operation code: Refer to the **R8C/Tiny Series Software Manual** (REJ09B0001).
   Chapter 4. Instruction Code/Number of Cycles contains diagrams showing operation code below each syntax. Operation code is shown in the bold frame in the diagrams.

Table 11.10 Correspondence Between Address Match Interrupt Sources and Associated Registers

Address Match Interrupt Source	Address Match Interrupt Enable Bit	Address Match Interrupt Register
Address match interrupt 0	AIER00	RMAD0
Address match interrupt 1	AIER10	RMAD1

11.6.1 Address Match Interrupt Enable Register i (AIERi) (i = 0 or 1)

Address 01C3h (AIER0), 01C7h (AIER1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	—	—	—	—	—	AIER00	AIER0 register
After Reset	0	0	0	0	0	0	0	0	

Symbol	—	—	—	—	—	—	—	AIER10	AIER1 register
After Reset	0	0	0	0	0	0	0	0	

Bit	Symbol	Bit Name	Function	R/W
b0	AIERi0	Address match interrupt i enable bit	0: Disabled 1: Enabled	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

11.6.2 Address Match Interrupt Register i (RMADi) (i = 0 or 1)

Address 01C2h to 01C0h (RMAD0), 01C6h to 01C4h (RMAD1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b23	b22	b21	b20	b19	b18	b17	b16
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	X	X	X	X

Bit	Symbol	Function	Setting Range	R/W
b19 to b0	—	Address setting register for address match interrupt	00000h to FFFFFh	R/W
b20	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b21	—			
b22	—			
b23	—			

11.7 Timer RC Interrupt, Timer RD Interrupt, Timer RG Interrupt, Synchronous Serial Communication Unit Interrupt, and Flash Memory Interrupt (Interrupts with Multiple Interrupt Request Sources)

The timer RC interrupt, timer RD0 interrupt, timer RD1 interrupt, timer RG interrupt, synchronous serial communication unit interrupt, and flash memory interrupt each have multiple interrupt request sources. An interrupt request is generated by the logical OR of several interrupt request sources and is reflected in the IR bit in the corresponding interrupt control register. Therefore, each of these peripheral functions has its own interrupt request source status register (status register) and interrupt request source enable register (enable register) to control the generation of interrupt requests (change of the IR bit in the interrupt control register). Table 11.11 lists the Registers Associated with Timer RC Interrupt, Timer RD Interrupt, Timer RG Interrupt, Synchronous Serial Communication Unit Interrupt, and Flash Memory Interrupt and Figure 11.12 shows a Block Diagram of Timer RD Interrupt.

Table 11.11 Registers Associated with Timer RC Interrupt, Timer RD Interrupt, Timer RG Interrupt, Synchronous Serial Communication Unit Interrupt, and Flash Memory Interrupt

Peripheral Function Name	Status Register of Interrupt Request Source	Enable Register of Interrupt Request Source	Interrupt Control Register
Timer RC	TRCSR	TRCIER	TRCIC
Timer RD0	TRDSR0	TRDIER0	TRD0IC
Timer RD1	TRDSR1	TRDIER1	TRD1IC
Timer RG	TRGSR	TRGIER	TRGIC
Synchronous serial communication unit	SSSR	SSER	SSUIC
Flash memory	RDYSTI	RDYSTIE	FMRDYIC
	BSYAEI	BSYAEIE	
		CMDERIE	

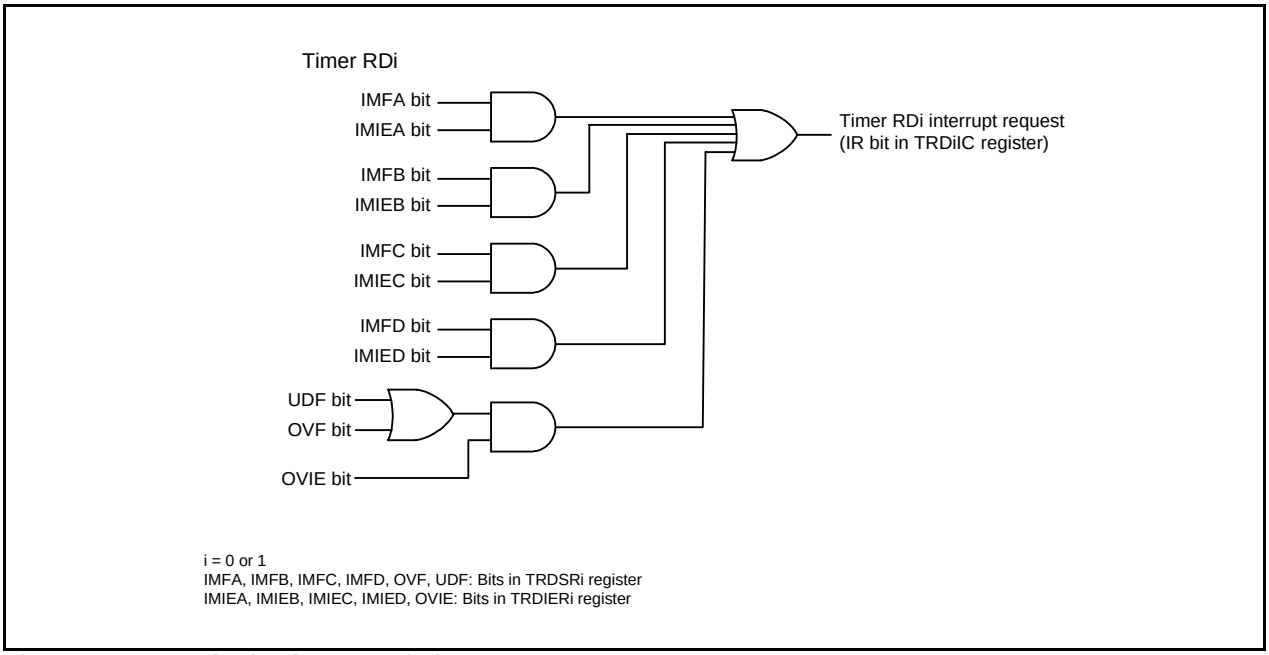


Figure 11.12 Block Diagram of Timer RD Interrupt

As with other maskable interrupts, the timer RC interrupt, timer RD0 interrupt, timer RD1 interrupt, timer RG interrupt, synchronous serial communication unit interrupt, and flash memory interrupt are controlled by the combination of the I flag, IR bit, bits ILVL0 to ILVL2, and IPL. However, since each interrupt source is generated by a combination of multiple interrupt request sources, the following differences from other maskable interrupts apply:

- When bits in the enable register are set to 1 and the corresponding bits in the status register are set to 1 (interrupt enabled), the IR bit in the interrupt control register is set to 1 (interrupt requested).
- When either bits in the status register or the corresponding bits in the enable register, or both are set to 0, the IR bit is set to 0 (no interrupt requested).
  That is, even if the interrupt is not acknowledged after the IR bit is set to 1, the interrupt request will not be retained.
  Also, the IR bit is not set to 0 even if 0 is written to this bit.
- Individual bits in the status register are not automatically set to 0 even if the interrupt is acknowledged.
  The IR bit is also not automatically set to 0 when the interrupt is acknowledged.
  Set individual bits in the status register to 0 in the interrupt routine. Refer to the status register figure for how to set individual bits in the status register to 0.
- When multiple bits in the enable register are set to 1 and other request sources are generated after the IR bit is set to 1, the IR bit remains 1.
- When multiple bits in the enable register are set to 1, use the status register to determine which request source causes an interrupt.

Refer to chapters of the individual peripheral functions (**19. Timer RC**, **20. Timer RD**, **23. Timer RG**, **26. Synchronous Serial Communication Unit (SSU),** and **30. Flash Memory**) for the status register and enable register.
For the interrupt control register, refer to **11.3 Interrupt Control**.

11.8 Notes on Interrupts

11.8.1 Reading Address 00000h

Do not read address 00000h by a program. When a maskable interrupt request is acknowledged, the CPU reads interrupt information (interrupt number and interrupt request level) from 00000h in the interrupt sequence. At this time, the IR bit for the acknowledged interrupt is set to 0.
If address 00000h is read by a program, the IR bit for the interrupt which has the highest priority among the enabled interrupts is set to 0. This may cause the interrupt to be canceled, or an unexpected interrupt to be generated.

11.8.2 SP Setting

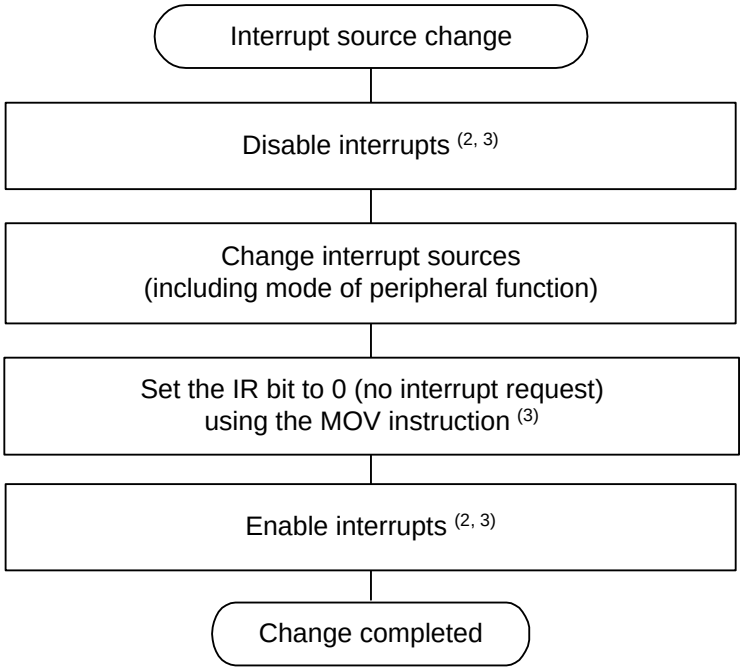
Set a value in the SP before an interrupt is acknowledged. The SP is set to 0000h after a reset. If an interrupt is acknowledged before setting a value in the SP, the program may run out of control.

11.8.3 External Interrupt and Key Input Interrupt

Either the “L” level width or “H” level width shown in the Electrical Characteristics is required for the signal input to pins $\overline{\text{INT0}}$ to $\overline{\text{INT4}}$ and pins $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$, regardless of the CPU clock.
For details, refer to **Table 32.22** (VCC = 5 V), **Table 32.30** (VCC = 3 V) **External Interrupt $\overline{\text{INTi}}$ (i = 0 to 4) Input, Key Input Interrupt $\overline{\text{KIi}}$ (i = 0 to 3)**.

11.8.4 Changing Interrupt Sources

The IR bit in the interrupt control register may be set to 1 (interrupt requested) when the interrupt source changes. To use an interrupt, set the IR bit to 0 (no interrupt requested) after changing interrupt sources.
Changing interrupt sources as referred to here includes all factors that change the source, polarity, or timing of the interrupt assigned to a software interrupt number. Therefore, if a mode change of a peripheral function involves the source, polarity, or timing of an interrupt, set the IR bit to 0 (no interrupt requested) after making these changes. Refer to the descriptions of the individual peripheral functions for related interrupts.
Figure 11.13 shows a Procedure Example for Changing Interrupt Sources.



IR bit: The interrupt control register bit for the interrupt whose source is to be changed

Notes:
1. The above settings must be executed individually. Do not execute two or more settings simultaneously (using one instruction).
2. To prevent interrupt requests from being generated disable the peripheral function before changing the interrupt source. In this case, use the I flag if all maskable interrupts can be disabled.
   If all maskable interrupts cannot be disabled, use bits ILVL0 to ILVL2 for the interrupt whose source is to be changed.
3. To change the interrupt source to the input with the digital filter used, wait for three or more cycles of the sampling clock of the digital filter before setting the IR bit to 0 (no interrupt request). Refer to **11.8.5 Rewriting Interrupt Control Register** for the instructions to use and related notes.

Figure 11.13 Procedure Example for Changing Interrupt Sources

11.8.5 Rewriting Interrupt Control Register

(a) The contents of the interrupt control register can be rewritten only while no interrupt requests corresponding to that register are generated. If an interrupt request may be generated, disable the interrupt before rewriting the contents of the interrupt control register.

(b) When rewriting the contents of the interrupt control register after disabling the interrupt, be careful to choose appropriate instructions.
Changing any bit other than the IR bit
If an interrupt request corresponding to the register is generated while executing the instruction, the IR bit may not be set to 1 (interrupt requested), and the interrupt may be ignored. If this causes a problem, use one of the following instructions to rewrite the contents of the register: AND, OR, BCLR, and BSET.

Changing the IR bit
Depending on the instruction used, the IR bit may not be set to 0 (no interrupt requested).
Use the MOV instruction to set the IR bit to 0.

(c) When using the I flag to disable an interrupt, set the I flag as shown in the sample programs below. Refer to (b) regarding rewriting the contents of interrupt control registers using the sample programs.

Examples 1 to 3 shows how to prevent the I flag from being set to 1 (interrupts enabled) before the contents of the interrupt control register are rewritten for the effects of the internal bus and the instruction queue buffer.

Example 1: Use the NOP instructions to pause program until the interrupt control register is rewritten

```
INT_SWITCH1:
    FCLR    I               ; Disable interrupts
    AND.B   #00H,0056H      ; Set the TRA0IC register to 00h
    NOP                     ;
    NOP
    FSET    I               ; Enable interrupts
```

Example 2: Use a dummy read to delay the FSET instruction

```
INT_SWITCH2:
    FCLR    I               ; Disable interrupts
    AND.B   #00H,0056H      ; Set the TRA0IC register to 00h
    MOV.W   MEM,R0          ; Dummy read
    FSET    I               ; Enable interrupts
```

Example 3: Use the POPC instruction to change the I flag

```
INT_SWITCH3:
    PUSHC   FLG
    FCLR    I               ; Disable interrupts
    AND.B   #00H,0056H      ; Set the TRA0IC register to 00h
    POPC    FLG             ; Enable interrupts
```

12. ID Code Areas

The ID code areas are used to implement a function that prevents the flash memory from being rewritten in standard serial I/O mode. This function prevents the flash memory from being read, rewritten, or erased.

12.1 Overview

The ID code areas are assigned to 0FFDFh, 0FFE3h, 0FFEBh, 0FFEFh, 0FFF3h, 0FFF7h, and 0FFFBh of the respective vector highest-order addresses of the fixed vector table. Figure 12.1 shows the ID Code Areas.

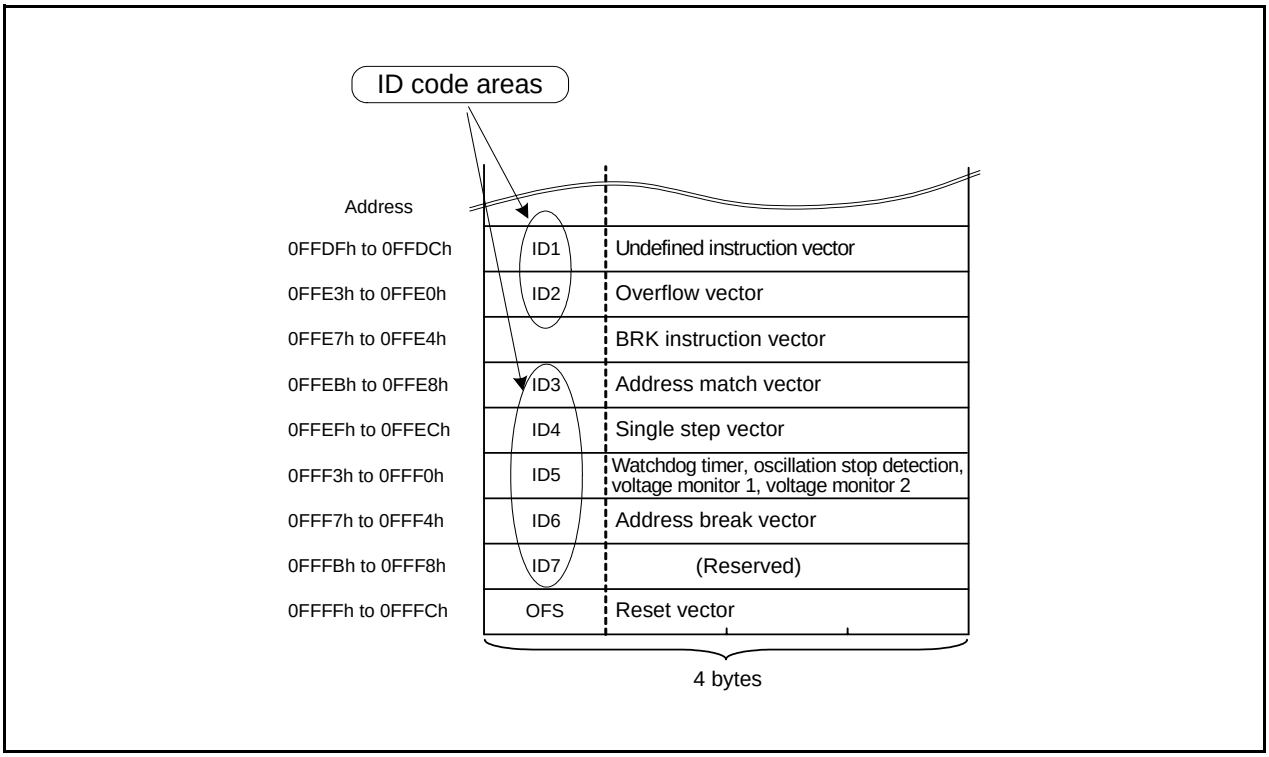


Figure 12.1 ID Code Areas

12.2 Functions

The ID code areas are used in standard serial I/O mode. Unless 3 bytes (addresses 0FFFCh to 0FFFEh) of the reset vector are set to FFFFFFh, the ID codes stored in the ID code areas and the ID codes sent from the serial programmer or the on-chip debugging emulator are checked to see if they match. If the ID codes match, the commands sent from the serial programmer or the on-chip debugging emulator are acknowledged. If the ID codes do not match, the commands are not acknowledged. To use the serial programmer or the on-chip debugging emulator, first write predetermined ID codes to the ID code areas.
If 3 bytes (addresses 0FFFCh to 0FFFEh) of the reset vector are set to FFFFFFh, the ID codes are not checked and all commands are accepted.

The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.

The character sequence of the ASCII codes “ALeRASE” is the reserved word used for the forced erase function. The character sequence of the ASCII codes “Protect” is the reserved word used for the standard serial I/O mode disabled function. Table 12.1 shows the ID Code Reserved Word. The reserved word is a set of reserved characters when all the addresses and data in the ID code storage addresses sequentially match Table 12.1. When the forced erase function or standard serial I/O mode disabled function is not used, use another character sequence of the ASCII codes.

Table 12.1 ID Code Reserved Word

ID Code Storage Address		ID Code Reserved Word (ASCII) (1)	
		ALeRASE	Protect
0FFDFh	ID1	41h (upper-case A)	50h (upper-case P)
0FFE3h	ID2	4Ch (upper-case L)	72h (lower-case r)
0FFEBh	ID3	65h (lower-case e)	6Fh (lower-case o)
0FFEFh	ID4	52h (upper-case R)	74h (lower-case t)
0FFF3h	ID5	41h (upper-case A)	65h (lower-case e)
0FFF7h	ID6	53h (upper-case S)	63h (lower-case c)
0FFFBh	ID7	45h (upper-case E)	74h (lower-case t)

Note:
1. Reserve word: A set of characters when all the addresses and data in the ID code storage addresses sequentially match Table 12.1.

12.3 Forced Erase Function

This function is used in standard serial I/O mode. When the ID codes sent from the serial programmer or the on-chip debugging emulator are “ALeRASE” in ASCII code, the content of the user ROM area will be erased at once. However, if the contents of the ID code addresses are set to other than “ALeRASE” (other than **Table 12.1 ID Code Reserved Word**) when the ROMCR bit in the OFS register is set to 1 and the ROMCP1 bit is set to 0 (ROM code protect enabled), forced erasure is not executed and the ID codes are checked with the ID code check function. Table 12.2 lists the Conditions and Operations of Forced Erase Function.
Also, when the contents of the ID code addresses are set to “ALeRASE” in ASCII code, if the ID codes sent from the serial programmer or the on-chip debugging emulator are “ALeRASE”, the content of the user ROM area will be erased. If the ID codes sent from the serial programmer are other than “ALeRASE”, the ID codes do not match and no command is acknowledged, thus the user ROM area remains protected.

Table 12.2 Conditions and Operations of Forced Erase Function

Condition			Operation
ID code from serial programmer or the on-chip debugging emulator	ID code in ID code storage address	Bits ROMCP1 and ROMCR in OFS register	
ALeRASE	ALeRASE	–	All erasure of user ROM area (forced erase function)
	Other than ALeRASE (1)	Other than 01b (ROM code protect disabled)	
		01b (ROM code protect enabled)	ID code check (ID code check function)
Other than ALeRASE	ALeRASE	–	ID code check (ID code check function. No ID code match.)
	Other than ALeRASE (1)	–	ID code check (ID code check function)

Note:
1. For “Protect”, refer to **12.4 Standard Serial I/O Mode Disabled Function**.

12.4 Standard Serial I/O Mode Disabled Function

This function is used in standard serial I/O mode. When the I/D codes in the ID code storage addresses are set to the reserved character sequence of the ASCII codes “Protect” (refer to **Table 12.1 ID Code Reserved Word**), communication with the serial programmer or the on-chip debugging emulator is not performed. This does not allow the flash memory to be read, rewritten, or erased using the serial programmer or the on-chip debugging emulator.
Also, if the ID codes are also set to the reserved character sequence of the ASCII codes “Protect” when the ROMCR bit in the OFS register is set to 1 and the ROMCP1 bit is set to 0 (ROM code protect enabled), ROM code protection cannot be disabled using the serial programmer or the on-chip debugging emulator. This prevents the flash memory from being read, rewritten, or erased using the serial programmer, the on-chip debugging emulator, or parallel programmer.

12.5 Notes on ID Code Areas

12.5.1 Setting Example of ID Code Areas

The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

- To set 55h in all of the ID code areas

```
.org 00FFDCH
.lword dummy | (55000000h)    ; UND
.lword dummy | (55000000h)    ; INTO
.lword dummy ; BREAK
.lword dummy | (55000000h)    ; ADDRESS MATCH
.lword dummy | (55000000h)    ; SET SINGLE STEP
.lword dummy | (55000000h)    ; WDT
.lword dummy | (55000000h)    ; ADDRESS BREAK
.lword dummy | (55000000h)    ; RESERVE
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

13. Option Function Select Area

13.1 Overview

The option function select area is used to select the MCU state after a reset, the function to prevent rewriting in parallel I/O mode, or the watchdog timer operation. The reset vector highest-order-address, 0FFFFh and 0FFDBh, are assigned as the option function select area. Figure 13.1 shows the Option Function Select Area.

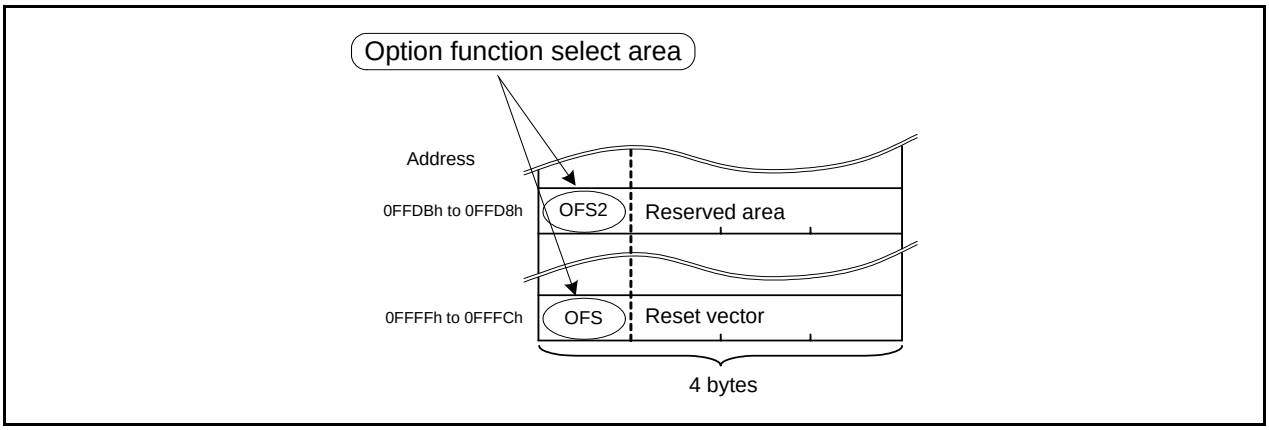


Figure 13.1 Option Function Select Area

13.2 Registers

Registers OFS and OFS2 are used to select the MCU state after a reset, the function to prevent rewriting in parallel I/O mode, or the watchdog timer operation.

13.2.1 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	—	—	ROMCP1	ROMCR	—	WDTON
After Reset	User Setting Value (Note 1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset. 1: Watchdog timer is stopped after reset.	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	—	Reserved bits	Set to 1.	R/W
b5	—			
b6	LVDAS	Voltage detection 0 circuit start bit (2)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protect mode enabled after reset 1: Count source protect mode disabled after reset	R/W

Notes:

1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS register. If the block including the OFS register is erased, the OFS register is set to FFh.
   When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.
2. To use power-on reset and voltage monitor 0 reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

For a setting example of the OFS register, refer to **13.3.1 Setting Example of Option Function Select Area**.

13.2.2 Option Function Select Register 2 (OFS2)

Address 0FFDBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	WDTRCS1	WDTRCS0	WDTUFS1	WDTUFS0
After Reset	User Setting Value (Note 1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTUFS0	Watchdog timer underflow period set bit	b1 b0 0 0: 03FFh 0 1: 0FFFh 1 0: 1FFFh 1 1: 3FFFh	R/W
b1	WDTUFS1			R/W
b2	WDTRCS0	Watchdog timer refresh acknowledgement period set bit	b3 b2 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100%	R/W
b3	WDTRCS1			R/W
b4	—	Reserved bits	Set to 1.	R/W
b5	—			
b6	—			
b7	—			

Note:

1. The OFS2 register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS2 register. If the block including the OFS2 register is erased, the OFS2 register is set to FFh.
   When blank products are shipped, the OFS2 register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS2 register is the value programmed by the user.

   For a setting example of the OFS2 register, refer to **13.3.1 Setting Example of Option Function Select Area**.

Bits WDTRCS0 and WDTRCS1 (Watchdog Timer Refresh Acknowledgement Period Set Bit)

Assuming that the period from when the watchdog timer starts counting until it underflows is 100%, the refresh acknowledgement period for the watchdog timer can be selected.
For details, refer to **14.3.1.1 Refresh Acknowledgment Period**.

13.3 Notes on Option Function Select Area

13.3.1 Setting Example of Option Function Select Area

The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

- To set FFh in the OFS register

```
.org 00FFFCH
.lword reset | (0FF000000h)      ; RESET
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

- To set FFh in the OFS2 register

```
.org 00FFDBH
.byte 0FFh
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

14. Watchdog Timer

The watchdog timer is a function that detects when a program is out of control. Use of the watchdog timer is recommended to improve the reliability of the system.

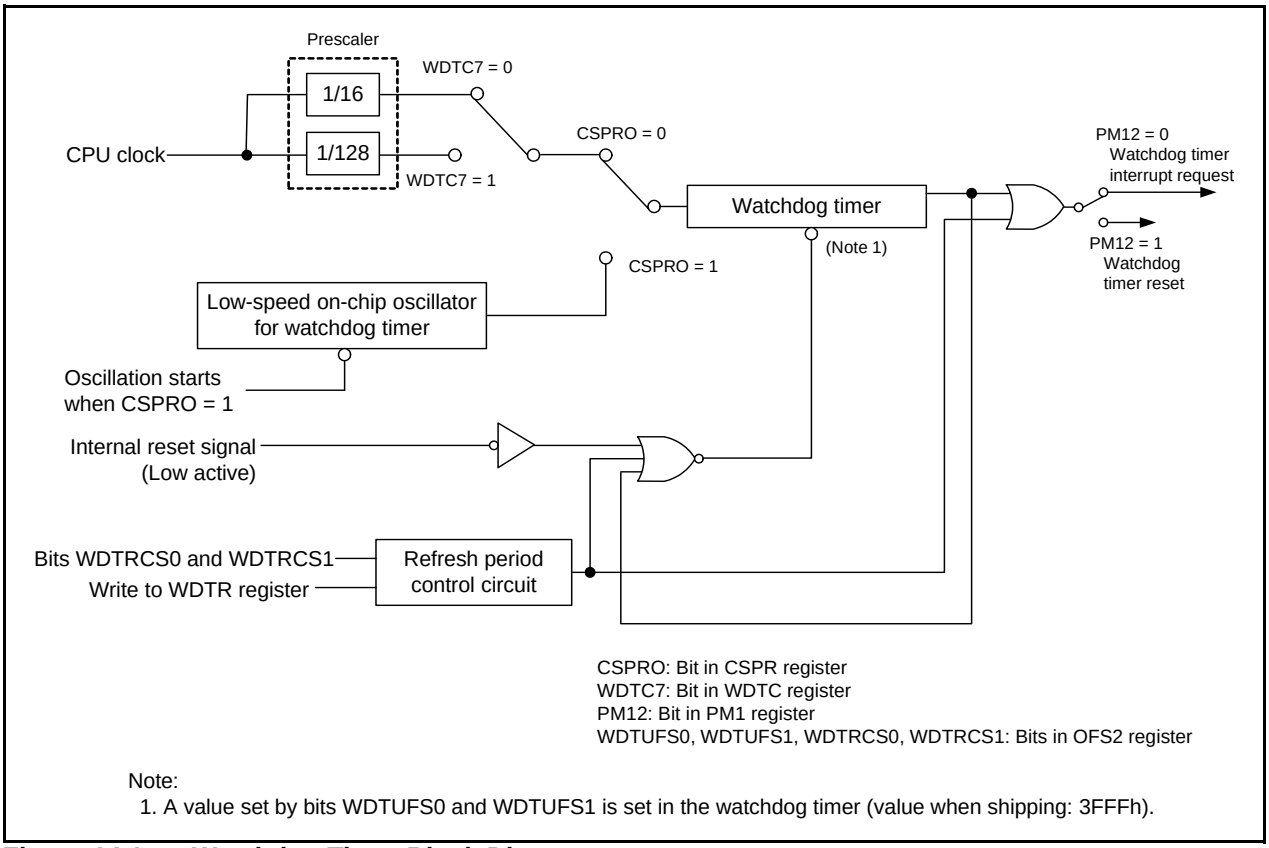
14.1 Overview

The watchdog timer contains a 14-bit counter and allows selection of count source protection mode enable or disable.
Table 14.1 lists the Watchdog Timer Specifications.
Refer to **5.5 Watchdog Timer Reset** for details of the watchdog timer reset.
Figure 14.1 shows a Watchdog Timer Block Diagram.

Table 14.1 Watchdog Timer Specifications

Item	Count Source Protection Mode Disabled	Count Source Protection Mode Enabled
Count source	CPU clock	Low-speed on-chip oscillator clock for the watchdog timer
Count operation	Decrement	
Count start condition	Either of the following can be selected: • After a reset, count starts automatically. • Count starts by writing to the WDTS register.	
Count stop condition	Stop mode, wait mode	None
Watchdog timer initialization conditions	• Reset • Write 00h and then FFh to the WDTR register (with acknowledgement period setting).(1) • Underflow	
Operations at underflow	Watchdog timer interrupt or watchdog timer reset	Watchdog timer reset
Selectable functions	• Division ratio of the prescaler Selected by the WDTC7 bit in the WDTC register. • Count source protection mode Whether count source protection mode is enabled or disabled after a reset can be selected by the CSPROINI bit in the OFS register (flash memory). If count source protection mode is disabled after a reset, it can be enabled or disabled by the CSPRO bit in the CSPR register (program). • Start or stop of the watchdog timer after a reset Selected by the WDTON bit in the OFS register (flash memory). • Initial value of the watchdog timer Selectable by bits WDTUFS0 and WDTUFS1 in the OFS2 register. • Refresh acknowledgement period for the watchdog timer Selectable by bits WDTRCS0 and WDTRCS1 in the OFS2 register.	

Note:
1. Write the WDTR register during the count operation of the watchdog timer.



Note:
1. A value set by bits WDTUFS0 and WDTUFS1 is set in the watchdog timer (value when shipping: 3FFFh).

Figure 14.1 Watchdog Timer Block Diagram

14.2 Registers

14.2.1 Processor Mode Register 1 (PM1)

Address 0005h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	PM12	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	PM12	WDT interrupt/reset switch bit	0: Watchdog timer interrupt 1: Watchdog timer reset (1)	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—	Reserved bit	Set to 0.	R/W

Note:
1. The PM12 bit is set to 1 when 1 is written by a program (and remains unchanged even if 0 is written to it). This bit is automatically set to 1 when the CSPRO bit in the CSPR register is set to 1 (count source protection mode enabled).

Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting the PM1 register.

14.2.2 Watchdog Timer Reset Register (WDTR)

Address 000Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	R/W
b7 to b0	Writing 00h and then FFh to this register initializes the watchdog timer. The initial value of the watchdog timer is specified by bits WDTUFS0 and WDTUFS1 in the OFS2 register. (1)	W

Note:
1. Write the WDTR register during the count operation of the watchdog timer.

14.2.3 Watchdog Timer Start Register (WDTS)

Address 000Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	R/W
b7 to b0	A write instruction to this register starts the watchdog timer.	W

14.2.4 Watchdog Timer Control Register (WDTC)

Address 000Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	WDTC7	—	—	—	—	—	—	—
After Reset	0	0	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	—	The following bits of the watchdog timer can be read. When bits WDTUFS1 to WDTUFS0 in the OFS2 register are set to 00b (03FFh): b5 to b0 01b (0FFFh): b7 to b2 10b (1FFFh): b8 to b3 11b (3FFFh): b9 to b4		R
b1	—			R
b2	—			R
b3	—			R
b4	—			R
b5	—			R
b6	—	Reserved bit	When read, the content is 0.	R
b7	WDTC7	Prescaler select bit	0: Divided-by-16 1: Divided-by-128	R/W

14.2.5 Count Source Protection Mode Register (CSPR)

Address 001Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPRO	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

The above applies when the CSPROINI bit in the OFS register is set to 1.

After Reset	1	0	0	0	0	0	0	0

The above applies when the CSPROINI bit in the OFS register is set to 0.

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	CSPRO	Count source protection mode select bit (1)	0: Count source protection mode disabled 1: Count source protection mode enabled	R/W

Note:
1. To set the CSPRO bit to 1, write 0 and then 1 to it. This bit cannot be set to 0 by a program. Disable interrupts and DTC activation between writing 0 and writing 1.

14.2.6 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	—	—	ROMCP1	ROMCR	—	WDTON
After Reset	User Setting Value (Note 1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset. 1: Watchdog timer is stopped after reset.	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	—	Reserved bits	Set to 1.	R/W
b5	—			
b6	LVDAS	Voltage detection 0 circuit start bit (2)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protect mode enabled after reset 1: Count source protect mode disabled after reset	R/W

Notes:

1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS register. If the block including the OFS register is erased, the OFS register is set to FFh.
   When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.
2. To use power-on reset and voltage monitor 0 reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

For a setting example of the OFS register, refer to **13.3.1 Setting Example of Option Function Select Area**.

14.2.7 Option Function Select Register 2 (OFS2)

Address 0FFDBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	WDTRCS1	WDTRCS0	WDTUFS1	WDTUFS0
After Reset	User Setting Value (Note 1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTUFS0	Watchdog timer underflow period set bit	b1 b0 0 0: 03FFh 0 1: 0FFFh 1 0: 1FFFh 1 1: 3FFFh	R/W
b1	WDTUFS1			R/W
b2	WDTRCS0	Watchdog timer refresh acknowledgement period set bit	b3 b2 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100%	R/W
b3	WDTRCS1			R/W
b4	—	Reserved bits	Set to 1.	R/W
b5	—			
b6	—			
b7	—			

Note:

1. The OFS2 register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS2 register. If the block including the OFS2 register is erased, the OFS2 register is set to FFh.
   When blank products are shipped, the OFS2 register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS2 register is the value programmed by the user.

   For a setting example of the OFS2 register, refer to **13.3.1 Setting Example of Option Function Select Area**.

Bits WDTRCS0 and WDTRCS1 (Watchdog Timer Refresh Acknowledgement Period Set Bit)

Assuming that the period from when the watchdog timer starts counting until it underflows is 100%, the refresh acknowledgement period for the watchdog timer can be selected.
For details, refer to **14.3.1.1 Refresh Acknowledgment Period**.

14.3 Functional Description

14.3.1 Common Items for Multiple Modes

14.3.1.1 Refresh Acknowledgment Period

The period for acknowledging refreshment operation to the watchdog timer (write to the WDTR register) can be selected by bits WDTRCS0 and WDTRCS1 in the OFS2 register. Figure 14.2 shows the Refresh Acknowledgement Period for Watchdog Timer.

Assuming that the period from when the watchdog timer starts counting until it underflows is 100%, a refresh operation executed during the refresh acknowledgement period is acknowledged. Any refresh operation executed during the period other than the above is processed as an incorrect write, and a watchdog timer interrupt or watchdog timer reset (selectable by the PM12 bit in the PM1 register) is generated.

Do not execute any refresh operation while the count operation of the watchdog timer is stopped.

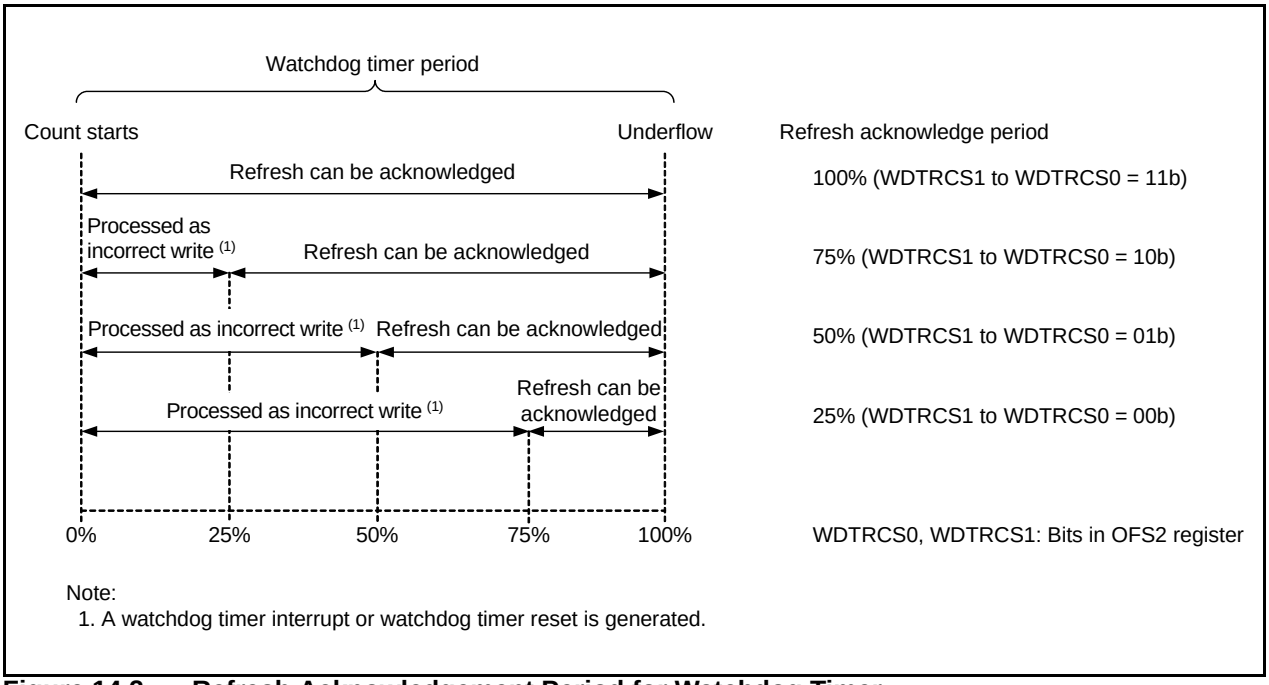


Figure 14.2 Refresh Acknowledgement Period for Watchdog Timer

14.3.2 Count Source Protection Mode Disabled

The count source for the watchdog timer is the CPU clock when count source protection mode is disabled. Table 14.2 lists the Watchdog Timer Specifications (Count Source Protection Mode Disabled).

Table 14.2 Watchdog Timer Specifications (Count Source Protection Mode Disabled)

Item	Specification
Count source	CPU clock
Count operation	Decrement
Period	$\frac{\text{Division ratio of prescaler (n)} \times \text{count value of watchdog timer (m)}}{\text{CPU clock}}$ (1) n: 16 or 128 (selected by the WDTC7 bit in the WDTC register) m: Value set by bits WDTUFS0 and WDTUFS1 in the OFS2 register Example: The period is approximately 13.1 ms when: - The CPU clock frequency is set to 20 MHz. - The prescaler is divided by 16. - Bits WDTUFS1 to WDTUFS0 are set to 11b (3FFFh).
Watchdog timer initialization conditions	• Reset • Write 00h and then FFh to the WDTR register.(3) • Underflow
Count start conditions	The operation of the watchdog timer after a reset is selected by the WDTON bit (2) in the OFS register (address 0FFFFh). • When the WDTON bit is set to 1 (watchdog timer is stopped after reset). The watchdog timer and prescaler are stopped after a reset and start counting when the WDTS register is written to. • When the WDTON bit is set to 0 (watchdog timer starts automatically after reset). The watchdog timer and prescaler start counting automatically after a reset.
Count stop condition	Stop mode, wait mode (Count resumes from the retained value after exiting.)
Operations at underflow	• When the PM12 bit in the PM1 register is set to 0. Watchdog timer interrupt • When the PM12 bit in the PM1 register is set to 1. Watchdog timer reset (refer to **5.5 Watchdog Timer Reset**)

Notes:
1. The watchdog timer is initialized when 00h and then FFh is written to the WDTR register. The prescaler is initialized after a reset. This may cause some errors due to the prescaler during the watchdog timer period.
2. The WDTON bit cannot be changed by a program. To set this bit, write 0 to bit 0 of address 0FFFFh with a flash programmer.
3. Write the WDTR register during the count operation of the watchdog timer.

14.3.3 Count Source Protection Mode Enabled

The count source for the watchdog timer is the low-speed on-chip oscillator clock for the watchdog timer when count source protection mode is enabled. If the CPU clock stops when a program is out of control, the clock can still be supplied to the watchdog timer.
Table 14.3 lists the Watchdog Timer Specifications (Count Source Protection Mode Enabled).

Table 14.3 Watchdog Timer Specifications (Count Source Protection Mode Enabled)

Item	Specification
Count source	Low-speed on-chip oscillator clock
Count operation	Decrement
Period	$\frac{\text{Count value of watchdog timer (m)}}{\text{Low-speed on-chip oscillator clock for the watchdog timer}}$ m: Value set by bits WDTUFS0 and WDTUFS1 in the OFS2 register Example: The period is approximately 8.2 ms when: - The on-chip oscillator clock for the watchdog timer is set to 125 kHz. - Bits WDTUFS1 to WDTUFS0 are set to 00b (03FFh).
Watchdog timer initialization conditions	• Reset • Write 00h and then FFh to the WDTR register. (3) • Underflow
Count start conditions	The operation of the watchdog timer after a reset is selected by the WDTON bit (1) in the OFS register (address 0FFFFh). • When the WDTON bit is set to 1 (watchdog timer is stopped after reset). The watchdog timer and prescaler are stopped after a reset and start counting when the WDTS register is written to. • When the WDTON bit is set to 0 (watchdog timer starts automatically after reset). The watchdog timer and prescaler start counting automatically after a reset.
Count stop condition	None (Count does not stop even in wait mode once it starts. The MCU does not enter stop mode.)
Operation at underflow	Watchdog timer reset (Refer to **5.5 Watchdog Timer Reset.**)
Registers, bits	• When the CSPPRO bit in the CSPR register is set to 1 (count source protection mode enabled) (2), the following are set automatically: - The low-speed on-chip oscillator for the watchdog timer is on. - The PM12 bit in the PM1 register is set to 1 (watchdog timer reset when the watchdog timer underflows).

Notes:
1. The WDTON bit cannot be changed by a program. To set this bit, write 0 to bit 0 of address 0FFFFh with a flash programmer.
2. Even if 0 is written to the CSPROINI bit in the OFS register, the CSPRO bit is set to 1. The CSPROINI bit cannot be changed by a program. To set this bit, write 0 to bit 7 of address 0FFFFh with a flash programmer.
3. Write the WDTR register during the count operation of the watchdog timer.

15. DTC

The DTC (data transfer controller) is a function that transfers data between the SFR and on-chip memory without using the CPU. This chip incorporates one DTC channel. The DTC is activated by a peripheral function interrupt to perform data transfers. The DTC and CPU use the same bus, and the DTC takes priority over the CPU in using the bus.
To control DTC data transfers, control data comprised of a transfer source address, a transfer destination address, and operating modes are allocated in the DTC control data area. Each time the DTC is activated, the DTC reads control data to perform data transfers.

15.1 Overview

Table 15.1 shows the DTC Specifications.

Table 15.1 DTC Specifications

Item		Specification
Activation sources		40 sources
Allocatable control data		24 sets
Address space which can be transferred		64 Kbytes (00000h to 0FFFFh)
Maximum number of transfer times	Normal mode	256 times
	Repeat mode	255 times
Maximum size of block to be transferred	Normal mode	256 bytes
	Repeat mode	255 bytes
Unit of transfers		Byte
Transfer mode	Normal mode	Transfers end on completion of the transfer causing the DTCCTj register value to change from 1 to 0.
	Repeat mode	On completion of the transfer causing the DTCCTj register value to change from 1 to 0, the repeat area address is initialized and the DTRLDj register value is reloaded to the DTCCTj register to continue transfers.
Address control	Normal mode	Fixed or incremented
	Repeat mode	Addresses of the area not selected as the repeat area are fixed or incremented.
Priority of activation sources		See **Table 15.5 DTC Activation Sources and DTC Vector Addresses**.
Interrupt request	Normal mode	When the data transfer causing the DTCCTj register value to change from 1 to 0 is performed, the activation source interrupt request is generated for the CPU, and interrupt handling is performed on completion of the data transfer.
	Repeat mode	When the data transfer causing the DTCCTj register value to change from 1 to 0 is performed while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled), the activation source interrupt request is generated for the CPU, and interrupt handling is performed on completion of the transfer.
Transfer start		When bits DTCENi0 to DTCENi7 in the DTCENi registers are 1 (activation enabled), data transfer is started each time the corresponding DTC activation sources are generated.
Transfer stop	Normal mode	• When bits DTCENi0 to DTCENi7 are set to 0 (activation disabled). • When the data transfer causing the DTCCTj register value to change from 1 to 0 is completed.
	Repeat mode	• When bits DTCENi0 to DTCENi7 are set to 0 (activation disabled). • When the data transfer causing the DTCCTj register value to change from 1 to 0 is completed while the RPTINT bit is 1 (interrupt generation enabled).

i = 0 to 6, j = 0 to 23

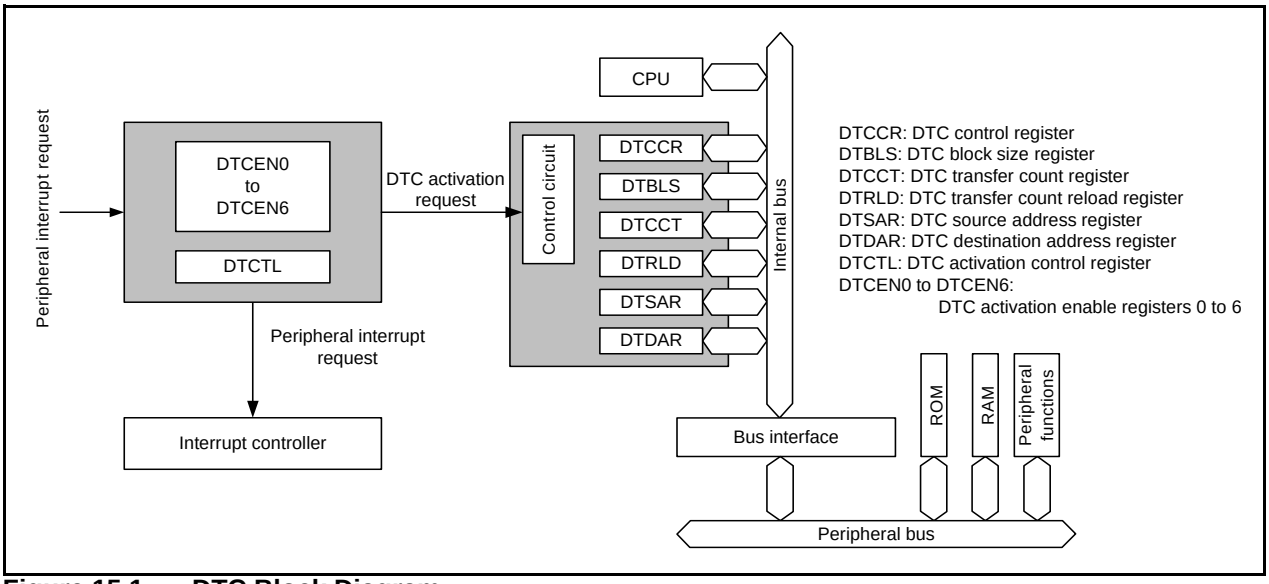


Figure 15.1 DTC Block Diagram

15.2 Registers

When the DTC is activated, control data (DTCCRj, DTBLSj, DTCCTj, DTRLDj, DTSARj, and DTDARj, j = 0 to 23) allocated in the control data area is read, and then transferred to the control registers (DTCCR, DTBLS, DTCCT, DTRLD, DTSAR, and DTDAR) in the DTC. On completion of the DTC data transfer, the contents of the DTC control registers are written back to the control data area.

Each DTCCR, DTBLS, DTCCT, DTRLD, DTSAR, and DTDAR register cannot be directly read or written to. DTCCRj, DTBLSj, DTCCTj, DTRLDj, DTSARj, and DTDARj are allocated as control data at addresses from 2C40h to 2CFFh in the DTC control data area, and can be directly accessed.
Also, registers DTCTL and DTCENi (i = 0 to 6) can be directly accessed.

15.2.1 DTC Control Register j (DTCCRj) (j = 0 to 23)

Address See **Table 15.4 Control Data Allocation Addresses**.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	RPTINT	CHNE	DAMOD	SAMOD	RPTSEL	MODE
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	MODE	Transfer mode select bit	0: Normal mode 1: Repeat mode	R/W
b1	RPTSEL	Repeat area select bit (1)	0: Transfer destination is the repeat area. 1: Transfer source is the repeat area.	R/W
b2	SAMOD	Source address control bit (2)	0: Fixed 1: Incremented	R/W
b3	DAMOD	Destination address control bit (2)	0: Fixed 1: Incremented	R/W
b4	CHNE	Chain transfer enable bit (3)	0: Chain transfers disabled 1: Chain transfers enabled	R/W
b5	RPTINT	Repeat mode interrupt enable bit (1)	0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b6	—	Reserved bits	Set to 0.	R/W
b7	—			

Notes:
1. This bit is valid when the MODE bit is 1 (repeat mode).
2. Settings of bits SAMOD and DAMOD are invalid for the repeat area.
3. Set the CHNE bit in the DTCCR23 register to 0 (chain transfers disabled).

15.2.2 DTC Block Size Register j (DTBLSj) (j = 0 to 23)

Address See **Table 15.4 Control Data Allocation Addresses**.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7 to b0	These bits specify the size of the data block to be transferred by one activation.	00h to FFh (1)	R/W

Note:
1. When the DTBLS register is set to 00h, the block size is 256 bytes.

15.2.3 DTC Transfer Count Register j (DTCCTj) (j = 0 to 23)

Address See **Table 15.4 Control Data Allocation Addresses**.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7 to b0	These bits specify the number of times of DTC data transfers.	00h to FFh (1)	R/W

Note:
1. When the DTCCT register is set to 00h, the number of transfer times is 256. Each time the DTC is activated, the DTCCT register is decremented by 1.

15.2.4 DTC Transfer Count Reload Register j (DTRLDj) (j = 0 to 23)

Address See **Table 15.4 Control Data Allocation Addresses**.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7 to b0	This register value is reloaded to the DTCCT register in repeat mode.	00h to FFh (1)	R/W

Note:
1. Set the initial value for the DTCCT register.

15.2.5 DTC Source Address Register j (DTSARj) (j = 0 to 23)

Address See **Table 15.4 Control Data Allocation Addresses**.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b15 to b0	These bits specify a transfer source address for data transfer.	0000h to FFFFh	R/W

15.2.6 DTC Destination Address Register j (DTDARj) (j = 0 to 23)

Address See **Table 15.4 Control Data Allocation Addresses**.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b15 to b0	These bits specify a transfer destination address for data transfer.	0000h to FFFFh	R/W

15.2.7 DTC Activation Enable Register i (DTCENi) (i = 0 to 6)

Address 0088h (DTCEN0), 0089h (DTCEN1), 008Ah (DTCEN2), 008Bh (DTCEN3), 008Ch (DTCEN4), 008Dh (DTCEN5), 008Eh (DTCEN6)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DTCENi7	DTCENi6	DTCENi5	DTCENi4	DTCENi3	DTCENi2	DTCENi1	DTCENi0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DTCENi0	DTC activation enable bit (1)	0: Activation disabled 1: Activation enabled	R/W
b1	DTCENi1			R/W
b2	DTCENi2			R/W
b3	DTCENi3			R/W
b4	DTCENi4			R/W
b5	DTCENi5			R/W
b6	DTCENi6			R/W
b7	DTCENi7			R/W

i = 0 to 6

Note:

1. For the operation of this bit, refer to **15.3.7 Interrupt Sources**.

The DTCENi registers enable/disable DTC activation by interrupt sources. Table 15.2 shows Correspondences between Bits DTCENi0 to DTCENi7 (i = 0 to 6) and Interrupt Sources.

Table 15.2 Correspondences between Bits DTCENi0 to DTCENi7 (i = 0 to 6) and Interrupt Sources

Register	DTCENi7 Bit	DTCENi6 Bit	DTCENi5 Bit	DTCENi4 Bit	DTCENi3 Bit	DTCENi2 Bit	DTCENi1 Bit	DTCENi0 Bit
DTCEN0	$\overline{\text{INT0}}$	$\overline{\text{INT1}}$	$\overline{\text{INT2}}$	$\overline{\text{INT3}}$	$\overline{\text{INT4}}$	—	—	—
DTCEN1	Key input	A/D conversion	UART0 reception	UART0 transmission	UART1 reception	UART1 transmission	UART2 reception	UART2 transmission
DTCEN2	SSU receive data full	SSU transmit data empty	Voltage monitor 2	Voltage monitor 1	—	—	Timer RC input-capture/ compare-match A	Timer RC input-capture/ compare-match B
DTCEN3	Timer RC input-capture/ compare-match C	Timer RC input-capture/ compare-match D	Timer RD0 input-capture/ compare-match A	Timer RD0 input-capture/ compare-match B	Timer RD0 input-capture/ compare-match C	Timer RD0 input-capture/ compare-match D	Timer RD1 input-capture/ compare-match A	Timer RD1 input-capture/ compare-match B
DTCEN4	Timer RD1 input-capture/ compare-match C	Timer RD1 input-capture/ compare-match D	—	—	—	—	—	—
DTCEN5	—	—	Timer RE	Timer RF	Timer RF compare-match 0	Timer RF compare-match 1	Timer RF capture	Timer RG input-capture/ compare-match A
DTCEN6	Timer RG input-capture/ compare-match B	Timer RA0	Timer RA1	Timer RB	Flash ready status	—	—	—

15.2.8 DTC Activation Control Register (DTCTL)

Address 0080h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	NMIF	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bit	Set to 0.	R/W
b1	NMIF	Non-maskable interrupt generation bit (1)	0: Non-maskable interrupts not generated 1: Non-maskable interrupts generated	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. This bit is set to 0 when the read result is 1 and 0 is written to the same bit. This bit remains unchanged even if the read result is 0 and 0 is written to the same bit. This bit remains unchanged if 1 is written to it.

The DTCTL register controls DTC activation when a non-maskable interrupt (an interrupt by the watchdog timer, oscillation stop detection, voltage monitor 1, or voltage monitor 2) is generated.

NMIF Bit (Non-Maskable Interrupt Generation Bit)

The NMIF bit is set to 1 when a watchdog timer interrupt, an oscillation stop detection interrupt, a voltage monitor 1 interrupt, or a voltage monitor 2 interrupt is generated.
When the NMIF bit is 1, the DTC is not activated even if the interrupt which enables DTC activation is generated. If the NMIF bit is changed to 1 during DTC transfer, the transfer is continued until it is completed.

When an interrupt source is the watchdog timer, wait for the following cycles before writing 0 to the NMIF bit:
If the WDTC7 bit in the WDTC register is set to 0 (divide-by-16 using the prescaler), wait for 16 cycles of the CPU clock after the interrupt source is generated.
If the WDTC7 bit is set to 1 (divide-by-128 using the prescaler), wait for 128 cycles of the CPU clock after the interrupt source is generated.
When an interrupt source is oscillation stop detection, set to the OCD1 bit in the OCD register to 0 (oscillation stop detection interrupt disabled) before writing 0 to the NMIF bit.

15.3 Function Description

15.3.1 Overview

When the DTC is activated, control data is read from the DTC control data area to perform data transfers and control data after data transfer is written back to the DTC control data area. Twenty-four sets of control data can be stored in the DTC control data area, which allows 24 types of data transfers to be performed.
There are two transfer modes: normal mode and repeat mode. When the CHNE bit in the DTCCRj (j = 0 to 23) register is set to 1 (chain transfers enabled), multiple control data is read and data transfers are continuously performed by one activation source (chain transfers).
A transfer source address is specified by the 16-bit register DTSARj, and a transfer destination address is specified by the 16-bit register DTDARj. The values in the registers DTSARj and DTDARj are separately fixed or incremented according to the control data on completion of the data transfer.

15.3.2 Activation Sources

The DTC is activated by an interrupt source. Figure 15.2 is a Block Diagram Showing Control of DTC Activation Sources.
The interrupt sources to activate the DTC are selected with the DTCENi (i = 0 to 6) registers.
The DTC sets 0 (activation disabled) to the corresponding bit among bits DTCENi0 to DTCENi7 in the DTCENi register during operation when the setting of data transfer (the first transfer in chain transfers) is either of the following:

- Transfer causing the DTCCTj (j = 0 to 23) register value to change to 0 in normal mode
- Transfer causing the DTCCTj register value to change to 0 while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled) in repeat mode

If the data transfer setting is not either of the above and the activation source is an interrupt source for timer RC, timer RD, timer RG, or the flash memory, the DTC sets 0 to the interrupt source flag corresponding to the activation source during operation.
Table 15.3 shows the DTC Activation Sources and Interrupt Source Flags for Setting to 0 during DTC Operation.
If multiple activation sources are simultaneously generated, the DTC activation will be performed according to the DTC activation source priority.
If multiple activation sources are simultaneously generated on completion of DTC operation, the next transfer will be performed according to the priority.
DTC activation is not affected by the I flag or interrupt control register, unlike with interrupt request operation. Therefore, even if interrupt requests cannot be acknowledged because interrupts are disabled, DTC activation requests can be acknowledged. The IR bit in the interrupt control register does not change even when an interrupt source to enable DTC activation is generated.

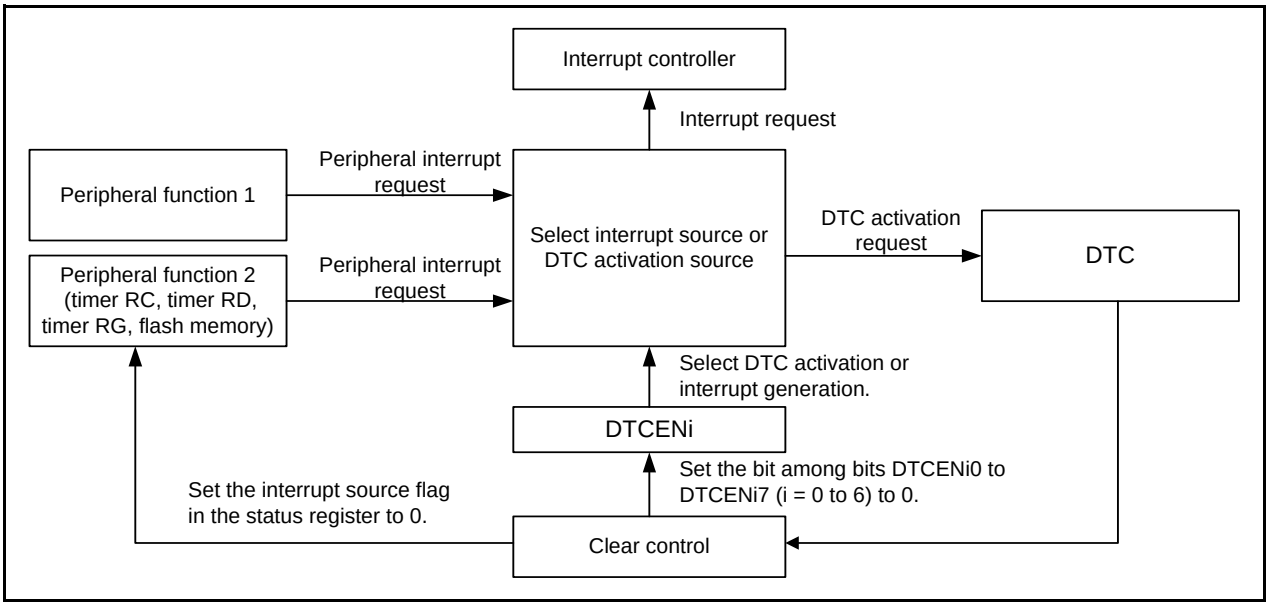


Figure 15.2 Block Diagram Showing Control of DTC Activation Sources

Table 15.3 DTC Activation Sources and Interrupt Source Flags for Setting to 0 during DTC Operation

DTC activation source generation	Interrupt Source Flag for Setting to 0
Timer RC input-capture/compare-match A	IMFA bit in TRCSR register
Timer RC input-capture/compare-match B	IMFB bit in TRCSR register
Timer RC input-capture/compare-match C	IMFC bit in TRCSR register
Timer RC input-capture/compare-match D	IMFD bit in TRCSR register
Timer RD0 input-capture/compare-match A	IMFA bit in TRDSR0 register
Timer RD0 input-capture/compare-match B	IMFB bit in TRDSR0 register
Timer RD0 input-capture/compare-match C	IMFC bit in TRDSR0 register
Timer RD0 input-capture/compare-match D	IMFD bit in TRDSR0 register
Timer RD1 input-capture/compare-match A	IMFA bit in TRDSR1 register
Timer RD1 input-capture/compare-match B	IMFB bit in TRDSR1 register
Timer RD1 input-capture/compare-match C	IMFC bit in TRDSR1 register
Timer RD1 input-capture/compare-match D	IMFD bit in TRDSR1 register
Timer RG input-capture/compare-match A	IMFA bit in TRGSR register
Timer RG input-capture/compare-match B	IMFB bit in TRGSR register
Flash ready status	RDYSTI bit in FST register

15.3.3 Control Data Allocation and DTC Vector Table

Control data is allocated in the order: Registers DTCCRj, DTBLSj, DTCCTj, DTRLDj, DTSARj, and DTDARj (j = 0 to 23). Table 15.4 shows the Control Data Allocation Addresses.

Table 15.4 Control Data Allocation Addresses

Register Symbol	Control Data No.	Address	DTCCRj Register	DTBLSj Register	DTCCTj Register	DTRLDj Register	DTSARj Register (Lower 8 Bits)	DTSARj Register (Higher 8 Bits)	DTDARj Register (Lower 8 Bits)	DTDARj Register (Higher 8 Bits)
DTCD0	Control Data 0	2C40h to 2C47h	2C40h	2C41h	2C42h	2C43h	2C44h	2C45h	2C46h	2C47h
DTCD1	Control Data 1	2C48h to 2C4Fh	2C48h	2C49h	2C4Ah	2C4Bh	2C4Ch	2C4Dh	2C4Eh	2C4Fh
DTCD2	Control Data 2	2C50h to 2C57h	2C50h	2C51h	2C52h	2C53h	2C54h	2C55h	2C56h	2C57h
DTCD3	Control Data 3	2C58h to 2C5Fh	2C58h	2C59h	2C5Ah	2C5Bh	2C5Ch	2C5Dh	2C5Eh	2C5Fh
DTCD4	Control Data 4	2C60h to 2C67h	2C60h	2C61h	2C62h	2C63h	2C64h	2C65h	2C66h	2C67h
DTCD5	Control Data 5	2C68h to 2C6Fh	2C68h	2C69h	2C6Ah	2C6Bh	2C6Ch	2C6Dh	2C6Eh	2C6Fh
DTCD6	Control Data 6	2C70h to 2C77h	2C70h	2C71h	2C72h	2C73h	2C74h	2C75h	2C76h	2C77h
DTCD7	Control Data 7	2C78h to 2C7Fh	2C78h	2C79h	2C7Ah	2C7Bh	2C7Ch	2C7Dh	2C7Eh	2C7Fh
DTCD8	Control Data 8	2C80h to 2C87h	2C80h	2C81h	2C82h	2C83h	2C84h	2C85h	2C86h	2C87h
DTCD9	Control Data 9	2C88h to 2C8Fh	2C88h	2C89h	2C8Ah	2C8Bh	2C8Ch	2C8Dh	2C8Eh	2C8Fh
DTCD10	Control Data 10	2C90h to 2C97h	2C90h	2C91h	2C92h	2C93h	2C94h	2C95h	2C96h	2C97h
DTCD11	Control Data 11	2C98h to 2C9Fh	2C98h	2C99h	2C9Ah	2C9Bh	2C9Ch	2C9Dh	2C9Eh	2C9Fh
DTCD12	Control Data 12	2CA0h to 2CA7h	2CA0h	2CA1h	2CA2h	2CA3h	2CA4h	2CA5h	2CA6h	2CA7h
DTCD13	Control Data 13	2CA8h to 2CAFh	2CA8h	2CA9h	2CAAh	2CABh	2CACh	2CADh	2CAEh	2CAFh
DTCD14	Control Data 14	2CB0h to 2CB7h	2CB0h	2CB1h	2CB2h	2CB3h	2CB4h	2CB5h	2CB6h	2CB7h
DTCD15	Control Data 15	2CB8h to 2CBFh	2CB8h	2CB9h	2CBAh	2CBBh	2CBCh	2CBDh	2CBEh	2CBFh
DTCD16	Control Data 16	2CC0h to 2CC7h	2CC0h	2CC1h	2CC2h	2CC3h	2CC4h	2CC5h	2CC6h	2CC7h
DTCD17	Control Data 17	2CC8h to 2CCFh	2CC8h	2CC9h	2CCAh	2CCBh	2CCCh	2CCDh	2CCEh	2CCFh
DTCD18	Control Data 18	2CD0h to 2CD7h	2CD0h	2CD1h	2CD2h	2CD3h	2CD4h	2CD5h	2CD6h	2CD7h
DTCD19	Control Data 19	2CD8h to 2CDFh	2CD8h	2CD9h	2CDAh	2CDBh	2CDCh	2CDDh	2CDEh	2CDFh
DTCD20	Control Data 20	2CE0h to 2CE7h	2CE0h	2CE1h	2CE2h	2CE3h	2CE4h	2CE5h	2CE6h	2CE7h
DTCD21	Control Data 21	2CE8h to 2CEFh	2CE8h	2CE9h	2CEAh	2CEBh	2CECh	2CEDh	2CEEh	2CEFh
DTCD22	Control Data 22	2CF0h to 2CF7h	2CF0h	2CF1h	2CF2h	2CF3h	2CF4h	2CF5h	2CF6h	2CF7h
DTCD23	Control Data 23	2CF8h to 2CFFh	2CF8h	2CF9h	2CFAh	2CFBh	2CFCh	2CFDh	2CFEh	2CFFh

j = 0 to 23

When the DTC is activated, one control data is selected according to the data read from the vector table which has been assigned to each activation source, and the selected control data is read from the DTC control data area.
Table 15.5 shows the DTC Activation Sources and DTC Vector Addresses. A one-byte vector table area is assigned to each activation source and one value from 00000000b to 00010111b (control data numbers in Table 15.4) is stored in each area to select one of the 24 control data sets.
Figures 15.3 to 15.7 show the DTC Internal Operation Flowchart.

Table 15.5 DTC Activation Sources and DTC Vector Addresses

Interrupt Request Source	Interrupt Name	Source No.	DTC Vector Address	Priority
External input	$\overline{\text{INT0}}$	0	2C00h	High
	$\overline{\text{INT1}}$	1	2C01h	
	$\overline{\text{INT2}}$	2	2C02h	
	$\overline{\text{INT3}}$	3	2C03h	
	$\overline{\text{INT4}}$	4	2C04h	
Key input	Key input	8	2C08h	
A/D	A/D conversion	9	2C09h	
UART0	UART0 reception	10	2C0Ah	
	UART0 transmission	11	2C0Bh	
UART1	UART1 reception	12	2C0Ch	
	UART1 transmission	13	2C0Dh	
UART2	UART2 reception	14	2C0Eh	
	UART2 transmission	15	2C0Fh	
SSU	Receive data full	16	2C10h	
	Transmit data empty	17	2C11h	
Voltage detection circuit	Voltage monitor 2	18	2C12h	
	Voltage monitor 1	19	2C13h	
Timer RC	Input-capture/compare-match A	22	2C16h	
	Input-capture/compare-match B	23	2C17h	
	Input-capture/compare-match C	24	2C18h	
	Input-capture/compare-match D	25	2C19h	
Timer RD0	Input-capture/compare-match A	26	2C1Ah	
	Input-capture/compare-match B	27	2C1Bh	
	Input-capture/compare-match C	28	2C1Ch	
	Input-capture/compare-match D	29	2C1Dh	
Timer RD1	Input-capture/compare-match A	30	2C1Eh	
	Input-capture/compare-match B	31	2C1Fh	
	Input-capture/compare-match C	32	2C20h	
	Input-capture/compare-match D	33	2C21h	
Timer RE	Timer RE	42	2C2Ah	
Timer RF	Timer RF	43	2C2Bh	
	Compare-match 0	44	2C2Ch	
	Compare-match 1	45	2C2Dh	
	Capture	46	2C2Eh	
Timer RG	Input-capture/compare-match A	47	2C2Fh	
	Input-capture/compare-match B	48	2C30h	
Timer RA0	Timer RA0	49	2C31h	
Timer RA1	Timer RA1	50	2C32h	
Timer RB	Timer RB	51	2C33h	
Flash memory	Flash ready status	52	2C34h	Low

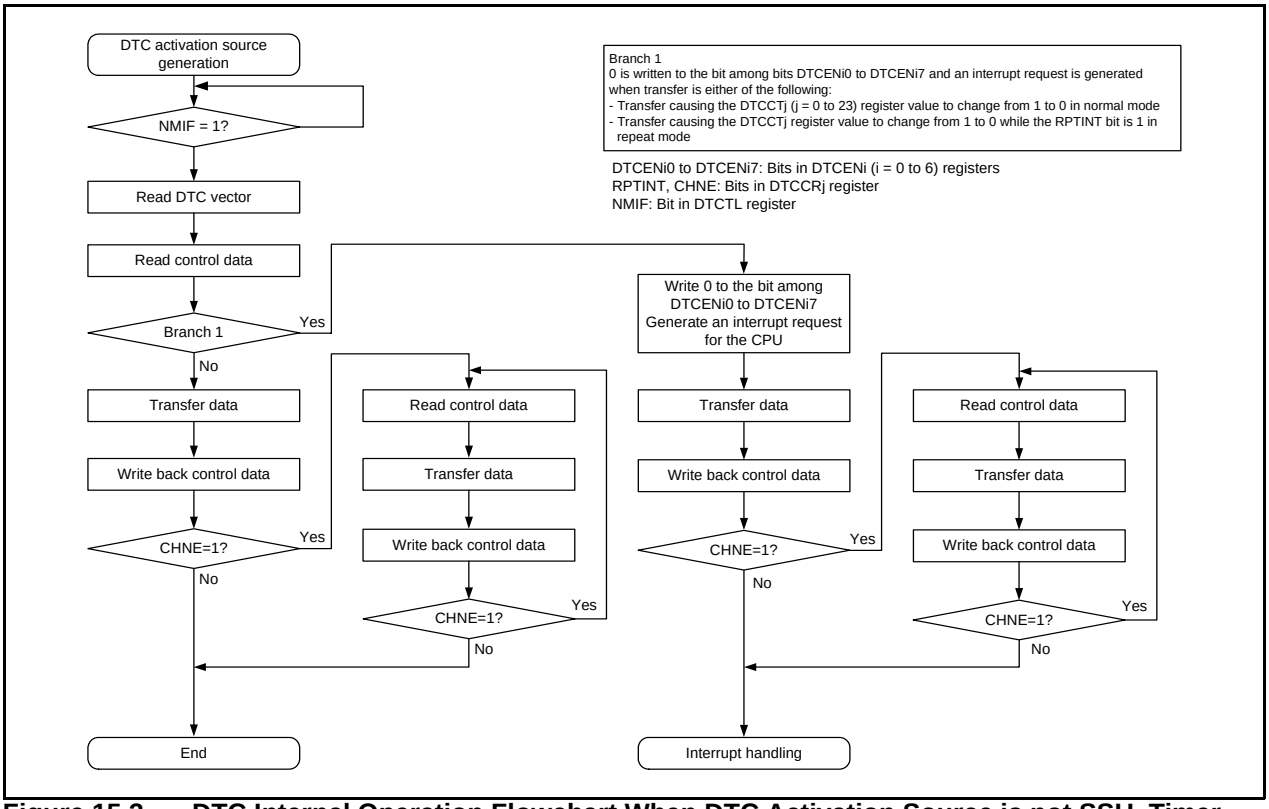


Figure 15.3 DTC Internal Operation Flowchart When DTC Activation Source is not SSU, Timer RC, Timer RD, Timer RG, or Flash Memory Interrupt Source

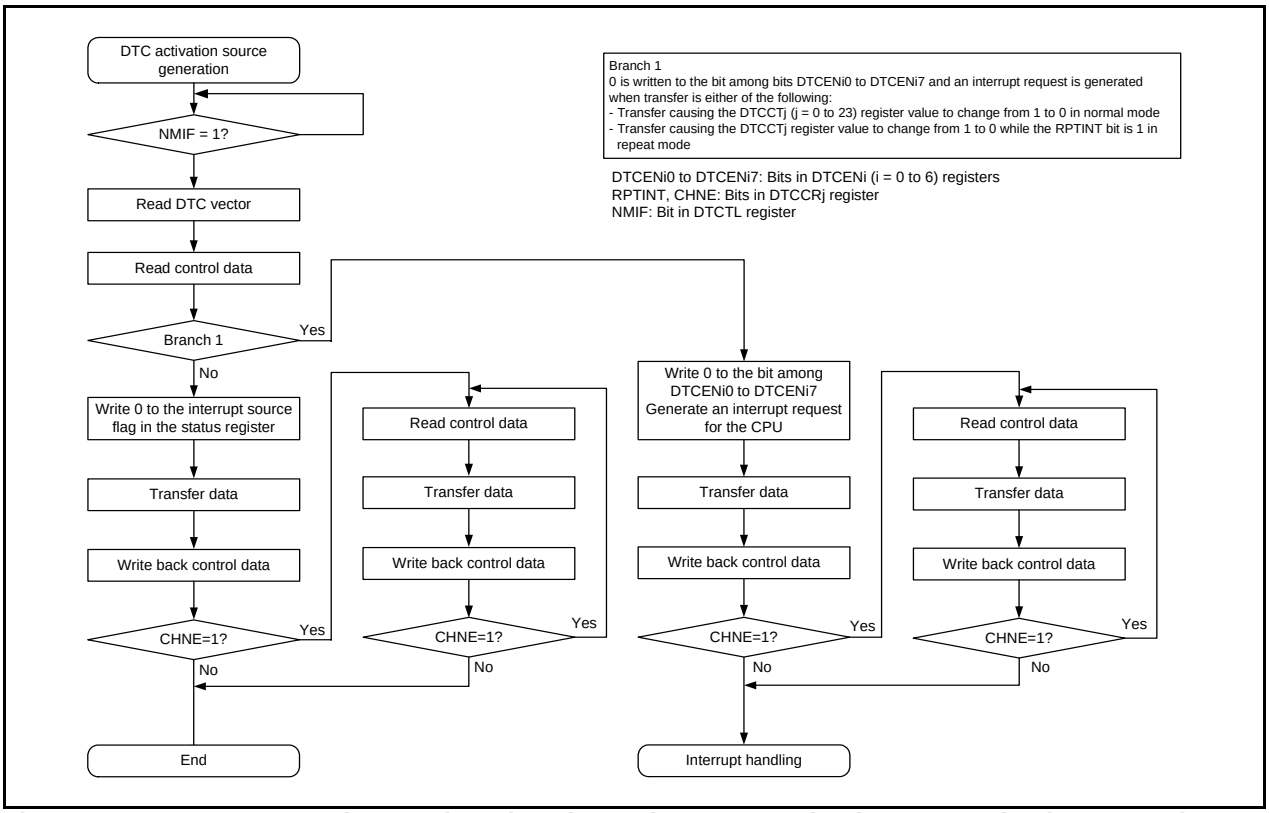
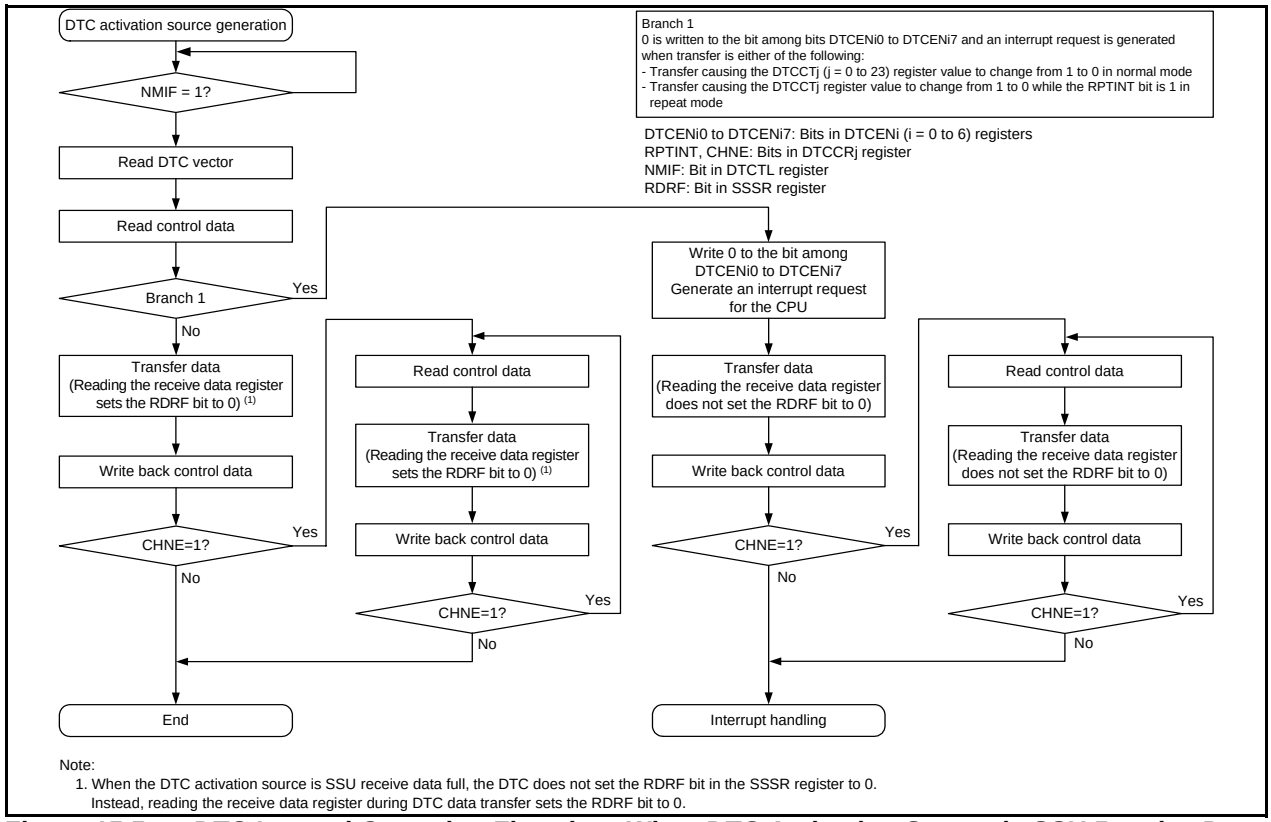
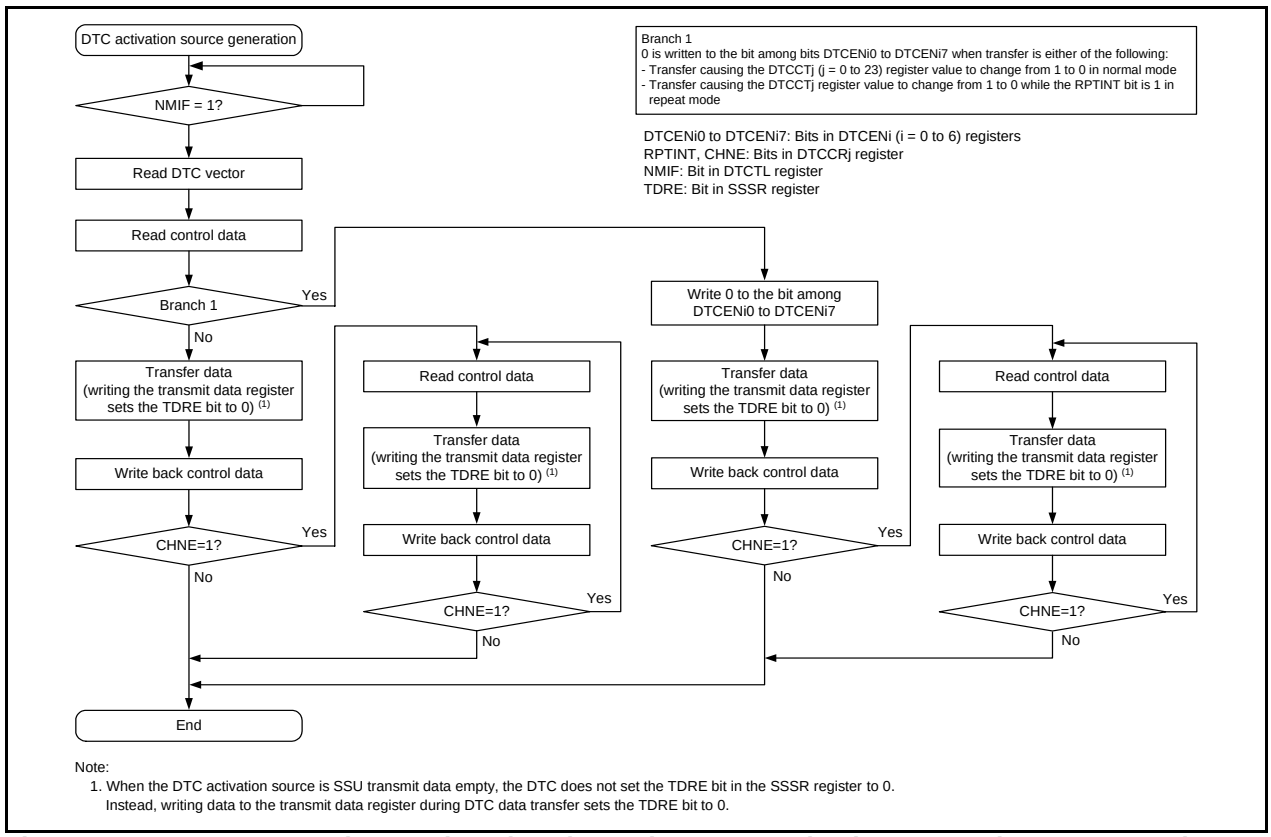


Figure 15.4 DTC Internal Operation Flowchart When DTC Activation Source is Timer RC, Timer RD, Timer RG, or Interrupt Source



Note:
1. When the DTC activation source is SSU receive data full, the DTC does not set the RDRF bit in the SSSR register to 0. Instead, reading the receive data register during DTC data transfer sets the RDRF bit to 0.

Figure 15.5 DTC Internal Operation Flowchart When DTC Activation Source is SSU Receive Data Full



Note:
1. When the DTC activation source is SSU transmit data empty, the DTC does not set the TDRE bit in the SSSR register to 0. Instead, writing data to the transmit data register during DTC data transfer sets the TDRE bit to 0.

Figure 15.6 DTC Internal Operation Flowchart When DTC Activation Source is SSU Transmit Data Empty

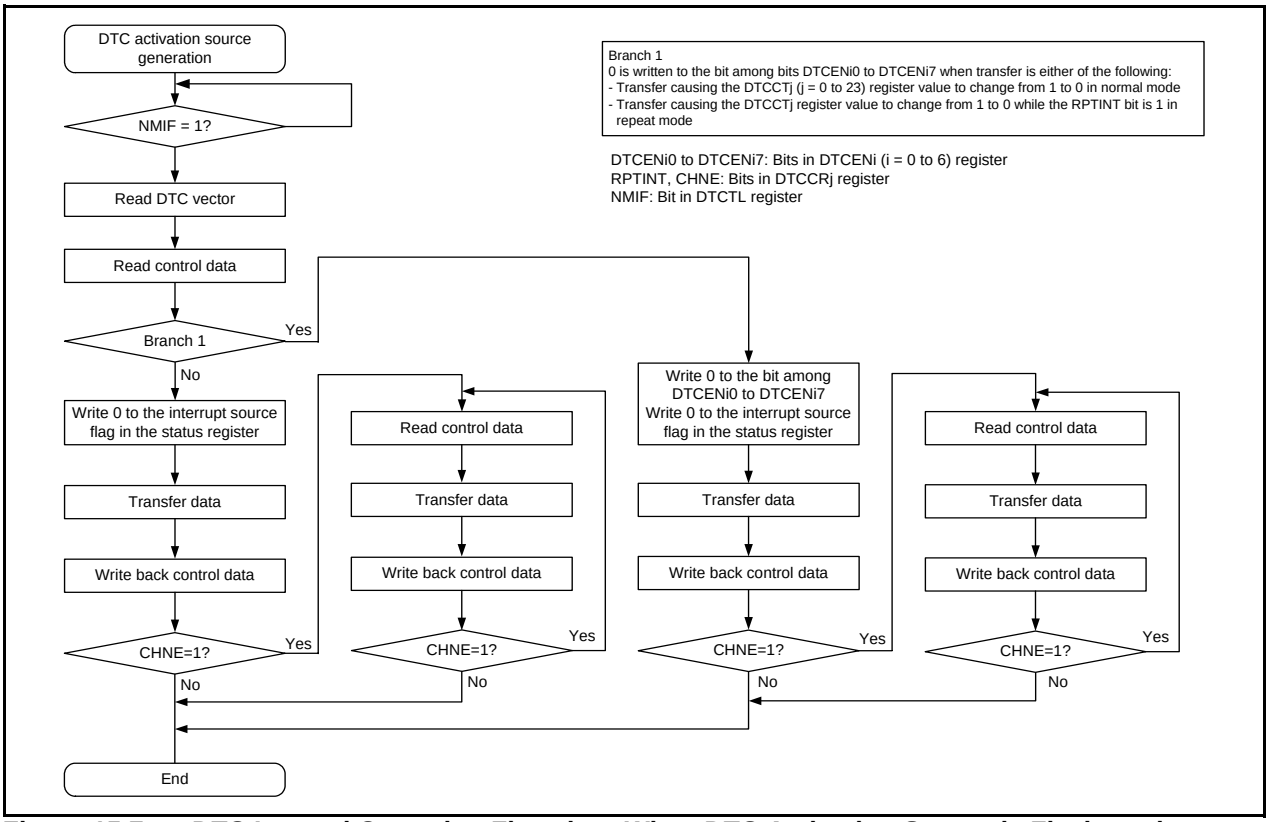


Figure 15.7 DTC Internal Operation Flowchart When DTC Activation Source is Flash ready status

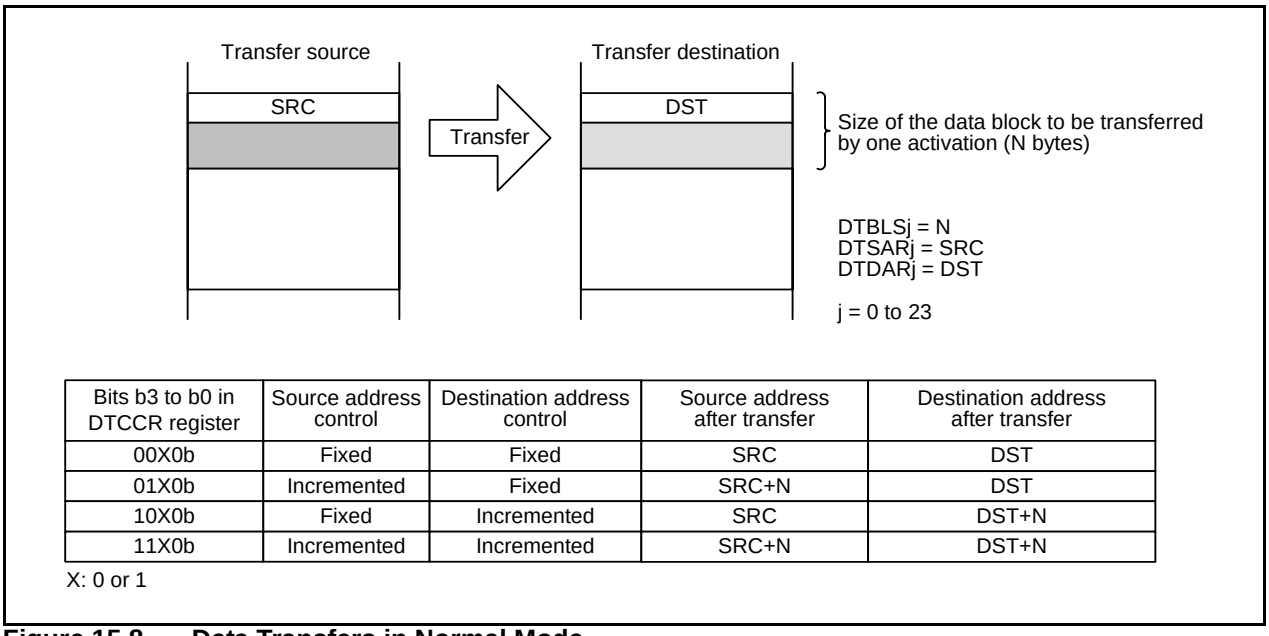
15.3.4 Normal Mode

One to 256 bytes of data are transferred by one activation. The number of transfer times can be 1 to 256. When the data transfer causing the DTCCTj (j = 0 to 23) register value to change to 0 is performed, an interrupt request for the CPU is generated during DTC operation.
Table 15.6 shows Register Functions in Normal Mode.
Figure 15.8 shows Data Transfers in Normal Mode.

Table 15.6 Register Functions in Normal Mode

Register	Symbol	Function
DTC block size register j	DTBLSj	Size of the data block to be transferred by one activation
DTC transfer count register j	DTCCTj	Number of times of data transfers
DTC transfer count reload register j	DTRLDj	Not used
DTC source address register j	DTSARj	Data transfer source address
DTC destination address register j	DTDARj	Data transfer destination address

j =0 to 23



Bits b3 to b0 in DTCCR register	Source address control	Destination address control	Source address after transfer	Destination address after transfer
00X0b	Fixed	Fixed	SRC	DST
01X0b	Incremented	Fixed	SRC+N	DST
10X0b	Fixed	Incremented	SRC	DST+N
11X0b	Incremented	Incremented	SRC+N	DST+N

X: 0 or 1

Figure 15.8 Data Transfers in Normal Mode

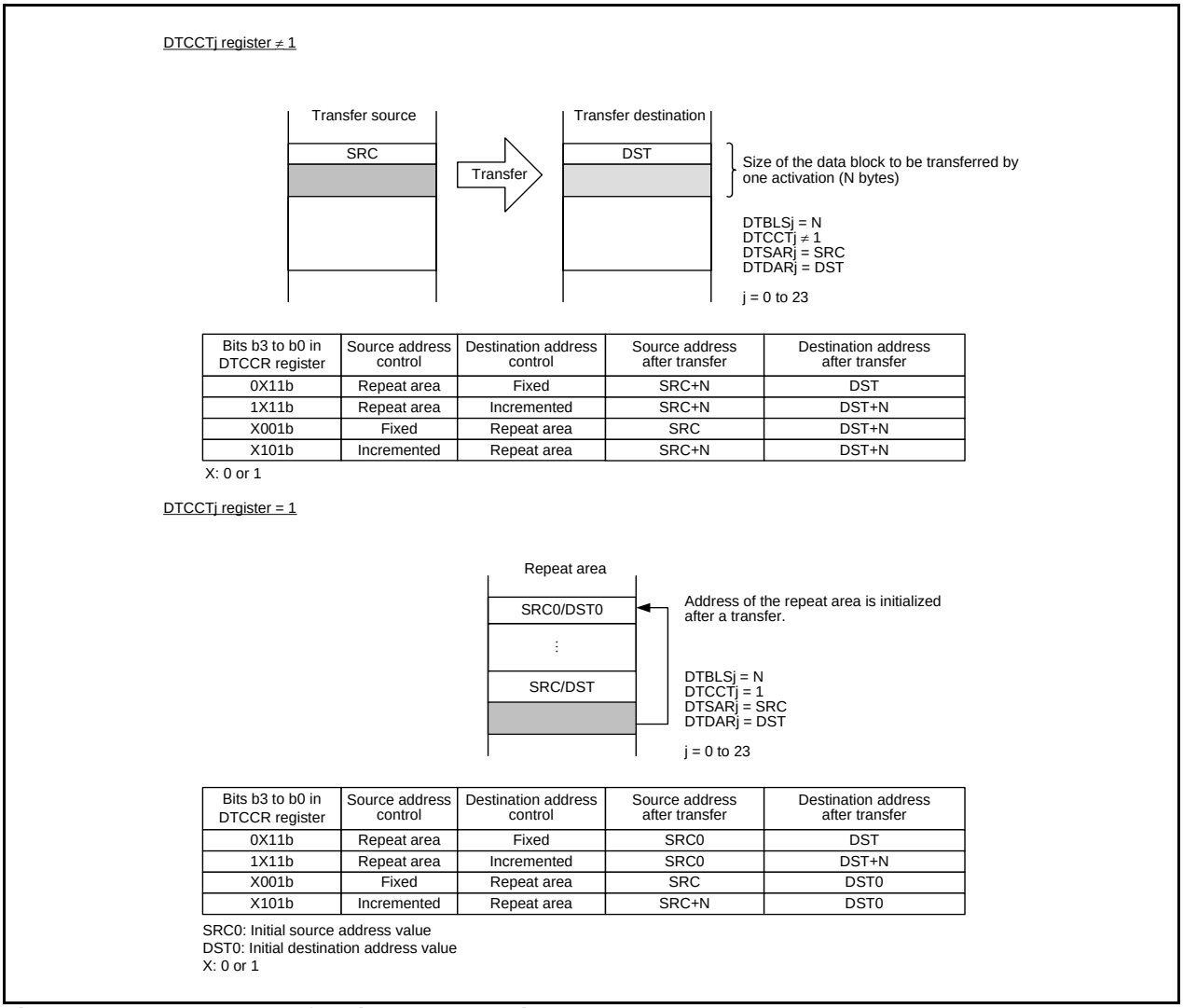
15.3.5 Repeat Mode

One to 255 bytes of data are transferred by one activation. Either of the transfer source or destination should be specified as the repeat area. The number of transfer times can be 1 to 255. On completion of the specified number of transfer times, the DTCCTj (i =0 to 23) register and the address specified for the repeat area are initialized to continue transfers. When the data transfer causing the DTCCTj register value to change to 0 is performed while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled), an interrupt request for the CPU is generated during DTC operation.
The lower 8 bits of the initial value for the repeat area address must be 00h. The size of data to be transferred must be set to 255 bytes or less before the specified number of transfer times is completed.
Table 15.7 shows Register Functions in Repeat Mode.
Figure 15.9 shows Data Transfers in Repeat Mode.

Table 15.7 Register Functions in Repeat Mode

Register	Symbol	Function
DTC block size register j	DTBLSj	Size of the data block to be transferred by one activation
DTC transfer count register j	DTCCTj	Number of times of data transfers
DTC transfer count reload register j	DTRLDj	This register value is reloaded to the DTCCT register. (Data transfer count is initialized.)
DTC source address register j	DTSARj	Data transfer source address
DTC destination address register j	DTDARj	Data transfer destination address

j =0 to 23



Bits b3 to b0 in DTCCR register	Source address control	Destination address control	Source address after transfer	Destination address after transfer
0X11b	Repeat area	Fixed	SRC+N	DST
1X11b	Repeat area	Incremented	SRC+N	DST+N
X001b	Fixed	Repeat area	SRC	DST+N
X101b	Incremented	Repeat area	SRC+N	DST+N

X: 0 or 1

Bits b3 to b0 in DTCCR register	Source address control	Destination address control	Source address after transfer	Destination address after transfer
0X11b	Repeat area	Fixed	SRC0	DST
1X11b	Repeat area	Incremented	SRC0	DST+N
X001b	Fixed	Repeat area	SRC	DST0
X101b	Incremented	Repeat area	SRC+N	DST0

SRC0: Initial source address value
DST0: Initial destination address value
X: 0 or 1

Figure 15.9 Data Transfers in Repeat Mode

15.3.6 Chain Transfers

When the CHNE bit in the DTCCRj (j = 0 to 22) register is 1 (chain transfers enabled), multiple data transfers can be continuously performed by one activation source. Figure 15.10 shows a Flow of Chain Transfers.
When the DTC is activated, one control data is selected according to the data read from the DTC vector address corresponding to the activation source, and the selected control data is read from the DTC control data area. When the CHNE bit for the control data is 1 (chain transfers enabled), the next control data immediately following the current control data is read and transferred after the current transfer is completed. This operation is repeated until the data transfer with the control data for which the CHNE bit is 0 (chain transfers disabled) is completed. Set the CHNE bit in the DTCCR23 register to “0” (chain transfers disabled).

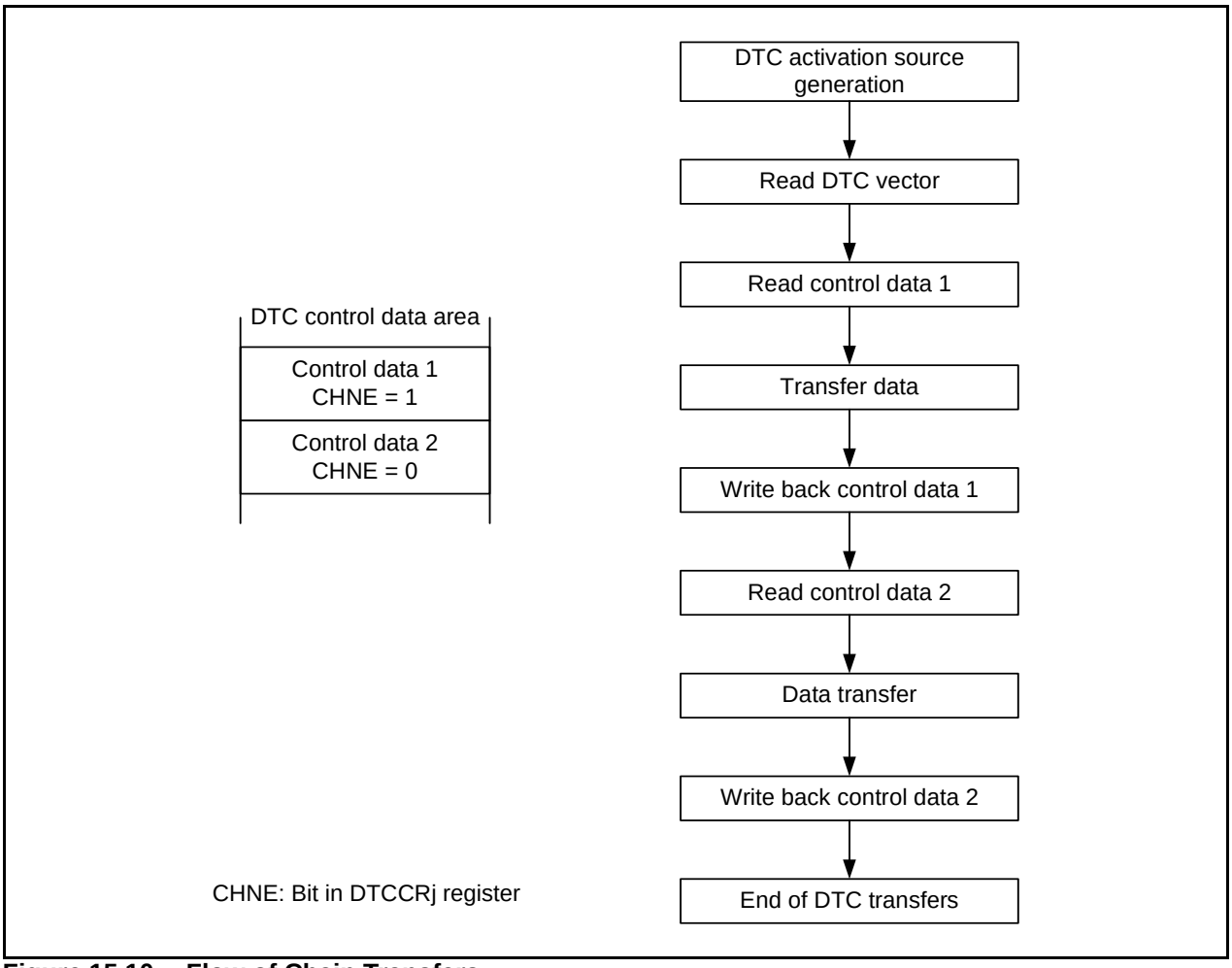


Figure 15.10 Flow of Chain Transfers

15.3.7 Interrupt Sources

When the data transfer causing the DTCCTj (j = 0 to 23) register value to change to 0 is performed in normal mode, and when the data transfer causing the DTCCTj register value to change to 0 is performed while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled) in repeat mode, the interrupt request corresponding to the activation source is generated for the CPU during DTC operation. However, no interrupt request is generated for the CPU when the activation source is SSU transmit data empty or flash ready status.
Interrupt requests for the CPU are affected by the I flag or interrupt control register. In chain transfers, whether the interrupt request is generated or not is determined either by the number of transfer times specified for the first type of the transfer or the RPTINT bit. When an interrupt request is generated for the CPU, the bit among bits DTCENi0 to DTCENi7 in the DTCENi (i = 0 to 6) registers corresponding to the activation source are set to 0 (activation disabled).

15.3.8 Operation Timings

The DTC requires five clock cycles to read control data allocated in the DTC control data area. The number of clock cycles required to write back control data differs depending on the control data settings.
Figure 15.11 shows an Example of DTC Operation Timings and Figure 15.12 shows an Example of DTC Operation Timings in Chain Transfers.
Table 15.8 shows the Specifications of Control Data Write-Back Operation.

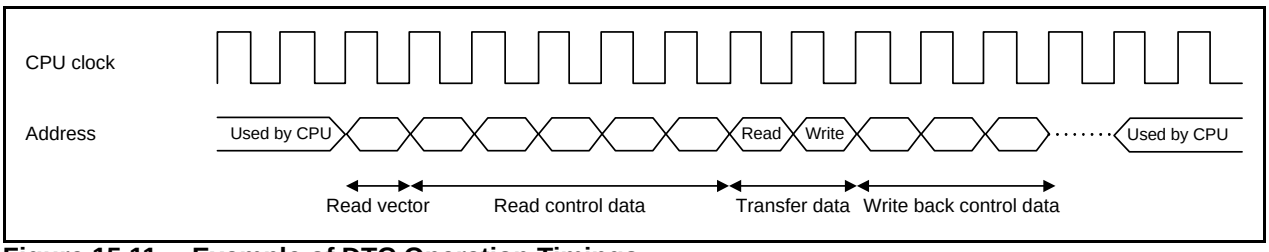


Figure 15.11 Example of DTC Operation Timings

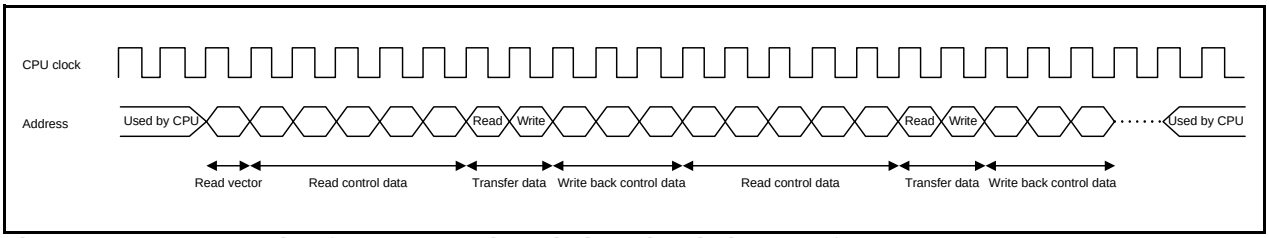


Figure 15.12 Example of DTC Operation Timings in Chain Transfers

Table 15.8 Specifications of Control Data Write-Back Operation

Bits b3 to b0 in DTCCR Register	Operating Mode	Address Control		Control Data to be Written Back				Number of Clock Cycles
		Source	Destination	DTCCTj Register	DTRLDj Register	DTSARj Register	DTDARj Register	
00X0b	Normal mode	Fixed	Fixed	Written back	Written back	Not written back	Not written back	1
01X0b		Incremented	Fixed	Written back	Written back	Written back	Not written back	2
10X0b		Fixed	Incremented	Written back	Written back	Not written back	Written back	2
11X0b		Incremented	Incremented	Written back	Written back	Written back	Written back	3
0X11b	Repeat mode	Repeat area	Fixed	Written back	Written back	Written back	Not written back	2
1X11b			Incremented	Written back	Written back	Written back	Written back	3
X001b		Fixed	Repeat area	Written back	Written back	Not written back	Written back	2
X101b		Incremented		Written back	Written back	Written back	Written back	3

j = 0 to 23
X: 0 or 1

The specifications for writing back control data in chained transfer operations depend on either normal mode or repeat mode as listed in Table 15.8 for each activation source, according to the operating mode set for each activation source.

15.3.9 Number of DTC Execution Cycles

Table 15.9 shows the Operations Following DTC Activation and Required Number of Cycles for each operation.
Table 15.10 shows the Number of Clock Cycles Required for Data Transfers.

Table 15.9 Operations Following DTC Activation and Required Number of Cycles

Vector Read	Control Data Read		Data Read	Data Write	Internal Operation
	Read	Write-back			
1	5	(Note 2)	(Note 1)	(Note 1)	1

Notes:
1. For the number of clock cycles required for data read/write, see **Table 15.10 Number of Clock Cycles Required for Data Transfers**.
2. For the number of clock cycles required for control data write-back, see **Table 15.8 Specifications of Control Data Write-Back Operation**.

Data is transferred as described below, when the DTBLSj (j = 0 to 23) register = N,
(1) When N = 2n (even), two-byte transfers are performed n times.
(2) When N = 2n + 1 (odd), two-byte transfers are performed n times followed by one time of one-byte transfer.

Table 15.10 Number of Clock Cycles Required for Data Transfers

Operation	Unit of Transfers	Internal RAM (During DTC Transfers)		Internal ROM (Program ROM)	Internal ROM (Data flash)	SFR (Word Access)		SFR (Byte Access)	SFR (DTC control data area)	
		Even Address	Odd Address			Even Address	Odd Address		Even Address	Odd Address
Data read	1-byte SK1	1		1	2	2		2	1	
	2-byte SK2	1	2	2	4	2	4	4	1	2
Data write	1-byte SL1	1		—	—	2		2	1	
	2-byte SL2	1	2	—	—	2	4	4	1	2

Note:
1. When the FMR23 bit in the FMR2 register is 1,
Four clock cycles to read one byte
Eight clock cycles to read two bytes

From Tables 15.9 and 15.10, the total number of required execution cycles can be obtained by the following formula:

Number of required execution cycles = 1 + Σ[formula A] + 2
Σ: Sum of the cycles for the number of transfer times performed by one activation source ([the number of transfer times for which CHNE is set to 1] + 1)

(1) For N = 2n (even)
Formula A = J + n • SK2 + n • SL2
(2) For N = 2n+1 (odd)
Formula A = J + n • SK2 + 1 • SK1 + n • SL2 + 1 • SL1
J: Number of cycles required to read control data (5 cycles) + number of cycles required to write back control data

To read data from or write data to the register that to be accessed in 16-bit units, set an even value of 2 or greater to the DTBLSj (j = 0 to 23) register.
The DTC performs accesses in 16-bit units.

15.3.10 DTC Activation Source Acknowledgement and Interrupt Source Flags

15.3.10.1 Interrupt Sources Except for Flash Memory, Timer RC, Timer RD, Timer RG, and Synchronous Serial Communication Unit (SSU)

When the DTC activation source is an interrupt source except for the flash memory, timer RC, timer RD, timer RG, or the synchronous serial communication unit, the same DTC activation source cannot be acknowledged for 8 to 12 cycles of the CPU clock after the interrupt source is generated. If an interrupt source is generated when a software command is executed, the same DTC activation source cannot be acknowledged for 9 to 16 cycles of the CPU clock. If a DTC activation source is generated during DTC operation and acknowledged, the same DTC activation source cannot be acknowledged for 8 to 12 cycles of the CPU clock on completion of the DTC transfer immediately before the DTC is activated by the source. When a software command is executed on completion of the DTC transfer immediately before the DTC is activated, the same DTC activation source cannot be acknowledged for 16 cycles of the CPU clock.

15.3.10.2 Flash Memory

When the DTC activation source is flash ready status, even if a flash ready status interrupt request is generated, it is not acknowledged as the DTC activation source after the RDYSTI bit in the FST register is set to 1 (flash ready status interrupt request) and before the DTC sets the RDYSTI bit to 0 (no flash ready status interrupt request). If a flash ready status interrupt request is generated after the DTC sets the RDYSTI bit to 0, the DTC acknowledges it as the activation source. 8 to 12 cycles of the CPU clock are required after the RDYSTI bit is set to 1 and before the DTC sets the interrupt request flag to 0. If a flash ready status interrupt is generated when a software command is executed, 9 to 16 cycles of the CPU clock are required before the DTC sets the interrupt source flag to 0. If a flash ready status interrupt request is generated during DTC operation and acknowledged as the DTC activation source, the RDYSTI bit is set to 0 after 8 to 12 cycles of the CPU clock on completion of the DTC transfer immediately before the DTC is activated by the source. When a software command is executed on completion of the DTC transfer immediately before the DTC is activated, the RDYSTI bit is set to 0 after 16 cycles of the CPU clock.

15.3.10.3 Timer RC, Timer RD, Timer RG

When the DTC activation source is an interrupt source for timer RC, timer RD, or timer RG, even if an input capture/compare match in individual timers occurs, it is not acknowledged as the DTC activation source after the interrupt source flag is set to 1 and before the DTC sets the flag to 0. If an input capture/compare match occurs after the DTC sets the interrupt source flag to 0, the DTC acknowledges it as the activation source. 8 to 12 cycles of the CPU clock plus 0.5 to 1.5 cycles of the timer operating clock are required after the interrupt source flag is set to 1 and before the DTC sets the flag to 0. If the interrupt request flag is set to 1 when a software command is executed, 9 to 16 cycles of the CPU clock plus 0.5 to 1.5 cycles of the timer operating clock are required before the DTC sets the interrupt source flag to 0. If a DTC activation source is generated from timer RC, timer RD, or timer RG during DTC operation and acknowledged, the interrupt source flag is set to 0 after 8 to 12 cycles of the CPU clock plus 0.5 to 1.5 cycles of the timer operating clock on completion of the DTC transfer immediately before the DTC is activated by the source. When a software command is executed on completion of the DTC transfer immediately before the DTC is activated, the interrupt source flag is set to 0 after 16 cycles of the CPU clock plus 0.5 to 1.5 cycles of the timer operating clock.

15.3.10.4 SSU Receive Data Full

When the DTC activation source is SSU receive data full, read the SSRDR register using a data transfer. The RDRF bit in the SSSR register is set to 0 (no data in SSRDR register) by reading the SSRDR register. If an interrupt source for receive data full is subsequently generated, the DTC acknowledges it as the activation source.

15.3.10.5 SSU Transmit Data Empty

When the DTC activation source is SSU transmit data empty, write to the SSTDR register using a data transfer. The TDRE bit in the SSSR register is set to 0 (data is not transferred from registers SSTDR to SSTRSR) by writing to the SSTDR register/the ICDRT register. If an interrupt source for transmit data empty is subsequently generated, the DTC acknowledges it as the activation source.

15.4 Notes on DTC

15.4.1 DTC activation source

- Do not generate any DTC activation sources before entering wait mode or during wait mode.
- Do not generate any DTC activation sources before entering stop mode or during stop mode.

15.4.2 DTCENi (i = 0 to 6) Registers

- Modify bits DTCENi0 to DTCENi7 only while an interrupt request corresponding to the register is not generated.
- When the interrupt source flag in the status register for the peripheral function is 1, do not modify the corresponding activation source bit among bits DTCENi0 to DTCENi7.
- Do not access the DTCENi registers using DTC transfers.

15.4.3 Peripheral Modules

- Do not set the status register bit for the peripheral function to 0 using a DTC transfer.
- When the DTC activation source is SSU receive data full, read the SSRDR register using a DTC transfer. The RDRF bit in the SSSR register is set to 0 (no data in SSRDR register) by reading the SSRDR register. However, the RDRF bit is not set to 0 by reading the SSRDR register when the DTC data transfer setting is either of the following:
  - Transfer causing the DTCCTj (j = 0 to 23) register value to change from 1 to 0 in normal mode
  - Transfer causing the DTCCRj register value to change from 1 to 0 while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled) in repeat mode.
- When the DTC activation source is SSU transmit data empty, write to the SSTDR register using a DTC transfer. The TDRE bit in the SSSR register is set to 0 (data is not transferred from registers SSTDR to SSTRSR) by writing to the SSTDR register.

15.4.4 Interrupt Request

- When the DTC activation source is either SSU transmit data empty or flash ready status, no interrupt request is generated for the CPU in either of the following cases:
  - When the DTC performs a data transfer that causes the DTCCTj register value to change to 0 in normal mode.
  - When the DTC performs a data transfer that causes the DTCCRj register value to change to 0 while the RPTINT bit in the DTCCRj register is 1 in repeat mode.

15.4.5 DTC Activation

- When the DTC is activated, operation may be shifted for one cycle before reading a vector.

15.4.6 Chain transfer

When performing chain transfers using several control data, the number of transfers set to the first control data is enabled and the number of transfers proceeded after the first control data is disabled.

Examples: When DTCCT0 = 5 and DTCCT1 = 10, chain transfers are performed as DTCCT0 = DTCCT1 = 5.
When DTCCT0 = 10 and DTCCT1 = 5, chain transfers are performed as DTCCT0 = DTCCT1 = 10.
When DTCCT0 = 10, DTCCT1 = 5, and DTCCT2 = 2, chain transfers are performed as DTCCT0 = DTCCT1 = DTCCT2 = 10.

16. General Overview of Timers

The MCU has three 8-bit timers with 8-bit prescalers, five 16-bit timers, and a timer with a 4-bit counter and an 8-bit counter. The three 8-bit timers with 8-bit prescalers are timer RA0, timer RA1, and timer RB. These timers contain a reload register to store the default value of the counter. The 16-bit timers are two timer RDs and three timers composed of timer RC, timer RF, and timer RG, and have input capture and output compare functions. The 4-bit and 8-bit counters are timer RE, and has an output compare function. All the timers operate independently.
Table 16.1 lists Functional Comparison of Timers.

Table 16.1 Functional Comparison of Timers

Item		Timer RA0	Timer RA1	Timer RB	Timer RC	Timer RD	Timer RE	Timer RF	Timer RG
Configuration		8-bit timer with 8-bit prescaler (with reload register)	8-bit timer with 8-bit prescaler (with reload register)	8-bit timer with 8-bit prescaler (with reload register)	16-bit timer (with input capture and output compare)	16-bit timer × 2 (with input capture and output compare)	4-bit counter 8-bit counter	16-bit timer (with input capture and output compare)	16-bit timer (with input capture and output compare)
Count		Decrement	Decrement	Decrement	Increment	Increment/Decrement	Increment	Increment	Increment/ Decrement
Count sources		• f1 • f2 • f8 • fOCO	• f1 • f2 • f8 • fOCO	• f1 • f2 • f8 • Timer RA underflow	• f1 • f2 • f4 • f8 • f32 • fOCO40M • fOCO-F • TRCCLK	• f1 • f2 • f4 • f8 • f32 • fOCO40M • fOCO-F • TRDCLK	• f4 • f8 • f32	• f1 • f8 • f32	• f1 • f2 • f4 • f8 • f32 • fOCO40M • TRGCLKA • TRGCLKB
Function	Count of the internal count source	Timer mode	Timer mode	Timer mode	Timer mode (output compare function)	Timer mode (output compare function)	—	Output compare mode	Timer mode (output compare function)
	Count of the external count source	Event counter mode	Event counter mode	—	Timer mode (output compare function)	Timer mode (output compare function)	—	—	Timer mode (output compare function), Phase counting mode
	External pulse width/period measurement	Pulse width measurement mode, pulse period measurement mode	Pulse width measurement mode, pulse period measurement mode	—	Timer mode (input capture function; 4 pins)	Timer mode (input compare function; 2 × 4 pins)	—	Input compare mode	Timer mode (Input capture function; 2 pins)
	PWM output	Pulse output mode (1), Event counter mode (1)	Pulse output mode (1), Event counter mode (1)	Programmable waveform generation mode	Timer mode (output compare function; 4 pins) (1), PWM mode (3 pins), PWM2 mode (1 pin)	Timer mode (output compare function; 2 × 4 pins) (1), PWM mode (2 × 3 pins), PWM3 mode (1 × 2 pins)	Output compare mode (1)	Output compare mode	Timer mode (output compare function; 2 pins), PWM mode (1 pin)
	One-shot waveform output	—	—	Programmable one-shot generation mode, Programmable wait one-shot generation mode	PWM mode (3 pins)	PWM mode (2 × 3 pins)	—	—	—
	Three-phase waveforms output	—	—	—	—	Reset synchronous PWM mode (2 × 3 pins, Sawtooth wave modulation), Complementary PWM mode (2 × 3 pins, triangular wave modulation, dead time)	—	—	—
Input pin		TRAIO0 INT2	TRAIO1 INT2	INT0	INT0, TRCCLK, TRCTRG, TRCIOA, TRCIOB, TRCIOC, TRCIOD	INT0, TRDCLK, TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1	—	TRFI	TRGCLKA, TRGCLKB, TRGIOA, TRGIOB
Output pin		TRAO0 TRAIO0	TRAO1 TRAIO1	TRBO	TRCIOA, TRCIOB, TRCIOC, TRCIOD	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1	TREO	TRFO00, TRFO01, TRFO02, TRFO10, TRFO11, TRFO12	TRGIOA, TRGIOB
Related interrupt		Timer RA0 interrupt INT2 interrupt	Timer RA1 interrupt INT2 interrupt	Timer RB interrupt, INT0 interrupt	Compare match/input capture A to D interrupt, Overflow interrupt, INT0 interrupt	Compare match/input capture A0 to D0 interrupt, Compare match/input capture A1 to D1 interrupt, Overflow interrupt, Underflow interrupt (2), INT0 interrupt	Timer RE interrupt	Compare 0 interrupt, Compare 1 interrupt, Capture interrupt, Timer RF interrupt	Compare match/ input capture A to B interrupt, Underflow interrupt (2), Overflow interrupt
Timer stop		Provided	Provided	Provided	Provided	Provided	Provided	Provided	Provided

Notes:
1. Rectangular waves are output in these modes. Since the waves are inverted at each overflow, the “H” and “L” level widths of the pulses are the same.
2. The underflow interrupt can be set to timer RD1 and timer RG.

17. Timer RA

Timer RA has two an 8-bit timers (timer RA0, timer RA1) with an 8-bit prescaler.

17.1 Overview

The prescaler and timer each consist of a reload register and counter. The reload register and counter are allocated at the same address, and can be accessed when accessing registers TRAiPRE and TRAi (i = 0 or 1) (refer to **Tables 17.2 to 17.6 the Specification of Each Modes**).
The count source for timer RAi (i = 0 or 1) is the operating clock that regulates the timing of timer operations such as counting and reloading.
Figure 17.1 shows a Timer RA Block Diagram. Table 17.1 lists the Pin Configuration of Timer RA.

Timer RA contains the following five operating modes:

- Timer mode: The timer counts the internal count source.
- Pulse output mode: The timer counts the internal count source and outputs pulses which invert the polarity by underflow of the timer.
- Event counter mode: The timer counts external pulses.
- Pulse width measurement mode: The timer measures the pulse width of an external pulse.
- Pulse period measurement mode: The timer measures the pulse period of an external pulse.

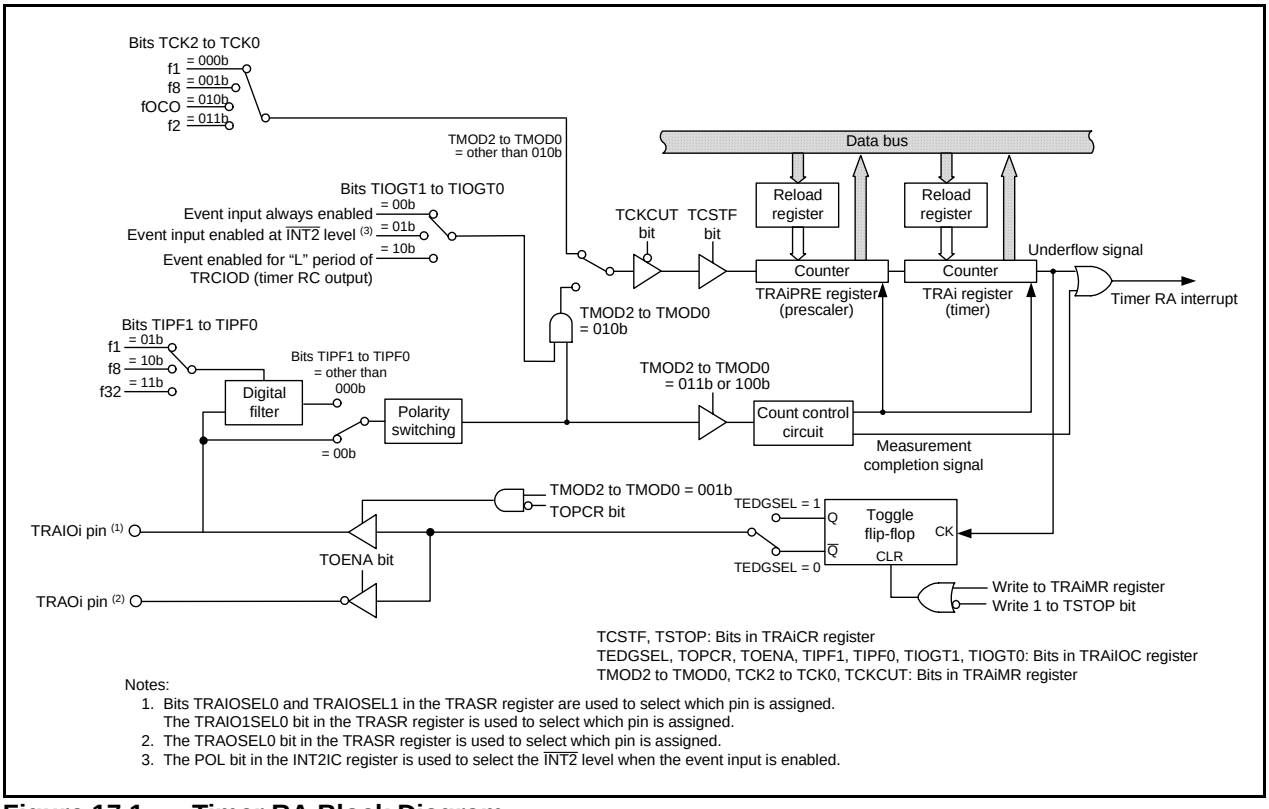


Figure 17.1 Timer RA Block Diagram

Table 17.1 Pin Configuration of Timer RA

Pin Name	Assigned Pin	I/O	Function
TRAIO0	P1_5, P1_7	I/O	Function differs according to the mode. Refer to descriptions of individual modes for details
TRAO0	P3_0, P3_7	Output	
TRAIO1	P6_4	I/O	
TRAO1	P6_3	Output	

17.2 Registers

17.2.1 Timer RAi Control Register (TRAiCR) (i = 0 or 1)

Address 0100h (TRA0CR), 0110h (TRA1CR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	TUNDF	TEDGF	—	TSTOP	TCSTF	TSTART
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RA count start bit (1)	0: Count stops 1: Count starts	R/W
b1	TCSTF	Timer RA count status flag (1)	0: Count stops 1: During count	R
b2	TSTOP	Timer RA count forcible stop bit (2)	When this bit is set to 1, the count is forcibly stopped. When read, its content is 0.	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TEDGF	Active edge judgment flag (3, 4)	0: Active edge not received 1: Active edge received (end of measurement period)	R/W
b5	TUNDF	Timer RA underflow flag (3, 4)	0: No underflow 1: Underflow	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

Notes:
1. Refer to **17.8 Notes on Timer RA** for precautions regarding bits TSTART and TCSTF.
2. When the TSTOP bit is set to 1, bits TSTART and TCSTF and registers TRAiPRE and TRAi are set to the values after a reset.
3. Bits TEDGF and TUNDF can be set to 0 by writing 0 to these bits by a program. However, their value remains unchanged when 1 is written.
4. Set to 0 in timer mode, pulse output mode, and event counter mode.

In pulse width measurement mode and pulse period measurement mode, use the MOV instruction to set the TRAiCR register. If it is necessary to avoid changing the values of bits TEDGF and TUNDF, write 1 to them.

17.2.2 Timer RAi I/O Control Register (TRAiIOC) (i = 0 or 1)

Address 0101h (TRA0IOC), 0111h (TRA1IOC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	TIOSEL	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIOi polarity switch bit	Function varies according to the operating mode.	R/W
b1	TOPCR	TRAIOi output control bit		R/W
b2	TOENA	TRAOi output enable bit		R/W
b3	TIOSEL	Hardware LIN function select bit		R/W
b4	TIPF0	TRAIOi input filter select bit		R/W
b5	TIPF1			R/W
b6	TIOGT0	TRAIOi event input control bit		R/W
b7	TIOGT1			R/W

17.2.3 Timer RAi Mode Register (TRAiMR) (i = 0 or 1)

Address 0102h (TRA0MR), 0112h (TRA1MR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCKCUT	TCK2	TCK1	TCK0	—	TMOD2	TMOD1	TMOD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TMOD0	Timer RA operating mode select bit	b2 b1 b0 0 0 0: Timer mode 0 0 1: Pulse output mode 0 1 0: Event counter mode 0 1 1: Pulse width measurement mode 1 0 0: Pulse period measurement mode 1 0 1: Do not set. 1 1 0: Do not set. 1 1 1: Do not set.	R/W
b1	TMOD1			R/W
b2	TMOD2			R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TCK0	Timer RA count source select bit	b6 b5 b4 0 0 0: f1 0 0 1: f8 0 1 0: fOCO 0 1 1: f2 1 0 0: Do not set. 1 0 1: Do not set. 1 1 0: Do not set. 1 1 1: Do not set.	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	TCKCUT	Timer RA count source cutoff bit	0: Provides count source 1: Cuts off count source	R/W

When both the TSTART and TCSTF bits in the TRAiCR register are set to 0 (count stops), rewrite this register.

17.2.4 Timer RAi Prescaler Register (TRAiPRE) (i = 0 or 1)

Address 0103h (TRA0PRE), 0113h (TRA1PRE)

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	—	—	—	—	—	—	
After Reset	1	1	1	1	1	1	1	1	(Note 1)

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Counts an internal count source	00h to FFh	R/W
	Pulse output mode		00h to FFh	R/W
	Event counter mode	Counts an external count source	00h to FFh	R/W
	Pulse width measurement mode	Measure pulse width of input pulses from external (counts internal count source)	00h to FFh	R/W
	Pulse period measurement mode	Measure pulse period of input pulses from external (counts internal count source)	00h to FFh	R/W

Note:
1. When the TSTOP bit in the TRAiCR register is set to 1, the TRAiPRE register is set to FFh.

17.2.5 Timer RAi Register (TRAi) (i = 0 or 1)

Address 0104h (TRA0), 0114h (TRA1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	—	—	—	—	—	—	
After Reset	1	1	1	1	1	1	1	1	(Note 1)

Bit	Mode	Function	Setting Range	R/W
b7 to b0	All modes	Counts on underflow of TRAiPRE register	00h to FFh	R/W

Note:
1. When the TSTOP bit in the TRAiCR register is set to 1, the TRAiPRE register is set to FFh.

17.2.6 Timer RA Pin Select Register (TRASR)

Address 0180h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	TRAIO1SEL0	—	TRAOSEL0	—	TRAIOSEL1	TRAIOSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRAIOSEL0	TRAIO0 pin select bit	b1 b0 0 0: TRAIO0 pin not used 0 1: P1_7 assigned 1 0: P1_5 assigned 1 1: Do not set.	R/W
b1	TRAIOSEL1			R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	TRAOSEL0	TRAO0 pin select bit	0: P3_7 assigned 1: P3_0 assigned	R/W
b4	—	Reserved bit	Set to 0.	R/W
b5	TRAIO1SEL0	TRAIO1 pin select bit	0: TRAIO1 pin not used 1: P6_4 assigned	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

The TRASR register selects which pin is assigned to the timer RA I/O. To use the I/O pin for timer RA, set this register.
Set the TRASR register before setting the timer RA associated registers. Also, do not change the setting value in this register during timer RA operation.

17.3 Timer Mode

In this mode, the timer counts an internally generated count source (refer to **Table 17.2 Timer Mode Specifications**).

Table 17.2 Timer Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO
Count operations	• Decrement • When the timer underflows, the contents of the reload register are reloaded and the count is continued.
Divide ratio	1/(n+1)(m+1) n: Value set in TRAiPRE register, m: Value set in TRAi register
Count start condition	1 (count starts) is written to the TSTART bit in the TRAiCR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRAiCR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRAiCR register.
Interrupt request generation timing	When timer RA underflows [timer RAi interrupt].
TRAIOi pin function	Programmable I/O port
TRAOi pin function	Programmable I/O port
Read from timer	The count value can be read by reading registers TRAi and TRAiPRE.
Write to timer	• When registers TRAiPRE and TRAi are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAiPRE and TRAi are written during the count, values are written to the reload register and counter (refer to **17.3.2 Timer Write Control during Count Operation**).

17.3.1 Timer RAi I/O Control Register (TRAiIOC) (i = 0 or 1) in Timer Mode

Address 0101h (TRA0IOC), 0111h (TRA1IOC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	TIOSEL	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIOi polarity switch bit	Set to 0 in timer mode.	R/W
b1	TOPCR	TRAIOi output control bit		R/W
b2	TOENA	TRAOi output enable bit		R/W
b3	TIOSEL	Hardware LIN function select bit	Set to 0. However, set to 1 when the hardware LIN function is used.	R/W
b4	TIPF0	TRAIOi input filter select bit	Set to 0 in timer mode.	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRAIOi event input control bit		R/W
b7	TIOGT1			R/W

17.3.2 Timer Write Control during Count Operation

Timer RA has a prescaler and a timer (which counts the prescaler underflows). The prescaler and timer each consist of a reload register and a counter. When writing to the prescaler or timer, values are written to both the reload register and counter.

However, values are transferred from the reload register to the counter of the prescaler in synchronization with the count source. In addition, values are transferred from the reload register to the counter of the timer in synchronization with prescaler underflows. Therefore, if the prescaler or timer is written to when count operation is in progress, the counter value is not updated immediately after the WRITE instruction is executed. Figure 17.2 shows an Operating Example of Timer RA when Counter Value is Rewritten during Count Operation.

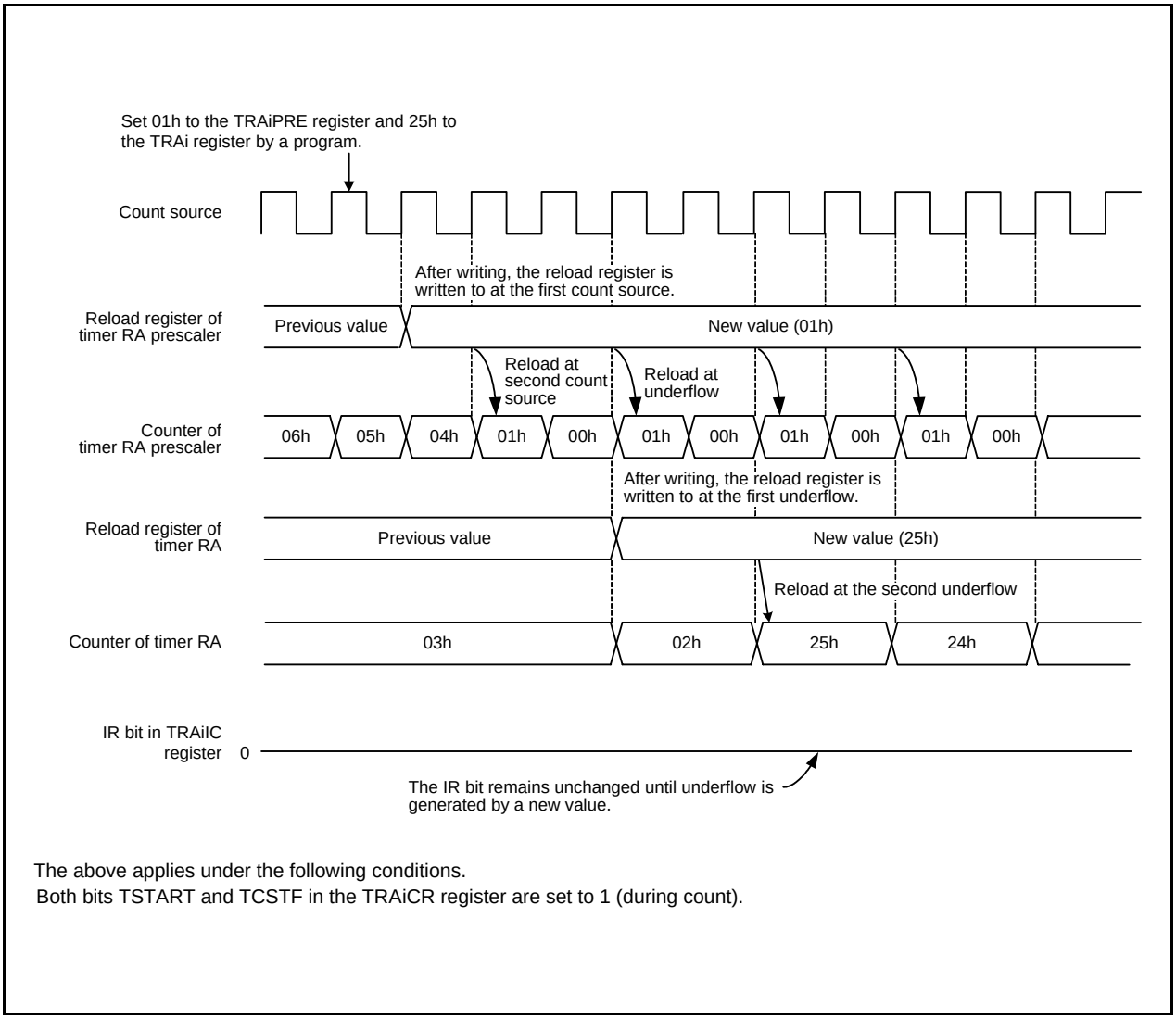


Figure 17.2 Operating Example of Timer RA when Counter Value is Rewritten during Count Operation

17.4 Pulse Output Mode

In pulse output mode, the internally generated count source is counted, and a pulse with inverted polarity is output from the TRAIOi pin each time the timer underflows (refer to **Table 17.3 Pulse Output Mode Specifications**).

Table 17.3 Pulse Output Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO
Count operations	• Decrement • When the timer underflows, the contents in the reload register is reloaded and the count is continued.
Divide ratio	1/(n+1)(m+1) n: Value set in TRAiPRE register, m: Value set in TRAi register
Count start condition	1 (count starts) is written to the TSTART bit in the TRAiCR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRAiCR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRAiCR register.
Interrupt request generation timing	When timer RA underflows [timer RAi interrupt].
TRAIOi pin function	Pulse output, programmable output port
TRAOi pin function	Programmable I/O port or inverted output of TRAIOi
Read from timer	The count value can be read by reading registers TRAi and TRAiPRE.
Write to timer	• When registers TRAiPRE and TRAi are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAiPRE and TRAi are written during the count, values are written to the reload register and counter (refer to **17.3.2 Timer Write Control during Count Operation**).
Selectable functions	• TRAIOi signal polarity switch function The level when the pulse output starts is selected by the TEDGSEL bit in the TRAiIOC register. (1) • TRAOi output function Pulses inverted from the TRAIOi output polarity can be output from the TRAOi pin (selectable by the TOENA bit in the TRAiIOC register). • Pulse output stop function Output from the TRAIOi pin is stopped by the TOPCR bit in the TRAiIOC register. • TRAIOi pin select function P1_5 or P1_7 is selected for the TRAIO0 pin by bits TRAIOSEL0 and TRAIOSEL1 in the TRASR register. P6_4 is selected for the TRAIO1 pin by the TRAIO1SEL0 bit in the TRASR register. • TRAO0 pin select function P3_0 or P3_7 is selected for theTRAO0 pin by the TRAOSEL0 bit in the TRASR register.

Note:
1. The level of the output pulse becomes the level when the pulse output starts when the TRAiMR register is written to.

17.4.1 Timer RAi I/O Control Register (TRAiIOC) (i = 0 or 1) in Pulse Output Mode

Address 0101h (TRA0IOC), 0111h (TRA1IOC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	TIOSEL	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIOi polarity switch bit	0: TRAIOi output starts at “H” 1: TRAIOi output starts at “L”	R/W
b1	TOPCR	TRAIOi output control bit (1)	0: TRAIOi output 1: TRAIOi output disabled	R/W
b2	TOENA	TRAOi output enable bit (2)	0: TRAIOi output disabled 1: TRAOi output (inverted TRAIOi output from P3_7 or P3_0)	R/W
b3	TIOSEL	Hardware LIN function select bit	Set to 0.	R/W
b4	TIPF0	TRAIOi input filter select bit	Set to 0 in pulse output mode.	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRAIOi event input control bit		R/W
b7	TIOGT1			R/W

Notes:
1. P1_5 or P1_7 is selected for the TRAIO0 pin by bits TRAIOSEL0 and TRAIOSEL1 in the TRASR register. P6_4 is selected for the TRAIO1 pin by the TRAIO1SEL0 bit in the TRASR register.
2. P3_0 or P3_7 is selected for theTRAO0 pin by the TRAOSEL0 bit in the TRASR register.

17.5 Event Counter Mode

In event counter mode, external signal inputs to the TRAIOi pin are counted (refer to **Table 17.4 Event Counter Mode Specifications**).

Table 17.4 Event Counter Mode Specifications

Item	Specification
Count source	External signal which is input to TRAIOi pin (active edge selectable by a program)
Count operations	• Decrement • When the timer underflows, the contents of the reload register are reloaded and the count is continued.
Divide ratio	1/(n+1)(m+1) n: setting value of TRAiPRE register, m: setting value of TRAi register
Count start condition	1 (count starts) is written to the TSTART bit in the TRAiCR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRAiCR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRAiCR register.
Interrupt request generation timing	When timer RA underflows [timer RAi interrupt].
TRAIOi pin function	Count source input
TRAOi pin function	Programmable I/O port or pulse output (1)
Read from timer	The count value can be read by reading registers TRAi and TRAiPRE.
Write to timer	• When registers TRAiPRE and TRAi are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAiPRE and TRAi are written during the count, values are written to the reload register and counter (refer to **17.3.2 Timer Write Control during Count Operation**).
Selectable functions	• TRAIOi input polarity switch function The active edge of the count source is selected by the TEDGSEL bit in the TRAiIOC register. • Count source input pin select function P1_5 or P1_7 is selected for the TRAIO0 pin by bits TRAIOSEL0 and TRAIOSEL1 in the TRASR register. P6_4 is selected for the TRAIO1 pin by the TRAIO1SEL0 bit in the TRASR register. • Pulse output function Pulses of inverted polarity can be output from the TRAOi pin each time the timer underflows (selectable by the TOENA bit in the TRAiIOC register). (1) • TRAOi pin select function P3_0 or P3_7 is selected for theTRAO0 pin by the TRAOSEL0 bit in the TRASR register. • Digital filter function Whether enabling or disabling the digital filter and the sampling frequency is selected by bits TIPF0 and TIPF1 in the TRAiIOC register. • Event input control function The enabled period for the event input to the TRAIOi pin is selected by bits TIOGT0 and TIOGT1 in the TRAiIOC register.

Note:

1. The level of the output pulse becomes the level when the pulse output starts when the TRAiMR register is written to.

17.5.1 Timer RAi I/O Control Register (TRAiIOC) (i = 0 or 1) in Event Counter Mode

Address 0101h (TRA0IOC), 0111h (TRA1IOC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	TIOSEL	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIOi polarity switch bit	0: Starts counting at rising edge of the TRAIOi input and TRAOi starts output at “L” 1: Starts counting at falling edge of the TRAIOi input and TRAOi starts output at “H”	R/W
b1	TOPCR	TRAIOi output control bit	Set to 0 in event counter mode.	R/W
b2	TOENA	TRAOi output enable bit (1)	0: TRAOi output disabled 1: TRAOi output	R/W
b3	TIOSEL	Hardware LIN function select bit	Set to 0.	R/W
b4	TIPF0	TRAIOi input filter select bit (2)	b5 b4 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRAIOi event input control bit	b7 b6 0 0: Event input always enabled 0 1: Event input enabled at $\overline{\text{INT2}}$ level (3) 1 0: Event enabled for “L” period of TRCIOD (timer RC output) 1 1: Do not set.	R/W
b7	TIOGT1			R/W

Notes:
1. P3_0 or P3_7 is selected for theTRAO0 pin by the TRAOSEL0 bit in the TRASR register.
2. When the same value from the TRAIOi pin is sampled three times continuously, the input is determined.
3. Make the following settings to use event input enabled at $\overline{\text{INT2}}$ level:
   - Set the $\overline{\text{INT2}}$EN bit in the INTEN register to 1 ($\overline{\text{INT2}}$ input enabled) and the INT2PL bit to 0 (one edge).
   - Set the $\overline{\text{INT2}}$ polarity by the POL bit in the INT2IC register.
     When the POL bit is set 0 (falling edge selected), the event input for the $\overline{\text{INT2}}$ high-level period is enabled.
     When the POL bit is set 1 (rising edge selected), the event input for the $\overline{\text{INT2}}$ low-level period is enabled.
   - Set the PD6_6 bit in the PD6 register to 0 (input mode).
   - Select the $\overline{\text{INT2}}$ digital filter by bits INT2F1 to INT2F0 in the INTF register.

   The IR bit in the INT2IC register is set to 1 (interrupt request) in accordance with the setting of the POL bit in the INT2IC register and the INT2PL bit in the INTEN register and a change in the $\overline{\text{INT2}}$ pin input (refer to **11.8 Notes on Interrupts**).
   For details on interrupts, refer to **11. Interrupts**.

17.6 Pulse Width Measurement Mode

In pulse width measurement mode, the pulse width of an external signal input to the TRAIOi pin is measured (refer to **Table 17.5 Pulse Width Measurement Mode Specifications**).
Figure 17.3 shows an Operating Example of Pulse Width Measurement Mode.

Table 17.5 Pulse Width Measurement Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO
Count operations	• Decrement • Continuously counts the selected signal only when measurement pulse is “H” level, or conversely only “L” level. • When the timer underflows, the contents of the reload register are reloaded and the count is continued.
Count start condition	1 (count starts) is written to the TSTART bit in the TRAiCR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRAiCR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRAiCR register.
Interrupt request generation timing	• When timer RAi underflows [timer RAi interrupt]. • Rising or falling of the TRAIOi input (end of measurement period) [timer RAi interrupt]
TRAIOi pin function	Measured pulse input
TRAOi pin function	Programmable I/O port
Read from timer	The count value can be read by reading registers TRAi and TRAiPRE.
Write to timer	• When registers TRAiPRE and TRAi are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAiPRE and TRAi are written during the count, values are written to the reload register and counter (refer to **17.3.2 Timer Write Control during Count Operation**).
Selectable functions	• Measurement level setting The “H” level or “L” level period is selected by the TEDGSEL bit in the TRAiIOC register. • Measured pulse input pin select function P1_5 or P1_7 is selected for the TRAIO0 pin by bits TRAIOSEL0 and TRAIOSEL1 in the TRASR register. P6_4 is selected for the TRAIO1 pin by the TRAIO1SEL0 bit in the TRASR register. • Digital filter function Whether enabling or disabling the digital filter and the sampling frequency is selected by bits TIPF0 and TIPF1 in the TRAiIOC register.

17.6.1 Timer RAi I/O Control Register (TRAiIOC) (i = 0 or 1) in Pulse Width Measurement Mode

Address 0101h (TRA0IOC), 0111h (TRA1IOC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	TIOSEL	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIOi polarity switch bit	0: TRAIOi input starts at “L” 1: TRAIOi input starts at “H”	R/W
b1	TOPCR	TRAIOi output control bit	Set to 0 in pulse width measurement mode.	R/W
b2	TOENA	TRAOi output enable bit		R/W
b3	TIOSEL	Hardware LIN function select bit	Set to 0. However, set to 1 when the hardware LIN function is used.	R/W
b4	TIPF0	TRAIOi input filter select bit (1)	b5 b4 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRAIOi event input control bit	Set to 0 in pulse width measurement mode.	R/W
b7	TIOGT1			R/W

Note:
1. When the same value from the TRAIOi pin is sampled three times continuously, the input is determined.

17.6.2 Operating Example

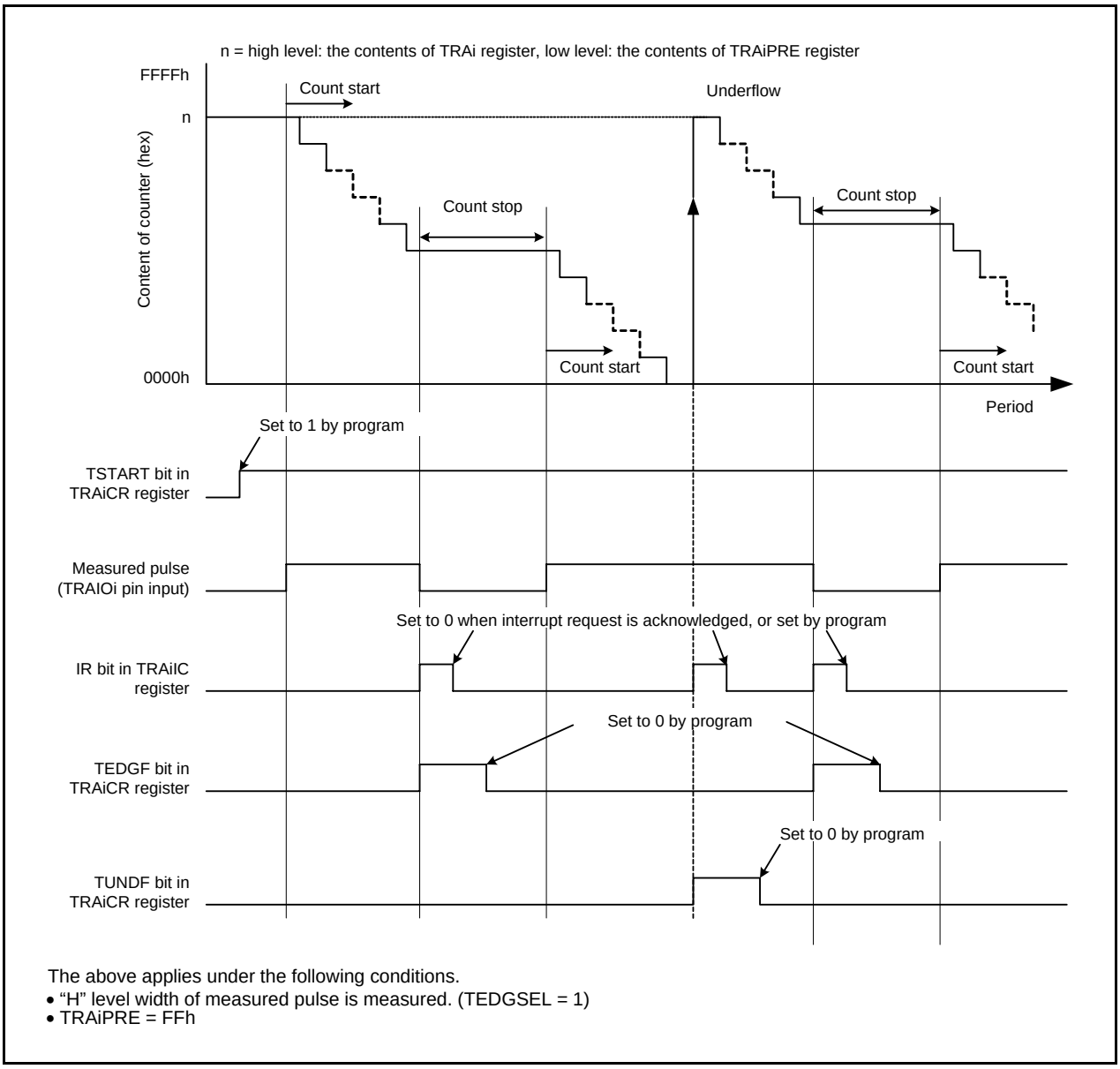


Figure 17.3 Operating Example of Pulse Width Measurement Mode

17.7 Pulse Period Measurement Mode

In pulse period measurement mode, the pulse period of an external signal input to the TRAIOi pin is measured (refer to **Table 17.6 Pulse Period Measurement Mode Specifications**).
Figure 17.4 shows an Operating Example of Pulse Period Measurement Mode.

Table 17.6 Pulse Period Measurement Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO
Count operations	• Decrement • After the active edge of the measured pulse is input, the contents of the read-out buffer are retained at the first underflow of timer RA prescaler. Then timer RA reloads the contents in the reload register at the second underflow of timer RA prescaler and continues counting.
Count start condition	1 (count starts) is written to the TSTART bit in the TRAiCR register.
Count stop conditions	• 0 (count stops) is written to TSTART bit in the TRAiCR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRAiCR register.
Interrupt request generation timing	• When timer RA underflows or reloads [timer RAi interrupt]. • Rising or falling of the TRAIOi input (end of measurement period) [timer RAi interrupt]
TRAIOi pin function	Measured pulse input (1)
TRAOi pin function	Programmable I/O port
Read from timer	The count value can be read by reading registers TRAi and TRAiPRE.
Write to timer	• When registers TRAiPRE and TRAi are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAiPRE and TRAi are written during the count, values are written to the reload register and counter (refer to **17.3.2 Timer Write Control during Count Operation**).
Selectable functions	• Measurement period selection The measurement period of the input pulse is selected by the TEDGSEL in the TRAiIOC register. • Measured pulse input pin select function P1_5 or P1_7 is selected for the TRAIO0 pin by bits TRAIOSEL0 and TRAIOSEL1 in the TRASR register. P6_4 is selected for the TRAIO1 pin by the TRAIO1SEL0 bit in the TRASR register. • Digital filter function Whether enabling or disabling the digital filter and the sampling frequency is selected by bits TIPF0 and TIPF1 in the TRAiIOC register.

Note:
1. Input a pulse with a period longer than twice the timer RA prescaler period. Input a pulse with a longer “H” and “L” width than the timer RA prescaler period. If a pulse with a shorter period is input to the TRAIOi pin, the input may be ignored.

17.7.1 Timer RAi I/O Control Register (TRAiIOC) (i = 0 or 1) in Pulse Period Measurement Mode

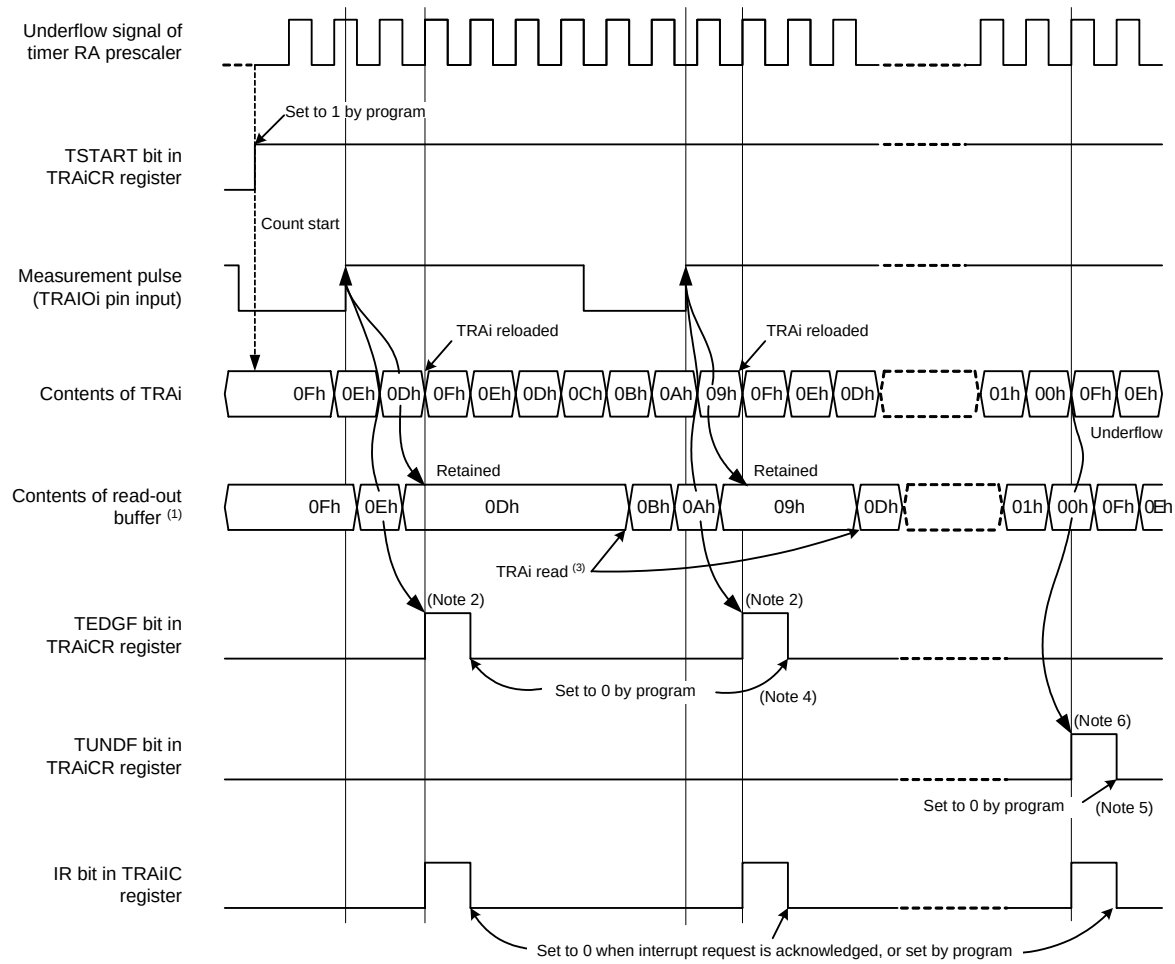
Address 0101h (TRA0IOC), 0111h (TRA1IOC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	TIOSEL	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIOi polarity switch bit	0: Measures measurement pulse from one rising edge to next rising edge 1: Measures measurement pulse from one falling edge to next falling edge	R/W
b1	TOPCR	TRAIOi output control bit	Set to 0 in pulse period measurement mode.	R/W
b2	TOENA	TRAOi output enable bit		R/W
b3	TIOSEL	Hardware LIN function select bit	Set to 0.	R/W
b4	TIPF0	TRAIOi input filter select bit (1)	b5 b4 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRAIOi event input control bit	Set to 0 in pulse period measurement mode.	R/W
b7	TIOGT1			R/W

Note:
1. When the same value from the TRAIOi pin is sampled three times continuously, the input is determined.

17.7.2 Operating Example



Conditions: The period from one rising edge to the next rising edge of the measured pulse is measured (TEDGSEL = 0) with the default value of the TRAi register as 0Fh.

Notes:
1. The contents of the read-out buffer can be read by reading the TRAi register in pulse period measurement mode.
2. After an active edge of the measured pulse is input, the TEDGF bit in the TRAiCR register is set to 1 (active edge received) when the timer RA prescaler underflows for the second time.
3. The TRAi register should be read before the next active edge is input after the TEDGF bit is set to 1 (active edge received). The contents in the read-out buffer are retained until the TRAi register is read. If the TRAi register is not read before the next active edge is input, the measured result of the previous period is retained.
4. To set to 0 by a program, use a MOV instruction to write 0 to the TEDGF bit in the TRAiCR register. At the same time, write 1 to the TUNDF bit in the TRACR register.
5. To set to 0 by a program, use a MOV instruction to write 0 to the TUNDF bit. At the same time, write 1 to the TEDGF bit.
6. Bits TUNDF and TEDGF are both set to 1 if timer RA underflows and reloads on an active edge simultaneously.

Figure 17.4 Operating Example of Pulse Period Measurement Mode

17.8 Notes on Timer RA

- Timer RA stops counting after a reset. Set the values in the timer RA and timer RA prescalers before the count starts.
- Even if the prescaler and timer RA are read out in 16-bit units, these registers are read 1 byte at a time by the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In pulse width measurement mode and pulse period measurement mode, bits TEDGF and TUNDF in the TRAiCR register can be set to 0 by writing 0 to these bits by a program. However, these bits remain unchanged if 1 is written. When using the READ-MODIFY-WRITE instruction for the TRAiCR register, the TEDGF or TUNDF bit may be set to 0 although these bits are set to 1 while the instruction is being executed. In this case, write 1 to the TEDGF or TUNDF bit which is not supposed to be set to 0 with the MOV instruction.
- When changing to pulse period measurement mode from another mode, the contents of bits TEDGF and TUNDF are undefined. Write 0 to bits TEDGF and TUNDF before the count starts.
- The TEDGF bit may be set to 1 by the first timer RA prescaler underflow generated after the count starts.
- When using the pulse period measurement mode, leave two or more periods of the timer RA prescaler immediately after the count starts, then set the TEDGF bit to 0.
- The TCSTF bit retains 0 (count stops) for 0 to 1 cycle of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.
  Do not write to the TRAiCR register until the TCSTF bit is set to 1. Also, do not access other registers associated with timer RA (1).
  Timer RA starts counting at the first valid edge of the count source after the TCSTF bit is set to 1 (during count).
  The TCSTF bit remains 1 for 0 to 1 cycle of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RA counting is stopped when the TCSTF bit is set to 0.
  Do not write to the TRAiCR register until the TCSTF bit is set to 0. Also, do not access other registers associated with timer RA (1).

  Note:
  1. Registers associated with timer RA: TRAiIOC, TRAiMR, TRAiPRE, and TRAi.

- When the TRAiPRE register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the count source clock for each write interval.
- When the TRAi register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the prescaler underflow for each write interval.
- Do not set 00h to the TRAi register in pulse width measurement mode and pulse period measurement mode.

18. Timer RB

Timer RB is an 8-bit timer with an 8-bit prescaler.

18.1 Overview

The prescaler and timer each consist of a reload register and counter (refer to **Tables 18.2 to 18.5 the Specifications of Each Mode**). Timer RB has timer RB primary and timer RB secondary as reload registers.
The count source for timer RB is the operating clock that regulates the timing of timer operations such as counting and reloading.
Figure 18.1 shows a Timer RB Block Diagram. Table 18.1 lists the Pin Configuration of Timer RB.

Timer RB has four operation modes listed as follows:

- Timer mode: The timer counts an internal count source (peripheral function clock or timer RA underflows).
- Programmable waveform generation mode: The timer outputs pulses of a given width successively.
- Programmable one-shot generation mode: The timer outputs a one-shot pulse.
- Programmable wait one-shot generation mode: The timer outputs a delayed one-shot pulse.

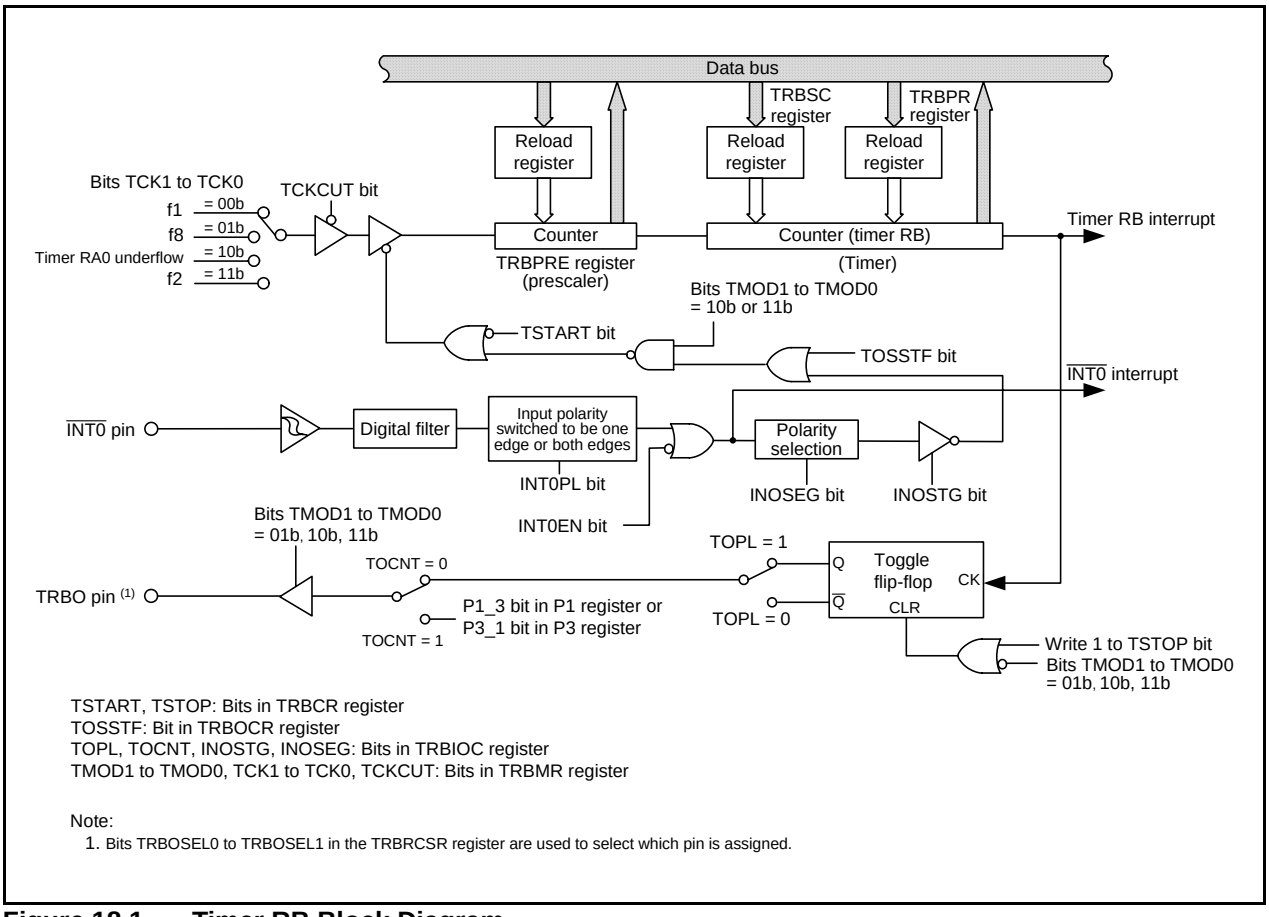


Figure 18.1 Timer RB Block Diagram

Table 18.1 Pin Configuration of Timer RB

Pin Name	Assigned Pin	I/O	Function
TRBO	P1_3 or P3_1	Output	Pulse output (programmable waveform generation mode, programmable one-shot generation mode, programmable wait one-shot generation mode)

18.2 Registers

18.2.1 Timer RB Control Register (TRBCR)

Address 0108h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	TSTOP	TCSTF	TSTART
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RB count start bit (1)	0: Count stops 1: Count starts	R/W
b1	TCSTF	Timer RB count status flag (1)	0: Count stops 1: During count (3)	R
b2	TSTOP	Timer RB count forcible stop bit (1, 2)	When this bit is set to 1, the count is forcibly stopped. When read, the content is 0.	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Notes:
1. Refer to **18.7 Notes on Timer RB** for precautions regarding bits TSTART, TCSTF and TSTOP.
2. When the TSTOP bit is set to 1, registers TRBPRE, TRBSC, TRBPR, and bits TSTART and TCSTF, and the TOSSTF bit in the TRBOCR register are set to values after a reset.
3. Indicates that count operation is in progress in timer mode or programmable waveform mode. In programmable one-shot generation mode or programmable wait one-shot generation mode, indicates that a one-shot pulse trigger has been acknowledged.

18.2.2 Timer RB One-Shot Control Register (TRBOCR)

Address 0109h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	TOSSTF	TOSSP	TOSST
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOSST	Timer RB one-shot start bit	When this bit is set to 1, one-shot trigger generated. When read, its content is 0.	R/W
b1	TOSSP	Timer RB one-shot stop bit	When this bit is set to 1, counting of one-shot pulses (including programmable wait one-shot pulses) stops. When read, the content is 0.	R/W
b2	TOSSTF	Timer RB one-shot status flag (1)	0: One-shot stopped 1: One-shot operating (Including wait period)	R
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. When 1 is set to the TSTOP bit in the TRBCR register, the TOSSTF bit is set to 0.

This register is enabled when bits TMOD1 to TMOD0 in the TRBMR register is set to 10b (programmable one-shot generation mode) or 11b (programmable wait one-shot generation mode).

18.2.3 Timer RB I/O Control Register (TRBIOC)

Address 010Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RB output level select bit	Function varies according to the operating mode.	R/W
b1	TOCNT	Timer RB output switch bit		R/W
b2	INOSTG	One-shot trigger control bit		R/W
b3	INOSEG	One-shot trigger polarity select bit		R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

18.2.4 Timer RB Mode Register (TRBMR)

Address 010Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCKCUT	—	TCK1	TCK0	TWRC	—	TMOD1	TMOD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TMOD0	Timer RB operating mode select bit (1)	b1 b0 0 0: Timer mode 0 1: Programmable waveform generation mode 1 0: Programmable one-shot generation mode 1 1: Programmable wait one-shot generation mode	R/W
b1	TMOD1			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	TWRC	Timer RB write control bit (2)	0: Write to reload register and counter 1: Write to reload register only	R/W
b4	TCK0	Timer RB count source select bit (1)	b5 b4 0 0: f1 0 1: f8 1 0: Timer RA0 underflow (3) 1 1: f2	R/W
b5	TCK1			R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	TCKCUT	Timer RB count source cutoff bit (1)	0: Provides count source 1: Cuts off count source	R/W

Notes:
1. Change bits TMOD1 and TMOD0; TCK1 and TCK0; and TCKCUT when both the TSTART and TCSTF bits in the TRBCR register set to 0 (count stops).
2. The TWRC bit can be set to either 0 or 1 in timer mode. In programmable waveform generation mode, programmable one-shot generation mode, or programmable wait one-shot generation mode, the TWRC bit must be set to 1 (write to reload register only).
3. To use the underflow signal of timer RA as the count source for timer RB, set timer RA in timer mode, pulse output mode, or event count mode.

18.2.5 Timer RB Prescaler Register (TRBPRE)

Address 010Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Counts an internal count source or timer RA0 underflows	00h to FFh	R/W
	Programmable waveform generation mode		00h to FFh	R/W
	Programmable one-shot generation mode		00h to FFh	R/W
	Programmable wait one-shot generation mode		00h to FFh	R/W

When the TSTOP bit in the TRBCR register is set to 1, the TRBPRE register is set to FFh.

18.2.6 Timer RB Secondary Register (TRBSC)

Address 010Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Disabled	00h to FFh	—
	Programmable waveform generation mode	Counts timer RB prescaler underflows (1)	00h to FFh	W (2)
	Programmable one-shot generation mode	Disabled	00h to FFh	—
	Programmable wait one-shot generation mode	Counts timer RB prescaler underflows (one-shot width is counted)	00h to FFh	W (2)

Notes:
1. The values of registers TRBPR and TRBSC are reloaded to the counter alternately and counted.
2. The count value can be read out by reading the TRBPR register even when the secondary period is being counted.

When the TSTOP bit in the TRBCR register is set to 1, the TRBSC register is set to FFh.
To write to the TRBSC register, perform the following steps.
(1) Write the value to the TRBSC register.
(2) Write the value to the TRBPR register. (If the value does not change, write the same value second time.)

18.2.7 Timer RB Primary Register (TRBPR)

Address 010Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Counts timer RB prescaler underflows	00h to FFh	R/W
	Programmable waveform generation mode	Counts timer RB prescaler underflows (1)	00h to FFh	R/W
	Programmable one-shot generation mode	Counts timer RB prescaler underflows (one-shot width is counted)	00h to FFh	R/W
	Programmable wait one-shot generation mode	Counts timer RB prescaler underflows (wait period width is counted)	00h to FFh	R/W

Note:
1. The values of registers TRBPR and TRBSC are reloaded to the counter alternately and counted.

When the TSTOP bit in the TRBCR register is set to 1, the TRBPR register is set to FFh.

18.2.8 Timer RB/RC Pin Select Register (TRBRCSR)

Address 0181h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	TRCCLKSEL2	TRCCLKSEL1	TRCCLKSEL0	—	—	TRBOSEL1	TRBOSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRBOSEL0	TRBO pin select bit	b1 b0 0 0: P1_3 assigned 0 1: P3_1 assigned 1 0: Do not set. 1 1: TRBO pin not used	R/W
b1	TRBOSEL1			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	TRCCLKSEL0	TRCCLK pin select bit	b6 b5 b4 0 0 0: TRCCLK pin not used 1 0 0: P5_0 assigned Other than above: Do not set.	R/W
b5	TRCCLKSEL1			R/W
b6	TRCCLKSEL2			R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

The TRBRCSR register selects which pin is assigned to the timer RB and timer RC I/O. To use the I/O pin for timer RB and timer RC, set this register.
Set bits TRBOSEL0 and TRBOSEL1 before setting the timer RB associated registers. Set bits TRCCLKSEL0 to TRCCLKSEL2 before setting the timer RC associated registers. Also, do not change the setting values of bits TRBOSEL0 and TRBOSEL1 during timer RB operation. Do not change the setting values of bits TRCCLKSEL0 to TRCCLKSEL2 during timer RC operation.

18.3 Timer Mode

In timer mode, a count source which is internally generated or timer RA0 underflows are counted (refer to **Table 18.2 Timer Mode Specifications**). Registers TRBOCR and TRBSC are not used in timer mode.

Table 18.2 Timer Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RA0 underflow
Count operations	• Decrement • When the timer underflows, it reloads the reload register contents before the count continues (when timer RB underflows, the contents of timer RB primary reload register is reloaded).
Divide ratio	1/(n+1)(m+1) n: setting value in TRBPRE register, m: setting value in TRBPR register
Count start condition	1 (count starts) is written to the TSTART bit in the TRBCR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRBCR register. • 1 (count forcibly stop) is written to the TSTOP bit in the TRBCR register.
Interrupt request generation timing	When timer RB underflows [timer RB interrupt].
TRBO pin function	Programmable I/O port
$\overline{\text{INT0}}$ pin function	Programmable I/O port or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read out by reading registers TRBPR and TRBPRE.
Write to timer	• When registers TRBPRE and TRBPR are written while the count is stopped, values are written to both the reload register and counter. • When registers TRBPRE and TRBPR are written to while count operation is in progress: If the TWRC bit in the TRBMR register is set to 0, the value is written to both the reload register and the counter. If the TWRC bit is set to 1, the value is written to the reload register only. (Refer to **18.3.2 Timer Write Control during Count Operation**.)

18.3.1 Timer RB I/O Control Register (TRBIOC) in Timer Mode

Address 010Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RB output level select bit	Set to 0 in timer mode.	R/W
b1	TOCNT	Timer RB output switch bit		R/W
b2	INOSTG	One-shot trigger control bit		R/W
b3	INOSEG	One-shot trigger polarity select bit		R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

18.3.2 Timer Write Control during Count Operation

Timer RB has a prescaler and a timer (which counts the prescaler underflows). The prescaler and timer each consist of a reload register and a counter. In timer mode, the TWRC bit in the TRBMR register can be used to select whether writing to the prescaler or timer during count operation is performed to both the reload register and counter or only to the reload register.

However, values are transferred from the reload register to the counter of the prescaler in synchronization with the count source. In addition, values are transferred from the reload register to the counter of the timer in synchronization with prescaler underflows. Therefore, even if the TWRC bit is set for writing to both the reload register and counter, the counter value is not updated immediately after the WRITE instruction is executed. In addition, if the TWRC bit is set for writing to the reload register only, the synchronization of the writing will be shifted if the prescaler value changes. Figure 18.2 shows an Operating Example of Timer RB when Counter Value is Rewritten during Count Operation.

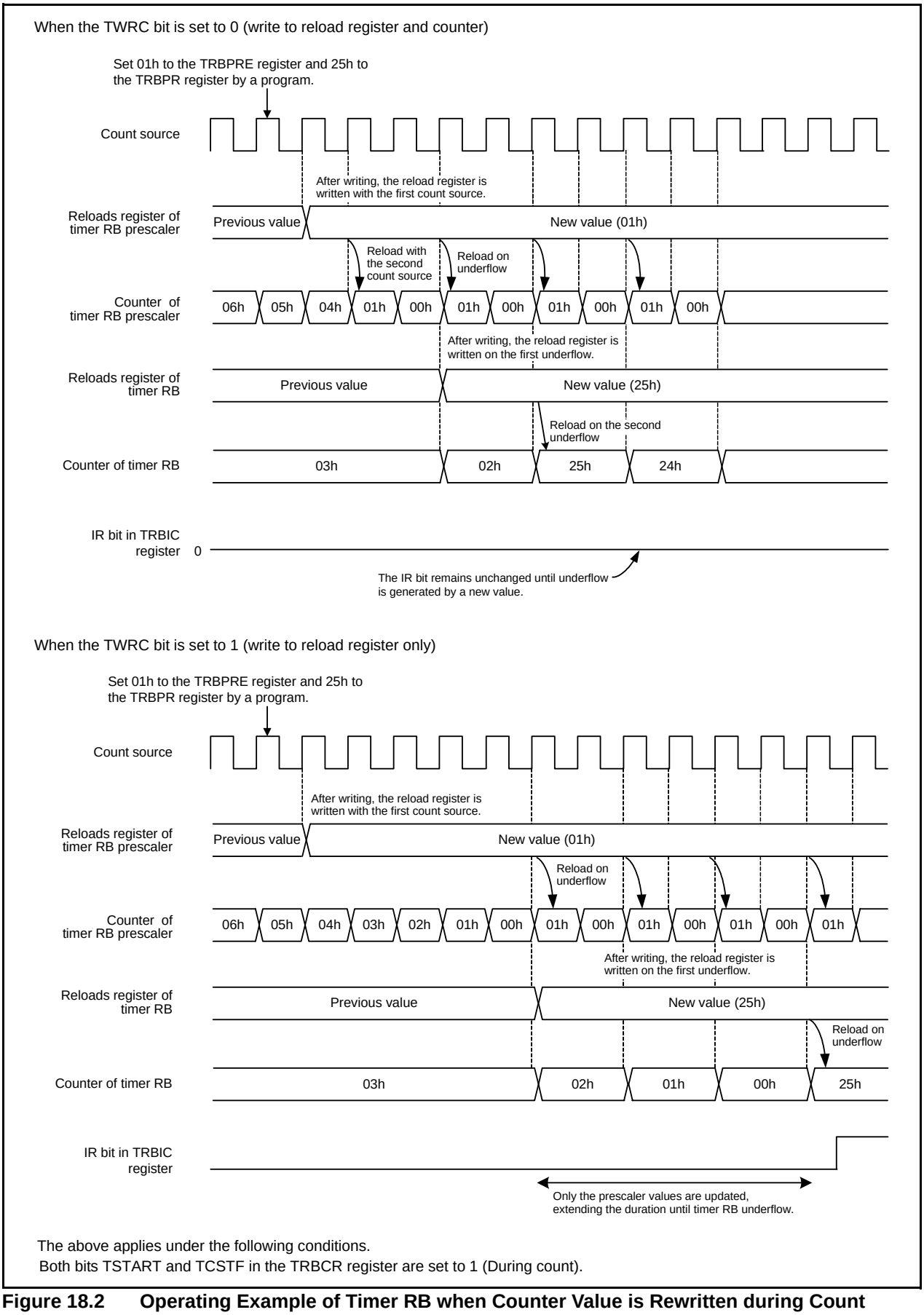


Figure 18.2 Operating Example of Timer RB when Counter Value is Rewritten during Count Operation

18.4 Programmable Waveform Generation Mode

In programmable waveform generation mode, the signal output from the TRBO pin is inverted each time the counter underflows, while the values in registers TRBPR and TRBSC are counted alternately (refer to Table 18.3 Programmable Waveform Generation Mode Specifications). Counting starts by counting the setting value in the TRBPR register. The TRBOCR register is unused in this mode.
Figure 18.3 shows an Operating Example of Timer RB in Programmable Waveform Generation Mode.

Table 18.3 Programmable Waveform Generation Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RA0 underflow
Count operations	• Decrement • When the timer underflows, it reloads the contents of the primary reload and secondary reload registers alternately before the count continues.
Width and period of output waveform	Primary period: (n+1)(m+1)/fi Secondary period: (n+1)(p+1)/fi Period: (n+1){(m+1)+(p+1)}/fi fi: Count source frequency n: Value set in TRBPRE register m: Value set in TRBPR register p: Value set in TRBSC register
Count start condition	1 (count start) is written to the TSTART bit in the TRBCR register.
Count stop conditions	• 0 (count stop) is written to the TSTART bit in the TRBCR register. • 1 (count forcibly stop) is written to the TSTOP bit in the TRBCR register.
Interrupt request generation timing	In half a cycle of the count source, after timer RB underflows during the secondary period (at the same time as the TRBO output change) [timer RB interrupt]
TRBO pin function	Programmable output port or pulse output
$\overline{\text{INT0}}$ pin function	Programmable I/O port or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read out by reading registers TRBPR and TRBPRE (1).
Write to timer	• When registers TRBPRE, TRBSC, and TRBPR are written while the count is stopped, values are written to both the reload register and counter. • When registers TRBPRE, TRBSC, and TRBPR are written to during count operation, values are written to the reload registers only. (2)
Selectable functions	• Output level select function The output level during primary and secondary periods is selected by the TOPL bit in the TRBIOC register. • TRBO pin output switch function Timer RB pulse output or P3_1 (P1_3) latch output is selected by the TOCNT bit in the TRBIOC register. (3)

Notes:
1. Even when counting the secondary period, the TRBPR register may be read.
2. The set values are reflected in the waveform output beginning with the following primary period after writing to the TRBPR register.
3. The value written to the TOCNT bit is enabled by the following.
   - When counting starts.
   - When a timer RB interrupt request is generated.
     The contents after the TOCNT bit is changed are reflected from the output of the following primary period.

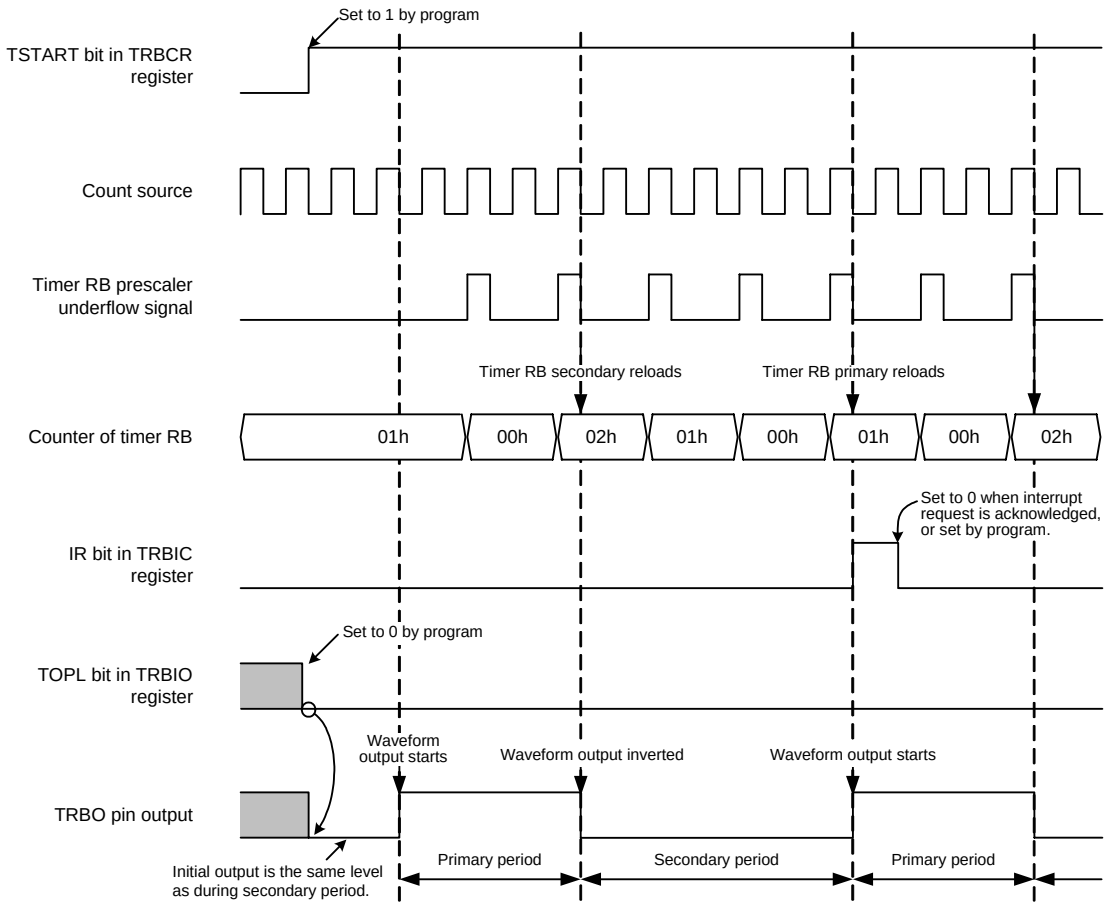
18.4.1 Timer RB I/O Control Register (TRBIOC) in Programmable Waveform Generation Mode

Address 010Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RB output level select bit	0: Outputs “H” for primary period Outputs “L” for secondary period Outputs “L” when the timer is stopped 1: Outputs “L” for primary period Outputs “H” for secondary period Outputs “H” when the timer is stopped	R/W
b1	TOCNT	Timer RB output switch bit	0: Outputs timer RB waveform 1: Outputs value in P3_1 (P1_3) port register	R/W
b2	INOSTG	One-shot trigger control bit	Set to 0 in programmable waveform generation mode.	R/W
b3	INOSEG	One-shot trigger polarity select bit		R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

18.4.2 Operating Example



The above applies under the following conditions.

TRBPRE = 01h, TRBPR = 01h, TRBSC = 02h
TRBIOC register TOCNT = 0 (timer RB waveform is output from the TRBO pin)

Figure 18.3 Operating Example of Timer RB in Programmable Waveform Generation Mode

18.5 Programmable One-shot Generation Mode

In programmable one-shot generation mode, a one-shot pulse is output from the TRBO pin by a program or an external trigger input (input to the $\overline{\text{INT0}}$ pin) (refer to Table 18.4 Programmable One-Shot Generation Mode Specifications). When a trigger is generated, the timer starts operating from the point only once for a given period equal to the set value in the TRBPR register. The TRBSC register is not used in this mode.
Figure 18.4 shows an Operating Example of Programmable One-Shot Generation Mode.

Table 18.4 Programmable One-Shot Generation Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RA0 underflow
Count operations	• Decrement the setting value in the TRBPR register • When the timer underflows, it reloads the contents of the reload register before the count completes and the TOSSTF bit is set to 0 (one-shot stops). • When the count stops, the timer reloads the contents of the reload register before it stops.
One-shot pulse output time	(n+1)(m+1)/fi fi: Count source frequency, n: Setting value in TRBPRE register, m: Setting value in TRBPR register
Count start conditions	• The TSTART bit in the TRBCR register is set to 1 (count starts) and the next trigger is generated • Set the TOSST bit in the TRBOCR register to 1 (one-shot starts) • Input trigger to the $\overline{\text{INT0}}$ pin
Count stop conditions	• When reloading completes after timer RB underflows during primary period • When the TOSSP bit in the TRBOCR register is set to 1 (one-shot stops) • When the TSTART bit in the TRBCR register is set to 0 (stops counting) • When the TSTOP bit in the TRBCR register is set to 1 (forcibly stops counting)
Interrupt request generation timing	In half a cycle of the count source, after the timer underflows (at the same time as the TRBO output ends) [timer RB interrupt]
TRBO pin function	Pulse output
$\overline{\text{INT0}}$ pin functions	• When the INOSTG bit in the TRBIOC register is set to 0 ($\overline{\text{INT0}}$ one-shot trigger disabled): programmable I/O port or $\overline{\text{INT0}}$ interrupt input • When the INOSTG bit in the TRBIOC register is set to 1 ($\overline{\text{INT0}}$ one-shot trigger enabled): external trigger ($\overline{\text{INT0}}$ interrupt input)
Read from timer	The count value can be read out by reading registers TRBPR and TRBPRE.
Write to timer	• When registers TRBPRE and TRBPR are written while the count is stopped, values are written to both the reload register and counter. • When registers TRBPRE and TRBPR are written during the count, values are written to the reload register only (the data is transferred to the counter at the following reload) (1).
Selectable functions	• Output level select function The output level of the one-shot pulse waveform is selected by the TOPL bit in the TRBIOC register. • One-shot trigger select function Refer to **18.5.3 One-Shot Trigger Selection**.

Note:
1. The set value is reflected at the following one-shot pulse after writing to the TRBPR register.

18.5.1 Timer RB I/O Control Register (TRBIOC) in Programmable One-Shot Generation Mode

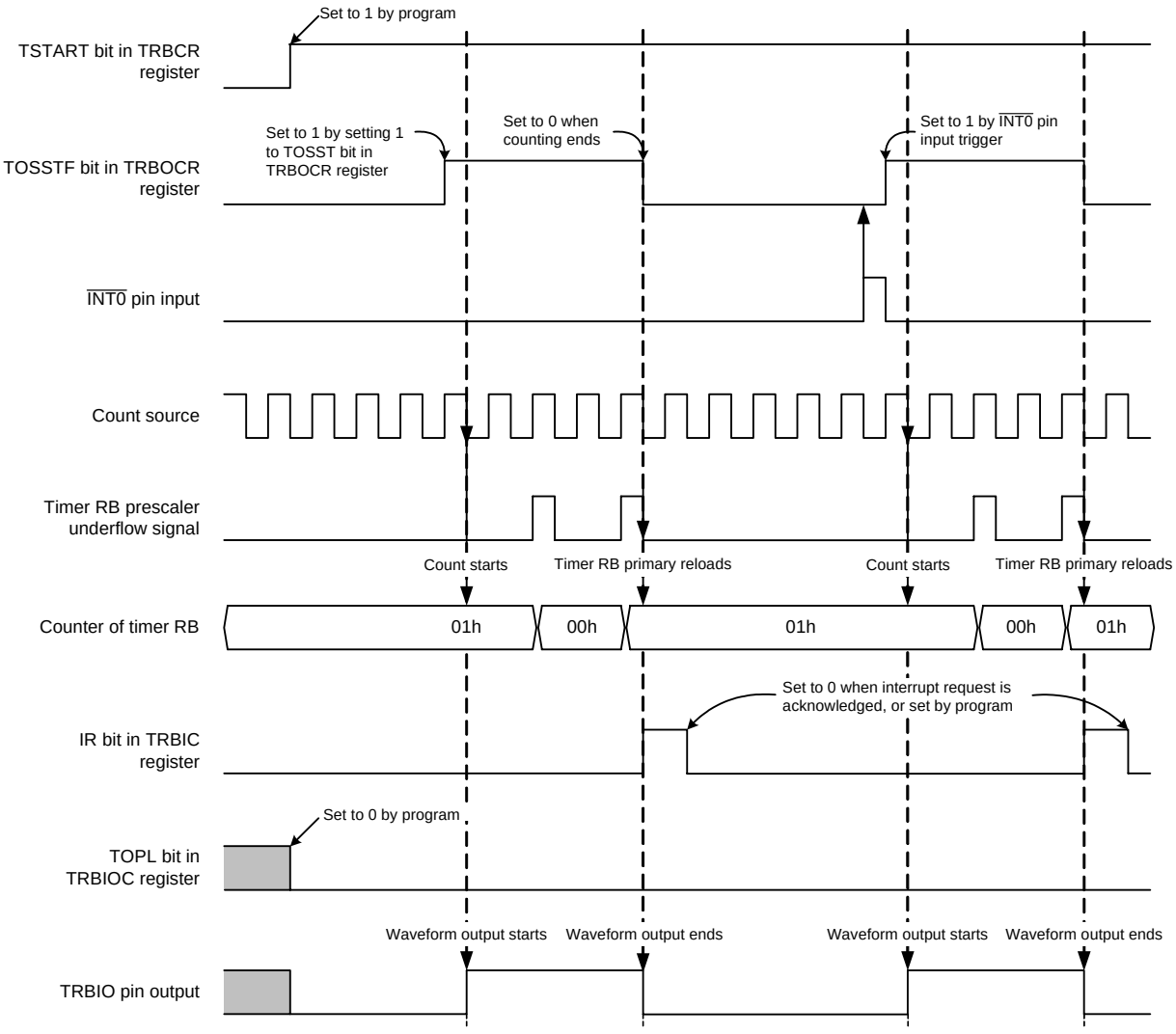
Address 010Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RB output level select bit	0: Outputs one-shot pulse “H” Outputs “L” when the timer is stopped 1: Outputs one-shot pulse “L” Outputs “H” when the timer is stopped	R/W
b1	TOCNT	Timer RB output switch bit	Set to 0 in programmable one-shot generation mode.	R/W
b2	INOSTG	One-shot trigger control bit (1)	0: $\overline{\text{INT0}}$ pin one-shot trigger disabled 1: $\overline{\text{INT0}}$ pin one-shot trigger enabled	R/W
b3	INOSEG	One-shot trigger polarity select bit (1)	0: Falling edge trigger 1: Rising edge trigger	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

Note:
1. Refer to **18.5.3 One-Shot Trigger Selection**.

18.5.2 Operating Example



The above applies under the following conditions.

TRBPRE = 01h, TRBPR = 01h
TRBIOC register TOPL = 0, TOCNT = 0
INOSTG = 1 (INT0 one-shot trigger enabled)
INOSEG = 1 (edge trigger at rising edge)

Figure 18.4 Operating Example of Programmable One-Shot Generation Mode

18.5.3 One-Shot Trigger Selection

In programmable one-shot generation mode and programmable wait one-shot generation mode, operation starts when a one-shot trigger is generated while the TCSTF bit in the TRBCR register is set to 1 (count starts).
A one-shot trigger can be generated by either of the following causes:
- 1 is written to the TOSST bit in the TRBOCR register by a program.
- Trigger input from the $\overline{\text{INT0}}$ pin.

When a one-shot trigger occurs, the TOSSTF bit in the TRBOCR register is set to 1 (one-shot operation in progress) after one or two cycles of the count source have elapsed. Then, in programmable one-shot generation mode, count operation begins and one-shot waveform output starts. (In programmable wait one-shot generation mode, count operation starts for the wait period.) If a one-shot trigger occurs while the TOSSTF bit is set to 1, no retriggering occurs.

To use trigger input from the $\overline{\text{INT0}}$ pin, input the trigger after making the following settings:
- Set the PD4_5 bit in the PD4 register to 0 (input port).
- Select the $\overline{\text{INT0}}$ digital filter with bits INT0F1 and INT0F0 in the INTF register.
- Select both edges or one edge with the INT0PL bit in INTEN register. If one edge is selected, further select falling or rising edge with the INOSEG bit in TRBIOC register.
- Set the INT0EN bit in the INTEN register to 1 (enabled).
- After completing the above, set the INOSTG bit in the TRBIOC register to 1 ($\overline{\text{INT0}}$ pin one-shot trigger enabled).

Note the following points with regard to generating interrupt requests by trigger input from the $\overline{\text{INT0}}$ pin.
- Processing to handle the interrupts is required. Refer to **11. Interrupts**, for details.
- If one edge is selected, use the POL bit in the INT0IC register to select falling or rising edge. (The INOSEG bit in the TRBIOC register does not affect $\overline{\text{INT0}}$ interrupts).
- If a one-shot trigger occurs while the TOSSTF bit is set to 1, timer RB operation is not affected, but the value of the IR bit in the INT0IC register changes.

18.6 Programmable Wait One-Shot Generation Mode

In programmable wait one-shot generation mode, a one-shot pulse is output from the TRBO pin by a program or an external trigger input (input to the $\overline{\text{INT0}}$ pin) (refer to Table 18.5 Programmable Wait One-Shot Generation Mode Specifications). When a trigger is generated from that point, the timer outputs a pulse only once for a given length of time equal to the setting value in the TRBSC register after waiting for a given length of time equal to the setting value in the TRBPR register.
Figure 18.5 shows an Operating Example of Programmable Wait One-Shot Generation Mode.

Table 18.5 Programmable Wait One-Shot Generation Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RA0 underflow
Count operations	• Decrement the timer RB primary setting value. • When a count of the timer RB primary underflows, the timer reloads the contents of timer RB secondary before the count continues. • When a count of the timer RB secondary underflows, the timer reloads the contents of timer RB primary before the count completes and the TOSSTF bit is set to 0 (one-shot stops). • When the count stops, the timer reloads the contents of the reload register before it stops.
Wait time	(n+1)(m+1)/fi fi: Count source frequency n: Value set in the TRBPRE register, m Value set in the TRBPR register
One-shot pulse output time	(n+1)(p+1)/fi fi: Count source frequency n: Value set in the TRBPRE register, p: Value set in the TRBSC register
Count start conditions	• The TSTART bit in the TRBCR register is set to 1 (count starts) and the next trigger is generated. • Set the TOSST bit in the TRBOCR register to 1 (one-shot starts). • Input trigger to the $\overline{\text{INT0}}$ pin
Count stop conditions	• When reloading completes after timer RB underflows during secondary period. • When the TOSSP bit in the TRBOCR register is set to 1 (one-shot stops). • When the TSTART bit in the TRBCR register is set to 0 (starts counting). • When the TSTOP bit in the TRBCR register is set to 1 (forcibly stops counting).
Interrupt request generation timing	In half a cycle of the count source after timer RB underflows during secondary period (complete at the same time as waveform output from the TRBO pin) [timer RB interrupt].
TRBO pin function	Pulse output
$\overline{\text{INT0}}$ pin functions	• When the INOSTG bit in the TRBIOC register is set to 0 ($\overline{\text{INT0}}$ one-shot trigger disabled): programmable I/O port or $\overline{\text{INT0}}$ interrupt input • When the INOSTG bit in the TRBIOC register is set to 1 ($\overline{\text{INT0}}$ one-shot trigger enabled): external trigger ($\overline{\text{INT0}}$ interrupt input)
Read from timer	The count value can be read out by reading registers TRBPR and TRBPRE.
Write to timer	• When registers TRBPRE, TRBSC, and TRBPR are written while the count stops, values are written to both the reload register and counter. • When registers TRBPRE, TRBSC, and TRBPR are written to during count operation, values are written to the reload registers only. (1)
Selectable functions	• Output level select function The output level of the one-shot pulse waveform is selected by the TOPL bit in the TRBIOC register. • One-shot trigger select function Refer to **18.5.3 One-Shot Trigger Selection**.

Note:
1. The set value is reflected at the following one-shot pulse after writing to registers TRBSC and TRBPR.

18.6.1 Timer RB I/O Control Register (TRBIOC) in Programmable Wait One-Shot Generation Mode

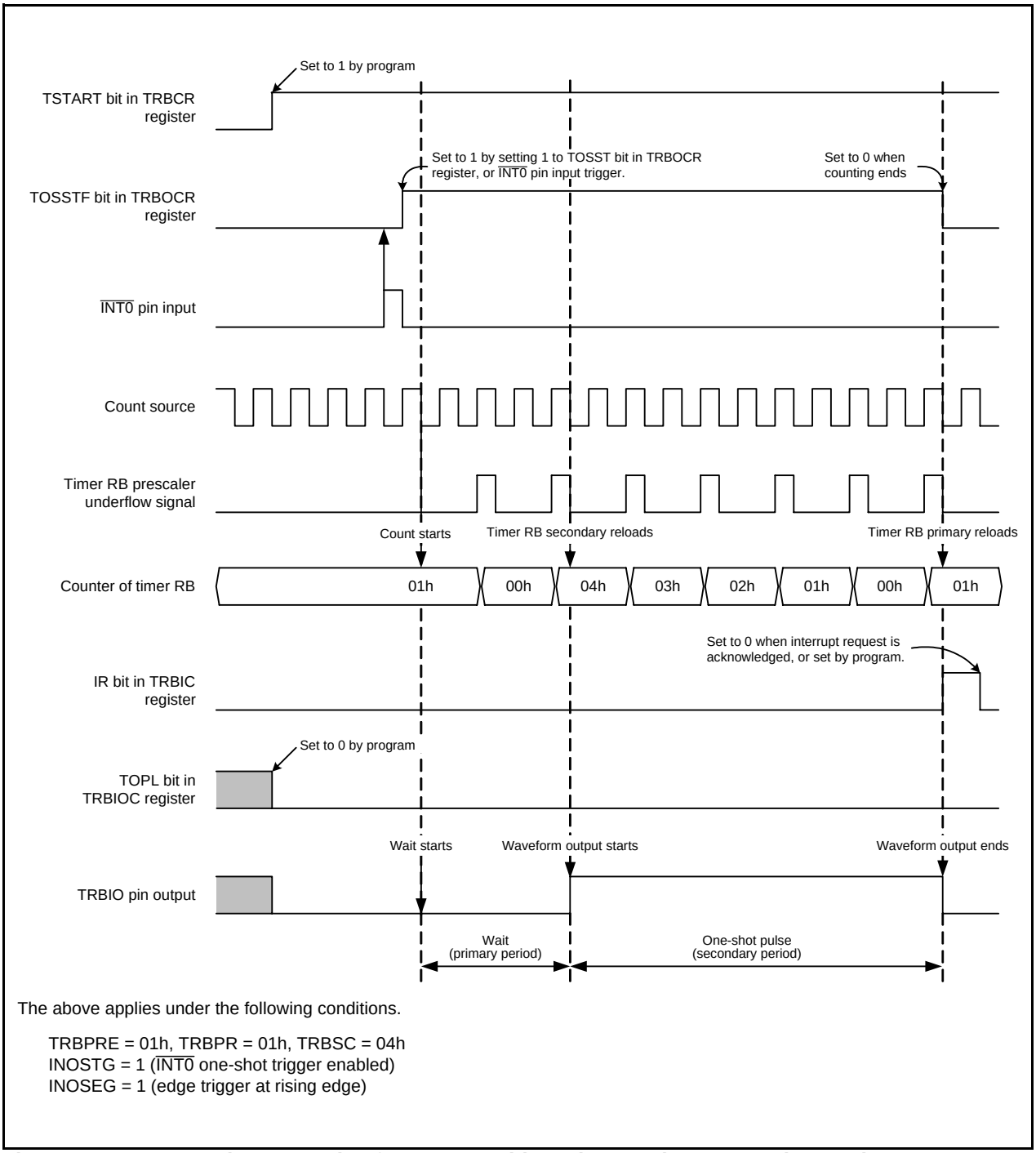
Address 010Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RB output level select bit	0: Outputs one-shot pulse “H” Outputs “L” when the timer stops or during wait 1: Outputs one-shot pulse “L” Outputs “H” when the timer stops or during wait	R/W
b1	TOCNT	Timer RB output switch bit	Set to 0 in programmable wait one-shot generation mode.	R/W
b2	INOSTG	One-shot trigger control bit (1)	0: $\overline{\text{INT0}}$ pin one-shot trigger disabled 1: $\overline{\text{INT0}}$ pin one-shot trigger enabled	R/W
b3	INOSEG	One-shot trigger polarity select bit (1)	0: Falling edge trigger 1: Rising edge trigger	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

Note:
1. Refer to **18.5.3 One-Shot Trigger Selection**.

18.6.2 Operating Example



The above applies under the following conditions.

TRBPRE = 01h, TRBPR = 01h, TRBSC = 04h
INOSTG = 1 (INT0 one-shot trigger enabled)
INOSEG = 1 (edge trigger at rising edge)

Figure 18.5 Operating Example of Programmable Wait One-Shot Generation Mode

18.7 Notes on Timer RB

- Timer RB stops counting after a reset. Set the values in the timer RB and timer RB prescalers before the count starts.
- Even if the prescaler and timer RB is read out in 16-bit units, these registers are read 1 byte at a time by the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In programmable one-shot generation mode and programmable wait one-shot generation mode, when setting the TSTART bit in the TRBCR register to 0 (stops counting) or setting the TOSSP bit in the TRBOCR register to 1 (stops one-shot), the timer reloads the value of reload register and stops. Therefore, in programmable one-shot generation mode and programmable wait one-shot generation mode, read the timer count value before the timer stops.
- The TCSTF bit remains 0 (count stops) for 1 to 2 cycles of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.
  During this time, do not access registers associated with timer RB (1) other than the TCSTF bit. Timer RB starts counting at the first valid edge of the count source after the TCSTF bit is set to 1 (during count).
  The TCSTF bit remains 1 for 1 to 2 cycles of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RB counting is stopped when the TCSTF bit is set to 0.
  During this time, do not access registers associated with timer RB (1) other than the TCSTF bit.

  Note:
  1. Registers associated with timer RB: TRBCR, TRBOCR, TRBIOC, TRBMR, TRBPRE, TRBSC, and TRBPR.

- If the TSTOP bit in the TRBCR register is set to 1 during timer operation, timer RB stops immediately.
- If 1 is written to the TOSST or TOSSP bit in the TRBOCR register, the value of the TOSSTF bit changes after one or two cycles of the count source have elapsed. If the TOSSP bit is written to 1 during the period between when the TOSST bit is written to 1 and when the TOSSTF bit is set to 1, the TOSSTF bit may be set to either 0 or 1 depending on the content state. Likewise, if the TOSST bit is written to 1 during the period between when the TOSSP bit is written to 1 and when the TOSSTF bit is set to 0, the TOSSTF bit may be set to either 0 or 1.
- To use the underflow signal of timer RA as the count source for timer RB, set timer RA in timer mode, pulse output mode, or event count mode.

18.7.1 Timer Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

18.7.2 Programmable Waveform Generation Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

18.7.3 Programmable One-shot Generation Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRE register is written continuously during count operation (TCSTF bit is set to 1), allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously during count operation (TCSTF bit is set to 1), allow three or more cycles of the prescaler underflow for each write interval.

18.7.4 Programmable Wait One-shot Generation Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

19. Timer RC

Timer RC is a 16-bit timer with four I/O pins.

19.1 Overview

Timer RC uses either f1, fOCO40M or fOCO-F as its operation clock. Table 19.1 lists the Timer RC Operation Clock.

Table 19.1 Timer RC Operation Clock

Condition	Timer RC Operation Clock
Count source is f1, f2, f4, f8, f32, or TRCCLK input (bits TCK2 to TCK0 in TRCCR1 register are set to a value from 000b to 101b)	f1
Count source is fOCO40M (bits TCK2 to TCK0 in TRCCR1 register are set to 110b)	fOCO40M
Count source is fOCO-F (bits TCK2 to TCK0 in TRCCR1 register are set to 111b)	fOCO-F

Table 19.2 lists the Pin Configuration of Timer RC, and Figure 19.1 shows a Timer RC Block Diagram.
Timer RC has three modes.

- Timer mode
  - Input capture function — The counter value is captured to a register, using an external signal as the trigger.
  - Output compare function — Matches between the counter and register values are detected. (Pin output state changes when a match is detected.)

The following two modes use the output compare function.

- PWM mode — Pulses of a given width are output continuously.
- PWM2 mode — A one-shot waveform or PWM waveform is output following the trigger after the wait time has elapsed.

Input capture function, output compare function, and PWM mode settings may be specified independently for each pin.
In PWM2 mode waveforms are output based on a combination of the counter or the register.

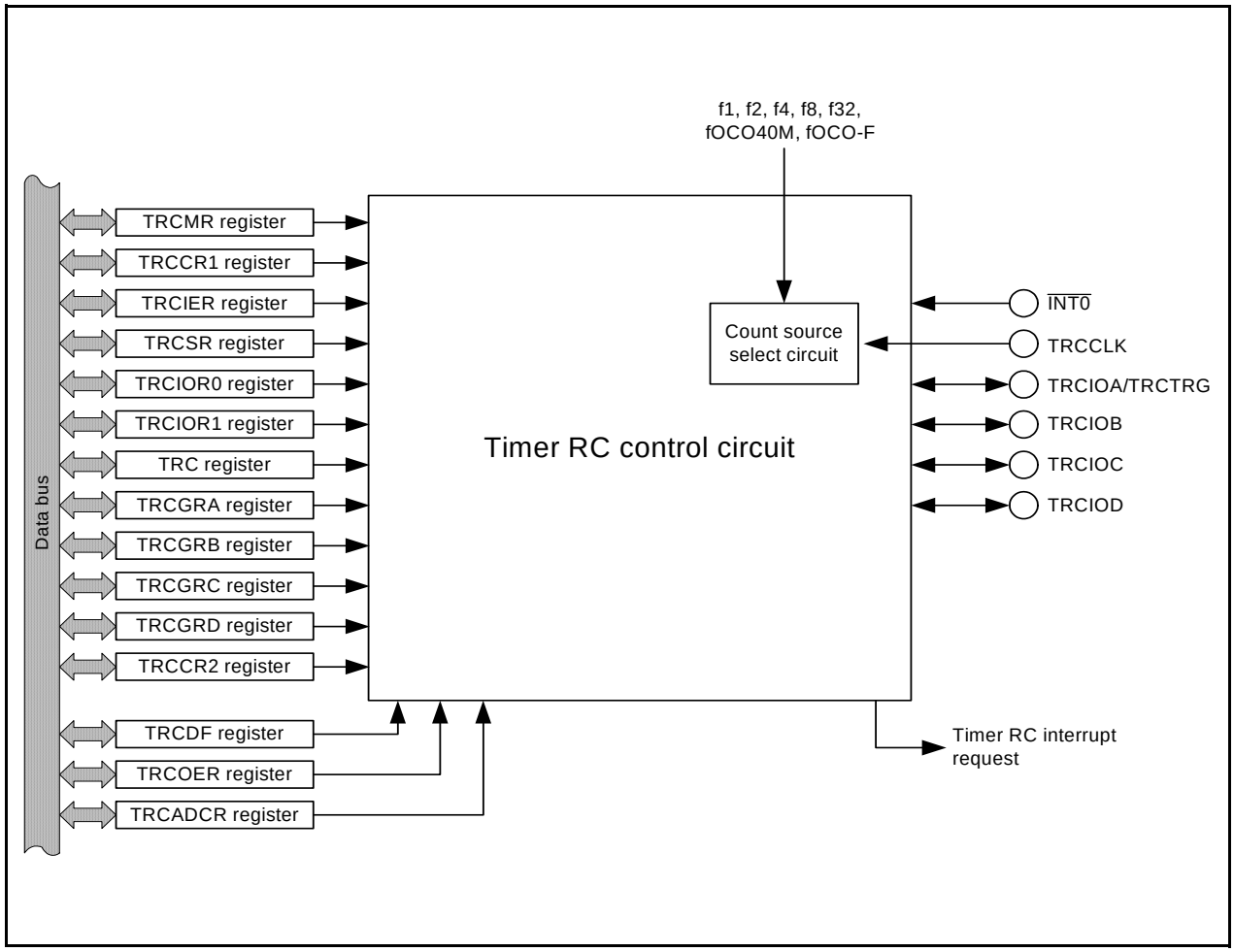


Figure 19.1 Timer RC Block Diagram

Table 19.2 Pin Configuration of Timer RC

Pin Name	Assigned Pin	I/O	Function
TRCIOA	P5_1	I/O	Function differs according to the mode. Refer to descriptions of individual modes for details
TRCIOB	P5_2		
TRCIOC	P5_3		
TRCIOD	P5_4		
TRCCLK	P5_0	Input	External clock input
TRCTRG	P5_1	Input	PWM2 mode external trigger input

19.2 Registers

Table 19.3 lists the Registers Associated with Timer RC.

Table 19.3 Registers Associated with Timer RC

Address	Symbol	Mode				Related Information
		Timer		PWM	PWM2	
		Input Capture Function	Output Compare Function			
0008h	MSTCR	Valid	Valid	Valid	Valid	19.2.1 Module Standby Control Register (MSTCR)
0120h	TRCMR	Valid	Valid	Valid	Valid	19.2.2 Timer RC Mode Register (TRCMR)
0121h	TRCCR1	Valid	Valid	Valid	Valid	Timer RC control register 1 19.2.3 Timer RC Control Register 1 (TRCCR1) 19.5.1 Timer RC Control Register 1 (TRCCR1) for Output Compare Function 19.6.1 Timer RC Control Register 1 (TRCCR1) in PWM Mode 19.7.1 Timer RC Control Register 1 (TRCCR1) in PWM2 Mode
0122h	TRCIER	Valid	Valid	Valid	Valid	19.2.4 Timer RC Interrupt Enable Register (TRCIER)
0123h	TRCSR	Valid	Valid	Valid	Valid	19.2.5 Timer RC Status Register (TRCSR)
0124h	TRCIOR0	Valid	Valid	–	–	Timer RC I/O control register 0, timer RC I/O control register 1 19.2.6 Timer RC I/O Control Register 0 (TRCIOR0) 19.2.7 Timer RC I/O Control Register 1 (TRCIOR1) 19.4.1 Timer RC I/O Control Register 0 (TRCIOR0) for Input Capture Function 19.4.2 Timer RC I/O Control Register 1 (TRCIOR1) for Input Capture Function 19.5.2 Timer RC I/O Control Register 0 (TRCIOR0) for Output Compare Function 19.5.3 Timer RC I/O Control Register 1 (TRCIOR1) for Output Compare Function
0125h	TRCIOR1					
0126h 0127h	TRC	Valid	Valid	Valid	Valid	19.2.8 Timer RC Counter (TRC)
0128h 0129h	TRCGRA	Valid	Valid	Valid	Valid	19.2.9 Timer RC General Registers A, B, C, and D (TRCGRA, TRCGRB, TRCGRC, TRCGRD)
012Ah 012Bh	TRCGRB					
012Ch 012Dh	TRCGRC					
012Eh 012Fh	TRCGRD					
0130h	TRCCR2	–	Valid	Valid	Valid	19.2.10 Timer RC Control Register 2 (TRCCR2)
0131h	TRCDF	Valid	–	–	Valid	19.2.11 Timer RC Digital Filter Function Select Register (TRCDF)
0132h	TRCOER	–	Valid	Valid	Valid	19.2.12 Timer RC Output Master Enable Register (TRCOER)
0133h	TRCADCR	–	Valid	Valid	Valid	19.2.13 Timer RC Trigger Control Register (TRCADCR)
0181h	TRBRCSR	Valid	Valid	Valid	Valid	19.2.14 Timer RB/RC Pin Select Register (TRBRCSR)
0182h	TRCPSR0	Valid	Valid	Valid	Valid	19.2.15 Timer RC Pin Select Register 0 (TRCPSR0)
0183h	TRCPSR1	Valid	Valid	Valid	Valid	19.2.16 Timer RC Pin Select Register 1 (TRCPSR1)

–: Invalid

19.2.1 Module Standby Control Register (MSTCR)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	MSTTRG	MSTTRC	MSTTRD	MSTIIC	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	MSTIIC	SSU standby bit	0: Active 1: Standby (1)	R/W
b4	MSTTRD	Timer RD standby bit	0: Active 1: Standby (2, 3)	R/W
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (4)	R/W
b6	MSTTRG	Timer RG standby bit	0: Active 1: Standby (5)	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. When the MSTIIC bit is set to 1 (standby), any access to the SSU associated registers (addresses 0193h to 019Dh) is disabled.
2. When the MSTTRD bit is set to 1 (standby), any access to the timer RD associated registers (addresses 0136h to 015Fh) is disabled.
3. To set the MSTTRD bit to 1 (standby), set bits TCK2 to TCK0 in the TRDCRi (i = 0 or 1) register to 000b (f1).
4. When the MSTTRC bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0120h to 0133h) is disabled.
5. When the MSTTRG bit is set to 1 (standby), any access to the timer RG associated registers (addresses 0170h to 017Fh) is disabled.

19.2.2 Timer RC Mode Register (TRCMR)

Address 0120h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TSTART	—	BFD	BFC	PWM2	PWMD	PWMC	PWMB
After Reset	0	1	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PWMB	PWM mode of TRCIOB select bit (1)	0: Timer mode 1: PWM mode	R/W
b1	PWMC	PWM mode of TRCIOC select bit (1)	0: Timer mode 1: PWM mode	R/W
b2	PWMD	PWM mode of TRCIOD select bit (1)	0: Timer mode 1: PWM mode	R/W
b3	PWM2	PWM2 mode select bit	0: PWM 2 mode 1: Timer mode or PWM mode	R/W
b4	BFC	TRCGRC register function select bit (2)	0: General register 1: Buffer register of TRCGRA register	R/W
b5	BFD	TRCGRD register function select bit	0: General register 1: Buffer register of TRCGRB register	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b7	TSTART	TRC count start bit	0: Count stops 1: Count starts	R/W

Notes:
1. These bits are enabled when the PWM2 bit is set to 1 (timer mode or PWM mode).
2. Set the BFC bit to 0 (general register) in PWM2 mode.

For notes on PWM2 mode, refer to **19.9.6 TRCMR Register in PWM2 Mode**.

19.2.3 Timer RC Control Register 1 (TRCCR1)

Address 0121h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR	TCK2	TCK1	TCK0	TOD	TOC	TOB	TOA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA	TRCIOA output level select bit (1)	Function varies according to the operating mode (function).	R/W
b1	TOB	TRCIOB output level select bit (1)		R/W
b2	TOC	TRCIOC output level select bit (1)		R/W
b3	TOD	TRCIOD output level select bit (1)		R/W
b4	TCK0	Count source select bit (1)	b6 b5 b4 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRCCLK input rising edge 1 1 0: fOCO40M 1 1 1: fOCO-F (2)	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	CCLR	TRC counter clear select bit	0: Disable clear (free-running operation) 1: Clear TRC counter by input capture or by compare match in TRCGRA	R/W

Notes:
1. Set to these bits when the TSTART bit in the TRCMR register is set to 0 (count stops).
2. To select fOCO-F, set it to the clock frequency higher than the CPU clock frequency.

19.2.4 Timer RC Interrupt Enable Register (TRCIER)

Address 0122h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	OVIE	—	—	—	IMIED	IMIEC	IMIEB	IMIEA
After Reset	0	1	1	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input capture / compare match interrupt enable bit A	0: Disable interrupt (IMIA) by the IMFA bit 1: Enable interrupt (IMIA) by the IMFA bit	R/W
b1	IMIEB	Input capture / compare match interrupt enable bit B	0: Disable interrupt (IMIB) by the IMFB bit 1: Enable interrupt (IMIB) by the IMFB bit	R/W
b2	IMIEC	Input capture / compare match interrupt enable bit C	0: Disable interrupt (IMIC) by the IMFC bit 1: Enable interrupt (IMIC) by the IMFC bit	R/W
b3	IMIED	Input capture / compare match interrupt enable bit D	0: Disable interrupt (IMID) by the IMFD bit 1: Enable interrupt (IMID) by the IMFD bit	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	OVIE	Overflow interrupt enable bit	0: Disable interrupt (OVI) by the OVF bit 1: Enable interrupt (OVI) by the OVF bit	R/W

19.2.5 Timer RC Status Register (TRCSR)

Address 0123h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	OVF	—	—	—	IMFD	IMFC	IMFB	IMFA
After Reset	0	1	1	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input capture / compare match flag A	[Source for setting this bit to 0] Write 0 after read (1). [Source for setting this bit to 1] Refer to **Table 19.4 Source for Setting Bit of Each Flag to 1**.	R/W
b1	IMFB	Input capture / compare match flag B		R/W
b2	IMFC	Input capture / compare match flag C		R/W
b3	IMFD	Input capture / compare match flag D		R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	OVF	Overflow flag	[Source for setting this bit to 0] Write 0 after read (1). [Source for setting this bit to 1] Refer to **Table 19.4 Source for Setting Bit of Each Flag to 1**.	R/W

Note:
1. The writing results are as follows:
   - This bit is set to 0 when the read result is 1 and 0 is written to the same bit.
   - This bit remains unchanged even if the read result is 0 and 0 is written to the same bit. (This bit remains 1 even if it is set to 1 from 0 after reading, and writing 0.)
   - This bit remains unchanged if 1 is written to it.

Table 19.4 Source for Setting Bit of Each Flag to 1

Bit Symbol	Timer Mode		PWM Mode	PWM2 Mode
	Input capture Function	Output Compare Function		
IMFA	TRCIOA pin input edge (1)	When the values of the registers TRC and TRCGRA match.		
IMFB	TRCIOB pin input edge (1)	When the values of the registers TRC and TRCGRB match.		
IMFC	TRCIOC pin input edge (1)	When the values of the registers TRC and TRCGRC match. (2)		
IMFD	TRCIOD pin input edge (1)	When the values of the registers TRC and TRCGRD match. (2)		
OVF	When the TRC register overflows.			

Notes:
1. Edge selected by bits IOj1 to IOj0 (j = A, B, C, or D).
2. Includes the condition that bits BFC and BFD are set to 1 (buffer registers of registers TRCGRA and TRCGRB).

19.2.6 Timer RC I/O Control Register 0 (TRCIOR0)

Address 0124h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRCGRA control bit	Function varies according to the operating mode (function).	R/W
b1	IOA1			R/W
b2	IOA2	TRCGRA mode select bit (1)	0: Output compare function 1: Input capture function	R/W
b3	IOA3	TRCGRA input capture input switch bit (3)	0: fOCO128 signal 1: TRCIOA pin input	R/W
b4	IOB0	TRCGRB control bit	Function varies according to the operating mode (function).	R/W
b5	IOB1			R/W
b6	IOB2	TRCGRB mode select bit (2)	0: Output compare function 1: Input capture function	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.
3. The IOA3 bit is enabled when the IOA2 bit is set to 1 (input capture function).

The TRCIOR0 register is enabled in timer mode. It is disabled in modes PWM and PWM2.

19.2.7 Timer RC I/O Control Register 1 (TRCIOR1)

Address 0125h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOC0	TRCGRC control bit	Function varies according to the operating mode (function).	R/W
b1	IOC1			R/W
b2	IOC2	TRCGRC mode select bit (1)	0: Output compare function 1: Input capture function	R/W
b3	IOC3	TRCGRC register function select bit	0: TRCIOA output register 1: General register or buffer register	R/W
b4	IOD0	TRCGRD control bit	Function varies according to the operating mode (function).	R/W
b5	IOD1			R/W
b6	IOD2	TRCGRD mode select bit (2)	0: Output compare function 1: Input capture function	R/W
b7	IOD3	TRCGRD register function select bit	0: TRCIOB output register 1: General register or buffer register	R/W

Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

The TRCIOR1 register is enabled in timer mode. It is disabled in modes PWM and PWM2.

19.2.8 Timer RC Counter (TRC)

Address 0127h to 0126h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15 to b0	Count a count source. Count operation is incremented. When an overflow occurs, the OVF bit in the TRCSR register is set to 1.	0000h to FFFFh	R/W

Access the TRC register in 16-bit units. Do not access it in 8-bit units.

19.2.9 Timer RC General Registers A, B, C, and D (TRCGRA, TRCGRB, TRCGRC, TRCGRD)

Address 0129h to 0128h (TRCGRA), 012Bh to 012Ah (TRCGRB), 012Dh to 012Ch (TRCGRC), 012Fh to 012Eh (TRCGRD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b15 to b0	Function varies according to the operating mode.	R/W

Access registers TRCGRA to TRCGRD in 16-bit units. Do not access them in 8-bit units.

19.2.10 Timer RC Control Register 2 (TRCCR2)

Address 0130h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCEG1	TCEG0	CSEL	—	—	POLD	POLC	POLB
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POLB	PWM mode output level control bit B (1)	0: TRCIOB output level selected as “L” active 1: TRCIOB output level selected as “H” active	R/W
b1	POLC	PWM mode output level control bit C (1)	0: TRCIOC output level selected as “L” active 1: TRCIOC output level selected as “H” active	R/W
b2	POLD	PWM mode output level control bit D (1)	0: TRCIOD output level selected as “L” active 1: TRCIOD output level selected as “H” active	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b4	—			
b5	CSEL	TRC count operation select bit (2)	0: Count continues at compare match with the TRCGRA register 1: Count stops at compare match with the TRCGRA register	R/W
b6	TCEG0	TRCTRG input edge select bit (3)	b7 b6 0 0: Disable the trigger input from the TRCTRG pin 0 1: Rising edge selected 1 0: Falling edge selected 1 1: Both edges selected	R/W
b7	TCEG1			R/W

Notes:
1. Enabled when in PWM mode.
2. Enabled when in output compare function, PWM mode, or PWM2 mode. For notes on PWM2 mode, refer to **19.9.6 TRCMR Register in PWM2 Mode**.
3. Enabled when in PWM2 mode.

19.2.11 Timer RC Digital Filter Function Select Register (TRCDF)

Address 0131h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DFCK1	DFCK0	—	DFTRG	DFD	DFC	DFB	DFA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DFA	TRCIOA pin digital filter function select bit (1)	0: Function is not used 1: Function is used	R/W
b1	DFB	TRCIOB pin digital filter function select bit (1)		R/W
b2	DFC	TRCIOC pin digital filter function select bit (1)		R/W
b3	DFD	TRCIOD pin digital filter function select bit (1)		R/W
b4	DFTRG	TRCTRG pin digital filter function select bit (2)		R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	DFCK0	Clock select bits for digital filter function (1, 2)	b7 b6 0 0: f32 0 1: f8 1 0: f1 1 1: Count source (clock selected by bits TCK2 to TCK0 in the TRCCR1 register)	R/W
b7	DFCK1			R/W

Notes:
1. These bits are enabled for the input capture function.
2. These bits are enabled when in PWM2 mode and bits TCEG1 to TCEG0 in the TRCCR2 register are set to 01b, 10b, or 11b (TRCTRG trigger input enabled).

19.2.12 Timer RC Output Master Enable Register (TRCOER)

Address 0132h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PTO	—	—	—	ED	EC	EB	EA
After Reset	0	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	EA	TRCIOA output disable bit (1)	0: Enable output 1: Disable output (The TRCIOA pin is used as a programmable I/O port.)	R/W
b1	EB	TRCIOB output disable bit (1)	0: Enable output 1: Disable output (The TRCIOB pin is used as a programmable I/O port.)	R/W
b2	EC	TRCIOC output disable bit (1)	0: Enable output 1: Disable output (The TRCIOC pin is used as a programmable I/O port.)	R/W
b3	ED	TRCIOD output disable bit (1)	0: Enable output 1: Disable output (The TRCIOD pin is used as a programmable I/O port.)	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	PTO	$\overline{\text{INT0}}$ of pulse output forced cutoff signal input enabled bit	0: Pulse output forced cutoff input disabled 1: Pulse output forced cutoff input enabled (Bits EA, EB, EC, and ED are set to 1 (disable output) when “L” is applied to the $\overline{\text{INT0}}$ pin)	R/W

Note:
1. These bits are disabled for input pins set to the input capture function.

19.2.13 Timer RC Trigger Control Register (TRCADCR)

Address 0133h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	ADTRGDE	ADTRGCE	ADTRGBE	ADTRGAE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADTRGAE	A/D trigger A enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRC and TRCGRA	R/W
b1	ADTRGBE	A/D trigger B enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRC and TRCGRB	R/W
b2	ADTRGCE	A/D trigger C enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRC and TRCGRC	R/W
b3	ADTRGDE	A/D trigger D enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRC and TRCGRD	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

19.2.14 Timer RB/RC Pin Select Register (TRBRCSR)

Address 0181h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	TRCCLKSEL2	TRCCLKSEL1	TRCCLKSEL0	—	—	TRBOSEL1	TRBOSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRBOSEL0	TRBO pin select bit	b1 b0 0 0: P1_3 assigned 0 1: P3_1 assigned 1 0: Do not set. 1 1: TRBO pin not used	R/W
b1	TRBOSEL1			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	TRCCLKSEL0	TRCCLK pin select bit	b6 b5 b4 0 0 0: TRCCLK pin not used 1 0 0: P5_0 assigned Other than above: Do not set.	R/W
b5	TRCCLKSEL1			R/W
b6	TRCCLKSEL2			R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

The TRBRCSR register selects which pin is assigned to the timer RB and timer RC I/O. To use the I/O pin for timer RB and timer RC, set this register.
Set bits TRBOSEL0 and TRBOSEL1 before setting the timer RB associated registers. Set bits TRCCLKSEL0 to TRCCLKSEL2 before setting the timer RC associated registers. Also, do not change the setting values of bits TRBOSEL0 and TRBOSEL1 during timer RB operation. Do not change the setting values of bits TRCCLKSEL0 to TRCCLKSEL2 during timer RC operation.

19.2.15 Timer RC Pin Select Register 0 (TRCPSR0)

Address 0182h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	TRCIOBSEL2	TRCIOBSEL1	TRCIOBSEL0	—	TRCIOASEL2	TRCIOASEL1	TRCIOASEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRCIOASEL0	TRCIOA/TRCTRG pin select bit	b2 b1 b0 0 0 0: TRCIOA/TRCTRG pin not used 1 0 1: P5_1 assigned Other than above: Do not set.	R/W
b1	TRCIOASEL1			R/W
b2	TRCIOASEL2			R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TRCIOBSEL0	TRCIOB pin select bit	b6 b5 b4 0 0 0: TRCIOB pin not used 1 1 1: P5_2 assigned Other than above: Do not set.	R/W
b5	TRCIOBSEL1			R/W
b6	TRCIOBSEL2			R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

The TRCPSR0 register selects which pin is assigned to the timer RC I/O. To use the I/O pin for timer RC, set this register.
Set the TRCPSR0 register before setting the timer RC associated registers. Also, do not change the setting value in this register during timer RC operation.

19.2.16 Timer RC Pin Select Register 1 (TRCPSR1)

Address 0183h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	TRCIODSEL2	TRCIODSEL1	TRCIODSEL0	—	TRCIOCSEL2	TRCIOCSEL1	TRCIOCSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRCIOCSEL0	TRCIOC pin select bit	b2 b1 b0 0 0 0: TRCIOC pin not used 1 1 0: P5_3 assigned Other than above: Do not set.	R/W
b1	TRCIOCSEL1			R/W
b2	TRCIOCSEL2			R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TRCIODSEL0	TRCIOD pin select bit	b6 b5 b4 0 0 0: TRCIOD pin not used 1 1 0: P5_4 assigned Other than above: Do not set.	R/W
b5	TRCIODSEL1			R/W
b6	TRCIODSEL2			R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

The TRCPSR1 register selects which pin is assigned to the timer RC I/O. To use the I/O pin for timer RC, set this register.
Set the TRCPSR1 register before setting the timer RC associated registers. Also, do not change the setting value in this register during timer RC operation.

19.3 Common Items for Multiple Modes

19.3.1 Count Source

The method of selecting the count source is common to all modes.
Table 19.5 lists the Count Source Selection, and Figure 19.2 shows a Count Source Block Diagram.

Table 19.5 Count Source Selection

Count Source	Selection Method
f1, f2, f4, f8, f32	Count source selected using bits TCK2 to TCK0 in TRCCR1 register
fOCO40M fOCO-F	FRA00 bit in FRA0 register set to 1 (high-speed on-chip oscillator on) Bits TCK2 to TCK0 in TRCCR1 register are set to 110b (fOCO40M) Bits TCK2 to TCK0 in TRCCR1 register are set to 111b (fOCO-F)
External signal input to TRCCLK pin	Bits TCK2 to TCK0 in TRCCR1 register are set to 101b (count source is rising edge of external clock) and the corresponding direction bit in the corresponding direction register is set is set to 0 (input mode)

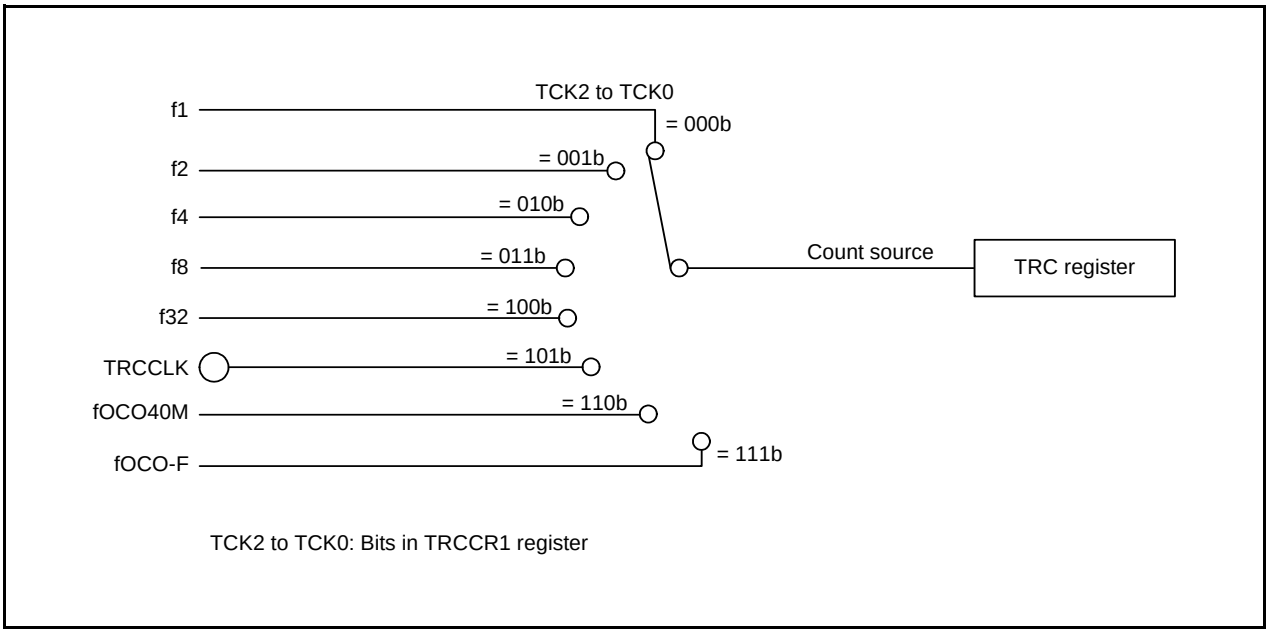


Figure 19.2 Count Source Block Diagram

The pulse width of the external clock input to the TRCCLK pin should be three cycles or more of the timer RC operation clock (see **Table 19.1 Timer RC Operation Clock**).
To select fOCO40M or fOCO-F as the count source, set the FRA00 bit in the FRA0 register set to 1 (high-speed on-chip oscillator on), and then set bits TCK2 to TCK0 in the TRCCR1 register to 110b (fOCO40M) or 111b (fOCO-F).

19.3.2 Buffer Operation

Bits BFC and BFD in the TRCMR register are used to select the TRCGRC or TRCGRD register as the buffer register for the TRCGRA or TRCGRB register.

- Buffer register for TRCGRA register: TRCGRC register
- Buffer register for TRCGRB register: TRCGRD register

Buffer operation differs depending on the mode.

Table 19.6 lists the Buffer Operation in Each Mode, Figure 19.3 shows the Buffer Operation for Input Capture Function, and Figure 19.4 shows the Buffer Operation for Output Compare Function.

Table 19.6 Buffer Operation in Each Mode

Function, Mode	Transfer Timing	Transfer Destination Register
Input capture function	Input capture signal input	Contents of TRCGRA (TRCGRB) register are transferred to buffer register
Output compare function PWM mode	Compare match between TRC register and TRCGRA (TRCGRB) register	Contents of buffer register are transferred to TRCGRA (TRCGRB) register
PWM2 mode	• Compare match between TRC register and TRCGRA register • TRCTRG pin trigger input	Contents of buffer register (TRCGRD) are transferred to TRCGRB register

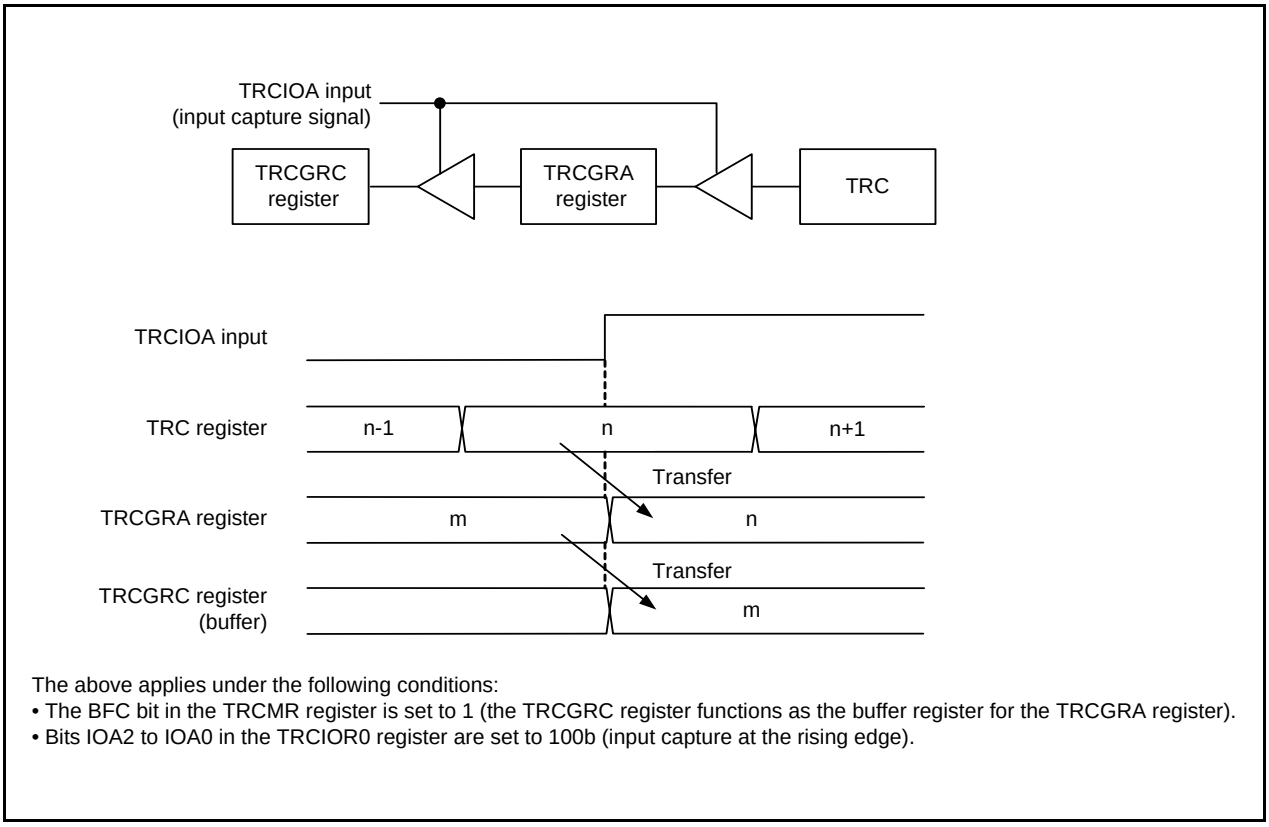
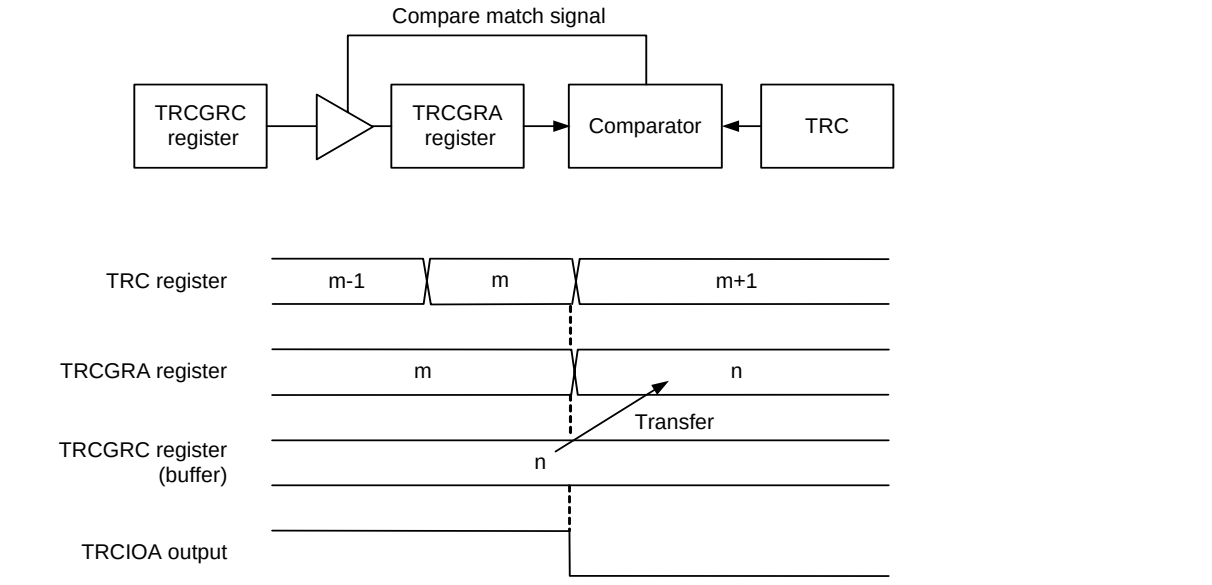


Figure 19.3 Buffer Operation for Input Capture Function



The above applies under the following conditions:
- The BFC bit in the TRCMR register is set to 1 (the TRCGRC register functions as the buffer register for the TRCGRA register).
- Bits IOA2 to IOA0 in the TRCIOR0 register are set to 001b (“L” output at compare match).

Figure 19.4 Buffer Operation for Output Compare Function

Make the following settings in timer mode.
- To use the TRCGRC register as the buffer register for the TRCGRA register:
  Set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
- To use the TRCGRD register as the buffer register for the TRCGRB register:
  Set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

The output compare function, PWM mode, or PWM2 mode, and the TRCGRC or TRCGRD register is functioning as a buffer register, the IMFC bit or IMFD bit in the TRCSR register is set to 1 when a compare match with the TRC register occurs.

The input capture function and the TRCGRC register or TRCGRD register is functioning as a buffer register, the IMFC bit or IMFD bit in the TRCSR register is set to 1 at the input edge of a signal input to the TRCIOC pin or TRCIOD pin.

19.3.3 Digital Filter

The input to TRCTRG or TRCIOj (j = A, B, C, or D) is sampled, and the level is considered to be determined when three matches occur. The digital filter function and sampling clock are selected using the TRCDF register. Figure 19.5 shows a Digital Filter Block Diagram.

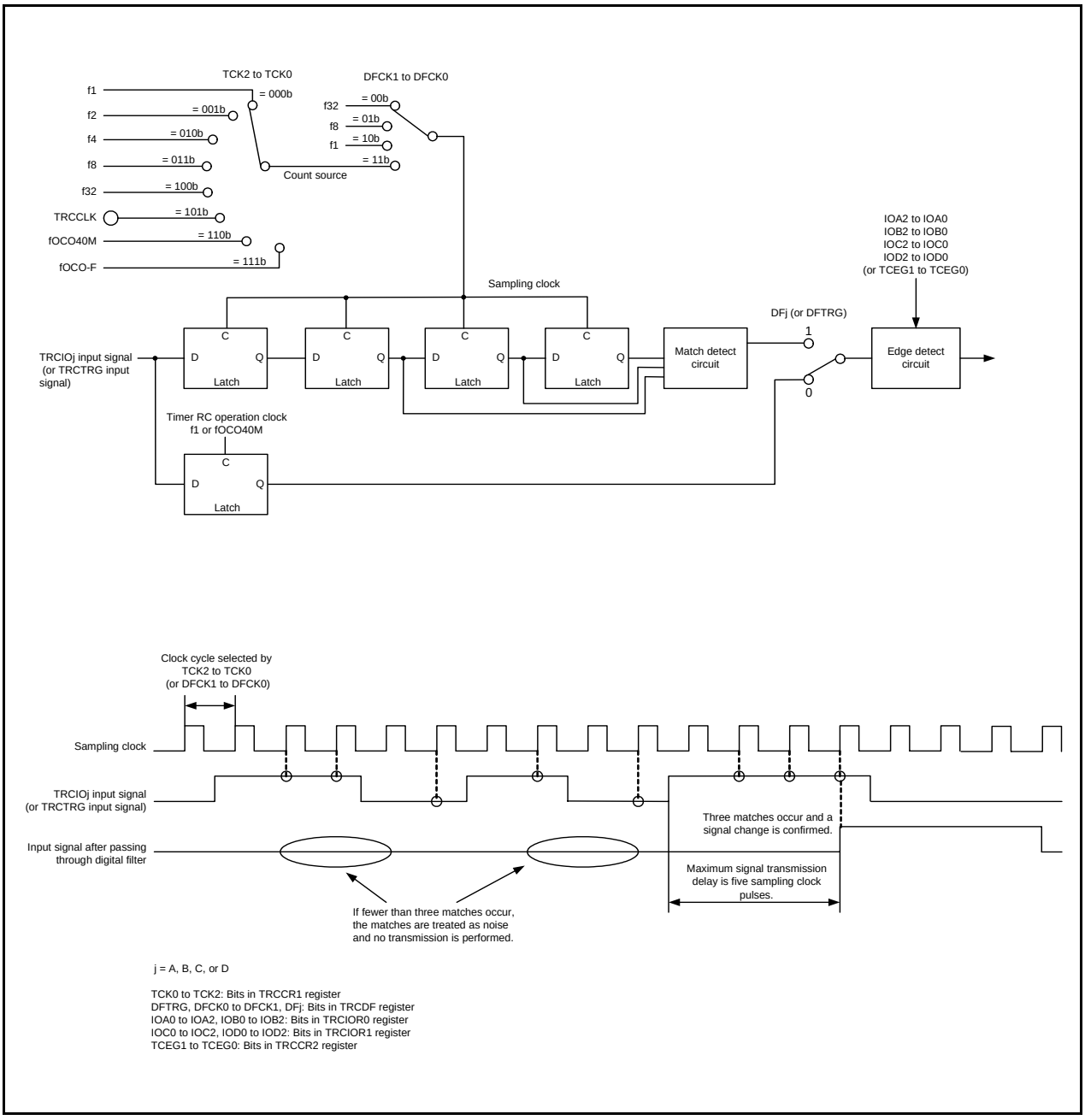


Figure 19.5 Digital Filter Block Diagram

19.3.4 Forced Cutoff of Pulse Output

When using the timer mode's output compare function, the PWM mode, or the PWM2 mode, pulse output from the TRCIOj (j = A, B, C, or D) output pin can be forcibly cut off and the TRCIOj pin set to function as a programmable I/O port by means of input to the $\overline{\text{INT0}}$ pin.
A pin used for output by the timer mode's output compare function, the PWM mode, or the PWM2 mode can be set to function as the timer RC output pin by setting the Ej bit in the TRCOER register to 0 (timer RC output enabled). If "L" is input to the $\overline{\text{INT0}}$ pin while the PTO bit in the TRCOER register is set to 1 (pulse output forced cutoff signal input $\overline{\text{INT0}}$ enabled), bits EA, EB, EC, and ED in the TRCOER register are all set to 1 (timer RC output disabled, TRCIOj output pin functions as the programmable I/O port). When one or two cycles of the timer RC operation clock after "L" input to the $\overline{\text{INT0}}$ pin (refer to **Table 19.1 Timer RC Operation Clock**) has elapsed, the TRCIOj output pin becomes a programmable I/O port.

Make the following settings to use this function:
- Set the pin state following forced cutoff of pulse output (high impedance (input), "L" output, or "H" output). (Refer to **7. I/O Ports**.)
- Set the INT0EN bit in the INTEN register to 1 ($\overline{\text{INT0}}$ input enabled) and the INT0PL bit to 0 (one edge), and set the POL bit in the INT0IC register to 0 (falling edge selected).
- Set the PD4_5 bit in the PD4 register to 0 (input mode).
- Select the $\overline{\text{INT0}}$ digital filter by bits INT0F1 to INT0F0 in the INTF register.
- Set the PTO bit in the TRCOER register to 1 (pulse output forced cutoff signal input $\overline{\text{INT0}}$ enabled).

The IR bit in the INT0IC register is set to 1 (interrupt request) in accordance with the setting of the POL bit in the INT0IC register and the INT0PL bit in the INTEN register and a change in the $\overline{\text{INT0}}$ pin input (refer to **11.8 Notes on Interrupts**).
For details on interrupts, refer to **11. Interrupts**.

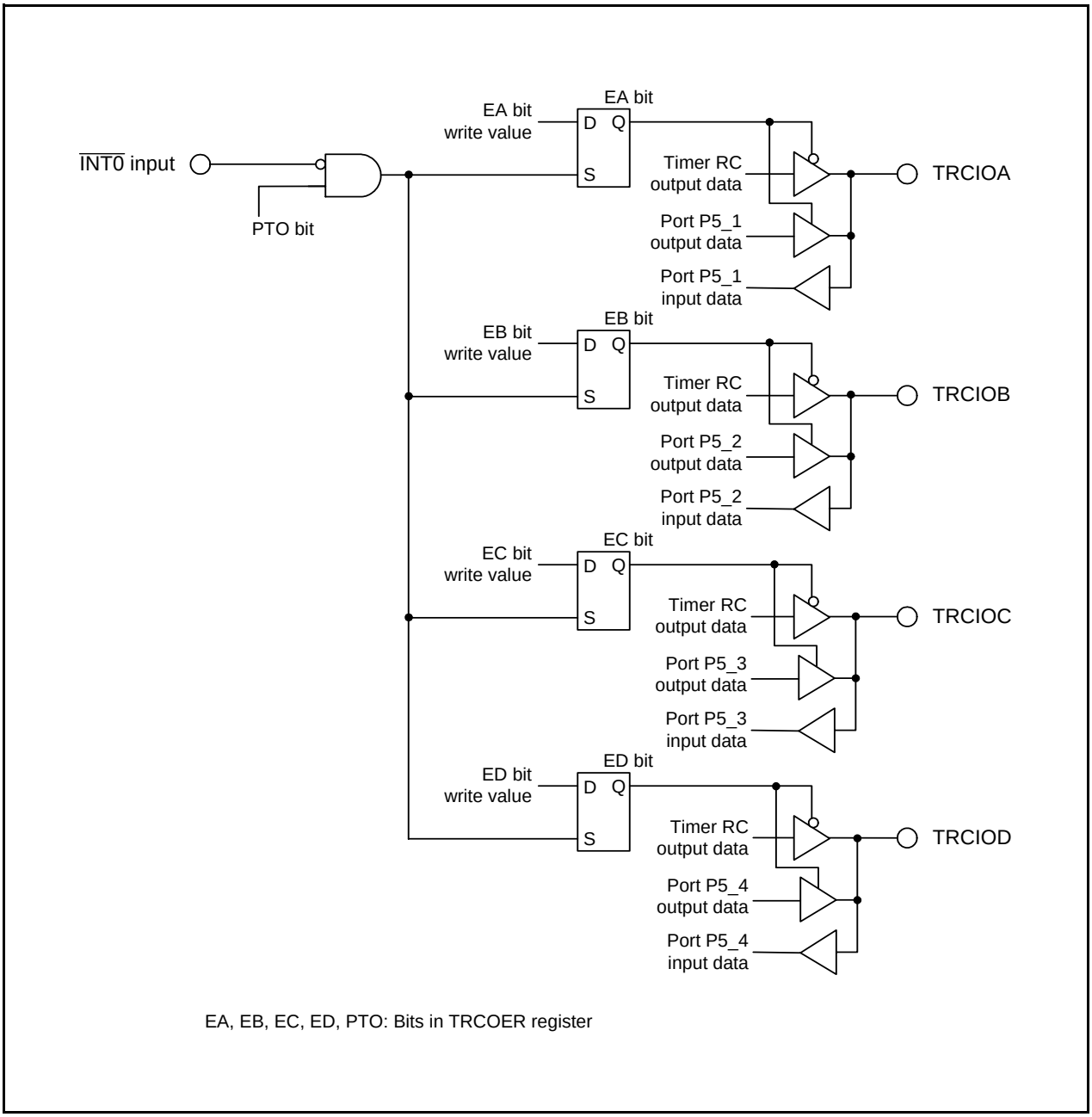


Figure 19.6 Forced Cutoff of Pulse Output

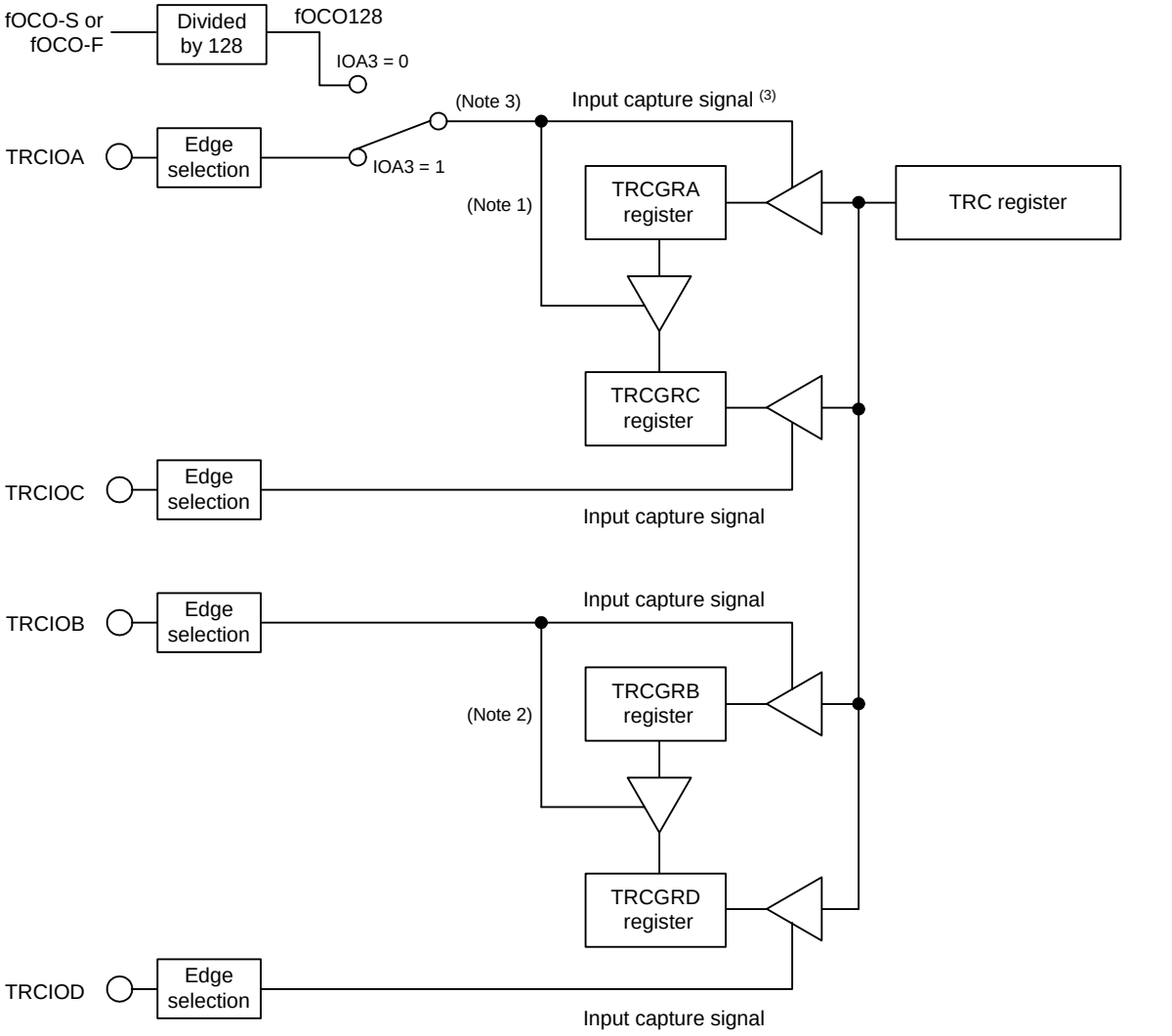
19.4 Timer Mode (Input Capture Function)

This function measures the width or period of an external signal. An external signal input to the TRCIOj (j = A, B, C, or D) pin acts as a trigger for transferring the contents of the TRC register (counter) to the TRCGRj register (input capture). The input capture function, or any other mode or function, can be selected for each individual pin. The TRCGRA register can also select fOCO128 signal as input-capture trigger input.
Table 19.7 lists the Specifications of Input Capture Function, Figure 19.7 shows a Block Diagram of Input Capture Function, Table 19.8 lists the Functions of TRCGRj Register when Using Input Capture Function, and Figure 19.8 shows an Operating Example of Input Capture Function.

Table 19.7 Specifications of Input Capture Function

Item	Specification
Count source	f1, f2, f4, f8, f32, fOCO40M, fOCO-F, or external signal (rising edge) input to TRCCLK pin
Count operation	Increment
Count period	• The CCLR bit in the TRCCR1 register is set to 0 (free running operation): 1/fk × 65,536 fk: Count source frequency • The CCLR bit in the TRCCR1 register is set to 1 (TRC register set to 0000h at TRCGRA input capture): 1/fk × (n + 1) n: TRCGRA register setting value
Count start condition	1 (count starts) is written to the TSTART bit in the TRCMR register.
Count stop condition	0 (count stops) is written to the TSTART bit in the TRCMR register. The TRC register retains a value before count stops.
Interrupt request generation timing	• Input capture (valid edge of TRCIOj input or fOCO128 signal edge) • The TRC register overflows.
TRCIOA, TRCIOB, TRCIOC, and TRCIOD pin functions	Programmable I/O port or input capture input (selectable individually for each pin)
$\overline{\text{INT0}}$ pin function	Programmable I/O port or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading TRC register.
Write to timer	The TRC register can be written to.
Select functions	• Input capture input pin selection One or more of pins TRCIOA, TRCIOB, TRCIOC, and TRCIOD • Input capture input valid edge selection Rising edge, falling edge, or both rising and falling edges • Buffer operation (Refer to **19.3.2 Buffer Operation**.) • Digital filter (Refer to **19.3.3 Digital Filter**.) • Timing for setting the TRC register to 0000h Overflow or input capture • Input-capture trigger selected fOCO128 can be selected for input-capture trigger input of the TRCGRA register.

j = A, B, C, or D



IOA3: Bit in TRCIOR0 register

Notes:
1. The BFC bit in the TRCMR register is set to 1 (TRCGRC register functions as the buffer register for the TRCGRA register)
2. The BFD bit in the TRCMR register is set to 1 (TRCGRD register functions as the buffer register for the TRCGRB register)
3. The trigger input of the TRCGRA register can select the TRCIOA pin input or fOCO128 signal.

Figure 19.7 Block Diagram of Input Capture Function

19.4.1 Timer RC I/O Control Register 0 (TRCIOR0) for Input Capture Function

Address 0124h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRCGRA control bit	b1 b0 0 0: Input capture to the TRCGRA register at the rising edge 0 1: Input capture to the TRCGRA register at the falling edge 1 0: Input capture to the TRCGRA register at both edges 1 1: Do not set.	R/W
b1	IOA1			R/W
b2	IOA2	TRCGRA mode select bit (1)	Set to 1 (input capture) in the input capture function.	R/W
b3	IOA3	TRCGRA input capture input switch bit (3)	0: fOCO128 signal 1: TRCIOA pin input	R/W
b4	IOB0	TRCGRB control bit	b5 b4 0 0: Input capture to the TRCGRB register at the rising edge 0 1: Input capture to the TRCGRB register at the falling edge 1 0: Input capture to the TRCGRB register at both edges 1 1: Do not set.	R/W
b5	IOB1			R/W
b6	IOB2	TRCGRB mode select bit (2)	Set to 1 (input capture) in the input capture function.	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.
3. The IOA3 bit is enabled when the IOA2 bit is set to 1 (input capture function).

19.4.2 Timer RC I/O Control Register 1 (TRCIOR1) for Input Capture Function

Address 0125h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOC0	TRCGRC control bit	b1 b0 0 0: Input capture to the TRCGRC register at the rising edge 0 1: Input capture to the TRCGRC register at the falling edge 1 0: Input capture to the TRCGRC register at both edges 1 1: Do not set.	R/W
b1	IOC1			R/W
b2	IOC2	TRCGRC mode select bit (1)	Set to 1 (input capture) in the input capture function.	R/W
b3	IOC3	TRCGRC register function select bit	Set to 1.	R/W
b4	IOD0	TRCGRD control bit	b5 b4 0 0: Input capture to the TRCGRD register at the rising edge 0 1: Input capture to the TRCGRD register at the falling edge 1 0: Input capture to the TRCGRD register at both edges 1 1: Do not set.	R/W
b5	IOD1			R/W
b6	IOD2	TRCGRD mode select bit (2)	Set to 1 (input capture) in the input capture function.	R/W
b7	IOD3	TRCGRD register function select bit	Set to 1.	R/W

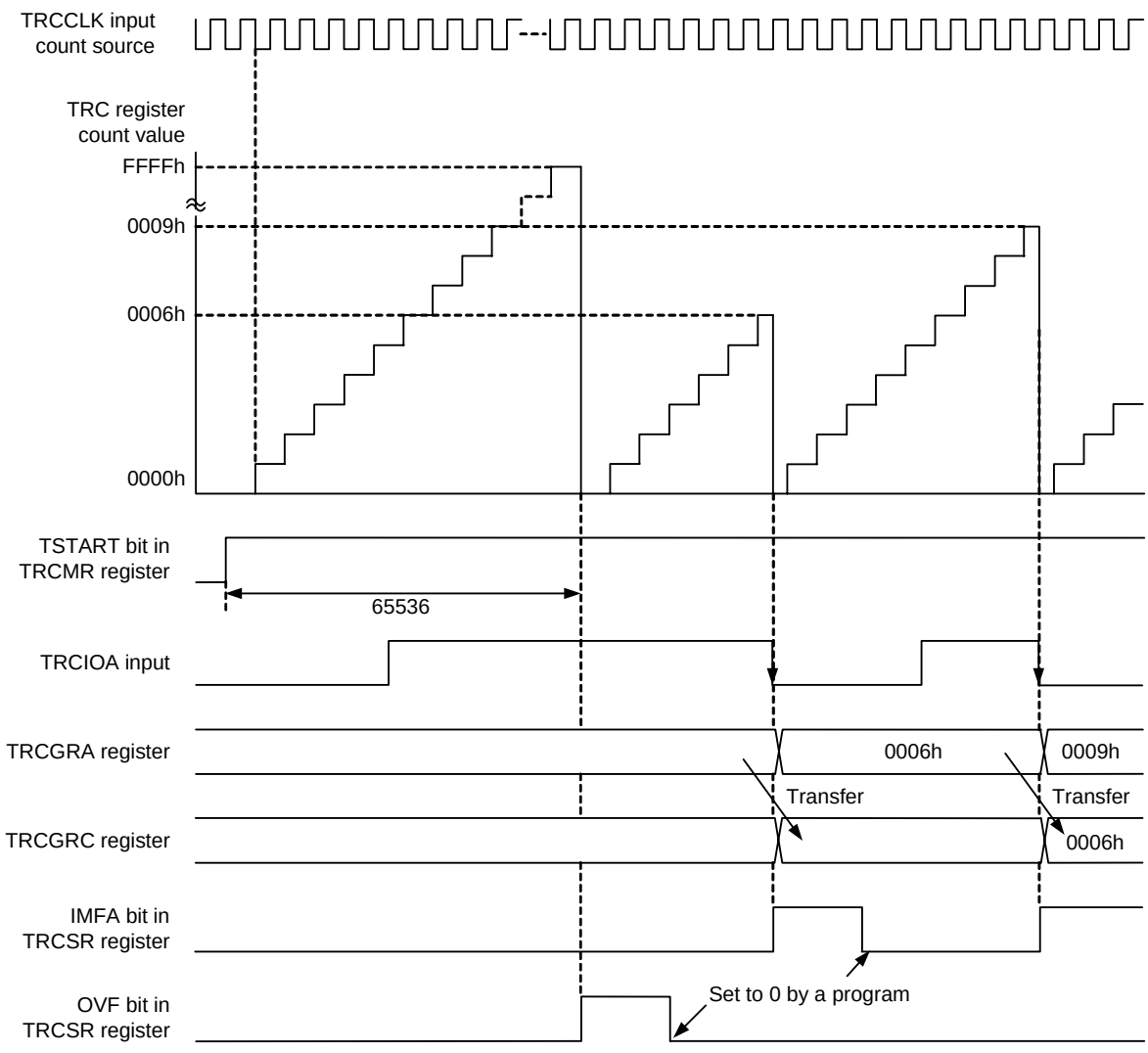
Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

Table 19.8 Functions of TRCGRj Register when Using Input Capture Function

Register	Setting	Register Function	Input Capture Input Pin
TRCGRA	–	General register. Can be used to read the TRC register value at input capture.	TRCIOA
TRCGRB			TRCIOB
TRCGRC	BFC = 0	General register. Can be used to read the TRC register value at input capture.	TRCIOC
TRCGRD	BFD = 0		TRCIOD
TRCGRC	BFC = 1	Buffer registers. Can be used to hold transferred value from the general register. (Refer to **19.3.2 Buffer Operation**.)	TRCIOA
TRCGRD	BFD = 1		TRCIOB

j = A, B, C, or D
BFC, BFD: Bits in TRCMR register

19.4.3 Operating Example



The above applies under the following conditions:
- The CCLR bit in the TRCCR1 register is set to 1 (Clear TRC counter by input capture).
- Bits TCK2 to TCK0 in the TRCCR1 register are set to 101b (the count source is TRCCLK input).
- Bits IOA2 to IOA0 in the TRCIORA register are set to 101b (input capture at the falling edge of the TRCIOA input).
- The BFC bit in the TRCMR register is set to 1 (the TRCGRC register functions as the buffer register for the TRCGRA register).

Figure 19.8 Operating Example of Input Capture Function

19.5 Timer Mode (Output Compare Function)

This function detects when the contents of the TRC register (counter) and the TRCGRj register (j = A, B, C, or D) match (compare match). When a match occurs a signal is output from the TRCIOj pin at a given level. The output compare function, or other mode or function, can be selected for each individual pin.
Table 19.9 lists the Specifications of Output Compare Function, Figure 19.9 shows a Block Diagram of Output Compare Function, Table 19.10 lists the Functions of TRCGRj Register when Using Output Compare Function, and Figure 19.10 shows an Operating Example of Output Compare Function.

Table 19.9 Specifications of Output Compare Function

Item	Specification
Count source	f1, f2, f4, f8, f32, fOCO40M, fOCO-F, or external signal (rising edge) input to TRCCLK pin
Count operation	Increment
Count period	• The CCLR bit in the TRCCR1 register is set to 0 (free running operation): 1/fk × 65,536 fk: Count source frequency • The CCLR bit in the TRCCR1 register is set to 1 (TRC register set to 0000h at TRCGRA compare match): 1/fk × (n + 1) n: TRCGRA register setting value
Waveform output timing	Compare match
Count start condition	1 (count starts) is written to the TSTART bit in the TRCMR register.
Count stop condition	• When the CSEL bit in the TRCCR2 register is set to 0 (count continues after compare match with TRCGRA). 0 (count stops) is written to the TSTART bit in the TRCMR register. The output compare output pin retains output level before count stops, the TRC register retains a value before count stops. • When the CSEL bit in the TRCCR2 register is set to 1 (count stops at compare match with TRCGRA register). The count stops at the compare match with the TRCGRA register. The output-compare output pin retains the level after the output is changed by the compare match.
Interrupt request generation timing	• Compare match (contents of registers TRC and TRCGRj match) • The TRC register overflows.
TRCIOA, TRCIOB, TRCIOC, and TRCIOD pin functions	Programmable I/O port or output compare output (Selectable individually for each pin)
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRC register.
Write to timer	The TRC register can be written to.
Select functions	• Output compare output pin selection One or more of pins TRCIOA, TRCIOB, TRCIOC, and TRCIOD • Compare match output level selection “L” output, “H” output, or toggle output • Initial output level selection Sets output level for period from count start to compare match • Timing for setting the TRC register to 0000h Overflow or compare match with the TRCGRA register • Buffer operation (Refer to **19.3.2 Buffer Operation**.) • Pulse output forced cutoff signal input (Refer to **19.3.4 Forced Cutoff of Pulse Output**.) • Can be used as an internal timer by disabling timer RC output • Changing output pins for registers TRCGRC and TRCGRD TRCGRC can be used for output control of the TRCIOA pin and TRCGRD can be used for output control of the TRCIOB pin. • A/D trigger generation

j = A, B, C, or D

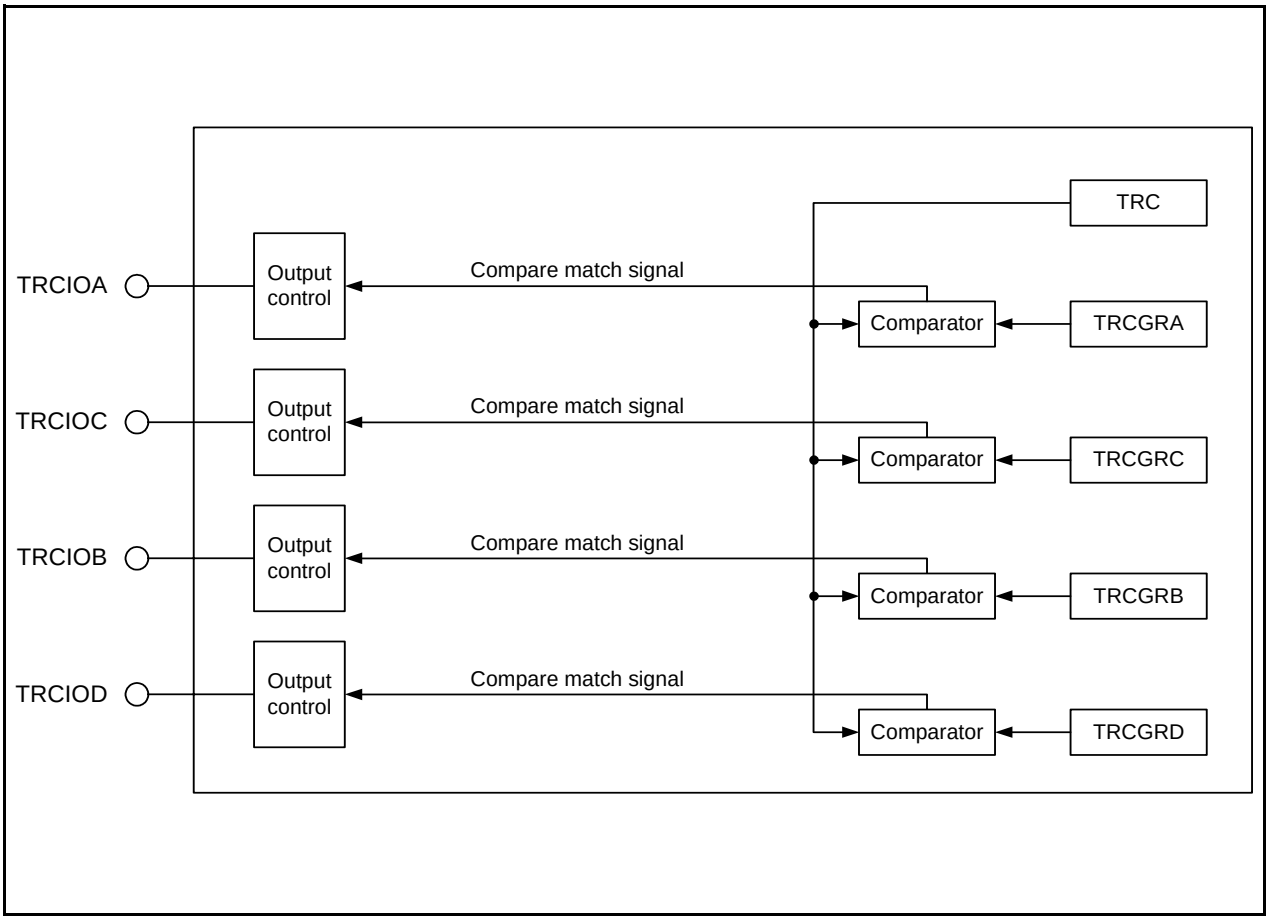


Figure 19.9 Block Diagram of Output Compare Function

19.5.1 Timer RC Control Register 1 (TRCCR1) for Output Compare Function

Address 0121h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR	TCK2	TCK1	TCK0	TOD	TOC	TOB	TOA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA	TRCIOA output level select bit (1, 2)	0: Initial output “L” 1: Initial output “H”	R/W
b1	TOB	TRCIOB output level select bit (1, 2)		R/W
b2	TOC	TRCIOC output level select bit (1, 2)		R/W
b3	TOD	TRCIOD output level select bit (1, 2)		R/W
b4	TCK0	Count source select bit (1)	b6 b5 b4 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRCCLK input rising edge 1 1 0: fOCO40M 1 1 1: fOCO-F (3)	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	CCLR	TRC counter clear select bit	0: Disable clear (free-running operation) 1: Clear by compare match in the TRCGRA register	R/W

Notes:
1. Set to these bits when the TSTART bit in the TRCMR register is set to 0 (count stops).
2. If the pin function is set for waveform output (refer to **7.5 Port Settings**), the initial output level is output when the TRCCR1 register is set.
3. To select fOCO-F, set it to the clock frequency higher than the CPU clock frequency.

Table 19.10 Functions of TRCGRj Register when Using Output Compare Function

Register	Setting	Register Function	Output Compare Output Pin
TRCGRA	–	General register. Write a compare value to one of these registers.	TRCIOA
TRCGRB			TRCIOB
TRCGRC	BFC = 0	General register. Write a compare value to one of these registers.	TRCIOC
TRCGRD	BFD = 0		TRCIOD
TRCGRC	BFC = 1	Buffer register. Write the next compare value to one of these registers. (Refer to **19.3.2 Buffer Operation**.)	TRCIOA
TRCGRD	BFD = 1		TRCIOB

j = A, B, C, or D
BFC, BFD: Bits in TRCMR register

19.5.2 Timer RC I/O Control Register 0 (TRCIOR0) for Output Compare Function

Address 0124h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRCGRA control bit	b1 b0 0 0: Disable pin output by compare match (TRCIOA pin functions as the programmable I/O port) 0 1: “L” output by compare match in the TRCGRA register 1 0: “H” output by compare match in the TRCGRA register 1 1: Toggle output by compare match in the TRCGRA register	R/W
b1	IOA1			R/W
b2	IOA2	TRCGRA mode select bit (1)	Set to 0 (output compare) in the output compare function.	R/W
b3	IOA3	TRCGRA input capture input switch bit	Set to 1.	R/W
b4	IOB0	TRCGRB control bit	b5 b4 0 0: Disable pin output by compare match (TRCIOB pin functions as the programmable I/O port) 0 1: “L” output by compare match in the TRCGRB register 1 0: “H” output by compare match in the TRCGRB register 1 1: Toggle output by compare match in the TRCGRB register	R/W
b5	IOB1			R/W
b6	IOB2	TRCGRB mode select bit (2)	Set to 0 (output compare) in the output compare function.	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in theTRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

19.5.3 Timer RC I/O Control Register 1 (TRCIOR1) for Output Compare Function

Address 0125h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOC0	TRCGRC control bit	b1 b0 0 0: Disable pin output by compare match 0 1: “L” output by compare match in the TRCGRC register 1 0: “H” output by compare match in the TRCGRC register 1 1: Toggle output by compare match in the TRCGRC register	R/W
b1	IOC1			R/W
b2	IOC2	TRCGRC mode select bit (1)	Set to 0 (output compare) in the output compare function.	R/W
b3	IOC3	TRCGRC register function select bit	0: TRCIOA output register 1: General register or buffer register	R/W
b4	IOD0	TRCGRD control bit	b5 b4 0 0: Disable pin output by compare match 0 1: “L” output by compare match in the TRCGRD register 1 0: “H” output by compare match in the TRCGRD register 1 1: Toggle output by compare match in the TRCGRD register	R/W
b5	IOD1			R/W
b6	IOD2	TRCGRD mode select bit (2)	Set to 0 (output compare) in the output compare function.	R/W
b7	IOD3	TRCGRD register function select bit	0: TRCIOB output register 1: General register or buffer register	R/W

Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in theTRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in theTRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

19.5.4 Timer RC Control Register 2 (TRCCR2) for Output Compare Function

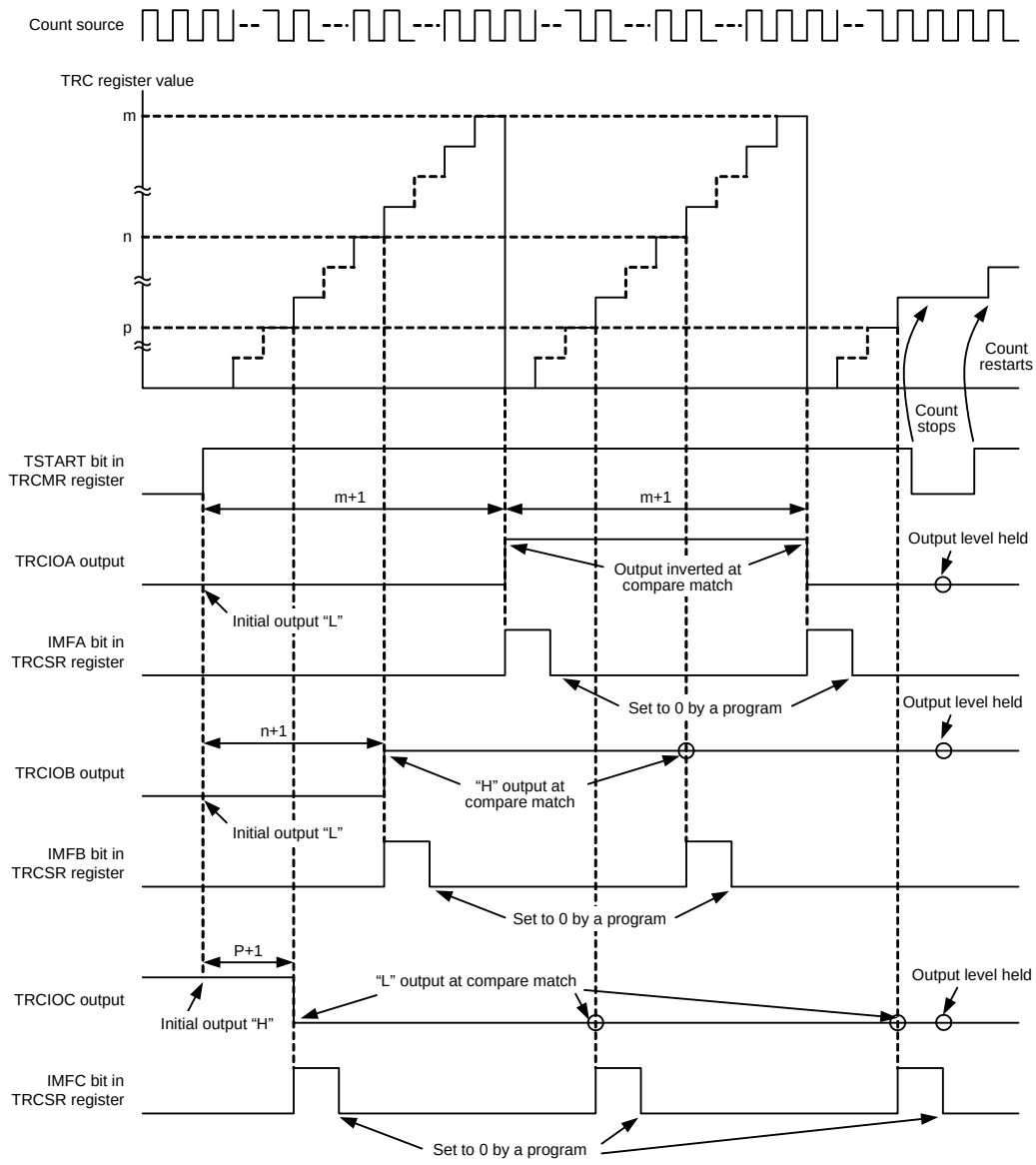
Address 0130h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCEG1	TCEG0	CSEL	—	—	POLD	POLC	POLB
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POLB	PWM mode output level control bit B (1)	0: TRCIOB output level selected as “L” active 1: TRCIOB output level selected as “H” active	R/W
b1	POLC	PWM mode output level control bit C (1)	0: TRCIOC output level selected as “L” active 1: TRCIOC output level selected as “H” active	R/W
b2	POLD	PWM mode output level control bit D (1)	0: TRCIOD output level selected as “L” active 1: TRCIOD output level selected as “H” active	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b4	—			
b5	CSEL	TRC count operation select bit (2)	0: Count continues at compare match with the TRCGRA register 1: Count stops at compare match with the TRCGRA register	R/W
b6	TCEG0	TRCTRG input edge select bit (3)	b7 b6 0 0: Disable the trigger input from the TRCTRG pin 0 1: Rising edge selected 1 0: Falling edge selected 1 1: Both edges selected	R/W
b7	TCEG1			R/W

Notes:
1. Enabled when in PWM mode.
2. Enabled when in output compare function, PWM mode, or PWM2 mode. For notes on PWM2 mode, refer to **19.9.6 TRCMR Register in PWM2 Mode**.
3. Enabled when in PWM2 mode.

19.5.5 Operating Example



m: TRCGRA register setting value
n: TRCGRB register setting value
p: TRCGRC register setting value

The above applies under the following conditions:

- Bits BFC and BFD in the TRCMR register are set to 0 (TRCGRC and TRCGRD do not operate as buffers).
- Bits EA, EB, and EC in the TRCOER register are set to 0 (output from TRCIOA, TRCIOB, and TRCIOC enabled).
- The CCLR bit in the TRCCR1 register is set to 1 (set the TRC register to 0000h by TRCGRA compare match).
- In the TRCCR1 register, bits TOA and TOB are set to 0 ("L" initial output until compare match) and the TOC bit is set to 1 ("H" initial output until compare match).
- Bits IOA2 to IOA0 in the TRCIOR0 register are set to 011b (TRCIOA output inverted at TRCGRA compare match).
- Bits IOB2 to IOB0 in the TRCIOR0 register are set to 010b ("H" TRCIOB output at TRCGRB compare match).
- Bits IOC2 to IOC2 in the TRCIOR1 register are set to 001b ("L" TRCIOC output at TRCGRC compare match).
- The CSEL bit in the TRCCR2 register is set to 0 (TRC count continues after TRCGRA compare match).

Figure 19.10 Operating Example of Output Compare Function

19.5.6 Changing Output Pins in Registers TRCGRC and TRCGRD

The TRCGRC register can be used for output control of the TRCIOA pin, and the TRCGRD register can be used for output control of the TRCIOB pin. Therefore, each pin output can be controlled as follows:

- TRCIOA output is controlled by the values in registers TRCGRA and TRCGRC.
- TRCIOB output is controlled by the values in registers TRCGRB and TRCGRD.

Change output pins in registers TRCGRC and TRCGRD as follows:

- Set the IOC3 bit in the TRCIOR1 register to 0 (TRCIOA output register) and set the IOD3 bit to 0 (TRCIOB output register).
- Set bits BFC and BFD in the TRCMR register to 0 (general register).
- Set different values in registers TRCGRC and TRCGRA. Also, set different values in registers TRCGRD and TRCGRB.

Figure 19.12 shows an Operating Example When TRCGRC Register is Used for Output Control of TRCIOA Pin and TRCGRD Register is Used for Output Control of TRCIOB Pin.

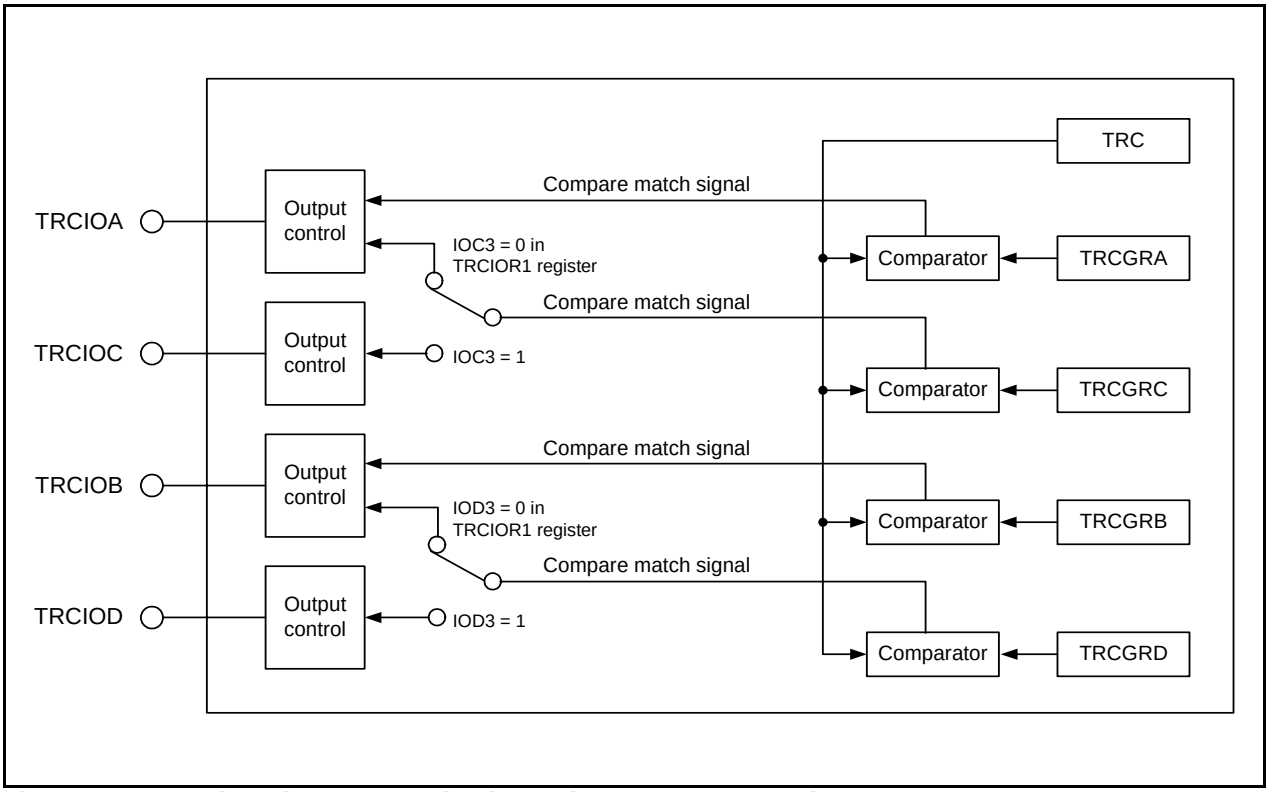
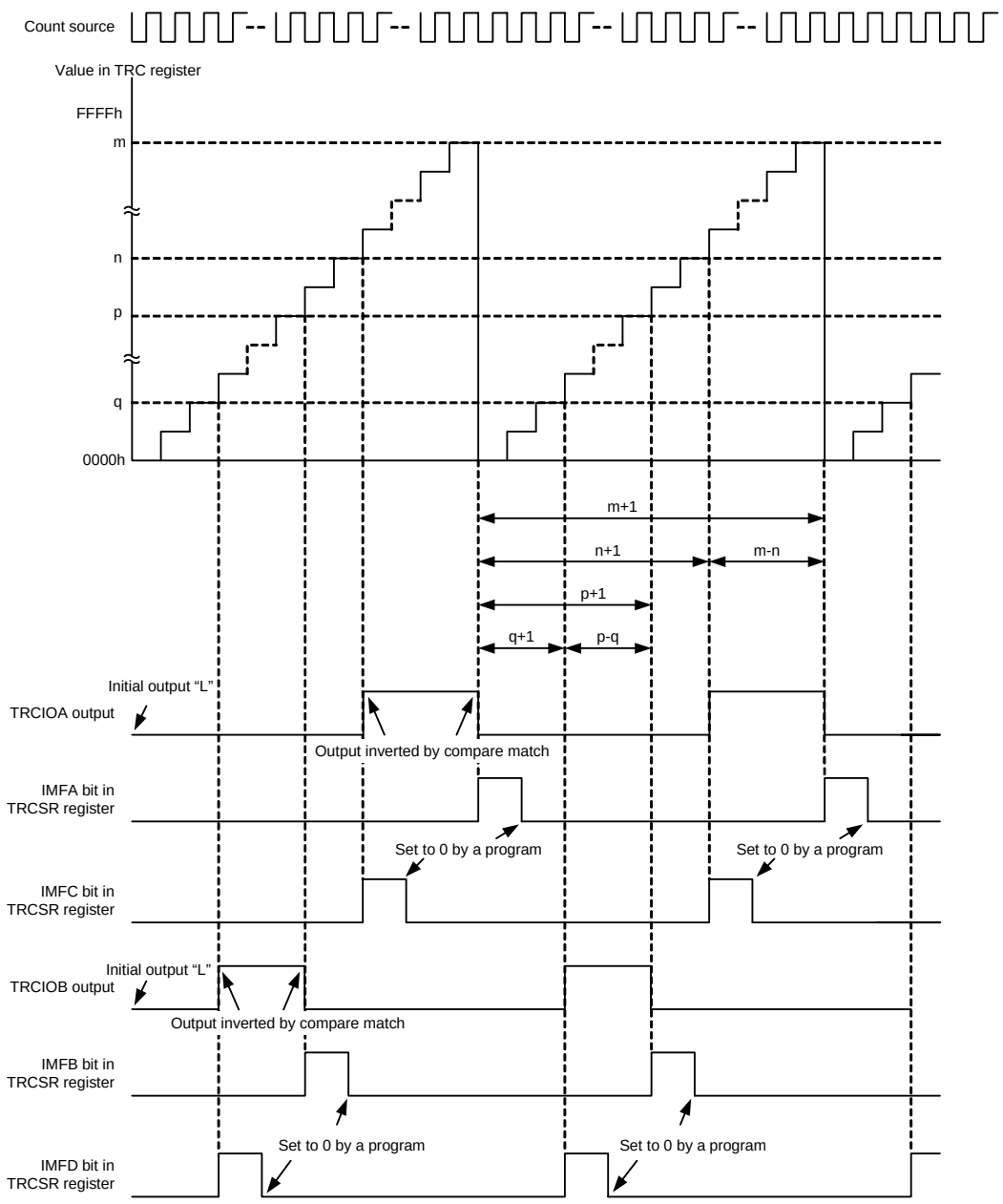


Figure 19.11 Changing Output Pins in Registers TRCGRC and TRCGRD



m: Value set in TRCGRA register
n: Value set in TRCGRC register
p: Value set in TRCGRB register
q: Value set in TRCGRD register

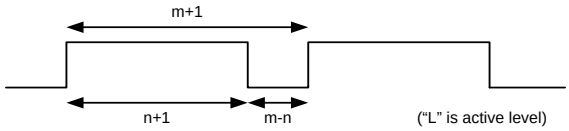
The above applies under the following conditions:
- Bits BFC and BFD in the TRCMR register are set to 0 (registers TRCGRC and TRCGRD are not used as buffer register).
- Bits EA and EB in the TRCOER register are set to 0 (enable TRCIOA and TRCIOB pin outputs).
- The CCLR bit in the TRCCR1 register are set to 1 (set the TRC register to 0000h by compare match in the TRCGRA register).
- Bits TOA and TOB in the TRCCR1 register are set to 0 (initial output "L" to compare match).
- Bits IOA2 to IOA0 in the TRCIOR0 register are set to 011b (TRCIOA output inverted at TRCGRA register compare match).
- Bits IOB2 to IOB0 in the TRCIOR0 register are set to 011b (TRCIOB output inverted at TRCGRB register compare match).
- Bits IOC2 to IOC0 in the TRCIOR1 register are set to 011b (TRCIOA output inverted at TRCGRC register compare match).
- The IOC3 bit in the TRCIOR1 register are set to 0 (TRCIOA output register).
- Bits IOD2 to IOD0 in the TRCIOR1 register are set to 011b (TRCIOB output inverted at TRCGRD register compare match).
- The IOD3 bit in the TRCIOR1 register are set to 0 (TRCIOB output register).
- The CSEL bit in the TRCCR2 register are set to 0 (TRC continues counting after compare match).

Figure 19.12 Operating Example When TRCGRC Register is Used for Output Control of TRCIOA Pin and TRCGRD Register is Used for Output Control of TRCIOB Pin

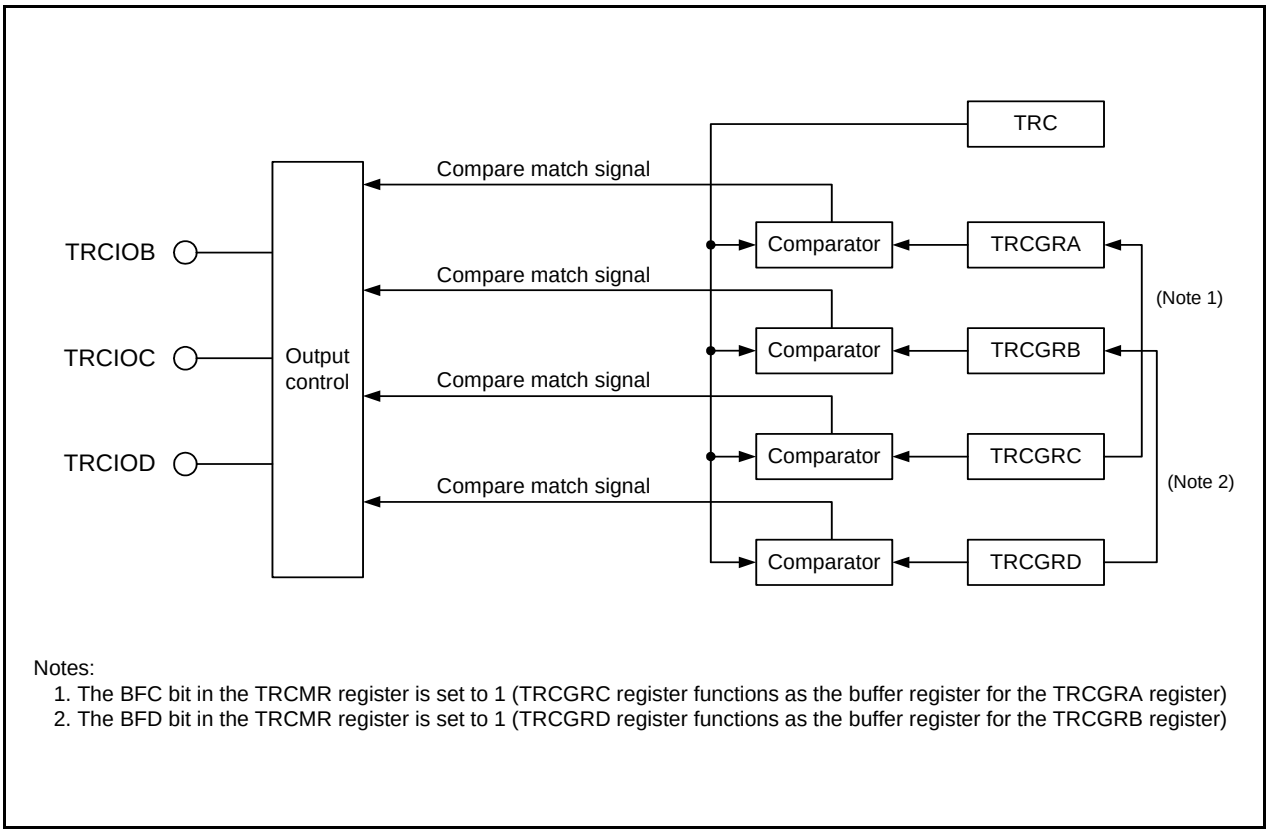
19.6 PWM Mode

This mode outputs PWM waveforms. A maximum of three PWM waveforms with the same period are output. The PWM mode, or the timer mode, can be selected for each individual pin. (However, since the TRCGRA register is used when using any pin for the PWM mode, the TRCGRA register cannot be used for the timer mode.)
Table 19.11 lists the Specifications of PWM Mode, Figure 19.13 shows a PWM Mode Block Diagram, Table 19.12 lists the Functions of TRCGRh Register in PWM Mode, and Figures 19.14 and 19.15 show Operating Examples of PWM Mode.

Table 19.11 Specifications of PWM Mode

Item	Specification
Count source	f1, f2, f4, f8, f32, fOCO40M, fOCO-F, or external signal (rising edge) input to TRCCLK pin
Count operation	Increment
PWM waveform	PWM period: 1/fk × (m + 1) Active level width: 1/fk × (m - n) Inactive width: 1/fk × (n + 1) fk: Count source frequency m: TRCGRA register setting value n: TRCGRj register setting value 
Count start condition	1 (count starts) is written to the TSTART bit in the TRCMR register.
Count stop condition	• When the CSEL bit in the TRCCR2 register is set to 0 (count continues after compare match with TRCGRA). 0 (count stops) is written to the TSTART bit in the TRCMR register. PWM output pin retains output level before count stops, TRC register retains value before count stops. • When the CSEL bit in the TRCCR2 register is set to 1 (count stops at compare match with TRCGRA register). The count stops at the compare match with the TRCGRA register. The PWM output pin retains the level after the output is changed by the compare match.
Interrupt request generation timing	• Compare match (contents of registers TRC and TRCGRh match) • The TRC register overflows.
TRCIOA pin function	Programmable I/O port
TRCIOB, TRCIOC, and TRCIOD pin functions	Programmable I/O port or PWM output (selectable individually for each pin)
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRC register.
Write to timer	The TRC register can be written to.
Select functions	• One to three pins selectable as PWM pins One or more of pins TRCIOB, TRCIOC, and TRCIOD • Active level selectable for each pin • Initial level selectable for each pin • Buffer operation (Refer to **19.3.2 Buffer Operation**.) • Pulse output forced cutoff signal input (Refer to **19.3.4 Forced Cutoff of Pulse Output**.) • A/D trigger generation

j = B, C, or D
h = A, B, C, or D



Notes:
1. The BFC bit in the TRCMR register is set to 1 (TRCGRC register functions as the buffer register for the TRCGRA register)
2. The BFD bit in the TRCMR register is set to 1 (TRCGRD register functions as the buffer register for the TRCGRB register)

Figure 19.13 PWM Mode Block Diagram

19.6.1 Timer RC Control Register 1 (TRCCR1) in PWM Mode

Address 0121h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR	TCK2	TCK1	TCK0	TOD	TOC	TOB	TOA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA	TRCIOA output level select bit (1)	Disabled in PWM mode	R/W
b1	TOB	TRCIOB output level select bit (1, 2)	0: Initial output selected as non-active level 1: Initial output selected as active level	R/W
b2	TOC	TRCIOC output level select bit (1, 2)		R/W
b3	TOD	TRCIOD output level select bit (1, 2)		R/W
b4	TCK0	Count source select bit (1)	b6 b5 b4 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRCCLK input rising edge 1 1 0: fOCO40M 1 1 1: fOCO-F (3)	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	CCLR	TRC counter clear select bit	0: Disable clear (free-running operation) 1: Clear by compare match in the TRCGRA register	R/W

Notes:
1. Set to these bits when the TSTART bit in the TRCMR register is set to 0 (count stops).
2. If the pin function is set for waveform output (refer to **7.5 Port Settings**), the initial output level is output when the TRCCR1 register is set.
3. To select fOCO-F, set it to the clock frequency higher than the CPU clock frequency.

19.6.2 Timer RC Control Register 2 (TRCCR2) in PWM Mode

Address 0130h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCEG1	TCEG0	CSEL	—	—	POLD	POLC	POLB
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POLB	PWM mode output level control bit B (1)	0: TRCIOB output level selected as “L” active 1: TRCIOB output level selected as “H” active	R/W
b1	POLC	PWM mode output level control bit C (1)	0: TRCIOC output level selected as “L” active 1: TRCIOC output level selected as “H” active	R/W
b2	POLD	PWM mode output level control bit D (1)	0: TRCIOD output level selected as “L” active 1: TRCIOD output level selected as “H” active	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b4	—			
b5	CSEL	TRC count operation select bit (2)	0: Count continues at compare match with the TRCGRA register 1: Count stops at compare match with the TRCGRA register	R/W
b6	TCEG0	TRCTRG input edge select bit (3)	b7 b6 0 0: Disable the trigger input from the TRCTRG pin 0 1: Rising edge selected 1 0: Falling edge selected 1 1: Both edges selected	R/W
b7	TCEG1			R/W

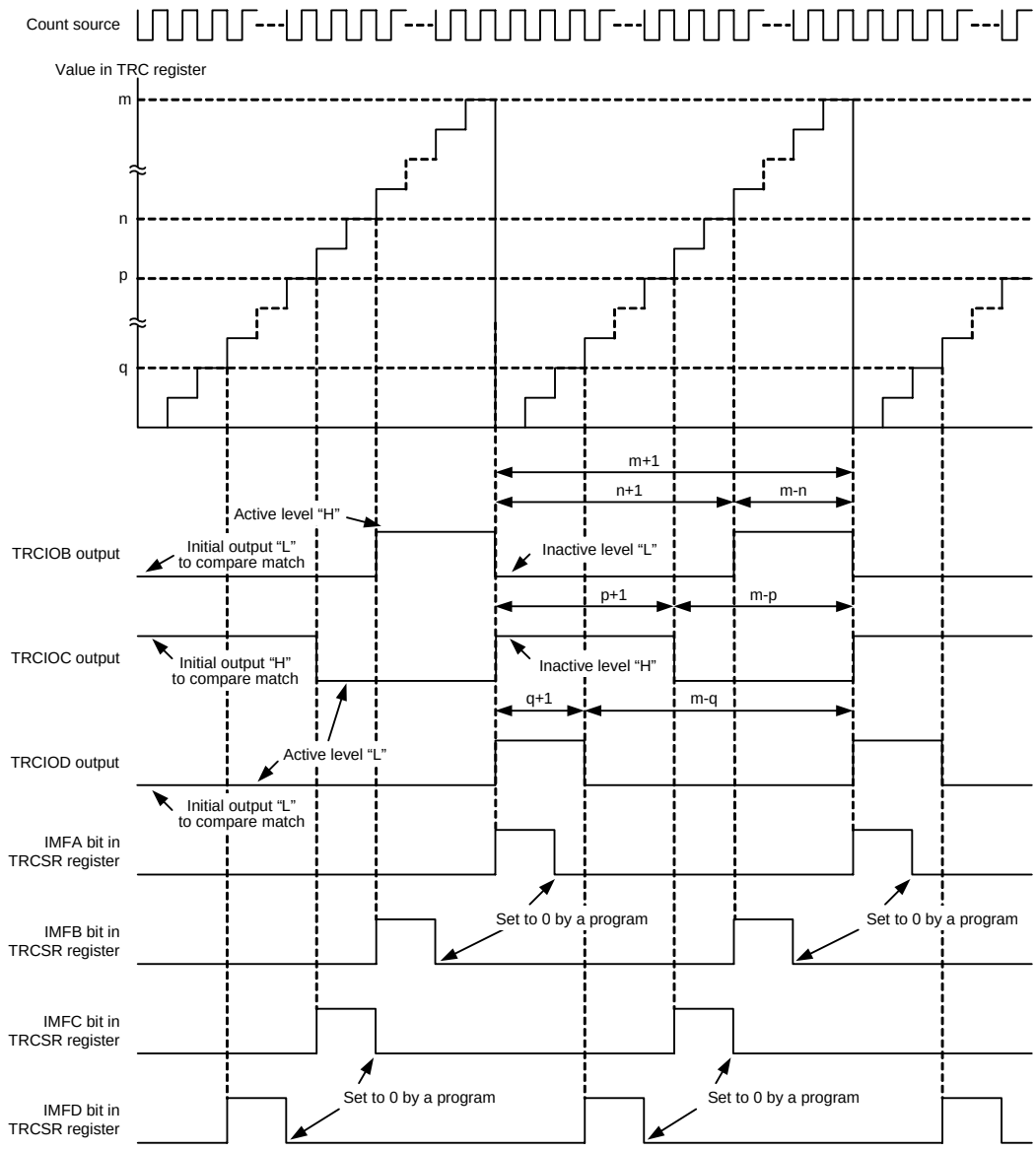
Notes:
1. Enabled when in PWM mode.
2. Enabled when in output compare function, PWM mode, or PWM2 mode. For notes on PWM2 mode, refer to **19.9.6 TRCMR Register in PWM2 Mode**
3. Enabled when in PWM2 mode.

Table 19.12 Functions of TRCGRh Register in PWM Mode

Register	Setting	Register Function	PWM Output Pin
TRCGRA	–	General register. Set the PWM period.	–
TRCGRB	–	General register. Set the PWM output change point.	TRCIOB
TRCGRC	BFC = 0	General register. Set the PWM output change point.	TRCIOC
TRCGRD	BFD = 0		TRCIOD
TRCGRC	BFC = 1	Buffer register. Set the next PWM period. (Refer to **19.3.2 Buffer Operation**.)	–
TRCGRD	BFD = 1	Buffer register. Set the next PWM output change point. (Refer to **19.3.2 Buffer Operation**.)	TRCIOB

h = A, B, C, or D
BFC, BFD: Bits in TRCMR register
Note:
1. The output level does not change even when a compare match occurs if the TRCGRA register value (PWM period) is the same as the TRCGRB, TRCGRC, or TRCGRD register value.

19.6.3 Operating Example



The above applies under the following conditions:
- Bits BFC and BFD in the TRCMR register are set to 0 (registers TRCGRC and TRCGRD do not operate as buffers).
- Bits EB, EC, and ED in the TRCOER register are set to 0 (output from TRCIOB, TRCIOC, and TRCIOD enabled).
- Bits TOB and TOC in the TRCCR1 register are set to 0 (inactive level), the TOD bit is set to 1 (active level).
- The POLB bit in the TRCCR2 register is set to 1 ("H" active), bits POLC and POLD are set to 0 ("L" active).

Figure 19.14 Operating Example of PWM Mode

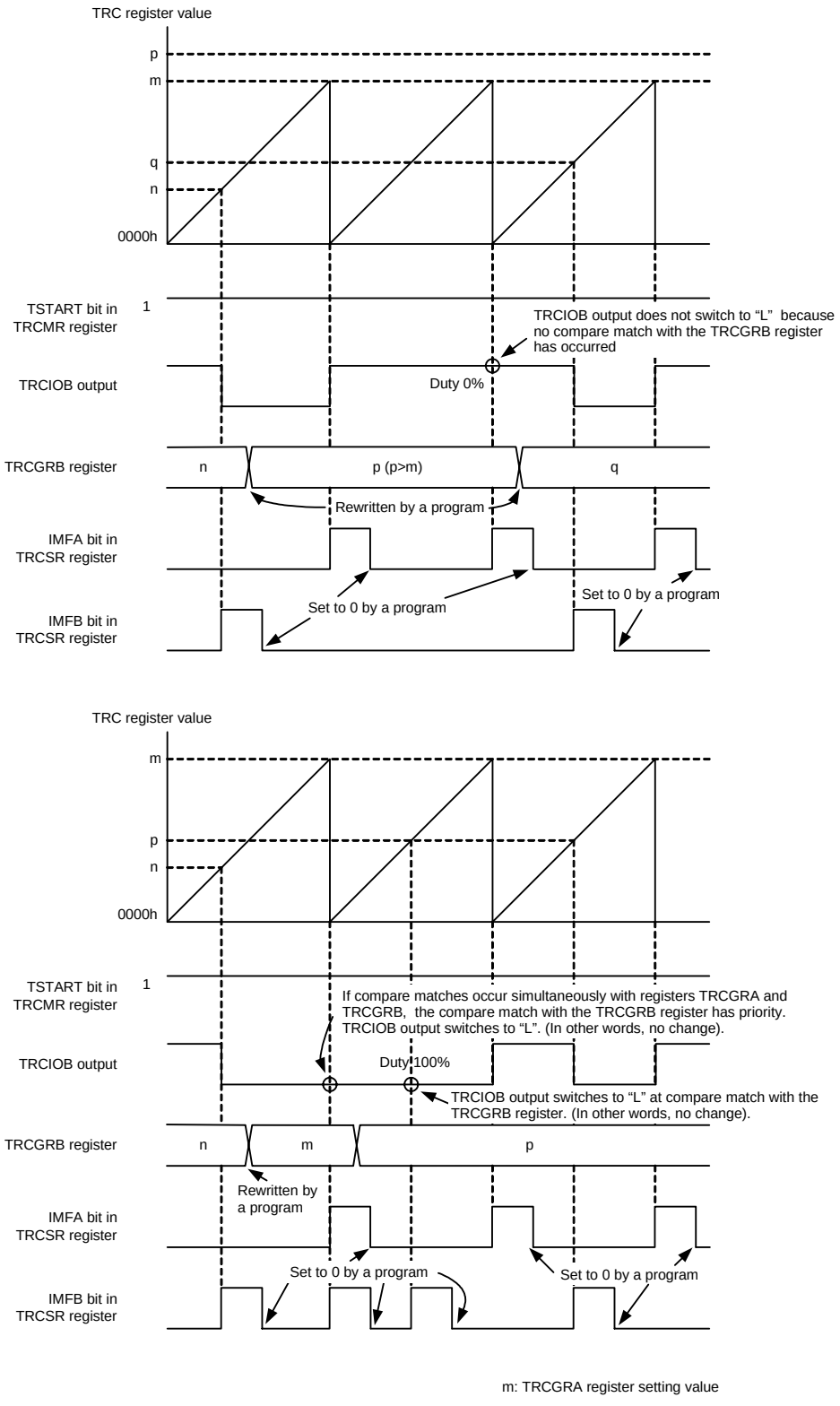
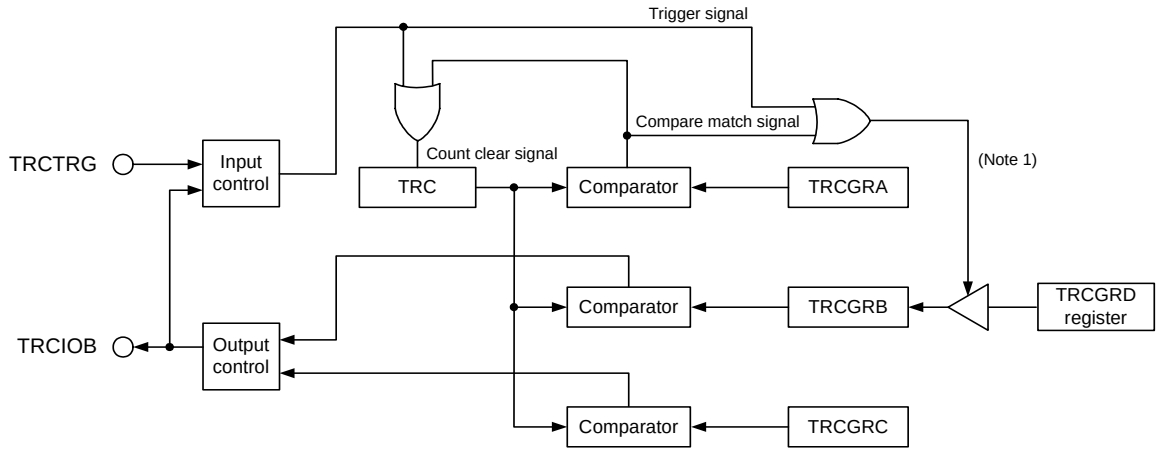


Figure 19.15 Operating Example of PWM Mode (Duty 0% and Duty 100%)

19.7 PWM2 Mode

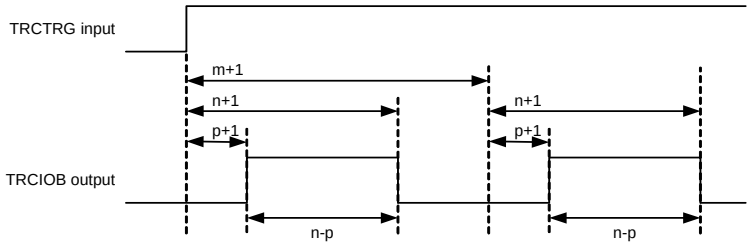
This mode outputs a single PWM waveform. After a given wait duration has elapsed following the trigger, the pin output switches to active level. Then, after a given duration, the output switches back to inactive level. Furthermore, the counter stops at the same time the output returns to inactive level, making it possible to use PWM2 mode to output a programmable wait one-shot waveform.
Since timer RC uses multiple general registers in PWM2 mode, other modes cannot be used in conjunction with it. Figure 19.16 shows a PWM2 Mode Block Diagram, Table 19.13 lists the Specifications of PWM2 Mode, Table 19.14 lists the Functions of TRCGRj Register in PWM2 Mode, and Figures 19.17 to 19.19 show Operating Examples of PWM2 Mode.



Note:
1. The BFD bit in the TRCMR register is set to 1 (the TRCGRD register functions as the buffer register for the TRCGRB register).

Figure 19.16 PWM2 Mode Block Diagram

Table 19.13 Specifications of PWM2 Mode

Item	Specification
Count source	f1, f2, f4, f8, f32, fOCO40M, fOCO-F, or external signal (rising edge) input to TRCCLK pin
Count operation	Increment TRC register
PWM waveform	PWM period: 1/fk × (m + 1) (no TRCTRG input) Active level width: 1/fk × (n - p) Wait time from count start or trigger: 1/fk × (p + 1) fk: Count source frequency m: TRCGRA register setting value n: TRCGRB register setting value p: TRCGRC register setting value  (TRCTRG: Rising edge, active level is “H”)
Count start conditions	• Bits TCEG1 to TCEG0 in the TRCCR2 register are set to 00b (TRCTRG trigger disabled) or the CSEL bit in the TRCCR2 register is set to 0 (count continues). 1 (count starts) is written to the TSTART bit in the TRCMR register. • Bits TCEG1 to TCEG0 in the TRCCR2 register are set to 01b, 10b, or 11b (TRCTRG trigger enabled) and the TSTART bit in the TRCMR register is set to 1 (count starts). A trigger is input to the TRCTRG pin
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRCMR register while the CSEL bit in the TRCCR2 register is set to 0 or 1. The TRCIOB pin outputs the initial level in accordance with the value of the TOB bit in the TRCCR1 register. The TRC register retains the value before count stops. • The count stops due to a compare match with TRCGRA while the CSEL bit in the TRCCR2 register is set to 1 The TRCIOB pin outputs the initial level. The TRC register retains the value before count stops if the CCLR bit in the TRCCR1 register is set to 0. The TRC register is set to 0000h if the CCLR bit in the TRCCR1 register is set to 1.
Interrupt request generation timing	• Compare match (contents of TRC and TRCGRj registers match) • The TRC register overflows
TRCIOA/TRCTRG pin function	Programmable I/O port or TRCTRG input
TRCIOB pin function	PWM output
TRCIOC and TRCIOD pin functions	Programmable I/O port
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRC register.
Write to timer	The TRC register can be written to.
Select functions	• External trigger and valid edge selection The edge or edges of the signal input to the TRCTRG pin can be used as the PWM output trigger: rising edge, falling edge, or both rising and falling edges • Buffer operation (Refer to **19.3.2 Buffer Operation**.) • Pulse output forced cutoff signal input (Refer to **19.3.4 Forced Cutoff of Pulse Output**.) • Digital filter (Refer to **19.3.3 Digital Filter**.) • A/D trigger generation

j = A, B, or C

19.7.1 Timer RC Control Register 1 (TRCCR1) in PWM2 Mode

Address 0121h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR	TCK2	TCK1	TCK0	TOD	TOC	TOB	TOA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA	TRCIOA output level select bit (1)	Disabled in PWM2 mode	R/W
b1	TOB	TRCIOB output level select bit (1, 2)	0: Active level “H” (Initial output “L” “H” output by compare match in the TRCGRC register “L” output by compare match in the TRCGRB register 1: Active level “L” (Initial output “H” “L” output by compare match in the TRCGRC register “H” output by compare match in the TRCGRB register	R/W
b2	TOC	TRCIOC output level select bit (1)	Disabled in PWM2 mode	R/W
b3	TOD	TRCIOD output level select bit (1)		R/W
b4	TCK0	Count source select bit (1)	b6 b5 b4 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRCCLK input rising edge 1 1 0: fOCO40M 1 1 1: fOCO-F (3)	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	CCLR	TRC counter clear select bit	0: Disable clear (free-running operation) 1: Clear by compare match in the TRCGRA register	R/W

Notes:
1. Set to these bits when the TSTART bit in the TRCMR register is set to 0 (count stops).
2. If the pin function is set for waveform output (refer to **7.5 Port Settings**), the initial output level is output when the TRCCR1 register is set.
3. To select fOCO-F, set it to the clock frequency higher than the CPU clock frequency.

19.7.2 Timer RC Control Register 2 (TRCCR2) in PWM2 Mode

Address 0130h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCEG1	TCEG0	CSEL	—	—	POLD	POLC	POLB
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POLB	PWM mode output level control bit B (1)	0: TRCIOB output level selected as “L” active 1: TRCIOB output level selected as “H” active	R/W
b1	POLC	PWM mode output level control bit C (1)	0: TRCIOC output level selected as “L” active 1: TRCIOC output level selected as “H” active	R/W
b2	POLD	PWM mode output level control bit D (1)	0: TRCIOD output level selected as “L” active 1: TRCIOD output level selected as “H” active	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b4	—			
b5	CSEL	TRC count operation select bit (2)	0: Count continues at compare match with the TRCGRA register 1: Count stops at compare match with the TRCGRA register	R/W
b6	TCEG0	TRCTRG input edge select bit (3)	b7 b6 0 0: Disable the trigger input from the TRCTRG pin 0 1: Rising edge selected 1 0: Falling edge selected 1 1: Both edges selected	R/W
b7	TCEG1			R/W

Notes:
1. Enabled when in PWM mode.
2. Enabled when in output compare function, PWM mode, or PWM2 mode. For notes on PWM2 mode, refer to **19.9.6 TRCMR Register in PWM2 Mode**.
3. Enabled when in PWM2 mode.

19.7.3 Timer RC Digital Filter Function Select Register (TRCDF) in PWM2 Mode

Address 0131h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DFCK1	DFCK0	—	DFTRG	DFD	DFC	DFB	DFA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DFA	TRCIOA pin digital filter function select bit (1)	0: Function is not used 1: Function is used	R/W
b1	DFB	TRCIOB pin digital filter function select bit (1)		R/W
b2	DFC	TRCIOC pin digital filter function select bit (1)		R/W
b3	DFD	TRCIOD pin digital filter function select bit (1)		R/W
b4	DFTRG	TRCTRG pin digital filter function select bit (2)		R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	DFCK0	Clock select bits for digital filter function (1, 2)	b7 b6 0 0: f32 0 1: f8 1 0: f1 1 1: Count source (clock selected by bits TCK2 to TCK0 in the TRCCR1 register)	R/W
b7	DFCK1			R/W

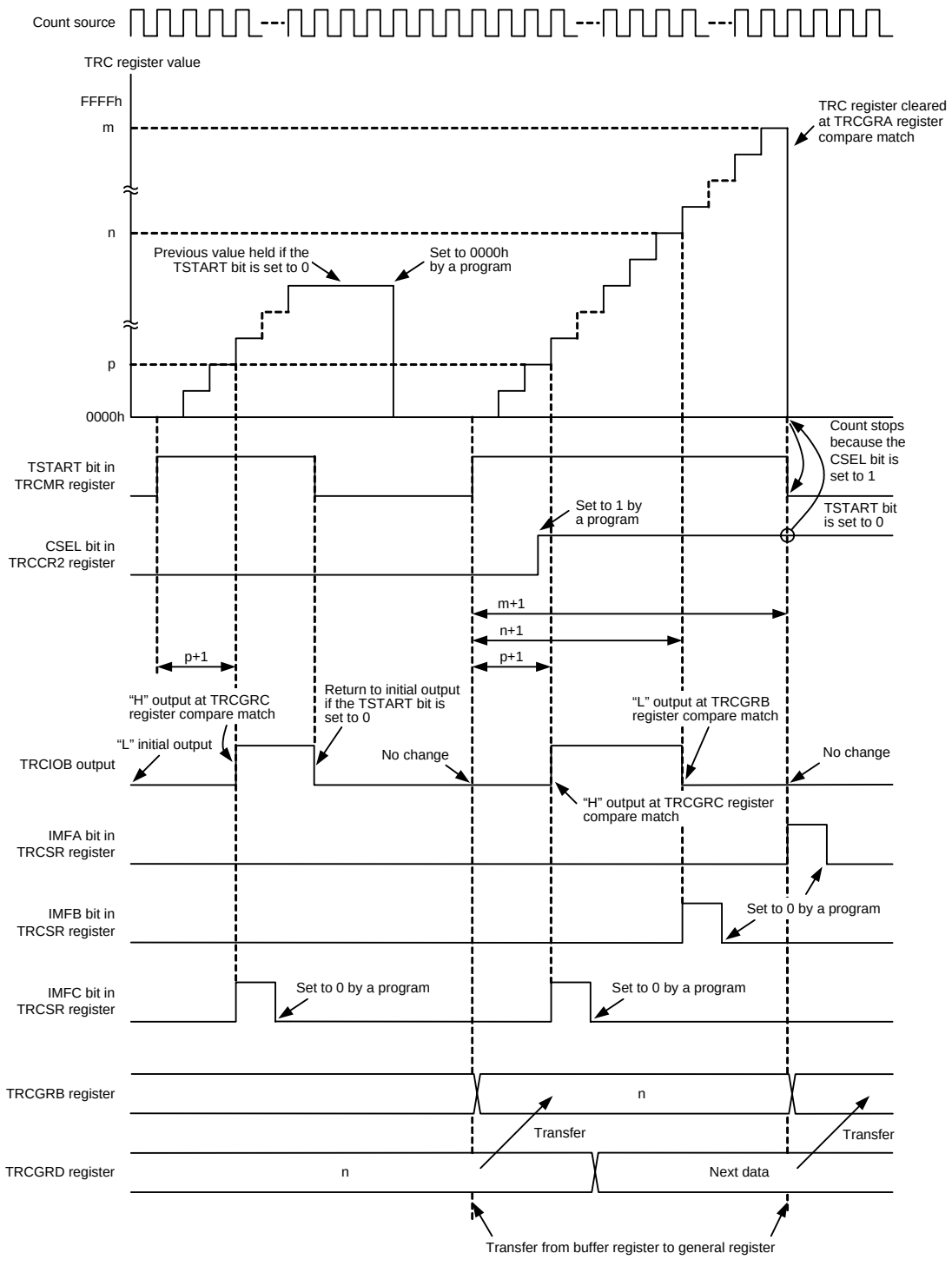
Notes:
1. These bits are enabled for the input capture function.
2. These bits are enabled when in PWM2 mode and bits TCEG1 to TCEG0 in the TRCCR2 register are set to 01b, 10b, or 11b (TRCTRG trigger input enabled).

Table 19.14 Functions of TRCGRj Register in PWM2 Mode

Register	Setting	Register Function	PWM2 Output Pin
TRCGRA	–	General register. Set the PWM period.	TRCIOB pin
TRCGRB (1)	–	General register. Set the PWM output change point.	
TRCGRC (1)	BFC = 0	General register. Set the PWM output change point (wait time after trigger).	
TRCGRD	BFD = 0	(Not used in PWM2 mode)	–
TRCGRD	BFD = 1	Buffer register. Set the next PWM output change point. (Refer to **19.3.2 Buffer Operation**.)	TRCIOB pin

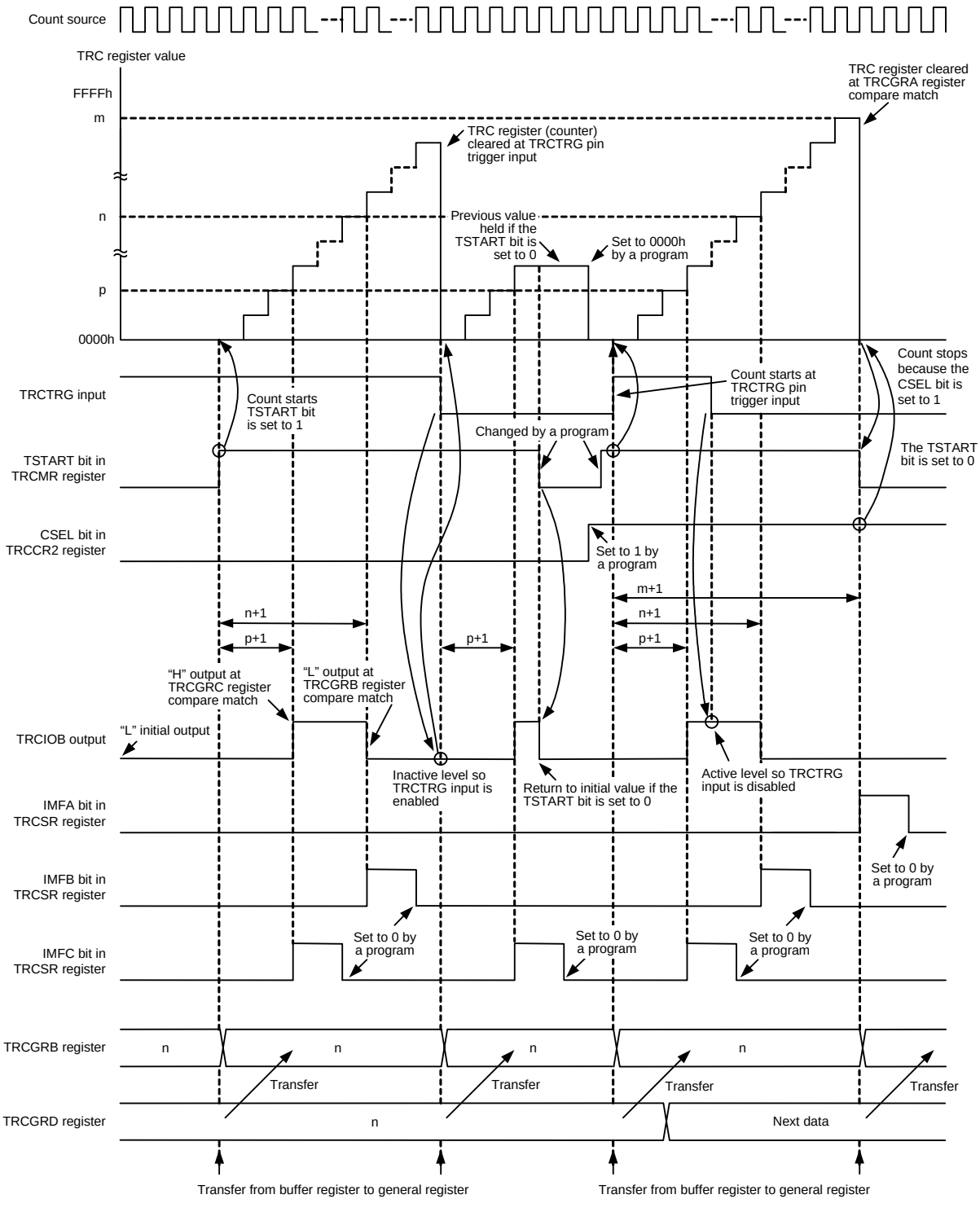
j = A, B, C, or D
BFC, BFD: Bits in TRCMR register
Note:
1. Do not set the TRCGRB and TRCGRC registers to the same value.

19.7.4 Operating Example



The above applies under the following conditions:
- The TOB bit in the TRCCR1 register is set to 0 (initial level is "L", "H" output at compare match with the TRCGRC register, "L" output at compare match with the TRCGRB register).
- Bits TCEG1 and TCEG0 in the TRCCR2 register are set to 00b (TRCTRG trigger input disabled).

Figure 19.17 Operating Example of PWM2 Mode (TRCTRG Trigger Input Disabled)



The above applies under the following conditions:
- The TOB bit in the TRCCR1 register is set to 0 (initial level is "L", "H" output at compare match with the TRCGRC register, "L" output at compare match with the TRCGRB register).
- Bits TCEG1 and TCEG0 in the TRCCR2 register are set to 11b (trigger at both rising and falling edges of TRCTRG input).

Figure 19.18 Operating Example of PWM2 Mode (TRCTRG Trigger Input Enabled)

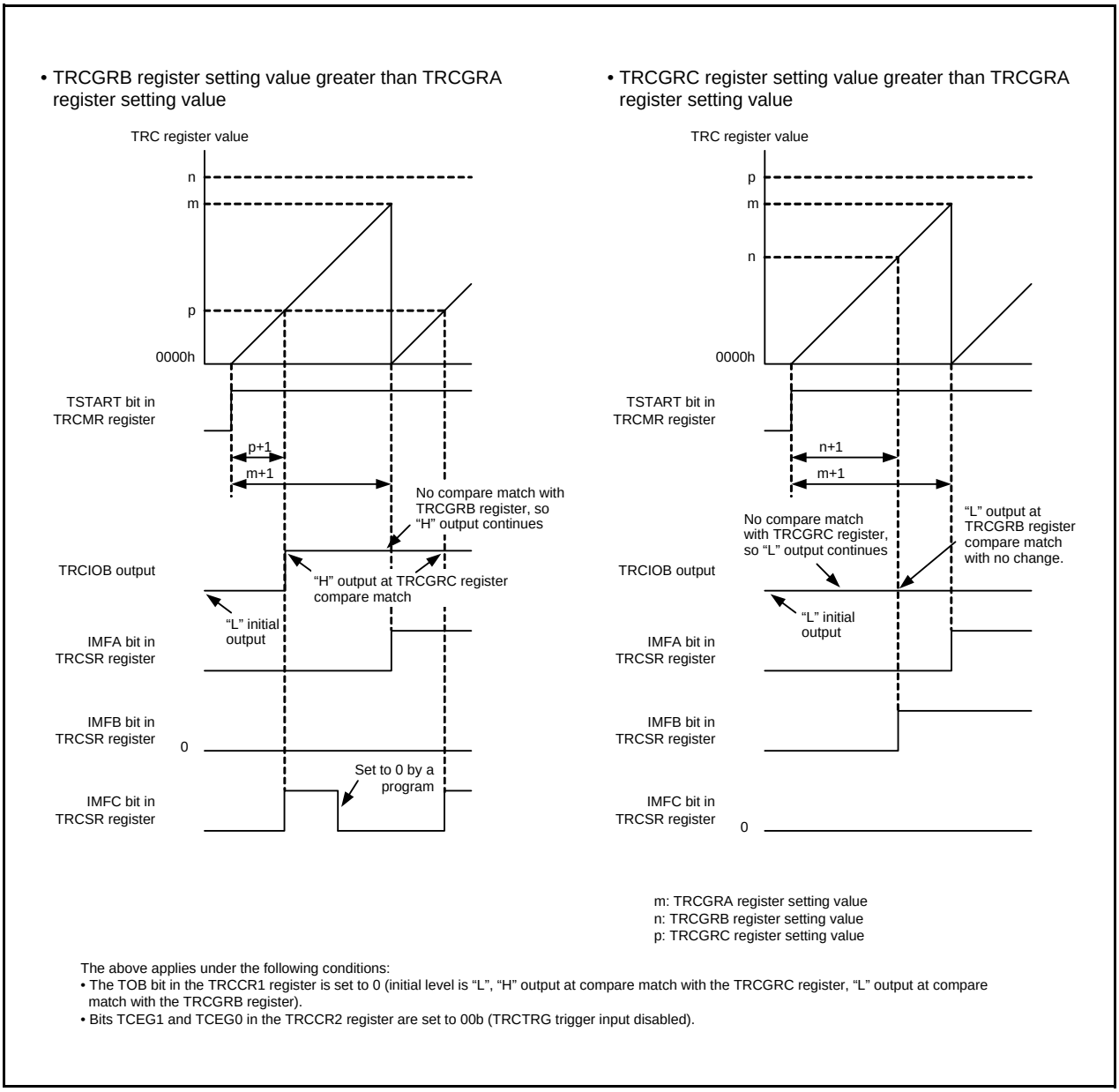


Figure 19.19 Operating Example of PWM2 Mode (Duty 0% and Duty 100%)

19.8 Timer RC Interrupt

Timer RC generates a timer RC interrupt request from five sources. The timer RC interrupt uses the single TRCIC register (bits IR and ILVL0 to ILVL2) and a single vector.
Table 19.15 lists the Registers Associated with Timer RC Interrupt, and Figure 19.20 is a Timer RC Interrupt Block Diagram.

Table 19.15 Registers Associated with Timer RC Interrupt

Timer RC Status Register	Timer RC Interrupt Enable Register	Timer RC Interrupt Control Register
TRCSR	TRCIER	TRCIC

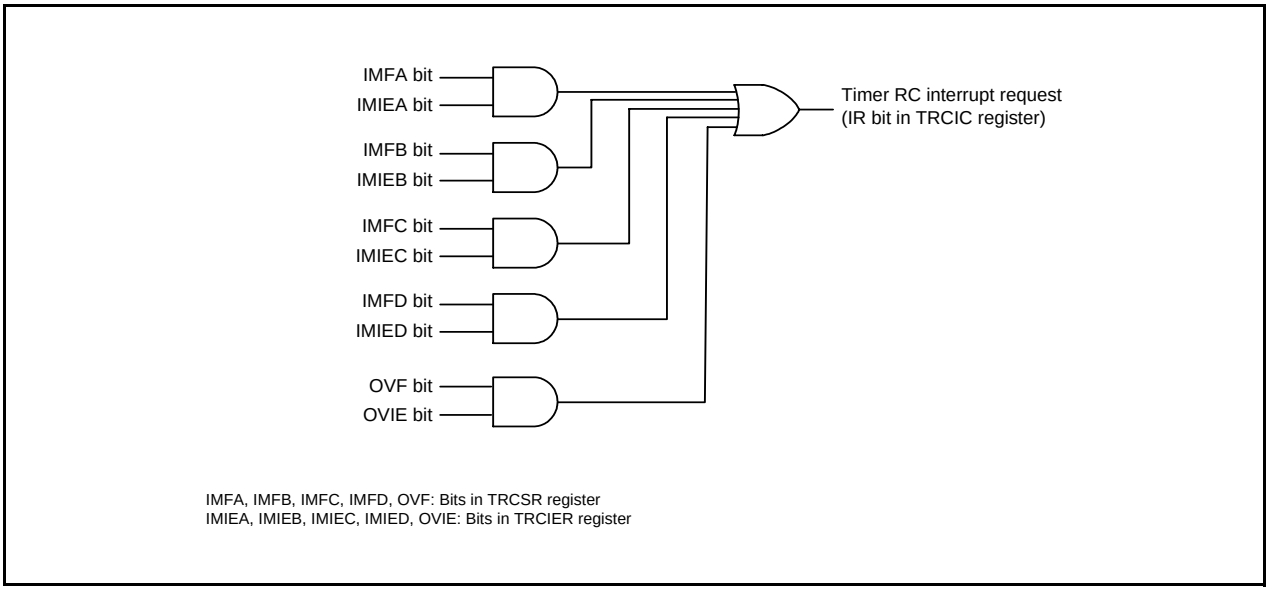


Figure 19.20 Timer RC Interrupt Block Diagram

Like other maskable interrupts, the timer RC interrupt is controlled by the combination of the I flag, IR bit, bits ILVL0 to ILVL2, and IPL. However, it differs from other maskable interrupts in the following respects because a single interrupt source (timer RC interrupt) is generated from multiple interrupt request sources.

- The IR bit in the TRCIC register is set to 1 (interrupt requested) when a bit in the TRCSR register is set to 1 and the corresponding bit in the TRCIER register is also set to 1 (interrupt enabled).
- The IR bit is set to 0 (no interrupt requested) when the bit in the TRCSR register or the corresponding bit in the TRCIER register is set to 0, or both are set to 0. In other words, the interrupt request is not maintained if the IR bit is once set to 1 but the interrupt is not acknowledged.
- If another interrupt source is triggered after the IR bit is set to 1, the IR bit remains set to 1 and does not change.
- If multiple bits in the TRCIER register are set to 1, use the TRCSR register to determine the source of the interrupt request.
- The bits in the TRCSR register are not automatically set to 0 when an interrupt is acknowledged. Set them to 0 within the interrupt routine. Refer to **19.2.5 Timer RC Status Register (TRCSR)**, for the procedure for setting these bits to 0.

Refer to **19.2.4 Timer RC Interrupt Enable Register (TRCIER)**, for details of the TRCIER register.
Refer to **11.3 Interrupt Control**, for details of the TRCIC register and **11.1.5.2 Relocatable Vector Tables**, for information on interrupt vectors.

19.9 Notes on Timer RC

19.9.1 TRC Register

- The following note applies when the CCLR bit in the TRCCR1 register is set to 1 (clear TRC register at compare match with TRCGRA register).
  When using a program to write a value to the TRC register while the TSTART bit in the TRCMR register is set to 1 (count starts), ensure that the write does not overlap with the timing with which the TRC register is set to 0000h.
  If the timing of the write to the TRC register and the setting of the TRC register to 0000h coincide, the write value will not be written to the TRC register and the TRC register will be set to 0000h.

- Reading from the TRC register immediately after writing to it can result in the value previous to the write being read out. To prevent this, execute the JMP.B instruction between the read and the write instructions.

```
Program Example     MOV.W   #XXXXh, TRC    ;Write
                    JMP.B   L1             ;JMP.B instruction
                L1: MOV.W   TRC,DATA       ;Read
```

19.9.2 TRCSR Register

Reading from the TRCSR register immediately after writing to it can result in the value previous to the write being read out. To prevent this, execute the JMP.B instruction between the read and the write instructions.

```
Program Example     MOV.B   #XXh, TRCSR    ;Write
                    JMP.B   L1             ;JMP.B instruction
                L1: MOV.B   TRCSR,DATA     ;Read
```

19.9.3 TRCCR1 Register

To set bits TCK2 to TCK0 in the TRCCR1 register to 111b (fOCO-F), set fOCO-F to the clock frequency higher than the CPU clock frequency.

19.9.4 Count Source Switching

- Stop the count before switching the count source.

Switching procedure
(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.

- When changing the count source from fOCO40M to another clock other than fOCO-F and stopping fOCO40M, wait 2 cycles of f1 or more after setting the clock switch, and then stop fOCO40M.

Switching procedure
(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change bits TCK2 to TCK0 in the TRCCR1 register.
(3) Wait 2 or more cycles of f1.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

- After switching the count source from fOCO-F to a clock other than fOCO40M, allow a minimum of one cycle of fOCO-F + fOCO40M to elapse after changing the clock setting before stopping fOCO-F.

Switching procedure

(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.
(3) Wait for a minimum of one cycle of fOCO-F + fOCO40M.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

19.9.5 Input Capture Function

- Set the pulse width of the input capture signal as follows:
  [When the digital filter is not used]
  Three or more cycles of the timer RC operation clock (refer to **Table 19.1 Timer RC Operation Clock**)
  [When the digital filter is used]
  Five cycles of the digital filter sampling clock + three cycles of the timer RC operating clock, minimum (refer to **Figure 19.5 Digital Filter Block Diagram**)
- The value of the TRC register is transferred to the TRCGRj register one or two cycles of the timer RC operation clock after the input capture signal is input to the TRCIOj (j = A, B, C, or D) pin (when the digital filter function is not used).

19.9.6 TRCMR Register in PWM2 Mode

When the CSEL bit in the TRCCR2 register is set to 1 (count stops at compare match with the TRCGRA register), do not set the TRCMR register at compare match timing of registers TRC and TRCGRA.

20. Timer RD

Timer RD has 2 16-bit timers (timer RD0 and RD1).

20.1 Overview

Each timer RDi (i = 0 or 1) has 4 I/O pins.
The operation clock of timer RD is f1, fOCO40M or fOCO-F. Table 20.1 lists the Timer RD Operation Clocks.

Table 20.1 Timer RD Operation Clocks

Condition	Operation Clock of Timer RD
The count source is f1, f2, f4, f8, f32, or TRDCLK input (bits TCK2 to TCK0 in registers TRDCR0 and TRDCR1 are set to a value from 000b to 101b).	f1
The count source is fOCO40M (bits TCK2 to TCK0 in registers TRDCR0 and TRDCR1 are set to 110b).	fOCO40M
The count source is fOCO-F (bits TCK2 to TCK0 in registers TRDCR0 and TRDCR1 are set to 111b).	fOCO-F

Figure 20.1 shows a Timer RD Block Diagram, and Table 20.2 lists the Pin Configuration of Timer RD.
Timer RD has 5 modes:

- Timer mode
  - Input capture function — Transfer the counter value to a register with an external signal as the trigger
  - Output compare function — Detect register value matches with a counter (Pin output can be changed at detection)

The following 4 modes use the output compare function.

- PWM mode — Output pulse of any width continuously
- Reset synchronous PWM mode — Output three-phase waveforms (6) without sawtooth wave modulation and dead time
- Complementary PWM mode — Output three-phase waveforms (6) with triangular wave modulation and dead time
- PWM3 mode — Output PWM waveforms (2) with a fixed period

In the input capture function, output compare function, and PWM mode, timer RD0 and timer RD1 have the equivalent functions, and functions or modes can be selected individually for each pin. Also, a combination of these functions and modes can be used in each timer RDi.
In reset synchronous PWM mode, complementary PWM mode, and PWM3 mode, a waveform is output with a combination of counters and registers in timer RD0 and timer RD1.

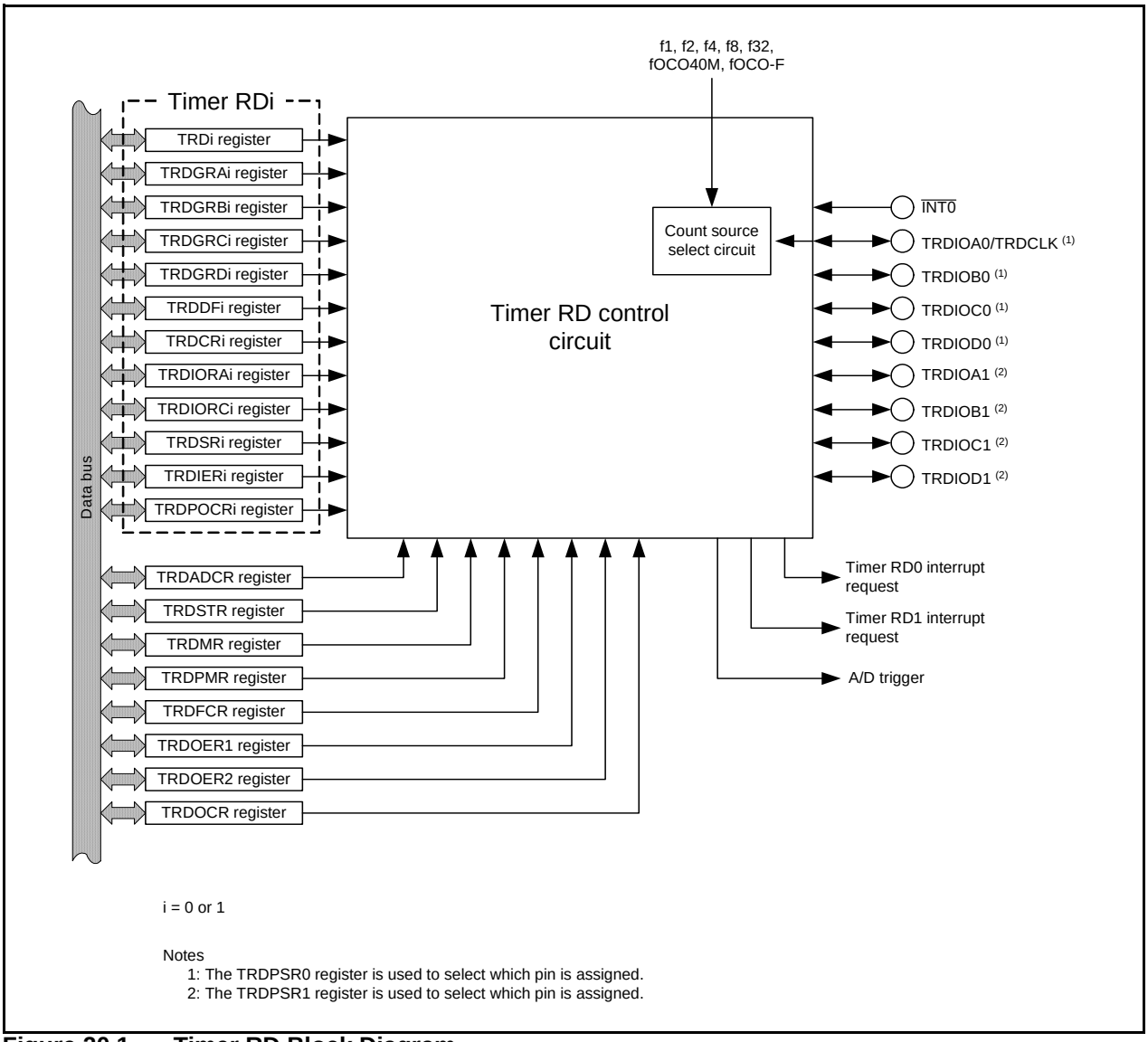


Figure 20.1 Timer RD Block Diagram

Table 20.2 Pin Configuration of Timer RD

Pin Name	Assigned Pin	I/O	Function
TRDIOA0/TRDCLK	P2_0	I/O	Function varies according to the mode. Refer to descriptions of individual modes for details.
TRDIOB0	P2_1	I/O	
TRDIOC0	P2_2	I/O	
TRDIOD0	P2_3	I/O	
TRDIOA1	P2_4	I/O	
TRDIOB1	P2_5	I/O	
TRDIOC1	P2_6	I/O	
TRDIOD1	P2_7	I/O	

20.2 Common Items for Multiple Modes

20.2.1 Count Sources

The count source selection method is the same in all modes. However, the external clock cannot be selected in PWM3 mode.

Table 20.3 Count Source Selection

Count Source	Selection
f1, f2, f4, f8, f32	The count source is selected by bits TCK2 to TCK0 in the TRDCRi register.
fOCO40M fOCO-F	The FRA00 bit in the FRA0 register is set to 1 (high-speed on-chip oscillator frequency). Bits TCK2 to TCK0 in the TRDCRi register is set to 110b (fOCO40M). Bits TCK2 to TCK0 in the TRDCRi register is set to 111b (fOCO-F).
External signal input to TRDCLK pin	The STCLK bit in the TRDFCR register is set to 1 (external clock input enabled). Bits TCK2 to TCK0 in the TRDCRi register are set to 101b (count source: external clock). The valid edge is selected by bits CKEG1 to CKEG0 in the TRDCRi register. The PD2_0 bit in the PD2 register is set to 0 (input mode).

i = 0 or 1

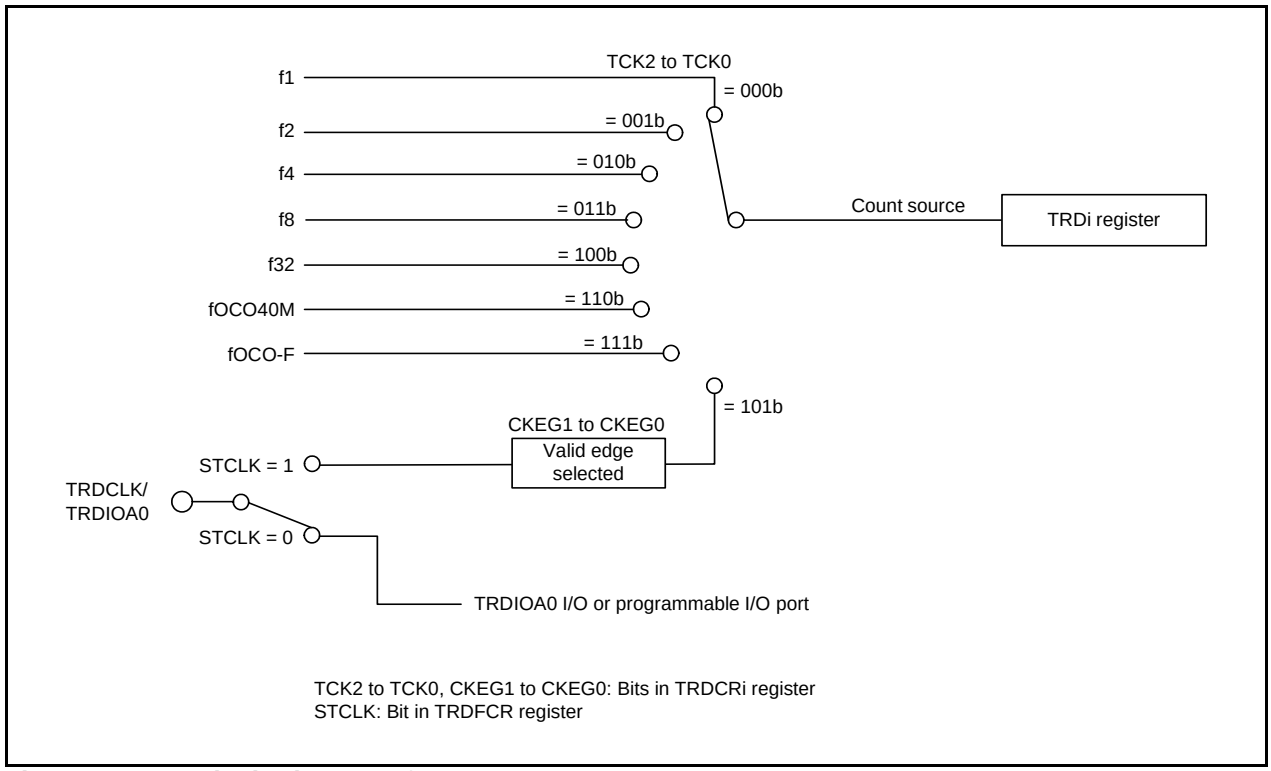


Figure 20.2 Block Diagram of Count Source

Set the pulse width of the external clock which inputs to the TRDCLK pin to 3 cycles or above of the operation clock of timer RD (refer to **Table 20.1 Timer RD Operation Clocks**).
When selecting fOCO40M or fOCO-F for the count source, set the FRA00 bit in the FRA0 register to 1 (high-speed on-chip oscillator on) before setting bits TCK2 to TCK0 in the TRDCRi register (i = 0 or 1) to 110b (fOCO40M) or 111b (fOCO-F).

20.2.2 Buffer Operation

The TRDGRCi (i = 0 or 1) register can be used as the buffer register of the TRDGRAi register, and the TRDGRDi register can be used as the buffer register of the TRDGRBi register by means of bits BFCi and BFDi in the TRDMR register.

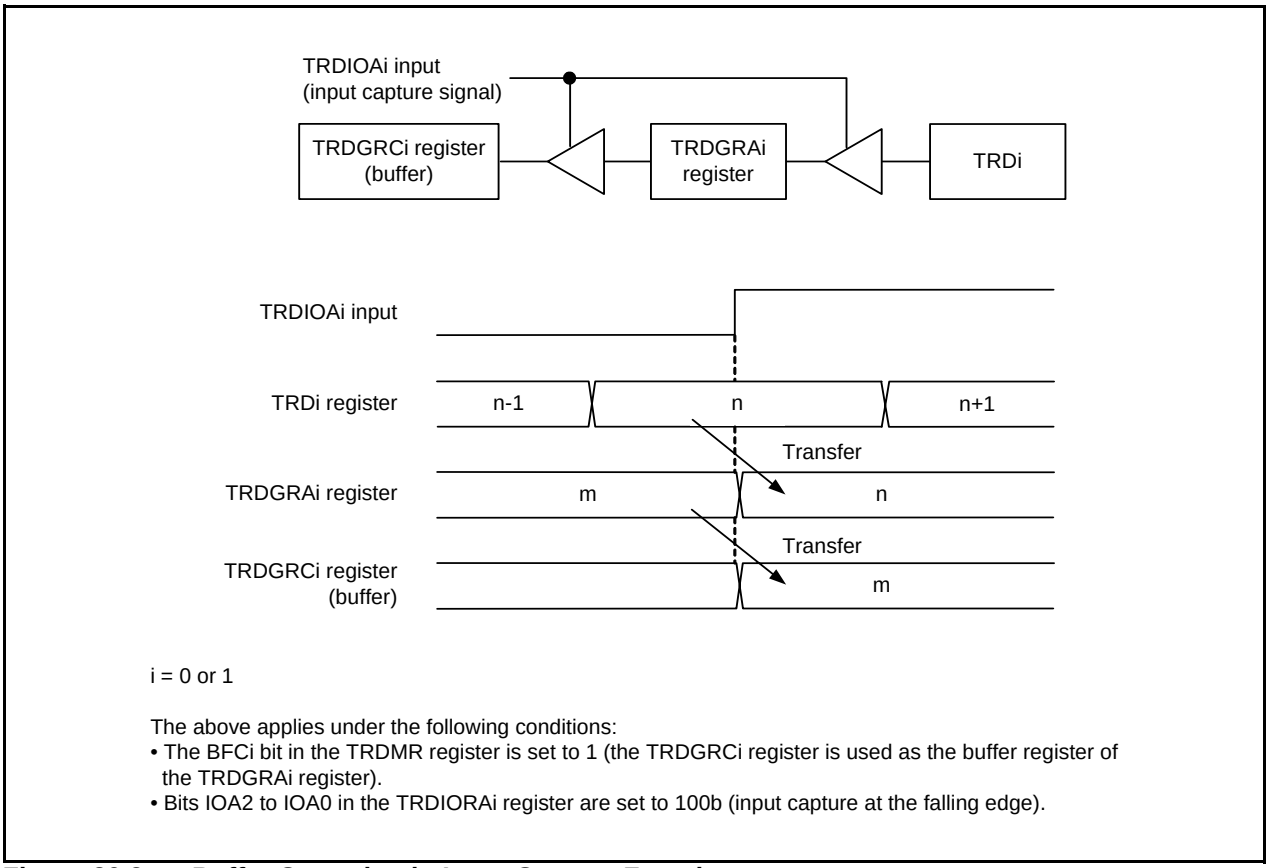
- TRDGRAi buffer register: TRDGRCi register
- TRDGRBi buffer register: TRDGRDi register

Buffer operation depends on the mode. Table 20.4 lists the Buffer Operation in Each Mode.

Table 20.4 Buffer Operation in Each Mode

Function and Mode	Transfer Timing	Transfer Register
Input capture function	Input capture signal input	Transfer content in TRDGRAi (TRDGRBi) register to buffer register
Output compare function PWM mode	Compare match with TRDi register and TRDGRAi (TRDGRBi) register	Transfer content in buffer register to TRDGRAi (TRDGRBi) register
Reset synchronous PWM mode	Compare match withTRD0 register and TRDGRA0 register	Transfer content in buffer register to TRDGRAi (TRDGRBi) register
Complementary PWM mode	• Compare match with TRD0 register and TRDGRA0 register • TRD1 register underflow	Transfer content in buffer register to registers TRDGRB0, TRDGRA1, and TRDGRB1
PWM3 mode	Compare match with TRD0 register and TRDGRA0 register	Transfer content in buffer register to registers TRDGRA0, TRDGRB0, TRDGRA1, and TRDGRB1

i = 0 or 1



i = 0 or 1

The above applies under the following conditions:
- The BFCi bit in the TRDMR register is set to 1 (the TRDGRCi register is used as the buffer register of the TRDGRAi register).
- Bits IOA2 to IOA0 in the TRDIORAi register are set to 100b (input capture at the falling edge).

Figure 20.3 Buffer Operation in Input Capture Function

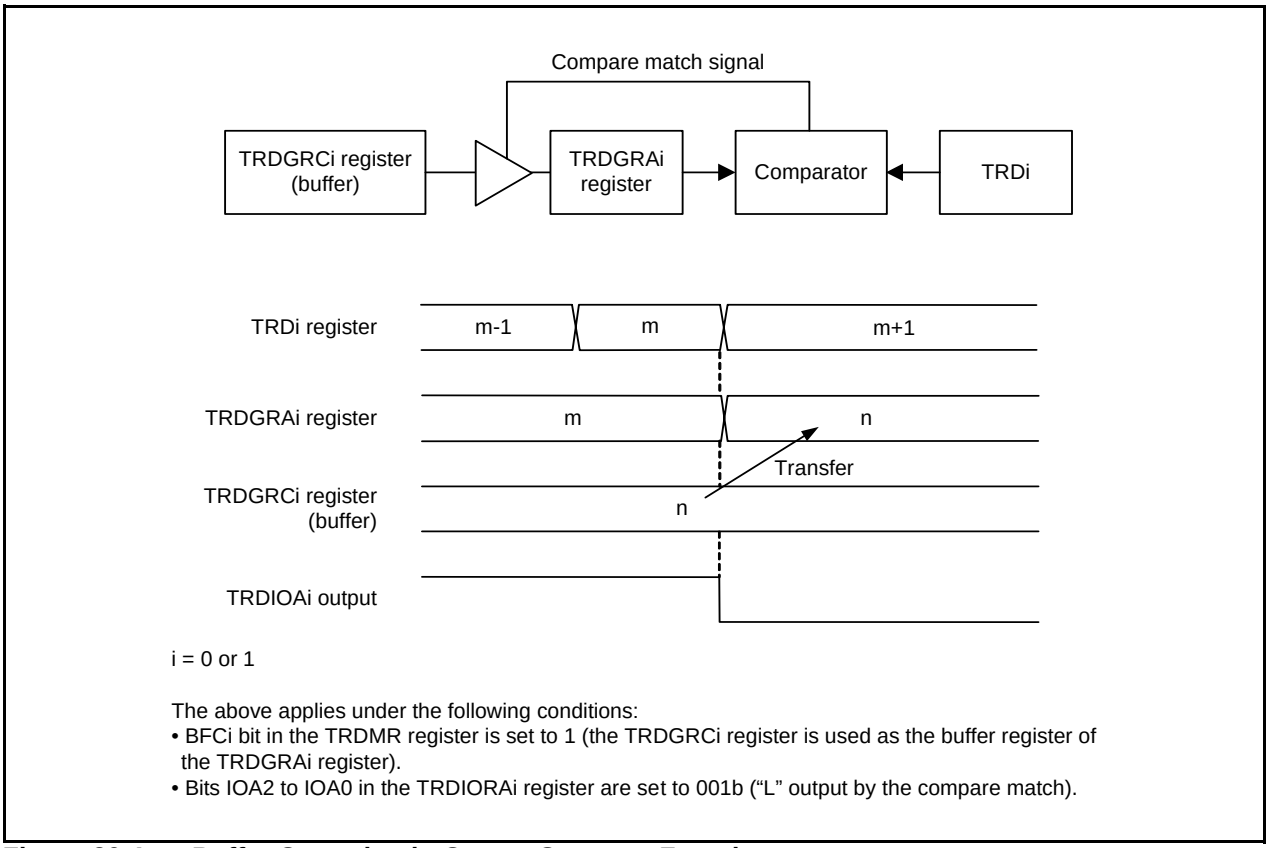


Figure 20.4 Buffer Operation in Output Compare Function

Perform the following for the timer mode (input capture and output compare functions).
When using the TRDGRCi (i = 0 or 1) register as the buffer register of the TRDGRAi register
- Set the IOC3 bit in the TRDIORCi register to 1 (general register or buffer register).
- Set the IOC2 bit in the TRDIORCi register to the same value as the IOA2 bit in the TRDIORAi register.

When using the TRDGRDi register as the buffer register of the TRDGRBi register
- Set the IOD3 bit in the TRDIORCi register to 1 (general register or buffer register).
- Set the IOD2 bit in the TRDIORCi register to the same value as the IOB2 bit in the TRDIORAi register.

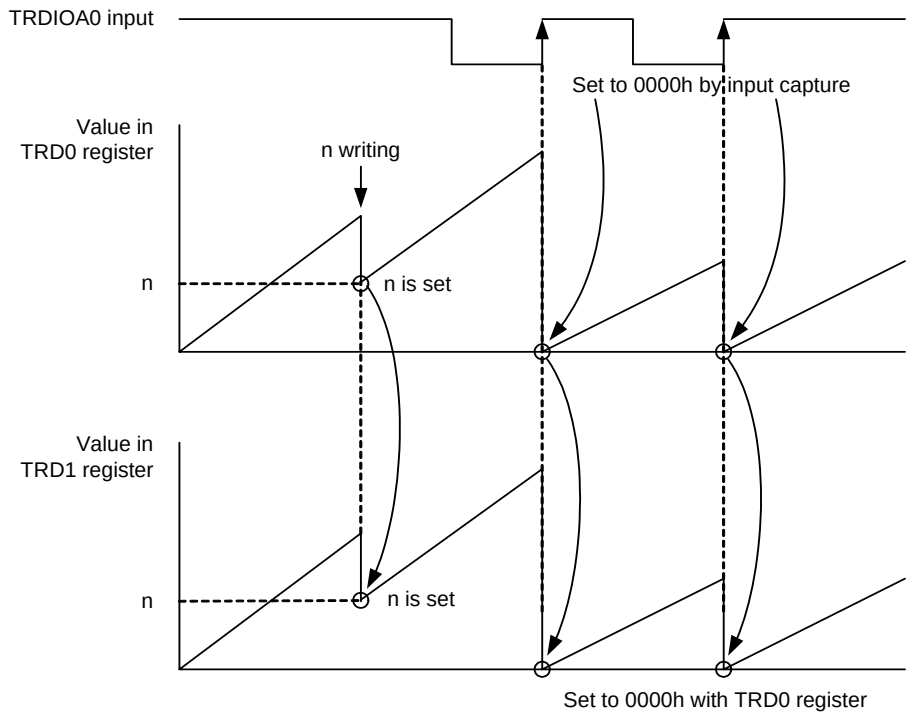
Bits IMFC and IMFD in the TRDSRi register are set to 1 at the input edge of the TRDIOCi pin when also using registers TRDGRCi and TRDGRDi as the buffer register in the input capture function.

When also using registers TRDGRCi and TRDGRDi as buffer registers for the output compare function, reset synchronous PWM mode, complementary PWM mode, and PWM3 mode, bits IMFC and IMFD in the TRDSRi register are set to 1 by a compare match with the TRDi register.

20.2.3 Synchronous Operation

The TRD1 register is synchronized with the TRD0 register.

- Synchronous preset
  When the SYNC bit in the TRDMR register is set to 1 (synchronous operation), the data is written to both the TRD0 and TRD1 registers after writing to the TRDi register.
- Synchronous clear
  When the SYNC bit in the TRDMR register is set to 1 and bits CCLR2 to CCLR0 in the TRDCRi register are set to 011b (synchronous clear), the TRD0 register is set to 0000h at the same time as the TRD1 register is set to 0000h.
  Also, when the SYNC bit in the TRDMR register is set to 1 and bits CCLR2 to CCLR0 in the TRDCRi register are set to 011b (synchronous clear), the TRD1 register is set to 0000h at the same time as the TRD0 register is set to 0000h.



The above applies under the following conditions:

- The SYNC bit in the TRDMR register is set to 1 (synchronous operation).
- Bits CCLR2 to CCLR0 in the TRDCR0 register are set to 001b (set the TRD0 register to 0000h in input capture).
  Bits CCLR2 to CCLR0 in the TRDCR1 register are set to 011b (set the TRD1 register to 0000h synchronizing with the TRD0 register).
- Bits IOA2 to IOA0 in the TRDIORA0 register are set to 100b.
- Bits CMD1 to CMD0 in the TRDFCR register are set to 00b.
  The PWM 3 bit in the TRDFCR register is set to 1.

} (Input capture at the rising edge of the TRDIOA0 input)

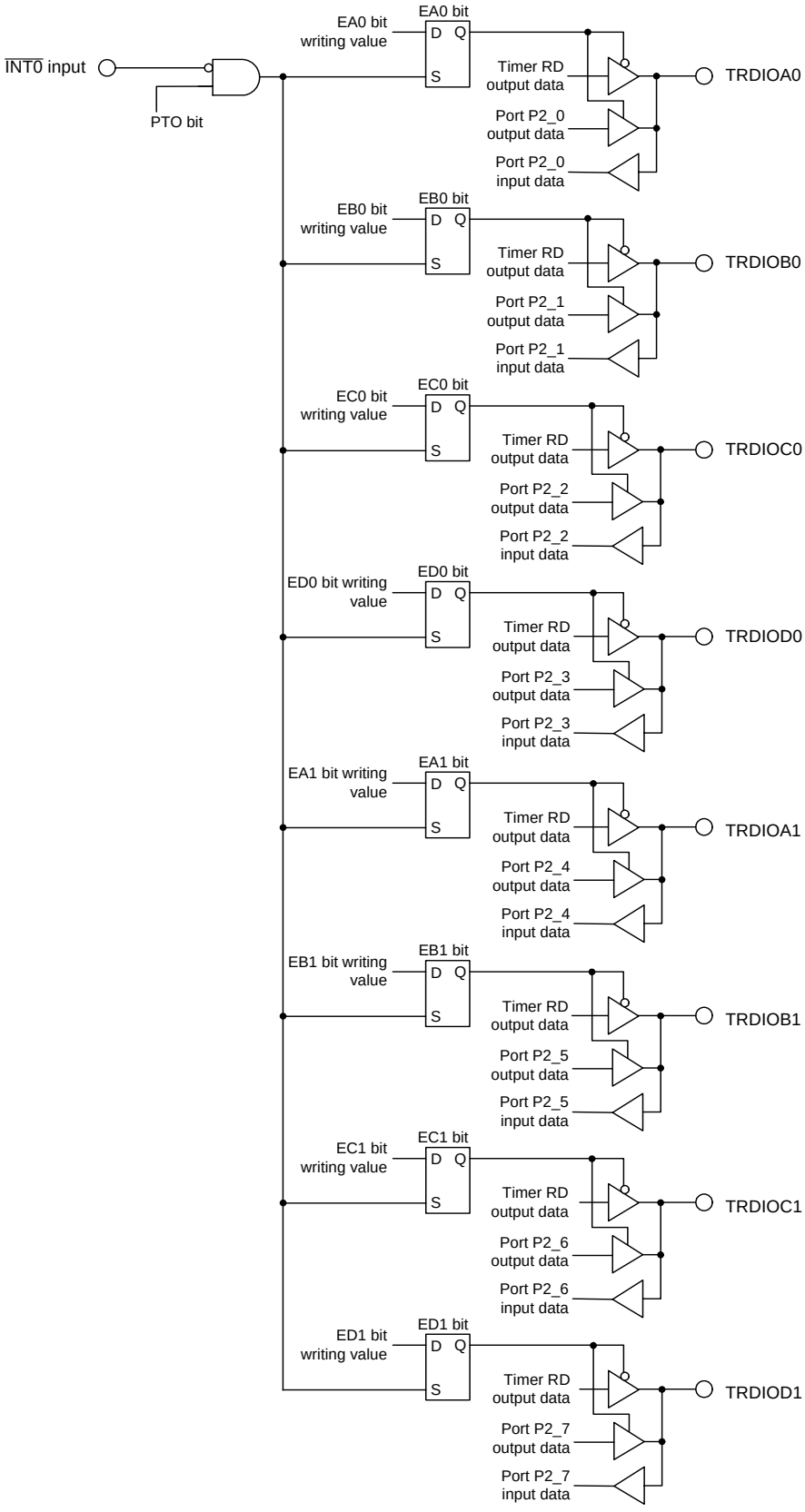
Figure 20.5 Synchronous Operation

20.2.4 Pulse Output Forced Cutoff

In the output compare function, PWM mode, reset synchronous PWM mode, complementary PWM mode, and PWM3 mode, the TRDIOji (i = 0 or 1, j = either A, B, C, or D) output pin can be forcibly set to a programmable I/O port by the $\overline{\text{INT0}}$ pin input, and pulse output can be cut off.
The pins used for output in these functions or modes can function as the output pin of timer RD when the applicable bit in the TRDOER1 register is set to 0 (enable timer RD output). When the PTO bit in the TRDOER2 register to 1 ($\overline{\text{INT0}}$ of pulse output forced cutoff signal input enabled), all bits in the TRDOER1 register are set to 1 (disable timer RD output, the TRDIOji output pin is used as the programmable I/O port) after "L" is applied to the $\overline{\text{INT0}}$ pin. The TRDIOji output pin is set to the programmable I/O port after "L" is applied to the $\overline{\text{INT0}}$ pin and waiting for 1 to 2 cycles of the timer RD operation clock (refer to **Table 20.1 Timer RD Operation Clocks**).

Make the following settings to use this function:
- Set the pin status (high impedance, "L" or "H" output) to pulse output forced cutoff by registers P2 and PD2.
- Set the INT0EN bit in the INTEN register to 1 (enable $\overline{\text{INT0}}$ input) and the INT0PL bit to 0 (one edge), and set the POL bit in the INT0IC register to 0 (falling edge selected).
- Set the PD4_5 bit in the PD4 register to 0 (input mode).
- Set the $\overline{\text{INT0}}$ digital filter by bits INT0F1 to INT0F0 in the INTF register.
- Set the PTO bit in the TRDOER2 register to 1 (enable pulse output forced cutoff signal input $\overline{\text{INT0}}$).

The IR bit in the INT0IC register is set to 1 (interrupt request) in accordance with the setting of the POL bit in the INT0IC register and the INT0PL bit in the INTEN register and a change in the $\overline{\text{INT0}}$ pin input (refer to **11.8 Notes on Interrupts**).
For details on interrupts, refer to **11. Interrupts**.



PTO: Bit in TRDOER2 register
EA0, EB0, EC0, ED0, EA1, EB1, EC1, ED1: Bits in TRDOER1 register

Figure 20.6 Pulse Output Forced Cutoff

20.3 Input Capture Function

The input capture function measures the external signal width and period. The content of the TRDi register (counter) is transferred to the TRDGRji register as a trigger of the TRDIOji (i = 0 or 1, j = either A, B, C, or D) pin external signal (input capture). Since this function is enabled with a combination of the TRDIOji pin and TRDGRji register, the input capture function, or any other mode or function, can be selected for each individual pin.
The TRDGRA0 register can also select fOCO128 signal as input-capture trigger input.
Figure 20.7 shows a Block Diagram of Input Capture Function, Table 20.5 lists the Input Capture Function Specifications. Figure 20.8 shows an Operating Example of Input Capture Function.

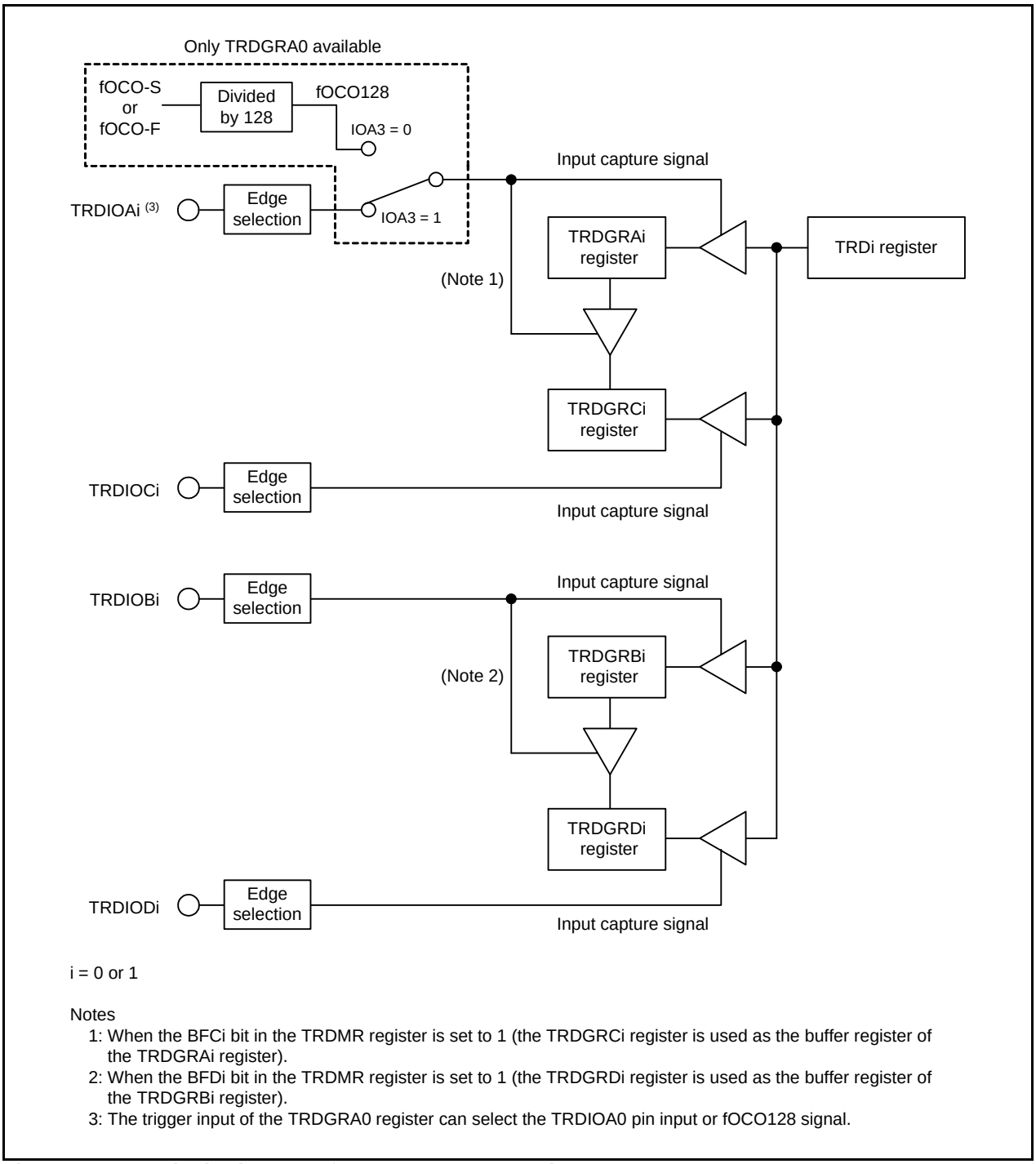


Figure 20.7 Block Diagram of Input Capture Function

Table 20.5 Input Capture Function Specifications

Item	Specification
Count sources	f1, f2, f4, f8, f32, fOCO40M, fOCO-F External signal input to the TRDCLK pin (valid edge selected by a program)
Count operations	Increment
Count period	When bits CCLR2 to CCLR0 in the TRDCRi register are set to 000b (free-running operation). 1/fk × 65536 fk: Frequency of count source
Count start condition	1 (count starts) is written to the TSTARTi bit in the TRDSTR register.
Count stop condition	0 (count stops) is written to the TSTARTi bit in the TRDSTR register when the CSELi bit in the TRDSTR register is set to 1.
Interrupt request generation timing	• Input capture (valid edge of TRDIOji input or fOCO128 signal edge) • TRDi register overflows
TRDIOA0 pin function	Programmable I/O port, input-capture input, or TRDCLK (external clock) input
TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1 to TRDIOD1 pin functions	Programmable I/O port, or input-capture input (selectable by pin)
$\overline{\text{INT0}}$ pin function	Programmable I/O port or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRDi register.
Write to timer	• When the SYNC bit in the TRDMR register is set to 0 (timer RD0 and timer RD1 operate independently). Data can be written to the TRDi register. • When the SYNC bit in the TRDMR register is set to 1 (timer RD0 and timer RD1 operate synchronously). Data can be written to both the TRD0 and TRD1 registers by writing to the TRDi register.
Selectable functions	• Input-capture input pin selection Either 1 pin or multiple pins among TRDIOAi, TRDIOBi, TRDIOCi, or TRDIODi. • Input-capture input valid edge selection The rising edge, falling edge, or both the rising and falling edges • Timing for setting the TRDi register to 0000h At overflow or input capture • Buffer operation (Refer to **20.2.2 Buffer Operation.**) • Synchronous operation (Refer to **20.2.3 Synchronous Operation.**) • Digital filter The TRDIOji input is sampled, and when the sampled input level match as 3 times, the level is determined. • Input-capture trigger selection fOCO128 can be selected for input-capture trigger input of the TRDGRA0 register.

i = 0 or 1, j = either A, B, C, or D

20.3.1 Module Standby Control Register (MSTCR)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	MSTTRG	MSTTRC	MSTTRD	MSTIIC	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	MSTIIC	SSU standby bit	0: Active 1: Standby (1)	R/W
b4	MSTTRD	Timer RD standby bit	0: Active 1: Standby (2, 3)	R/W
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (4)	R/W
b6	MSTTRG	Timer RG standby bit	0: Active 1: Standby (5)	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. When the MSTIIC bit is set to 1 (standby), any access to the SSU associated registers (addresses 0193h to 019Dh) is disabled.
2. When the MSTTRD bit is set to 1 (standby), any access to the timer RD associated registers (addresses 0136h to 015Fh) is disabled.
3. To set the MSTTRD bit to 1 (standby), set bits TCK2 to TCK0 in the TRDCRi (i = 0 or 1) register to 000b (f1).
4. When the MSTTRC bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0120h to 0133h) is disabled.
5. When the MSTTRG bit is set to 1 (standby), any access to the timer RG associated registers (addresses 0170h to 017Fh) is disabled.

20.3.2 Timer RD Start Register (TRDSTR) [Timer mode (in Input Capture Function)]

Address 0137h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	CSEL1	CSEL0	TSTART1	TSTART0
After Reset	1	1	1	1	1	1	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART0	TRD0 count start flag	0: Count stops 1: Count starts	R/W
b1	TSTART1	TRD1 count start flag		R/W
b2	CSEL0	TRD0 count operation select bit	Set to 1 in the input capture function.	R/W
b3	CSEL1	TRD1 count operation select bit		R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	—			

Set the TRDSTR register using the MOV instruction (do not use the bit handling instruction). Refer to **20.10.1 TRDSTR Register** of **Notes on Timer RD**.

20.3.3 Timer RD Mode Register (TRDMR) [Timer mode (in Input Capture Function)]

Address 0138h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BFD1	BFC1	BFD0	BFC0	—	—	—	SYNC
After Reset	0	0	0	0	1	1	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	SYNC	Timer RD synchronous bit	0: Registers TRD0 and TRD1 operate independently 1: Registers TRD0 and TRD1 operate synchronously	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b2	—			
b3	—			
b4	BFC0	TRDGRC0 register function select bit	0: General register 1: Buffer register of TRDGRA0 register	R/W
b5	BFD0	TRDGRD0 register function select bit	0: General register 1: Buffer register of TRDGRB0 register	R/W
b6	BFC1	TRDGRC1 register function select bit	0: General register 1: Buffer register of TRDGRA1 register	R/W
b7	BFD1	TRDGRD1 register function select bit	0: General register 1: Buffer register of TRDGRB1 register	R/W

20.3.4 Timer RD PWM Mode Register (TRDPMR) [Timer mode (in Input Capture Function)]

Address 0139h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	PWMD1	PWMC1	PWMB1	—	PWMD0	PWMC0	PWMB0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PWMB0	PWM mode of TRDIOB0 select bit	Set to 0 (timer mode) in the input capture function.	R/W
b1	PWMC0	PWM mode of TRDIOC0 select bit		R/W
b2	PWMD0	PWM mode of TRDIOD0 select bit		R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b4	PWMB1	PWM mode of TRDIOB1 select bit	Set to 0 (timer mode) in the input capture function.	R/W
b5	PWMC1	PWM mode of TRDIOC1 select bit		R/W
b6	PWMD1	PWM mode of TRDIOD1 select bit		R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

20.3.5 Timer RD Function Control Register (TRDFCR) [Timer mode (in Input Capture Function)]

Address 013Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PWM3	STCLK	ADEG	ADTRG	OLS1	OLS0	CMD1	CMD0
After Reset	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CMD0	Combination mode select bit (1)	Set to 00b (timer mode, PWM mode, or PWM3 mode) in the input capture function.	R/W
b1	CMD1			R/W
b2	OLS0	Normal-phase output level select bit (in reset synchronous PWM mode or complementary PWM mode)	This bit is disabled in the input capture function.	R/W
b3	OLS1	Counter-phase output level select bit (in reset synchronous PWM mode or complementary PWM mode)		R/W
b4	ADTRG	A/D trigger enable bit (in complementary PWM mode)		R/W
b5	ADEG	A/D trigger edge select bit (in complementary PWM mode)		R/W
b6	STCLK	External clock input select bit	0: External clock input disabled 1: External clock input enabled	R/W
b7	PWM3	PWM3 mode select bit (2)	Set this bit to 1 (other than PWM3 mode) in the input capture function.	R/W

Notes:
1. Set bits CMD1 to CMD0 when both the TSTART0 and TSTART1 bits in the TRDSTR register are set to 0 (count stops).
2. When bits CMD1 to CMD0 are set to 00b (timer mode, PWM mode, or PWM3 mode), the setting of the PWM3 bit is enabled.

20.3.6 Timer RD Digital Filter Function Select Register i (TRDDFi) (i = 0 or 1) [Timer mode (in Input Capture Function)]

Address 013Eh (TRDDF0), 013Fh (TRDDF1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DFCK1	DFCK0	—	—	DFD	DFC	DFB	DFA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DFA	TRDIOA pin digital filter function select bit	0: Function is not used 1: Function is used	R/W
b1	DFB	TRDIOB pin digital filter function select bit		R/W
b2	DFC	TRDIOC pin digital filter function select bit		R/W
b3	DFD	TRDIOD pin digital filter function select bit		R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	DFCK0	Clock select bits for digital filter function	b7 b6 0 0: f32 0 1: f8 1 0: f1 1 1: Count source (clock selected by bits TCK2 to TCK0 in the TRCCRi register)	R/W
b7	DFCK1			R/W

20.3.7 Timer RD Control Register i (TRDCRi) (i = 0 or 1) [Timer mode (in Input Capture Function)]

Address 0140h (TRDCR0), 0150h (TRDCR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TCK2	TCK1	TCK0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TCK0	Count source select bit	b2 b1 b0 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRDCLK input (1) 1 1 0: fOCO40M 1 1 1: fOCO-F (4)	R/W
b1	TCK1			R/W
b2	TCK2			R/W
b3	CKEG0	External clock edge select bit (2)	b4 b3 0 0: Count at the rising edge 0 1: Count at the falling edge 1 0: Count at both edges 1 1: Do not set.	R/W
b4	CKEG1			R/W
b5	CCLR0	TRDi counter clear select bit	b7 b6 b5 0 0 0: Disable clear (free-running operation) 0 0 1: Clear by input capture in the TRDGRAi register 0 1 0: Clear by input capture in the TRDGRBi register 0 1 1: Synchronous clear (clear simultaneously with other timer RDi counter) (3) 1 0 0: Do not set. 1 0 1: Clear by input capture in the TRDGRCi register 1 1 0: Clear by input capture in the TRDGRDi register 1 1 1: Do not set.	R/W
b6	CCLR1			R/W
b7	CCLR2			R/W

Notes:
1. Enabled when the STCLK bit in the TRDFCR register is 1 (external clock input enabled).
2. Enabled when bits TCK2 to TCK0 are set to 101b (TRDCLK input) and the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).
3. This setting is enabled when the SYNC bit in the TRDMR register is set to 1 (registers TRD0 and TRD1 operate synchronously).
4. To select fOCO-F, set it to the clock frequency higher than the CPU clock frequency.

20.3.8 Timer RD I/O Control Register Ai (TRDIORAi) (i = 0 or 1) [Timer mode (in Input Capture Function)]

Address 0141h (TRDIORA0), 0151h (TRDIORA1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRDGRA control bit	b1 b0 0 0: Input capture to the TRDGRAi register at the rising edge 0 1: Input capture to the TRDGRAi register at the falling edge 1 0: Input capture to the TRDGRAi register at both edges 1 1: Do not set.	R/W
b1	IOA1			R/W
b2	IOA2	TRDGRA mode select bit (1)	Set to 1 (input capture) in the input capture function.	R/W
b3	IOA3	Input capture input switch bit (3, 4)	0: fOCO128 Signal 1: TRDIOA0 pin input	R/W
b4	IOB0	TRDGRB control bit	b5 b4 0 0: Input capture to the TRDGRBi register at the rising edge 0 1: Input capture to the TRDGRBi register at the falling edge 1 0: Input capture to the TRDGRBi register at both edges 1 1: Do not set.	R/W
b5	IOB1			R/W
b6	IOB2	TRDGRB mode select bit (2)	Set to 1 (input capture) in the input capture function.	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Notes:
1. To select 1 (the TRDGRCi register is used as a buffer register of the TRDGRAi register) for this bit by the BFCi bit in the TRDMR register, set the IOC2 bit in the TRDIORCi register to the same value as the IOA2 bit in the TRDIORAi register.
2. To select 1 (the TRDGRDi register is used as a buffer register of the TRDGRBi register) for this bit by the BFDi bit in the TRDMR register, set the IOD2 bit in the TRDIORCi register to the same value as the IOB2 bit in the TRDIORAi register.
3. The IOA3 bit is enabled in the TRDIORA0 register only. Set to the IOA3 bit in TRDIORA1 to 1.
4. The IOA3 bit is enabled when the IOA2 bit is set to 1 (input capture function).

20.3.9 Timer RD I/O Control Register Ci (TRDIORCi) (i = 0 or 1) [Timer mode (in Input Capture Function)]

Address 0142h (TRDIORC0), 0152h (TRDIORC1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOC0	TRDGRC control bit	b1 b0 0 0: Input capture to the TRDGRCi register at the rising edge 0 1: Input capture to the TRDGRCi register at the falling edge 1 0: Input capture to the TRDGRCi register at both edges 1 1: Do not set.	R/W
b1	IOC1			R/W
b2	IOC2	TRDGRC mode select bit (1)	Set to 1 (input capture) in the input capture function.	R/W
b3	IOC3	TRDGRC register function select bit	Set to 1 (general register or buffer register) in the input capture function.	R/W
b4	IOD0	TRDGRD control bit	b5 b4 0 0: Input capture to the TRDGRDi register at the rising edge 0 1: Input capture to the TRDGRDi register at the falling edge 1 0: Input capture to the TRDGRDi register at both edges 1 1: Do not set.	R/W
b5	IOD1			R/W
b6	IOD2	TRDGRD mode select bit (2)	Set to 1 (input capture) in the input capture function.	R/W
b7	IOD3	TRDGRD register function select bit	Set to 1 (general register or buffer register) in the input capture function.	R/W

Notes:
1. To select 1 (the TRDGRCi register is used as a buffer register of the TRDGRAi register) for this bit by the BFCi bit in the TRDMR register, set the IOC2 bit in the TRDIORCi register to the same value as the IOA2 bit in the TRDIORAi register.
2. To select 1 (the TRDGRDi register is used as a buffer register of the TRDGRBi register) for this bit by the BFDi bit in the TRDMR register, set the IOD2 bit in the TRDIORCi register to the same value as the IOB2 bit in the TRDIORAi register.

20.3.10 Timer RD Status Register i (TRDSRi) (i = 0 or 1) [Timer mode (in Input Capture Function)]

Address 0143h (TRDSR0), 0153h (TRDSR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	UDF	OVF	IMFD	IMFC	IMFB	IMFA	
After Reset	1	1	1	0	0	0	0	0	TRDSR0 register
After Reset	1	1	0	0	0	0	0	0	TRDSR1 register

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input capture / compare match flag A	[Source for setting this bit to 0] Write 0 after read (2). [Source for setting this bit to 1]. TRDSR0 register: fOCO128 signal edge when the IOA3 bit in the TRDIORA0 register is set to 0 (fOCO128 signal). TRDIOA0 pin input edge when the IOA3 bit in the TRDIORA0 register is set to 1 (TRDIOA0 input) (3). TRDSR1 register: Input edge of TRDIOA1 pin (3).	R/W
b1	IMFB	Input capture / compare match flag B	[Source for setting this bit to 0] Write 0 after read (2). [Source for setting this bit to 1] Input edge of TRDIOBi pin (3).	R/W
b2	IMFC	Input capture / compare match flag C	[Source for setting this bit to 0] Write 0 after read (2). [Source for setting this bit to 1] Input edge of TRDIOCi pin (4).	R/W
b3	IMFD	Input capture / compare match flag D	[Source for setting this bit to 0] Write 0 after read (2). [Source for setting this bit to 1] Input edge of TRDIODi pin (4).	R/W
b4	OVF	Overflow flag	[Source for setting this bit to 0] Write 0 after read (2). [Source for setting this bit to 1] When the TRDi register overflows.	R/W
b5	UDF	Underflow flag (1)	This bit is disabled in the input capture function.	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b7	—			

Notes:
1. Nothing is assigned to b5 in the TRDSR0 register. When writing to b5, write 0. When reading, the content is 1.
2. The writing results are as follows:
   - This bit is set to 0 when the read result is 1 and 0 is written to the same bit.
   - This bit remains unchanged even if the read result is 0 and 0 is written to the same bit. (This bit remains 1 even if it is set to 1 from 0 after reading, and writing 0.)
   - This bit remains unchanged if 1 is written to it.
3. Edge selected by bits IOj1 to IOj0 (j = A or B) in the TRDIORAi register.
4. Edge selected by bits IOk1 to IOk0 (k = C or D) in the TRDIORCi register.
   Including when the BFki bit in the TRDMR register is set to 1 (TRDGRki is used as the buffer register)

20.3.11 Timer RD Interrupt Enable Register i (TRDIERi) (i = 0 or 1) [Timer mode (in Input Capture Function)]

Address 0144h (TRDIER0), 0154h (TRDIER1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	OVIE	IMIED	IMIEC	IMIEB	IMIEA
After Reset	1	1	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input capture/compare match interrupt enable bit A	0: Disable interrupt (IMIA) by the IMFA bit 1: Enable interrupt (IMIA) by the IMFA bit	R/W
b1	IMIEB	Input capture/compare match interrupt enable bit B	0: Disable interrupt (IMIB) by the IMFB bit 1: Enable interrupt (IMIB) by the IMFB bit	R/W
b2	IMIEC	Input capture/compare match interrupt enable bit C	0: Disable interrupt (IMIC) by the IMFC bit 1: Enable interrupt (IMIC) by the IMFC bit	R/W
b3	IMIED	Input capture/compare match interrupt enable bit D	0: Disable interrupt (IMID) by the IMFD bit 1: Enable interrupt (IMID) by the IMFD bit	R/W
b4	OVIE	Overflow/underflow interrupt enable bit	0: Disable interrupt (OVI) by the OVF bit 1: Enable interrupt (OVI) by the OVF bit	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b6	—			
b7	—			

20.3.12 Timer RD Counter i (TRDi) (i = 0 or 1) [Timer mode (in Input Capture Function)]

Address 0147h to 0146h (TRD0), 0157h to 0156h (TRD1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15 to b0	Count the count source. Count operation is incremented. When an overflow occurs, the OVF bit in the TRDSRi register is set to 1.	0000h to FFFFh	R/W

Access the TRDi register in 16-bit units. Do not access it in 8-bit units.

20.3.13 Timer RD General Registers Ai, Bi, Ci, and Di (TRDGRAi, TRDGRBi, TRDGRCi, TRDGRDi) (i = 0 or 1) [Timer mode (in Input Capture Function)]

Address 0149h to 0148h (TRDGRA0), 014Bh to 014Ah (TRDGRB0),
014Dh to 014Ch (TRDGRC0), 014Fh to 014Eh (TRDGRD0),
0159h to 0158h (TRDGRA1), 015Bh to 015Ah (TRDGRB1),
015Dh to 015Ch (TRDGRC1), 015Fh to 015Eh (TRDGRD1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b15 to b0	Refer to **Table 20.6 TRDGRji Register Functions in Input Capture Function**	R/W

Access registers TRDGRAi to TRDGRDi in 16-bit units. Do not access them in 8-bit units.

The following registers are disabled in the input capture function: TRDOER1, TRDOER2, TRDOCR, TRDPOCR0, and TRDPOCR1.

Table 20.6 TRDGRji Register Functions in Input Capture Function

Register	Setting	Register Function	Input-Capture Input Pin
TRDGRAi	–	General register The value in the TRDi register can be read at input capture.	TRDIOAi
TRDGRBi			TRDIOBi
TRDGRCi	BFCi = 0	General register The value in the TRDi register can be read at input capture.	TRDIOCi
TRDGRDi	BFDi = 0		TRDIODi
TRDGRCi	BFCi = 1	Buffer register The value in the TRDi register can be read at input capture. (Refer to **20.2.2 Buffer Operation**)	TRDIOAi
TRDGRDi	BFDi = 1		TRDIOBi

i = 0 or 1, j = either A, B, C, or D
BFCi, BFDi: Bits in TRDMR register

Set the pulse width of the input capture signal applied to the TRDIOji pin to 3 cycles or more of the timer RD operation clock (refer to **Table 20.1 Timer RD Operation Clocks**) for no digital filter (the DFj bit in the TRDDFi register set to 0).

20.3.14 Timer RD Pin Select Register 0 (TRDPSR0)

Address 0184h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	TRDIOD0SEL0	—	TRDIOC0SEL0	—	TRDIOB0SEL0	—	TRDIOA0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRDIOA0SEL0	TRDIOA0/TRDCLK pin select bit	0: TRDIOA0/TRDCLK pin not used 1: P2_0 assigned	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	TRDIOB0SEL0	TRDIOB0 pin select bit	0: TRDIOB0 pin not used 1: P2_1 assigned	R/W
b3	—	Reserved bit	Set to 0.	R/W
b4	TRDIOC0SEL0	TRDIOC0 pin select bit	0: TRDIOC0 pin not used 1: P2_2 assigned	R/W
b5	—	Reserved bit	Set to 0.	R/W
b6	TRDIOD0SEL0	TRDIOD0 pin select bit	0: TRDIOD0 pin not used 1: P2_3 assigned	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

The TRDPSR0 register selects which pin is assigned to the timer RD I/O. To use the I/O pin for timer RD, set this register.
Set the TRDPSR0 register before setting the timer RD associated registers. Also, do not change the setting value in this register during timer RD operation.

20.3.15 Timer RD Pin Select Register 1 (TRDPSR1)

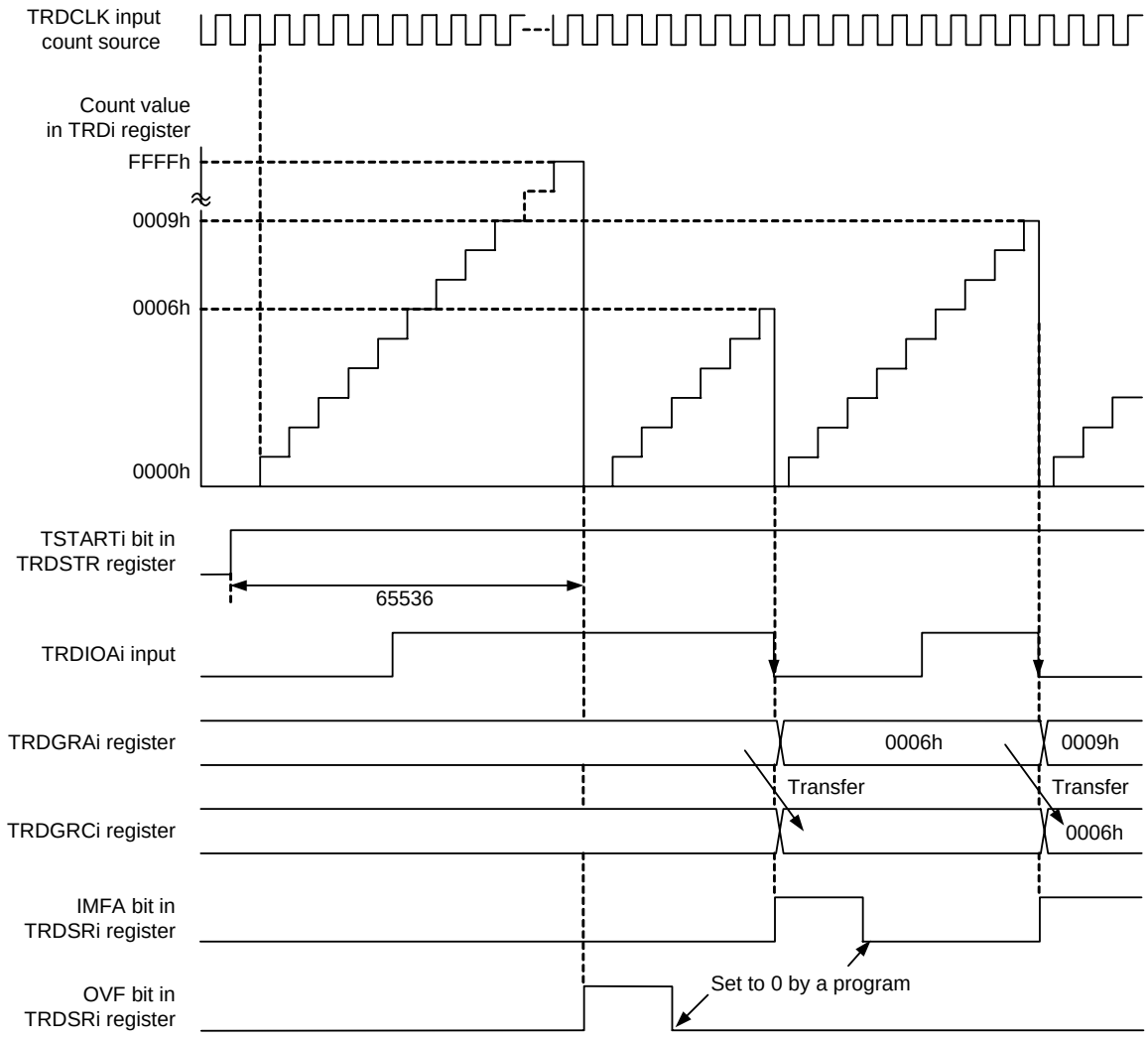
Address 0185h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	TRDIOD1SEL0	—	TRDIOC1SEL0	—	TRDIOB1SEL0	—	TRDIOA1SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRDIOA1SEL0	TRDIOA1 pin select bit	0: TRDIOA1 pin not used 1: P2_4 assigned	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	TRDIOB1SEL0	TRDIOB1 pin select bit	0: TRDIOB1 pin not used 1: P2_5 assigned	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TRDIOC1SEL0	TRDIOC1 pin select bit	0: TRDIOC1 pin not used 1: P2_6 assigned	R/W
b5	—	Reserved bit	Set to 0.	R/W
b6	TRDIOD1SEL0	TRDIOD1 pin select bit	0: TRDIOD1 pin not used 1: P2_7 assigned	R/W
b7	—	Reserved bit	Set to 0.	R/W

The TRDPSR1 register selects which pin is assigned to the timer RD I/O. To use the I/O pin for timer RD, set this register.
Set the TRDPSR1 register before setting the timer RD associated registers. Also, do not change the setting value in this register during timer RD operation.

20.3.16 Operating Example



i = 0 or 1

The above applies under the following conditions:
Bits CCLR2 to CCLR0 in the TRDCRi register are set to 001b. (the TRDi register set to 0000h by TRDGRAi register input capture).
Bits TCK2 to TCK0 in the TRDCRi register are set to 101b (TRDCLK input for the count source).
Bits CKEG1 to CKEG0 in the TRDCRi register are set to 01b (count at the falling edge for the count source).
Bits IOA2 to IOA0 in the TRDIORAi register are set to 101b (input capture at the falling edge of the TRDIOAi input).
The BFCi bit in the TRDMR register is set to 1 (the TRDGRCi register is used as the buffer register of the TRDGRAi register).

Figure 20.8 Operating Example of Input Capture Function

20.3.17 Digital Filter

The TRDIOji input is sampled, and when the sampled input level matches 3 times, its level is determined. Select the digital filter function and sampling clock by the TRDDFi register.

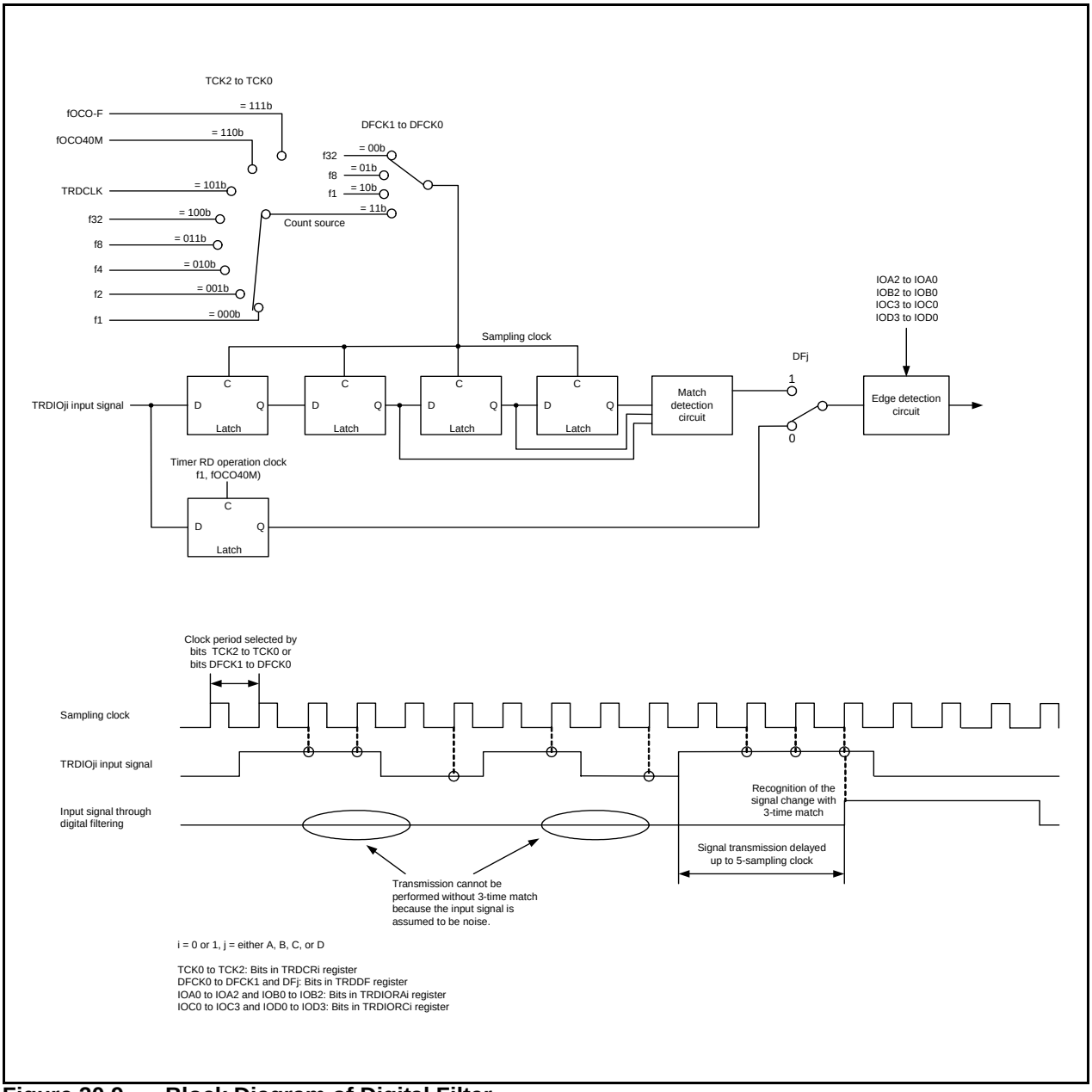


Figure 20.9 Block Diagram of Digital Filter

20.4 Timer Mode (Output Compare Function)

This function detects matches (compare match) between the content of the TRDGRji (j = either A, B, C, or D) register and the content of the TRDi (i = 0 or 1) register. When the content matches, a user-set level is output from the TRDIOji pin. Since this function is enabled with a combination of the TRDIOji pin and TRDGRji register, the output compare function, or any other mode or function, can be selected for each individual pin. Figure 20.10 shows a Block Diagram of Output Compare Function, Table 20.7 lists the Output Compare Function Specifications. Figure 20.11 shows an Operating Example of Output Compare Function.

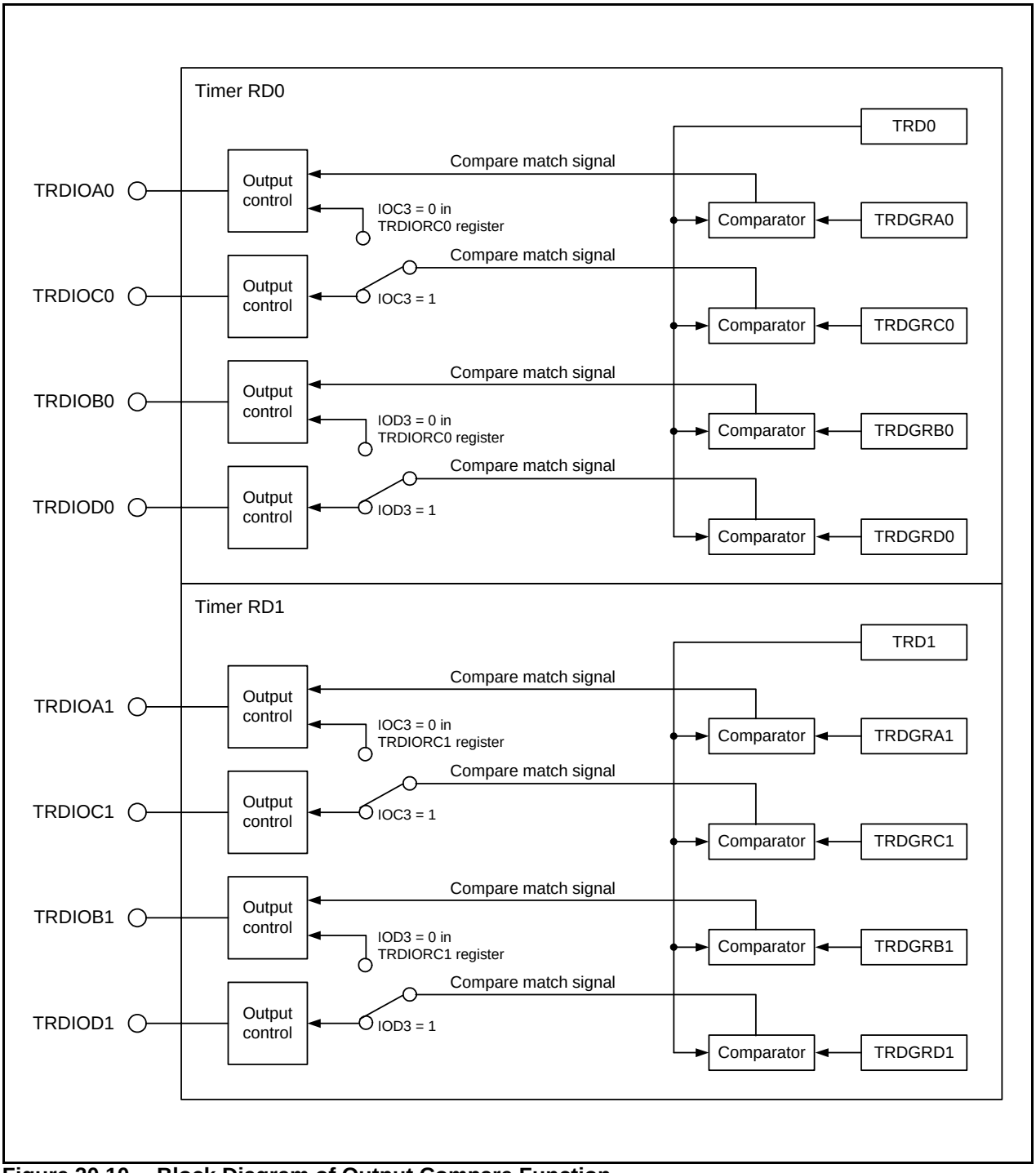


Figure 20.10 Block Diagram of Output Compare Function

Table 20.7 Output Compare Function Specifications

Item	Specification
Count sources	f1, f2, f4, f8, f32, fOCO40M, fOCO-F External signal input to the TRDCLK pin (valid edge selected by a program)
Count operations	Increment
Count period	• When bits CCLR2 to CCLR0 in the TRDCRi register are set to 000b (free-running operation) 1/fk × 65536 fk: Frequency of count source • Bits CCLR1 to CCLR0 in the TRDCRi register are set to 01b or 10b (set the TRDi register to 0000h at the compare match in the TRDGRji register). Frequency of count source x (n+1) n: Setting value in the TRDGRji register
Waveform output timing	Compare match
Count start condition	1 (count starts) is written to the TSTARTi bit in the TRDSTR register.
Count stop conditions	• 0 (count stops) is written to the TSTARTi bit in the TRDSTR register when the CSELi bit in the TRDSTR register is set to 1. The output compare output pin holds output level before the count stops. • When the CSELi bit in the TRDSTR register is set to 0, the count stops at the compare match in the TRDGRAi register. The output compare output pin holds level after output change by the compare match.
Interrupt request generation timing	• Compare match (content of the TRDi register matches content of the TRDGRji register.) • TRDi register overflows
TRDIOA0 pin function	Programmable I/O port, output-compare output, or TRDCLK (external clock) input
TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1 to TRDIOD1 pin functions	Programmable I/O port or output-compare output (Selectable by pin)
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRDi register.
Write to timer	• When the SYNC bit in the TRDMR register is set to 0 (timer RD0 and timer RD1 operate independently). Data can be written to the TRDi register. • When the SYNC bit in the TRDMR register is set to 1 (timer RD0 and timer RD1 operate synchronously). Data can be written to both the TRD0 and TRD1 registers by writing to the TRDi register.
Selectable functions	• Output-compare output pin selection Either 1 pin or multiple pins among TRDIOAi, TRDIOBi, TRDIOCi, or TRDIODi. • Output level at the compare match selection “L” output, “H” output, or output level inverted • Initial output level selected Set the level at period from the count start to the compare match. • Timing for setting the TRDi register to 0000h Overflow or compare match in the TRDGRAi register • Buffer operation (Refer to **20.2.2 Buffer Operation.**) • Synchronous operation (Refer to **20.2.3 Synchronous Operation.**) • Changing output pins for registers TRDGRCi and TRDGRDi The TRDGRCi register can be used as output control of the TRDIOAi pin and the TRDGRDi register can be used as output control of the TRDIOBi pin. • Pulse output forced cutoff signal input (Refer to **20.2.4 Pulse Output Forced Cutoff.**) • Timer RD can be used as the internal timer without output. • A/D trigger generation

i = 0 or 1, j = either A, B, C, or D

20.4.1 Module Standby Control Register (MSTCR)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	MSTTRG	MSTTRC	MSTTRD	MSTIIC	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	MSTIIC	SSU standby bit	0: Active 1: Standby (1)	R/W
b4	MSTTRD	Timer RD standby bit	0: Active 1: Standby (2, 3)	R/W
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (4)	R/W
b6	MSTTRG	Timer RG standby bit	0: Active 1: Standby (5)	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. When the MSTIIC bit is set to 1 (standby), any access to the SSU associated registers (addresses 0193h to 019Dh) is disabled.
2. When the MSTTRD bit is set to 1 (standby), any access to the timer RD associated registers (addresses 0136h to 015Fh) is disabled.
3. To set the MSTTRD bit to 1 (standby), set bits TCK2 to TCK0 in the TRDCRi (i = 0 or 1) register to 000b (f1).
4. When the MSTTRC bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0120h to 0133h) is disabled.
5. When the MSTTRG bit is set to 1 (standby), any access to the timer RG associated registers (addresses 0170h to 017Fh) is disabled.

20.4.2 Timer RD Trigger Control Register (TRDADCR)

Address 0136h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADTRGD1E	ADTRGC1E	ADTRGB1E	ADTRGA1E	ADTRGD0E	ADTRGC0E	ADTRGB0E	ADTRGA0E
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADTRGA0E	A/D trigger A0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRA0	R/W
b1	ADTRGB0E	A/D trigger B0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRB0	R/W
b2	ADTRGC0E	A/D trigger C0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRC0	R/W
b3	ADTRGD0E	A/D trigger D0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRD0	R/W
b4	ADTRGA1E	A/D trigger A1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRA1	R/W
b5	ADTRGB1E	A/D trigger B1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRB1	R/W
b6	ADTRGC1E	A/D trigger C1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRC1	R/W
b7	ADTRGD1E	A/D trigger D1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRD1	R/W

20.4.3 Timer RD Start Register (TRDSTR) [Timer mode (in Output Compare Function)]

Address 0137h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	CSEL1	CSEL0	TSTART1	TSTART0
After Reset	1	1	1	1	1	1	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART0	TRD0 count start flag (3)	0: Count stops (1) 1: Count starts	R/W
b1	TSTART1	TRD1 count start flag (4)	0: Count stops (2) 1: Count starts	R/W
b2	CSEL0	TRD0 count operation select bit	0: Count stops at the compare match with the TRDGRA0 register 1: Count continues after the compare match with the TRDGRA0 register	R/W
b3	CSEL1	TRD1 count operation select bit	0: Count stops at the compare match with the TRDGRA1 register 1: Count continues after the compare match with the TRDGRA1 register	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	—			

Notes:
1. When the CSEL0 bit is set to 1, write 0 to the TSTART0 bit.
2. When the CSEL1 bit is set to 1, write 0 to the TSTART1 bit.
3. When the CSEL0 bit is set to 0 and the compare match signal (TRDIOA0) is generated, this bit is set to 0 (count stops).
4. When the CSEL1 bit is set to 0 and the compare match signal (TRDIOA1) is generated, this bit is set to 0 (count stops).

Set the TRDSTR register using the MOV instruction (do not use the bit handling instruction). Refer to **20.10.1 TRDSTR Register** of **Notes on Timer RD**.

20.4.4 Timer RD Mode Register (TRDMR) [Timer mode (in Output Compare Function)]

Address 0138h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BFD1	BFC1	BFD0	BFC0	—	—	—	SYNC
After Reset	0	0	0	0	1	1	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	SYNC	Timer RD synchronous bit	0: Registers TRD0 and TRD1 operate independently 1: Registers TRD0 and TRD1 operate synchronously	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b2	—			
b3	—			
b4	BFC0	TRDGRC0 register function select bit (1)	0: General register 1: Buffer register of TRDGRA0 register	R/W
b5	BFD0	TRDGRD0 register function select bit (1)	0: General register 1: Buffer register of TRDGRB0 register	R/W
b6	BFC1	TRDGRC1 register function select bit (1)	0: General register 1: Buffer register of TRDGRA1 register	R/W
b7	BFD1	TRDGRD1 register function select bit (1)	0: General register 1: Buffer register of TRDGRB1 register	R/W

Note:
1. When selecting 0 (change the TRDGRji register output pin) by the IOj3 (j = C or D) bit in the TRDIORCi (i = 0 or 1) register, set the BFji bit in the TRDMR register to 0.

20.4.5 Timer RD PWM Mode Register (TRDPMR) [Timer mode (in Output Compare Function)]

Address 0139h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	PWMD1	PWMC1	PWMB1	—	PWMD0	PWMC0	PWMB0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PWMB0	PWM mode of TRDIOB0 select bit	Set to 0 (timer mode) in the output compare function.	R/W
b1	PWMC0	PWM mode of TRDIOC0 select bit		R/W
b2	PWMD0	PWM mode of TRDIOD0 select bit		R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b4	PWMB1	PWM mode of TRDIOB1 select bit	Set to 0 (timer mode) in the output compare function.	R/W
b5	PWMC1	PWM mode of TRDIOC1 select bit		R/W
b6	PWMD1	PWM mode of TRDIOD1 select bit		R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

20.4.6 Timer RD Function Control Register (TRDFCR) [Timer mode (in Output Compare Function)]

Address 013Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PWM3	STCLK	ADEG	ADTRG	OLS1	OLS0	CMD1	CMD0
After Reset	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CMD0	Combination mode select bit (1)	Set to 00b (timer mode, PWM mode, or PWM3 mode) in the output compare function.	R/W
b1	CMD1			R/W
b2	OLS0	Normal-phase output level select bit (in reset synchronous PWM mode or complementary PWM mode)	This bit is disabled in the output compare function.	R/W
b3	OLS1	Counter-phase output level select bit (in reset synchronous PWM mode or complementary PWM mode)		R/W
b4	ADTRG	A/D trigger enable bit (in complementary PWM mode)		R/W
b5	ADEG	A/D trigger edge select bit (in complementary PWM mode)		R/W
b6	STCLK	External clock input select bit	0: External clock input disabled 1: External clock input enabled	R/W
b7	PWM3	PWM3 mode select bit (2)	Set this bit to 1 (other than PWM3 mode) in the output compare function.	R/W

Notes:
1. Set bits CMD1 to CMD0 when both the TSTART0 and TSTART1 bits in the TRDSTR register are set to 0 (count stops).
2. When bits CMD1 to CMD0 are set to 00b (timer mode, PWM mode, or PWM3 mode), the setting of the PWM3 bit is enabled.

20.4.7 Timer RD Output Master Enable Register 1 (TRDOER1) [Timer mode (in Output Compare Function)]

Address 013Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ED1	EC1	EB1	EA1	ED0	EC0	EB0	EA0
After Reset	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	EA0	TRDIOA0 output disable bit	0: Enable output 1: Disable output (The TRDIOA0 pin is used as a programmable I/O port.)	R/W
b1	EB0	TRDIOB0 output disable bit	0: Enable output 1: Disable output (The TRDIOB0 pin is used as a programmable I/O port.)	R/W
b2	EC0	TRDIOC0 output disable bit	0: Enable output 1: Disable output (The TRDIOC0 pin is used as a programmable I/O port.)	R/W
b3	ED0	TRDIOD0 output disable bit	0: Enable output 1: Disable output (The TRDIOD0 pin is used as a programmable I/O port.)	R/W
b4	EA1	TRDIOA1 output disable bit	0: Enable output 1: Disable output (The TRDIOA1 pin is used as a programmable I/O port.)	R/W
b5	EB1	TRDIOB1 output disable bit	0: Enable output 1: Disable output (The TRDIOB1 pin is used as a programmable I/O port.)	R/W
b6	EC1	TRDIOC1 output disable bit	0: Enable output 1: Disable output (The TRDIOC1 pin is used as a programmable I/O port.)	R/W
b7	ED1	TRDIOD1 output disable bit	0: Enable output 1: Disable output (The TRDIOD1 pin is used as a programmable I/O port.)	R/W

20.4.8 Timer RD Output Master Enable Register 2 (TRDOER2) [Timer mode (in Output Compare Function)]

Address 013Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PTO	—	—	—	—	—	—	—
After Reset	0	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	PTO	$\overline{\text{INT0}}$ of pulse output forced cutoff signal input enabled bit (1)	0: Pulse output forced cutoff input disabled 1: Pulse output forced cutoff input enabled (All bits in the TRDOER1 register are set to 1 (disable output) when “L” is applied to the $\overline{\text{INT0}}$ pin.)	R/W

Note:
1. Refer to **20.2.4 Pulse Output Forced Cutoff**.

20.4.9 Timer RD Output Control Register (TRDOCR) [Timer mode (in Output Compare Function)]

Address 013Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TOD1	TOC1	TOB1	TOA1	TOD0	TOC0	TOB0	TOA0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA0	TRDIOA0 output level select bit	0: Initial output “L” 1: Initial output “H”	R/W
b1	TOB0	TRDIOB0 output level select bit	0: Initial output “L” 1: Initial output “H”	R/W
b2	TOC0	TRDIOC0 initial output level select bit	0: “L” 1: “H”	R/W
b3	TOD0	TRDIOD0 initial output level select bit		R/W
b4	TOA1	TRDIOA1 initial output level select bit		R/W
b5	TOB1	TRDIOB1 initial output level select bit		R/W
b6	TOC1	TRDIOC1 initial output level select bit		R/W
b7	TOD1	TRDIOD1 initial output level select bit		R/W

Write to the TRDOCR register when both the TSTART0 and TSTART1 bits in the TRDSTR register are set to 0 (count stopped).

If the pin function is set for waveform output (refer to **7.5 Port Settings**), the initial output level is output when the TRDOCR register is set.

20.4.10 Timer RD Control Register i (TRDCRi) (i = 0 or 1) [Timer mode (in Output Compare Function)]

Address 0140h (TRDCR0), 0150h (TRDCR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TCK2	TCK1	TCK0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TCK0	Count source select bit	b2 b1 b0 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRDCLK input (1) 1 1 0: fOCO40M 1 1 1: fOCO-F (4)	R/W
b1	TCK1			R/W
b2	TCK2			R/W
b3	CKEG0	External clock edge select bit (2)	b4 b3 0 0: Count at the rising edge 0 1: Count at the falling edge 1 0: Count at both edges 1 1: Do not set.	R/W
b4	CKEG1			R/W
b5	CCLR0	TRDi counter clear select bit	b7 b6 b5 0 0 0: Disable clear (free-running operation) 0 0 1: Clear by compare match with the TRDGRAi register 0 1 0: Clear by compare match with the TRDGRBi register 0 1 1: Synchronous clear (clear simultaneously with other timer RDi counter) (3) 1 0 0: Do not set. 1 0 1: Clear by compare match with the TRDGRCi register 1 1 0: Clear by compare match with the TRDGRDi register 1 1 1: Do not set.	R/W
b6	CCLR1			R/W
b7	CCLR2			R/W

Notes:
1. Enabled when the STCLK bit in the TRDFCR register is 1 (external clock input enabled).
2. Enabled when bits TCK2 to TCK0 are set to 101b (TRDCLK input) and the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).
3. This setting is enabled when the SYNC bit in the TRDMR register is set to 1 (registers TRD0 and TRD1 operate synchronously).
4. To select fOCO-F, set it to the clock frequency higher than the CPU clock frequency.

20.4.11 Timer RD I/O Control Register Ai (TRDIORAi) (i = 0 or 1) [Timer mode (in Output Compare Function)]

Address 0141h (TRDIORA0), 0151h (TRDIORA1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRDGRA control bit	b1 b0 0 0: Disable pin output by the compare match (TRDIOAi pin functions as programmable I/O port) 0 1: “L” output at compare match with the TRDGRAi register 1 0: “H” output at compare match with the TRDGRAi register 1 1: Toggle output by compare match with the TRDGRAi register	R/W
b1	IOA1			R/W
b2	IOA2	TRDGRA mode select bit (1)	Set to 0 (output compare) in the output compare function.	R/W
b3	IOA3	Input capture input switch bit	Set to 1.	R/W
b4	IOB0	TRDGRB control bit	b5 b4 0 0: Disable pin output by the compare match (TRDIOBi pin functions as programmable I/O port) 0 1: “L” output at compare match with the TRDGRBi register 1 0: “H” output at compare match with the TRDGRBi 1 1: Toggle output by compare match with the TRDGRBi register	R/W
b5	IOB1			R/W
b6	IOB2	TRDGRB mode select bit (2)	Set to 0 (output compare) in the output compare function.	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Notes:
1. To select 1 (the TRDGRCi register is used as a buffer register of the TRDGRAi register) for this bit by the BFCi bit in the TRDMR register, set the IOC2 bit in the TRDIORCi register to the same value as the IOA2 bit in the TRDIORAi register.
2. To select 1 (the TRDGRDi register is used as a buffer register of the TRDGRBi register) for this bit by the BFDi bit in the TRDMR register, set the IOD2 bit in the TRDIORCi register to the same value as the IOB2 bit in the TRDIORAi register.

20.4.12 Timer RD I/O Control Register Ci (TRDIORCi) (i = 0 or 1) [Timer mode (in Output Compare Function)]

Address 0142h (TRDIORC0), 0152h (TRDIORC1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOC0	TRDGRC control bit	b1 b0 0 0: Disable pin output by compare match 0 1: "L" output at compare match with the TRDGRCi register 1 0: "H" output at compare match with the TRDGRCi register 1 1: Toggle output by compare match with the TRDGRCi register	R/W
b1	IOC1			R/W
b2	IOC2	TRDGRC mode select bit (1)	Set to 0 (output compare) in the output compare function.	R/W
b3	IOC3	TRDGRC register function select bit	0: TRDIOA output register (Refer to **20.4.20 Changing Output Pins in Registers TRDGRCi (i = 0 or 1) and TRDGRDi**.) 1: General register or buffer register	R/W
b4	IOD0	TRDGRD control bit	b5 b4 0 0: Disable pin output by compare match 0 1: "L" output at compare match with the TRDGRDi register 1 0: "H" output at compare match with the TRDGRDi register 1 1: Toggle output by compare match with the TRDGRDi register	R/W
b5	IOD1			R/W
b6	IOD2	TRDGRD mode select bit (2)	Set to 0 (output compare) in the output compare function.	R/W
b7	IOD3	TRDGRD register function select bit	0: TRDIOB output register (Refer to **20.4.20 Changing Output Pins in Registers TRDGRCi (i = 0 or 1) and TRDGRDi**.) 1: General register or buffer register	R/W

Notes:
1. To select 1 (the TRDGRCi register is used as a buffer register of the TRDGRAi register) for this bit by the BFCi bit in the TRDMR register, set the IOC2 bit in the TRDIORCi register to the same value as the IOA2 bit in the TRDIORAi register.
2. To select 1 (the TRDGRDi register is used as a buffer register of the TRDGRBi register) for this bit by the BFDi bit in the TRDMR register, set the IOD2 bit in the TRDIORCi register to the same value as the IOB2 bit in the TRDIORAi register.

20.4.13 Timer RD Status Register i (TRDSRi) (i = 0 or 1) [Timer mode (in Output Compare Function)]

Address 0143h (TRDSR0), 0153h (TRDSR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	UDF	OVF	IMFD	IMFC	IMFB	IMFA	
After Reset	1	1	1	0	0	0	0	0	TRDSR0 register
After Reset	1	1	0	0	0	0	0	0	TRDSR1 register

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input capture / compare match flag A	[Source for setting this bit to 0] Write 0 after read (2) [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRAi register.	R/W
b1	IMFB	Input capture / compare match flag B	[Source for setting this bit to 0] Write 0 after read (2) [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRBi register.	R/W
b2	IMFC	Input capture / compare match flag C	[Source for setting this bit to 0] Write 0 after read (2) [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRCi register (3).	R/W
b3	IMFD	Input capture / compare match flag D	[Source for setting this bit to 0] Write 0 after read (2) [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRDi register (3).	R/W
b4	OVF	Overflow flag	[Source for setting this bit to 0] Write 0 after read (2) [Source for setting this bit to 1] When the TRDi register overflows.	R/W
b5	UDF	Underflow flag (1)	This bit is disabled in the output compare function.	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b7	—			

Notes:
1. Nothing is assigned to b5 in the TRDSR0 register. When writing to b5, write 0. When reading, the content is 1.
2. The writing results are as follows:
   - This bit is set to 0 when the read result is 1 and 0 is written to the same bit.
   - This bit remains unchanged even if the read result is 0 and 0 is written to the same bit. (This bit remains 1 even if it is set to 1 from 0 after reading, and writing 0.)
   - This bit remains unchanged if 1 is written to it.
3. Including when the BFji bit in the TRDMR register is set to 1 (TRDGRji is used as the buffer register).

20.4.14 Timer RD Interrupt Enable Register i (TRDIERi) (i = 0 or 1) [Timer mode (in Output Compare Function)]

Address 0144h (TRDIER0), 0154h (TRDIER1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	OVIE	IMIED	IMIEC	IMIEB	IMIEA
After Reset	1	1	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input capture/compare match interrupt enable bit A	0: Disable interrupt (IMIA) by the IMFA bit 1: Enable interrupt (IMIA) by the IMFA bit	R/W
b1	IMIEB	Input capture/compare match interrupt enable bit B	0: Disable interrupt (IMIB) by the IMFB bit 1: Enable interrupt (IMIB) by the IMFB bit	R/W
b2	IMIEC	Input capture/compare match interrupt enable bit C	0: Disable interrupt (IMIC) by the IMFC bit 1: Enable interrupt (IMIC) by the IMFC bit	R/W
b3	IMIED	Input capture/compare match interrupt enable bit D	0: Disable interrupt (IMID) by the IMFD bit 1: Enable interrupt (IMID) by the IMFD bit	R/W
b4	OVIE	Overflow/underflow interrupt enable bit	0: Disable interrupt (OVI) by the OVF bit 1: Enable interrupt (OVI) by the OVF bit	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b6	—			
b7	—			

20.4.15 Timer RD Counter i (TRDi) (i = 0 or 1) [Timer mode (in Output Compare Function)]

Address 0147h to 0146h (TRD0), 0157h to 0156h (TRD1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15 to b0	Count the count source. Count operation is incremented. When an overflow occurs, the OVF bit in the TRDSRi register is set to 1.	0000h to FFFFh	R/W

Access the TRDi register in 16-bit units. Do not access it in 8-bit units.

20.4.16 Timer RD General Registers Ai, Bi, Ci, and Di (TRDGRAi, TRDGRBi, TRDGRCi, TRDGRDi) (i = 0 or 1) [Timer mode (in Output Compare Function)]

Address 0149h to 0148h (TRDGRA0), 014Bh to 014Ah (TRDGRB0),
014Dh to 014Ch (TRDGRC0), 014Fh to 014Eh (TRDGRD0),
0159h to 0158h (TRDGRA1), 015Bh to 015Ah (TRDGRB1),
015Dh to 015Ch (TRDGRC1), 015Fh to 015Eh (TRDGRD1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b15 to b0	Refer to **Table 20.8 TRDGRji Register Function in Output Compare Function**	R/W

Access registers TRDGRAi to TRDGRDi in 16-bit units. Do not access them in 8-bit units.

The following registers are disabled in the output compare function: TRDDF0, TRDDF1, TRDPOCR0, and TRDPOCR1.

Table 20.8 TRDGRji Register Function in Output Compare Function

Register	Setting		Register Function		Output-Compare Output Pin
	BFji	IOj3			
TRDGRAi	–	–	General register. Write the compare value.		TRDIOAi
TRDGRBi					TRDIOBi
TRDGRCi	0	1	General register. Write the compare value.		TRDIOCi
TRDGRDi					TRDIODi
TRDGRCi	1	1	Buffer register. Write the next compare value		TRDIOAi
TRDGRDi			(Refer to **20.2.2 Buffer Operation**.)		TRDIOBi
TRDGRCi	0	0	TRDIOAi output control	(Refer to **20.4.20 Changing Output Pins in Registers TRDGRCi (i = 0 or 1) and TRDGRDi**.)	TRDIOAi
TRDGRDi			TRDIOBi output control		TRDIOBi

i = 0 or 1, j = either A, B, C, or D
BFji: Bit in TRDMR register IOj3: Bit in TRDIORCi register

20.4.17 Timer RD Pin Select Register 0 (TRDPSR0)

Address 0184h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	TRDIOD0SEL0	—	TRDIOC0SEL0	—	TRDIOB0SEL0	—	TRDIOA0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRDIOA0SEL0	TRDIOA0/TRDCLK pin select bit	0: TRDIOA0/TRDCLK pin not used 1: P2_0 assigned	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	TRDIOB0SEL0	TRDIOB0 pin select bit	0: TRDIOB0 pin not used 1: P2_1 assigned	R/W
b3	—	Reserved bit	Set to 0.	R/W
b4	TRDIOC0SEL0	TRDIOC0 pin select bit	0: TRDIOC0 pin not used 1: P2_2 assigned	R/W
b5	—	Reserved bit	Set to 0.	R/W
b6	TRDIOD0SEL0	TRDIOD0 pin select bit	0: TRDIOD0 pin not used 1: P2_3 assigned	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

The TRDPSR0 register selects which pin is assigned to the timer RD I/O. To use the I/O pin for timer RD, set this register.
Set the TRDPSR0 register before setting the timer RD associated registers. Also, do not change the setting value in this register during timer RD operation.

20.4.18 Timer RD Pin Select Register 1 (TRDPSR1)

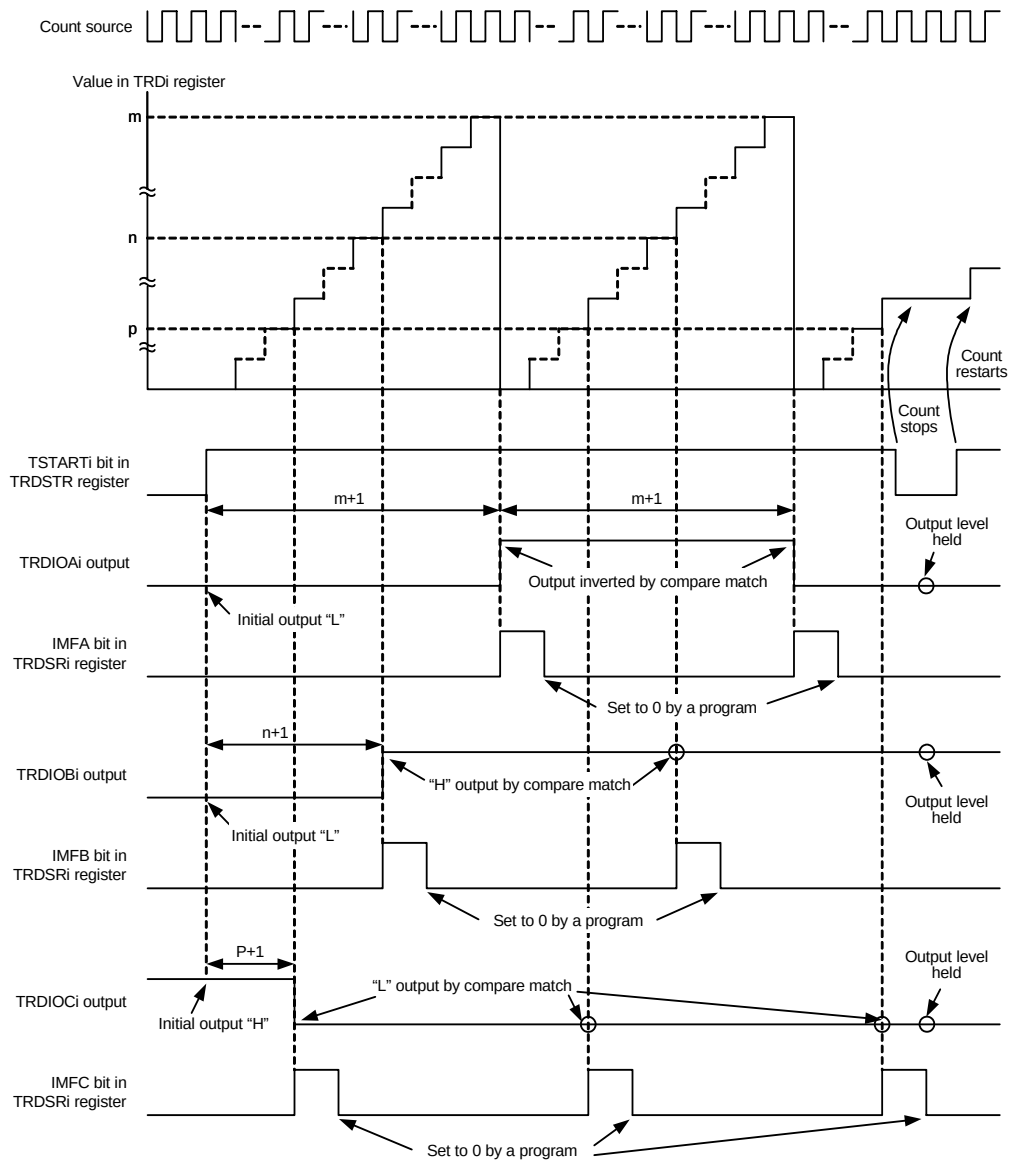
Address 0185h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	TRDIOD1SEL0	—	TRDIOC1SEL0	—	TRDIOB1SEL0	—	TRDIOA1SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRDIOA1SEL0	TRDIOA1 pin select bit	0: TRDIOA1 pin not used 1: P2_4 assigned	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	TRDIOB1SEL0	TRDIOB1 pin select bit	0: TRDIOB1 pin not used 1: P2_5 assigned	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TRDIOC1SEL0	TRDIOC1 pin select bit	0: TRDIOC1 pin not used 1: P2_6 assigned	R/W
b5	—	Reserved bit	Set to 0.	R/W
b6	TRDIOD1SEL0	TRDIOD1 pin select bit	0: TRDIOD1 pin not used 1: P2_7 assigned	R/W
b7	—	Reserved bit	Set to 0.	R/W

The TRDPSR1 register selects which pin is assigned to the timer RD I/O. To use the I/O pin for timer RD, set this register.
Set the TRDPSR1 register before setting the timer RD associated registers. Also, do not change the setting value in this register during timer RD operation.

20.4.19 Operating Example



i = 0 or 1

M: Value set in TRDGRAi register
n: Value set in TRDGRBi register
p: Value set in TRDGRCi register

The above applies under the following conditions:
The CSELi bit in the TRDSTR register is set to 1 (the TRDi register is not stopped by compare match).
Bits BFCi and BFDi in the TRDMR register are set to 0 (registers TRDGRCi and TRDGRDi are not used as buffer registers).
Bits EAi, EBi, and ECi in the TRDOER1 register are set to 0 (enable the TRDIOAi, TRDIOBi and TRDIOCi pin outputs).
Bits CCLR2 to CCLR0 in the TRDCRi register are set to 001b (set the TRDi register to 000h by compare match in the TRDGRAi register).
Bits TOAi and TOBi in the TRDOCR register is set to 0 (initial output "L" to compare match), the TOCi bit is set to 1 (initial output "H" to compare match).
Bits IOA2 to IOA0 in the TRDIORAi register are set to 011b (TRDIOAi output inverted at TRDGRAi register compare match).
Bits IOB2 to IOB0 in the TRDIORAi register are set to 010b (TRDIOBi "H" output at TRDGRBi register compare match).
Bits IOC3 to IOC0 in the TRDIORCi register are set to 1001b (TRDIOCi "L" output at TRDGRCi register compare match).
Set bits IOD3 to IOD0 in the TRDIORCi register to 1000b (TRDGRDi register does not control TRDIOBi pin output, pin output at compare match is disabled).

Figure 20.11 Operating Example of Output Compare Function

20.4.20 Changing Output Pins in Registers TRDGRCi (i = 0 or 1) and TRDGRDi

The TRDGRCi register can be used for output control of the TRDIOAi pin, and the TRDGRDi register can be used for output control of the TRDIOBi pin. Therefore, each pin output can be controlled as follows:

- TRDIOAi output is controlled by the values in registers TRDGRAi and TRDGRCi.
- TRDIOBi output is controlled by the values in registers TRDGRBi and TRDGRDi.

Change output pins in registers TRDGRCi and TRDGRDi as follows:

- Select 0 (change TRDGRji register output pin) by the IOj3 (j = C or D) bit in the TRDIORCi register.
- Set the BFji bit in the TRDMR register to 0 (general register).
- Set different values in registers TRDGRCi and TRDGRAi. Also, set different values in registers TRDGRDi and TRDGRBi.

Figure 20.13 shows an Operating Example When TRDGRCi Register is Used for Output Control of TRDIOAi Pin and TRDGRDi Register is Used for Output Control of TRDIOBi Pin.

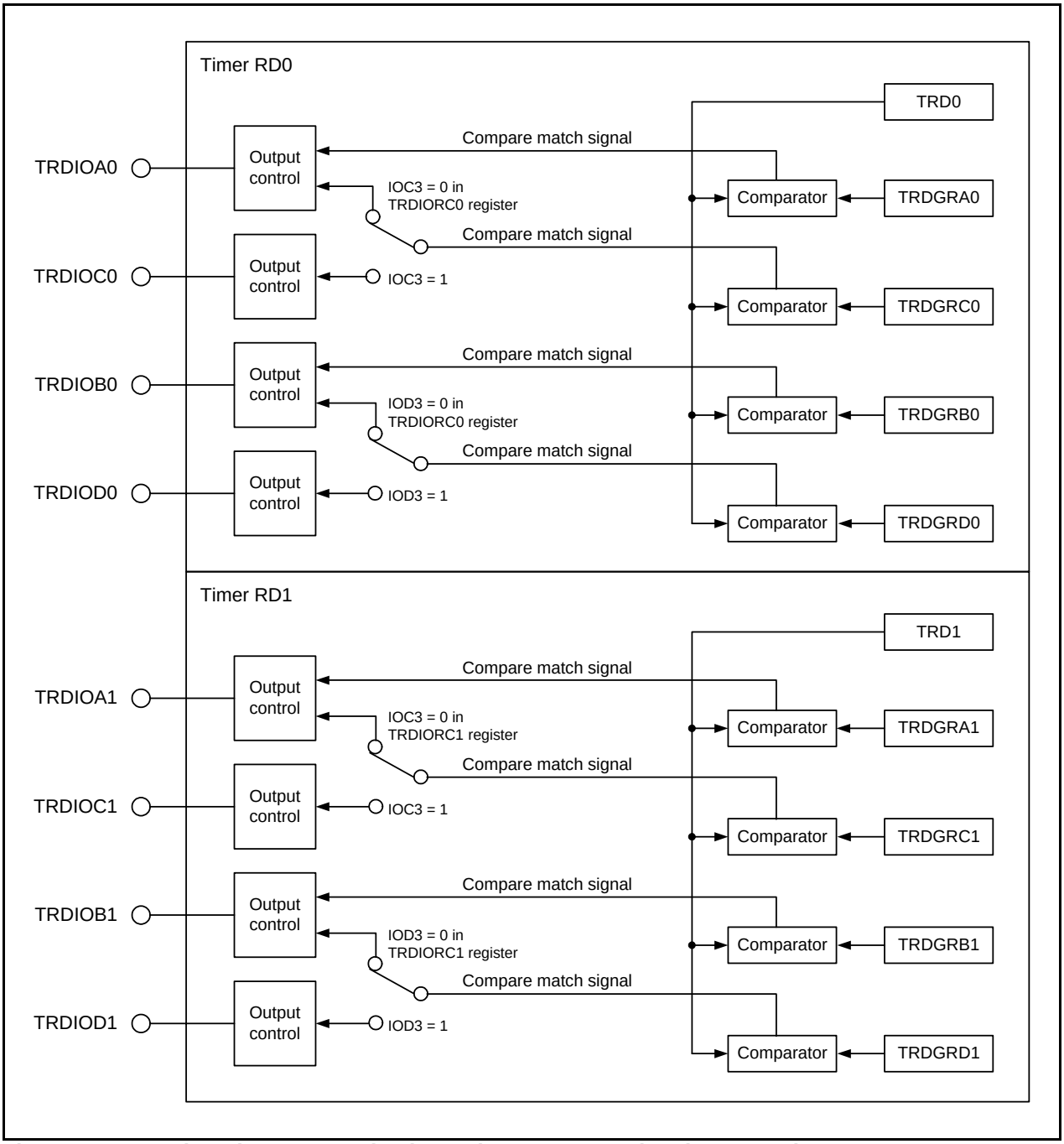
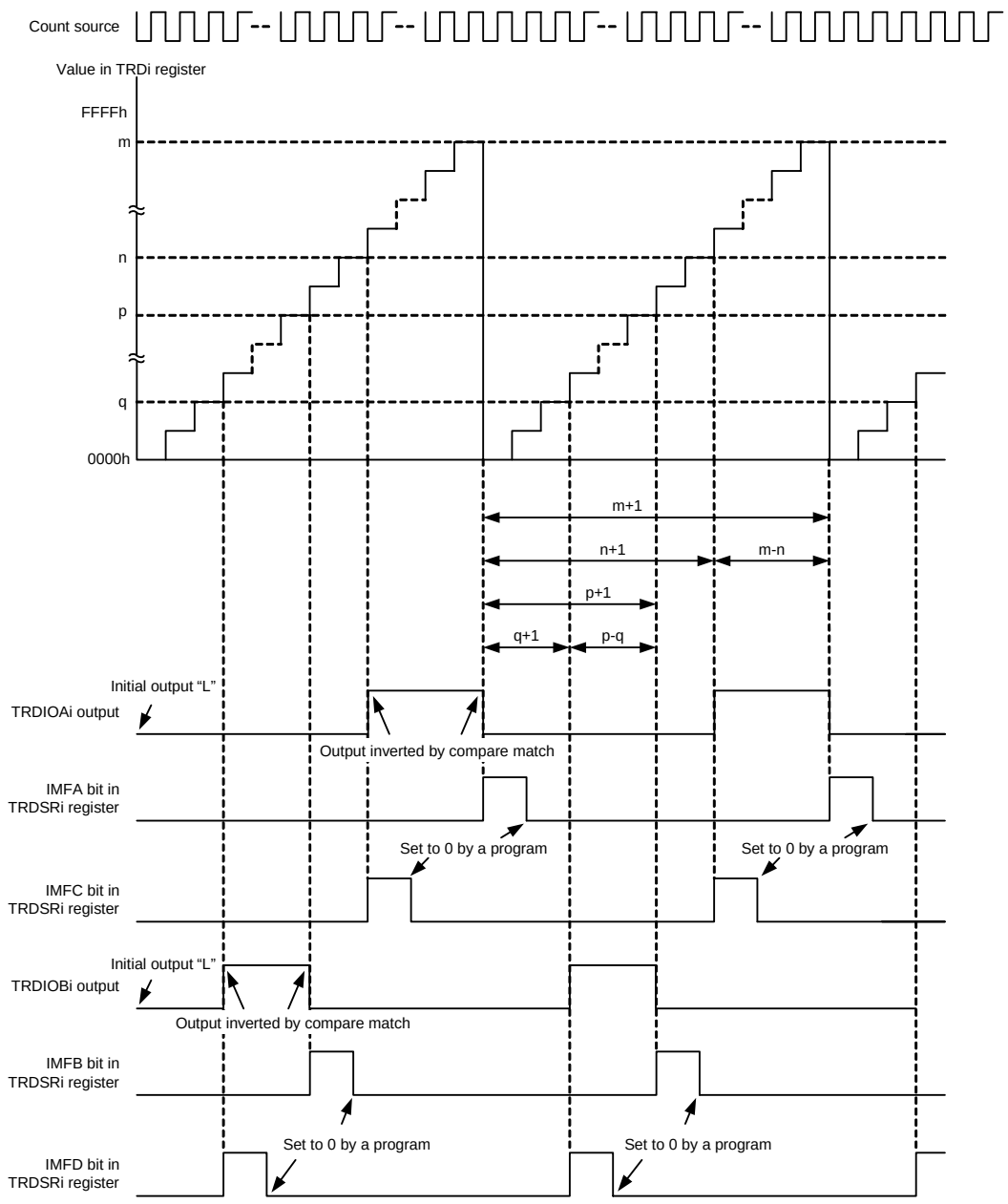


Figure 20.12 Changing Output Pins in Registers TRDGRCi and TRDGRDi



m: Value set in TRDGRAi register
n: Value set in TRDGRCi register
p: Value set in TRDGRBi register
q: Value set in TRDGRDi register

i = 0 or 1

The above applies under the following conditions:
The CSELi bit in the TRDSTR register is set to 1 (the TRDi register is not stopped by compare match).
Bits BFCi and BFDi in the TRDMR register are set to 0 (registers TRDGRCi and TRDGRDi are not used as buffer register).
Bits EAi and EBi in the TRDOER1 register are set to 0 (enable TRDIOAi and TRDIOBi pin outputs).
Bits CCLR2 to CCLR0 in the TRDCRi register are set to 001b (set the TRDi register to 0000h by compare match in the TRDGRAi register).
Bits TOAi and TOBi in the TRDOCR register are set to 0 (initial output "L" to compare match).
Bits IOA2 to IOA0 in the TRDIORAi register are set to 011b (TRDIOAi output inverted at TRDGRAi register compare match).
Bits IOB2 to IOB0 in the TRDIORAi register are set to 011b (TRDIOBi output inverted at TRDGRBi register compare match).
Bits IOC3 to IOC0 in the TRDIORCi register are set to 0011b (TRDIOAi output inverted at TRDGRCi register compare match).
Bits IOD3 to IOD0 in the TRDIORCi register are set to 0011b (TRDIOBi output inverted at TRDGRDi register compare match).

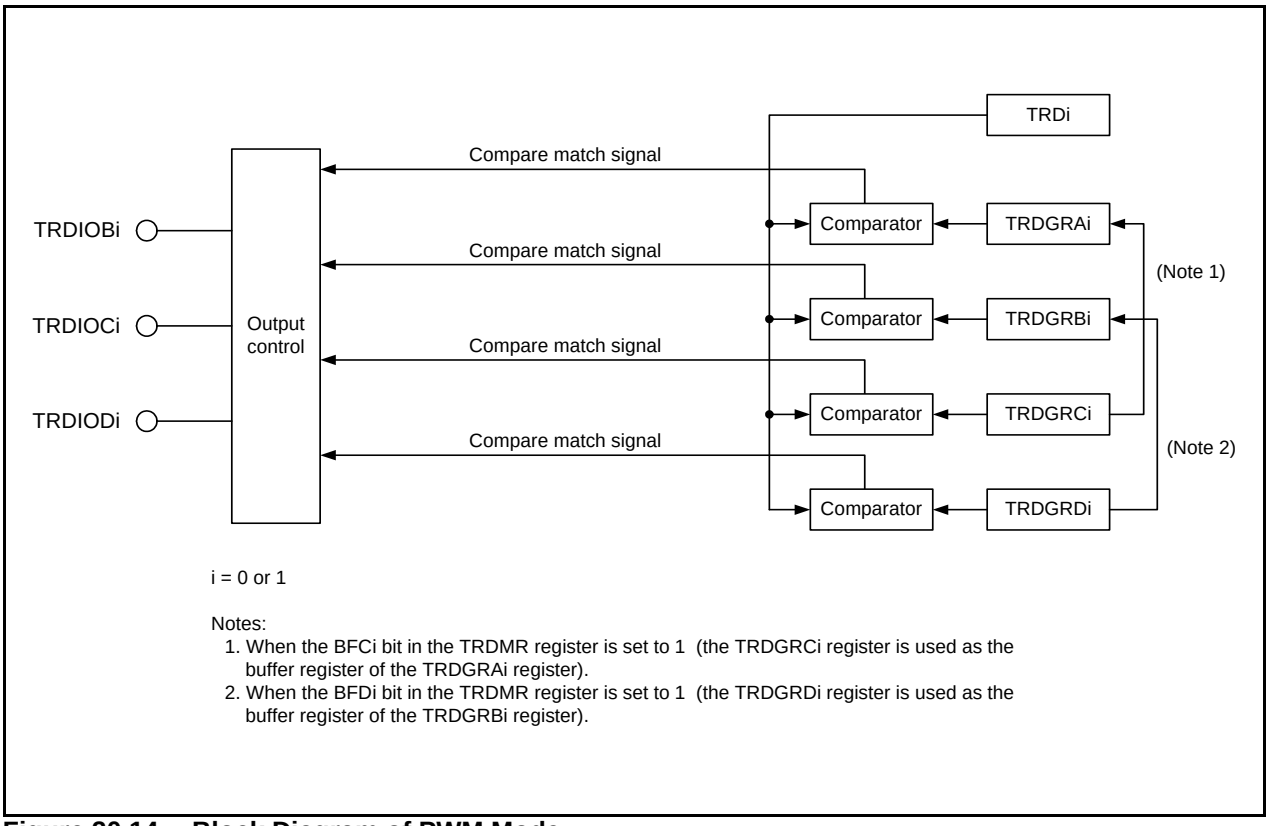
Figure 20.13 Operating Example When TRDGRCi Register is Used for Output Control of TRDIOAi Pin and TRDGRDi Register is Used for Output Control of TRDIOBi Pin

20.4.21 A/D Trigger Generation

A compare match signal with registers TRDi (i = 0 or 1) and TRDGRji (j = A, B, C, or D) can be used as the conversion start trigger of the A/D converter.
The TRDADCR register is used to select which compare match is used.

20.5 PWM Mode

In PWM mode, a PWM waveform is output. Up to 3 PWM waveforms with the same period can be output by timer RDi (i = 0 to 1). Also, up to 6 PWM waveforms with the same period can be output by synchronizing timer RD0 and timer RD1. Since this mode functions by a combination of the TRDIOji (i = 0 or 1, j = B, C, or D) pin and TRDGRji register, the PWM mode, or any other mode or function, can be selected for each individual pin. (However, since the TRDGRAi register is used when using any pin for PWM mode, the TRDGRAi register cannot be used for other modes.)
Figure 20.14 shows a Block Diagram of PWM Mode, and Table 20.9 lists the PWM Mode Specifications. Figures 20.15 and 20.16 show the Operations of PWM Mode.

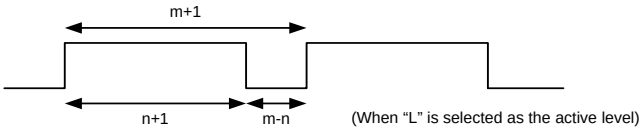


i = 0 or 1

Notes:
1. When the BFCi bit in the TRDMR register is set to 1 (the TRDGRCi register is used as the buffer register of the TRDGRAi register).
2. When the BFDi bit in the TRDMR register is set to 1 (the TRDGRDi register is used as the buffer register of the TRDGRBi register).

Figure 20.14 Block Diagram of PWM Mode

Table 20.9 PWM Mode Specifications

Item	Specification
Count sources	f1, f2, f4, f8, f32, fOCO40M, fOCO-F External signal input to the TRDCLK pin (valid edge selected by a program)
Count operations	Increment
PWM waveform	PWM period: 1/fk x (m+1) Active level width: 1/fk x (m-n) Inactive level width: 1/fk x (n+1) fk: Frequency of count source m: Value set in the TRDGRAi register n: Value set in the TRDGRji register 
Count start condition	1 (count starts) is written to the TSTARTi bit in the TRDSTR register.
Count stop conditions	• 0 (count stops) is written to the TSTARTi bit in the TRDSTR register when the CSELi bit in the TRDSTR register is set to 1. The PWM output pin holds output level before the count stops. • When the CSELi bit in the TRDSTR register is set to 0, the count stops at the compare match in the TRDGRAi register. The PWM output pin holds level after output change by compare match.
Interrupt request generation timing	• Compare match (The content of the TRDi register matches content of the TRDGRhi register.) • TRDi register overflows
TRDIOA0 pin function	Programmable I/O port or TRDCLK (external clock) input
TRDIOA1 pin function	Programmable I/O port
TRDIOB0, TRDIOC0, TRDIOD0, TRDIOB1, TRDIOC1, TRDIOD1 pin functions	Programmable I/O port or pulse output (selectable by pin)
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRDi register.
Write to timer	The value can be written to the TRDi register.
Selectable functions	• One to three PWM output pins selectable with timer RDi Either 1 pin or multiple pins of the TRDIOBi, TRDIOCi or TRDIODi pin. • Active level selectable for each pin. • Initial output level selectable for each pin. • Synchronous operation (Refer to **20.2.3 Synchronous Operation**.) • Buffer operation (Refer to **20.2.2 Buffer Operation**.) • Pulse output forced cutoff signal input (Refer to **20.2.4 Pulse Output Forced Cutoff**.) • A/D trigger generation

i = 0 or 1
j = either B, C, or D
h = either A, B, C, or D

20.5.1 Module Standby Control Register (MSTCR)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	MSTTRG	MSTTRC	MSTTRD	MSTIIC	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	MSTIIC	SSU standby bit	0: Active 1: Standby (1)	R/W
b4	MSTTRD	Timer RD standby bit	0: Active 1: Standby (2, 3)	R/W
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (4)	R/W
b6	MSTTRG	Timer RG standby bit	0: Active 1: Standby (5)	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. When the MSTIIC bit is set to 1 (standby), any access to the SSU associated registers (addresses 0193h to 019Dh) is disabled.
2. When the MSTTRD bit is set to 1 (standby), any access to the timer RD associated registers (addresses 0136h to 015Fh) is disabled.
3. To set the MSTTRD bit to 1 (standby), set bits TCK2 to TCK0 in the TRDCRi (i = 0 or 1) register to 000b (f1).
4. When the MSTTRC bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0120h to 0133h) is disabled.
5. When the MSTTRG bit is set to 1 (standby), any access to the timer RG associated registers (addresses 0170h to 017Fh) is disabled.

20.5.2 Timer RD Trigger Control Register (TRDADCR)

Address 0136h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADTRGD1E	ADTRGC1E	ADTRGB1E	ADTRGA1E	ADTRGD0E	ADTRGC0E	ADTRGB0E	ADTRGA0E
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADTRGA0E	A/D trigger A0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRA0	R/W
b1	ADTRGB0E	A/D trigger B0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRB0	R/W
b2	ADTRGC0E	A/D trigger C0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRC0	R/W
b3	ADTRGD0E	A/D trigger D0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRD0	R/W
b4	ADTRGA1E	A/D trigger A1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRA1	R/W
b5	ADTRGB1E	A/D trigger B1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRB1	R/W
b6	ADTRGC1E	A/D trigger C1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRC1	R/W
b7	ADTRGD1E	A/D trigger D1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRD1	R/W

20.5.3 Timer RD Start Register (TRDSTR) in PWM Mode

Address 0137h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	CSEL1	CSEL0	TSTART1	TSTART0
After Reset	1	1	1	1	1	1	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART0	TRD0 count start flag (3)	0: Count stops (1) 1: Count starts	R/W
b1	TSTART1	TRD1 count start flag (4)	0: Count stops (2) 1: Count starts	R/W
b2	CSEL0	TRD0 count operation select bit	0: Count stops at the compare match with the TRDGRA0 register 1: Count continues after the compare match with the TRDGRA0 register	R/W
b3	CSEL1	TRD1 count operation select bit	0: Count stops at the compare match with the TRDGRA1 register 1: Count continues after the compare match with the TRDGRA1 register	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	—			

Notes:
1. When the CSEL0 bit is set to 1, write 0 to the TSTART0 bit.
2. When the CSEL1 bit is set to 1, write 0 to the TSTART1 bit.
3. When the CSEL0 bit is set to 0 and the compare match signal (TRDIOA0) is generated, this bit is set to 0 (count stops).
4. When the CSEL1 bit is set to 0 and the compare match signal (TRDIOA1) is generated, this bit is set to 0 (count stops).

Set the TRDSTR register using the MOV instruction (do not use the bit handling instruction). Refer to **20.10.1 TRDSTR Register** of **Notes on Timer RD**.

20.5.4 Timer RD Mode Register (TRDMR) in PWM Mode

Address 0138h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BFD1	BFC1	BFD0	BFC0	—	—	—	SYNC
After Reset	0	0	0	0	1	1	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	SYNC	Timer RD synchronous bit	0: Registers TRD0 and TRD1 operate independently 1: Registers TRD0 and TRD1 operate synchronously	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b2	—			
b3	—			
b4	BFC0	TRDGRC0 register function select bit	0: General register 1: Buffer register of TRDGRA0 register	R/W
b5	BFD0	TRDGRD0 register function select bit	0: General register 1: Buffer register of TRDGRB0 register	R/W
b6	BFC1	TRDGRC1 register function select bit	0: General register 1: Buffer register of TRDGRA1 register	R/W
b7	BFD1	TRDGRD1 register function select bit	0: General register 1: Buffer register of TRDGRB1 register	R/W

20.5.5 Timer RD PWM Mode Register (TRDPMR) in PWM Mode

Address 0139h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	PWMD1	PWMC1	PWMB1	—	PWMD0	PWMC0	PWMB0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PWMB0	PWM mode of TRDIOB0 select bit	0: Timer mode 1: PWM mode	R/W
b1	PWMC0	PWM mode of TRDIOC0 select bit		R/W
b2	PWMD0	PWM mode of TRDIOD0 select bit		R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b4	PWMB1	PWM mode of TRDIOB1 select bit	0: Timer mode 1: PWM mode	R/W
b5	PWMC1	PWM mode of TRDIOC1 select bit		R/W
b6	PWMD1	PWM mode of TRDIOD1 select bit		R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

20.5.6 Timer RD Function Control Register (TRDFCR) in PWM Mode

Address 013Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PWM3	STCLK	ADEG	ADTRG	OLS1	OLS0	CMD1	CMD0
After Reset	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CMD0	Combination mode select bit (1)	Set to 00b (timer mode, PWM mode, or PWM3 mode) in PWM mode.	R/W
b1	CMD1			R/W
b2	OLS0	Normal-phase output level select bit (in reset synchronous PWM mode or complementary PWM mode)	This bit is disabled in PWM mode.	R/W
b3	OLS1	Counter-phase output level select bit (in reset synchronous PWM mode or complementary PWM mode)		R/W
b4	ADTRG	A/D trigger enable bit (in complementary PWM mode)		R/W
b5	ADEG	A/D trigger edge select bit (in complementary PWM mode)		R/W
b6	STCLK	External clock input select bit	0: External clock input disabled 1: External clock input enabled	R/W
b7	PWM3	PWM3 mode select bit (2)	Set this bit to 1 (other than PWM3 mode) in PWM mode.	R/W

Notes:
1. Set bits CMD1 to CMD0 when both the TSTART0 and TSTART1 bits in the TRDSTR register are set to 0 (count stops).
2. When bits CMD1 to CMD0 are set to 00b (timer mode, PWM mode, or PWM3 mode), the setting of the PWM3 bit is enabled.

20.5.7 Timer RD Output Master Enable Register 1 (TRDOER1) in PWM Mode

Address 013Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ED1	EC1	EB1	EA1	ED0	EC0	EB0	EA0
After Reset	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	EA0	TRDIOA0 output disable bit	Set this bit to 1 (the TRDIOA0 pin is used as a programmable I/O port) in PWM mode.	R/W
b1	EB0	TRDIOB0 output disable bit	0: Enable output 1: Disable output (The TRDIOB0 pin is used as a programmable I/O port.)	R/W
b2	EC0	TRDIOC0 output disable bit	0: Enable output 1: Disable output (The TRDIOC0 pin is used as a programmable I/O port.)	R/W
b3	ED0	TRDIOD0 output disable bit	0: Enable output 1: Disable output (The TRDIOD0 pin is used as a programmable I/O port.)	R/W
b4	EA1	TRDIOA1 output disable bit	Set this bit to 1 (the TRDIOA1 pin is used as a programmable I/O port) in PWM mode.	R/W
b5	EB1	TRDIOB1 output disable bit	0: Enable output 1: Disable output (The TRDIOB1 pin is used as a programmable I/O port.)	R/W
b6	EC1	TRDIOC1 output disable bit	0: Enable output 1: Disable output (The TRDIOC1 pin is used as a programmable I/O port.)	R/W
b7	ED1	TRDIOD1 output disable bit	0: Enable output 1: Disable output (The TRDIOD1 pin is used as a programmable I/O port.)	R/W

20.5.8 Timer RD Output Master Enable Register 2 (TRDOER2) in PWM Mode

Address 013Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PTO	—	—	—	—	—	—	—
After Reset	0	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	PTO	$\overline{\text{INT0}}$ of pulse output forced cutoff signal input enabled bit (1)	0: Pulse output forced cutoff input disabled 1: Pulse output forced cutoff input enabled (All bits in the TRDOER1 register are set to 1 (disable output) when “L” is applied to the $\overline{\text{INT0}}$ pin.)	R/W

Note:
1. Refer to **20.2.4 Pulse Output Forced Cutoff**.

20.5.9 Timer RD Output Control Register (TRDOCR) in PWM Mode

Address 013Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TOD1	TOC1	TOB1	TOA1	TOD0	TOC0	TOB0	TOA0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA0	TRDIOA0 output level select bit	Set this bit to 0 (enable output) in PWM mode.	R/W
b1	TOB0	TRDIOB0 output level select bit (1)	0: Initial output is inactive level 1: Initial output is active level	R/W
b2	TOC0	TRDIOC0 initial output level select bit (1)		R/W
b3	TOD0	TRDIOD0 initial output level select bit (1)		R/W
b4	TOA1	TRDIOA1 initial output level select bit	Set this bit to 0 (enable output) in PWM mode.	R/W
b5	TOB1	TRDIOB1 initial output level select bit (1)	0: Inactive level 1: Active level	R/W
b6	TOC1	TRDIOC1 initial output level select bit (1)		R/W
b7	TOD1	TRDIOD1 initial output level select bit (1)		R/W

Note:
1. If the pin function is set for waveform output (refer to **7.5 Port Settings**), the initial output level is output when the TRDOCR register is set.

   Write to the TRDOCR register when both the TSTART0 and TSTART1 bits in the TRDSTR register are set to 0 (count stops).

20.5.10 Timer RD Control Register i (TRDCRi) (i = 0 or 1) in PWM Mode

Address 0140h (TRDCR0), 0150h (TRDCR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TCK2	TCK1	TCK0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TCK0	Count source select bit	b2 b1 b0 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRDCLK input (1) 1 1 0: fOCO40M 1 1 1: fOCO-F (3)	R/W
b1	TCK1			R/W
b2	TCK2			R/W
b3	CKEG0	External clock edge select bit (2)	b4 b3 0 0: Count at the rising edge 0 1: Count at the falling edge 1 0: Count at both edges 1 1: Do not set.	R/W
b4	CKEG1			R/W
b5	CCLR0	TRDi counter clear select bit	Set to 001b (the TRDi register cleared at compare match with TRDGRAi register) in PWM mode.	R/W
b6	CCLR1			R/W
b7	CCLR2			R/W

Notes:
1. Enabled when the STCLK bit in the TRDFCR register is 1 (external clock input enabled).
2. Enabled when bits TCK2 to TCK0 are set to 101b (TRDCLK input) and the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).
3. To select fOCO-F, set it to the clock frequency higher than the CPU clock frequency.

20.5.11 Timer RD Status Register i (TRDSRi) (i = 0 or 1) in PWM Mode

Address 0143h (TRDSR0), 0153h (TRDSR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	UDF	OVF	IMFD	IMFC	IMFB	IMFA	
After Reset	1	1	1	0	0	0	0	0	TRDSR0 register
After Reset	1	1	0	0	0	0	0	0	TRDSR1 register

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input capture / compare match flag A	[Source for setting this bit to 0] Write 0 after read (2) [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRAi register.	R/W
b1	IMFB	Input capture / compare match flag B	[Source for setting this bit to 0] Write 0 after read (2) [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRBi register.	R/W
b2	IMFC	Input capture / compare match flag C	[Source for setting this bit to 0] Write 0 after read (2) [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRCi register (3).	R/W
b3	IMFD	Input capture / compare match flag D	[Source for setting this bit to 0] Write 0 after read (2) [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRDi register (3).	R/W
b4	OVF	Overflow flag	[Source for setting this bit to 0] Write 0 after read (2) [Source for setting this bit to 1] When the TRDi register overflows.	R/W
b5	UDF	Underflow flag (1)	This bit is disabled in PWM Mode.	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b7	—			

Notes:
1. Nothing is assigned to b5 in the TRDSR0 register. When writing to b5, write 0. When reading, the content is 1.
2. The writing results are as follows:
   - This bit is set to 0 when the read result is 1 and 0 is written to the same bit.
   - This bit remains unchanged even if the read result is 0 and 0 is written to the same bit. (This bit remains 1 even if it is set to 1 from 0 after reading, and writing 0.)
   - This bit remains unchanged if 1 is written to it.
3. Including when the BFji bit in the TRDMR register is set to 1 (TRDGRji is used as the buffer register).

20.5.12 Timer RD Interrupt Enable Register i (TRDIERi) (i = 0 or 1) in PWM Mode

Address 0144h (TRDIER0), 0154h (TRDIER1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	OVIE	IMIED	IMIEC	IMIEB	IMIEA
After Reset	1	1	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input capture/compare match interrupt enable bit A	0: Disable interrupt (IMIA) by the IMFA bit 1: Enable interrupt (IMIA) by the IMFA bit	R/W
b1	IMIEB	Input capture/compare match interrupt enable bit B	0: Disable interrupt (IMIB) by the IMFB bit 1: Enable interrupt (IMIB) by the IMFB bit	R/W
b2	IMIEC	Input capture/compare match interrupt enable bit C	0: Disable interrupt (IMIC) by the IMFC bit 1: Enable interrupt (IMIC) by the IMFC bit	R/W
b3	IMIED	Input capture/compare match interrupt enable bit D	0: Disable interrupt (IMID) by the IMFD bit 1: Enable interrupt (IMID) by the IMFD bit	R/W
b4	OVIE	Overflow/underflow interrupt enable bit	0: Disable interrupt (OVI) by the OVF bit 1: Enable interrupt (OVI) by the OVF bit	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b6	—			
b7	—			

20.5.13 Timer RD PWM Mode Output Level Control Register i (TRDPOCRi) (i = 0 or 1) in PWM Mode

Address 0145h (TRDPOCR0), 0155h (TRDPOCR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	POLD	POLC	POLB
After Reset	1	1	1	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POLB	PWM mode output level control bit B	0: “L” active TRDIOBi output level is selected 1: “H” active TRDIOBi output level is selected	R/W
b1	POLC	PWM mode output level control bit C	0: “L” active TRDIOCi output level is selected 1: “H” active TRDIOCi output level is selected	R/W
b2	POLD	PWM mode output level control bit D	0: “L” active TRDIODi output level is selected 1: “H” active TRDIODi output level is selected	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b4	—			
b5	—			
b6	—			
b7	—			

20.5.14 Timer RD Counter i (TRDi) (i = 0 or 1) in PWM Mode

Address 0147h to 0146h (TRD0), 0157h to 0156h (TRD1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15 to b0	Count the count source. Count operation is incremented. When an overflow occurs, the OVF bit in the TRDSRi register is set to 1.	0000h to FFFFh	R/W

Access the TRDi register in 16-bit units. Do not access it in 8-bit units.

20.5.15 Timer RD General Registers Ai, Bi, Ci, and Di (TRDGRAi, TRDGRBi, TRDGRCi, TRDGRDi) (i = 0 or 1) in PWM Mode

Address 0149h to 0148h (TRDGRA0), 014Bh to 014Ah (TRDGRB0),
014Dh to 014Ch (TRDGRC0), 014Fh to 014Eh (TRDGRD0),
0159h to 0158h (TRDGRA1), 015Bh to 015Ah (TRDGRB1),
015Dh to 015Ch (TRDGRC1), 015Fh to 015Eh (TRDGRD1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b15 to b0	Refer to **Table 20.10 TRDGRji Register Functions in PWM Mode**	R/W

Access registers TRDGRAi to TRDGRDi in 16-bit units. Do not access them in 8-bit units.

The following registers are disabled in the PWM mode: TRDDF0, TRDDF1, TRDIORA0, TRDIORC0, TRDIORA1, and TRDIORC1.

Table 20.10 TRDGRji Register Functions in PWM Mode

Register	Setting	Register Function	PWM Output Pin
TRDGRAi	–	General register. Set the PWM period	–
TRDGRBi	–	General register. Set the changing point of PWM output	TRDIOBi
TRDGRCi	BFCi = 0	General register. Set the changing point of PWM output	TRDIOCi
TRDGRDi	BFDi = 0		TRDIODi
TRDGRCi	BFCi = 1	Buffer register. Set the next PWM period (Refer to **20.2.2 Buffer Operation**.)	–
TRDGRDi	BFDi = 1	Buffer register. Set the changing point of the next PWM output (Refer to **20.2.2 Buffer Operation**.)	TRDIOBi

i = 0 or 1
BFCi, BFDi: Bits in TRDMR register

20.5.16 Timer RD Pin Select Register 0 (TRDPSR0)

Address 0184h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	TRDIOD0SEL0	—	TRDIOC0SEL0	—	TRDIOB0SEL0	—	TRDIOA0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRDIOA0SEL0	TRDIOA0/TRDCLK pin select bit	0: TRDIOA0/TRDCLK pin not used 1: P2_0 assigned	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	TRDIOB0SEL0	TRDIOB0 pin select bit	0: TRDIOB0 pin not used 1: P2_1 assigned	R/W
b3	—	Reserved bit	Set to 0.	R/W
b4	TRDIOC0SEL0	TRDIOC0 pin select bit	0: TRDIOC0 pin not used 1: P2_2 assigned	R/W
b5	—	Reserved bit	Set to 0.	R/W
b6	TRDIOD0SEL0	TRDIOD0 pin select bit	0: TRDIOD0 pin not used 1: P2_3 assigned	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

The TRDPSR0 register selects which pin is assigned to the timer RD I/O. To use the I/O pin for timer RD, set this register.
Set the TRDPSR0 register before setting the timer RD associated registers. Also, do not change the setting value in this register during timer RD operation.

20.5.17 Timer RD Pin Select Register 1 (TRDPSR1)

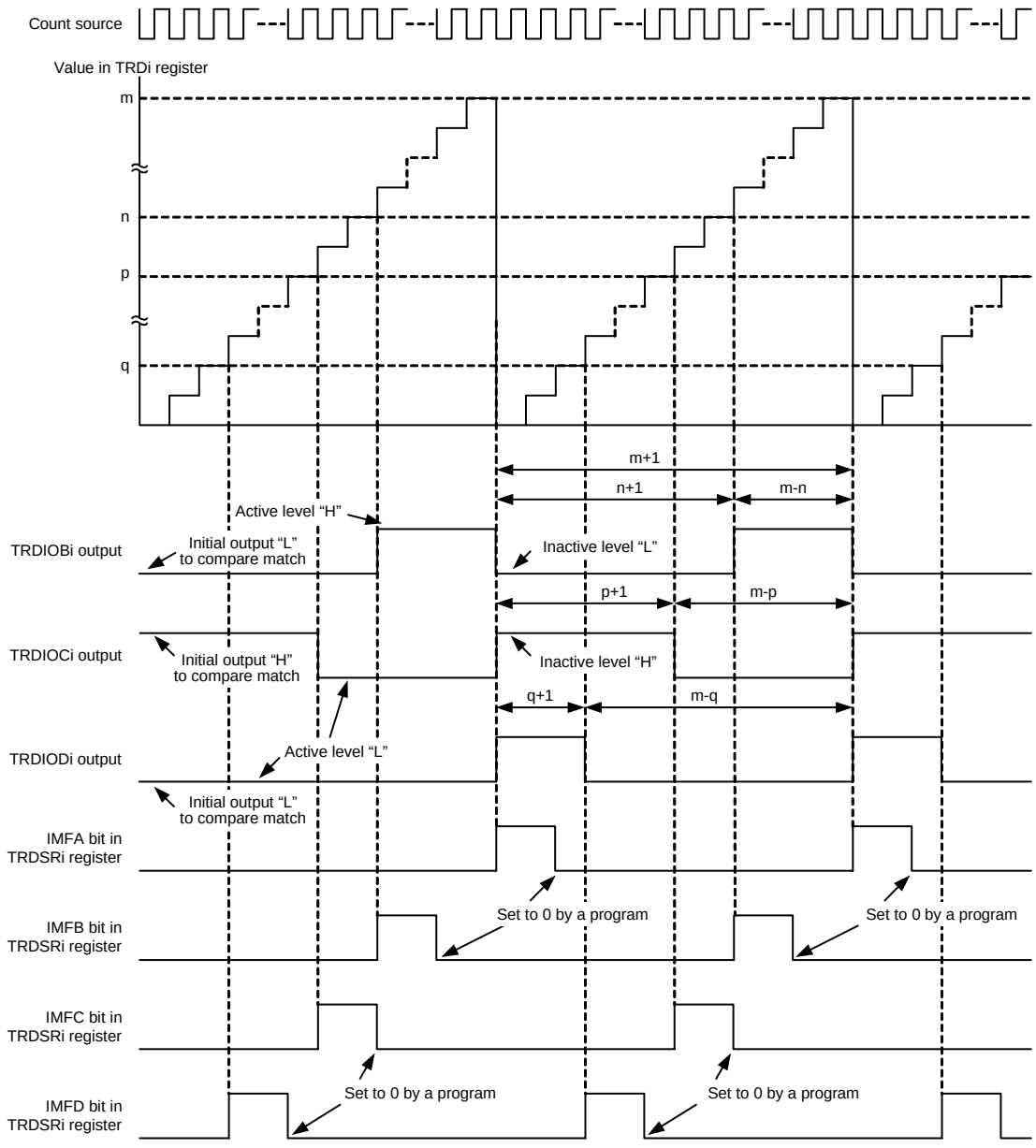
Address 0185h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	TRDIOD1SEL0	—	TRDIOC1SEL0	—	TRDIOB1SEL0	—	TRDIOA1SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRDIOA1SEL0	TRDIOA1 pin select bit	0: TRDIOA1 pin not used 1: P2_4 assigned	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	TRDIOB1SEL0	TRDIOB1 pin select bit	0: TRDIOB1 pin not used 1: P2_5 assigned	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TRDIOC1SEL0	TRDIOC1 pin select bit	0: TRDIOC1 pin not used 1: P2_6 assigned	R/W
b5	—	Reserved bit	Set to 0.	R/W
b6	TRDIOD1SEL0	TRDIOD1 pin select bit	0: TRDIOD1 pin not used 1: P2_7 assigned	R/W
b7	—	Reserved bit	Set to 0.	R/W

The TRDPSR1 register selects which pin is assigned to the timer RD I/O. To use the I/O pin for timer RD, set this register.
Set the TRDPSR1 register before setting the timer RD associated registers. Also, do not change the setting value in this register during timer RD operation.

20.5.18 Operating Example



i = 0 or 1

m: Value set in TRDGRAi register
n: Value set in TRDGRBi register
p: Value set in TRDGRCi register
q: Value set in TRDGRDi register

The above applies under the following conditions:
Bits BFCi and BFDi in the TRDMR register are set to 0 (registers TRDGRCi and TRDGRDi are not used as buffer registers).
Bits EBi, ECi and EDi in the TRDOER1 register are set to 0 (enable TRDIOBi, TRDIOCi and TRDIODi pin outputs).
Bits TOBi and TOCi in the TRDOCR register are set to 0 (inactive level), the TODi bit is set to 1 (active level).
The POLB bit in the TRDPOCRi register is set to 1 (active level “H”), bits POLC and POLD are set to 0 (active level “L”).

Figure 20.15 Operating Example of PWM Mode

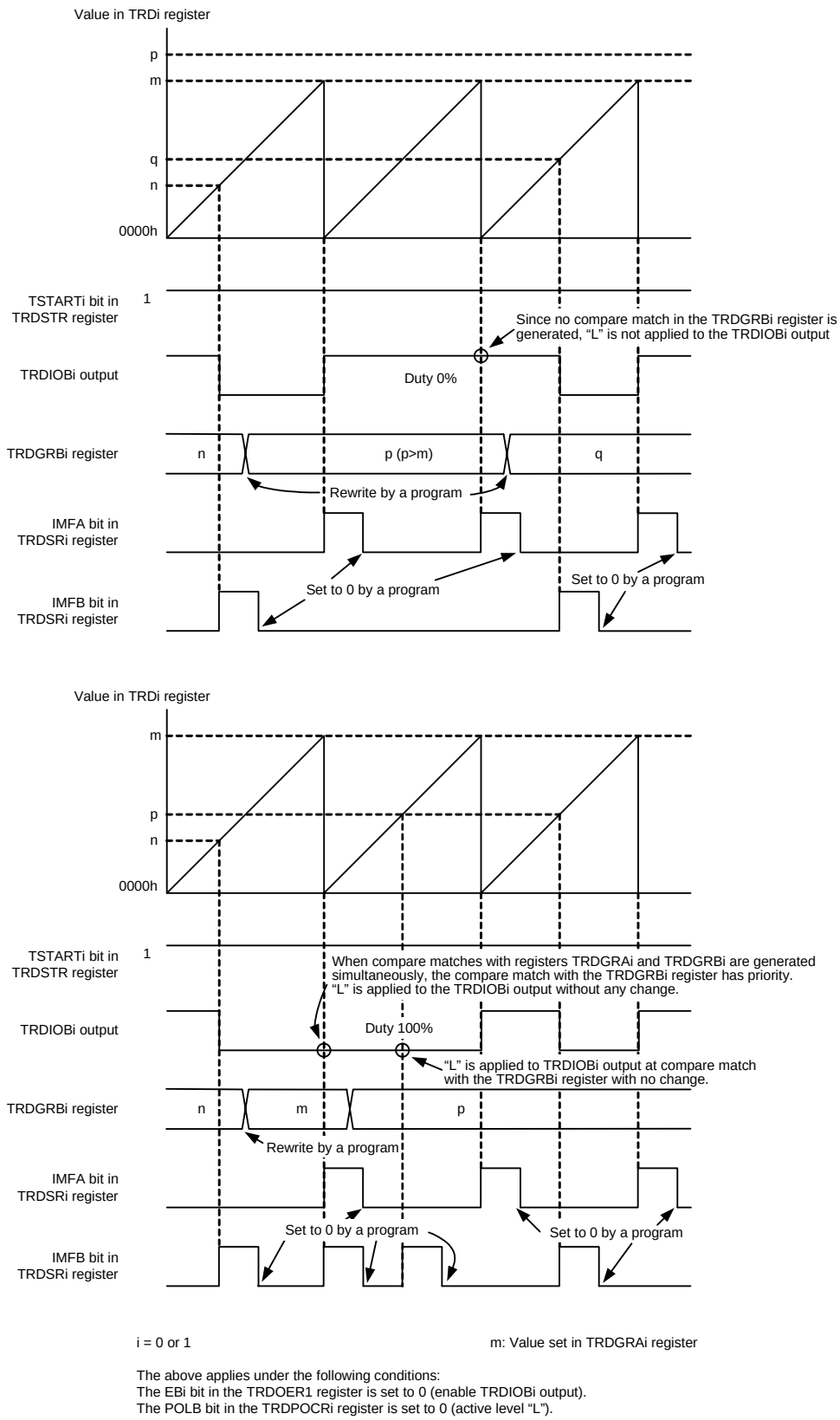


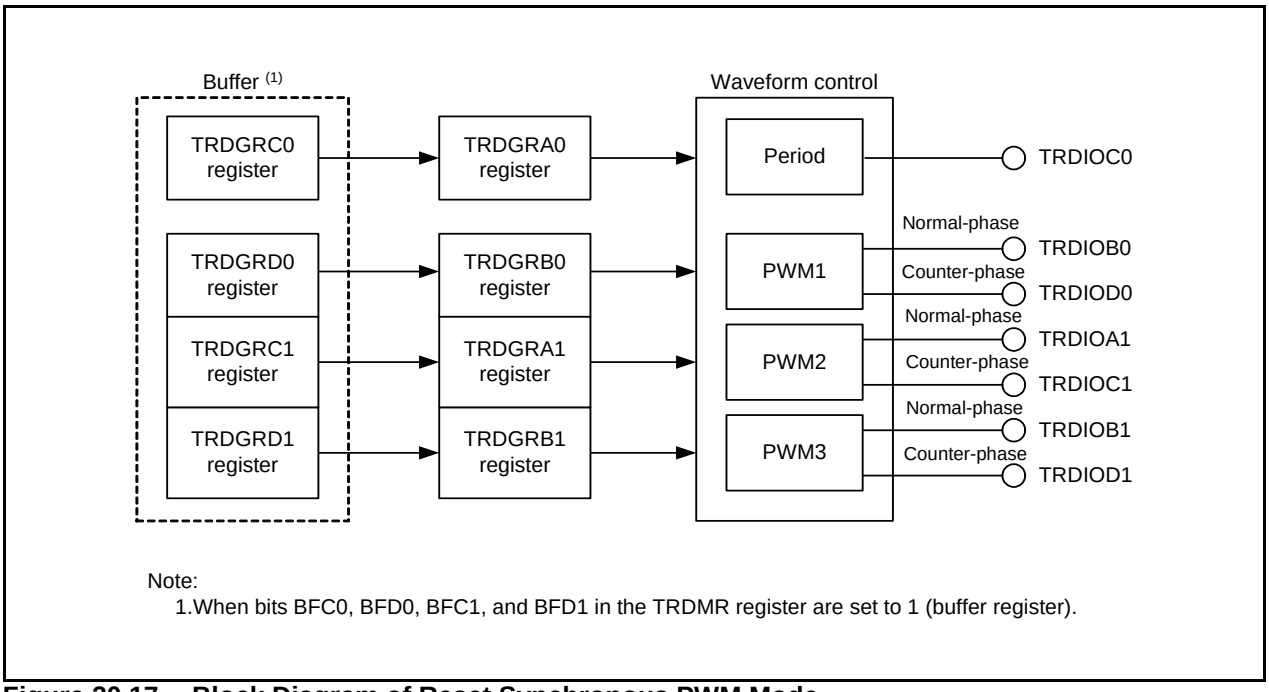
Figure 20.16 Operating Example of PWM Mode (Duty 0%, Duty 100%)

20.5.19 A/D Trigger Generation

A compare match signal with registers TRDi (i = 0 or 1) and TRDGRji (j = A, B, C, or D) can be used as the conversion start trigger of the A/D converter.
The TRDADCR register is used to select which compare match is used.

20.6 Reset Synchronous PWM Mode

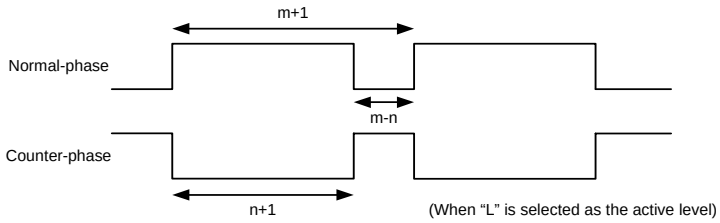
In this mode, 3 normal-phases and 3 counter-phases of the PWM waveform are output with the same period (three-phase, sawtooth wave modulation, and no dead time).
Figure 20.17 shows a Block Diagram of Reset Synchronous PWM Mode, and Table 20.11 lists the Reset Synchronous PWM Mode Specifications. Figure 20.18 shows an Operating Example of Reset Synchronous PWM Mode.
Refer to **Figure 20.16 Operating Example of PWM Mode (Duty 0%, Duty 100%)** for an operating example of PWM Mode with duty 0% and duty 100%.



Note:
1.When bits BFC0, BFD0, BFC1, and BFD1 in the TRDMR register are set to 1 (buffer register).

Figure 20.17 Block Diagram of Reset Synchronous PWM Mode

Table 20.11 Reset Synchronous PWM Mode Specifications

Item	Specification
Count sources	f1, f2, f4, f8, f32, fC2, fOCO40M, fOCO-F External signal input to the TRDCLK pin (valid edge selected by a program)
Count operations	The TRD0 register is incremented (the TRD1 register is not used).
PWM waveform	PWM period : 1/fk × (m+1) Active level width of normal-phase : 1/fk × (m-n) Active level width of counter-phase: 1/fk × (n+1) fk: Frequency of count source m: Value set in the TRDGRA0 register n: Value set in the TRDGRB0 register (PWM1 output), Value set in the TRDGRA1 register (PWM2 output), Value set in the TRDGRB1 register (PWM3 output) 
Count start condition	1 (count starts) is written to the TSTART0 bit in the TRDSTR register.
Count stop conditions	• 0 (count stops) is written to the TSTART0 bit when the CSEL0 bit in the TRDSTR register is set to 1. (The PWM output pin outputs the initial output level selected by bits OLS0 and OLS1 in the TRDFCR register.) • When the CSEL0 bit in the TRDSTR register is set to 0, the count stops at the compare match in the TRDGRA0 register. (The PWM output pin outputs the initial output level selected by bits OLS0 and OLS1 in the TRDFCR register.)
Interrupt request generation timing	• Compare match (the content of the TRD0 register matches content of registers TRDGRj0, TRDGRA1, and TRDGRB1). • The TRD0 register overflows
TRDIOA0 pin function	Programmable I/O port or TRDCLK (external clock) input
TRDIOB0 pin function	PWM1 output normal-phase output
TRDIOD0 pin function	PWM1 output counter-phase output
TRDIOA1 pin function	PWM2 output normal-phase output
TRDIOC1 pin function	PWM2 output counter-phase output
TRDIOB1 pin function	PWM3 output normal-phase output
TRDIOD1 pin function	PWM3 output counter-phase output
TRDIOC0 pin function	Output inverted every PWM period
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRD0 register.
Write to timer	The value can be written to the TRD0 register.
Selectable functions	• The normal-phase and counter-phase active level and initial output level are selected individually. • Buffer operation (Refer to **20.2.2 Buffer Operation**.) • Pulse output forced cutoff signal input (Refer to **20.2.4 Pulse Output Forced Cutoff**.) • A/D trigger generation

j = either A, B, C, or D

20.6.1 Module Standby Control Register (MSTCR)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	MSTTRG	MSTTRC	MSTTRD	MSTIIC	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	MSTIIC	SSU standby bit	0: Active 1: Standby (1)	R/W
b4	MSTTRD	Timer RD standby bit	0: Active 1: Standby (2, 3)	R/W
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (4)	R/W
b6	MSTTRG	Timer RG standby bit	0: Active 1: Standby (5)	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. When the MSTIIC bit is set to 1 (standby), any access to the SSU associated registers (addresses 0193h to 019Dh) is disabled.
2. When the MSTTRD bit is set to 1 (standby), any access to the timer RD associated registers (addresses 0136h to 015Fh) is disabled.
3. To set the MSTTRD bit to 1 (standby), set bits TCK2 to TCK0 in the TRDCRi (i = 0 or 1) register to 000b (f1).
4. When the MSTTRC bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0120h to 0133h) is disabled.
5. When the MSTTRG bit is set to 1 (standby), any access to the timer RG associated registers (addresses 0170h to 017Fh) is disabled.

20.6.2 Timer RD Trigger Control Register (TRDADCR)

Address 0136h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADTRGD1E	ADTRGC1E	ADTRGB1E	ADTRGA1E	ADTRGD0E	ADTRGC0E	ADTRGB0E	ADTRGA0E
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADTRGA0E	A/D trigger A0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRA0	R/W
b1	ADTRGB0E	A/D trigger B0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRB0	R/W
b2	ADTRGC0E	A/D trigger C0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRC0	R/W
b3	ADTRGD0E	A/D trigger D0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRD0	R/W
b4	ADTRGA1E	A/D trigger A1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRA1	R/W
b5	ADTRGB1E	A/D trigger B1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRB1	R/W
b6	ADTRGC1E	A/D trigger C1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRC1	R/W
b7	ADTRGD1E	A/D trigger D1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRD1	R/W

20.6.3 Timer RD Start Register (TRDSTR) in Reset Synchronous PWM Mode

Address 0137h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	CSEL1	CSEL0	TSTART1	TSTART0
After Reset	1	1	1	1	1	1	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART0	TRD0 count start flag (3)	0: Count stops (1) 1: Count starts	R/W
b1	TSTART1	TRD1 count start flag (4)	0: Count stops (2) 1: Count starts	R/W
b2	CSEL0	TRD0 count operation select bit	0: Count stops at the compare match with the TRDGRA0 register 1: Count continues after the compare match with the TRDGRA0 register	R/W
b3	CSEL1	TRD1 count operation select bit	0: Count stops at the compare match with the TRDGRA1 register 1: Count continues after the compare match with the TRDGRA1 register	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	—			

Notes:
1. When the CSEL0 bit is set to 1, write 0 to the TSTART0 bit.
2. When the CSEL1 bit is set to 1, write 0 to the TSTART1 bit.
3. When the CSEL0 bit is set to 0 and the compare match signal (TRDIOA0) is generated, this bit is set to 0 (count stops).
4. When the CSEL1 bit is set to 0 and the compare match signal (TRDIOA1) is generated, this bit is set to 0 (count stops).

Set the TRDSTR register using the MOV instruction (do not use the bit handling instruction). Refer to **20.10.1 TRDSTR Register** of **Notes on Timer RD**.

20.6.4 Timer RD Mode Register (TRDMR) in Reset Synchronous PWM Mode

Address 0138h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BFD1	BFC1	BFD0	BFC0	—	—	—	SYNC
After Reset	0	0	0	0	1	1	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	SYNC	Timer RD synchronous bit	Set this bit to 0 (registers TRD and TRD1 operate independently) in reset synchronous PWM mode.	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b2	—			
b3	—			
b4	BFC0	TRDGRC0 register function select bit	0: General register 1: Buffer register of TRDGRA0 register	R/W
b5	BFD0	TRDGRD0 register function select bit	0: General register 1: Buffer register of TRDGRB0 register	R/W
b6	BFC1	TRDGRC1 register function select bit	0: General register 1: Buffer register of TRDGRA1 register	R/W
b7	BFD1	TRDGRD1 register function select bit	0: General register 1: Buffer register of TRDGRB1 register	R/W

20.6.5 Timer RD Function Control Register (TRDFCR) in Reset Synchronous PWM Mode

Address 013Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PWM3	STCLK	ADEG	ADTRG	OLS1	OLS0	CMD1	CMD0
After Reset	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CMD0	Combination mode select bit (1)	Set to 01b (reset synchronous PWM mode) in reset synchronous PWM mode.	R/W
b1	CMD1			R/W
b2	OLS0	Normal-phase output level select bit (in reset synchronous PWM mode or complementary PWM mode)	0: Initial output “H”, Active level “L” 1: Initial output “L”, Active level “H”	R/W
b3	OLS1	Counter-phase output level select bit (in reset synchronous PWM mode or complementary PWM mode)		R/W
b4	ADTRG	A/D trigger enable bit (in complementary PWM mode)	This bit is disabled in reset synchronous PWM mode.	R/W
b5	ADEG	A/D trigger edge select bit (in complementary PWM mode)		R/W
b6	STCLK	External clock input select bit	0: External clock input disabled 1: External clock input enabled	R/W
b7	PWM3	PWM3 mode select bit (2)	This bit is disabled in reset synchronous PWM mode.	R/W

Notes:
1. Set bits CMD1 to CMD0 when both the TSTART0 and TSTART1 bits are set to 0 (count stops).
2. When bits CMD1 to CMD0 are set to 00b (timer mode, PWM mode, or PWM3 mode), the setting of the PWM3 bit is enabled.

20.6.6 Timer RD Output Master Enable Register 1 (TRDOER1) in Reset Synchronous PWM Mode

Address 013Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ED1	EC1	EB1	EA1	ED0	EC0	EB0	EA0
After Reset	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	EA0	TRDIOA0 output disable bit	Set this bit to 1 (the TRDIOA0 pin is used as a programmable I/O port) in reset synchronous PWM mode.	R/W
b1	EB0	TRDIOB0 output disable bit	0: Enable output 1: Disable output (The TRDIOB0 pin is used as a programmable I/O port.)	R/W
b2	EC0	TRDIOC0 output disable bit	0: Enable output 1: Disable output (The TRDIOC0 pin is used as a programmable I/O port.)	R/W
b3	ED0	TRDIOD0 output disable bit	0: Enable output 1: Disable output (The TRDIOD0 pin is used as a programmable I/O port.)	R/W
b4	EA1	TRDIOA1 output disable bit	0: Enable output 1: Disable output (The TRDIOA1 pin is used as a programmable I/O port.)	R/W
b5	EB1	TRDIOB1 output disable bit	0: Enable output 1: Disable output (The TRDIOB1 pin is used as a programmable I/O port.)	R/W
b6	EC1	TRDIOC1 output disable bit	0: Enable output 1: Disable output (The TRDIOC1 pin is used as a programmable I/O port.)	R/W
b7	ED1	TRDIOD1 output disable bit	0: Enable output 1: Disable output (The TRDIOD1 pin is used as a programmable I/O port.)	R/W

20.6.7 Timer RD Output Master Enable Register 2 (TRDOER2) in Reset Synchronous PWM Mode

Address 013Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PTO	—	—	—	—	—	—	—
After Reset	0	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	PTO	$\overline{\text{INT0}}$ of pulse output forced cutoff signal input enabled bit (1)	0: Pulse output forced cutoff input disabled 1: Pulse output forced cutoff input enabled (All bits in the TRDOER1 register are set to 1 (disable output) when “L” is applied to the $\overline{\text{INT0}}$ pin.)	R/W

Note:
1. Refer to **20.2.4 Pulse Output Forced Cutoff**.

20.6.8 Timer RD Control Register 0 (TRDCR0) in Reset Synchronous PWM Mode

Address 0140h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TCK2	TCK1	TCK0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TCK0	Count source select bit	b2 b1 b0 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRDCLK input (1) 1 1 0: fOCO40M 1 1 1: fOCO-F (3)	R/W
b1	TCK1			R/W
b2	TCK2			R/W
b3	CKEG0	External clock edge select bit (2)	b4 b3 0 0: Count at the rising edge 0 1: Count at the falling edge 1 0: Count at both edges 1 1: Do not set.	R/W
b4	CKEG1			R/W
b5	CCLR0	TRD0 counter clear select bit	Set to 001b (TRD0 register cleared at compare match with TRDGRA0 register) in reset synchronous PWM mode.	R/W
b6	CCLR1			R/W
b7	CCLR2			R/W

Notes:
1. Enabled when the STCLK bit in the TRDFCR register is 1 (external clock input enabled).
2. Enabled when bits TCK2 to TCK0 are set to 101b (TRDCLK input) and the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).
3. To select fOCO-F, set it to the clock frequency higher than the CPU clock frequency.

The TRDCR1 register is not used in reset synchronous PWM mode.

20.6.9 Timer RD Status Register i (TRDSRi) (i = 0 or 1) in Reset Synchronous PWM Mode

Address 0143h (TRDSR0), 0153h (TRDSR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	UDF	OVF	IMFD	IMFC	IMFB	IMFA	
After Reset	1	1	1	0	0	0	0	0	TRDSR0 register
After Reset	1	1	0	0	0	0	0	0	TRDSR1 register

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input capture / compare match flag A	[Source for setting this bit to 0] Write 0 after read (2). [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRAi register.	R/W
b1	IMFB	Input capture / compare match flag B	[Source for setting this bit to 0] Write 0 after read (2). [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRBi register.	R/W
b2	IMFC	Input capture / compare match flag C	[Source for setting this bit to 0] Write 0 after read (2). [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRCi register (3).	R/W
b3	IMFD	Input capture / compare match flag D	[Source for setting this bit to 0] Write 0 after read (2). [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRDi register (3).	R/W
b4	OVF	Overflow flag	[Source for setting this bit to 0] Write 0 after read (2). [Source for setting this bit to 1] When the TRDi register overflows.	R/W
b5	UDF	Underflow flag (1)	This bit is disabled in reset synchronous PWM mode.	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b7	—			

Notes:
1. Nothing is assigned to b5 in the TRDSR0 register. When writing to b5, write 0. When reading, the content is 1.
2. The writing results are as follows:
   - This bit is set to 0 when the read result is 1 and 0 is written to the same bit.
   - This bit remains unchanged even if the read result is 0 and 0 is written to the same bit. (This bit remains 1 even if it is set to 1 from 0 after reading, and writing 0.)
   - This bit remains unchanged if 1 is written to it.
3. Including when the BFji bit in the TRDMR register is set to 1 (TRDGRji is used as the buffer register).

20.6.10 Timer RD Interrupt Enable Register i (TRDIERi) (i = 0 or 1) in Reset Synchronous PWM Mode

Address 0144h (TRDIER0), 0154h (TRDIER1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	OVIE	IMIED	IMIEC	IMIEB	IMIEA
After Reset	1	1	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input capture/compare match interrupt enable bit A	0: Disable interrupt (IMIA) by the IMFA bit 1: Enable interrupt (IMIA) by the IMFA bit	R/W
b1	IMIEB	Input capture/compare match interrupt enable bit B	0: Disable interrupt (IMIB) by the IMFB bit 1: Enable interrupt (IMIB) by the IMFB bit	R/W
b2	IMIEC	Input capture/compare match interrupt enable bit C	0: Disable interrupt (IMIC) by the IMFC bit 1: Enable interrupt (IMIC) by the IMFC bit	R/W
b3	IMIED	Input capture/compare match interrupt enable bit D	0: Disable interrupt (IMID) by the IMFD bit 1: Enable interrupt (IMID) by the IMFD bit	R/W
b4	OVIE	Overflow/underflow interrupt enable bit	0: Disable interrupt (OVI) by the OVF bit 1: Enable interrupt (OVI) by the OVF bit	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b6	—			
b7	—			

20.6.11 Timer RD Counter 0 (TRD0) in Reset Synchronous PWM Mode

Address 0147h to 0146h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15 to b0	Count the count source. Count operation is incremented. When an overflow occurs, the OVF bit in the TRDSR0 register is set to 1.	0000h to FFFFh	R/W

Access the TRD0 register in 16-bit units. Do not access it in 8-bit units.
The TRD1 register is not used in reset synchronous PWM mode.

20.6.12 Timer RD General Registers Ai, Bi, Ci, and Di (TRDGRAi, TRDGRBi, TRDGRCi, TRDGRDi) (i = 0 or 1) in Reset Synchronous PWM Mode

Address 0149h to 0148h (TRDGRA0), 014Bh to 014Ah (TRDGRB0),
014Dh to 014Ch (TRDGRC0), 014Fh to 014Eh (TRDGRD0),
0159h to 0158h (TRDGRA1), 015Bh to 015Ah (TRDGRB1),
015Dh to 015Ch (TRDGRC1), 015Fh to 015Eh (TRDGRD1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b15 to b0	Refer to **Table 20.12 TRDGRji Register Functions in Reset Synchronous PWM Mode**	R/W

Access registers TRDGRAi to TRDGRDi in 16-bit units. Do not access them in 8-bit units.

The following registers are disabled in the reset synchronous PWM mode: TRDPMR, TRDOCR, TRDDF0, TRDDF1, TRDIORA0, TRDIORC0, TRDPOCR0, TRDIORA1, TRDIORC1, and TRDPOCR1.

Table 20.12 TRDGRji Register Functions in Reset Synchronous PWM Mode

Register	Setting	Register Function	PWM Output Pin
TRDGRA0	–	General register. Set the PWM period.	(Output inverted every PWM period and TRDIOC0 pin)
TRDGRB0	–	General register. Set the changing point of PWM1 output.	TRDIOB0 TRDIOD0
TRDGRC0	BFC0 = 0	(These registers are not used in reset synchronous PWM mode.)	–
TRDGRD0	BFD0 = 0		
TRDGRA1	–	General register. Set the changing point of PWM2 output.	TRDIOA1 TRDIOC1
TRDGRB1	–	General register. Set the changing point of PWM3 output.	TRDIOB1 TRDIOD1
TRDGRC1	BFC1 = 0	(These points are not used in reset synchronous PWM mode.)	–
TRDGRD1	BFD1 = 0		
TRDGRC0	BFC0 = 1	Buffer register. Set the next PWM period. (Refer to **20.2.2 Buffer Operation.**)	(Output inverted every PWM period and TRDIOC0 pin)
TRDGRD0	BFD0 = 1	Buffer register. Set the changing point of the next PWM1 output. (Refer to **20.2.2 Buffer Operation**.)	TRDIOB0 TRDIOD0
TRDGRC1	BFC1 = 1	Buffer register. Set the changing point of the next PWM2 output. (Refer to **20.2.2 Buffer Operation**.)	TRDIOA1 TRDIOC1
TRDGRD1	BFD1 = 1	Buffer register. Set the changing point of the next PWM3 output. (Refer to **20.2.2 Buffer Operation**.)	TRDIOB1 TRDIOD1

BFC0, BFD0, BFC1, BFD1: Bits in TRDMR register

20.6.13 Timer RD Pin Select Register 0 (TRDPSR0)

Address 0184h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	TRDIOD0SEL0	—	TRDIOC0SEL0	—	TRDIOB0SEL0	—	TRDIOA0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRDIOA0SEL0	TRDIOA0/TRDCLK pin select bit	0: TRDIOA0/TRDCLK pin not used 1: P2_0 assigned	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	TRDIOB0SEL0	TRDIOB0 pin select bit	0: TRDIOB0 pin not used 1: P2_1 assigned	R/W
b3	—	Reserved bit	Set to 0.	R/W
b4	TRDIOC0SEL0	TRDIOC0 pin select bit	0: TRDIOC0 pin not used 1: P2_2 assigned	R/W
b5	—	Reserved bit	Set to 0.	R/W
b6	TRDIOD0SEL0	TRDIOD0 pin select bit	0: TRDIOD0 pin not used 1: P2_3 assigned	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

The TRDPSR0 register selects which pin is assigned to the timer RD I/O. To use the I/O pin for timer RD, set this register.
Set the TRDPSR0 register before setting the timer RD associated registers. Also, do not change the setting value in this register during timer RD operation.

20.6.14 Timer RD Pin Select Register 1 (TRDPSR1)

Address 0185h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	TRDIOD1SEL0	—	TRDIOC1SEL0	—	TRDIOB1SEL0	—	TRDIOA1SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRDIOA1SEL0	TRDIOA1 pin select bit	0: TRDIOA1 pin not used 1: P2_4 assigned	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	TRDIOB1SEL0	TRDIOB1 pin select bit	0: TRDIOB1 pin not used 1: P2_5 assigned	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TRDIOC1SEL0	TRDIOC1 pin select bit	0: TRDIOC1 pin not used 1: P2_6 assigned	R/W
b5	—	Reserved bit	Set to 0.	R/W
b6	TRDIOD1SEL0	TRDIOD1 pin select bit	0: TRDIOD1 pin not used 1: P2_7 assigned	R/W
b7	—	Reserved bit	Set to 0.	R/W

The TRDPSR1 register selects which pin is assigned to the timer RD I/O. To use the I/O pin for timer RD, set this register.
Set the TRDPSR1 register before setting the timer RD associated registers. Also, do not change the setting value in this register during timer RD operation.

20.6.15 Operating Example

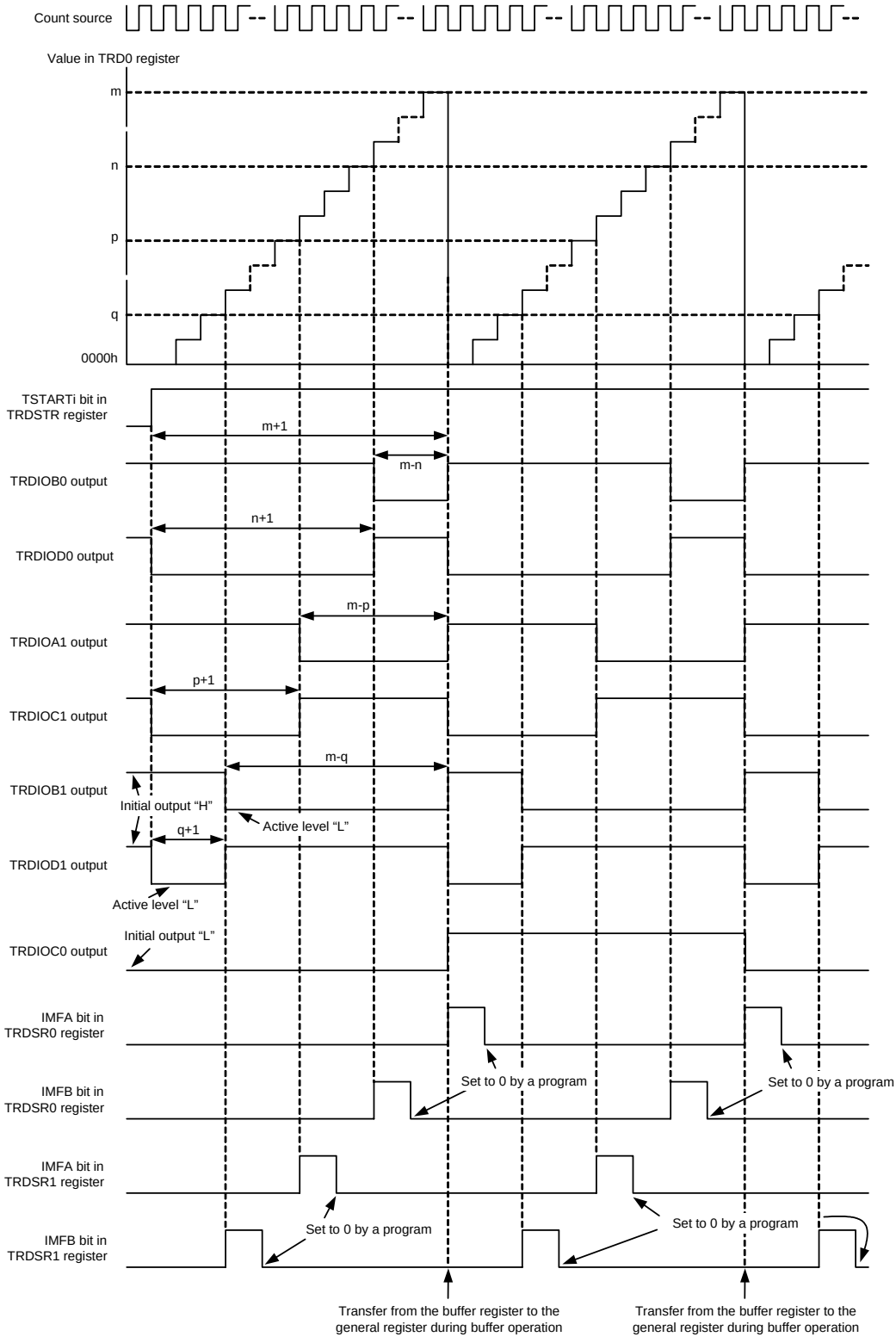


Figure 20.18 Operating Example of Reset Synchronous PWM Mode

20.6.16 A/D Trigger Generation

A compare match signal with registers TRDi (i = 0 or 1) and TRDGRji (j = A, B, C, or D) can be used as the conversion start trigger of the A/D converter.
The TRDADCR register is used to select which compare match is used.

20.7 Complementary PWM Mode

In this mode, 3 normal-phases and 3 counter-phases of the PWM waveform are output with the same period (three-phase, triangular wave modulation, and with dead time).
Figure 20.19 shows a Block Diagram of Complementary PWM Mode, and Table 20.13 lists the Complementary PWM Mode Specifications. Figure 20.20 shows Output Model of Complementary PWM Mode, and Figure 20.21 shows Operating Example of Complementary PWM Mode.

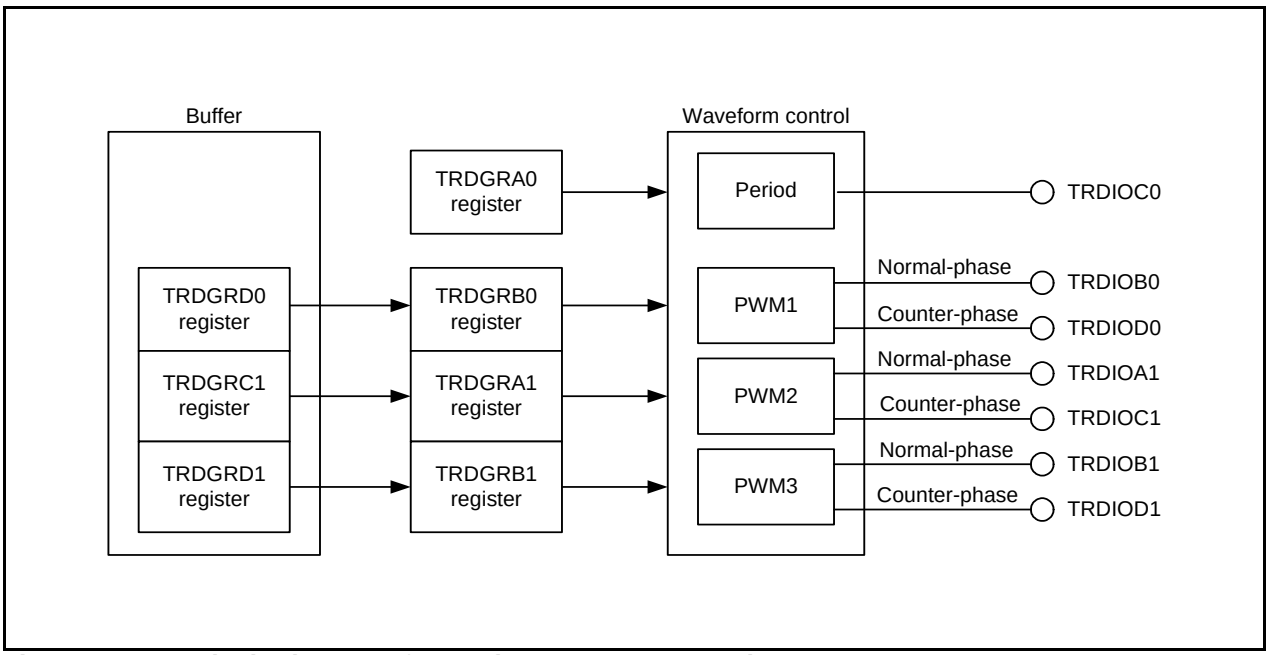
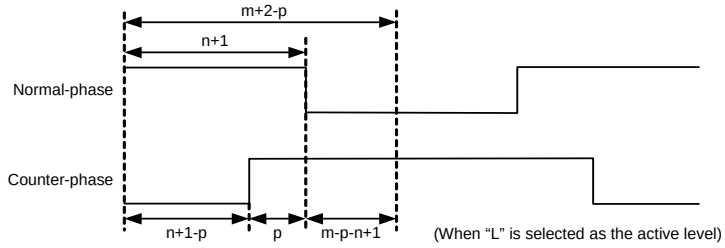


Figure 20.19 Block Diagram of Complementary PWM Mode

Table 20.13 Complementary PWM Mode Specifications

Item	Specification
Count sources	f1, f2, f4, f8, f32, fOCO40M, fOCO-F External signal input to the TRDCLK pin (valid edge selected by a program) Set bits TCK2 to TCK0 in the TRDCR1 register to the same value (same count source) as bits TCK2 to TCK0 in the TRDCR0 register.
Count operations	Increment or decrement Registers TRD0 and TRD1 are decremented with the compare match in registers TRD0 and TRDGRA0 during increment operation. The TRD1 register value is changed from 0000h to FFFFh during decrement operation, and registers TRD0 and TRD1 are incremented.
PWM operations	PWM period: 1/fk × (m+2-p) × 2 (1) Dead time: p Active level width of normal-phase: 1/fk × (m-n-p+1) × 2 Active level width of counter-phase: 1/fk × (n+1-p) × 2 fk: Frequency of count source m: Value set in the TRDGRA0 register n: Value set in the TRDGRB0 register (PWM1 output) Value set in the TRDGRA1 register (PWM2 output) Value set in the TRDGRB1 register (PWM3 output) p: Value set in the TRD0 register 
Count start condition	1 (count starts) is written to bits TSTART0 and TSTART1 in the TRDSTR register.
Count stop conditions	0 (count stops) is written to bits TSTART0 and TSTART1 when the CSEL0 bit in the TRDSTR register is set to 1. (The PWM output pin outputs the initial output level selected by bits OLS0 and OLS1 in the TRDFCR register.)
Interrupt request generation timing	• Compare match (The content of the TRDi register matches content of the TRDGRji register.) • The TRD1 register underflows
TRDIOA0 pin function	Programmable I/O port or TRDCLK (external clock) input
TRDIOB0 pin function	PWM1 output normal-phase output
TRDIOD0 pin function	PWM1 output counter-phase output
TRDIOA1 pin function	PWM2 output normal-phase output
TRDIOC1 pin function	PWM2 output counter-phase output
TRDIOB1 pin function	PWM3 output normal-phase output
TRDIOD1 pin function	PWM3 output counter-phase output
TRDIOC0 pin function	Output inverted every 1/2 period of PWM
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRDi register.
Write to timer	The value can be written to the TRDi register.
Selectable functions	• Pulse output forced cutoff signal input (Refer to **20.2.4 Pulse Output Forced Cutoff.**) • The normal-phase and counter-phase active level and initial output level are selected individually. • Transfer timing from the buffer register selection • A/D trigger generation

i = 0 or 1, j = either A, B, C, or D

Note:

1. After a count starts, the PWM period is fixed.

20.7.1 Module Standby Control Register (MSTCR)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	MSTTRG	MSTTRC	MSTTRD	MSTIIC	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	MSTIIC	SSU standby bit	0: Active 1: Standby (1)	R/W
b4	MSTTRD	Timer RD standby bit	0: Active 1: Standby (2, 3)	R/W
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (4)	R/W
b6	MSTTRG	Timer RG standby bit	0: Active 1: Standby (5)	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. When the MSTIIC bit is set to 1 (standby), any access to the SSU associated registers (addresses 0193h to 019Dh) is disabled.
2. When the MSTTRD bit is set to 1 (standby), any access to the timer RD associated registers (addresses 0136h to 015Fh) is disabled.
3. To set the MSTTRD bit to 1 (standby), set bits TCK2 to TCK0 in the TRDCRi (i = 0 or 1) register to 000b (f1).
4. When the MSTTRC bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0120h to 0133h) is disabled.
5. When the MSTTRG bit is set to 1 (standby), any access to the timer RG associated registers (addresses 0170h to 017Fh) is disabled.

20.7.2 Timer RD Trigger Control Register (TRDADCR) in Complementary PWM Mode

Address 0136h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADTRGD1E	ADTRGC1E	ADTRGB1E	ADTRGA1E	ADTRGD0E	ADTRGC0E	ADTRGB0E	ADTRGA0E
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADTRGA0E	A/D trigger A0 enable bit	Set to 0.	R/W
b1	ADTRGB0E	A/D trigger B0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRB0	R/W
b2	ADTRGC0E	A/D trigger C0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRC0	R/W
b3	ADTRGD0E	A/D trigger D0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRD0	R/W
b4	ADTRGA1E	A/D trigger A1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRA1	R/W
b5	ADTRGB1E	A/D trigger B1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRB1	R/W
b6	ADTRGC1E	A/D trigger C1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRC1	R/W
b7	ADTRGD1E	A/D trigger D1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRD1	R/W

20.7.3 Timer RD Start Register (TRDSTR) in Complementary PWM Mode

Address 0137h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	CSEL1	CSEL0	TSTART1	TSTART0
After Reset	1	1	1	1	1	1	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART0	TRD0 count start flag (3)	0: Count stops (1) 1: Count starts	R/W
b1	TSTART1	TRD1 count start flag (4)	0: Count stops (2) 1: Count starts	R/W
b2	CSEL0	TRD0 count operation select bit	0: Count stops at the compare match with the TRDGRA0 register 1: Count continues after the compare match with the TRDGRA0 register	R/W
b3	CSEL1	TRD1 count operation select bit	0: Count stops at the compare match with the TRDGRA1 register 1: Count continues after the compare match with the TRDGRA1 register	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	—			

Notes:
1. When the CSEL0 bit is set to 1, write 0 to the TSTART0 bit.
2. When the CSEL1 bit is set to 1, write 0 to the TSTART1 bit.
3. When the CSEL0 bit is set to 0 and the compare match signal (TRDIOA0) is generated, this bit is set to 0 (count stops).
4. When the CSEL1 bit is set to 0 and the compare match signal (TRDIOA1) is generated, this bit is set to 0 (count stops).

Set the TRDSTR register using the MOV instruction (do not use the bit handling instruction). Refer to **20.10.1 TRDSTR Register** of **Notes on Timer RD**.

20.7.4 Timer RD Mode Register (TRDMR) in Complementary PWM Mode

Address 0138h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BFD1	BFC1	BFD0	BFC0	—	—	—	SYNC
After Reset	0	0	0	0	1	1	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	SYNC	Timer RD synchronous bit	Set this bit to 0 (registers TRD0 and TRD1 operate independently) in complementary PWM mode.	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b2	—			
b3	—			
b4	BFC0	TRDGRC0 register function select bit	Set this bit to 0 (general register) in complementary PWM mode.	R/W
b5	BFD0	TRDGRD0 register function select bit	0: General register 1: Buffer register of TRDGRB0 register	R/W
b6	BFC1	TRDGRC1 register function select bit	0: General register 1: Buffer register of TRDGRA1 register	R/W
b7	BFD1	TRDGRD1 register function select bit	0: General register 1: Buffer register of TRDGRB1 register	R/W

20.7.5 Timer RD Function Control Register (TRDFCR) in Complementary PWM Mode

Address 013Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PWM3	STCLK	ADEG	ADTRG	OLS1	OLS0	CMD1	CMD0
After Reset	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CMD0	Combination mode select bit (1, 2)	b1 b0 1 0: Complementary PWM mode (transfer from the buffer register to the general register at the underflow in the TRD1 register) 1 1: Complementary PWM mode (transfer from the buffer register to the general register at the compare match with registers TRD0 and TRDGRA0.) Other than above: Do not set.	R/W
b1	CMD1			R/W
b2	OLS0	Normal-phase output level select bit (in reset synchronous PWM mode or complementary PWM mode)	0: Initial output “H”, Active level “L” 1: Initial output “L”, Active level “H”	R/W
b3	OLS1	Counter-phase output level select bit (in reset synchronous PWM mode or complementary PWM mode)	0: Initial output “H”, Active level “L” 1: Initial output “L”, Active level “H”	R/W
b4	ADTRG	A/D trigger enable bit (in complementary PWM mode)	0: Disable A/D trigger 1: Enable A/D trigger (3)	R/W
b5	ADEG	A/D trigger edge select bit (in complementary PWM mode)	0: A/D trigger is generated at compare match between registers TRD0 and TRDGRA0 1: A/D trigger is generated at underflow in the TRD1 register	R/W
b6	STCLK	External clock input select bit	0: External clock input disabled 1: External clock input enabled	R/W
b7	PWM3	PWM3 mode select bit (4)	This bit is disabled in complementary PWM mode.	R/W

Notes:
1. When setting bits CMD1 to CMD0 to 10b or 11b, the MCU enters complementary PWM mode in spite of the setting of the TRDPMR register.
2. Set bits CMD1 to CMD0 when both the TSTART0 and TSTART1 bits in the TRDSTR register are set to 0 (count stops).
3. Set bits ADCAP1 to ADCAP0 in the ADMOD register to 01b (A/D conversion starts by conversion trigger from timer RD).
4. When bits CMD1 to CMD0 are set to 00b (timer mode, PWM mode, or PWM3 mode), the setting of the PWM3 bit is enabled.

20.7.6 Timer RD Output Master Enable Register 1 (TRDOER1) in Complementary PWM Mode

Address 013Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ED1	EC1	EB1	EA1	ED0	EC0	EB0	EA0
After Reset	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	EA0	TRDIOA0 output disable bit	Set this bit to 1 (the TRDIOA0 pin is used as a programmable I/O port) in complementary PWM mode.	R/W
b1	EB0	TRDIOB0 output disable bit	0: Enable output 1: Disable output (The TRDIOB0 pin is used as a programmable I/O port.)	R/W
b2	EC0	TRDIOC0 output disable bit	0: Enable output 1: Disable output (The TRDIOC0 pin is used as a programmable I/O port.)	R/W
b3	ED0	TRDIOD0 output disable bit	0: Enable output 1: Disable output (The TRDIOD0 pin is used as a programmable I/O port.)	R/W
b4	EA1	TRDIOA1 output disable bit	0: Enable output 1: Disable output (The TRDIOA1 pin is used as a programmable I/O port.)	R/W
b5	EB1	TRDIOB1 output disable bit	0: Enable output 1: Disable output (The TRDIOB1 pin is used as a programmable I/O port.)	R/W
b6	EC1	TRDIOC1 output disable bit	0: Enable output 1: Disable output (The TRDIOC1 pin is used as a programmable I/O port.)	R/W
b7	ED1	TRDIOD1 output disable bit	0: Enable output 1: Disable output (The TRDIOD1 pin is used as a programmable I/O port.)	R/W

20.7.7 Timer RD Output Master Enable Register 2 (TRDOER2) in Complementary PWM Mode

Address 013Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PTO	—	—	—	—	—	—	—
After Reset	0	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	PTO	$\overline{\text{INT0}}$ of pulse output forced cutoff signal input enabled bit (1)	0: Pulse output forced cutoff input disabled 1: Pulse output forced cutoff input enabled (All bits in the TRDOER1 register are set to 1 (disable output) when “L” is applied to the $\overline{\text{INT0}}$ pin.)	R/W

Note:
1. Refer to **20.2.4 Pulse Output Forced Cutoff**.

20.7.8 Timer RD Control Register i (TRDCRi) (i = 0 or 1) in Complementary PWM Mode

Address 0140h (TRDCR0), 0150h (TRDCR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TCK2	TCK1	TCK0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TCK0	Count source select bit (2)	b2 b1 b0 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRDCLK input (1) 1 1 0: fOCO40M 1 1 1: fOCO-F (4)	R/W
b1	TCK1			R/W
b2	TCK2			R/W
b3	CKEG0	External clock edge select bit (2, 3)	b4 b3 0 0: Count at the rising edge 0 1: Count at the falling edge 1 0: Count at both edges 1 1: Do not set.	R/W
b4	CKEG1			R/W
b5	CCLR0	TRDi counter clear select bit	Set to 000b (disable clearing (free-running operation)) in complementary PWM mode.	R/W
b6	CCLR1			R/W
b7	CCLR2			R/W

Notes:
1. Enabled when the STCLK bit in the TRDFCR register is 1 (external clock input enabled).
2. Set bits TCK2 to TCK0 and bits CKEG1 to CKEG0 in registers TRDCR0 and TRDCR1 to the same values.
3. Enabled when bits TCK2 to TCK0 are set to 101b (TRDCLK input) and the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).
4. To select fOCO-F, set it to the clock frequency higher than the CPU clock frequency.

20.7.9 Timer RD Status Register i (TRDSRi) (i = 0 or 1) in Complementary PWM Mode

Address 0143h (TRDSR0), 0153h (TRDSR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	UDF	OVF	IMFD	IMFC	IMFB	IMFA	
After Reset	1	1	1	0	0	0	0	0	TRDSR0 register
After Reset	1	1	0	0	0	0	0	0	TRDSR1 register

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input capture / compare match flag A	[Source for setting this bit to 0] Write 0 after read (2). [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRAi register.	R/W
b1	IMFB	Input capture / compare match flag B	[Source for setting this bit to 0] Write 0 after read (2). [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRBi register.	R/W
b2	IMFC	Input capture / compare match flag C	[Source for setting this bit to 0] Write 0 after read (2). [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRCi register (3).	R/W
b3	IMFD	Input capture / compare match flag D	[Source for setting this bit to 0] Write 0 after read (2). [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRDi register (3).	R/W
b4	OVF	Overflow flag	[Source for setting this bit to 0] Write 0 after read (2). [Source for setting this bit to 1] When the TRDi register overflows.	R/W
b5	UDF	Underflow flag (1)	[Source for setting this bit to 0] Write 0 after read (2). [Source for setting this bit to 1] When the TRD1 register underflows.	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b7	—			

Notes:
1. Nothing is assigned to b5 in the TRDSR0 register. When writing to b5, write 0. When reading, the content is 1.
2. The writing results are as follows:
   - This bit is set to 0 when the read result is 1 and 0 is written to the same bit.
   - This bit remains unchanged even if the read result is 0 and 0 is written to the same bit. (This bit remains 1 even if it is set to 1 from 0 after reading, and writing 0.)
   - This bit remains unchanged if 1 is written to it.
3. Including when the BFji bit in the TRDMR register is set to 1 (TRDGRji is used as the buffer register).

20.7.10 Timer RD Interrupt Enable Register i (TRDIERi) (i = 0 or 1) in Complementary PWM Mode

Address 0144h (TRDIER0), 0154h (TRDIER1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	OVIE	IMIED	IMIEC	IMIEB	IMIEA
After Reset	1	1	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input capture/compare match interrupt enable bit A	0: Disable interrupt (IMIA) by the IMFA bit 1: Enable interrupt (IMIA) by the IMFA bit	R/W
b1	IMIEB	Input capture/compare match interrupt enable bit B	0: Disable interrupt (IMIB) by the IMFB bit 1: Enable interrupt (IMIB) by the IMFB bit	R/W
b2	IMIEC	Input capture/compare match interrupt enable bit C	0: Disable interrupt (IMIC) by the IMFC bit 1: Enable interrupt (IMIC) by the IMFC bit	R/W
b3	IMIED	Input capture/compare match interrupt enable bit D	0: Disable interrupt (IMID) by the IMFD bit 1: Enable interrupt (IMID) by the IMFD bit	R/W
b4	OVIE	Overflow/underflow interrupt enable bit	0: Disable interrupt (OVI) by the OVF or UDF bit 1: Enable interrupt (OVI) by the OVF or UDF bit	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b6	—			
b7	—			

20.7.11 Timer RD Counter 0 (TRD0) in Complementary PWM Mode

Address 0147h to 0146h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15 to b0	Set the dead time. Count a count source. Count operation is incremented or decremented. When an overflow occurs, the OVF bit in the TRDSR0 register is set to 1.	0000h to FFFFh	R/W

Access the TRD0 register in 16-bit units. Do not access it in 8-bit units.

20.7.12 Timer RD Counter 1 (TRD1) in Complementary PWM Mode

Address 0157h to 0156h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15 to b0	Set 0000h. Count a count source. Count operation is incremented or decremented. When an underflow occurs, the UDF bit in the TRDSR1 register is set to 1.	0000h to FFFFh	R/W

Access the TRD1 register in 16-bit units. Do not access it in 8-bit units.

20.7.13 Timer RD General Registers Ai, Bi, C1, and Di (TRDGRAi, TRDGRBi, TRDGRC1, TRDGRDi) (i = 0 or 1) in Complementary PWM Mode

Address 0149h to 0148h (TRDGRA0), 014Bh to 014Ah (TRDGRB0),
014Fh to 014Eh (TRDGRD0),
0159h to 0158h (TRDGRA1), 015Bh to 015Ah (TRDGRB1),
015Dh to 015Ch (TRDGRC1), 015Fh to 015Eh (TRDGRD1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b15 to b0	Refer to **Table 20.14 TRDGRji Register Functions in Complementary PWM Mode**	R/W

Access registers TRDGRAi to TRDGRDi in 16-bit units. Do not access them in 8-bit units.
The TRDGRC0 register is not used in complementary PWM mode.

The following registers are disabled in the complementary PWM mode: TRDPMR, TRDOCR, TRDDF0, TRDDF1, TRDIORA0, TRDIORC0, TRDPOCR0, TRDIORA1, TRDIORC1, and TRDPOCR1.

Table 20.14 TRDGRji Register Functions in Complementary PWM Mode

Register	Setting	Register Function	PWM Output Pin
TRDGRA0	–	General register. Set the PWM period at initialization. Setting range: Setting value or above in TRD0 register FFFFh - TRD0 register setting value or below Do not write to this register when the TSTART0 and TSTART1 bits in the TRDSTR register are set to 1 (count starts).	(Output inverted every half period of TRDIOC0 pin)
TRDGRB0	–	General register. Set the changing point of PWM1 output at initialization. Setting range: Setting value or above in TRD0 register TRDGRA0 register - TRD0 register setting value or below Do not write to this register when the TSTART0 and TSTART1 bits in the TRDSTR register are set to 1 (count starts).	TRDIOB0 TRDIOD0
TRDGRA1	–	General register. Set the changing point of PWM2 output at initialization. Setting range: Setting value or above in TRD0 register TRDGRA0 register - TRD0 register setting value or below Do not write to this register when the TSTART0 and TSTART1 bits in the TRDSTR register are set to 1 (count starts).	TRDIOA1 TRDIOC1
TRDGRB1	–	General register. Set the changing point of PWM3 output at initialization. Setting range: Setting value or above in TRD0 register TRDGRA0 register - TRD0 register setting value or below Do not write to this register when the TSTART0 and TSTART1 bits in the TRDSTR register are set to 1 (count starts).	TRDIOB1 TRDIOD1
TRDGRC0	–	This register is not used in complementary PWM mode.	–
TRDGRD0	BFD0 = 1	Buffer register. Set the changing point of next PWM1 output. (Refer to **20.2.2 Buffer Operation.**) Setting range: Setting value or above in TRD0 register TRDGRA0 register - TRD0 register setting value or below Set this register to the same value as the TRDGRB0 register for initialization.	TRDIOB0 TRDIOD0
TRDGRC1	BFC1 = 1	Buffer register. Set the changing point of next PWM2 output. (Refer to **20.2.2 Buffer Operation.**) Setting range: Setting value or above in TRD0 register TRDGRA0 register - TRD0 register setting value or below Set this register to the same value as the TRDGRA1 register for initialization.	TRDIOA1 TRDIOC1
TRDGRD1	BFD1 = 1	Buffer register. Set the changing point of next PWM3 output. (Refer to **20.2.2 Buffer Operation.**) Setting range: Setting value or above in TRD0 register TRDGRA0 register - TRD0 register setting value or below Set this register to the same value as the TRDGRB1 register for initialization.	TRDIOB1 TRDIOD1

BFD0, BFC1, BFD1: Bits in TRDMR register

Since values cannot be written to the TRDGRB0, TRDGRA1, or TRDGRB1 register directly after count operation starts (prohibited item), use the TRDGRD0, TRDGRC1, or TRDGRD1 register as a buffer register. However, to write data to the TRDGRD0, TRDGRC1, or TRDGRD1 register, set bits BFD0, BFC1, and BFD1 to 0 (general register). After this, bits BFD0, BFC1, and BFD1 may be set to 1 (buffer register).

20.7.14 Timer RD Pin Select Register 0 (TRDPSR0)

Address 0184h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	TRDIOD0SEL0	—	TRDIOC0SEL0	—	TRDIOB0SEL0	—	TRDIOA0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRDIOA0SEL0	TRDIOA0/TRDCLK pin select bit	0: TRDIOA0/TRDCLK pin not used 1: P2_0 assigned	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	TRDIOB0SEL0	TRDIOB0 pin select bit	0: TRDIOB0 pin not used 1: P2_1 assigned	R/W
b3	—	Reserved bit	Set to 0.	R/W
b4	TRDIOC0SEL0	TRDIOC0 pin select bit	0: TRDIOC0 pin not used 1: P2_2 assigned	R/W
b5	—	Reserved bit	Set to 0.	R/W
b6	TRDIOD0SEL0	TRDIOD0 pin select bit	0: TRDIOD0 pin not used 1: P2_3 assigned	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

The TRDPSR0 register selects which pin is assigned to the timer RD I/O. To use the I/O pin for timer RD, set this register.
Set the TRDPSR0 register before setting the timer RD associated registers. Also, do not change the setting value in this register during timer RD operation.

20.7.15 Timer RD Pin Select Register 1 (TRDPSR1)

Address 0185h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	TRDIOD1SEL0	—	TRDIOC1SEL0	—	TRDIOB1SEL0	—	TRDIOA1SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRDIOA1SEL0	TRDIOA1 pin select bit	0: TRDIOA1 pin not used 1: P2_4 assigned	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	TRDIOB1SEL0	TRDIOB1 pin select bit	0: TRDIOB1 pin not used 1: P2_5 assigned	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TRDIOC1SEL0	TRDIOC1 pin select bit	0: TRDIOC1 pin not used 1: P2_6 assigned	R/W
b5	—	Reserved bit	Set to 0.	R/W
b6	TRDIOD1SEL0	TRDIOD1 pin select bit	0: TRDIOD1 pin not used 1: P2_7 assigned	R/W
b7	—	Reserved bit	Set to 0.	R/W

The TRDPSR1 register selects which pin is assigned to the timer RD I/O. To use the I/O pin for timer RD, set this register.
Set the TRDPSR1 register before setting the timer RD associated registers. Also, do not change the setting value in this register during timer RD operation.

20.7.16 Operating Example

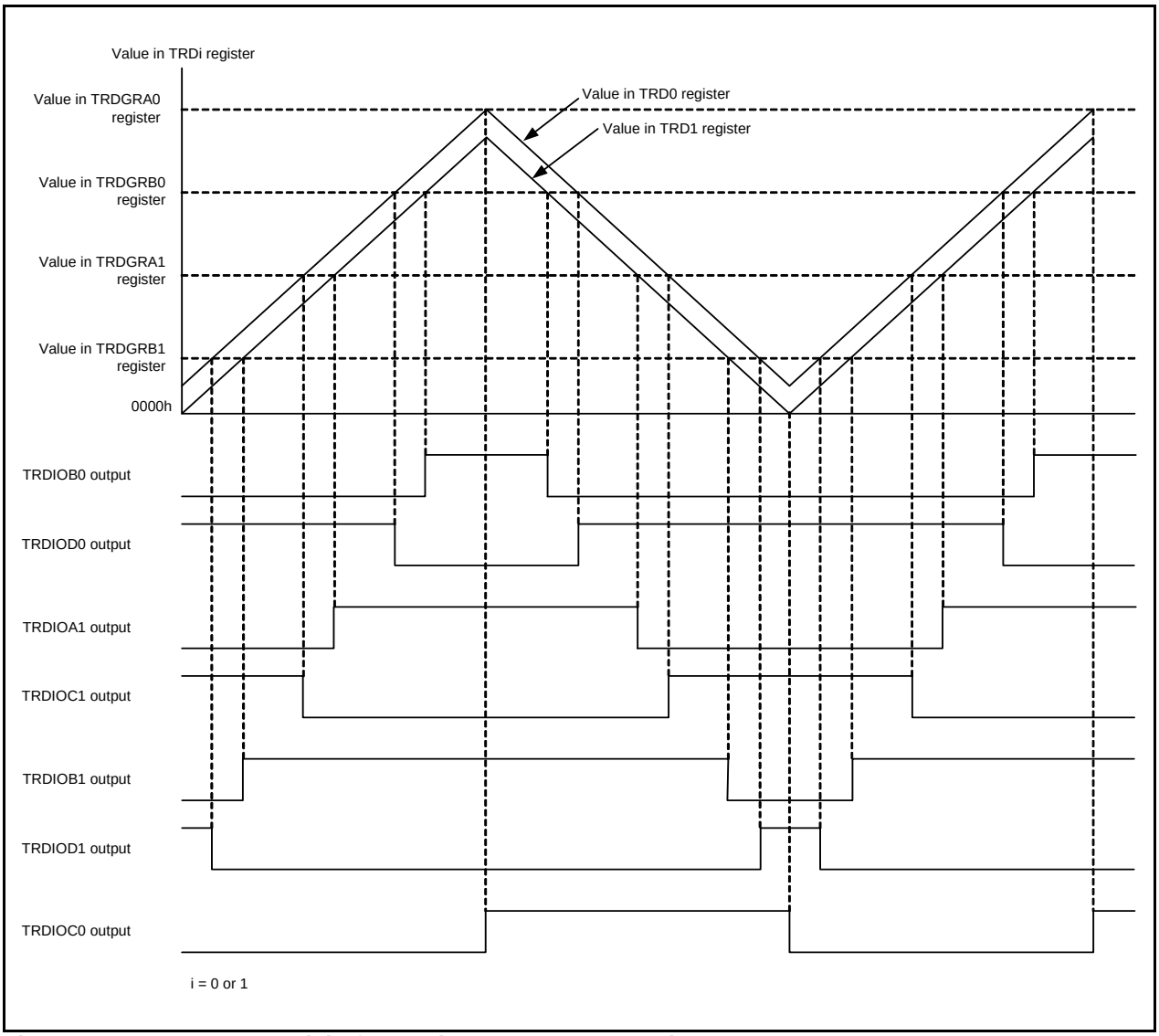


Figure 20.20 Output Model of Complementary PWM Mode

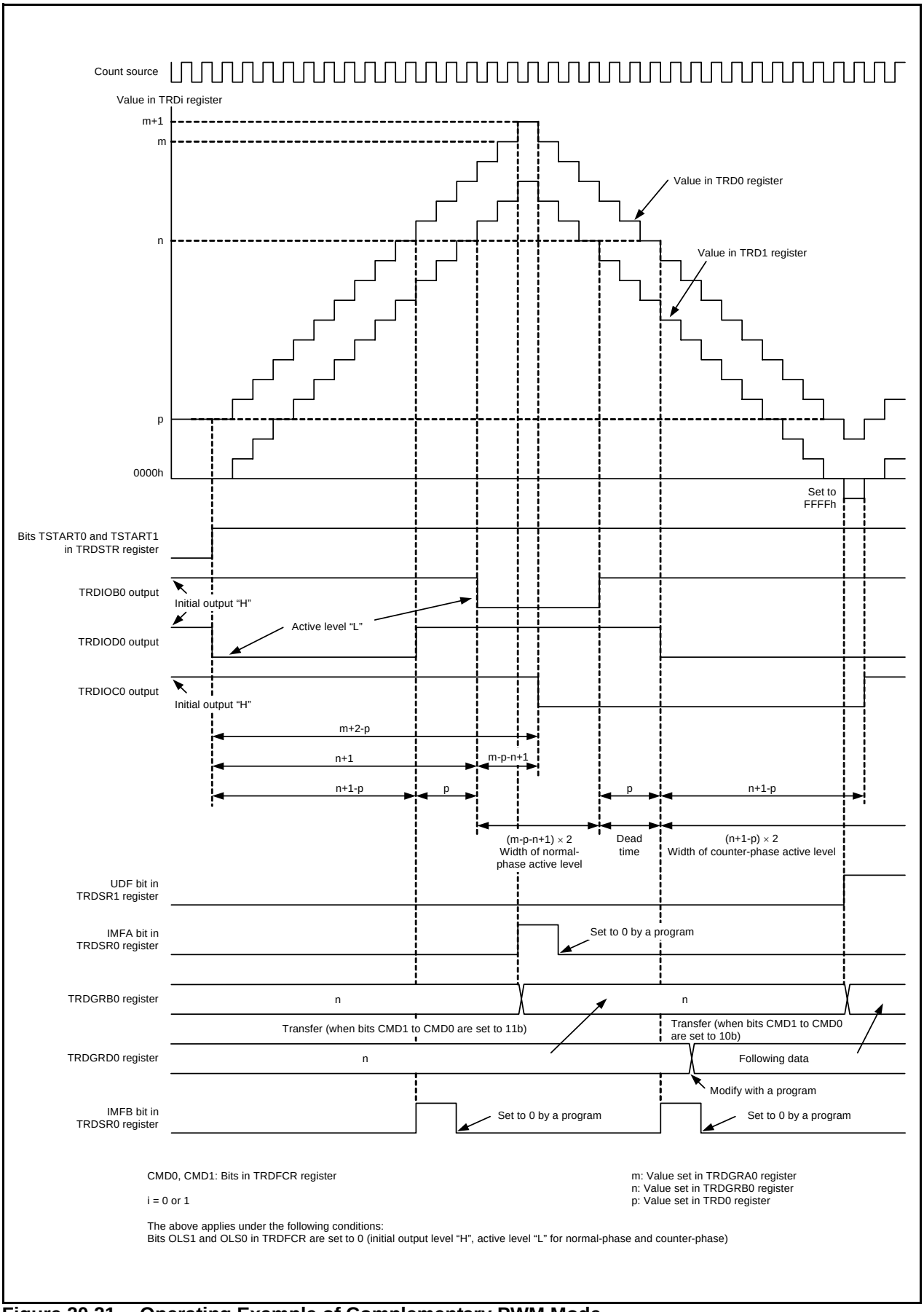


Figure 20.21 Operating Example of Complementary PWM Mode

20.7.17 Transfer Timing from Buffer Register

- Transfer from the TRDGRD0, TRDGRC1, or TRDGRD1 register to the TRDGRB0, TRDGRA1, or TRDGRB1 register.
  When bits CMD1 to CMD0 in the TRDFCR register are set to 10b, the content is transferred when the TRD1 register underflows.
  When bits CMD1 to CMD0 are set to 11b, the content is transferred at compare match between registers TRD0 and TRDGRA0.

20.7.18 A/D Trigger Generation

Compare match between registers TRD0 and TRDGRA0 and TRD1 underflow can be used as the conversion start trigger of the A/D converter.
Use bits ADEG and ADTRG in the TRDFCR register and the TRDADCR register to make settings.
In addition, set bits ADCAP1 to ADCAP0 in the ADMOD register to 01b (A/D conversion starts by conversion trigger from timer RD).

20.8 PWM3 Mode

In this mode, 2 PWM waveforms are output with the same period.
Figure 20.22 shows a Block Diagram of PWM3 Mode, and Table 20.15 lists the PWM3 Mode Specifications.
Figure 20.23 shows an Operating Example of PWM3 Mode.

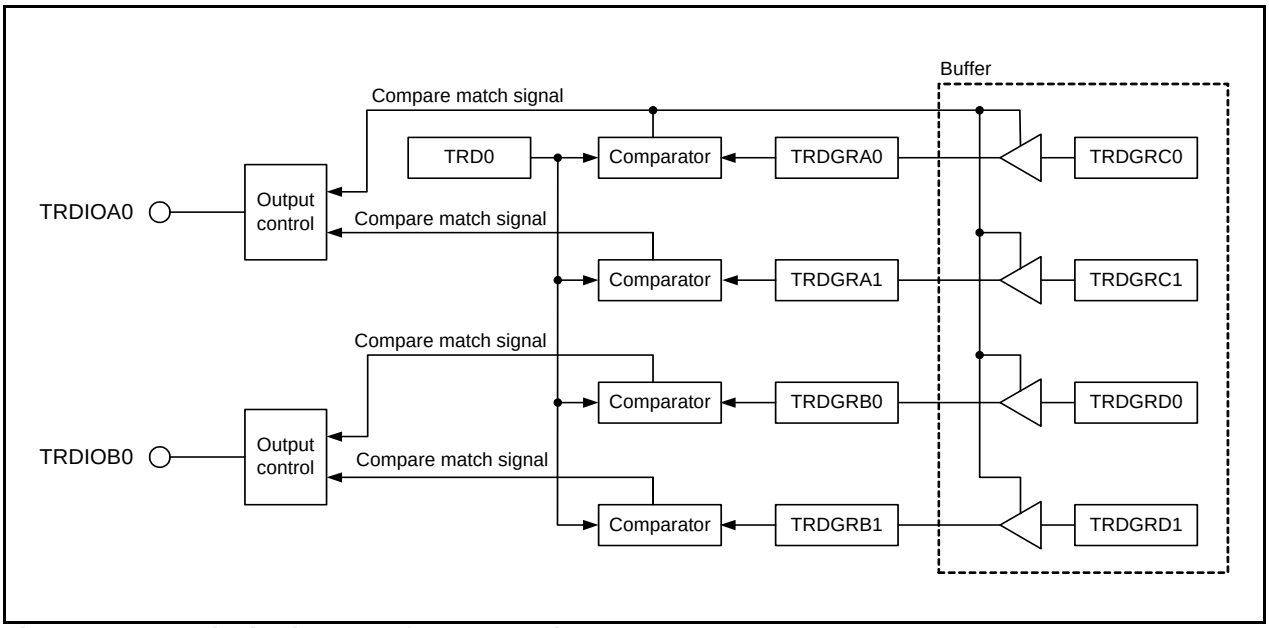
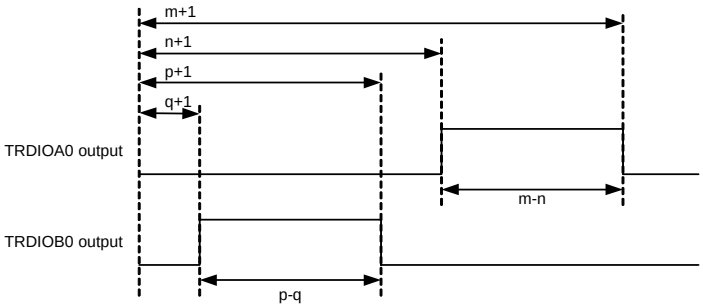


Figure 20.22 Block Diagram of PWM3 Mode

Table 20.15 PWM3 Mode Specifications

Item	Specification
Count sources	f1, f2, f4, f8, f32, fOCO40M, fOCO-F
Count operations	The TRD0 register is incremented (the TRD1 is not used).
PWM waveform	PWM period: 1/fk × (m+1) Active level width of TRDIOA0 output: 1/fk × (m-n) Active level width of TRDIOB0 output: 1/fk × (p-q) fk: Frequency of count source m: Value set in the TRDGRA0 register n: Value set in the TRDGRA1 register p: Value set in the TRDGRB0 register q: Value set in the TRDGRB1 register  (When “H” is selected as the active level)
Count start condition	1 (count starts) is written to the TSTART0 bit in the TRDSTR register.
Count stop conditions	• 0 (count stops) is written to the TSTART0 bit in the TRDSTR register when the CSEL0 bit in the TRDSTR register is set to 1. The PWM output pin holds output level before the count stops • When the CSEL0 bit in the TRDSTR register is set to 0, the count stops at compare match with the TRDGRA0 register. The PWM output pin holds level after output change by compare match.
Interrupt request generation timing	• Compare match (The content of the TRDi register matches content of the TRDGRji register.) • The TRD0 register overflows
TRDIOA0, TRDIOB0 pin functions	PWM output
TRDIOC0, TRDIOD0, TRDIOA1 to TRDIOD1 pin functions	Programmable I/O port
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRD0 register.
Write to timer	The value can be written to the TRD0 register.
Selectable functions	• Pulse output forced cutoff signal input (Refer to **20.2.4 Pulse Output Forced Cutoff.**) • Buffer operation (Refer to **20.2.2 Buffer Operation.**) • Active level selectable for each pin • A/D trigger generation

i = 0 or 1, j = either A, B, C, or D

20.8.1 Module Standby Control Register (MSTCR)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	MSTTRG	MSTTRC	MSTTRD	MSTIIC	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	MSTIIC	SSU standby bit	0: Active 1: Standby (1)	R/W
b4	MSTTRD	Timer RD standby bit	0: Active 1: Standby (2, 3)	R/W
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (4)	R/W
b6	MSTTRG	Timer RG standby bit	0: Active 1: Standby (5)	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. When the MSTIIC bit is set to 1 (standby), any access to the SSU associated registers (addresses 0193h to 019Dh) is disabled.
2. When the MSTTRD bit is set to 1 (standby), any access to the timer RD associated registers (addresses 0136h to 015Fh) is disabled.
3. To set the MSTTRD bit to 1 (standby), set bits TCK2 to TCK0 in the TRDCRi (i = 0 or 1) register to 000b (f1).
4. When the MSTTRC bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0120h to 0133h) is disabled.
5. When the MSTTRG bit is set to 1 (standby), any access to the timer RG associated registers (addresses 0170h to 017Fh) is disabled.

20.8.2 Timer RD Trigger Control Register (TRDADCR)

Address 0136h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADTRGD1E	ADTRGC1E	ADTRGB1E	ADTRGA1E	ADTRGD0E	ADTRGC0E	ADTRGB0E	ADTRGA0E
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADTRGA0E	A/D trigger A0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRA0	R/W
b1	ADTRGB0E	A/D trigger B0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRB0	R/W
b2	ADTRGC0E	A/D trigger C0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRC0	R/W
b3	ADTRGD0E	A/D trigger D0 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD0 and TRDGRD0	R/W
b4	ADTRGA1E	A/D trigger A1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRA1	R/W
b5	ADTRGB1E	A/D trigger B1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRB1	R/W
b6	ADTRGC1E	A/D trigger C1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRC1	R/W
b7	ADTRGD1E	A/D trigger D1 enable bit	0: A/D trigger disabled 1: A/D trigger generated at compare match with registers TRD1 and TRDGRD1	R/W

20.8.3 Timer RD Start Register (TRDSTR) in PWM3 Mode

Address 0137h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	CSEL1	CSEL0	TSTART1	TSTART0
After Reset	1	1	1	1	1	1	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART0	TRD0 count start flag (3)	0: Count stops (1) 1: Count starts	R/W
b1	TSTART1	TRD1 count start flag (4)	0: Count stops (2) 1: Count starts	R/W
b2	CSEL0	TRD0 count operation select bit	0: Count stops at the compare match with the TRDGRA0 register 1: Count continues after the compare match with the TRDGRA0 register	R/W
b3	CSEL1	TRD1 count operation select bit [this bit is not used in PWM3 mode]	0: Count stops at the compare match with the TRDGRA1 register 1: Count continues after the compare match with the TRDGRA1 register	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	—			

Notes:
1. When the CSEL0 bit is set to 1, write 0 to the TSTART0 bit.
2. When the CSEL1 bit is set to 1, write 0 to the TSTART1 bit.
3. When the CSEL0 bit is set to 0 and the compare match signal (TRDIOA0) is generated, this bit is set to 0 (count stops).
4. When the CSEL1 bit is set to 0 and the compare match signal (TRDIOA1) is generated, this bit is set to 0 (count stops).

Set the TRDSTR register using the MOV instruction (do not use the bit handling instruction). Refer to **20.10.1 TRDSTR Register** of **Notes on Timer RD**.

20.8.4 Timer RD Mode Register (TRDMR) in PWM3 Mode

Address 0138h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BFD1	BFC1	BFD0	BFC0	—	—	—	SYNC
After Reset	0	0	0	0	1	1	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	SYNC	Timer RD synchronous bit	Set this bit to 0 (TRD0 and TRD1 operate independently) in PWM3 mode.	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b2	—			
b3	—			
b4	BFC0	TRDGRC0 register function select bit	0: General register 1: Buffer register of TRDGRA0 register	R/W
b5	BFD0	TRDGRD0 register function select bit	0: General register 1: Buffer register of TRDGRB0 register	R/W
b6	BFC1	TRDGRC1 register function select bit	0: General register 1: Buffer register of TRDGRA1 register	R/W
b7	BFD1	TRDGRD1 register function select bit	0: General register 1: Buffer register of TRDGRB1 register	R/W

20.8.5 Timer RD Function Control Register (TRDFCR) in PWM3 Mode

Address 013Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PWM3	STCLK	ADEG	ADTRG	OLS1	OLS0	CMD1	CMD0
After Reset	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CMD0	Combination mode select bit (1)	Set to 00b (timer mode, PWM mode, or PWM3 mode) in PWM3 mode.	R/W
b1	CMD1			R/W
b2	OLS0	Normal-phase output level select bit (enabled in reset synchronous PWM mode or complementary PWM mode)	This bit is disabled in PWM3 mode.	R/W
b3	OLS1	Counter-phase output level select bit (enabled in reset synchronous PWM mode or complementary PWM mode)		R/W
b4	ADTRG	A/D trigger enable bit (enabled in complementary PWM mode)		R/W
b5	ADEG	A/D trigger edge select bit (enabled in complementary PWM mode)		R/W
b6	STCLK	External clock input select bit	Set this bit to 0 (external clock input disabled) in PWM3 mode.	R/W
b7	PWM3	PWM3 mode select bit (2)	Set this bit to 0 (PWM3 mode) in PWM3 mode.	R/W

Notes:
1. Set bits CMD1 to CMD0 when both the TSTART0 and TSTART1 bits in the TRDSTR register are set to 0 (count stops).
2. When bits CMD1 to CMD0 are set to 00b (timer mode, PWM mode, or PWM3 mode), the setting of the PWM3 bit is enabled.

20.8.6 Timer RD Output Master Enable Register 1 (TRDOER1) in PWM3 Mode

Address 013Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ED1	EC1	EB1	EA1	ED0	EC0	EB0	EA0
After Reset	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	EA0	TRDIOA0 output disable bit	0: Enable output 1: Disable output (The TRDIOA0 pin is used as a programmable I/O port.)	R/W
b1	EB0	TRDIOB0 output disable bit	0: Enable output 1: Disable output (The TRDIOB0 pin is used as a programmable I/O port.)	R/W
b2	EC0	TRDIOC0 output disable bit	Set these bits to 1 (programmable I/O port) in PWM3 mode.	R/W
b3	ED0	TRDIOD0 output disable bit		R/W
b4	EA1	TRDIOA1 output disable bit		R/W
b5	EB1	TRDIOB1 output disable bit		R/W
b6	EC1	TRDIOC1 output disable bit		R/W
b7	ED1	TRDIOD1 output disable bit		R/W

20.8.7 Timer RD Output Master Enable Register 2 (TRDOER2) in PWM3 Mode

Address 013Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PTO	—	—	—	—	—	—	—
After Reset	0	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	PTO	$\overline{\text{INT0}}$ of pulse output forced cutoff signal input enabled bit (1)	0: Pulse output forced cutoff input disabled 1: Pulse output forced cutoff input enabled (All bits in the TRDOER1 register are set to 1 (disable output) when “L” is applied to the $\overline{\text{INT0}}$ pin.)	R/W

Note:
1. Refer to **20.2.4 Pulse Output Forced Cutoff**.

20.8.8 Timer RD Output Control Register (TRDOCR) in PWM3 Mode

Address 013Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TOD1	TOC1	TOB1	TOA1	TOD0	TOC0	TOB0	TOA0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA0	TRDIOA0 output level select bit (1)	0: Active level “H”, initial output “L”, output “H” at compare match with the TRDGRA1 register, output “L” at compare match with the TRDGRA0 register 1: Active level “L”, initial output “H”, output “L” at compare match with the TRDGRA1 register, output “H” at compare match with the TRDGRA0 register	R/W
b1	TOB0	TRDIOB0 output level select bit (1)	0: Active level “H”, initial output “L”, output “H” at compare match with the TRDGRB1register, output “L” at compare match with the TRDGRB0 register 1: Active level “L”, initial output “H”, output “L” at compare match with the TRDGRB1 register, output “H” at compare match with the TRDGRB0 register	R/W
b2	TOC0	TRDIOC0 initial output level select bit	These bits are disabled in PWM3 mode.	R/W
b3	TOD0	TRDIOD0 initial output level select bit		R/W
b4	TOA1	TRDIOA1 initial output level select bit		R/W
b5	TOB1	TRDIOB1 initial output level select bit		R/W
b6	TOC1	TRDIOC1 initial output level select bit		R/W
b7	TOD1	TRDIOD1 initial output level select bit		R/W

Note:

1. If the pin function is set for waveform output (refer to **7.5 Port Settings**), the initial output level is output when the TRDOCR register is set.

   Write to the TRDOCR register when both bits TSTART0 and TSTART1 in the TRDSTR register are set to 0 (count stops).

20.8.9 Timer RD Control Register 0 (TRDCR0) in PWM3 Mode

Address 0140h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TCK2	TCK1	TCK0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TCK0	Count source select bit	b2 b1 b0 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: Do not set. 1 1 0: fOCO40M 1 1 1: fOCO-F (1)	R/W
b1	TCK1			R/W
b2	TCK2			R/W
b3	CKEG0	External clock edge select bit	These bits are disabled in PWM3 mode.	R/W
b4	CKEG1			R/W
b5	CCLR0	TRD0 counter clear select bit	Set to 001b (the TRD0 register cleared at compare match with TRDGRA0 register) in PWM3 mode.	R/W
b6	CCLR1			R/W
b7	CCLR2			R/W

Note:
1. To select fOCO-F, set it to the clock frequency higher than the CPU clock frequency.

The TRDCR1 register is not used in PWM3 mode.

20.8.10 Timer RD Status Register i (TRDSRi) (i = 0 or 1) in PWM3 Mode

Address 0143h (TRDSR0), 0153h (TRDSR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	UDF	OVF	IMFD	IMFC	IMFB	IMFA	
After Reset	1	1	1	0	0	0	0	0	TRDSR0 register
After Reset	1	1	0	0	0	0	0	0	TRDSR1 register

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input capture / compare match flag A	[Source for setting this bit to 0] Write 0 after read (2). [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRAi register.	R/W
b1	IMFB	Input capture / compare match flag B	[Source for setting this bit to 0] Write 0 after read (2). [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRBi register.	R/W
b2	IMFC	Input capture / compare match flag C	[Source for setting this bit to 0] Write 0 after read (2). [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRCi register (3).	R/W
b3	IMFD	Input capture / compare match flag D	[Source for setting this bit to 0] Write 0 after read (2). [Source for setting this bit to 1] When the value in the TRDi register matches with the value in the TRDGRDi register (3).	R/W
b4	OVF	Overflow flag	[Source for setting this bit to 0] Write 0 after read (2). [Source for setting this bit to 1] When the TRDi register overflows.	R/W
b5	UDF	Underflow flag (1)	This bit is disabled in PWM3 Mode.	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b7	—			

Notes:
1. Nothing is assigned to b5 in the TRDSR0 register. When writing to b5, write 0. When reading, the content is 1.
2. The writing results are as follows:
   - This bit is set to 0 when the read result is 1 and 0 is written to the same bit.
   - This bit remains unchanged even if the read result is 0 and 0 is written to the same bit. (This bit remains 1 even if it is set to 1 from 0 after reading, and writing 0.)
   - This bit remains unchanged if 1 is written to it.
3. Including w hen the BFji (j = C or D) bit in the TRDMR register is set to 1 (TRDGRji is used as the buffer register).

20.8.11 Timer RD Interrupt Enable Register i (TRDIERi) (i = 0 or 1) in PWM3 Mode

Address 0144h (TRDIER0), 0154h (TRDIER1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	OVIE	IMIED	IMIEC	IMIEB	IMIEA
After Reset	1	1	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input capture/compare match interrupt enable bit A	0: Disable interrupt (IMIA) by the IMFA bit 1: Enable interrupt (IMIA) by the IMFA bit	R/W
b1	IMIEB	Input capture/compare match interrupt enable bit B	0: Disable interrupt (IMIB) by the IMFB bit 1: Enable interrupt (IMIB) by the IMFB bit	R/W
b2	IMIEC	Input capture/compare match interrupt enable bit C	0: Disable interrupt (IMIC) by the IMFC bit 1: Enable interrupt (IMIC) by the IMFC bit	R/W
b3	IMIED	Input capture/compare match interrupt enable bit D	0: Disable interrupt (IMID) by the IMFD bit 1: Enable interrupt (IMID) by the IMFD bit	R/W
b4	OVIE	Overflow/underflow interrupt enable bit	0: Disable interrupt (OVI) by the OVF bit 1: Enable interrupt (OVI) by the OVF bit	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b6	—			
b7	—			

20.8.12 Timer RD Counter 0 (TRD0) in PWM3 Mode

Address 0147h to 0146h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15 to b0	Count a count source. Count operation is incremented. When an overflow occurs, the OVF bit in the TRDSR0 register is set to 1.	0000h to FFFFh	R/W

Access the TRD0 register in 16-bit units. Do not access it in 8-bit units.
The TRD1 register is not used in PWM3 mode.

20.8.13 Timer RD General Registers Ai, Bi, Ci, and Di (TRDGRAi, TRDGRBi, TRDGRCi, TRDGRDi) (i = 0 or 1) in PWM3 Mode

Address 0149h to 0148h (TRDGRA0), 014Bh to 014Ah (TRDGRB0),
014Dh to 014Ch (TRDGRC0), 014Fh to 014Eh (TRDGRD0),
0159h to 0158h (TRDGRA1), 015Bh to 015Ah (TRDGRB1),
015Dh to 015Ch (TRDGRC1), 015Fh to 015Eh (TRDGRD1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b15 to b0	Refer to **Table 20.16 TRDGRji Register Functions in PWM3 Mode**	R/W

Access registers TRDGRAi to TRDGRDi in 16-bit units. Do not access them in 8-bit units.

The following registers are disabled in the PWM3 mode function: TRDPMR, TRDDF0, TRDDF1, TRDIORA0, TRDIORC0, TRDPOCR0, TRDIORA1, TRDIORC1, and TRDPOCR1.

Table 20.16 TRDGRji Register Functions in PWM3 Mode

Register	Setting	Register Function	PWM Output Pin
TRDGRA0	–	General register. Set the PWM period. Setting range: Value set in TRDGRA1 register or above	TRDIOA0
TRDGRA1		General register. Set the changing point (the active level timing) of PWM output. Setting range: Value set in TRDGRA0 register or below	
TRDGRB0		General register. Set the changing point (the timing that returns to initial output level) of PWM output. Setting range: Value set in TRDGRB1 register or above Value set in TRDGRA0 register or below	TRDIOB0
TRDGRB1		General register. Set the changing point (active level timing) of PWM output. Setting range: Value set in TRDGRB0 register or below	
TRDGRC0	BFC0 = 0	(These registers is not used in PWM3 mode.)	–
TRDGRC1	BFC1 = 0		
TRDGRD0	BFD0 = 0		
TRDGRD1	BFD1 = 0		
TRDGRC0	BFC0 = 1	Buffer register. Set the next PWM period. (Refer to **20.2.2 Buffer Operation**.) Setting range: Value set in TRDGRC1 register or above	TRDIOA0
TRDGRC1	BFC1 = 1	Buffer register. Set the changing point of next PWM output. (Refer to **20.2.2 Buffer Operation**.) Setting range: Value set in TRDGRC0 register or below	
TRDGRD0	BFD0 = 1	Buffer register. Set the changing point of next PWM output. (Refer to **20.2.2 Buffer Operation**.) Setting range: Value set in TRDGRD1 register or above, setting value or below in TRDGRC0 register.	TRDIOB0
TRDGRD1	BFD1 = 1	Buffer register. Set the changing point of next PWM output. (Refer to **20.2.2 Buffer Operation**.) Setting range: Value set in TRDGRD0 register or below	

BFC0, BFD0, BFC1, BFD1: Bits in TRDMR register

Registers TRDGRC0, TRDGRC1, TRDGRD0, and TRDGRD1 are not used in PWM3 mode. To use them as buffer registers, set bits BFC0, BFC1, BFD0, and BFD1 to 0 (general register) and write a value to the TRDGRC0, TRDGRC1, TRDGRD0, or TRDGRD1 register. After this, bits BFC0, BFC1, BFD0, and BFD1 may be set to 1 (buffer register).

20.8.14 Timer RD Pin Select Register 0 (TRDPSR0)

Address 0184h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	TRDIOD0SEL0	—	TRDIOC0SEL0	—	TRDIOB0SEL0	—	TRDIOA0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRDIOA0SEL0	TRDIOA0/TRDCLK pin select bit	0: TRDIOA0/TRDCLK pin not used 1: P2_0 assigned	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	TRDIOB0SEL0	TRDIOB0 pin select bit	0: TRDIOB0 pin not used 1: P2_1 assigned	R/W
b3	—	Reserved bit	Set to 0.	R/W
b4	TRDIOC0SEL0	TRDIOC0 pin select bit	0: TRDIOC0 pin not used 1: P2_2 assigned	R/W
b5	—	Reserved bit	Set to 0.	R/W
b6	TRDIOD0SEL0	TRDIOD0 pin select bit	0: TRDIOD0 pin not used 1: P2_3 assigned	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

The TRDPSR0 register selects which pin is assigned to the timer RD I/O. To use the I/O pin for timer RD, set this register.
Set the TRDPSR0 register before setting the timer RD associated registers. Also, do not change the setting value in this register during timer RD operation.

20.8.15 Timer RD Pin Select Register 1 (TRDPSR1)

Address 0185h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	TRDIOD1SEL0	—	TRDIOC1SEL0	—	TRDIOB1SEL0	—	TRDIOA1SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRDIOA1SEL0	TRDIOA1 pin select bit	0: TRDIOA1 pin not used 1: P2_4 assigned	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	TRDIOB1SEL0	TRDIOB1 pin select bit	0: TRDIOB1 pin not used 1: P2_5 assigned	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TRDIOC1SEL0	TRDIOC1 pin select bit	0: TRDIOC1 pin not used 1: P2_6 assigned	R/W
b5	—	Reserved bit	Set to 0.	R/W
b6	TRDIOD1SEL0	TRDIOD1 pin select bit	0: TRDIOD1 pin not used 1: P2_7 assigned	R/W
b7	—	Reserved bit	Set to 0.	R/W

The TRDPSR1 register selects which pin is assigned to the timer RD I/O. To use the I/O pin for timer RD, set this register.
Set the TRDPSR1 register before setting the timer RD associated registers. Also, do not change the setting value in this register during timer RD operation.

20.8.16 Operating Example

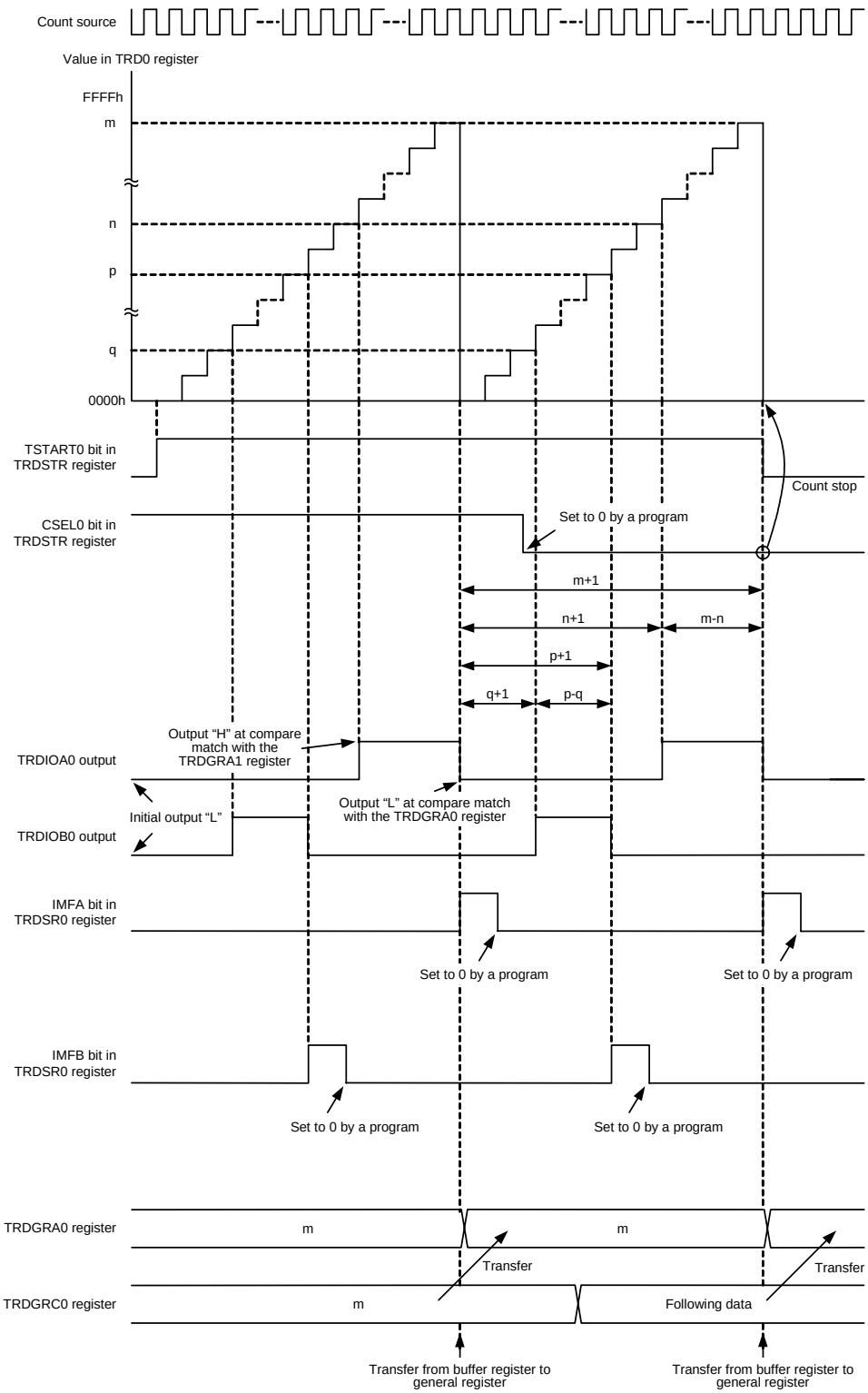


Figure 20.23 Operating Example of PWM3 Mode

20.8.17 A/D Trigger Generation

A compare match signal with registers TRDi (i = 0 or 1) and TRDGRji (j = A, B, C, or D) can be used as the conversion start trigger of the A/D converter.
The TRDADCR register is used to select which compare match is used.

20.9 Timer RD Interrupt

Timer RD generates the timer RDi (i = 0 or 1) interrupt request from six sources for each timer RD0 and timer RD1. The timer RD interrupt has 1 TRDiIC register (bits IR, and ILVL0 to ILVL2), and 1 vector for each timer RD0 and timer RD1.

Table 20.17 Registers Associated with Timer RD Interrupt

	Timer RD Status Register	Timer RD Interrupt Enable Register	Timer RD Interrupt Control Register
Timer RD0	TRDSR0	TRDIER0	TRD0IC
Timer RD1	TRDSR1	TRDIER1	TRD1IC

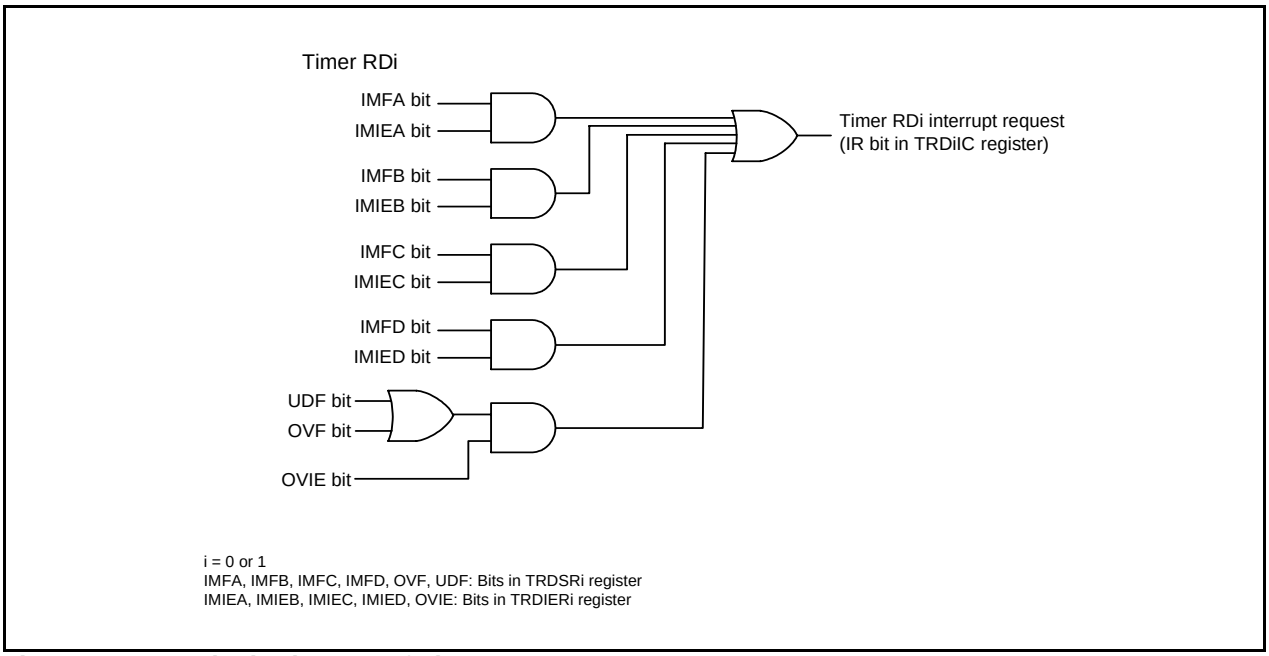


Figure 20.24 Block Diagram of Timer RD Interrupt

As with other maskable interrupts, the timer RD interrupt is controlled by the combination of the I flag, IR bit, bits ILVL0 to ILVL2, and IPL. However, since the interrupt source (timer RD interrupt) is generated by a combination of multiple interrupt request sources, the following differences from other maskable interrupts apply:

- When bits in the TRDSRi register corresponding to bits set to 1 in the TRDIERi register are set to 1 (enable interrupt), the IR bit in the TRDiIC register is set to 1 (interrupt requested).
- When either bits in the TRDSRi register or bits in the TRDIERi register corresponding to bits in the TRDSRi register, or both of them, are set to 0, the IR bit is set to 0 (interrupt not requested). Therefore, even though the interrupt is not acknowledged after the IR bit is set to 1, the interrupt request will not be maintained.
- When the conditions of other request sources are met, the IR bit remains 1.
- When multiple bits in the TRDIERi register are set to 1, which request source causes an interrupt is determined by the TRDSRi register.
- Since each bit in the TRDSRi register is not automatically set to 0 even if the interrupt is acknowledged, set each bit to 0 in the interrupt routine. For information on how to set these bits to 0, refer to the descriptions of the registers used in the different modes (**20.3.10, 20.4.13, 20.5.11, 20.6.9, 20.7.9, and 20.8.10**).

Refer to **Registers TRDSR0 to TRDSR1 in each mode (20.3.10, 20.4.13, 20.5.11, 20.6.9, 20.7.9, and 20.8.10)** for the TRDSRi register. Refer to **Registers TRDIER0 to TRDIER1 in each mode (20.3.11, 20.4.14, 20.5.12, 20.6.10, 20.7.10, and 20.8.11)** for the TRDIERi register.
Refer to **11.3 Interrupt Control** for information on the TRDiIC register and **11.1.5.2 Relocatable Vector Tables** for the interrupt vectors.

20.10 Notes on Timer RD

20.10.1 TRDSTR Register

- Set the TRDSTR register using the MOV instruction.

- When the CSELi (i = 0 to 1) bit is set to 0 (the count stops at compare match of registers TRDi and TRDGRAi), the count does not stop and the TSTARTi bit remains unchanged even if 0 (count stops) is written to the TSTARTi bit.
  Therefore, set the TSTARTi bit to 0 to change other bits without changing the TSTARTi bit when the CSELi bit is se to 0.
  To stop counting by a program, set the TSTARTi bit after setting the CSELi bit to 1. Although the CSELi bit is set to 1 and the TSTARTi bit is set to 0 at the same time (with 1 instruction), the count cannot be stopped.

- Table 20.18 lists the TRDIOji (j = A, B, C, or D) Pin Output Level when Count Stops to use the TRDIOji (j = A, B, C, or D) pin with the timer RD output.

Table 20.18 TRDIOji (j = A, B, C, or D) Pin Output Level when Count Stops

Count Stop	TRDIOji Pin Output when Count Stops
When the CSELi bit is set to 1, set the TSTARTi bit to 0 and the count stops.	The pin holds the output level immediately before the count stops. (The pin outputs the initial output level selected by bits OLS0 and OLS1 in the TRDFCR register in complementary and reset synchronous PWM modes.)
When the CSELi bit is set to 0, the count stops at compare match of registers TRDi and TRDGRAi.	The pin holds the output level after the output changes by compare match. (The pin outputs the initial output level selected by bits OLS0 and OLS1 in the TRDFCR register in complementary and reset synchronous PWM modes.)

20.10.2 TRDi Register (i = 0 or 1)

- When writing the value to the TRDi register by a program while the TSTARTi bit in the TRDSTR register is set to 1 (count starts), avoid overlapping with the timing for setting the TRDi register to 0000h, and then write. If the timing for setting the TRDi register to 0000h overlaps with the timing for writing the value to the TRDi register, the value is not written and the TRDi register is set to 0000h.
  These precautions are applicable when selecting the following by bits CCLR2 to CCLR0 in the TRDCRi register.
  - 001b (Clear the TRDi register by input capture/compare match in the TRDGRAi register.)
  - 010b (Clear the TRDi register by input capture/compare match in the TRDGRBi register.)
  - 011b (Synchronous clear)
  - 101b (Clear the TRDi register by input capture/compare match in the TRDGRCi register.)
  - 110b (Clear the TRDi register by input capture/compare match in the TRDGRDi register.)

- When writing the value to the TRDi register and continuously reading the same register, the value before writing may be read. In this case, execute the JMP.B instruction between the writing and reading.

```
Program example     MOV.W   #XXXXh, TRD0     ;Writing
                    JMP.B   L1               ;JMP.B
                L1: MOV.W   TRD0,DATA        ;Reading
```

20.10.3 TRDSRi Register (i = 0 or 1)

When writing the value to the TRDSRi register and continuously reading the same register, the value before writing may be read. In this case, execute the JMP.B instruction between the writing and reading.

```
Program example     MOV.B   #XXh, TRDSR0     ;Writing
                    JMP.B   L1               ;JMP.B
                L1: MOV.B   TRDSR0,DATA      ;Reading
```

20.10.4 TRDCRi Register (i = 0 or 1)

To set bits TCK2 to TCK0 in the TRDCRi register to 111b (fOCO-F), set fOCO-F to the clock frequency higher than the CPU clock frequency.

20.10.5 Count Source Switching

- Switch the count source after the count stops.

Switching procedure
(1) Set the TSTARTi (i = 0 or 1) bit in the TRDSTR register to 0 (count stops).
(2) Change bits TCK2 to TCK0 in the TRDCRi register.

- When changing the count source from fOCO40M to another clock other than fOCO-F and stopping fOCO40M, wait 2 cycles of f1 or more after setting the clock switch, and then stop fOCO40M.

Switching procedure
(1) Set the TSTARTi (i = 0 or 1) bit in the TRDSTR register to 0 (count stops).
(2) Change bits TCK2 to TCK0 in the TRDCRi register.
(3) Wait 2 or more cycles of f1.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

- After switching the count source from fOCO-F to a clock other than fOCO40M, allow a minimum of one cycle of fOCO-F + fOCO40M to elapse after changing the clock setting before stopping fOCO-F.

Switching procedure
(1) Set the TSTARTi (i = 0 to 1) bit in the TRDSTR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRDCRi register.
(3) Wait for a minimum of one cycle of fOCO-F + fOCO40M.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

20.10.6 Input Capture Function

- Set the pulse width of the input capture signal to 3 or more cycles of the timer RD operation clock (refer to **Table 20.1 Timer RD Operation Clocks**).
- The value in the TRDi register is transferred to the TRDGRji register 2 to 3 cycles of the timer RD operation clock after the input capture signal is applied to the TRDIOji pin (i = 0 or 1, j = either A, B, C, or D) (no digital filter).

20.10.7 Reset Synchronous PWM Mode

- When reset synchronous PWM mode is used for motor control, make sure OLS0 = OLS1.
- Set to reset synchronous PWM mode by the following procedure:

Switching procedure
(1) Set the TSTART0 bit in the TRDSTR register to 0 (count stops).
(2) Set bits CMD1 to CMD0 in the TRDFCR register to 00b (timer mode, PWM mode, and PWM3 mode).
(3) Set bits CMD1 to CMD0 to 01b (reset synchronous PWM mode).
(4) Set the other registers associated with timer RD again.

20.10.8 Complementary PWM Mode

- When complementary PWM mode is used for motor control, make sure OLS0 = OLS1.
- Change bits CMD1 to CMD0 in the TRDFCR register in the following procedure.

Switching procedure: When setting to complementary PWM mode (including re-set), or changing the transfer timing from the buffer register to the general register in complementary PWM mode.

(1) Set both the TSTART0 and TSTART1 bits in the TRDSTR register to 0 (count stops).
(2) Set bits CMD1 to CMD0 in the TRDFCR register to 00b (timer mode, PWM mode, and PWM3 mode).
(3) Set bits CMD1 to CMD0 to 10b or 11b (complementary PWM mode).
(4) Set the registers associated with other timer RD again.

Switching procedure: When stopping complementary PWM mode

(1) Set both the TSTART0 and TSTART1 bits in the TRDSTR register to 0 (count stops).
(2) Set bits CMD1 to CMD to 00b (timer mode, PWM mode, and PWM3 mode).

- Do not write to TRDGRA0, TRDGRB0, TRDGRA1, or TRDGRB1 register during operation.
  When changing the PWM waveform, transfer the values written to registers TRDGRD0, TRDGRC1, and TRDGRD1 to registers TRDGRB0, TRDGRA1, and TRDGRB1 using the buffer operation.
  However, to write data to the TRDGRD0, TRDGRC1, or TRDGRD1 register, set bits BFD0, BFC1, and BFD1 to 0 (general register). After this, bits BFD0, BFC1, and BFD1 may be set to 1 (buffer register).
  The PWM period cannot be changed.
- If the value in the TRDGRA0 register is assumed to be m, the TRD0 register counts m-1, m, m+1, m, m-1, in that order, when changing from increment to decrement operation.
  When changing from m to m+1, the IMFA bit is set to 1. Also, bits CMD1 to CMD0 in the TRDFCR register are set to 11b (complementary PWM mode, buffer data transferred at compare match between registers TRD0 and TRDGRA0), the content in the buffer registers (TRDGRD0, TRDGRC1, and TRDGRD1) is transferred to the general registers (TRDGRB0, TRDGRA1, and TRDGRB1).
  During m+1, m, and m-1 operation, the IMFA bit remains unchanged and data are not transferred to registers such as the TRDGRA0 register.

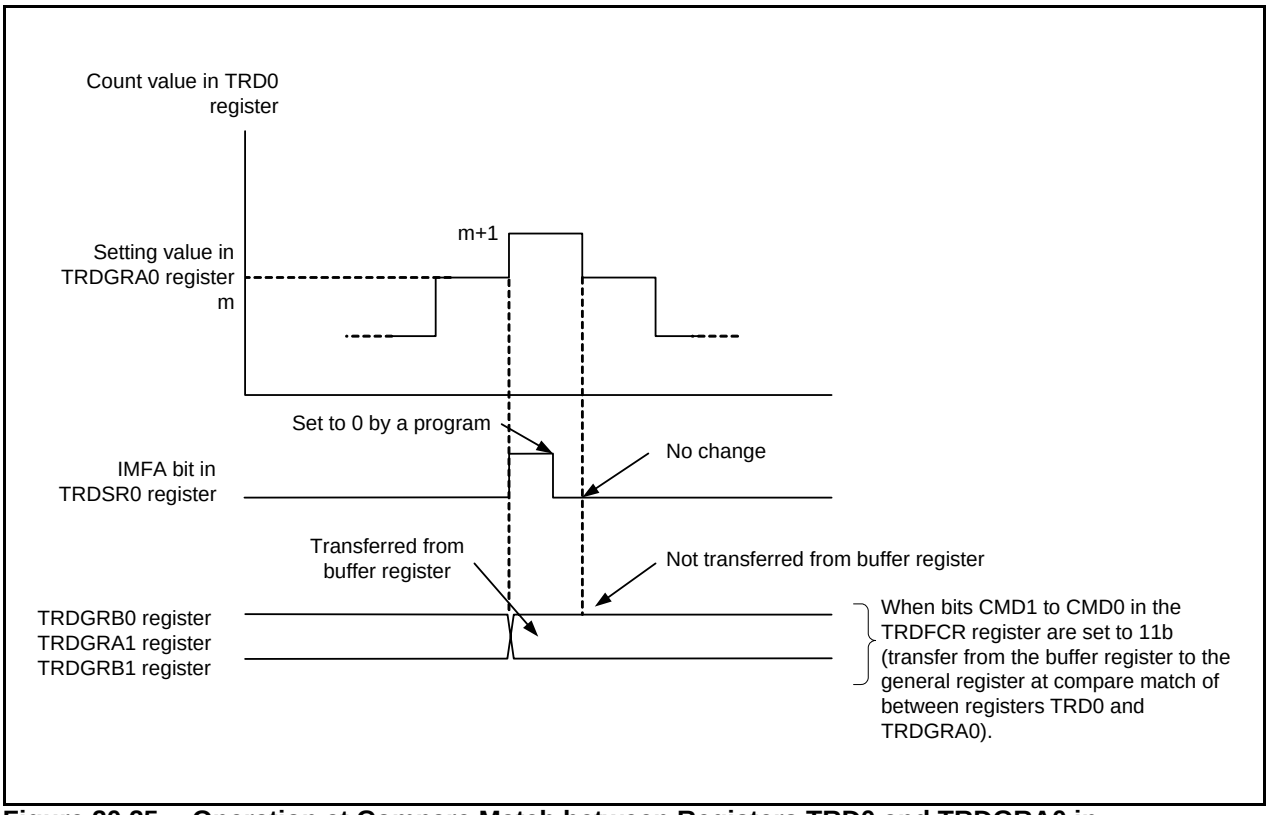


Figure 20.25 Operation at Compare Match between Registers TRD0 and TRDGRA0 in Complementary PWM Mode

- The TRD1 register counts 1, 0, FFFFh, 0, 1, in that order, when changing from decrement to increment operation.

  The UDF bit is set to 1 when changing between 1, 0, and FFFFh operation. Also, when bits CMD1 to CMD0 in the TRDFCR register are set to 10b (complementary PWM mode, buffer data transferred at underflow in the TRD1 register), the content in the buffer registers (TRDGRD0, TRDGRC1, and TRDGRD1) is transferred to the general registers (TRDGRB0, TRDGRA1, and TRDGRB1). During FFFFh, 0, 1 operation, data are not transferred to registers such as the TRDGRB0 register. Also, at this time, the OVF bit remains unchanged.

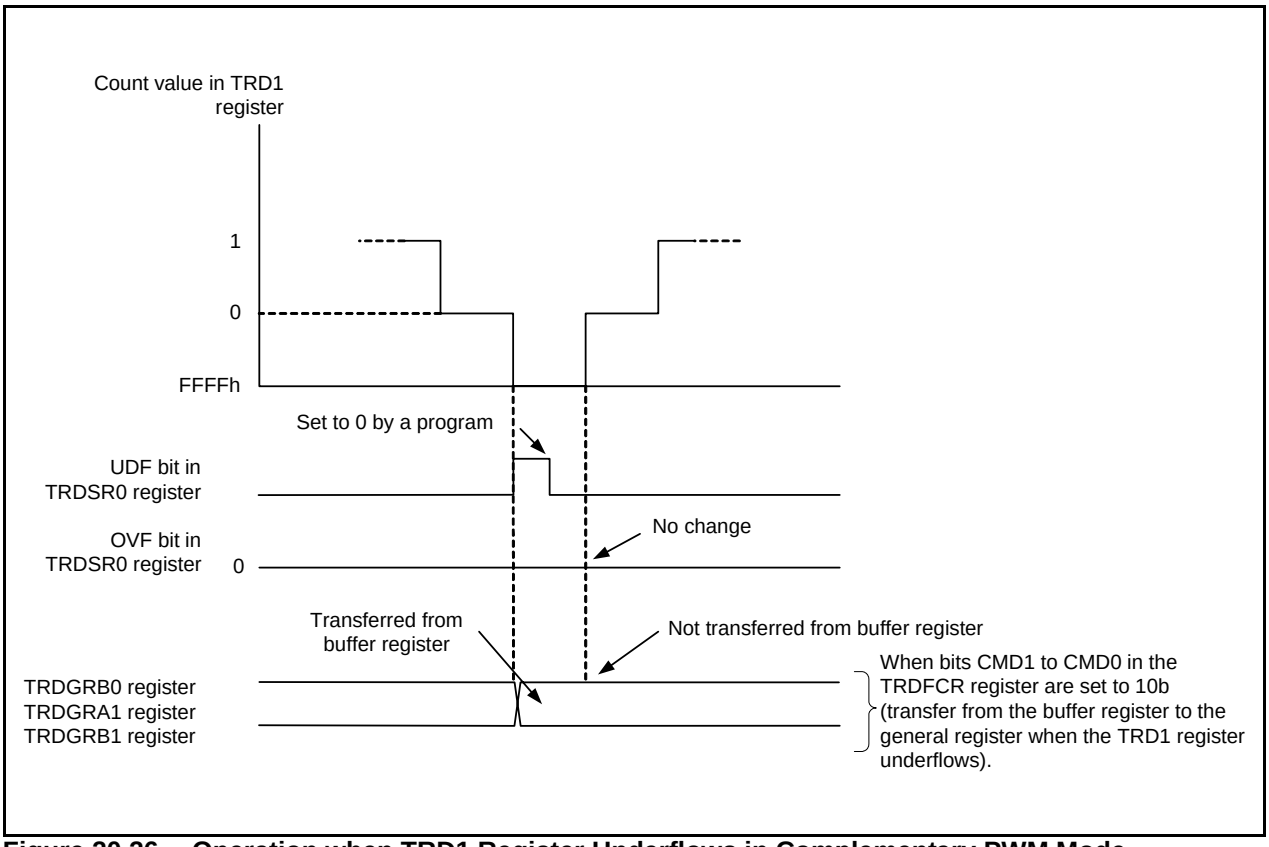


Figure 20.26 Operation when TRD1 Register Underflows in Complementary PWM Mode

- Select with bits CMD1 to CMD0 the timing of data transfer from the buffer register to the general register. However, transfer takes place with the following timing in spite of the value of bits CMD1 to CMD0 in the following cases:

  Value in buffer register ≥ value in TRDGRA0 register:
  Transfer take place at underflow of the TRD1 register.
  After this, when the buffer register is set to 0001h or above and a smaller value than the value of the TRDGRA0 register, and the TRD1 register underflows for the first time after setting, the value is transferred to the general register. After that, the value is transferred with the timing selected by bits CMD1 to CMD0.

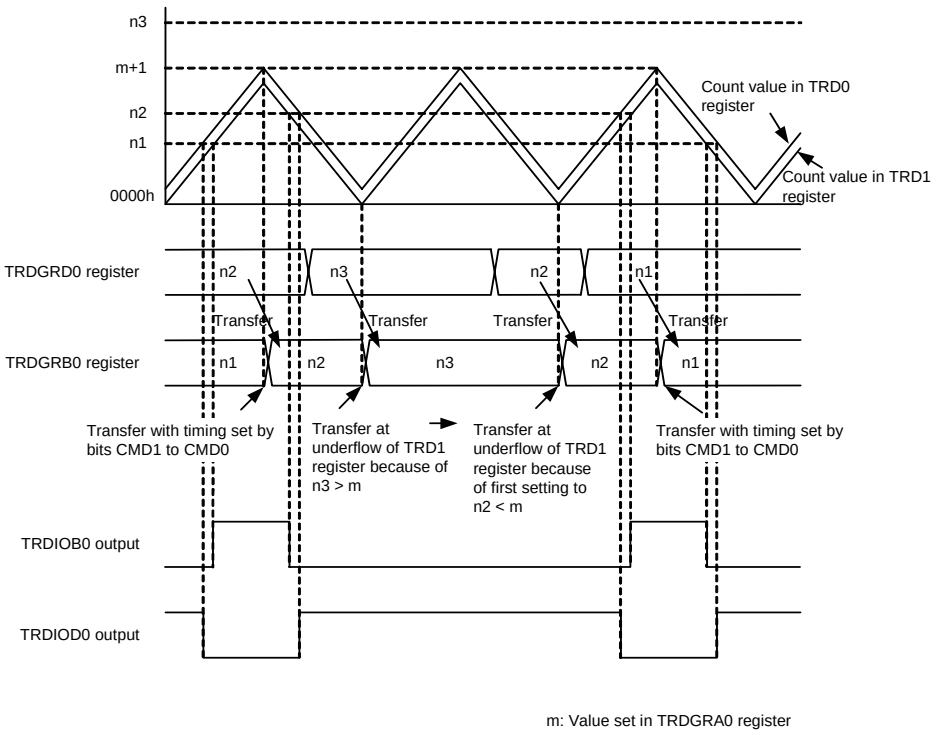
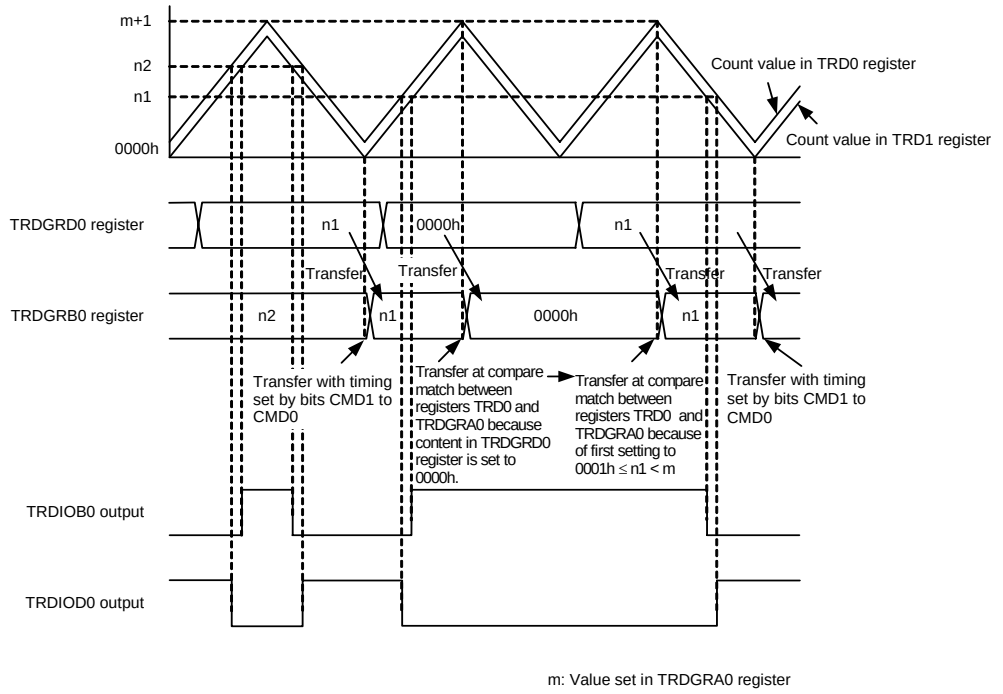


Figure 20.27 Operation when Value in Buffer Register ≥ Value in TRDGRA0 Register in Complementary PWM Mode

When the value in the buffer register is set to 0000h:
Transfer takes place at compare match between registers TRD0 and TRDGRA0.
After this, when the buffer register is set to 0001h or above and a smaller value than the value of the TRDGRA0 register, and a compare match occurs between registers TRD0 and TRDGRA0 for the first time after setting, the value is transferred to the general register. After that, the value is transferred with the timing selected by bits CMD1 to CMD0.



The above applies under the following conditions:
- Bits CMD1 to CMD0 in the TRDFCR register are set to 10b (data in the buffer register is transferred at underflow of the TRD1 register in PWM mode).
- Both the OLS0 and OLS1 bits in the TRDFCR register are set to 1 (active “H” for normal-phase and counter-phase).

Figure 20.28 Operation when Value in Buffer Register Is Set to 0000h in Complementary PWM Mode

21. Timer RE

Timer RE has an 8-bit counter with a 4-bit prescaler.

21.1 Overview

Timer RE have the following mode:

- Output compare mode Count a count source and detect compare matches.

The count source for timer RE is the operating clock that regulates the timing of timer operations.
Table 21.1 lists the Pin Configuration of Timer RE.

Table 21.1 Pin Configuration of Timer RE

Pin Name	Assigned Pin	I/O	Function
TREO	P0_4 or P6_0	Output	• Output f2, f4, or f8 • Compare output

21.2 Output Compare Mode

In output compare mode, the internal count source divided by 2 is counted using the 4-bit or 8-bit counter and compare value match is detected with the 8-bit counter. Figure 21.1 shows a Block Diagram of Output Compare Mode and Table 21.2 lists the Output Compare Mode Specifications. Figure 21.2 shows the Operating Example in Output Compare Mode.

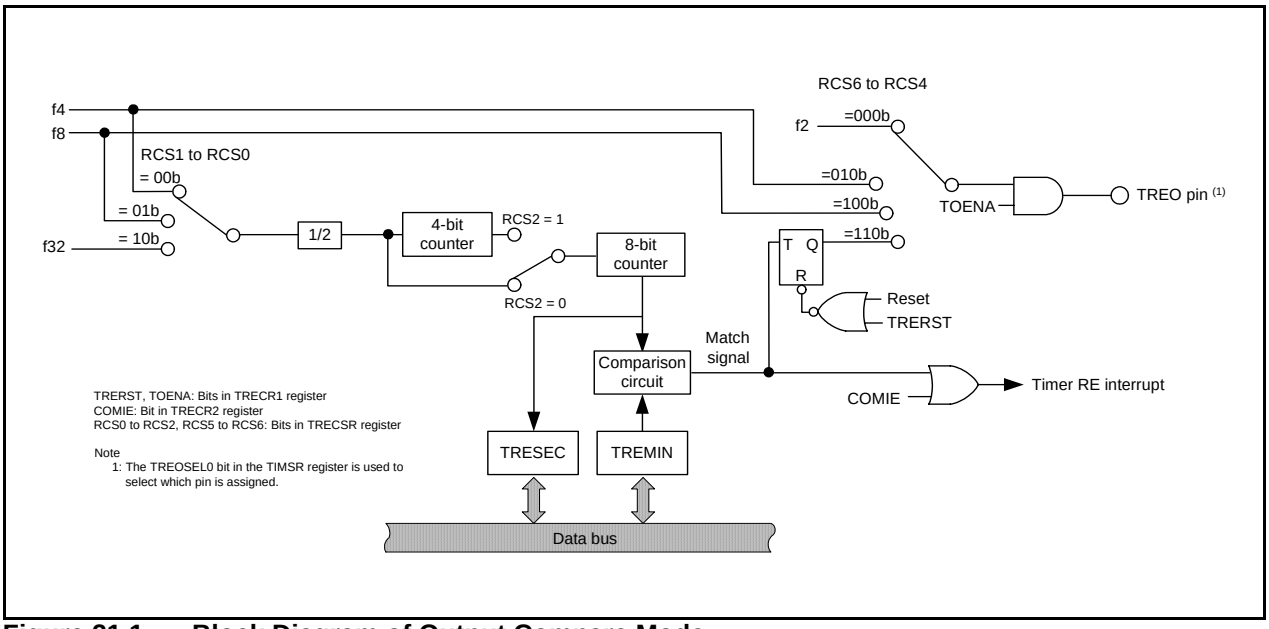


Figure 21.1 Block Diagram of Output Compare Mode

Table 21.2 Output Compare Mode Specifications

Item	Specification
Count sources	f4, f8, f32
Count operations	• Increment • When the 8-bit counter content matches with the TREMIN register content, the value returns to 00h and count continues. The count value is held while count stops.
Count period	• When RCS2 = 0 (4-bit counter is not used) 1/fi x 2 x (n+1) • When RCS2 = 1 (4-bit counter is used) 1/fi x 32 x (n+1) fi: Frequency of count source n: Setting value of TREMIN register
Count start condition	1 (count starts) is written to the TSTART bit in the TRECR1 register
Count stop condition	0 (count stops) is written to the TSTART bit in the TRECR1 register
Interrupt request generation timing	When the 8-bit counter content matches with the TREMIN register content
TREO pin function	Select any one of the following: • Programmable I/O ports • Output f2, f4, or f8 • Compare output
Read from timer	When reading the TRESEC register, the 8-bit counter value can be read. When reading the TREMIN register, the compare value can be read.
Write to timer	Writing to the TRESEC register is disabled. When bits TSTART and TCSTF in the TRECR1 register are set to 0 (timer stops), writing to the TREMIN register is enabled.
Selectable functions	• Select use of 4-bit counter • Compare output function Every time the 8-bit counter value matches the TREMIN register value, TREO output polarity is reversed. The TREO pin outputs “L” after reset is deasserted and the timer RE is reset by the TRERST bit in the TRECR1 register. Output level is held by setting the TSTART bit to 0 (count stops). • TREO pin select function P0_4 or P6_0 is selected by the TREOSEL0 bit in the TIMSR register.

21.2.1 Timer RE Counter Data Register (TRESEC)

Address 0118h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	R/W
b7 to b0	8-bit counter data can be read. Although Timer RE stops counting, the count value is held. The TRESEC register is set to 00h at the compare match.	R

21.2.2 Timer RE Compare Data Register (TREMIN)

Address 0119h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	R/W
b7 to b0	8-bit compare data is stored.	R/W

21.2.3 Timer RE Control Register 1 (TRECR1)

Address 011Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TSTART	—	—	TRERST	—	TOENA	TCSTF	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	TCSTF	Timer RE count status flag	0: Count stopped 1: Counting	R
b2	TOENA	TREO pin output enable bit	0: Disable clock output 1: Enable clock output	R/W
b3	—	Reserved bit	Set to 0.	R/W
b4	TRERST	Timer RE reset bit	When setting this bit to 0, after setting it to 1, the following will occur. • Registers TRESEC, TREMIN, and TRECR2 are set to 00h. • Bits TCSTF and TSTART in the TRECR1 register are set to 0. • The 8-bit counter is set to 00h and the 4-bit counter is set to 0h.	R/W
b5	—	Reserved bits	Set to 0.	R/W
b6	—			
b7	TSTART	Timer RE count start bit	0: Count stops 1: Count starts	R/W

21.2.4 Timer RE Control Register 2 (TRECR2)

Address 011Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	COMIE	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	—			
b4	—			
b5	COMIE	Compare match interrupt enable bit	0: Disable compare match interrupt 1: Enable compare match interrupt	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

21.2.5 Timer RE Count Source Select Register (TRECSR)

Address 011Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	RCS6	RCS5	RCS4	RCS3	RCS2	RCS1	RCS0
After Reset	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	RCS0	Count source select bit (1)	b1 b0 0 0: f4 0 1: f8 1 0: f32 1 1: Do not set.	R/W
b1	RCS1			R/W
b2	RCS2	4-bit counter select bit (1)	0: Not used 1: Used	R/W
b3	RCS3	Output compare mode enable bit (1)	0: Used 1: Not used	R/W
b4	RCS4	Clock output select bit (2)	b6 b5 b4 0 0 0: f2 0 1 0: f4 1 0 0: f8 1 1 0: Compare output Other than above: Do not set.	R/W
b5	RCS5			R/W
b6	RCS6			R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. Write to bits RCS0 to RCS3 when the TCSTF bit in the TRECR1 register is set to 0 (count stopped).
2. Write to bits RCS4 to RCS6 when the TOENA bit in the TRECR1 register is set to 0 (disable clock output).

21.2.6 Timer Pin Select Register (TIMSR)

Address 0186h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRGCLKBSEL	TRGCLKASEL	TRGIOBSEL	TRGIOASEL	—	TRFISEL0	—	TREOSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TREOSEL0	TREO pin select bit	0: P0_4 pin assigned 1: P6_0 pin assigned	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	TRFISEL0	TRFI pin select bit	0: TRFI pin not used 1: P8_3 pin assigned	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TRGIOASEL	TRGIOA pin select bit	0: TRGIOA pin not used 1: P5_6 pin assigned	R/W
b5	TRGIOBSEL	TRGIOB pin select bit	0: TRGIOB pin not used 1: P5_7 pin assigned	R/W
b6	TRGCLKASEL	TRGCLKA pin select bit	0: TRGCLKA pin not used 1: P3_0 pin assigned	R/W
b7	TRGCLKBSEL	TRGCLKB pin select bit	0: TRGCLKB pin not used 1: P3_2 pin assigned	R/W

The TIMSR register selects which pin is assigned as the timers RE, RF, and RG I/O. To use the I/O pin for timers RE, RF, and RG, set this register.
Set the TIMSR register before setting the registers associated with timers RE, RF, and RG. Also, do not change the setting value in this register during the operation of timers RE, RF, and RG.

21.2.7 Operating Example

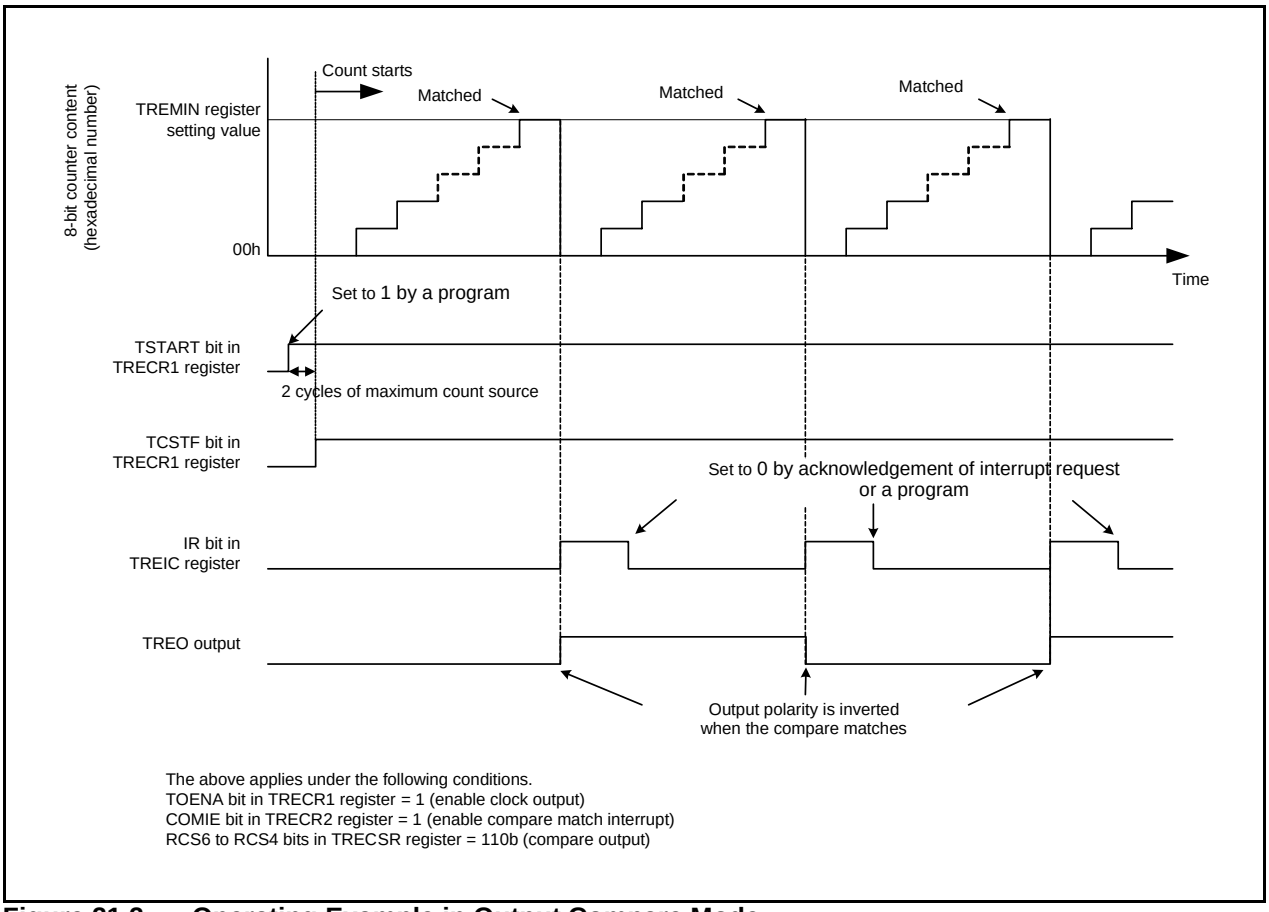


Figure 21.2 Operating Example in Output Compare Mode

21.3 Notes on Timer RE

21.3.1 Starting and Stopping Count

Timer RE has the TSTART bit for instructing the count to start or stop, and the TCSTF bit, which indicates count start or stop. Bits TSTART and TCSTF are in the TRECR1 register.
Timer RE starts counting and the TCSTF bit is set to 1 (count starts) when the TSTART bit is set to 1 (count starts). It takes up to 2 cycles of the count source until the TCSTF bit is set to 1 after setting the TSTART bit to 1. During this time, do not access registers associated with timer RE (1) other than the TCSTF bit.
Also, timer RE stops counting when setting the TSTART bit to 0 (count stops) and the TCSTF bit is set to 0 (count stops). It takes the time for up to 2 cycles of the count source until the TCSTF bit is set to 0 after setting the TSTART bit to 0. During this time, do not access registers associated with timer RE other than the TCSTF bit.

Note:
1. Registers associated with timer RE: TREMIN, TRECR1, TRECR2, and TRECSR.

21.3.2 Register Setting

Write to the following registers or bits when timer RE is stopped.
- Registers TRESEC, TREMIN, and TRECR2
- Bits RCS0 to RCS3 in TRECSR register

Timer RE is stopped when bits TSTART and TCSTF in the TRECR1 register are set to 0 (timer RE stopped).

Also, set all above-mentioned registers and bits (immediately before timer RE count starts) before setting the TRECR2 register.

22. Timer RF

Timer RF is a 16-bit timer.

22.1 Overview

The count source for timer RF is the operating clock that regulates the timing of timer operations. Figure 22.1 shows a Block Diagram of Timer RF. Table 22.1 shows the Pin Configuration of Timer RF. Figure 22.2 shows a Block Diagram of CMP Waveform Generation Unit. Figure 22.3 shows a Block Diagram of CMP Waveform Output Unit.

Timer RF has two modes.

- Input capture mode — Transfer the counter value to a register as a trigger of the external signal
- Output compare mode — Detect the register value match with a counter (Pin output can be changed at detection)

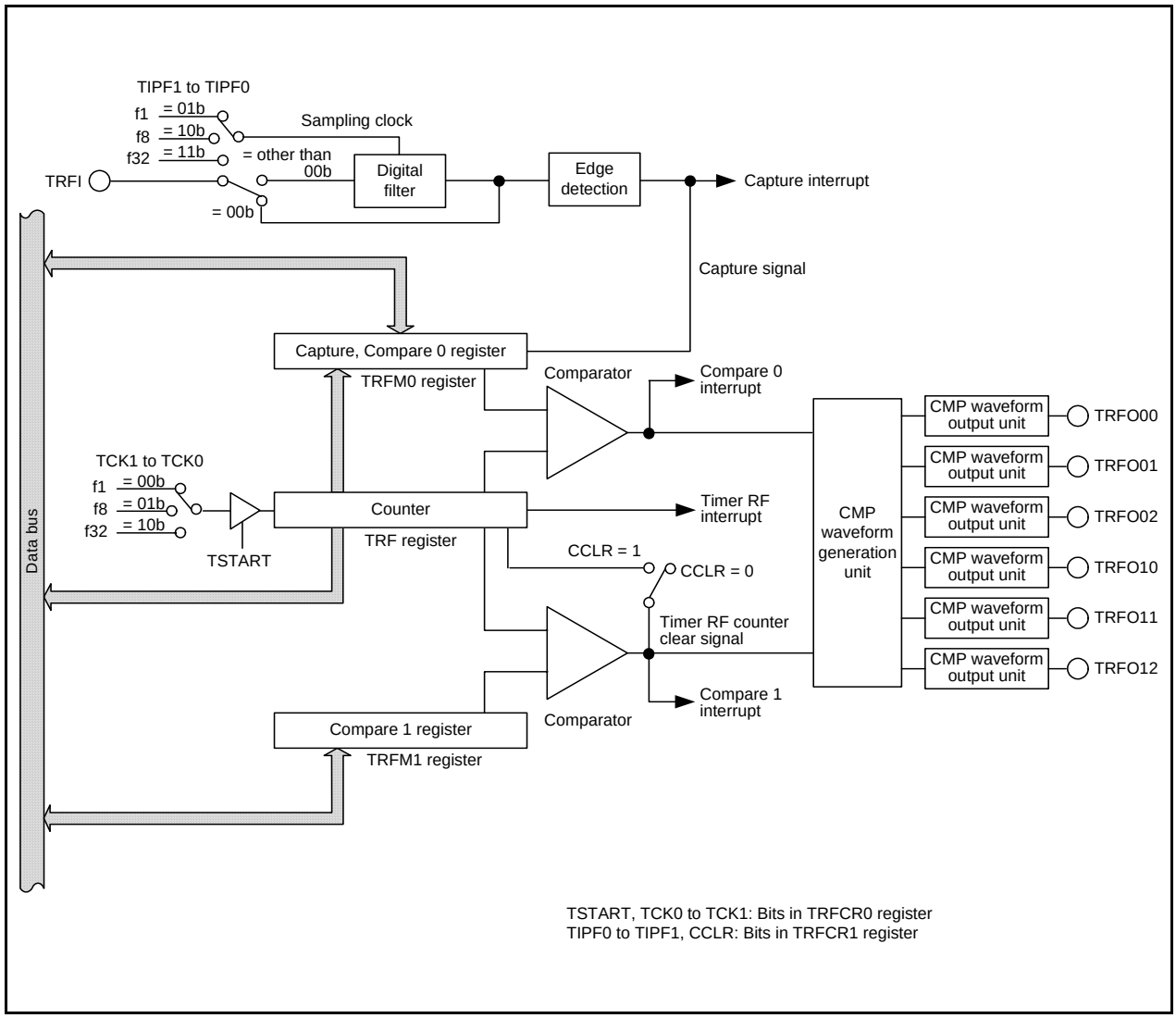


Figure 22.1 Block Diagram of Timer RF

Table 22.1 Pin Configuration of Timer RF

Pin Name	Assigned Pin	I/O	Function
TRFI	P8_3	Input	Measured pulse input (Input capture mode)
TRFO00	P8_0	Output	Output compare output (Output compare mode)
TRFO01	P8_1	Output	
TRFO02	P8_2	Output	
TRFO10	P8_3	Output	
TRFO11	P8_4	Output	
TRFO12	P8_5	Output	

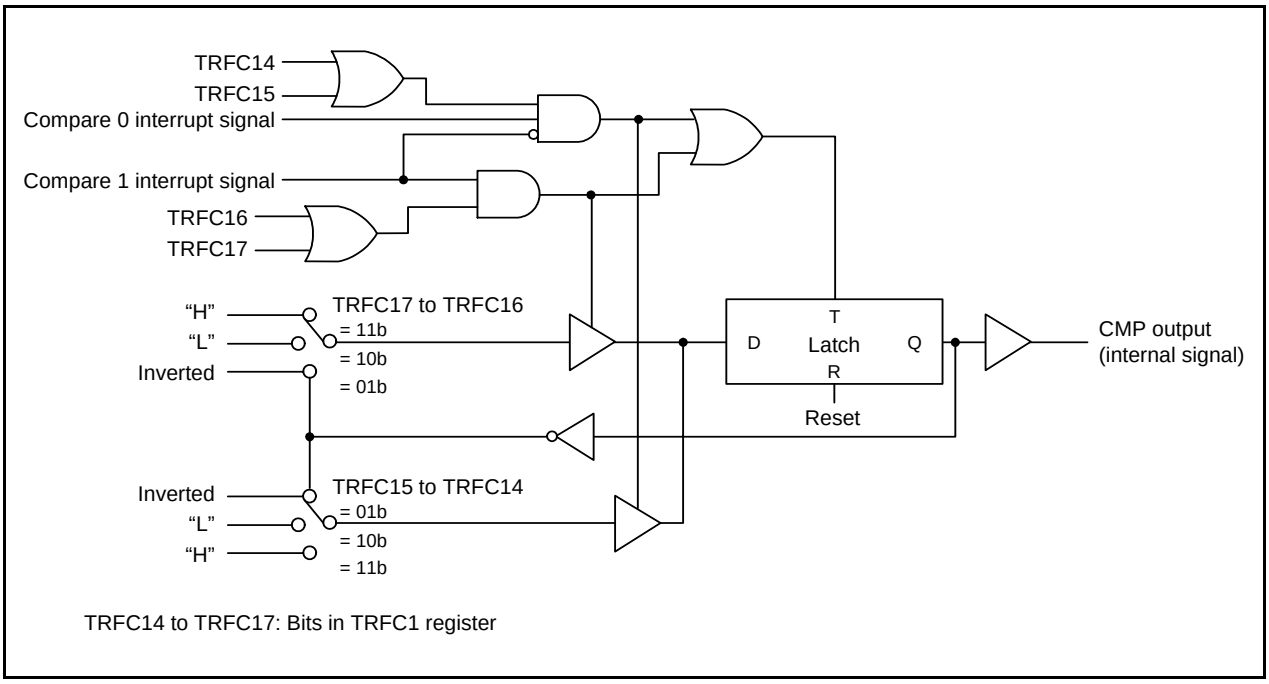


Figure 22.2 Block Diagram of CMP Waveform Generation Unit

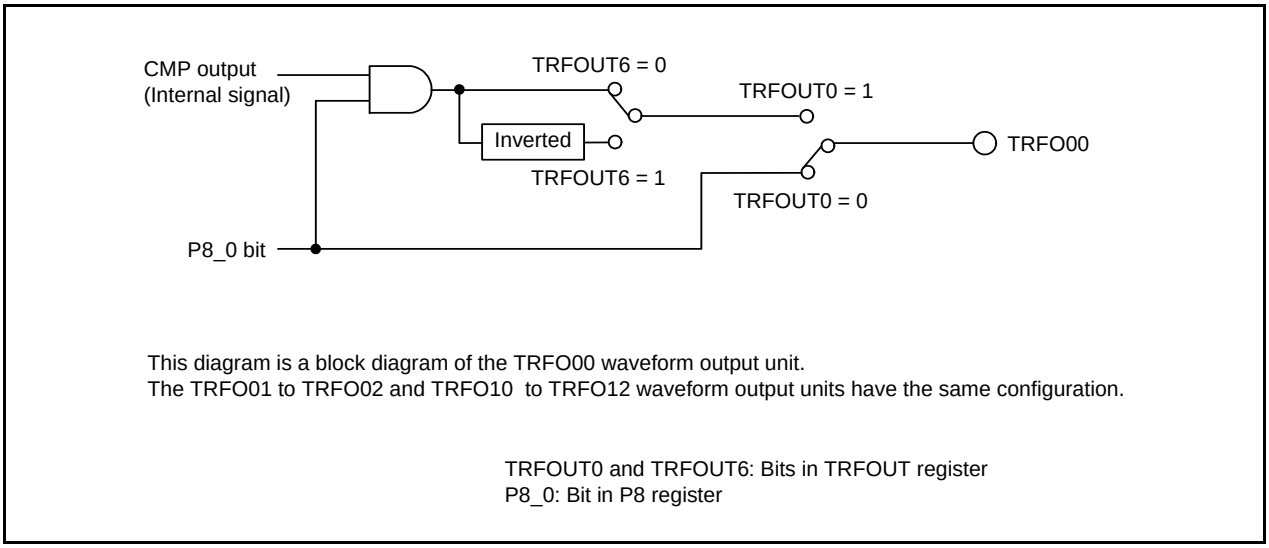


Figure 22.3 Block Diagram of CMP Waveform Output Unit

22.2 Registers

22.2.1 Timer RF Register (TRF)

Address 0091h to 0090h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	R/W
b15-b0	Count source increment. 0000h can be read when the TSTART bit is set to 0 (count stops). Count value can be read when the TSTART bit is set to 1 (count starts).	R

Access the TRF register in 16-bit units.

22.2.2 Capture and Compare 0 Register (TRFM0)

Address 009Dh to 009Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	—	—	—	—	—	—	
After Reset	0	0	0	0	0	0	0	0	(1)

Bit	b15	b14	b13	b12	b11	b10	b9	b8	
Symbol	—	—	—	—	—	—	—	—	
After Reset	0	0	0	0	0	0	0	0	(1)

Bit	Mode	Function	Setting Range	R/W
b15-b0	Input capture mode	When the active edge of the measured pulse is input, store the value in the TRF register	—	R
	Output compare mode (2)	Store the value compared with TRF register (counter)	0000h to FFFFh	R/W

Notes:
1. When the TMOD bit in the TRFCR1 register is set to 1, the value is set to FFFFh.
2. When setting a value in the TRFM0 register, set the TMOD bit in the TRFCR1 register to 1 (output compare mode). When the TMOD bit is set to 0 (input capture mode), no value can be written.

Access the TRFM0 register in 16-bit units.

22.2.3 Compare 1 Register (TRFM1)

Address 009Fh to 009Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Mode	Function	Setting Range	R/W
b15-b0	Output compare mode	Store the value compared with TRF register (counter)	0000h to FFFFh	R/W

Access the TRFM1 register in 16-bit units.

22.2.4 Timer RF Control Register 0 (TRFCR0)

Address 009Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	TRFC06	TRFC05	TRFC04	TRFC03	TCK1	TCK0	TSTART
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RF count start bit	0: Count stops 1: Count starts	R/W
b1	TCK0	Timer RF count source select bits (1)	b2 b1 0 0: f1 0 1: f8 1 0: f32 1 1: Do not set.	R/W
b2	TCK1			R/W
b3	TRFC03	Capture polarity select bits (1)	b4 b3 0 0: Rising edge 0 1: Falling edge 1 0: Both edges 1 1: Do not set.	R/W
b4	TRFC04			R/W
b5	TRFC05	CMP output select bit 0 when count stops	0: TRFC06 bit disabled Holds output level before count stops 1: TRFC06 bit enabled	R/W
b6	TRFC06	CMP output select bit 1 when count stops	0: “L” output when count stops 1: “H” output when count stops	R/W
b7	—	Reserved bit	Set to 0.	R/W

Note:
1. Rewrite this bit when the TSTART bit is set to 0 (count stops).

22.2.5 Timer RF Control Register 1 (TRFCR1)

Address 009Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRFC17	TRFC16	TRFC15	TRFC14	TMOD	CCLR	TIPF1	TIPF0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TIPF0	TRFI filter select bits (1)	b1 b0 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b1	TIPF1			R/W
b2	CCLR	TRF register count operation select bit (2, 3)	0: Free-running operation 1: Set TRF register to 0000h when compare 1 is matched.	R/W
b3	TMOD	Timer RF operation mode select bit (3)	0: Input capture mode (2, 4) 1: Output compare mode	R/W
b4	TRFC14	Compare 0 output select bits (2)	b5 b4 CMP output when compare 0 is matched 0 0: Unchanged 0 1: Inverted 1 0: “L” 1 1: “H”	R/W
b5	TRFC15			R/W
b6	TRFC16	Compare 1 output select bits (2)	b7 b6 CMP output when compare 1 is matched 0 0: Unchanged 0 1: Inverted 1 0: “L” 1 1: “H”	R/W
b7	TRFC17			R/W

Notes:
1. If filter enabled, when the same value from the TRFI pin is sampled three times continuously, the input is determined.
2. When the TMOD bit is set to 0 (input capture mode), set bits CCLR, and TRFC14 to TRFC17 to 0.
3. When the TSTART bit in the TRFCR0 register is set to 0 (count stops), rewrite bits CCLR and TMOD.
4. When the TMOD bit is set to 0 (input capture mode), set bits ILVL2 to ILVL0 in the CMP1IC register to 000b (level 0) and set the IR bit to 0 (no interrupt requested).

22.2.6 Timer RF Output Control Register (TRFOUT)

Address 0187h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRFOUT7	TRFOUT6	TRFOUT5	TRFOUT4	TRFOUT3	TRFOUT2	TRFOUT1	TRFOUT0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRFOUT0	TRFO00 output enable bit	0: Output disabled 1: Output enabled	R/W
b1	TRFOUT1	TRFO01 output enable bit		R/W
b2	TRFOUT2	TRFO02 output enable bit		R/W
b3	TRFOUT3	TRFO10 output enable bit		R/W
b4	TRFOUT4	TRFO11 output enable bit		R/W
b5	TRFOUT5	TRFO12 output enable bit		R/W
b6	TRFOUT6	TRFO00 to TRFO02 output invert bit	0: Output not inverted 1: Output inverted	R/W
b7	TRFOUT7	TRFO10 to TRFO12 output invert bit		R/W

22.2.7 Timer Pin Select Register (TIMSR)

Address 0186h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRGCLKBSEL	TRGCLKASEL	TRGIOBSEL	TRGIOASEL	—	TRFISEL0	—	TREOSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TREOSEL0	TREO pin select bit	0: P0_4 pin assigned 1: P6_0 pin assigned	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	TRFISEL0	TRFI pin select bit	0: TRFI pin not used 1: P8_3 pin assigned	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TRGIOASEL	TRGIOA pin select bit	0: TRGIOA pin not used 1: P5_6 pin assigned	R/W
b5	TRGIOBSEL	TRGIOB pin select bit	0: TRGIOB pin not used 1: P5_7 pin assigned	R/W
b6	TRGCLKASEL	TRGCLKA pin select bit	0: TRGCLKA pin not used 1: P3_0 pin assigned	R/W
b7	TRGCLKBSEL	TRGCLKB pin select bit	0: TRGCLKB pin not used 1: P3_2 pin assigned	R/W

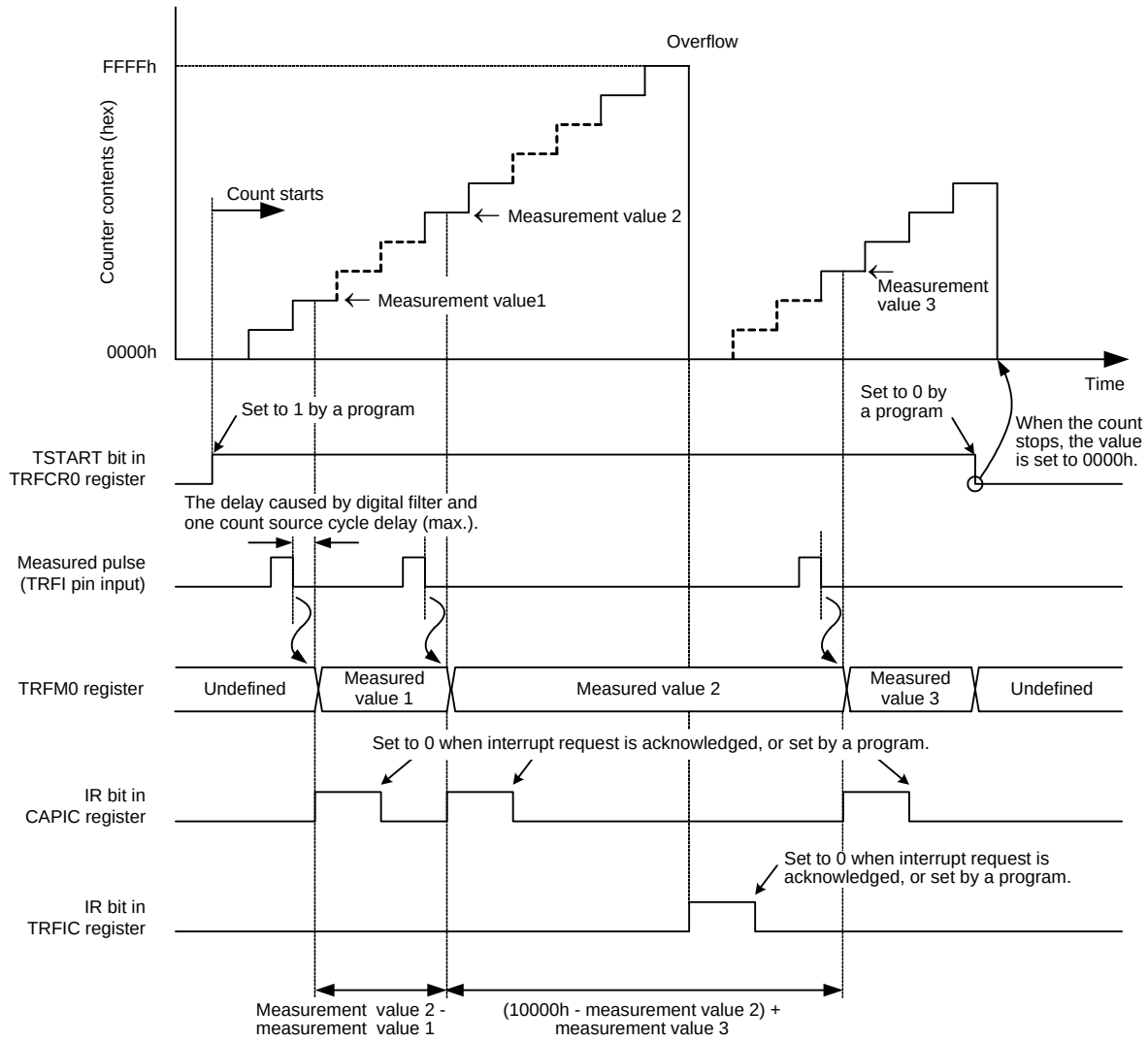
The TIMSR register selects which pin is assigned as the timers RE, RF, and RG I/O. To use the I/O pin for timers RE, RF, and RG, set this register.
Set the TIMSR register before setting the registers associated with timers RE, RF, and RG. Also, do not change the setting value in this register during the operation of timers RE, RF, and RG.

22.3 Input Capture Mode

In input capture mode, the edge of the TRFI pin input signal is used as a trigger to latch the timer value and the width or the period of external signal is measured. The TRFI input is equipped with a digital filter, and this prevents errors caused by noise or the like from occurring. Table 22.2 shows the Input Capture Mode Specifications. Figure 22.4 shows an Operating Example in Input Capture Mode.

Table 22.2 Input Capture Mode Specifications

Item	Specification
Count sources	f1, f8, f32
Count operations	• Increment • Transfer the value in the TRF register to the TRFM0 register at the valid edge of the measured pulse.
Count period	1/fk × 65536 fk: Frequency of count source
Count start condition	The TSTART bit in the TRFCR0 register is set to 1 (count starts).
Count stop condition	The TSTART bit in the TRFCR0 register is set to 0 (count stops).
Interrupt request generation timing	• The valid edge of TRFI input [capture interrupt] • When timer RF overflows [timer RF interrupt]
TRFI pin function	Measured pulse input
TRFO00 to TRFO02, TRFO11 to TRFO12 pin functions	Programmable I/O port
Counter value reset timing	In the following cases, the value in the TRF register is set to 0000h. • When the TSTART bit in the TRFCR0 register is set to 0 (count stops).
Read from timer	• The count value can be read out by reading the TRF register. • The count value at the measured pulse valid edge input can be read out by reading the TRFM0 register.
Write to timer	Write to the TRF and TRFM0 registers is disabled.
Select functions	• TRFI polarity selected Selects the valid edge of the measured pulse. (Bits TRFC03 to TRFC04 in the TRFCR0 register.) • Digital filter function The TRFI input is sampled, and when the sampled input level matches as three times, the level is determined. Selects the sampling clock of the digital filter. (Bits TIPF0 to TIPF1 in the TRFCR1 register.)



The above applies under the following conditions.

Bits TRFC04 to TRFC03 in TRFCR0 register = 01b (Capture input polarity is set for falling edge.)

Figure 22.4 Operating Example in Input Capture Mode

22.3.1 Digital Filter

The TRFI input is sampled, and when the sampled input level matches three times, its level is determined. Select the digital filter function and sampling clock by the TRFCR1 register.

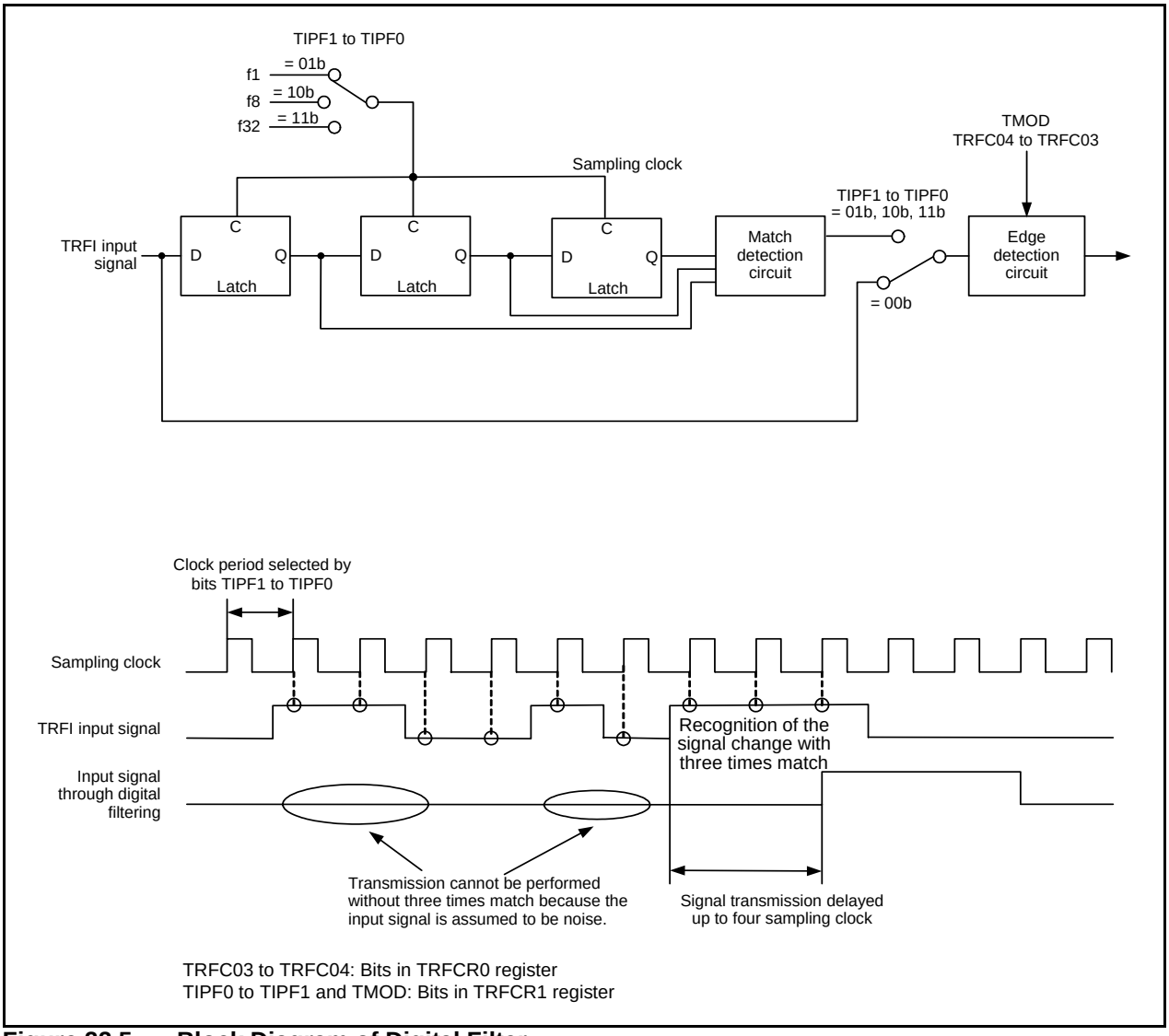


Figure 22.5 Block Diagram of Digital Filter

22.4 Output Compare Mode

In output compare mode, when the value of the TRF register matches the value of the TRFM0 (compare 0 match) or TRFM1 (compare 1 match) register, a user-set level is output mode from the output-compare output pin.
Table 22.3 shows the Output Compare Mode Specifications. Table 22.4 shows the Output in Output Compare Mode (Example of TRFO00 Pin). Figure 22.6 shows an Operating Example in Output Compare Mode. Figure 22.7 shows the Operating Example in Output Compare Mode ("L" and "H" Held Output in Count Stops).

Table 22.3 Output Compare Mode Specifications

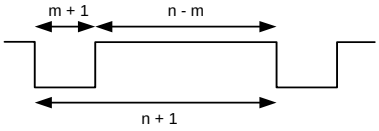
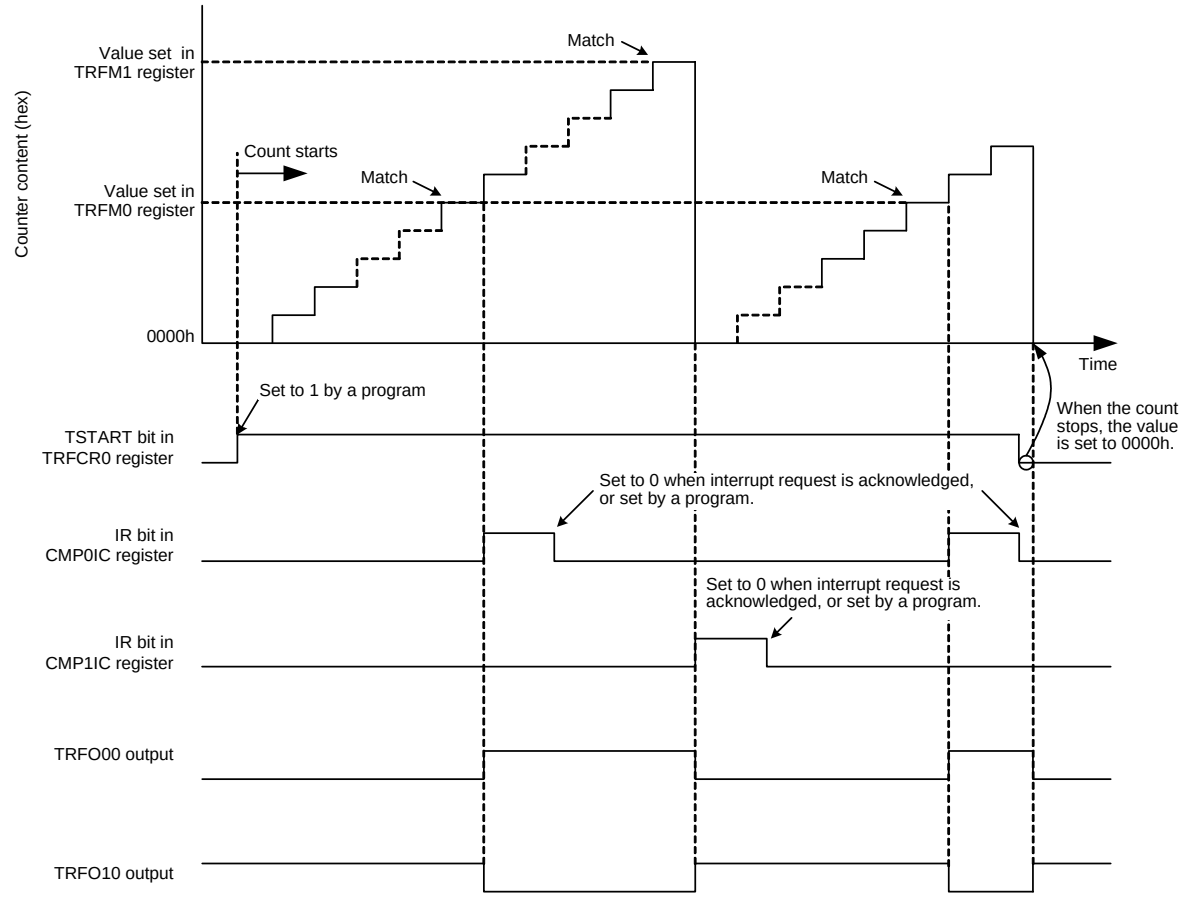
Item	Specification
Count sources	f1, f8, f32
Count operations	Increment
PWM waveform	PWM period: 1/fk × (n + 1) "L" level width: 1/fk × (m + 1) "H" level width: 1/fk × (n - m) fk: Frequency of count source m: Value set in the TRFM0 register n: Value set in the TRFM1 register  It applies under the following conditions. • CMP output "H" when compare 0 is matched • CMP output "L" when compare 1 is matched • CMP output not inverted
Count start condition	The TSTART bit in the TRFCR0 register is set to 1 (count starts).
Count stop condition	The TSTART bit in the TRFCR0 register is set to 0 (count stops).
Interrupt request generation timing	• When compare 0 match is generated [compare 0 interrupt] • When compare 1 match is generated [compare 1 interrupt] • When time RF overflows [timer RF interrupt].
TRFO00 to TRFO12 pins function	Programmable I/O port or output-compare output
Counter value reset timing	In the following cases, the value in the TRF register is set to 0000h. • When the TSTART bit in the TRFCR0 register is set to 0 (count stops). • The CCLR bit in the TRFCR1 register is set to 1 (the TRF register is set to 0000h at compare 1 match) in the compare 1 matches.
Read from timer	• The count value can be read out by reading the TRF register. • The value in the compare register can be read out by reading registers TRFM0 and TRFM1.
Write to timer	Write to the TRF register is disabled
Select functions	• Output-compare output pin selected Either 1 pin or multiple pins among TRFO00 to TRFO02, or TRFO10 to TRFO12 (bits TRFOUT0 to TRFOUT5 in the TRFOUT register). • Output level at the compare match Selects "H", "L", inverted, or unchanged (bits TRFC14 to TRFC17 in the TRFCR1 register). • Output level inverted Selects output level inverted or not inverted (bits TRFOUT6 to TRFOUT7 in the TRFOUT register). • Output level at the count stops Selects "H", "L", or unchanged (bits TRFC05 to TRFC06 in the TRFCR0 register). • Timing to set the TRF register to 0000h Overflow or compare 1 match in the TRFM1 register (the CCLR bit in the TRFCR1 register).

Table 22.4 Output in Output Compare Mode (Example of TRFO00 Pin)

TRFO00 Output		Bit Setting Value					
		TRFCR0 Register			TRFOUT Register		P8 Register
		TRFC06	TRFC05	TSTART	TRFOUT6	TRFOUT0	P8_0
Counting	CMP output	X	X	1	0	1	1
	Inverted output of CMP output	X	X	1	1	1	1
	“L” output	X	X	1	0	1	0
	“H” output	X	X	1	1	1	0
Count stops	Holds output level before count stops	X	0	0	X	1	1
	“L” output	0	1	0	X	1	1
	“H” output	1	1	0	X	1	1

X: 0 or 1



The above applies under the following conditions.

TRFC05 bit in TRFCR0 register = 1, TRFC06 bit in TRFCR0 register = 0 (“L” output when count stops)
CCLR bit in TRFCR1 register = 1 (TRF register is set to 0000h at compare 1 match occurrence)
TMOD bit in TRFCR1 register = 1 (output compare mode)
Bits TRFC15 to TRFC14 in TRFCR1 register = 11b (CMP output level is set to “H” at compare 0 match)
Bits TRFC17 to TRFC16 in TRFCR1 register = 10b (CMP output level is set to “L” at compare 1 match)
TRFOUT6 bit in TRFOUT register = 0 (not inverted)
TRFOUT7 bit in TRFOUT register = 1 (inverted)
TRFOUT0 bit in TRFOUT register = 1 (TRFO00 output enabled)
TRFOUT3 bit in TRFOUT register = 1 (TRFO10 output enabled)
P8_0 bit in P8 register = 1 (“H”)
P8_3 bit in P8 register = 1 (“H”)

Figure 22.6 Operating Example in Output Compare Mode

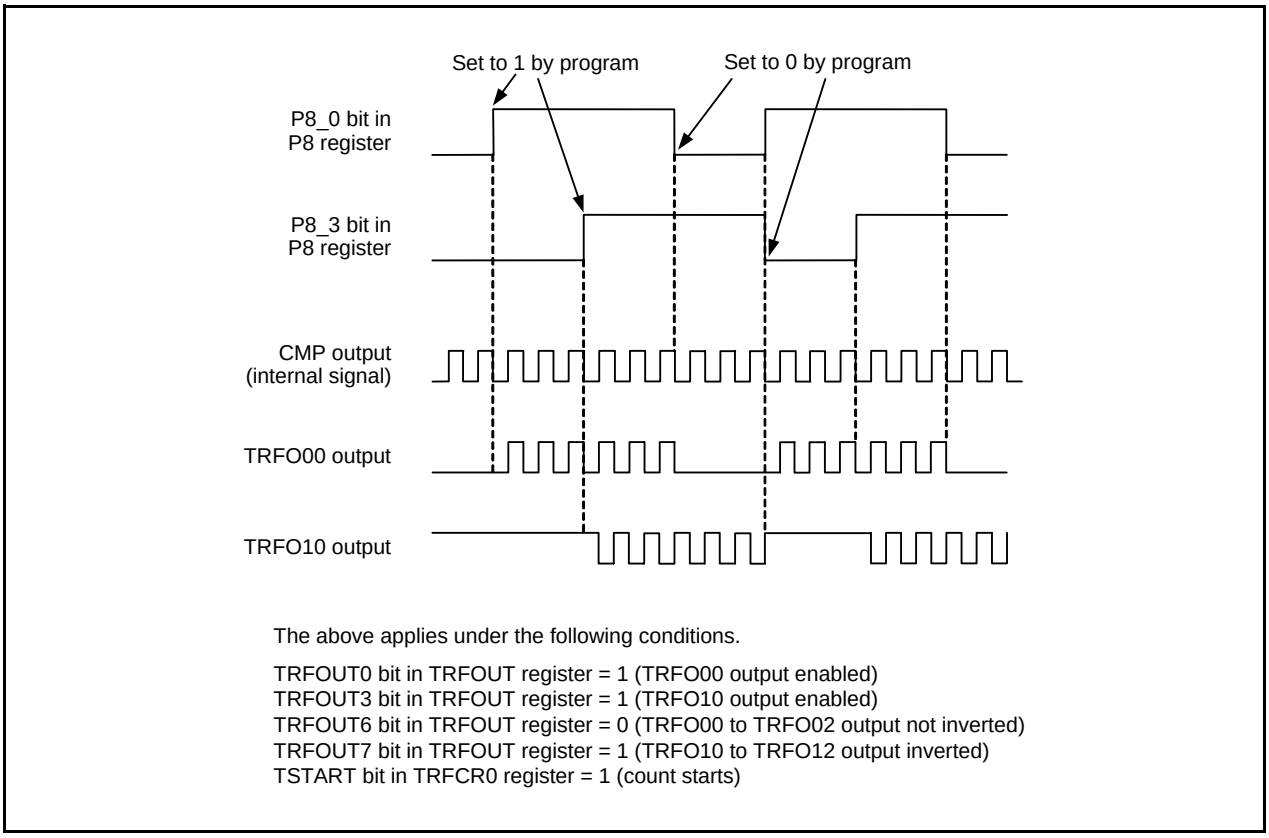


Figure 22.7 Operating Example in Output Compare Mode (“L” and “H” Held Output in Count Stops)

In output compare mode, the same PWM waveform is output from all of pins TRFO00 to TRFO02 and TRFO10 to TRFO12 during count operation. Note that the output waveform can be inverted for pins TRFO00 to TRFO02 or for pins TRFO10 to TRFO12. The output can also be fixed at “L” or “H” for individual pins for a given period.
The behavior when count operation stops can be selected from the following two options: the output level before the count stops is maintained, or output is fixed at “L” or “H”.

The values in the compare i register can be read by reading the TRFMi (i = 0 or 1) register. Writing to the TRFMi register causes the values to be stored in the compare i register in the following timing:
- If the TSTART bit is set to 0 (count stops)
  Values are stored simultaneously with the write to the TRFMi register.
- If the TSTART bit is set to 1 (count starts) and the CCLR bit in the TRFCR1 register is set to 0 (free running)
  Values are stored when the TRF register (counter) overflows.
- If the TSTART bit is set to 1 and the CCLR bit is set to 1 (TRF register set to 0000h at compare 1 match)
  Values are stored when the compare 1 and TRF register (counter) values match.

22.5 Notes on Timer RF

- Access registers TRF, TRFM0, and TRFM1 in 16-bit units.

Example of reading timer RF:

```
MOV.W    0090H,R0    ; Read out timer RF
```

- In input capture mode, a capture interrupt request is generated by inputting an edge selected by bits TRFC03 and TRFC04 in the TRFCR0 register even when the TSTART bit in the TRFCR0 register is set to 0 (count stops).

23. Timer RG

Timer RG is a 16-bit timer with two I/O pins.

23.1 Overview

Timer RG uses either f1 or fOCO40M as its operating clock. Table 23.1 lists the Timer RG Operating Clocks.

Table 23.1 Timer RG Operating Clocks

Condition	Timer RG Operating Clock
The count source is f1, f2, f4, f8, f32, TRGCLKA input, or TRGCLKB input. (Bits TCK2 toTCK0 in the TRGCR register are set to 000b to 101b, and 111b.)	f1
The count source is fOCO40M. (Bits TCK2 toTCK0 in the TRGCR register are set to 110b.)	fOCO40M

Figure 23.1 shows the Timer RG Block Diagram and Table 23.2 lists the Timer RG Pin Configuration.

Timer RG supports the following three modes:

- Timer mode
  - Input capture function: Count at the rising edge, falling edge, or both rising/falling edges
  - Output compare function: Low-level output/high-level output/toggle output

- PWM mode: PWM output available with any duty
- Phase counting mode: Automatic measurement available for the counts of the two-phase encoder

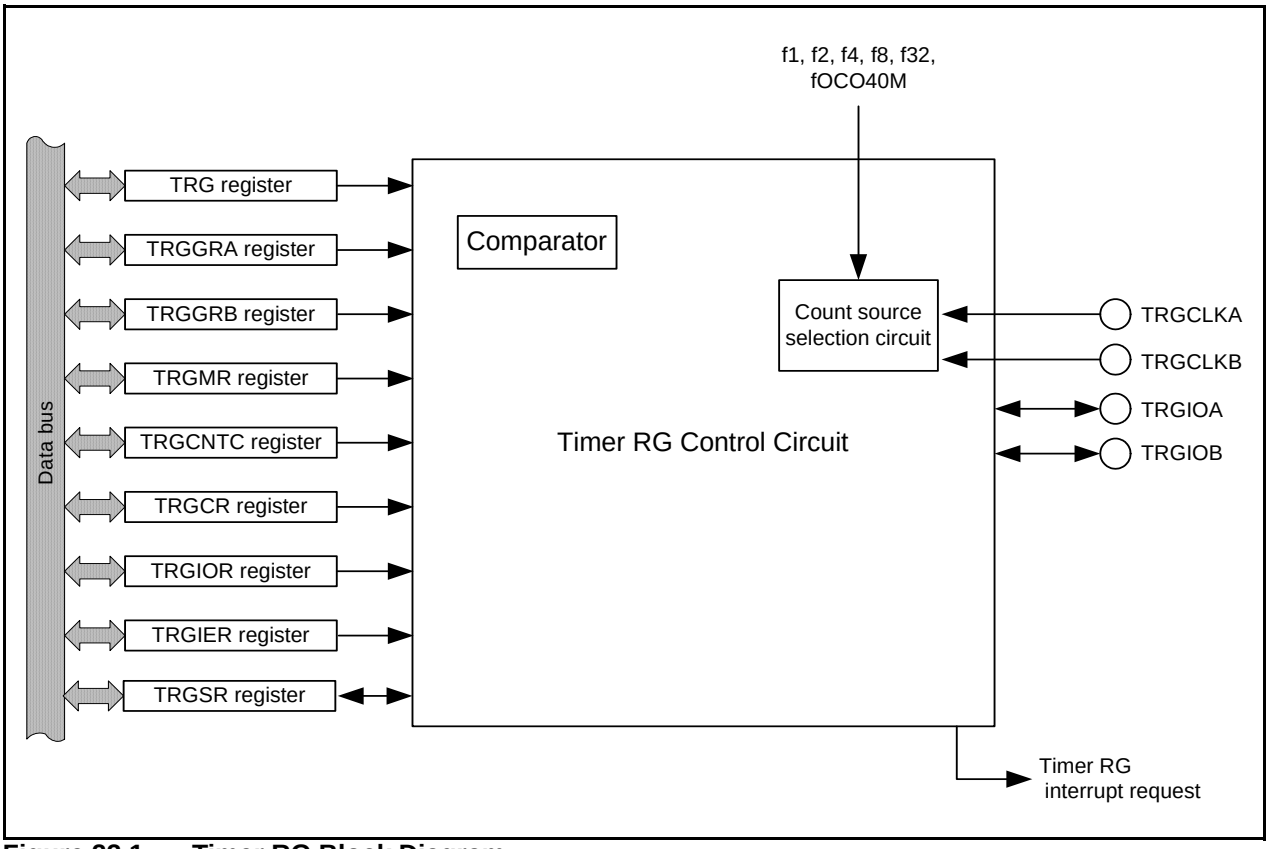


Figure 23.1 Timer RG Block Diagram

Table 23.2 Timer RG Pin Configuration

Pin Name	Assigned Pin	I/O	Function
TRGCLKA	P3_0	Input	• In phase counting mode A-phase input • In other than phase counting mode External clock A input
TRGCLKB	P3_2	Input	• In phase counting mode B-phase input • In other than phase counting mode External clock B input
TRGIOA	P5_6	I/O	• In timer mode (output compare function) TRGGRA output-compare output • In timer mode (input capture function) TRGGRA input-capture input • In PWM mode PWM output
TRGIOB	P5_7	I/O	• In timer mode (output compare function) TRGGRB output-compare output • In timer mode (input capture function) TRGGRB input-capture input

23.2 Registers

23.2.1 Timer RG Mode Register (TRGMR)

Address 0170h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TSTART	—	DFCK1	DFCK0	DFB	DFA	MDF	PWM
After Reset	0	1	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PWM	PWM mode select bit	0: Timer Mode 1: PWM mode	R/W
b1	MDF	Phase counting mode select bit	0: Increment 1: Phase counting mode	R/W
b2	DFA	Digital filer function select bit for TRGIOA pin	0: Digital filter function not used 1: Digital filter function used	R/W
b3	DFB	Digital filer function select bit for TRGIOB pin	0: Digital filter function not used 1: Digital filter function used	R/W
b4	DFCK0	Digital filter function clock select bit	b5 b4 0 0: f32 0 1: f8 1 0: f1 1 1: Clock selected by bits TCK0 to TCK2 in TRGCR register	R/W
b5	DFCK1			R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b7	TSTART	TRG count start bit	0: Count stops 1: Count starts	R/W

MDF Bit (Phase Counting Mode Select Bit)

When the MDF bit is set to 0, the counter counts the count source set by bits TCK0 to TCK2 in the TRGCR register.

When the MDF bit is set to 1, the counter counts the phase of input signals from the TRGCLKj pin (j = A or B) as listed in **Table 23.12 Increment/Decrement Conditions for TRG Register**.

23.2.2 Timer RG Count Control Register (TRGCNTC)

Address 0171h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CNTEN7	CNTEN6	CNTEN5	CNTEN4	CNTEN3	CNTEN2	CNTEN1	CNTEN0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CNTEN0	Counter enable bit 0	0: Disabled 1: Decrement When TRGCLKA input is high and at the rising edge of TRGCLKB input	R/W
b1	CNTEN1	Counter enable bit 1	0: Disabled 1: Decrement When TRGCLKB input is low and at the rising edge of TRGCLKA input	R/W
b2	CNTEN2	Counter enable bit 2	0: Disabled 1: Decrement When TRGCLKA input is low and at the falling edge of TRGCLKB input	R/W
b3	CNTEN3	Counter enable bit 3	0: Disabled 1: Decrement When TRGCLKB input is high and at the falling edge of TRGCLKA input	R/W
b4	CNTEN4	Counter enable bit 4	0: Disabled 1: Increment When TRGCLKB input is low and at the falling edge of TRGCLKA input	R/W
b5	CNTEN5	Counter enable bit 5	0: Disabled 1: Increment When TRGCLKA input is high and at the falling edge of TRGCLKB input	R/W
b6	CNTEN6	Counter enable bit 6	0: Disabled 1: Increment When TRGCLKB input is high and at the rising edge of TRGCLKA input	R/W
b7	CNTEN7	Counter enable bit 7	0: Disabled 1: Increment When TRGCLKA input is low and at the rising edge of TRGCLKB input	R/W

The TRGCNTC register is used in phase counting mode. This register sets its count conditions.

23.2.3 Timer RG Control Register (TRGCR)

Address 0172h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	CCLR1	CCLR0	CKEG1	CKEG0	TCK2	TCK1	TCK0
After Reset	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TCK0	Count source select bit (1)	b2 b1 b0 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRGCLKA input 1 1 0: fOCO40M 1 1 1: TRGCLKB input	R/W
b1	TCK1			R/W
b2	TCK2			R/W
b3	CKEG0	External clock active edge select bit (1)	b4 b3 0 0: Count at the rising edge 0 1: Count at the falling edge 1 0: Count at both the rising/falling edges 1 1: Do not set.	R/W
b4	CKEG1			R/W
b5	CCLR0	TRG register clear source select bit	b6 b5 0 0: Clear disabled 0 1: TRG register cleared by input capture or compare match with TRGGRA register 1 0: TRG register cleared by input capture or compare match with TRGGRB register 1 1: Do not set.	R/W
b6	CCLR1			R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Note:
1. In phase counting mode, the settings of bits TCK0 to TCK2 and bits CKEG0 and CKEG1 are disabled and the operation of phase counting mode has priority.

When writing to the TRG or TRGCR register, make sure the TSTART bit in the TRGMR register is 0 (count stops).

23.2.4 Timer RG Interrupt Enable Register (TRGIER)

Address 0173h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	OVIE	UDIE	IMIEB	IMIEA
After Reset	1	1	1	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input-capture/compare-match interrupt enable bit A	0: Interrupt by IMFA flag disabled 1: Interrupt by IMFA flag enabled	R/W
b1	IMIEB	Input-capture/compare-match interrupt enable bit B	0: Interrupt by IMFB flag disabled 1: Interrupt by IMFB flag enabled	R/W
b2	UDIE	Underflow interrupt enable bit	0: Interrupt by UDF flag disabled 1: Interrupt by UDF flag enabled	R/W
b3	OVIE	Overflow interrupt enable bit	0: Interrupt by OVF flag disabled 1: Interrupt by OVF flag enabled	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	—			

23.2.5 Timer RG Status Register (TRGSR)

Address 0174h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	DIRF	OVF	UDF	IMFB	IMFA
After Reset	1	1	1	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input-capture/compare-match flag A	[Condition for setting to 0] Write 0 after reading (1, 2)	R/W
b1	IMFB	Input-capture/compare-match flag B	[Condition for setting to 1] Refer to **Table 23.3 Conditions for Setting Bit of Each Flag to 1**.	R/W
b2	UDF	Underflow flag		R/W
b3	OVF	Overflow flag		R/W
b4	DIRF	Count direction flag	0: TRG register is decremented 1: TRG register is incremented	R
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b6	—			
b7	—			

Notes:
1. The writing results are as follows:
   - This bit is set to 0 when the reading result is 1 and 0 is written to the same bit.
   - This bit remains unchanged even if the reading result is 0 and 0 is written to the same bit. (This bit remains 1 even if it is set to 1 from 0 after reading, and writing 0.)
   - This bit remains unchanged if 1 is written to it.
2. When setting bits IMFA, IMFB, UDF, and OVF in the TRGSR register to 0, use the MOV instruction to write 0 to only the specified bit and write 1 to the other bits. Then write 0Fh continuously after this writing. Disable interrupts and DTC activation before writing 0Fh.

Table 23.3 Conditions for Setting Bit of Each Flag to 1

Bit Symbol	Timer Mode		PWM Mode
	Input Capture Function	Output Compare Function	
IMFA	TRGIOA pin input edge (1)	When the values of registers TRG and TRGGRA match.	
IMFB	TRGIOB pin input edge (1)	When the values of registers TRG and TRGGRB match.	
UDF	When the TRG register underflows.		
OVF	When the TRG register overflows.		

Note:
1. Edge selected by bits IOj1 to IOj0 (j = A or B) in the TRGIOR register.

When reading the TRGSR register after writing to it, insert one or more NOP instructions between the instructions used for writing and reading.

23.2.6 Timer RG I/O Control Register (TRGIOR)

Address 0175h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BUFB	IOB2	IOB1	IOB0	BUFA	IOA2	IOA1	IOA0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRGGRA control bit	Function varies depending on the operating mode (function).	R/W
b1	IOA1			R/W
b2	IOA2	TRGGRA mode select bit	0: Output compare function (1) 1: Input capture function (2)	R/W
b3	BUFA	TRGGRC register function select bit	0: Not used as the buffer register of the TRGGRA register 1: Used as the buffer register of the TRGGRA register	R/W
b4	IOB0	TRGGRB control bit	Function varies depending on the operating mode (function).	R/W
b5	IOB1			R/W
b6	IOB2	TRGGRB mode select bit	0: Output compare function (3) 1: Input capture function (4)	R/W
b7	BUFB	TRGGRD register function select bit	0: Not used as the buffer register of the TRGGRB register 1: Used as the buffer register of the TRGGRB register	R/W

Notes:
1. When the IOA2 bit is set to 0 (output compare function), the TRGGRA register functions as a compare match register. After reset, the TRGIOA pin outputs a low-level signal until the first compare match occurs.
2. When the IOA2 bit is set to 1 (input capture function), the TRGGRA register functions as an input capture register.
3. When the IOB2 bit is set to 0 (output compare function), the TRGGRB register functions as a compare match register. After reset, the TRGIOB pin outputs a low-level signal the until the first compare match occurs.
4. When the IOB2 bit is set to 1 (input capture function), the TRGGRB register functions as an input capture register.

23.2.7 Timer RG Counter (TRG)

Address 0177h to 0176h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15 to b0	In phase counting mode, count operation is increment/decrement. In other modes, count operation is increment.	0000h to FFFFh	R/W

The TRG register is connected to the CPU via the internal 16-bit bus and should be always accessed in 16-bit units. This register operates incrementing/decrementing and can also operate free-running, period counting, or external event counting. It can be cleared to 0000h by the compare match with the corresponding TRGGRA or TRGGRB register, or the input capture to registers TRGGRA and TRGGRB (count clear function).
When the TRG register overflows (FFFFh → 0000h), the OVF flag in the TRGSR register is set to 1.
When the TRG register underflows (0000h → FFFFh), the UDF flag in the TRGSR register is set to 1.

23.2.8 Timer RG General Register A, B, C, D (TRGGRA, TRGGRB, TRGGRC, TRGGRD)

Address 0179h to 0178h (TRGGRA), 017Bh to 017Ah (TRGGRB),
017Dh to 017Ch (TRGGRC), 017Fh to 017Eh (TRGGRD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b15 to b0	Function varies depending on the operating mode (function).	R/W

Registers TRGGRA and TRGGRB are 16-bit readable/writable registers with both the output compare and input capture register functions. These functions can be switched by setting the TRGIOR register.

When registers TRGGRA and TRGGRB are used as output compare registers, the values of registers TRGGRA and TRGGRB and the value of the TRG register are always compared. When their values match (compare match), bits IMFA and IMFB in the TRGSR register are set to 1. Compare match output can be set by the TRGIOR register.

When registers TRGGRA and TRGGRB are used as input capture registers, the value of the TRG register is stored upon detecting externally input capture signals. Bits IMFA and IMFB in the TRGSR register are set to 1 at this time. The detection edge of input capture signals is selected by setting the TRGIOR register.

The TRGGRC register can also be used as the buffer register of the TRGGRA register and the TRGGRD register can be used as the buffer register of the TRGGRB register, respectively. These functions can be selected by setting bits BUFA and BUFB in the TRGIOR register.
For example, when the TRGGRA register is set as an output compare register and the TRGGRC register is set as the buffer register of the TRGGRA register, the value of the TRGGRC register is transferred to the TRGGRA register each time compare match A occurs.
When the TRGGRA register is set as an input capture register and the TRGGRC register is set as the buffer register of the TRGGRA register, the value of the TRG register is transferred to the TRGGRA register and the value of the TRGGRA register value is transferred to the TRGGRC register each time an input capture occurs.

Registers TRGGRA and TRGGRB are connected to the CPU via the internal 16-bit bus and should be accessed in 16-bit units. These registers are set as output compare registers (pin output disabled) at reset.

23.2.9 Timer Pin Select Register (TIMSR)

Address 0186h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRGCLKBSEL	TRGCLKASEL	TRGIOBSEL	TRGIOASEL	—	TRFISEL0	—	TREOSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TREOSEL0	TREO pin select bit	0: P0_4 pin assigned 1: P6_0 pin assigned	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	TRFISEL0	TRFI pin select bit	0: TRFI pin not used 1: P8_3 pin assigned	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TRGIOASEL	TRGIOA pin select bit	0: TRGIOA pin not used 1: P5_6 pin assigned	R/W
b5	TRGIOBSEL	TRGIOB pin select bit	0: TRGIOB pin not used 1: P5_7 pin assigned	R/W
b6	TRGCLKASEL	TRGCLKA pin select bit	0: TRGCLKA pin not used 1: P3_0 pin assigned	R/W
b7	TRGCLKBSEL	TRGCLKB pin select bit	0: TRGCLKB pin not used 1: P3_2 pin assigned	R/W

The TIMSR register selects which pin is assigned as the timers RE, RF, and RG I/O. To use the I/O pin for timers RE, RF, and RG, set this register.
Set the TIMSR register before setting the registers associated with timers RE, RF, and RG. Also, do not change the setting value in this register during the operation of timers RE, RF, and RG.

23.3 Common Items for Multiple Modes

23.3.1 Count Sources

Table 23.4 lists the Count Source Selection and Figure 23.2 shows the Count Source Block Diagram.
When phase counting mode is selected, the settings of bits TCK0 to TCK2 and bits CKEG0 and CKEG1 in the TRGCR register are disabled.

Table 23.4 Count Source Selection

Count Source	Selection Method
f1 f2, f4, f8, f32	The count source is selected by bits TCK0 to TCK2 in the TRGCR register.
fOCO40M	- The FRA00 bit in the FRA0 register is set to 1 (high-speed on-chip oscillator on). - Bits TCK2 to TCK0 in the TRGCR register are set to 110b (fOCO40M).
External signal input to TRGCLKA or TRGCLKB pin	- Bits TCK2 to TCK0 in the TRGCR register are set to 101b (TRGCLKA input) or 111b (TRGCLKB input). - The active edge is selected by bits CKEG0 and CKEG1 in the TRGCR register. - The corresponding bit in the direction register is set to 0 (input mode).

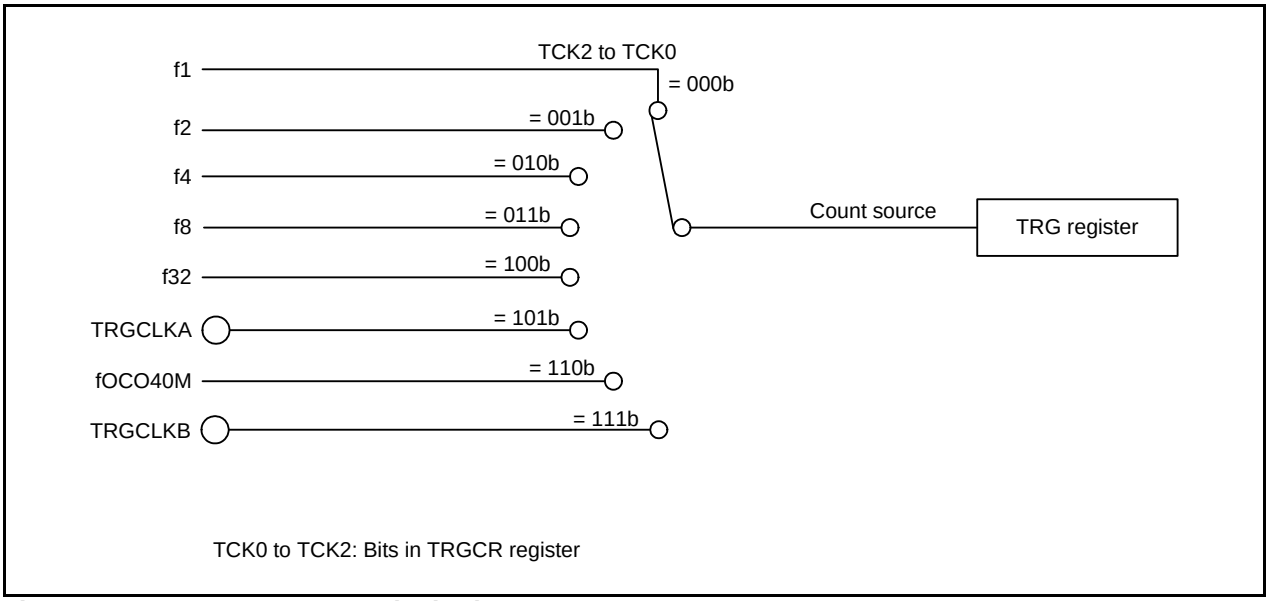


Figure 23.2 Count Source Block Diagram

The pulse width of an external clock input to the TRGCLKj pin (j =A or B) should be set to three cycles or more of the timer RG operating clock (see **Table 23.1 Timer RG Operating Clocks**).

23.3.2 Buffer Operation

The BUFA or BUFB bit in the TRGIOR register can be used to select the TRGGRC or TRGGRD register as the buffer register of the TRGGRA or TRGGRB register.

- Buffer register of TRGGRA register: TRGGRC register
- Buffer register of TRGGRB register: TRGGRD register

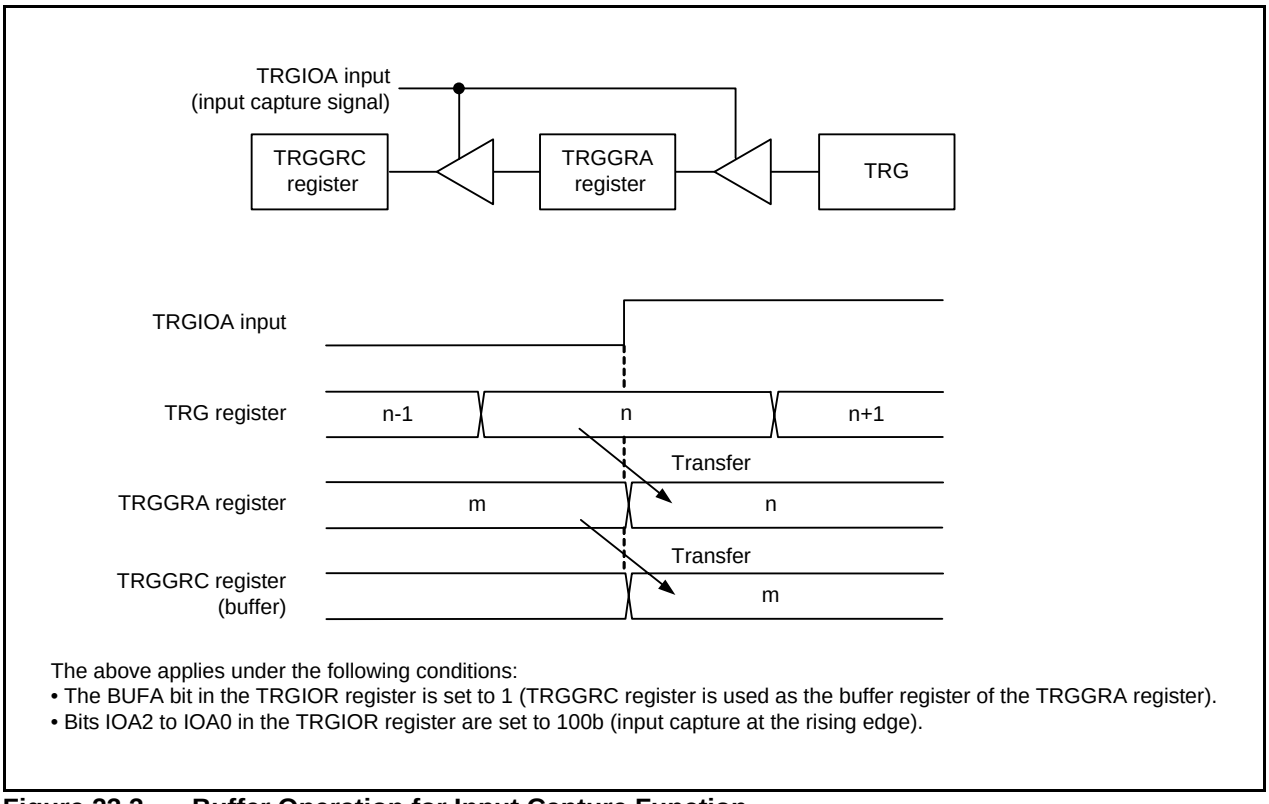
Buffer operation differs depending on the mode.

Table 23.5 lists the Buffer Operation in Each Mode.

Figure 23.3 shows the Buffer Operation for Input Capture Function and Figure 23.4 shows the Buffer Operation for Output Compare Function.

Table 23.5 Buffer Operation in Each Mode

Function, Mode	Transfer Timing	Transfer Destination Register
Input capture function	Input capture signal input	The content of the TRGGRA (TRGGRB) register is transferred to the buffer register.
Output compare function PWM mode	Compare match between the TRG register and the TRGGRA (TRGGRB) register	The content of the buffer register is transferred to the TRGGRA (TRGGRB) register.



The above applies under the following conditions:
- The BUFA bit in the TRGIOR register is set to 1 (TRGGRC register is used as the buffer register of the TRGGRA register).
- Bits IOA2 to IOA0 in the TRGIOR register are set to 100b (input capture at the rising edge).

Figure 23.3 Buffer Operation for Input Capture Function

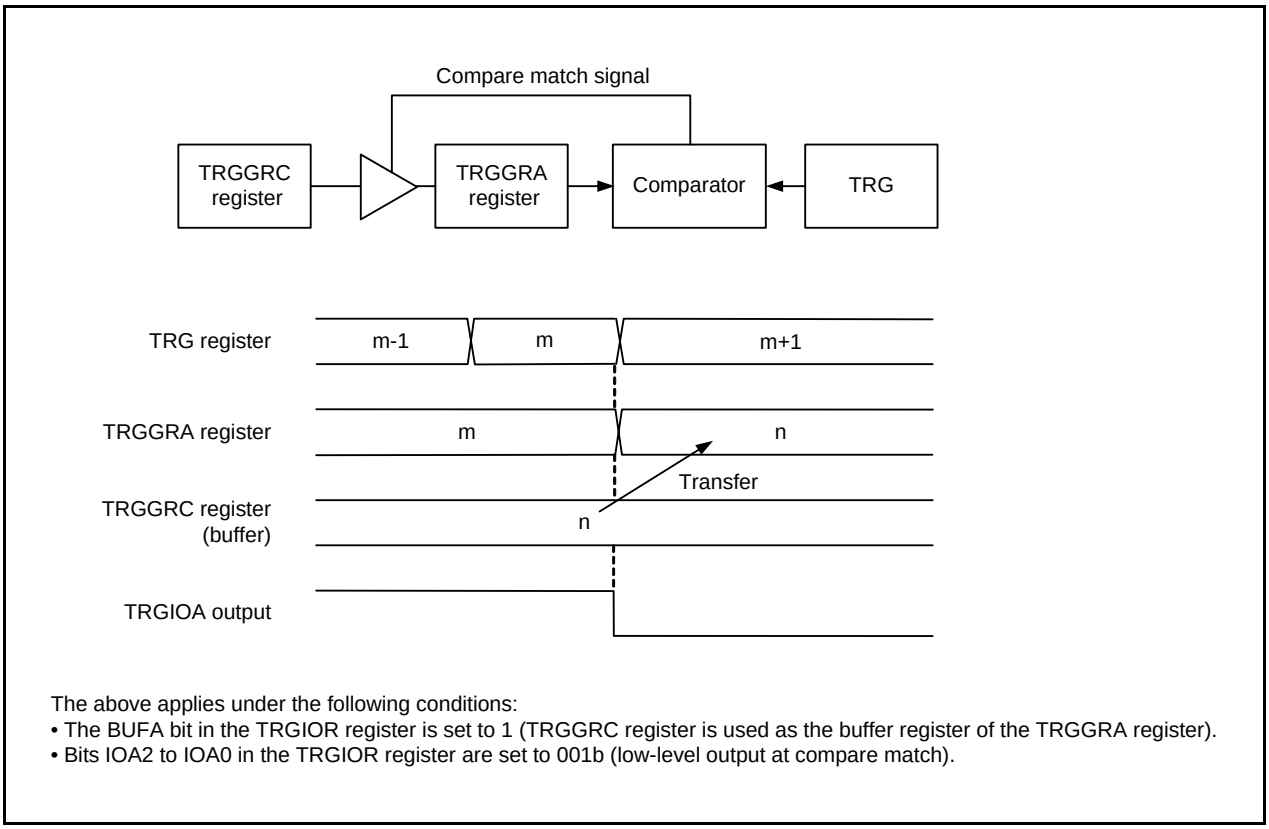


Figure 23.4 Buffer Operation for Output Compare Function

23.3.3 Digital Filter

The input to TRGIOj (j = A or B) is sampled and the level is determined when three matches occur. The digital filter function and sampling clock are selected by using the TRGMR register.
Figure 23.5 shows the Digital Filter Block Diagram.

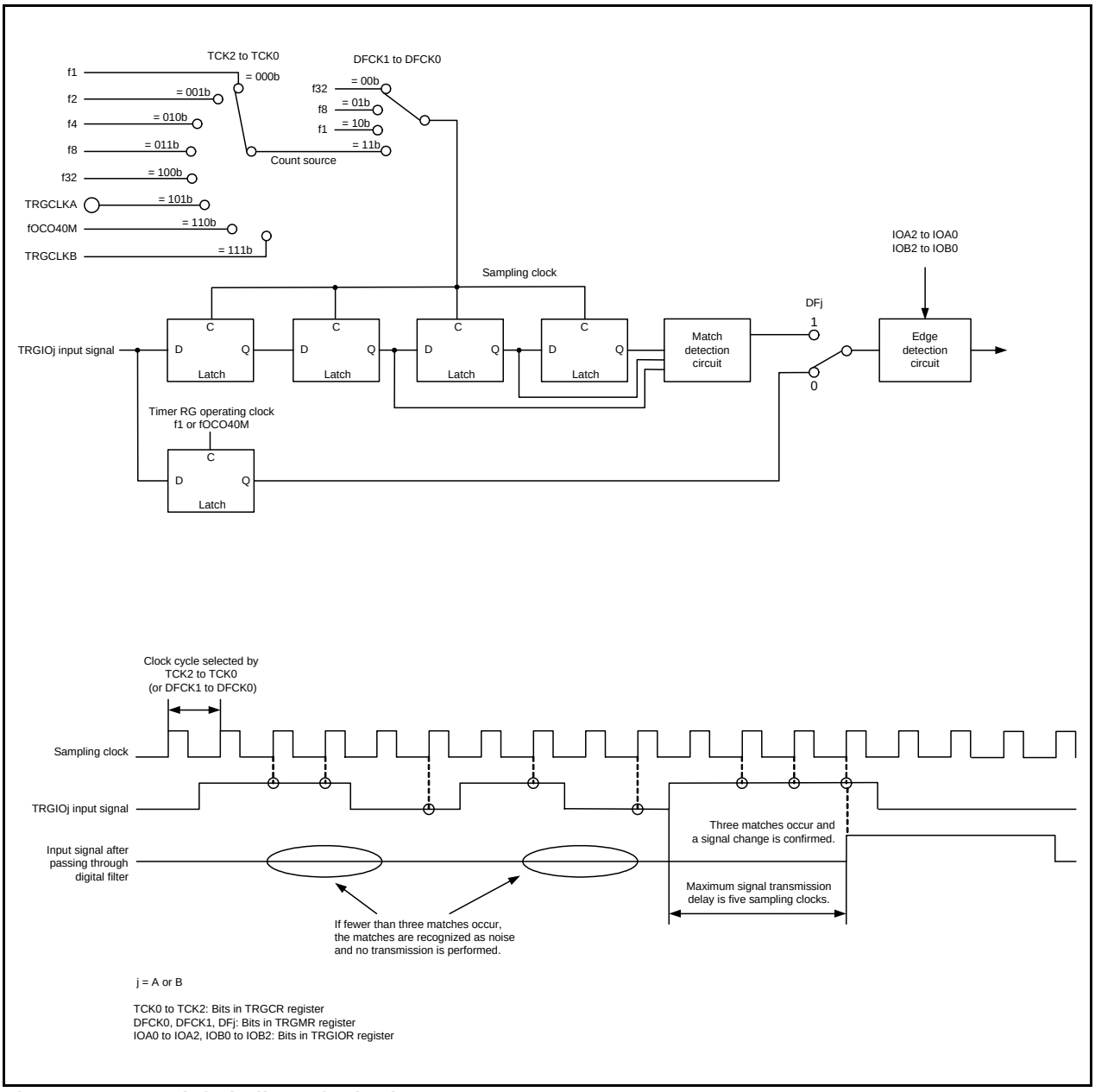


Figure 23.5 Digital Filter Block Diagram

23.4 Timer Mode (Input Capture Function)

The value of the TRG register can be transferred to registers TRGGRA and TRGGRB upon detecting the input edge of the input capture/output compare pins (TRGIOA and TRGIOB). The detection edge can be selected from the rising edge/falling edge/both edges.
The input capture function can be used for measuring pulse widths and periods.
Table 23.6 lists the Input Capture Function Specifications.

Table 23.6 Input Capture Function Specifications

Item	Specification
Count sources	f1, f2, f4, f8, f32, fOCO40M External signal input to the TRGCLKj pin (active edge selectable by a program)
Count operation	Increment
Count period	When bits CCLR1 to CCLR01 in the TRGCR register are set to 00b (free-running operation) 1/fk × 65,536 fk: Frequency of count source
Count start condition	1 (count starts) is written to the TSTART bit in the TRGMR register.
Count stop condition	0 (count stops) is written to the TSTART bit in the TRGMR register.
Interrupt request generation timing	• Input capture (active edge of the TRGIOj input) • TRG register overflow
TRGIOA/TRGIOB pin functions	Programmable I/O port or input-capture input (selectable for each individual pin)
TRGCLKA/TRGCLKB pin functions	Programmable I/O port or external clock input
Read from timer	The count value can be read by reading the TRG register.
Write to timer	The TRG register can be written to.
Selectable functions	• Input-capture input pin selection Either one or both of pins TRGIOA and TRGIOB • Active edge selection for input-capture input Rising edge, falling edge, or both rising and falling edges • Timing for setting the TRG register to 0000h Overflow or input capture • Buffer operation (Refer to **23.3.2 Buffer Operation**.) • Digital filter (Refer to **23.3.3 Digital Filter**.)

j = A or B

23.4.1 Timer RG I/O Control Register (TRGIOR) in Timer Mode (Input Capture Function)

Address 0175h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BUFB	IOB2	IOB1	IOB0	BUFA	IOA2	IOA1	IOA0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRGGRA control bit	b1 b0 0 0: Input capture to TRGGRA at the rising edge 0 1: Input capture to TRGGRA at the falling edge 1 0: Input capture to TRGGRA at both edges 1 1: Do not set.	R/W
b1	IOA1			R/W
b2	IOA2	TRGGRA mode select bit (1)	Set to 1 (input capture) in the input capture function.	R/W
b3	BUFA	TRGGRC register function select bit	0: Not used as the buffer register of the TRGGRA register 1: Used as the buffer register of the TRGGRA register	R/W
b4	IOB0	TRGGRB control bit	b5 b4 0 0: Input capture to TRGGRB at the rising edge 0 1: Input capture to TRGGRB at the falling edge 1 0: Input capture to TRGGRB at both edges 1 1: Do not set.	R/W
b5	IOB1			R/W
b6	IOB2	TRGGRB mode select bit (2)	Set to 1 (input capture) in the input capture function.	R/W
b7	BUFB	TRGGRD register function select bit	0: Not used as the buffer register of the TRGGRB register 1: Used as the buffer register of the TRGGRB register	R/W

Notes:
1. When the IOA2 bit is set to 1 (input capture function), the TRGGRA register functions as an input capture register.
2. When the IOB2 bit is set to 1 (input capture function), the TRGGRB register functions as an input capture register.

23.4.2 Procedure Example for Setting Input Capture Operation

Figure 23.6 shows a Procedure Example for Setting Input Capture Operation.

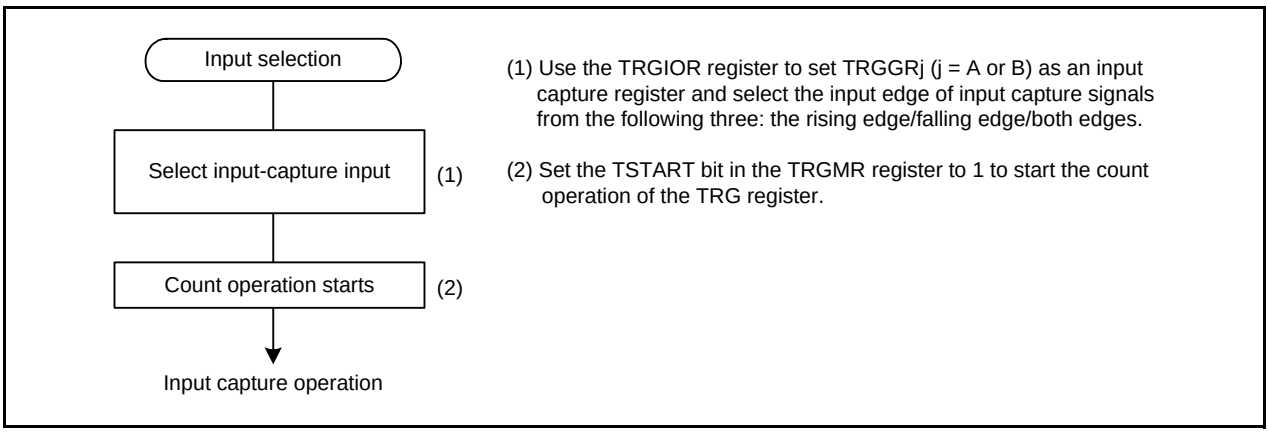


Figure 23.6 Procedure Example for Setting Input Capture Operation

23.4.3 Input Capture Signal Timing

For input-capture input, the rising edge/falling edge/both edges can be selected by setting the TRGIOR register. Figure 23.7 shows the Input-Capture Input Signal Timing.

The pulse width of input-capture input signals should be 1.5 f1 or more for a single edge and 2.5 f1 or more for both edges.

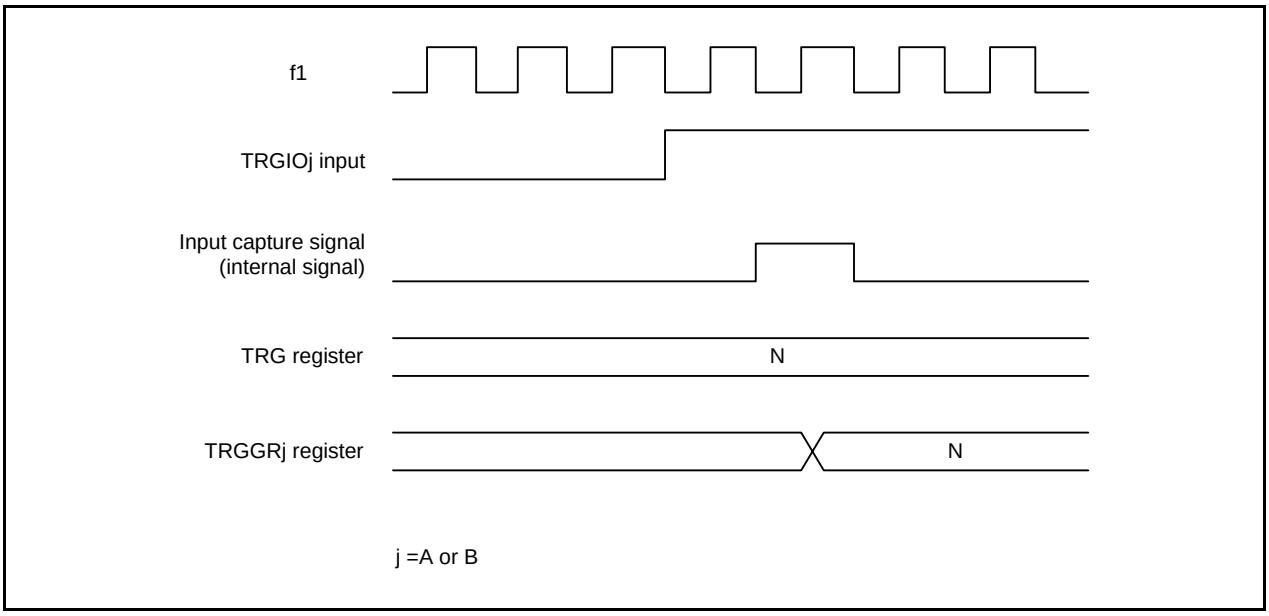


Figure 23.7 Input-Capture Input Signal Timing

23.4.4 Operating Example

Figure 23.8 shows an Operating Example of Input Capture.
This example applies when both the rising/falling edges are selected as the input-capture input edge of the TRGIOA pin and the falling edge is selected as the input-capture input edge of the TRGIOB pin, and the TRG register is set to be cleared by the input capture to the TRGGRB register.

(1) Use the TRGIOR register to set registers TRGGRA and TRGGRB as input capture registers and select the input edge of input capture signals from the following three: the rising edge/falling edge/ both edges.
(2) Set the TSTART bit in TRGMR to 1 and start the count operation of the TRG register.

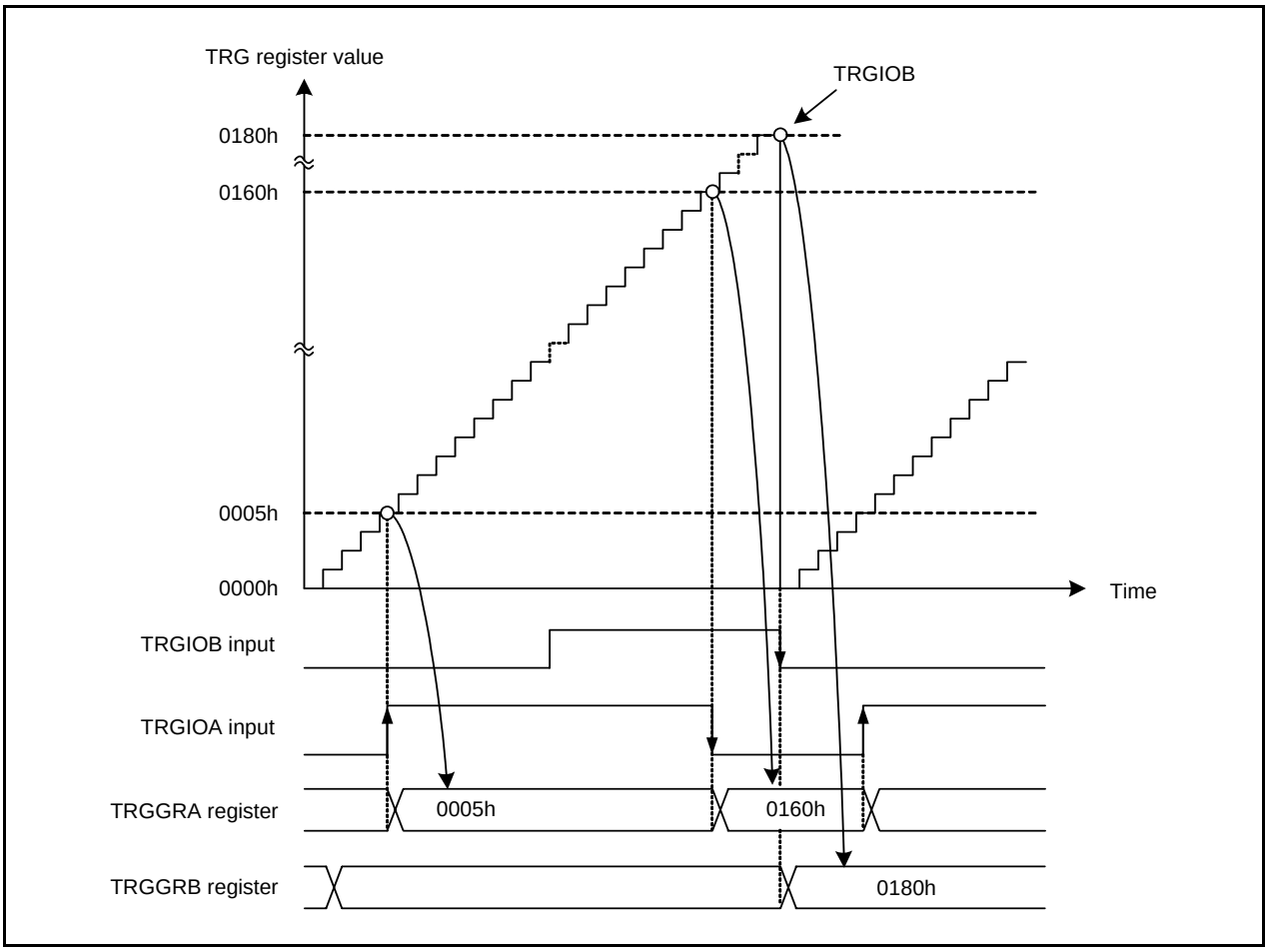


Figure 23.8 Operating Example of Input Capture

23.5 Timer Mode (Output Compare Function)

This mode (output compare function) detects when the contents of the TRG register and the TRGGRA or TRGGRB register match (compare match). When a match occurs, a signal is output from the TRGIOA or TRGIOB pin at a given level.
Table 23.7 lists the Output Compare Function Specifications.

Table 23.7 Output Compare Function Specifications

Item	Specification
Count sources	f1, f2, f4, f8, f32, fOCO40M External signal input to the TRGCLKj pin (active edge selectable by a program)
Count operation	Increment
Count periods	• When bits CCLR1 to CCLR01 in the TRGCR register are set to 00b (free-running operation) 1/fk × 65,536 fk: Frequency of count source • When bits CCLR1 to CCLR01 in the TRGCR register are set to 01b or 10b (TRG is set to 0000h by the compare match with TRGGRj) 1/fk × (n+1) n: Value set in the TRGGRj register
Waveform output timing	Compare match
Count start condition	1 (count starts) is written to the TSTART bit in the TRGMR register.
Count stop condition	0 (count stops) is written to the TSTART bit in the TRGMR register.
Interrupt request generation timing	• Compare match (the contents of the TRG register and the TRGGRj register match) • TRG register overflow
TRGIOA/TRGIOB pin functions	Programmable I/O port or output-compare output (selectable for each individual pin)
TRGCLKA/TRGCLKB pin functions	Programmable I/O port or external clock input
Read from timer	The count value can be read by reading the TRG register.
Write to timer	The TRG register can be written to.
Selectable functions	• Output-compare output pin selection Either one or both of pins TRGIOA and TRGIOB • Output level selection at compare match Low-level output, high-level output, or inverted output level • Timing for setting the TRG register to 0000h Overflow or compare match with the TRGGRj register • Buffer operation (Refer to **23.3.2 Buffer Operation**.)

j = A or B

23.5.1 Timer RG I/O Control Register (TRGIOR) in Timer Mode (Output Compare Function)

Address 0175h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BUFB	IOB2	IOB1	IOB0	BUFA	IOA2	IOA1	IOA0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRGGRA control bit	b1 b0 0 0: Pin output by compare match is disabled (TRGIOA pin functions as a programmable I/O port) 0 1: Low-level output at compare match with TRGGRA 1 0: High-level output at compare match with TRGGRA 1 1: Toggle output at compare match with TRGGRA	R/W
b1	IOA1			R/W
b2	IOA2	TRGGRA mode select bit (1)	Set to 0 (output compare) in the output compare function.	R/W
b3	BUFA	TRGGRC register function select bit	0: Not used as the buffer register of the TRGGRA register 1: Used as the buffer register of the TRGGRA register	R/W
b4	IOB0	TRGGRB control bit	b5 b4 0 0: Pin output by compare match is disabled (TRGIOB pin functions as a programmable I/O port.) 0 1: Low-level output at compare match with TRGGRB 1 0: High-level output at compare match with TRGGRB 1 1: Toggle output at compare match with TRGGRB	R/W
b5	IOB1			R/W
b6	IOB2	TRGGRB mode select bit (2)	Set to 0 (output compare) in the output compare function.	R/W
b7	BUFB	TRGGRD register function select bit	0: Not used as the buffer register of the TRGGRB register 1: Used as the buffer register of the TRGGRB register	R/W

Notes:

1. When the IOA2 bit is set to 0 (output compare function), the TRGGRA register functions as a compare match register. After reset, the TRGIOA pin outputs as follows until the first compare match occurs.
   IOA1 to IOA0 = 01b: High-level output
   10b: Low-level output
   11b: Low-level output
2. When the IOB2 bit is set to 0 (output compare function), the TRGGRB register functions as a compare match register. After reset, the TRGIOB pin outputs as follows until the first compare match occurs.
   IOB1 to IOB0 = 01b: High-level output
   10b: Low-level output
   11b: Low-level output

23.5.2 Procedure Example for Setting Waveform Output by Compare Match

Figure 23.9 shows an Operating Example of Waveform Output by Compare Match.

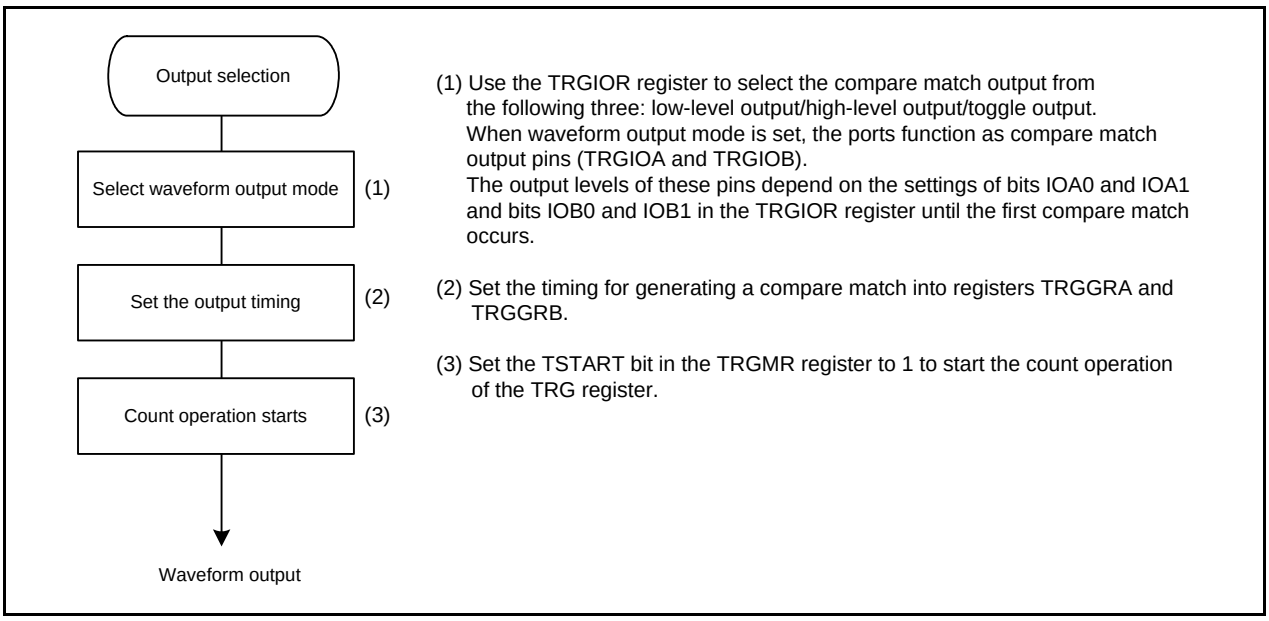


Figure 23.9 Operating Example of Waveform Output by Compare Match

23.5.3 Output-Compare Output Timing

A compare match signal is generated at the last state when the TRG register and the TRGGRA or TRGGRB register match (at the timing for updating the count value that the TRG register matches). When the compare match signal is generated, the output value set by the TRGIOR register is output to the output-compare output pin (TRGIOA or TRGIOB). After the TRG register and the TRGGRA or TRGGRB register, no compare match signal is generated until the TRG input clock is generated.
Figure 23.10 shows the Output-Compare Output Timing.

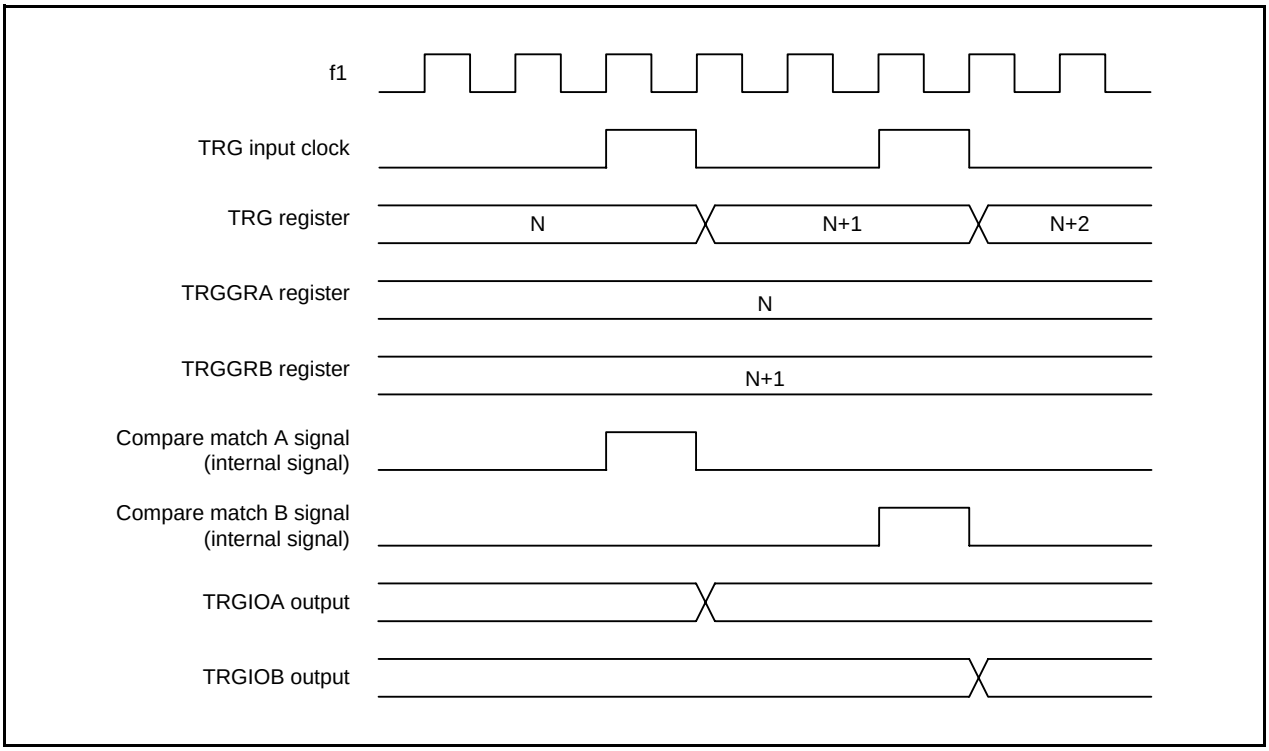


Figure 23.10 Output-Compare Output Timing

23.5.4 Operating Example

Figure 23.11 shows an Operating Example of Low-Level Output and High-Level Output.
This example applies when the TRG register is set for free-running operation, and low-level output is set at compare match A and high-level output is set at compare match B. When the set level and the pin level match, the pin level does not change.

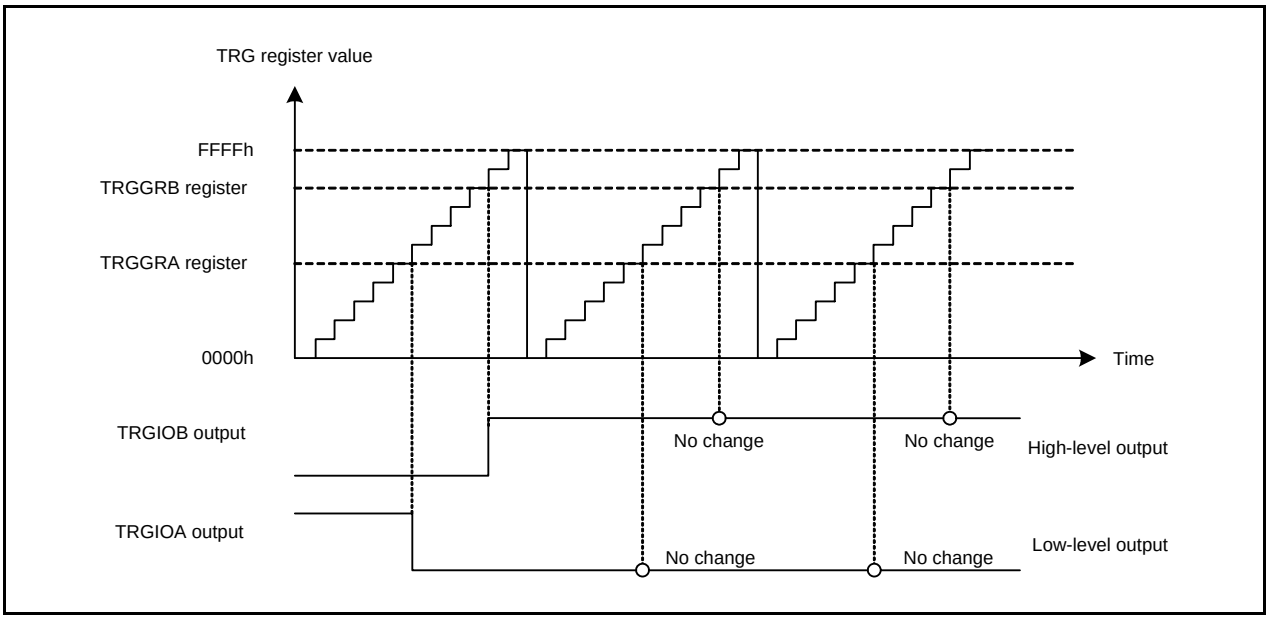


Figure 23.11 Operating Example of Low-Level Output and High-Level Output

Figure 23.12 shows an Operating Example of Toggle Output.
This example applies when the TRG register is set for period counting operation (counter clear at compare match B), and toggle output is set at both compare match A and B.
Use the TRGIOR register to select the compare match output from the following three: low-level output/high-level output/toggle output. When waveform output mode is set, the ports function as compare match output pins (TRGIOA and TRGIOB).
Set the timing for generating a compare match into registers TRGGRA and TRGGRB.
Set the TSTART bit in the TRGMR register to 1 to start the count operation of the TRG register.

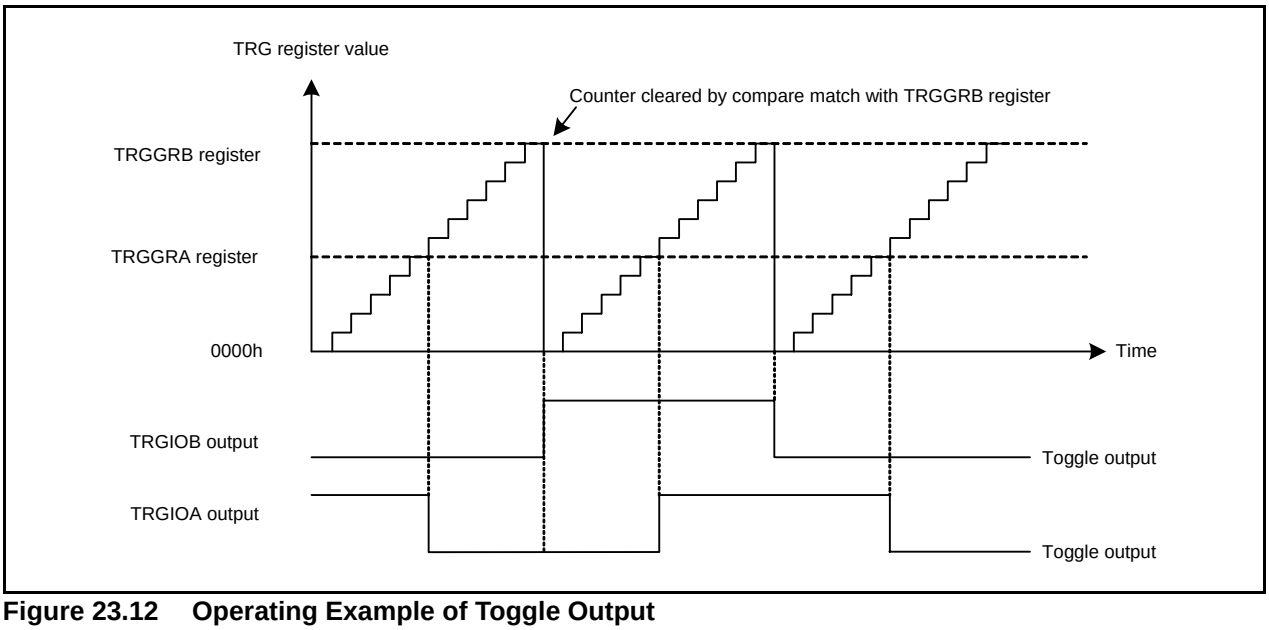


Figure 23.12 Operating Example of Toggle Output

23.6 PWM Mode

In PWM mode, registers TRGGRA and TRGGRB are used as a pair and a PWM waveform is output from the TRGIOA output pin. The output setting by the TRGIOR register is invalid for the pins set to PWM mode. Set the high-level output timing for a PWM waveform into the TRGGRA register and the low-level output timing for a PWM waveform into the TRGGRB register.
By setting the compare match with either the TRGGRA or TRGGRB register as the counter clear source for the TRG register, a PWM waveform with duty 0% to 100% can be output from the TRGIOA pin.

Table 23.8 lists the PWM Mode Specifications. Table 23.9 lists the Combination of PWM Output Pins and Registers. When the setting values in registers TRGGRA and TRGGRB are the same, the output value does not change even if a compare match occurs.

Table 23.8 PWM Mode Specifications

Item	Specification
Count sources	f1, f2, f4, f8, f32, fOCO40M External signal input to the TRGCLKj pin (active edge selectable by a program)
Count operation	Increment
PWM waveform	• The high-level output timing of a PWM waveform is set into the TRGGRA register. • The low-level output timing of a PWM waveform is set into the TRGGRB register.
Count start condition	1 (count starts) is written to the TSTART bit in the TRGMR register.
Count stop condition	0 (count stops) is written to the TSTART bit in the TRGMR register.
Interrupt request generation timing	• Compare match (the contents of the TRG register and TRGRj register match) • TRG register overflow
TRGIOA pin function	PWM output
TRGIOB pin function	Programmable I/O port
TRGCLKA/TRGCLKB pin functions	Programmable I/O port or external clock input
Read from timer	The count value can be read by reading the TRG register.
Write to timer	The TRG register can be written to.
Selectable functions	• Timing for setting the TRG register to 0000h Overflow or compare match with the TRGGRj register • Buffer operation (Refer to **23.3.2 Buffer Operation**.)

j = A or B

Table 23.9 Combination of PWM Output Pins and Registers

Output Pin	High-Level Output	Low-Level Output
TRGIOA	TRGGRA	TRGGRB
TRGIOB	I/O port function	

23.6.1 Procedure Example for Setting PWM Mode

Figure 23.13 shows a Procedure Example for Setting PWM Mode.

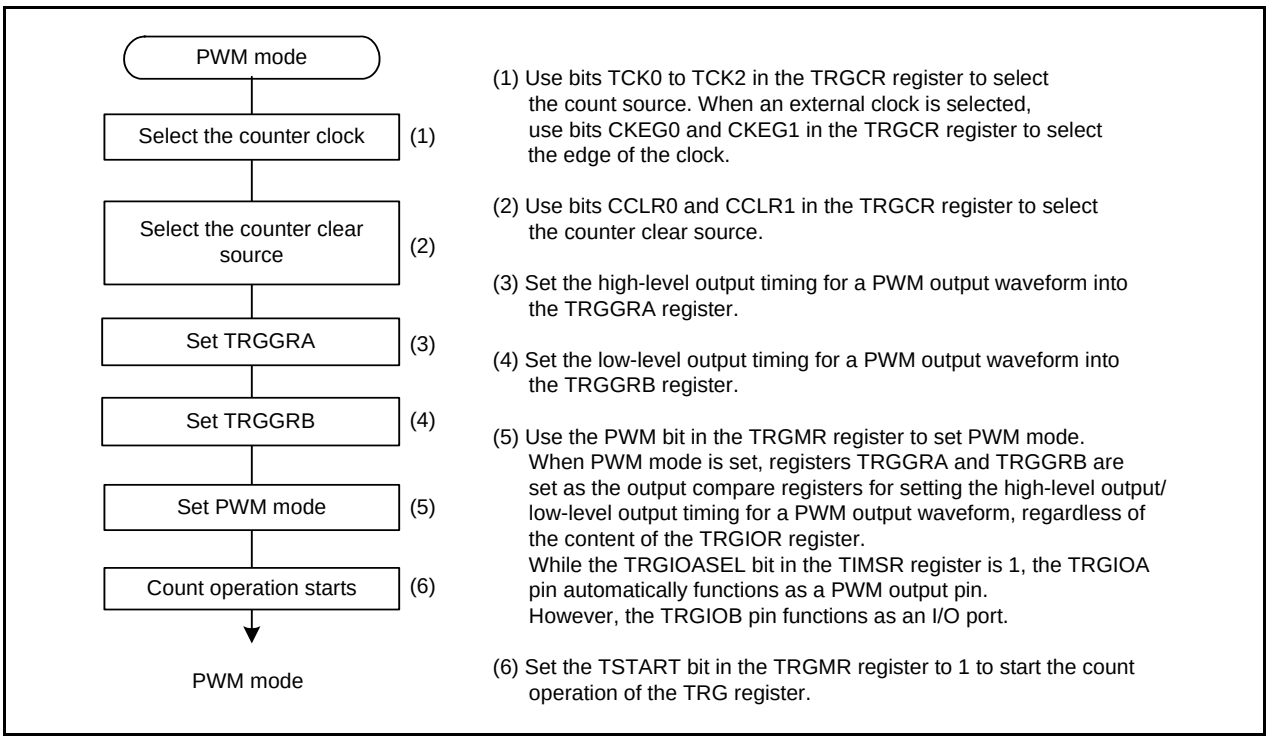


Figure 23.13 Procedure Example for Setting PWM Mode

23.6.2 Operating Example

Figure 23.14 shows an Operating Example (1) in PWM Mode.
When PWM mode is set while the TRGIOASEL bit in the TIMSR register is 1, the TRGIOA pin automatically functions as an output pin, and high-level output is set at the compare match with the TRGGRA register and low-level output is set at the compare match with the TRGGRB register. However, regardless of the setting of the TRGIOR register, the TRGIOB pin functions as an I/O port.

This example applies when the compare match with the TRGGRA or TRGGRB register is set as the counter clear source for the TRG register. The initial status of the TRGIOA pin depend only on the counter clear sources. This correspondence is shown in Table 23.10.

Table 23.10 Correspondence between Initial Status of TRGIOA Pin and Counter Clear Sources

Counter Clear Source	Initial Status of TRGIOA Pin
Compare match with TRGGRA register	High
Compare match with TRGGRB register	Low

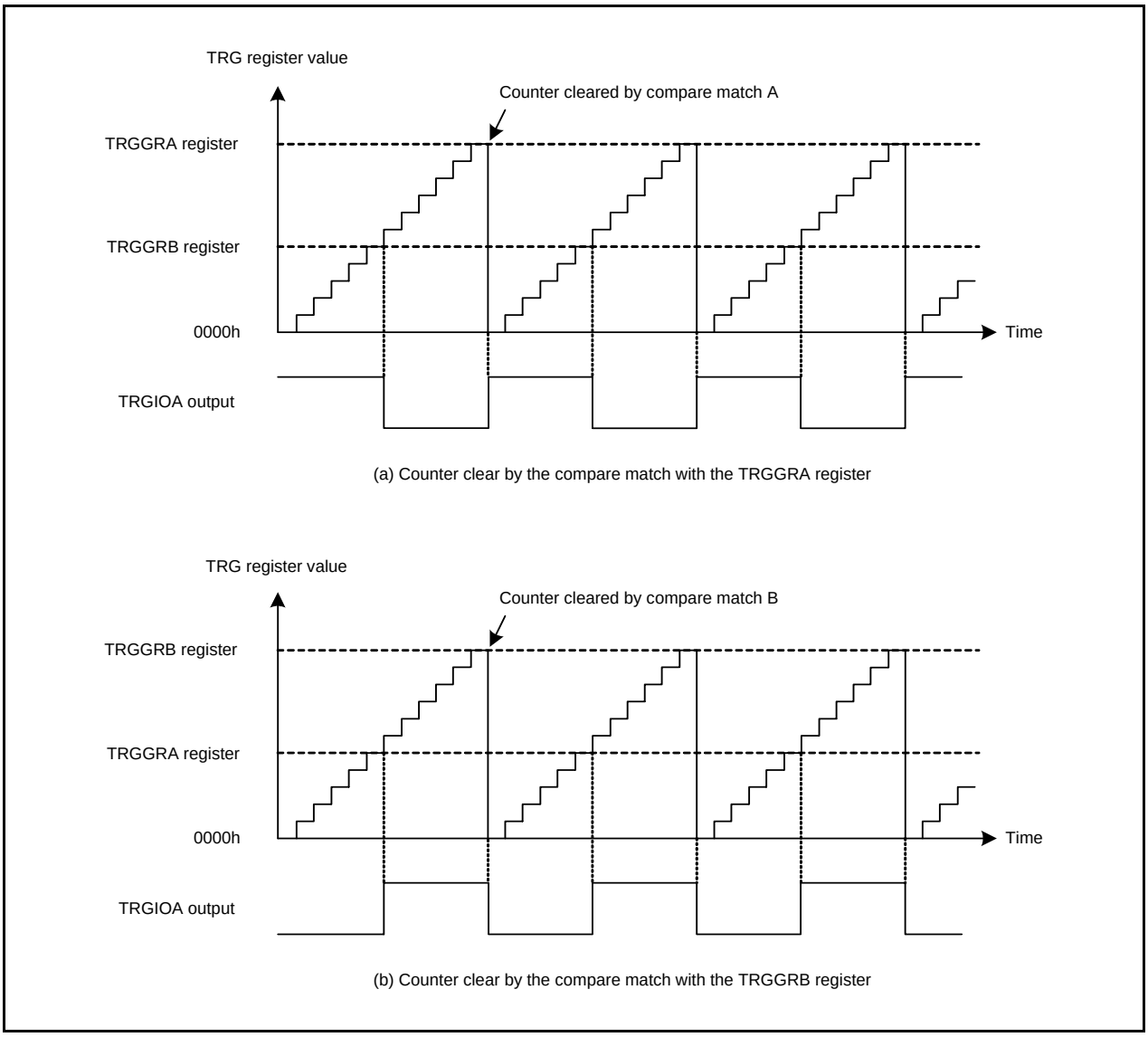


Figure 23.14 Operating Example (1) in PWM Mode

Figure 23.15 shows an example for outputting a PWM waveform with duty 0% and duty 100%.
A PWM waveform is set to duty 0% when the compare match with the TRGGRB register is set as the counter clear source with the following:

- TRGGRA setting value > TRGGRB setting value

A PWM waveform is set to duty 100% when the compare match with TRGGRA register is set as the counter clear source with the following:

- TRGGRB setting value > TRGGRA setting value

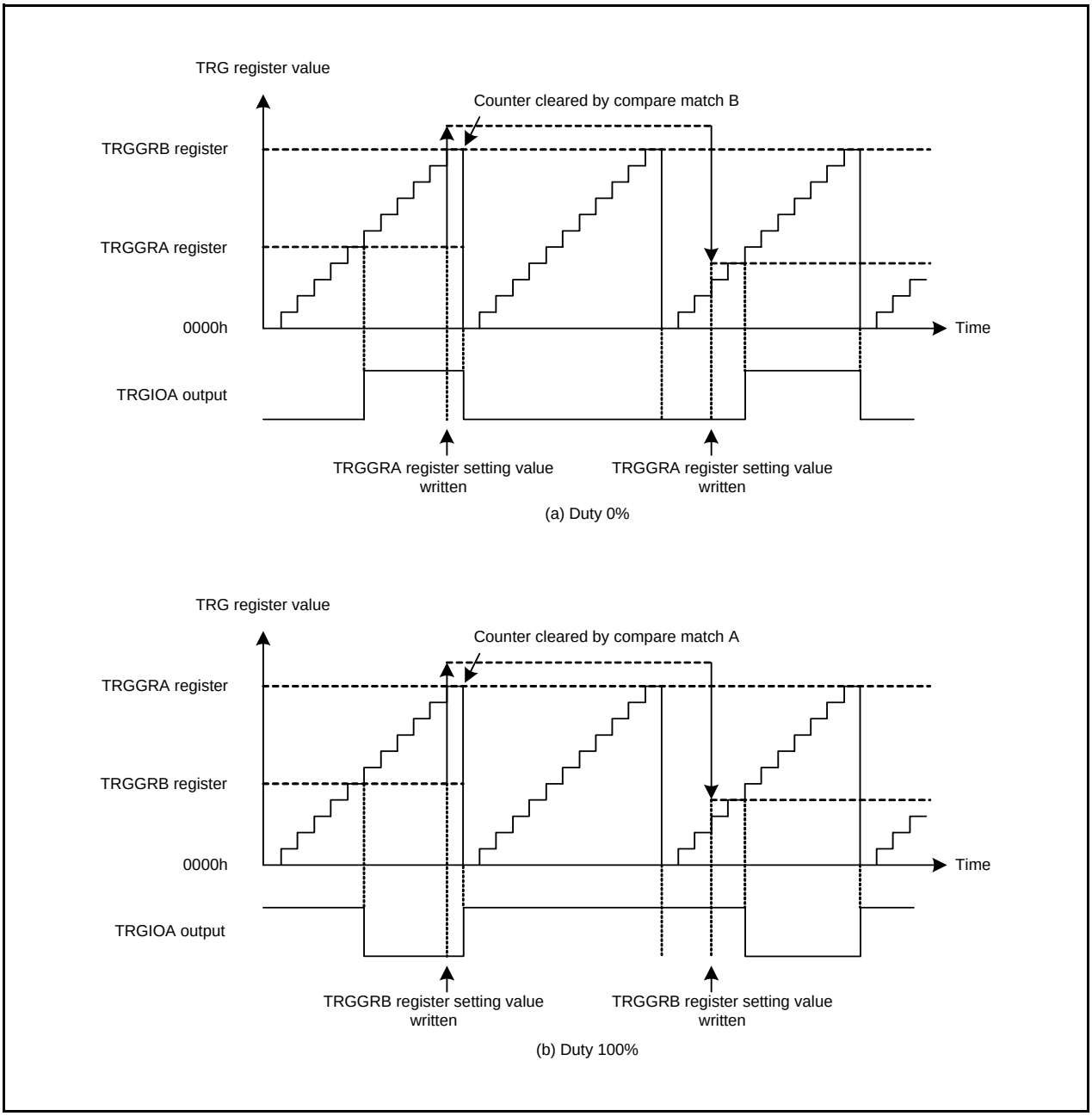


Figure 23.15 Operating Example (2) in PWM Mode

23.7 Phase Counting Mode

In phase counting mode, a phase difference between external input signals from two pins TRGCLKA and TRGCLKB is detected and the TRG register is incremented/decremented.

When phase counting mode is set while the TRGCLKASEL is 1 and the TRGCLKBSEL bit is 1, regardless of the settings of bits TCK0 to TCK2 and bits CKEG0 and CKEG1 in the TRGCR register, pins TRGCLKA and TRGCLKB automatically function as external clock input pins and the TRG register is incrermented/decremented by bits CNTEN0 to CNTEN7 in the TRGCNTC register. However, bits CCLR0 and CCLR1 in the TRGCR register and registers TRGIOR, TRGIER, TRGSR, TRGGRA, and TRGGRB are enabled. This allows the input capture/output compare functions, PWM output function, and interrupt sources to be used.

The TRG register operates counting at both the rising/falling edges of pins TRGCLKA and TRGCLKB by bits CNTEN0 to CNTEN7. Table 23.12 lists the Increment/Decrement Conditions for TRG Register. Table 23.11 lists the Phase Counting Mode Specifications.

Table 23.11 Phase Counting Mode Specifications

Item	Specification
Count source	External signal input to the TRGCLKj pin
Count operations	Increment/decrement
Count start condition	1 (count starts) is written to the TSTART bit in the TRGMR register.
Count stop condition	0 (count stops) is written to the TSTART bit in the TRGMR register.
Interrupt request generation timing	• Input capture (active edge of the TRGIOj input) • Compare match (the contents of the TRG register and the TRGRj register match) • TRG register underflow • TRG register overflow
TRGIOA pin function	Programmable I/O port, input-capture input, output-compare output, or PWM output
TRGIOB pin function	Programmable I/O port, input-capture input, or output-compare output
TRGCLKA/TRGCLKB pin functions	External clock input
Read from timer	The count value can be read by reading the TRG register.
Write to timer	The TRG register can be written to.
Selectable functions	• Selection of counter addition/substitution conditions Selectable by bits CNTEN7 to CNTEN0 bits in the TRGCNTC register. • Input capture/output compare functions and PWM functions can be used.

j = A or B

Table 23.12 Increment/Decrement Conditions for TRG Register

TRGCLKB pin	↑		High		↓		Low		High		↓		Low		↑	
TRGCLKA pin	Low		↑		High		↓		↓		Low		↑		High	
Bits CNTEN7 to CNTEN0 in TRGCNTC register	CNTEN7		CNTEN6		CNTEN5		CNTEN4		CNTEN3		CNTEN2		CNTEN1		CNTEN0	
Value	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Count direction	–	+1	–	+1	–	+1	–	+1	–	–1	–	–1	–	–1	–	–1

23.7.1 Timer RG Control Register (TRGCR) in Phase Counting Mode

Address 0172h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	CCLR1	CCLR0	CKEG1	CKEG0	TCK2	TCK1	TCK0
After Reset	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TCK0	Count source select bit	Disabled in phase counting mode.	R/W
b1	TCK1			R/W
b2	TCK2			R/W
b3	CKEG0	External clock active edge select bit	Disabled in phase counting mode.	R/W
b4	CKEG1			R/W
b5	CCLR0	TRG register clear select bit	b6 b5 0 0: Clear disabled 0 1: TRG register cleared by input capture or compare match with TRGGRA 1 0: TRG register cleared by input capture or compare match with TRGGRB 1 1: Do not set.	R/W
b6	CCLR1			R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

23.7.2 Procedure Example for Setting Phase Counting Mode

Figure 23.16 shows a Procedure Example for Setting Phase Counting Mode.

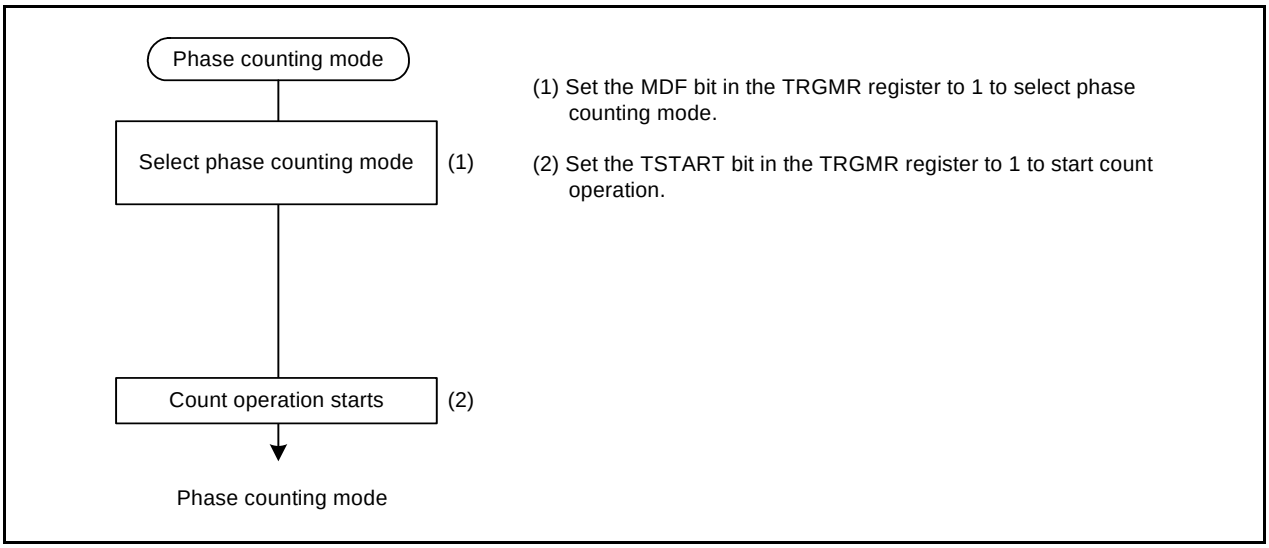


Figure 23.16 Procedure Example for Setting Phase Counting Mode

23.7.3 Operating Example

Figures 23.17 to 23.20 show operating examples in phase counting mode. Table 23.12 lists the Increment/Decrement Conditions for TRG Register.

In phase counting mode, the TRG register is incremented/decremented at both the rising (↑)/falling (↓) edges of pins TRGCLKA and TRGCLKB by bits CNTEN0 to CNTEN7 in the TRGCNTC register.

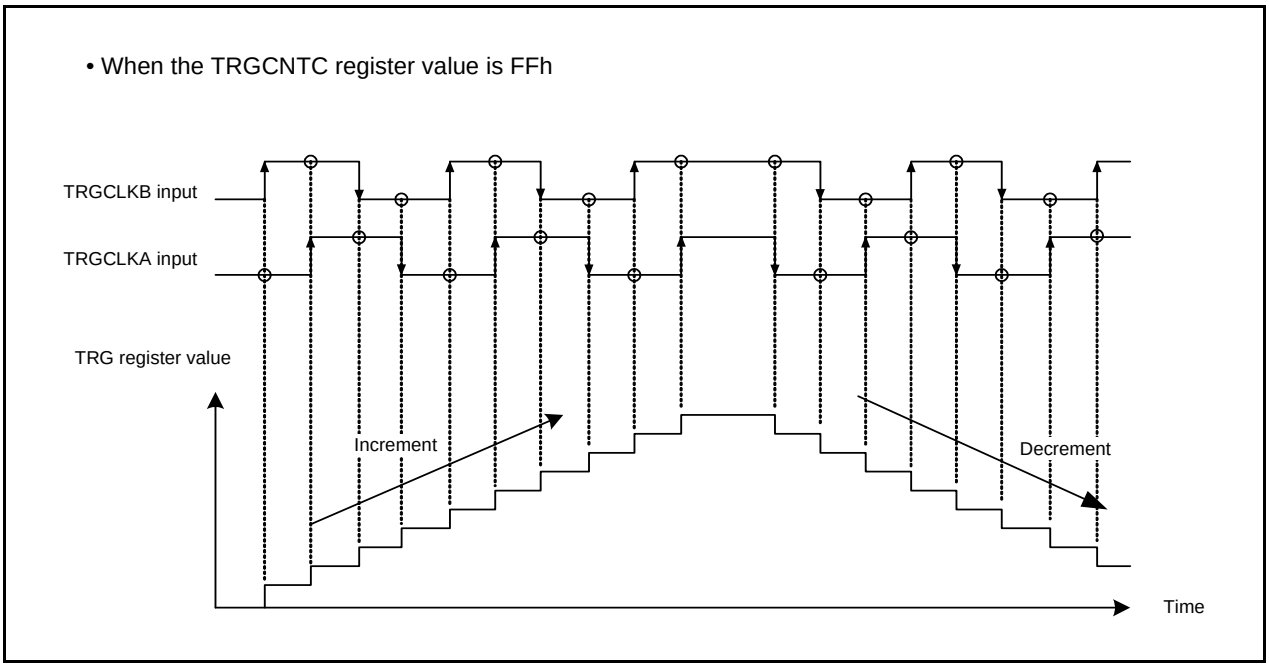


Figure 23.17 Operating Example 1 in Phase Counting Mode

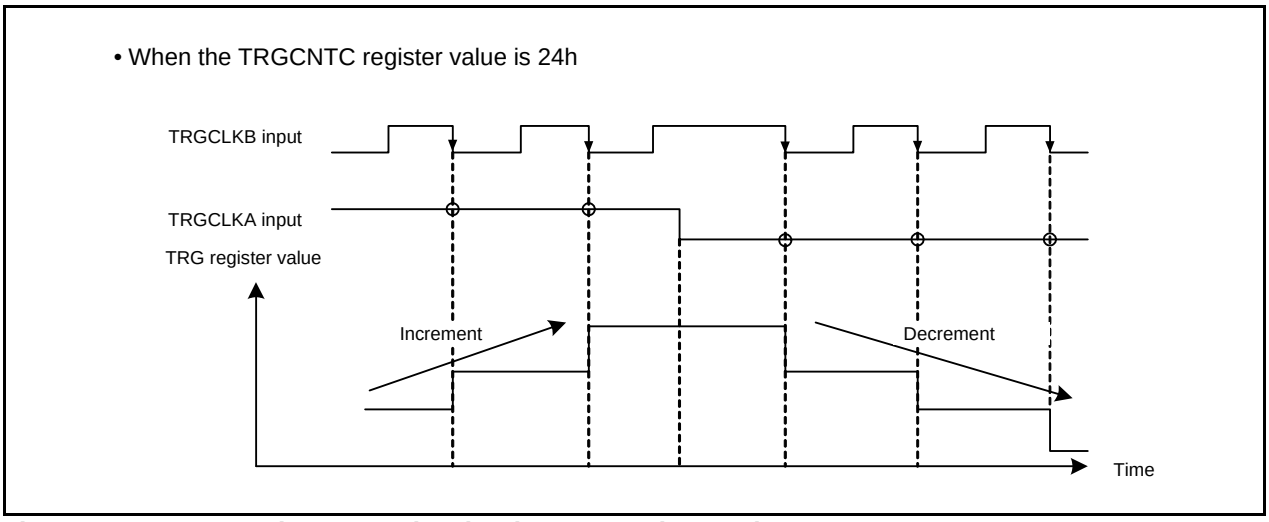


Figure 23.18 Operating Example 2 in Phase Counting Mode

• When the TRGCNTC register value is 28h

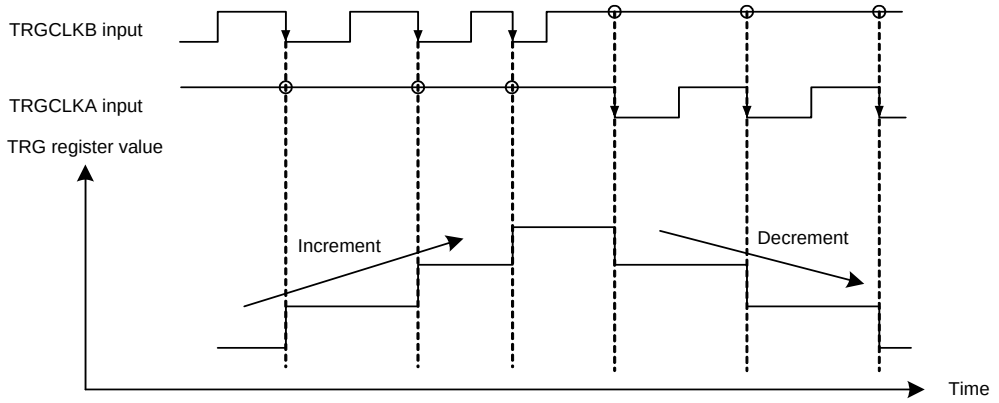


Figure 23.19 Operating Example 3 in Phase Counting Mode

• When the TRGCNTC register value is 5Ah

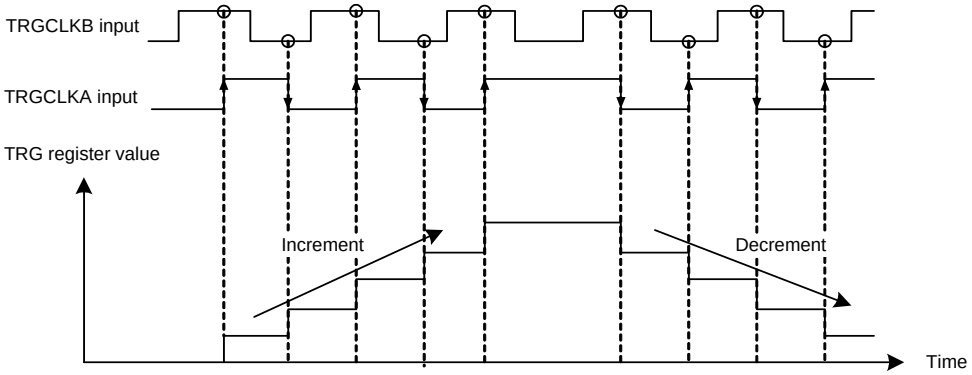


Figure 23.20 Operating Example 4 in Phase Counting Mode

23.8 Timer RG Interrupt

Timer RG generates a timer RG interrupt request from four sources. The timer RG interrupt uses the single TRGIC register (bits IR and ILVL0 to ILVL2) and a single vector.
Table 23.13 lists the Registers Associated with Timer RG Interrupt and Figure 23.21 is the Timer RG Interrupt Block Diagram.

Table 23.13 Registers Associated with Timer RG Interrupt

Timer RG Status Register	Timer RG Interrupt Enable Register	Timer RG Interrupt Control Register
TRGSR	TRGIER	TRGIC

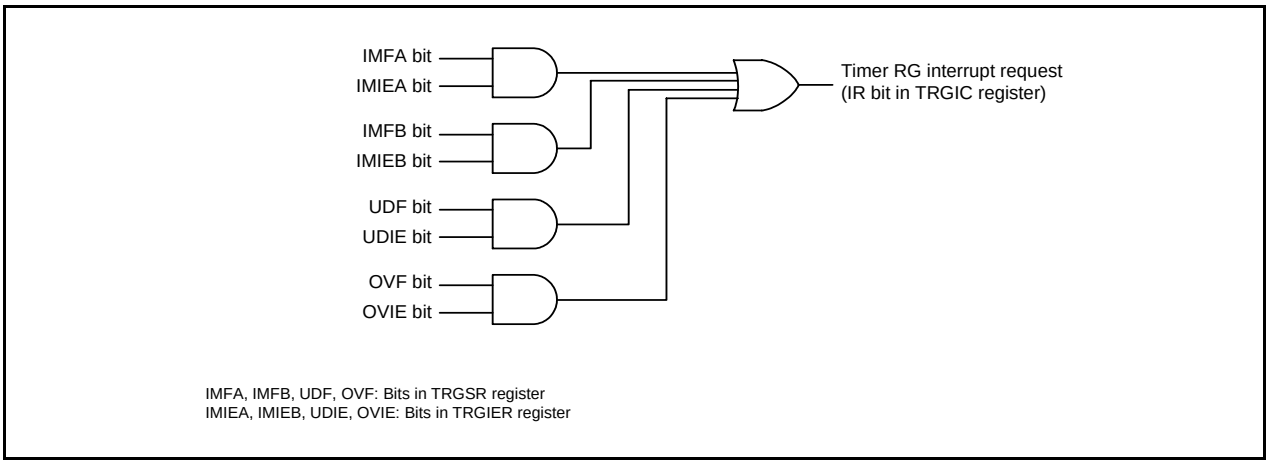


Figure 23.21 Timer RG Interrupt Block Diagram

Like other maskable interrupts, the timer RG interrupt is controlled by the combination of the I flag, IR bit, bits ILVL0 to ILVL2, and IPL. However, it differs from other maskable interrupts in the following respects because a single interrupt source (timer RG interrupt) is generated from multiple interrupt request sources.

- The IR bit in the TRGIC register is set to 1 (interrupt requested) when a bit in the TRGSR register is set to 1 and the corresponding bit in the TRGIER register is also set to 1 (interrupt enabled).
- The IR bit is set to 0 (no interrupt requested) when the bit in the TRGSR register or the corresponding bit in the TRGIER register is set to 0, or both are set to 0. In other words, the interrupt request is not maintained if the IR bit is once set to 1 but the interrupt is not acknowledged.
- If another interrupt source is triggered after the IR bit is set to 1, the IR bit remains set to 1 and does not change.
- If multiple bits in the TRGIER register are set to 1, use the TRGSR register to determine the source of the interrupt request.
- The bits in the TRGSR register are not automatically set to 0 when an interrupt is acknowledged. Set them to 0 within the interrupt routine. Refer to **23.2.5 Timer RG Status Register (TRGSR)**, for the procedure for setting these bits to 0.

Refer to **23.2.4 Timer RG Interrupt Enable Register (TRGIER)**, for details of the TRGIER register.
Refer to **11.3 Interrupt Control**, for details of the TRGIC register and **11.1.5.2 Relocatable Vector Tables**, for information on interrupt vectors.

23.9 Notes on Timer RG

23.9.1 Phase Difference, Overlap, and Pulse Width in Phase Counting Mode

The phase difference and overlap between external input signals from pins TRGCLKA and TRGCLKB should be 1.5 f1 or more, respectively. The pulse width should be 2.5 f1 or more. Figure 23.22 shows the Phase Difference, Overlap, and Pulse Width in Phase Counting Mode.

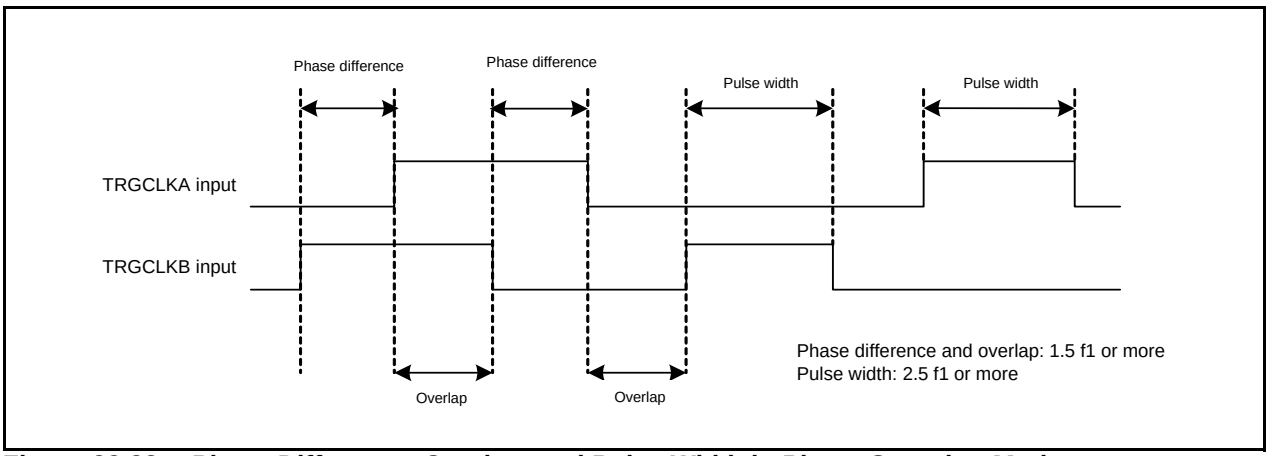


Figure 23.22 Phase Difference, Overlap, and Pulse Width in Phase Counting Mode

23.9.2 Timer RG Counter (TRG)

When writing to the TRG register or TRGCR register, make sure the TSTART bit in the TRGMR register is set to 0 (count stops).

23.9.3 Timer Mode

When using the output compare function in timer mode, use the TRGIOR register to select the compare match output from the following three: low-level output, high-level output, or toggle output. When waveform output mode is selected, the port functions as the compare match output pin (TRGIOA or TRGIOB) while the TRGIOASEL0 bit or the TRGIOBSEL0 bit in the TRGPSR register is 1. The output level of these pins depend on the settings of bits IOA0 and IOA1, or bits IOB0 and IOB1 in the TRGIOR register until the first compare match occurs.

After setting the TRGIOR register, the output level is undefined for one cycle of the timer RG operating clock, and the corresponding level to bits IOA0 and IOA1 or bits IOB0 and IOB1 is output.

23.9.4 PWM Mode

When using PWM mode, the TRGIOA pin becomes the PWM output pin by setting the PWM bit in the TRGMR register to 1 (PWM mode) while the TRGIOASEL0 bit in the TRGPSR register is 1. The output level of the PWM output pin depends on the settings of bits CCLR0 and CCLR1 in the TRGCR register until the first compare match occurs.

After setting the PWM bit, the output level is undefined for one cycle of the timer RG operating clock, and the corresponding level to bits CCLR0 and CCLR1 is output.

24. Serial Interface (UARTi (i = 0 or 1))

The serial interface consists of three channels, UART0 to UART2. This chapter describes the UARTi (i = 0 or 1).

24.1 Overview

UART0 and UART 1 have a dedicated timer to generate a transfer clock and operate independently. UART0 and UART1 support clock synchronous serial I/O mode and clock asynchronous serial I/O mode (UART mode). Figure 24.1 shows a UARTi (i = 0 or 1) Block Diagram. Figure 24.2 shows a Block Diagram of UARTi Transmit/Receive Unit. Table 24.1 lists the Pin Configuration of UARTi (i = 0 or 1).

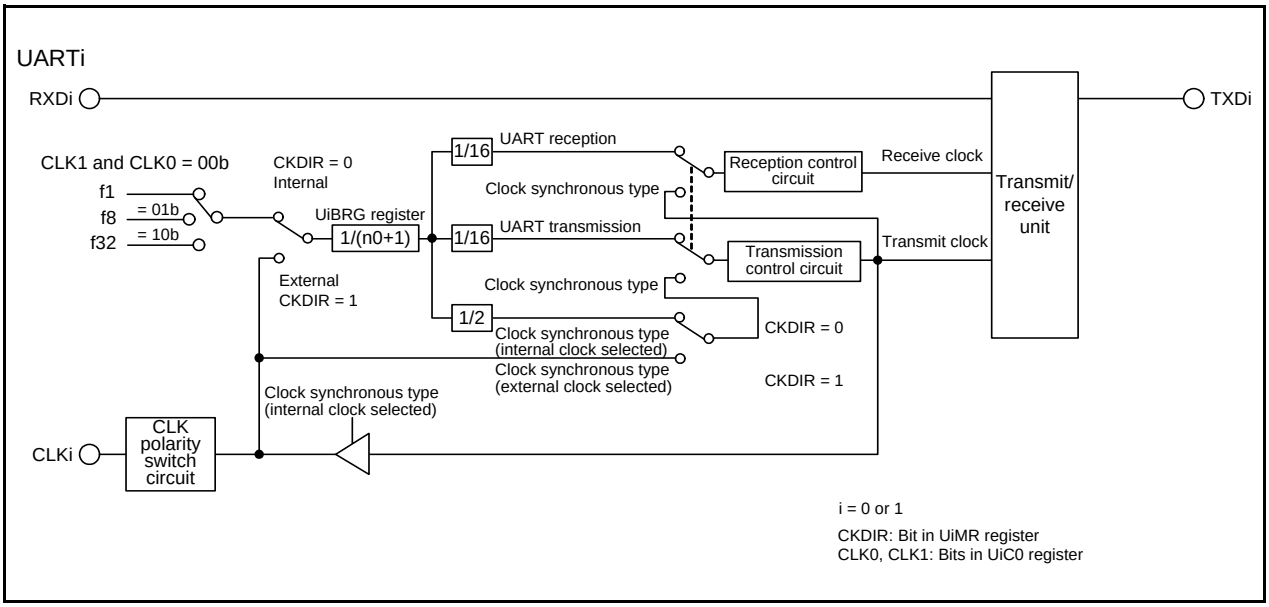


Figure 24.1 UARTi (i = 0 or 1) Block Diagram

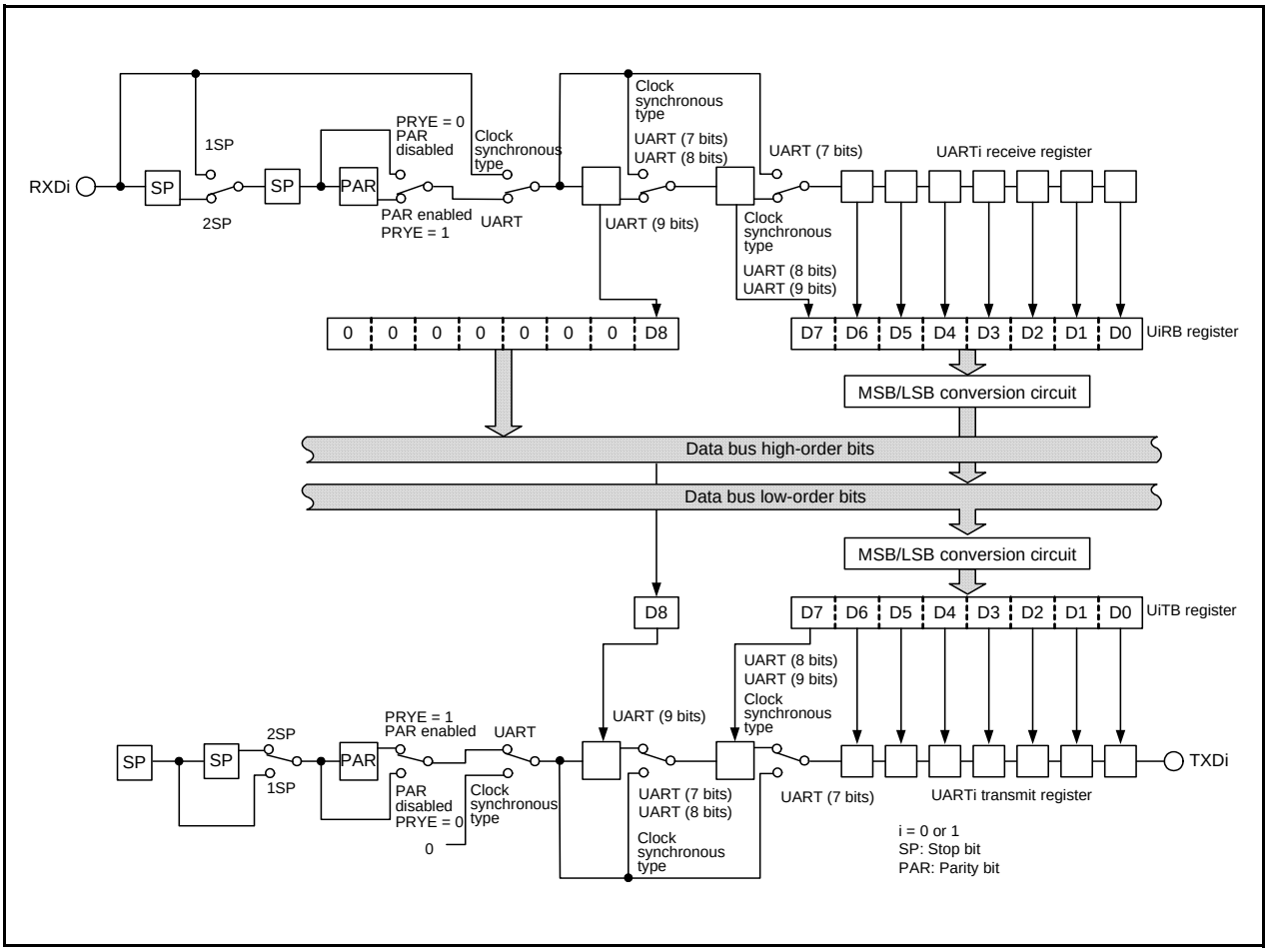


Figure 24.2 Block Diagram of UARTi Transmit/Receive Unit

Table 24.1 Pin Configuration of UARTi (i = 0 or 1)

Pin Name	Assigned Pin	I/O	Function
TXD0	P1_4	Output	Serial data output
RXD0	P1_5	Input	Serial data input
CLK0	P1_6	I/O	Transfer clock I/O
TXD1	P0_1 or P6_3	Output	Serial data output
RXD1	P0_2 or P6_4	Input	Serial data input
CLK1	P0_3 or P6_5	I/O	Transfer clock I/O

24.2 Registers

24.2.1 UARTi Transmit/Receive Mode Register (UiMR) (i = 0 or 1)

Address 00A0h (U0MR), 0160h (U1MR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	PRYE	PRY	STPS	CKDIR	SMD2	SMD1	SMD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SMD0	Serial I/O mode select bit	b2 b1 b0 0 0 0: Serial interface disabled 0 0 1: Clock synchronous serial I/O mode 1 0 0: UART mode, transfer data 7 bits long 1 0 1: UART mode, transfer data 8 bits long 1 1 0: UART mode, transfer data 9 bits long Other than above: Do not set.	R/W
b1	SMD1			R/W
b2	SMD2			R/W
b3	CKDIR	Internal/external clock select bit	0: Internal clock 1: External clock	R/W
b4	STPS	Stop bit length select bit	0: One stop bit 1: Two stop bits	R/W
b5	PRY	Odd/even parity select bit	Enabled when PRYE = 1 0: Odd parity 1: Even parity	R/W
b6	PRYE	Parity enable bit	0: Parity disabled 1: Parity enabled	R/W
b7	—	Reserved bit	Set to 0.	R/W

24.2.2 UARTi Bit Rate Register (UiBRG) (i = 0 or 1)

Address 00A1h (U0BRG), 0161h (U1BRG)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7 to b0	If the setting value is n, UiBRG divides the count source by n+1.	00h to FFh	W

Write to the UiBRG register while transmission and reception stop.
Use the MOV instruction to write to this register.
Set bits CLK0 and CLK1 in the UiC0 register before writing to the UiBRG register.

24.2.3 UARTi Transmit Buffer Register (UiTB) (i = 0 or 1)

Address 00A3h to 00A2h (U0TB), 0163h to 0162h (U1TB)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Function	R/W
b0	—	Transmit data	W
b1	—		
b2	—		
b3	—		
b4	—		
b5	—		
b6	—		
b7	—		
b8	—		
b9	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.	—
b10	—		
b11	—		
b12	—		
b13	—		
b14	—		
b15	—		

If the transfer data is 9 bits long, write data to the high-order byte first, then low-order byte of the UiTB register. Use the MOV instruction to write to this register.

24.2.4 UARTi Transmit/Receive Control Register 0 (UiC0) (i = 0 or 1)

Address 00A4h (U0C0), 0164h (U1C0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	UFORM	CKPOL	NCH	—	TXEPT	—	CLK1	CLK0
After Reset	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CLK0	BRG count source select bit (1)	b1 b0 0 0: f1 selected 0 1: f8 selected 1 0: f32 selected 1 1: Do not use.	R/W
b1	CLK1			R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	TXEPT	Transmit register empty flag	0: Data present in the transmit register (transmission in progress) 1: No data in the transmit register (transmission completed)	R
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	NCH	Data output select bit	0: TXDi pin set to CMOS output 1: TXDi pin set to N-channel open-drain output	R/W
b6	CKPOL	CLK polarity select bit	0: Transmit data output at the falling edge and receive data input at the rising edge of the transfer clock 1: Transmit data output at the rising edge and receive data input at the falling edge of the transfer clock	R/W
b7	UFORM	Transfer format select bit	0: LSB first 1: MSB first	R/W

Note:
1. If the BRG count source is switched, set the UiBRG register again.

24.2.5 UARTi Transmit/Receive Control Register 1 (UiC1) (i = 0 or 1)

Address 00A5h (U0C1), 0165h (U1C1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	UiRRM	UiIRS	RI	RE	TI	TE
After Reset	0	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	TE	Transmit enable bit	0: Transmission disabled 1: Transmission enabled	R/W
b1	TI	Transmit buffer empty flag	0: Data present in the UiTB register 1: No data in the UiTB register	R
b2	RE	Receive enable bit	0: Reception disabled 1: Reception enabled	R/W
b3	RI	Receive complete flag (1)	0: No data in the UiRB register 1: Data present in the UiRB register	R
b4	UiIRS	UARTi transmit interrupt source select bit	0: Transmission buffer empty (TI = 1) 1: Transmission completed (TXEPT = 1)	R/W
b5	UiRRM	UARTi continuous receive mode enable bit (2)	0: Continuous receive mode disabled 1: Continuous receive mode enabled	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

Notes:
1. The RI bit is set to 0 when the higher byte of the UiRB register is read.
2. In UART mode, set the UiRRM bit to 0 (continuous receive mode disabled).

24.2.6 UARTi Receive Buffer Register (UiRB) (i = 0 or 1)

Address 00A7h to 00A6h (U0RB), 0167h to 0166h (U1RB)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	SUM	PER	FER	OER	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	—	—	Receive data (D7 to D0)	R
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			
b8	—	—	Receive data (D8)	R
b9	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b10	—			
b11	—			
b12	OER	Overrun error flag (1)	0: No overrun error 1: Overrun error	R
b13	FER	Framing error flag (1, 2)	0: No framing error 1: Framing error	R
b14	PER	Parity error flag (1, 2)	0: No parity error 1: Parity error	R
b15	SUM	Error sum flag (1, 2)	0: No error 1: Error	R

Notes:
1. Bits SUM, PER, FER, and OER are set to 0 (no error) when either of the following is set:
   - Bits SMD2 to SMD0 in the UiMR register are set to 000b (serial interface disabled), or
   - The RE bit in the UiC1 register is set to 0 (reception disabled)

   The SUM bit is set to 0 (no error) when all of bits PER, FER, and OER are set to 0 (no error).
   Bits PER and FER are also set to 0 when the high-order byte of the UiRB register is read.
   When setting bits SMD2 to SMD0 in the UiMR register to 000b, set the TE bit in the UiC1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
2. These error flags are invalid when bits SMD2 to SMD0 in the UiMR register are set to 001b (clock synchronous serial I/O mode). When read, the content is undefined.

Always read the UiRB register in 16-bit units.

24.2.7 UART0 Pin Select Register (U0SR)

Address 0188h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	CLK0SEL0	—	RXD0SEL0	—	TXD0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TXD0SEL0	TXD0 pin select bit	0: TXD0 pin not used 1: P1_4 assigned	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	RXD0SEL0	RXD0 pin select bit	0: RXD0 pin not used 1: P1_5 assigned	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	CLK0SEL0	CLK0 pin select bit	0: CLK0 pin not used 1: P1_6 assigned	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	—			
b7	—			

The U0SR register selects which pin is assigned to the UART0 I/O. To use the I/O pin for UART0, set this register.
Set the U0SR register before setting the UART0 associated registers. Also, do not change the setting value in this register during UART0 operation.

24.2.8 UART1 Pin Select Register (U1SR)

Address 0189h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	CLK1SEL1	CLK1SEL0	RXD1SEL1	RXD1SEL0	TXD1SEL1	TXD1SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TXD1SEL0	TXD1 pin select bit	b1 b0 0 0: TXD1 pin not used 0 1: P0_1 assigned 1 0: P6_3 assigned 1 1: Do not set.	R/W
b1	TXD1SEL1			R/W
b2	RXD1SEL0	RXD1 pin select bit	b3 b2 0 0: RXD1 pin not used 0 1: P0_2 assigned 1 0: P6_4 assigned 1 1: Do not set.	R/W
b3	RXD1SEL1			R/W
b4	CLK1SEL0	CLK1 pin select bit	b5 b4 0 0: CLK1 pin not used 0 1: P0_3 assigned 1 0: Do not set. 1 1: P6_5 assigned	R/W
b5	CLK1SEL1			R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

The U1SR register selects which pin is assigned to the UART1 I/O. To use the I/O pin for UART1, set this register.
Set the U1SR register before setting the UART1 associated registers. Also, do not change the setting value in this register during UART1 operation.

24.3 Clock Synchronous Serial I/O Mode

In clock synchronous serial I/O mode, data is transmitted and received using a transfer clock.
Table 24.2 lists the Clock Synchronous Serial I/O Mode Specifications. Table 24.3 lists the Registers Used and Settings in Clock Synchronous Serial I/O Mode.

Table 24.2 Clock Synchronous Serial I/O Mode Specifications

Item	Specification
Transfer data format	• Transfer data length: 8 bits
Transfer clocks	• The CKDIR bit in the UiMR register is set to 0 (internal clock): fi/(2(n+1)) fi = f1, f8, f32 n = setting value in the UiBRG register: 00h to FFh • The CKDIR bit is set to 1 (external clock): Input from the CLKi pin
Transmit start conditions	• To start transmission, the following requirements must be met: (1) - The TE bit in the UiC1 register is set to 1 (transmission enabled). - The TI bit in the UiC1 register is set to 0 (data present in the UiTB register).
Receive start conditions	• To start reception, the following requirements must be met: (1) - The RE bit in the UiC1 register is set to 1 (reception enabled). - The TE bit in the UiC1 register is set to 1 (transmission enabled). - The TI bit in the UiC1 register is set to 0 (data present in the UiTB register).
Interrupt request generation timing	• For transmission: One of the following can be selected. - The UiIRS bit is set to 0 (transmit buffer empty): When data is transferred from the UiTB register to the UARTi transmit register (at start of transmission). - The UiIRS bit is set to 1 (transmission completed): When data transmission from the UARTi transmit register is completed. • For reception: When data is transferred from the UARTi receive register to the UiRB register (at completion of reception).
Error detection	• Overrun error (2) This error occurs if the serial interface starts receiving the next unit of data before reading the UiRB register and receives the 7th bit of the next unit of data.
Selectable functions	• CLK polarity selection Transfer data input/output can be selected to occur synchronously with the rising or the falling edge of the transfer clock. • LSB first, MSB first selection Whether transmitting or receiving data begins with bit 0 or begins with bit 7 can be selected. • Continuous receive mode selection Reception is enabled immediately by reading the UiRB register.

i = 0 or 1
Notes:
1. When an external clock is selected, the requirements must be met in either of the following states:
   - The external clock is held high when the CKPOL bit in the UiC0 register is set to 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock)
   - The external clock is held low when the CKPOL bit in the UiC0 register is set to 1 (transmit data output at the rising edge and receive data input at the falling edge of the transfer clock)
2. If an overrun error occurs, the receive data (b0 to b8) in the UiRB register will be undefined.
   The IR bit in the SiRIC register remains unchanged.

Table 24.3 Registers Used and Settings in Clock Synchronous Serial I/O Mode (1)

Register	Bit	Function
UiTB	b0 to b7	Set data transmission.
UiRB	b0 to b7	Receive data can be read.
	OER	Overrun error flag
UiBRG	b0 to b7	Set a bit rate.
UiMR	SMD2 to SMD0	Set to 001b.
	CKDIR	Select the internal clock or external clock.
UiC0	CLK1, CLK0	Select the count source for the UiBRG register.
	TXEPT	Transmit register empty flag
	NCH	Select TXDi pin output mode.
	CKPOL	Select the transfer clock polarity.
	UFORM	Select LSB first or MSB first.
UiC1	TE	Set to 1 to enable transmission/reception
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Receive complete flag
	UiIRS	Select the UARTi transmit interrupt source.
	UiRRM	Set to 1 to use continuous receive mode.

i = 0 or 1

Note:

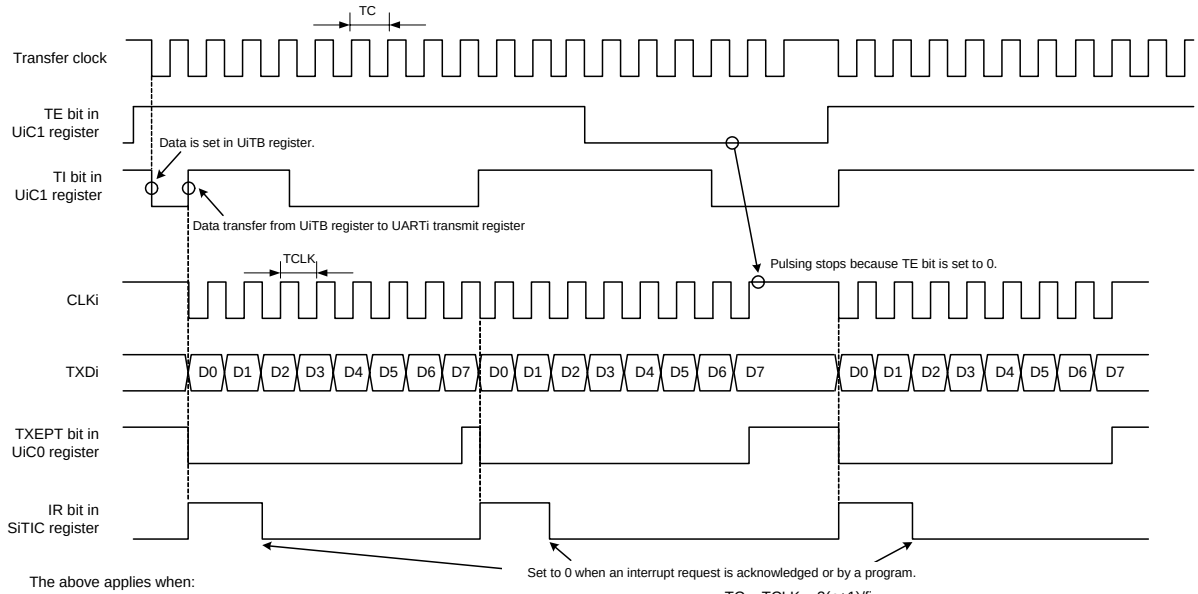
1. Set the bits not listed in this table to 0 when writing to the above registers in clock synchronous serial I/O mode.

Table 24.4 lists the I/O Pin Functions in Clock Synchronous Serial I/O Mode.
After UARTi (i = 0 or 1) operating mode is selected, the TXDi pin outputs a “H” level until transfer starts. (If the NCH bit is set to 1 (N-channel open-drain output), this pin is in the high-impedance state.)

Table 24.4 I/O Pin Functions in Clock Synchronous Serial I/O Mode

Pin Name	Function	Selection Method
TXD0 (P1_4)	Serial data output	TXD0SEL0 bit in U0SR register = 1 For reception only: P1_4 can be used as a port by setting TXD0SEL0 bit = 0.
RXD0 (P1_5)	Serial data input	RXD0SEL0 bit in U0SR register = 1 PD1_5 bit in PD1 register = 0 For transmission only: P1_5 can be used as a port by setting RXD0SEL0 bit = 0.
CLK0 (P1_6)	Transfer clock output	CLK0SEL0 bit in U0SR register = 1 CKDIR bit in U0MR register = 0
	Transfer clock input	CLK0SEL0 bit in U0SR register = 1 CKDIR bit in U0MR register = 1 PD1_6 bit in PD1 register = 0
TXD1 (P0_1 or P6_3)	Serial data output	• TXD1 (P0_1) Bits TXD1SEL1 to TXD1SEL0 in U1SR register = 01b (P0_1) • TXD1 (P6_3) Bits TXD1SEL1 to TXD1SEL0 in U1SR register = 10b (P6_3) • For reception only, P0_1 and P6_3 can be used as a port by setting bits TXD1SEL1 to TXD1SEL0 = 00b.
RXD1 (P0_2 or P6_4)	Serial data input	• RXD1 (P0_2) Bits RXD1SEL1 to RXD1SEL0 in U1SR register = 01b (P0_2) PD0_2 bit in PD0 register = 0 • RXD1 (P6_4) Bits RXD1SEL1 to RXD1SEL0 in U1SR register = 10b (P6_4) PD6_4 bit in PD6 register = 0 • For transmission only, P0_2 and P6_4 can be used as a port by setting bits RXD1SEL1 to RXD1SEL0 = 00b.
CLK1 (P0_3 or P6_5)	Transfer clock output	• CLK1 (P0_3) Bits CLK1SEL1 to CLK1SEL0 in U1SR register = 01b (P0_3) CKDIR bit in U1MR register = 0 • CLK1 (P6_5) Bits CLK1SEL1 to CLK1SEL0 in U1SR register = 11b (P6_5) CKDIR bit in U1MR register = 0
	Transfer clock input	• CLK1 (P0_3) Bits CLK1SEL1 to CLK1SEL0 in U1SR register = 01b (P0_3) CKDIR bit in U1MR register = 1 PD0_3 bit in PD0 register = 0 • CLK1 (P6_5) Bits CLK1SEL1 to CLK1SEL0 in U1SR register = 11b (P6_5) CKDIR bit in U1MR register = 1 PD6_5 bit in PD6 register = 0

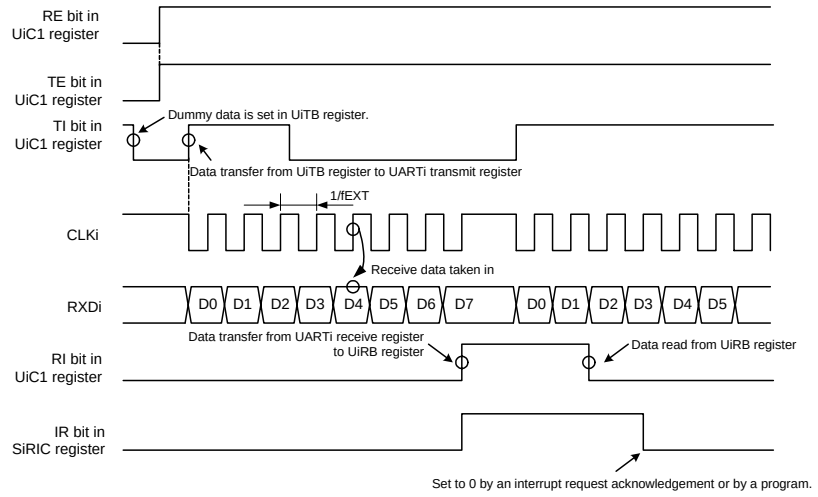
• Transmit Timing Example (Internal Clock Selected)



The above applies when:
- CKDIR bit in UiMR register = 0 (internal clock)
- CKPOL bit in UiC0 register = 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock)
- UiIRS bit in UiC1 register = 0 (interrupt request generation when the transmit buffer is empty)

TC = TCLK = 2(n+1)/fi
fi: Frequency of UiBRG count source (f1, f8, f32)
n: Setting value in UiBRG register

• Receive Timing Example (External Clock Selected)



The above applies when:
- CKDIR bit in UiMR register = 1 (external clock)
- CKPOL bit in UiC0 register = 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock)

The following should be met when “H” is applied to the CLKi pin before receiving data:
- TE bit in UiC1 register = 1 (transmission enabled)
- RE bit in UiC1 register = 1 (reception enabled)
- Dummy data is written to UiTB register

fEXT: Frequency of external clock

i = 0 or 1

Figure 24.3 Transmit and Receive Timing in Clock Synchronous Serial I/O Mode

24.3.1 Measure for Dealing with Communication Errors

If communication is aborted or a communication error occurs while transmitting or receiving in clock synchronous serial I/O mode, follow the procedures below:

(1) Set the TE bit in the UiC1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
(2) Set bits SMD2 to SMD0 in the UiMR register to 000b (serial interface disabled).
(3) Set bits SMD2 to SMD0 in the UiMR register to 001b (clock synchronous serial I/O mode).
(4) Set the TE bit in the UiC1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).

24.3.2 Polarity Select Function

Figure 24.4 shows the Transfer Clock Polarity. Use the CKPOL bit in the UiC0 (i = 0 or 1) register to select the transfer clock polarity.

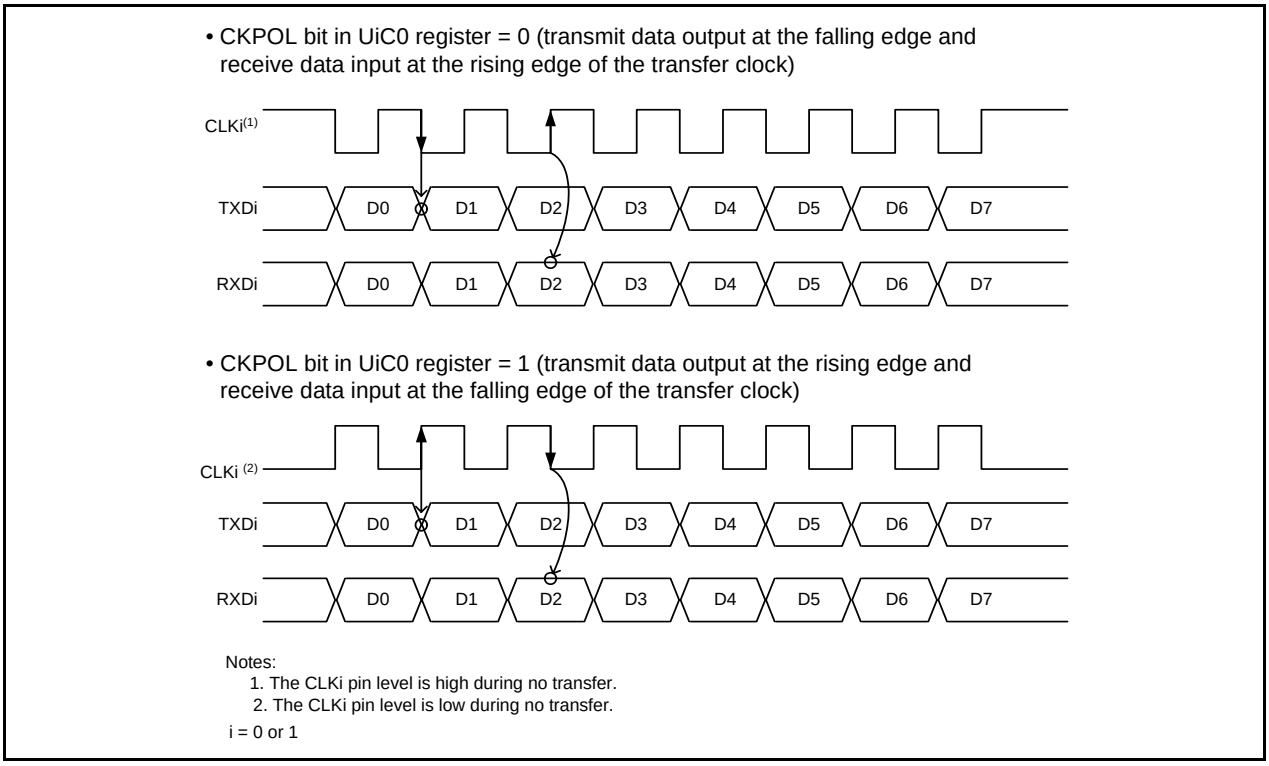


Figure 24.4 Transfer Clock Polarity

24.3.3 LSB First/MSB First Select Function

Figure 24.5 shows the Transfer Format. Use the UFORM bit in the UiC0 (i = 0 to 1) register to select the transfer format.

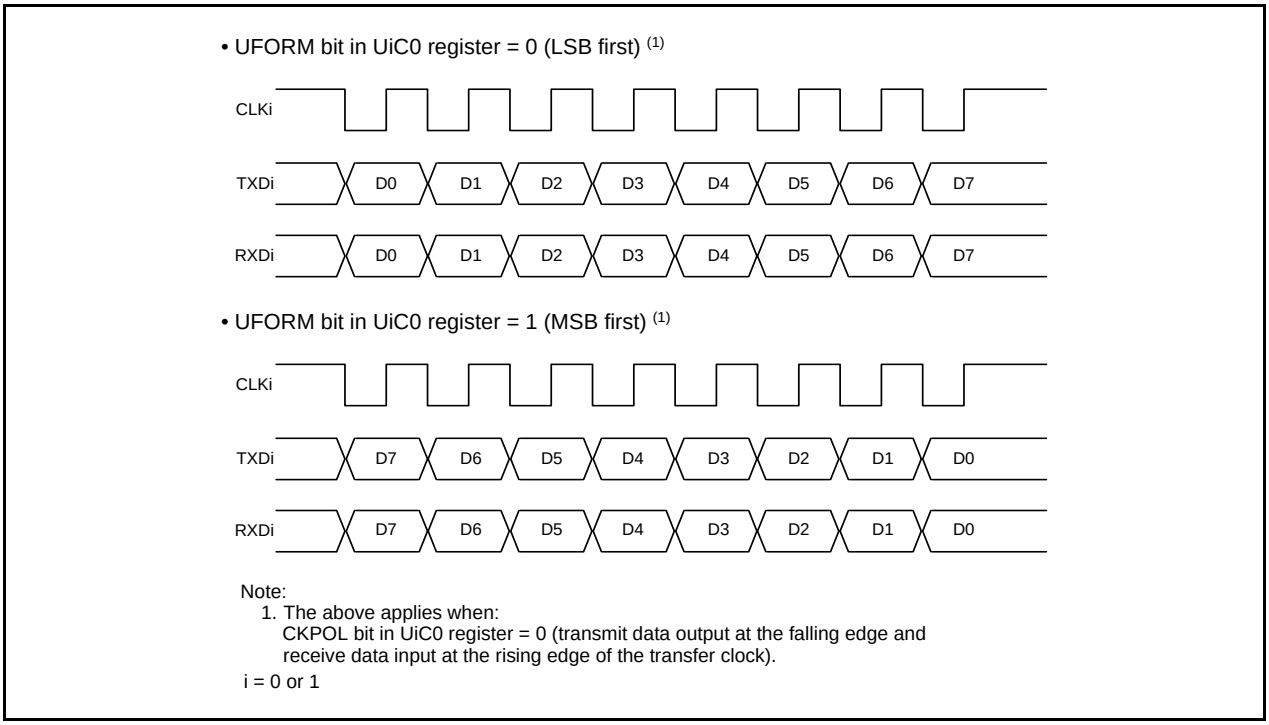


Figure 24.5 Transfer Format

24.3.4 Continuous Receive Mode

Continuous receive mode is selected by setting the UiRRM bit in the UiC1 register (i = 0 or 1) to 1 (continuous receive mode enabled). In this mode, reading the UiRB register sets the TI bit in the UiC1 register to 0 (data present in the UiTB register). If the UiRRM bit is set to 1, do not write dummy data to the UiTB register by a program.

24.4 Clock Asynchronous Serial I/O (UART) Mode

The UART mode allows data transmission and reception after setting the desired bit rate and transfer data format. Table 24.5 lists the UART Mode Specifications. Table 24.6 lists the Registers Used and Settings in UART Mode.

Table 24.5 UART Mode Specifications

Item	Specification
Transfer data formats	• Character bits (transfer data): Selectable among 7, 8 or 9 bits • Start bit: 1 bit • Parity bit: Selectable among odd, even, or none • Stop bits: Selectable among 1 or 2 bits
Transfer clocks	• The CKDIR bit in the UiMR register is set to 0 (internal clock): fj/(16(n+1)) fj = f1, f8, f32 n = setting value in the UiBRG register: 00h to FFh • The CKDIR bit is set to 1 (external clock): fEXT/(16(n+1)) fEXT: Input from the CLKi pin, n = setting value in the UiBRG register: 00h to FFh
Transmit start conditions	• To start transmission, the following requirements must be met: - The TE bit in the UiC1 register is set to 1 (transmission enabled). - The TI bit in the UiC1 register is set to 0 (data present in the UiTB register).
Receive start conditions	• To start reception, the following requirements must be met: - The RE bit in the UiC1 register is set to 1 (reception enabled). - Start bit detection
Interrupt request generation timing	• For transmission: One of the following can be selected. - The UiIRS bit is set to 0 (transmit buffer empty): When data is transferred from the UiTB register to the UARTi transmit register (at start of transmission). - The UiIRS bit is set to 1 (transfer completed): When data transmission from the UARTi transmit register is completed. • For reception: When data is transferred from the UARTi receive register to the UiRB register (at completion of reception).
Error detection	• Overrun error (1) This error occurs if the serial interface starts receiving the next unit of data before reading the UiRB register and receive the bit one before the last stop bit of the next unit of data. • Framing error This error occurs when the set number of stop bits is not detected. (2) • Parity error This error occurs when parity is enabled, and the number of 1's in the parity and character bits do not match the set number of 1's. (2) • Error sum flag This flag is set to 1 if an overrun, framing, or parity error occurs.

i = 0 or 1

Notes:

1. If an overrun error occurs, the receive data (b0 to b8) in the UiRB register will be undefined.
2. The framing error flag and the parity error flag are set to 1 when data is transferred from the UART0 receive register to the U0RB register.

Table 24.6 Registers Used and Settings in UART Mode

Register	Bit	Function
UiTB	b0 to b8	Set transmit data. (1)
UiRB	b0 to b8	Receive data can be read. (2)
	OER,FER,PER,SUM	Error flag
UiBRG	b0 to b7	Set a bit rate.
UiMR	SMD2 to SMD0	Set to 100b when transfer data is 7 bits long. Set to 101b when transfer data is 8 bits long. Set to 110b when transfer data is 9 bits long.
	CKDIR	Select the internal clock or external clock.
	STPS	Select the stop bit.
	PRY, PRYE	Select whether parity is included and whether odd or even.
UiC0	CLK0, CLK1	Select the count source for the UiBRG register.
	TXEPT	Transmit register empty flag
	NCH	Select TXDi pin output mode.
	CKPOL	Set to 0.
	UFORM	Select LSB first or MSB first when transfer data is 8 bits long. Set to 0 when transfer data is 7 bits or 9 bits long.
UiC1	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Receive complete flag
	UiIRS	Select the UARTi transmit interrupt source.
	UiRRM	Set to 0.

i = 0 or 1

Notes:

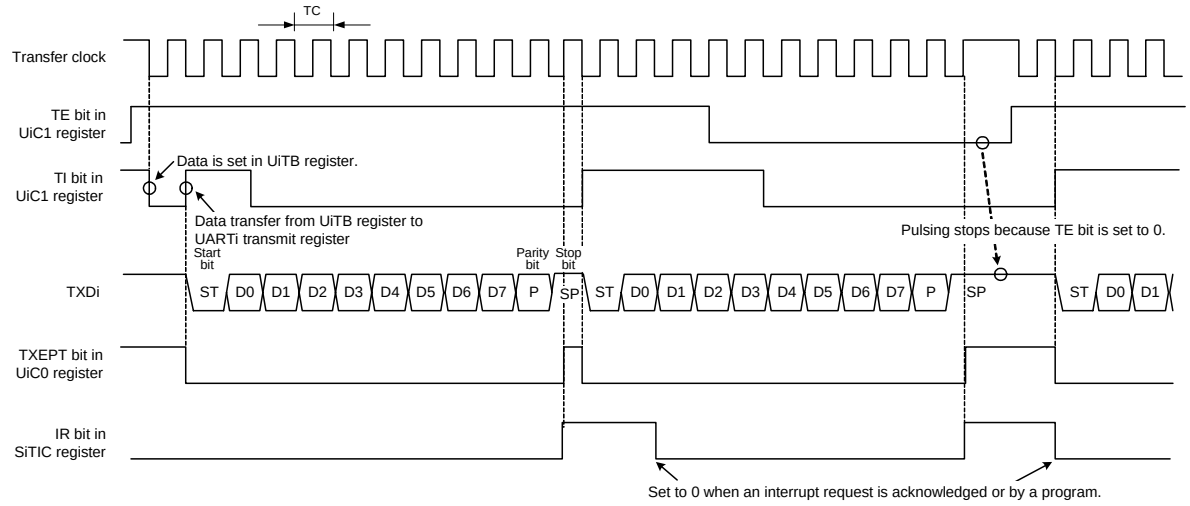
1. The bits used for transmission/receive data are as follows:
   - Bits b0 to b6 when transfer data is 7 bits long
   - Bits b0 to b7 when transfer data is 8 bits long
   - Bits b0 to b8 when transfer data is 9 bits long
2. The contents of the following are undefined:
   - Bits 7 and 8 when the transfer data is 7 bits long
   - Bit 8 when the transfer data is 8 bits long

Table 24.7 lists the I/O Pin Functions in UART Mode.
After the UARTi (i = 0 to 1) operating mode is selected, the TXDi pin outputs a “H” level until transfer starts. (If the NCH bit is set to 1 (N-channel open-drain output), this pin is in the high-impedance state.)

Table 24.7 I/O Pin Functions in UART Mode

Pin name	Function	Selection Method
TXD0 (P1_4)	Serial data output	TXD0SEL0 bit in U0SR register = 1 For reception only: P1_4 can be used as a port by setting TXD0SEL0 bit = 0.
RXD0 (P1_5)	Serial data input	RXD0SEL0 bit in U0SR register = 1 PD1_5 bit in PD1 register = 0 For transmission only: P1_5 can be used as a port by setting RXD0SEL0 bit = 0.
CLK0 (P1_6)	Programmable I/O port	CLK0SEL0 bit in U0SR register = 0 (CLK0 pin not used)
	Transfer clock input	CLK0SEL0 bit in U0SR register = 1 CKDIR bit in U0MR register = 1 PD1_6 bit in PD1 register = 0
TXD1 (P0_1 or P6_3)	Serial data output	• TXD1 (P0_1) Bits TXD1SEL1 to TXD1SEL0 in U1SR register = 01b (P0_1) • TXD1 (P6_3) Bits TXD1SEL1 to TXD1SEL0 in U1SR register = 10b (P6_3) • For reception only, P0_1 and P6_3 can be used as a port by setting bits TXD1SEL1 to TXD1SEL0 = 00b.
RXD1 (P0_2 or P6_4)	Serial data input	• RXD1 (P0_2) Bits RXD1SEL1 to RXD1SEL0 in U1SR register = 01b (P0_2) PD0_2 bit in PD0 register = 0 • RXD1 (P6_4) Bits RXD1SEL1 to RXD1SEL0 in U1SR register = 10b (P6_4)PD6_4 bit in PD6 register = 0 • For transmission only, P0_2 and P6_4 can be used as a port by setting bits RXD1SEL1 to RXD1SEL0 = 00b.
CLK1 (P0_3 or P6_5)	Programmable I/O port	Bits CLK1SEL1 to CLK1SEL0 in U1SR register = 00b (CLK1 pin not used)
	Transfer clock input	• CLK1 (P0_3) Bits CLK1SEL1 to CLK1SEL0 in U1SR register = 01b (P0_3) CKDIR bit in U1MR register = 1 PD0_3 bit in PD0 register = 0 • CLK1 (P6_5) Bits CLK1SEL1 to CLK1SEL0 in U1SR register = 11b (P6_5) CKDIR bit in U1MR register = 1 PD6_5 bit in PD6 register = 0

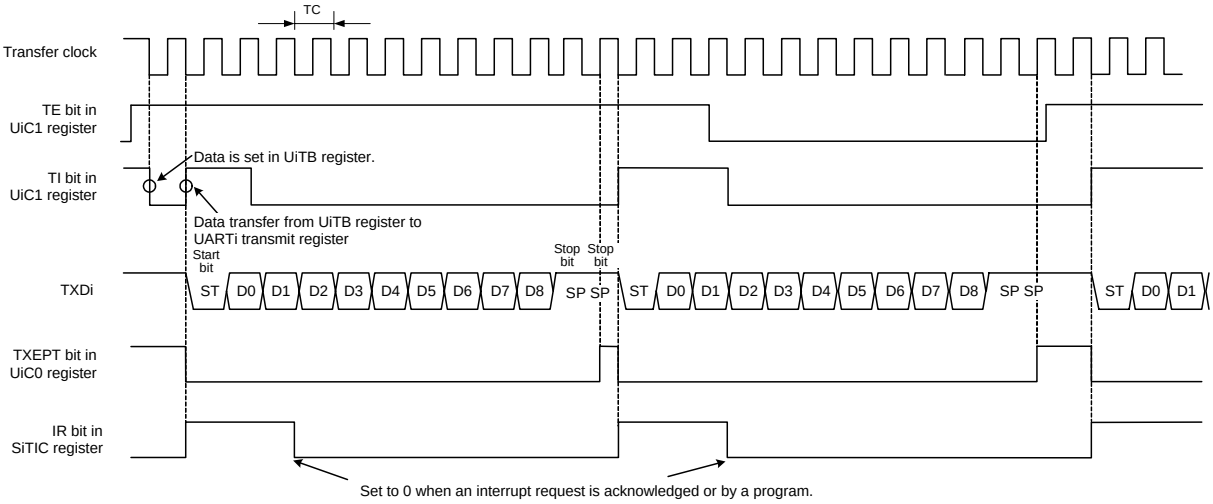
• Transmit Timing Example When Transfer Data is 8 Bits Long (Parity Enabled, One Stop Bit)



The above applies when:
- PRYE bit in UiMR register = 1 (parity enabled)
- STPS bit in UiMR register = 0 (one stop bit)
- UiIRS bit in UiC1 register = 1
  (interrupt request generation when transmission is completed)

TC = 16 (n + 1) / fj or 16 (n + 1) / fEXT
fj: Frequency of UiBRG count source (f1, f8, f32)
fEXT: Frequency of UiBRG count source (external clock)
n: Setting value in UiBRG register
i = 0 or 1

• Transmit Timing Example When Transfer Data is 9 Bits Long (Parity Disabled, Two Stop Bits)

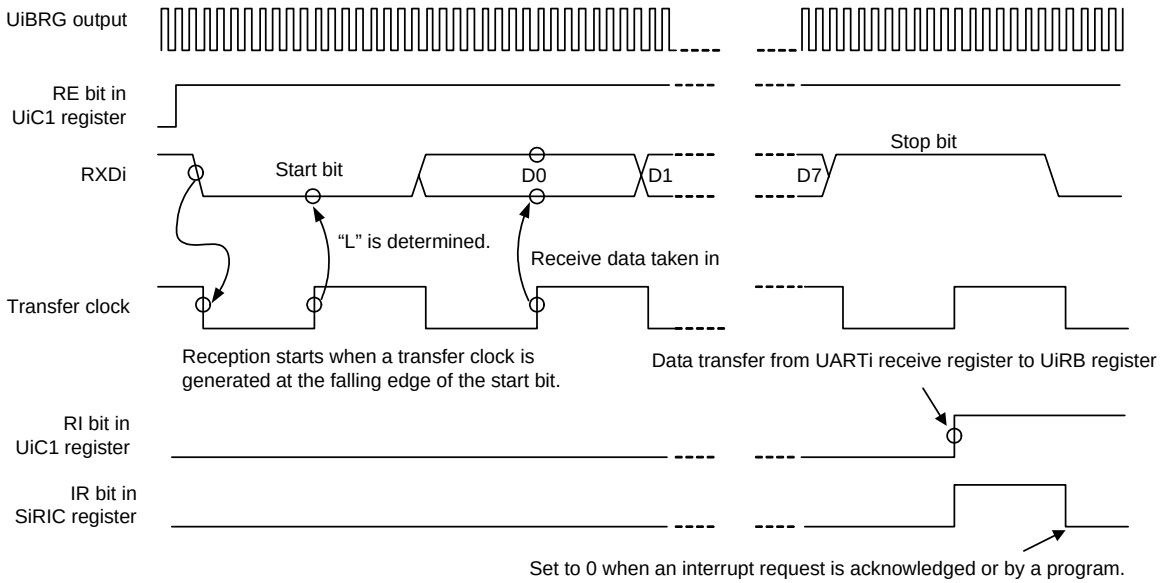


The above applies when:
- PRYE bit in UiMR register = 0 (parity disabled)
- STPS bit in UiMR register = 1 (two stop bits)
- UiIRS bit in UiC1 register = 0
  (interrupt request generation when the transmit buffer is empty)

TC = 16 (n + 1) / fj or 16 (n + 1) / fEXT
fj: Frequency of UiBRG count source (f1, f8, f32)
fEXT: Frequency of UiBRG count source (external clock)
n: Setting value in UiBRG register
i = 0 or 1

Figure 24.6 Transmit Timing in UART Mode

• Receive Timing Example When Transfer Data is 8 Bits Long (Parity Disabled, One Stop Bit)



The above applies when :
- PRYE bit in UiMR register = 0 (parity disabled)
- STPS bit in UiMR register = 0 (one stop bit)

i = 0 or 1

Figure 24.7 Receive Timing in UART Mode

24.4.1 Bit Rate

In UART mode, the bit rate is the frequency divided by the UiBRG (i = 0 or 1) register and divided by 16.

UART mode

• Internal clock selected

$$\text{Setting value in UiBRG register} = \frac{fj}{\text{Bit Rate} \times 16} - 1$$

fj: Count source frequency of UiBRG register (f1, f8, or f32)

• External clock selected

$$\text{Setting value in UiBRG register} = \frac{fEXT}{\text{Bit Rate} \times 16} - 1$$

fEXT: Count source frequency of UiBRG register (external clock)

i = 0 or 1

Figure 24.8 Formula for Calculating Setting Value in UiBRG (i = 0 or 1) Register

Table 24.8 Bit Rate Setting Example in UART Mode (Internal Clock Selected)

Bit Rate (bps)	UiBRG Count Source	System Clock = 20 MHz			System Clock = 18.432 MHz (1)			System Clock = 8 MHz		
		UiBRG Setting Value	Actual Time (bps)	Setting Error (%)	UiBRG Setting Value	Actual Time (bps)	Setting Error (%)	UiBRG Setting Value	Actual Time (bps)	Setting Error (%)
1200	f8	129 (81h)	1201.92	0.16	119 (77h)	1200.00	0.00	51 (33h)	1201.92	0.16
2400	f8	64 (40h)	2403.85	0.16	59 (3Bh)	2400.00	0.00	25 (19h)	2403.85	0.16
4800	f8	32 (20h)	4734.85	-1.36	29 (1Dh)	4800.00	0.00	12 (0Ch)	4807.69	0.16
9600	f1	129 (81h)	9615.38	0.16	119 (77h)	9600.00	0.00	51 (33h)	9615.38	0.16
14400	f1	86 (56h)	14367.82	-0.22	79 (4Fh)	14400.00	0.00	34 (22h)	14285.71	-0.79
19200	f1	64 (40h)	19230.77	0.16	59 (3Bh)	19200.00	0.00	25 (19h)	19230.77	0.16
28800	f1	42 (2Ah)	29069.77	0.94	39 (27h)	28800.00	0.00	16 (10h)	29411.76	2.12
38400	f1	32 (20h)	37878.79	-1.36	29 (1Dh)	38400.00	0.00	12 (0Ch)	38461.54	0.16
57600	f1	21 (15h)	56818.18	-1.36	19 (13h)	57600.00	0.00	8 (08h)	55555.56	-3.55
115200	f1	10 (0Ah)	113636.36	-1.36	9 (09h)	115200.00	0.00	–	–	–

i = 0 or 1

Note:

1. For the high-speed on-chip oscillator, the correction value in the FRA4 register should be written into the FRA1 register and the correction value in the FRA5 register should be written into the FRA3 register.
   This applies when the high-speed on-chip oscillator is selected as the system clock and bits FRA22 to FRA20 in the FRA2 register are set to 000b (divide-by-2 mode). For the precision of the high-speed on-chip oscillator, refer to **32. Electrical Characteristics**.

24.4.2 Measure for Dealing with Communication Errors

If communication is aborted or a communication error occurs while transmitting or receiving in UART mode, follow the procedures below:

(1) Set the TE bit in the UiC1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
(2) Set bits SMD2 to SMD0 in the UiMR register to 000b (serial interface disabled).
(3) Set bits SMD2 to SMD0 in the UiMR register to 100b (UART mode, transfer data 7 bits long), 101b (UART mode, transfer data 8 bits long), or 110b (UART mode, transfer data 9 bits long).
(4) Set the TE bit in the UiC1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).

24.5 Notes on Serial Interface (UARTi (i = 0 or 1))

- When reading data from the UiRB (i = 0 or 1) register either in clock synchronous serial I/O mode or in clock asynchronous serial I/O mode, always read data in 16-bit units.
  When the high-order byte of the UiRB register is read, bits PER and FER in the UiRB register and the RI bit in the UiC1 register are set to 0.
  To check receive errors, read the UiRB register and then use the read data.

  Program example to read the receive buffer register:
  ```
  MOV.W    00A6H,R0    ; Read the U0RB register
  ```

- When writing data to the UiTB register in clock asynchronous serial I/O mode with 9-bit transfer data length, write data to the high-order byte first and then the low-order byte, in 8-bit units.

  Program example to write to the transmit buffer register:
  ```
  MOV.B    #XXH,00A3H  ; Write to the high-order byte of the U0TB register
  MOV.B    #XXH,00A2H  ; Write to the low-order byte of the U0TB register
  ```

25. Serial Interface (UART2)

The serial interface consists of three channels, UART0 to UART2. This chapter describes the UART2.

25.1 Overview

UART2 has a dedicated timer to generate a transfer clock.
Figure 25.1 shows a UART2 Block Diagram. Figure 25.2 shows a Block Diagram of UART2 Transmit/Receive Unit. Table 25.1 lists the Pin Configuration of UART2.

UART2 has the following modes:

- Clock synchronous serial I/O mode
- Clock asynchronous serial I/O mode (UART mode)
- Special mode 1 (I^2C mode)
- Serial mode 3 (bus collision detection function, IE mode)
- Multiprocessor communication function

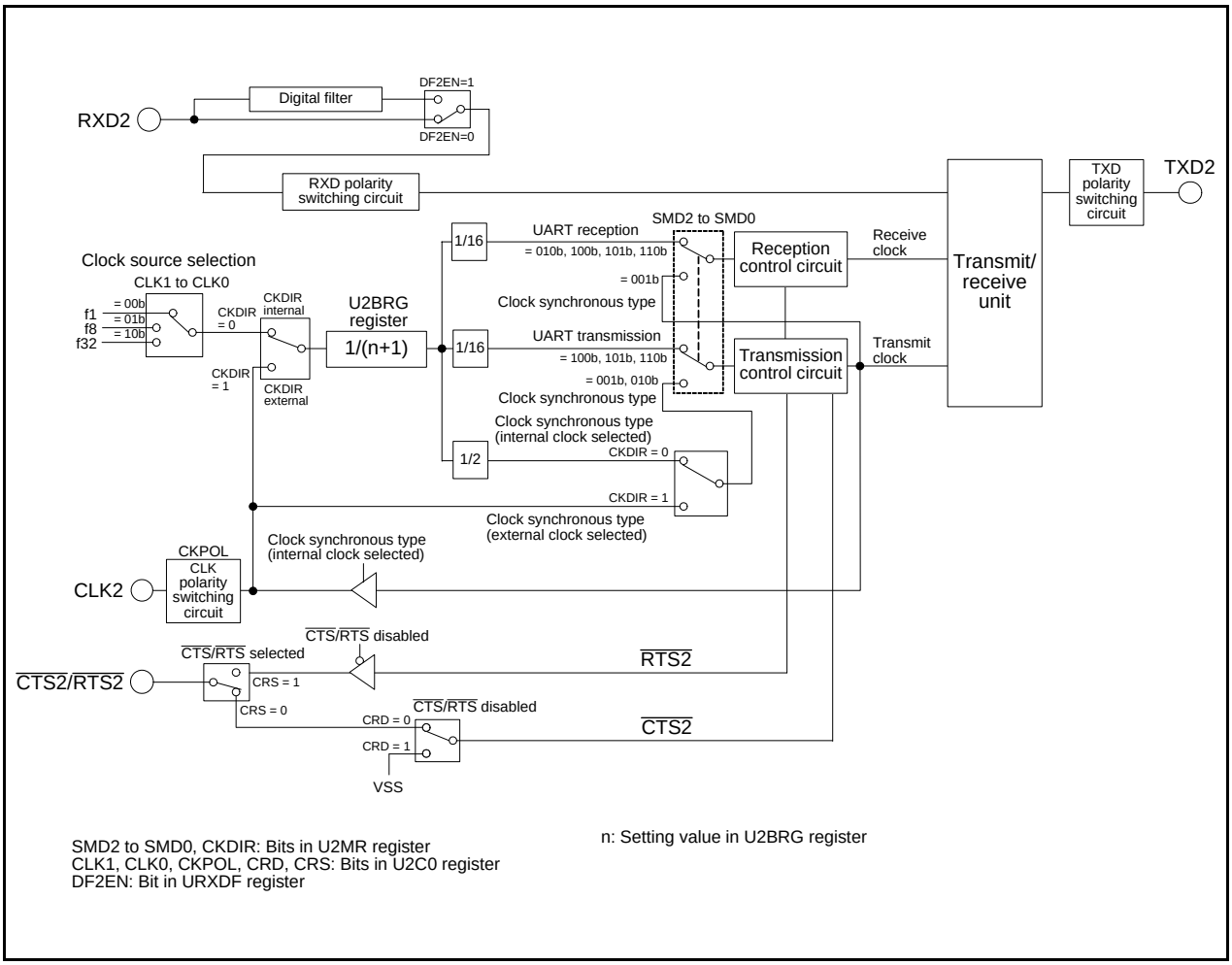


Figure 25.1 UART2 Block Diagram

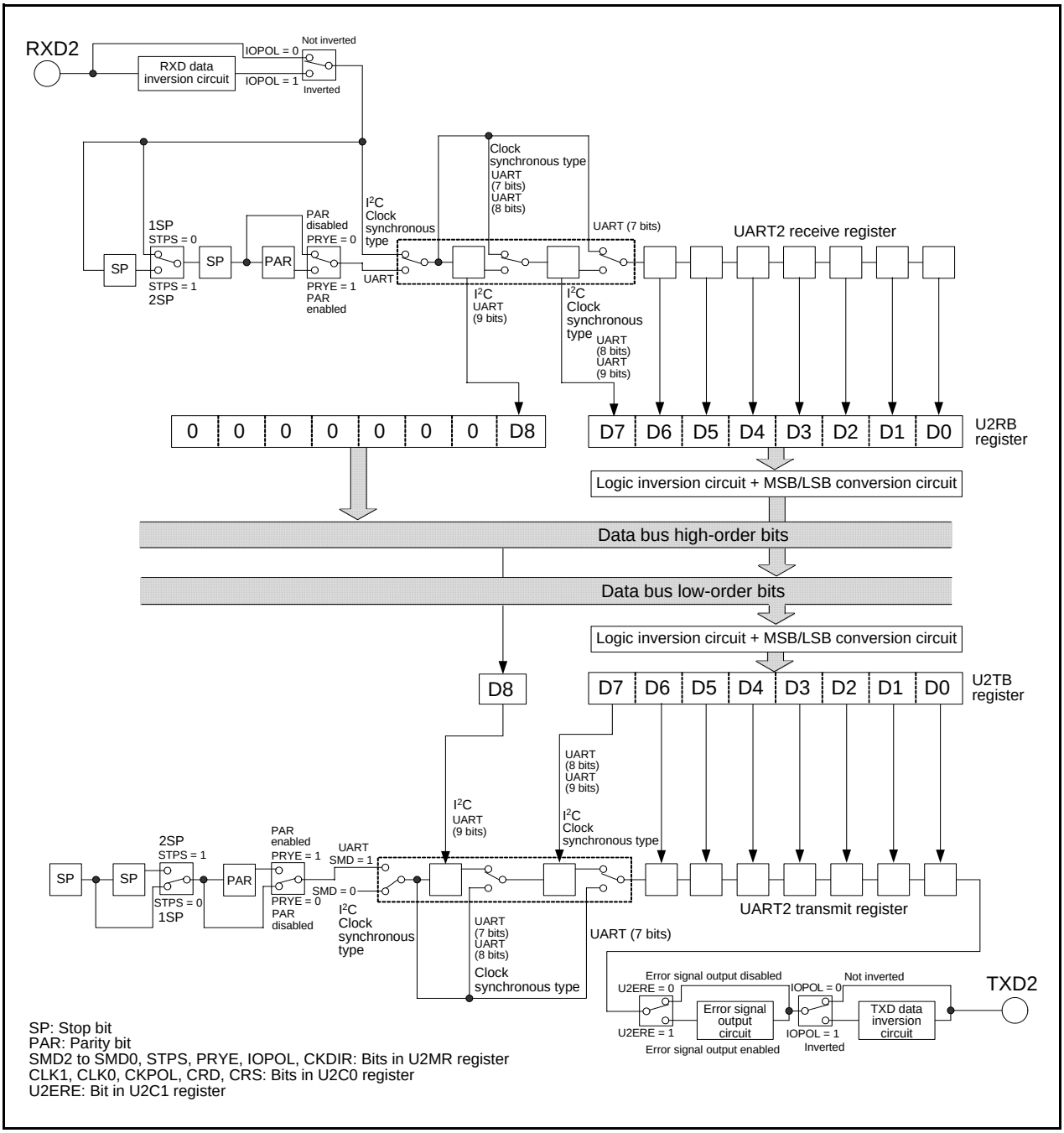


Figure 25.2 Block Diagram of UART2 Transmit/Receive Unit

Table 25.1 Pin Configuration of UART2

Pin Name	Assigned Pin	I/O	Function
TXD2	P3_4, P3_7, or P6_6	Output	Serial data output
RXD2	P3_4, P3_7, or P6_7	Input	Serial data input
CLK2	P3_5 or P6_5	I/O	Transfer clock I/O
$\overline{\text{CTS2}}$	P3_3	Input	Transmit control input
$\overline{\text{RTS2}}$	P3_3	Output	Receive control input
SCL2	P3_4, P3_7, or P6_7	I/O	I2C mode clock I/O
SDA2	P3_4, P3_7, or P6_6	I/O	I2C mode data I/O

25.2 Registers

25.2.1 UART2 Transmit/Receive Mode Register (U2MR)

Address 00A8h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IOPOL	PRYE	PRY	STPS	CKDIR	SMD2	SMD1	SMD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SMD0	Serial I/O mode select bit	b2 b1 b0 0 0 0: Serial interface disabled 0 0 1: Clock synchronous serial I/O mode 0 1 0: I²C mode 1 0 0: UART mode, transfer data 7 bits long 1 0 1: UART mode, transfer data 8 bits long 1 1 0: UART mode, transfer data 9 bits long Other than above: Do not set.	R/W
b1	SMD1			R/W
b2	SMD2			R/W
b3	CKDIR	Internal/external clock select bit	0: Internal clock 1: External clock	R/W
b4	STPS	Stop bit length select bit	0: One stop bit 1: Two stop bits	R/W
b5	PRY	Odd/even parity select bit	Enabled when PRYE = 1 0: Odd parity 1: Even parity	R/W
b6	PRYE	Parity enable bit	0: Parity disabled 1: Parity enabled	R/W
b7	IOPOL	TXD, RXD I/O polarity switch bit	0: Not inverted 1: Inverted	R/W

25.2.2 UART2 Bit Rate Register (U2BRG)

Address 00A9h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7 to b0	If the setting value is n, U2BRG divides the count source by n+1.	00h to FFh	W

Write to the U2BRG register while transmission and reception stop.
Use the MOV instruction to write to this register.
Set bits CLK1 to CLK0 in the U2C0 register before writing to the U2BRG register.

25.2.3 UART2 Transmit Buffer Register (U2TB)

Address 00ABh to 00AAh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	MPTB
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Function	R/W
b0	—	Transmit data (D7 to D0)	W
b1	—		
b2	—		
b3	—		
b4	—		
b5	—		
b6	—		
b7	—		
b8	MPTB	Transmit data (D8) (1) [When the multiprocessor communication function is not used] Transmit data (D8) [When the multiprocessor communication function is used] • To transfer an ID, set the MPTB bit to 1. • To transfer data, set the MPTB bit to 0.	W
b9	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.	—
b10	—		
b11	—		
b12	—		
b13	—		
b14	—		
b15	—		

Note:
1. Set bits b0 to b7 after setting the MPTB bit.

Use the MOV instruction to write to the UART2 transmit buffer register (U2TB). When the MP bit in the U2SMR5 register is 0 (multiprocessor communication disabled) and the transfer data length is 9 bits, write in 16-bit units or write to the higher byte first and then the lower byte in 8-bit units.

25.2.4 UART2 Transmit/Receive Control Register 0 (U2C0)

Address 00ACh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	UFORM	CKPOL	NCH	CRD	TXEPT	CRS	CLK1	CLK0
After Reset	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CLK0	U2BRG count source select bit (1)	b1 b0 0 0: f1 selected 0 1: f8 selected 1 0: f32 selected 1 1: Do not set.	R/W
b1	CLK1			R/W
b2	CRS	$\overline{\text{CTS}}$/$\overline{\text{RTS}}$ function select bit	Enabled when CRD = 0 0: $\overline{\text{CTS}}$ function selected 1: $\overline{\text{RTS}}$ function selected	R/W
b3	TXEPT	Transmit register empty flag	0: Data present in the transmit register (transmission in progress) 1: No data in the transmit register (transmission completed)	R
b4	CRD	$\overline{\text{CTS}}$/$\overline{\text{RTS}}$ disable bit	0: $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ function enabled 1: $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ function disabled	R/W
b5	NCH	Data output select bit	0: Pins TXD2/SDA2, SCL2 set to CMOS output 1: Pins TXD2/SDA2, SCL2 set to N-channel open-drain output	R/W
b6	CKPOL	CLK polarity select bit	0: Transmit data output at the falling edge and receive data input at the rising edge of the transfer clock 1: Transmit data output at the rising edge and receive data input at the falling edge of the transfer clock	R/W
b7	UFORM	Transfer format select bit (2)	0: LSB first 1: MSB first	R/W

Notes:
1. If bits CLK1 to CLK0 are switched, set the U2BRG register again.
2. The UFORM bit is enabled when bits SMD2 to SMD0 in the U2MR register are set to 001b (clock synchronous serial I/O mode), or set to 101b (UART mode, transfer data 8 bits long).
   Set the UFORM bit to 1 when bits SMD2 to SMD0 are set to 010b (I^2C mode), and to 0 when bits SMD2 to SMD0 are set to 100b (UART mode, transfer data 7 bits long) or 110b (UART mode, transfer data 9 bits long).

25.2.5 UART2 Transmit/Receive Control Register 1 (U2C1)

Address 00ADh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	U2ERE	U2LCH	U2RRM	U2IRS	RI	RE	TI	TE
After Reset	0	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	TE	Transmit enable bit	0: Transmission disabled 1: Transmission enabled	R/W
b1	TI	Transmit buffer empty flag	0: Data present in the U2TB register 1: No data in the U2TB register	R
b2	RE	Receive enable bit	0: Reception disabled 1: Reception enabled	R/W
b3	RI	Receive complete flag	0: No data in the U2RB register 1: Data present in the U2RB register	R
b4	U2IRS	UART2 transmit interrupt source select bit	0: Transmit buffer empty (TI = 1) 1: Transmission completed (TXEPT = 1)	R/W
b5	U2RRM	UART2 continuous receive mode enable bit	0: Continuous receive mode disabled 1: Continuous receive mode enabled	R/W
b6	U2LCH	Data logic select bit (1)	0: Not inverted 1: Inverted	R/W
b7	U2ERE	Error signal output enable bit	0: Output disabled 1: Output enabled	R/W

Note:

1. The U2LCH bit is enabled when bits SMD2 to SMD0 in the U2MR register are set to 001b (clock synchronous serial I/O mode), 100b (UART mode, transfer data 7 bits long), or 101b (UART mode, transfer data 8 bits long). Set the U2LCH bit to 0 when bits SMD2 to SMD0 are set to 010b (I^2C mode) or 110b (UART mode, transfer data 9 bits long).

25.2.6 UART2 Receive Buffer Register (U2RB)

Address 00AFh to 00AEh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	SUM	PER	FER	OER	—	—	—	MPRB
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	—	—	Receive data (D7 to D0)	R
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			
b8	MPRB	—	Receive data (D8) (1) [When the multiprocessor communication function is not used] Receive data (D8) [When the multiprocessor communication function is used] • When the MPRB bit is set to 0, received D0 to D7 are data fields. • When the MPRB bit is set to 1, received D0 to D7 are ID fields.	R
b9	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b10	—			
b11	—	Reserved bit	Set to 0.	R/W
b12	OER	Overrun error flag (1)	0: No overrun error 1: Overrun error	R
b13	FER	Framing error flag (1, 2)	0: No framing error 1: Framing error	R
b14	PER	Parity error flag (1, 2)	0: No parity error 1: Parity error	R
b15	SUM	Error sum flag (1, 2)	0: No error 1: Error	R

Notes:
1. When bits SMD2 to SMD0 in the U2MR register are set to 000b (serial interface disabled) or the RE bit in the U2C1 register is set to 0 (reception disabled), all of bits SUM, PER, FER, and OER are set to 0 (no error). The SUM bit is set to 0 (no error) when all of bits PER, FER, and OER are set to 0 (no error). Bits PER and FER are set to 0 by reading the lower byte of the U2RB register.
   When setting bits SMD2 to SMD0 in the U2MR register to 000b, set the TE bit in the U2C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
2. These error flags are disabled when bits SMD2 to SMD0 in the U2MR register are set to 001b (clock synchronous serial I/O mode) or to 010b (I^2C mode). When read, the content is undefined.

25.2.7 UART2 Digital Filter Function Select Register (URXDF)

Address 00B0h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	DF2EN	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	DF2EN	RXD2 digital filter enable bit (1)	0: RXD2 digital filter disabled 1: RXD2 digital filter enabled	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. The RXD2 digital filter can be used only in clock asynchronous serial I/O (UART) mode. When bits SMD2 to SMD0 in the U2MR register are set to 001b (clock synchronous serial I/O mode) or 010b (I^2C mode), set the DF2EN bit to 0 (RXD2 digital filter disabled).

25.2.8 UART2 Special Mode Register 5 (U2SMR5)

Address 00BBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	MPIE	—	—	—	MP
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	MP	Multiprocessor communication enable bit	0: Multiprocessor communication disabled 1: Multiprocessor communication enabled (1)	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	—			
b4	MPIE	Multiprocessor communication control bit	This bit is enabled when the MP bit is set to 1 (multiprocessor communication enabled). When the MPIE bit is set to 1, the following will result: • Receive data in which the multiprocessor bit is 0 is ignored. Setting of the RI bit in the U2C1 register and bits OER and FER in the U2RB register to 1 is disabled. • On receiving receive data in which the multiprocessor bit is 1, the MPIE bit is set to 0 and receive operation other than multiprocessor communication is performed.	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	—			
b7	—	Reserved bit	Set to 0.	R/W

Note:
1. When the MP bit is set to 1 (multiprocessor communication enabled), the settings of bits PRY and PRYE in the U2MR register are disabled. If bits SMD2 to SMD0 in the U2MR register are set to 001b (clock synchronous serial I/O mode), set the MP bit to 0 (multiprocessor communication disabled).

25.2.9 UART2 Special Mode Register 4 (U2SMR4)

Address 00BCh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SWC9	SCLHI	ACKC	ACKD	STSPSEL	STPREQ	RSTAREQ	STAREQ
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	STAREQ	Start condition generate bit (1)	0: Clear 1: Start	R/W
b1	RSTAREQ	Restart condition generate bit (1)	0: Clear 1: Start	R/W
b2	STPREQ	Stop condition generate bit (1)	0: Clear 1: Start	R/W
b3	STSPSEL	SCL, SDA output select bit	0: Start and stop conditions not output 1: Start and stop conditions output	R/W
b4	ACKD	ACK data bit	0: ACK 1: NACK	R/W
b5	ACKC	ACK data output enable bit	0: Serial interface data output 1: ACK data output	R/W
b6	SCLHI	SCL output stop enable bit	0: Disabled 1: Enabled	R/W
b7	SWC9	SCL wait bit 3	0: SCL “L” hold disabled 1: SCL “L” hold enabled	R/W

Note:
1. This bit is set to 0 when each condition is generated.

25.2.10 UART2 Special Mode Register 3 (U2SMR3)

Address 00BDh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DL2	DL1	DL0	—	NODC	—	CKPH	—
After Reset	0	0	0	X	0	X	0	X

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b1	CKPH	Clock phase set bit	0: No clock delay 1: With clock delay	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b3	NODC	Clock output select bit	0: CLK2 set to CMOS output 1: CLK2 set to N-channel open-drain output	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b5	DL0	SDA2 digital delay setup bit (1, 2)	b7 b6 b5 0 0 0: No delay 0 0 1: 1 to 2 cycle(s) of U2BRG count source 0 1 0: 2 to 3 cycles of U2BRG count source 0 1 1: 3 to 4 cycles of U2BRG count source 1 0 0: 4 to 5 cycles of U2BRG count source 1 0 1: 5 to 6 cycles of U2BRG count source 1 1 0: 6 to 7 cycles of U2BRG count source 1 1 1: 7 to 8 cycles of U2BRG count source	R/W
b6	DL1			R/W
b7	DL2			R/W

Notes:
1. Bits DL2 to DL0 are used to generate a delay in SDA2 output digitally in I^2C mode. In other than I^2C mode, set these bits to 000b (no delay).
2. The amount of delay varies with the load on pins SCL2 and SDA2. When an external clock is used, the amount of delay increases by about 100 ns.

25.2.11 UART2 Special Mode Register 2 (U2SMR2)

Address 00BEh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	SDHI	SWC2	STAC	—	SWC	CSC	IICM2
After Reset	X	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IICM2	I^2C mode select bit 2	Refer to **Table 25.12 I^2C Mode Functions**.	R/W
b1	CSC	Clock synchronization bit	0: Disabled 1: Enabled	R/W
b2	SWC	SCL wait output bit	0: Disabled 1: Enabled	R/W
b3	—	Reserved bit	Set to 0.	R/W
b4	STAC	UART2 initialization bit	0: Disabled 1: Enabled	R/W
b5	SWC2	SCL wait output bit 2	0: Transfer clock 1: “L” output	R/W
b6	SDHI	SDA output disable bit	0: Enabled 1: Disabled (high-impedance)	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—

25.2.12 UART2 Special Mode Register (U2SMR)

Address 00BFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	SSS	ACSE	ABSCS	—	BBS	—	IICM
After Reset	X	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IICM	I^2C mode select bit	0: Other than I^2C mode 1: I^2C mode	R/W
b1	—	Reserved bit	Set to 0.	R/W
b2	BBS	Bus busy flag (1)	0: Stop condition detected 1: Start condition detected (busy)	R/W
b3	—	Reserved bit	Set to 0.	R/W
b4	ABSCS	Bus collision detect sampling clock select bit	0: Rising edge of transfer clock 1: Underflow signal of Timer RB (2)	R/W
b5	ACSE	Auto clear function select bit of transmit enable bit	0: No auto clear function 1: Auto clear at bus collision occurrence	R/W
b6	SSS	Transmit start condition select bit	0: Not synchronized to RXD2 1: Synchronized to RXD2 (2)	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—

Notes:
1. The BBS bit is set to 0 by writing 0 by a program (Writing 1 has no effect).
2. When a transfer begins, the SSS bit is set to 0 (not synchronized to RXD2).

25.2.13 UART2 Pin Select Register 0 (U2SR0)

Address 018Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	RXD2SEL2	RXD2SEL1	RXD2SEL0	—	TXD2SEL2	TXD2SEL1	TXD2SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TXD2SEL0	TXD2/SDA2 pin select bit	b2 b1 b0 0 0 0: TXD2/SDA2 pin not used 0 0 1: P3_7 assigned 0 1 0: P3_4 assigned 1 0 1: P6_6 assigned Other than above: Do not set.	R/W
b1	TXD2SEL1			R/W
b2	TXD2SEL2			R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	RXD2SEL0	RXD2/SCL2 pin select bit	b6 b5 b4 0 0 0: RXD2/SCL2 pin not used 0 0 1: P3_4 assigned 0 1 0: P3_7 assigned 1 0 1: P6_7 assigned Other than above: Do not set.	R/W
b5	RXD2SEL1			R/W
b6	RXD2SEL2			R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

The U2SR0 register selects which pin is assigned to the UART2 I/O. To use the I/O pin for UART2, set this register.
Set the U2SR0 register before setting the UART2 associated registers. Also, do not change the setting value in this register during UART2 operation.

25.2.14 UART2 Pin Select Register 1 (U2SR1)

Address 018Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	CTS2SEL0	—	—	CLK2SEL1	CLK2SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CLK2SEL0	CLK2 pin select bit	b1 b0 0 0: CLK2 pin not used 0 1: P3_5 assigned 1 0: Do not set. 1 1: P6_5 assigned	R/W
b1	CLK2SEL1			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	CTS2SEL0	$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$ pin select bit	0: $\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$ pin not used 1: P3_3 assigned	R/W
b5	—	Reserved bit	Set to 0.	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

The U2SR1 register selects which pin is assigned to the UART2 I/O. To use the I/O pin for UART2, set this register.
Set the U2SR1 register before setting the UART2 associated registers. Also, do not change the setting value in this register during UART2 operation.

25.3 Clock Synchronous Serial I/O Mode

In clock synchronous serial I/O mode, data is transmitted and received using a transfer clock.
Table 25.2 lists the Clock Synchronous Serial I/O Mode Specifications. Table 25.3 lists the Registers Used and Settings in Clock Synchronous Serial I/O Mode.

Table 25.2 Clock Synchronous Serial I/O Mode Specifications

Item	Specification
Transfer data format	Transfer data length: 8 bits
Transfer clock	• The CKDIR bit in the U2MR register is set to 0 (internal clock): fj/(2(n+1)) fj = f1, f8, f32 n = setting value in the U2BRG register: 00h to FFh • The CKDIR bit is set to 1 (external clock): Input from the CLK2 pin
Transmit/receive control	Selectable from the $\overline{\text{CTS}}$ function, $\overline{\text{RTS}}$ function, or $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ function disabled.
Transmit start conditions	To start transmission, the following requirements must be met: (1) • The TE bit in the U2C1 register is set to 1 (transmission enabled) • The $\overline{\text{TI}}$ bit in the U2C1 register is set to 0 ($\overline{\text{data present}}$ in the U2TB register) • If the $\overline{\text{CTS}}$ function is selected, input to the $\overline{\text{CTS2}}$ pin = “L”.
Receive start conditions	To start reception, the following requirements must be met: (1) • The RE bit in the U2C1 register is set to 1 (reception enabled). • The TE bit in the U2C1 register is set to 1 (transmission enabled). • The TI bit in the U2C1 register is set to 0 (data present in the U2TB register).
Interrupt request generation timing	For transmission, one of the following conditions can be selected. • The U2IRS bit in the U2C1 register is set to 0 (transmit buffer empty): When data is transferred from the U2TB register to the UART2 transmit register (at start of transmission). • The U2IRS bit is set to 1 (transmission completed): When data transmission from the UART2 transmit register is completed. For reception • When data is transferred from the UART2 receive register to the U2RB register (at completion of reception).
Error detection	Overrun error (2) This error occurs if the serial interface starts receiving the next unit of data before reading the U2RB register and receives the 7th bit of the next unit of data.
Selectable functions	• CLK polarity selection Transfer data I/O can be selected to occur synchronously with the rising or falling edge of the transfer clock. • LSB first, MSB first selection Whether transmitting or receiving data begins with bit 0 or begins with bit 7 can be selected. • Continuous receive mode selection Reception is enabled immediately by reading the U2RB register. • Serial data logic switching This function inverts the logic value of the transmit/receive data.

Notes:
1. When an external clock is selected, the requirements must be met in either of the following states:
   - The external clock is held high when the CKPOL bit in the U2C0 register is set to 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock)
   - The external clock is held low when the CKPOL bit in the U2C0 register is set to 1 (transmit data output at the rising edge and receive data input at the falling edge of the transfer clock)
2. If an overrun error occurs, the receive data in the U2RB register will be undefined. The IR bit in the S2RIC register does not change to 1 (interrupt requested).

Table 25.3 Registers Used and Settings in Clock Synchronous Serial I/O Mode

Register	Bit	Function
U2TB (1)	b0 to b7	Set transmit data.
U2RB (1)	b0 to b7	Receive data can be read.
	OER	Overrun error flag
U2BRG	b0 to b7	Set a bit rate.
U2MR (1)	SMD2 to SMD0	Set to 001b.
	CKDIR	Select the internal clock or external clock.
	IOPOL	Set to 0.
U2C0	CLK1, CLK0	Select the count source for the U2BRG register.
	CRS	Select either $\overline{\text{CTS}}$ or $\overline{\text{RTS}}$ to use functions.
	TXEPT	Transmit register empty flag
	CRD	Enable or disable the $\overline{\text{CTS}}$ or $\overline{\text{RTS}}$ function.
	NCH	Select TXD2 pin output mode.
	CKPOL	Select the transfer clock polarity.
	UFORM	Select LSB first or MSB first.
U2C1	TE	Set to 1 to enable transmission/reception.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Receive complete flag
	U2IRS	Select the source of UART2 transmit interrupt.
	U2RRM	Set to 1 to use continuous receive mode.
	U2LCH	Set to 1 to use inverted data logic.
	U2ERE	Set to 0.
U2SMR	b0 to b7	Set to 0.
U2SMR2	b0 to b7	Set to 0.
U2SMR3	b0 to b2	Set to 0.
	NODC	Select clock output mode.
	b4 to b7	Set to 0.
U2SMR4	b0 to b7	Set to 0.
URXDF	DF2EN	Set to 0.
U2SMR5	MP	Set to 0.

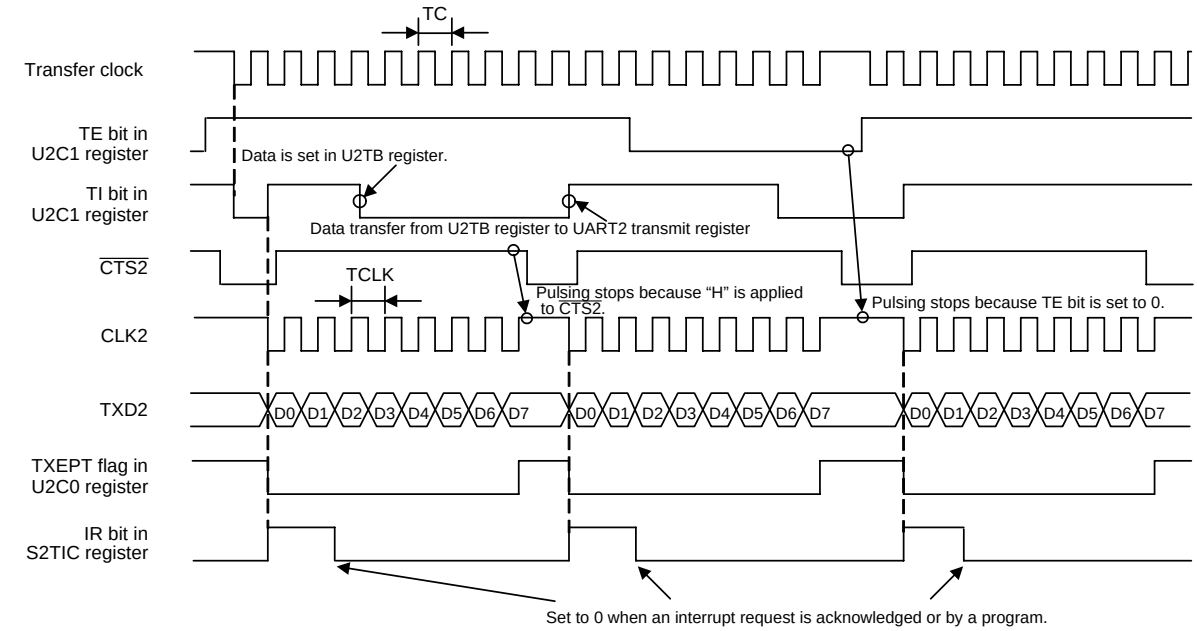
Note:
1. Set the bits not listed in this table to 0 when writing to the above registers in clock synchronous serial I/O mode.

Table 25.4 lists the Pin Functions in Clock Synchronous Serial I/O Mode (Multiple Transfer Clock Output Pin Function Not Selected).
Note that for a period from when UART2 operating mode is selected to when transfer starts, the TXD2 pin outputs a “H” level. (When N-channel open-drain output is selected, this pin is in the high-impedance state.)
Figure 25.3 shows the Transmit and Receive Timing in Clock Synchronous Serial I/O Mode.

Table 25.4 Pin Functions in Clock Synchronous Serial I/O Mode (Multiple Transfer Clock Output Pin Function Not Selected)

Pin Name	Function	Selection Method
TXD2 (P3_4, P3_7, or P6_6)	Serial data output	• When TXD2 (P3_4) TXD2SEL2 to TXD2SEL0 bits in U2SR0 register = 010b(P3_4) • When TXD2 (P3_7) TXD2SEL2 to TXD2SEL0 bits in U2SR0 register =001b(P3_7) • When TXD2 (P6_6) TXD2SEL2 to TXD2SEL0 bits in U2SR0 register =101b(P6_6) • For reception only: P3_4, P3_7, and P6_6 can be used as ports by setting bits TXD2SEL2 to TXD2SEL0 to 000b.
RXD2 (P3_4, P3_7, or P6_7)	Serial data input	• When RXD2 (P3_4) RXD2SEL2 to RXD2SEL0 bits in U2SR0 register =001b(P3_4) PD3_4 bit in PD3 register =0 • When RXD2 (P3_7) RXD2SEL2 to RXD2SEL0 bits in U2SR0 register =010b(P3_7) PD3_7 bit in PD3 register =0 • When RXD2 (P6_7) RXD2SEL2 to RXD2SEL0 bits in U2SR0 register =101b(P6_7) PD6_7 bit in PD6 register =0 • For transmission only: P3_4, P3_7, and P6_7 can be used as ports by setting bits RXD2SEL2 to RXD2SEL0 to 00b.
CLK2 (P3_5 or P6_5)	Transfer clock output	• When CLK2 (P3_5) CLK2SEL1, CLK2SEL0 bit in U2SR1 register =01b(P3_5) CKDIR bit in U2MR register =0 • When CLK2 (P6_5) CLK2SEL1, CLK2SEL0 bit in U2SR1 register =11b(P6_5) CKDIR bit in U2MR register =0
	Transfer clock input	• When CLK2 (P3_5) CLK2SEL1, CLK2SEL0 bit in U2SR1 register =01b(P3_5) CKDIR bit in U2MR register =1 PD3_5 bit in PD3 register =0 • When CLK2 (P6_5) CLK2SEL1, CLK2SEL0 bit in U2SR1 register =11b(P6_5) CKDIR bit in U2MR register =1 PD6_5 bit in PD6 register =0
$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$(P3_3)	$\overline{\text{CTS}}$ input	CTS2SEL0 bit in U2SR1 register =1 CRD bit in U2C0 register =0 CRS bit in U2C0 register =0 PD3_3 bit in PD3 register =0
	$\overline{\text{RTS}}$ output	CTS2SEL0 bit in U2SR1 register =1 CRD bit in U2C0 register =0 CRS bit in U2C0 register =1
	I/O port	CTS2SEL0 bit in U2SR1 register =0

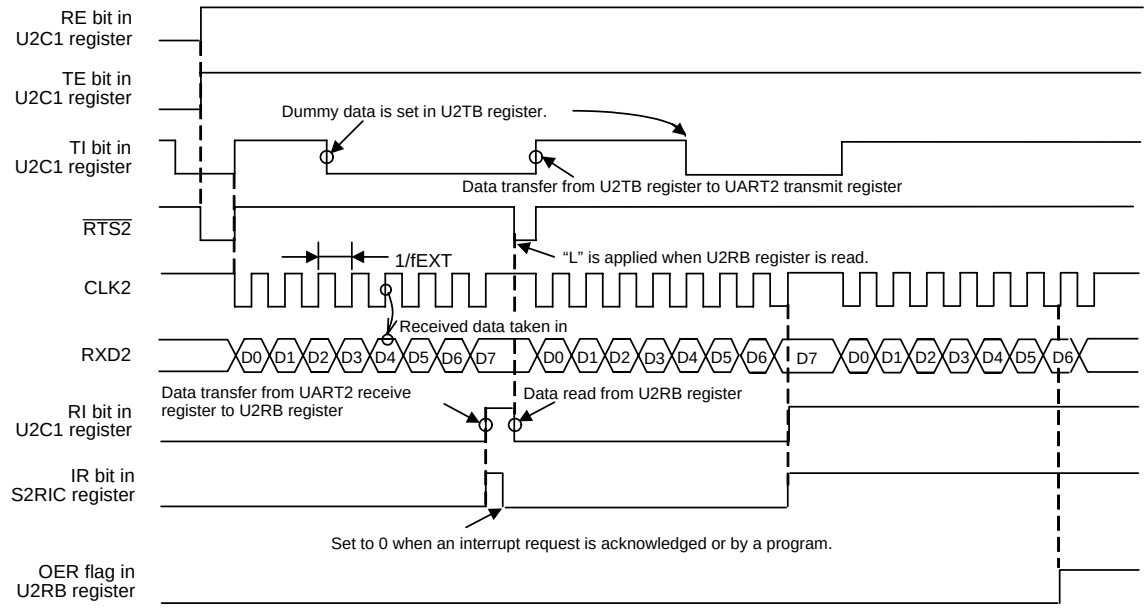
(1) Transmit Timing Example (Internal Clock Selected)



The above applies when:
- CKDIR bit in U2MR register = 0 (internal clock)
- CRD bit in U2C0 register = 0 (CTS/RTS function enabled), CRS bit = 0 (CTS function selected)
- CKPOL bit in U2C0 register = 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock)
- U2IRS bit in U2C1 register = 0 (interrupt request generation when the U2TB register is empty)

TC = TCLK = 2(n+1)/fj
fj: Frequency of U2BRG count source (f1, f8, f32)
n: Setting value in U2BRG register

(2) Receive Timing Example (External Clock Selected)



The above applies when:
- CKDIR bit in U2MR register = 1 (external clock)
- CRD bit in U2C0 register = 0 (CTS/RTS function enabled), CRS bit = 1 (RTS function selected)
- CKPOL bit in U2C0 register = 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock)

fEXT: Frequency of external clock

Make sure the following conditions are met when the CLK2 pin input before receiving data is high:
- TE bit in U2C0 register = 1 (transmission enabled)
- RE bit in U2C1 register = 1 (reception enabled)
- Dummy data is written to U2TB register

Figure 25.3 Transmit and Receive Timing in Clock Synchronous Serial I/O Mode

25.3.1 Measure for Dealing with Communication Errors

If communication is aborted or a communication error occurs while transmitting or receiving in clock synchronous serial I/O mode, follow the procedures below:

(1) Set the TE bit in the U2C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
(2) Set bits SMD2 to SMD0 in the U2MR register to 000b (serial interface disabled).
(3) Set bits SMD2 to SMD0 in the U2MR register to 001b (clock synchronous serial I/O mode).
(4) Set the TE bit in the U2C1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).

25.3.2 CLK Polarity Select Function

Use the CKPOL bit in the U2C0 register to select the transfer clock polarity. Figure 25.4 shows the Transfer Clock Polarity.

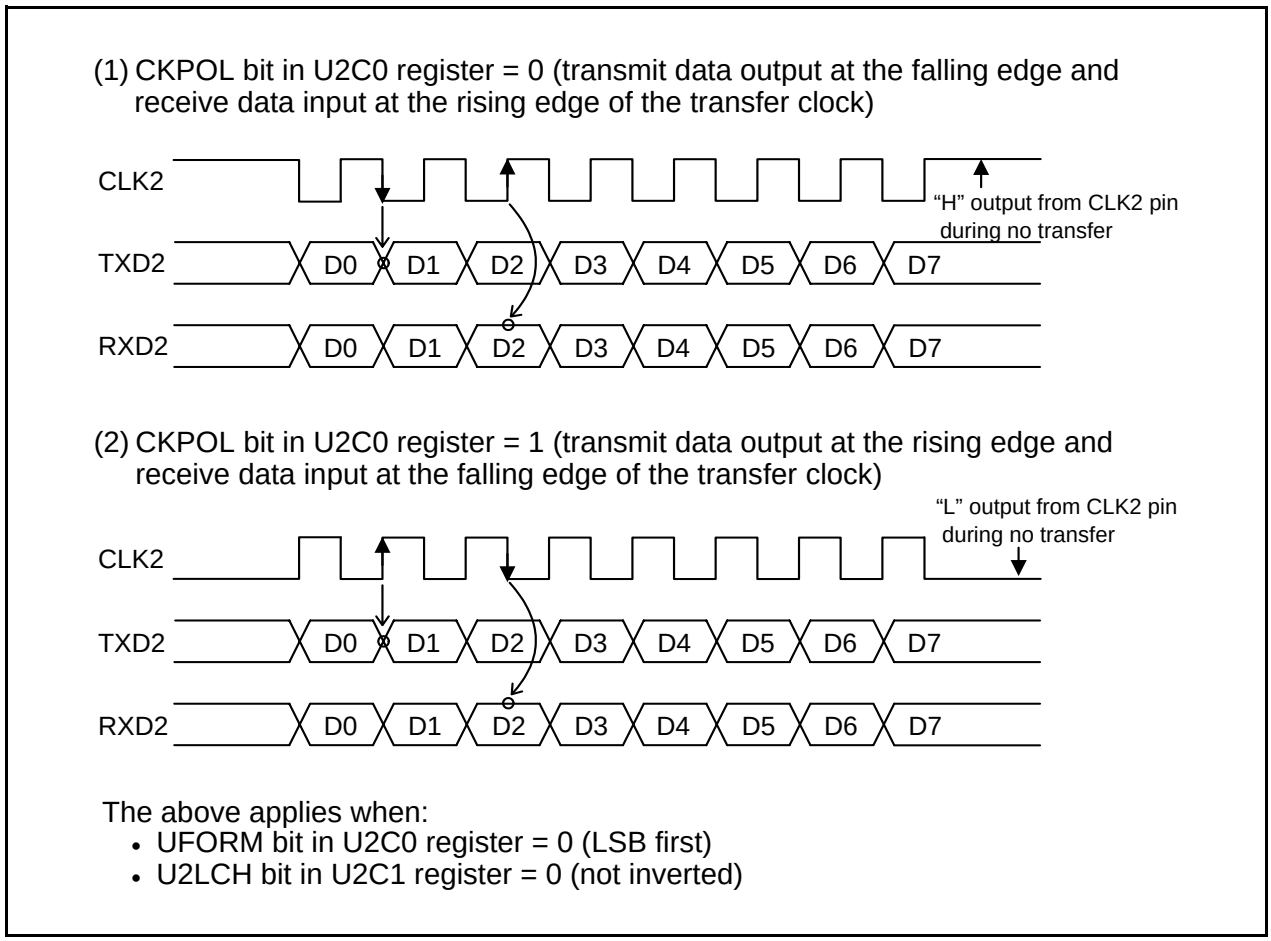


Figure 25.4 Transfer Clock Polarity

25.3.3 LSB First/MSB First Select Function

Use the UFORM bit in the U2C0 register to select the transfer format. Figure 25.5 shows the Transfer Format.

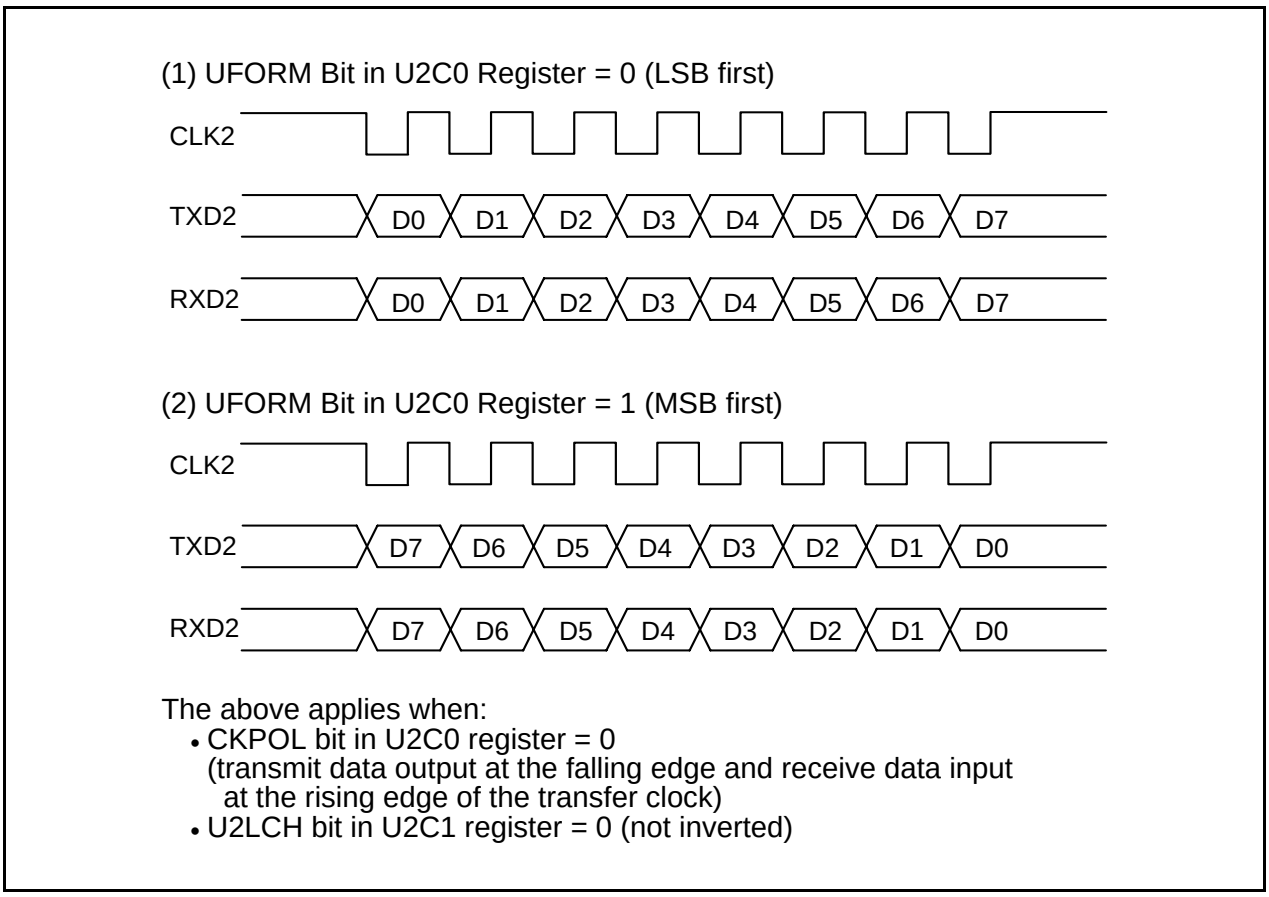


Figure 25.5 Transfer Format

25.3.4 Continuous Receive Mode

In continuous receive mode, receive operation is enabled when the receive buffer register is read. It is not necessary to write dummy data to the transmit buffer register to enable receive operation in this mode. However, a dummy read of the receive buffer register is required when starting the operating mode.

When the U2RRM bit in the U2C1 register is set to 1 (continuous receive mode), the TI bit in the U2C1 register is set to 0 (data present in the U2TB register) by reading the U2RB register. If the U2RRM bit is set to 1, do not write dummy data to the U2TB register by a program.

25.3.5 Serial Data Logic Switching Function

If the U2LCH bit in the U2C1 register is set to 1 (inverted), the data written to the U2TB register has its logic inverted before being transmitted. Similarly, the received data has its logic inverted when read from the U2RB register. Figure 25.6 shows the Serial Data Logic Switching.

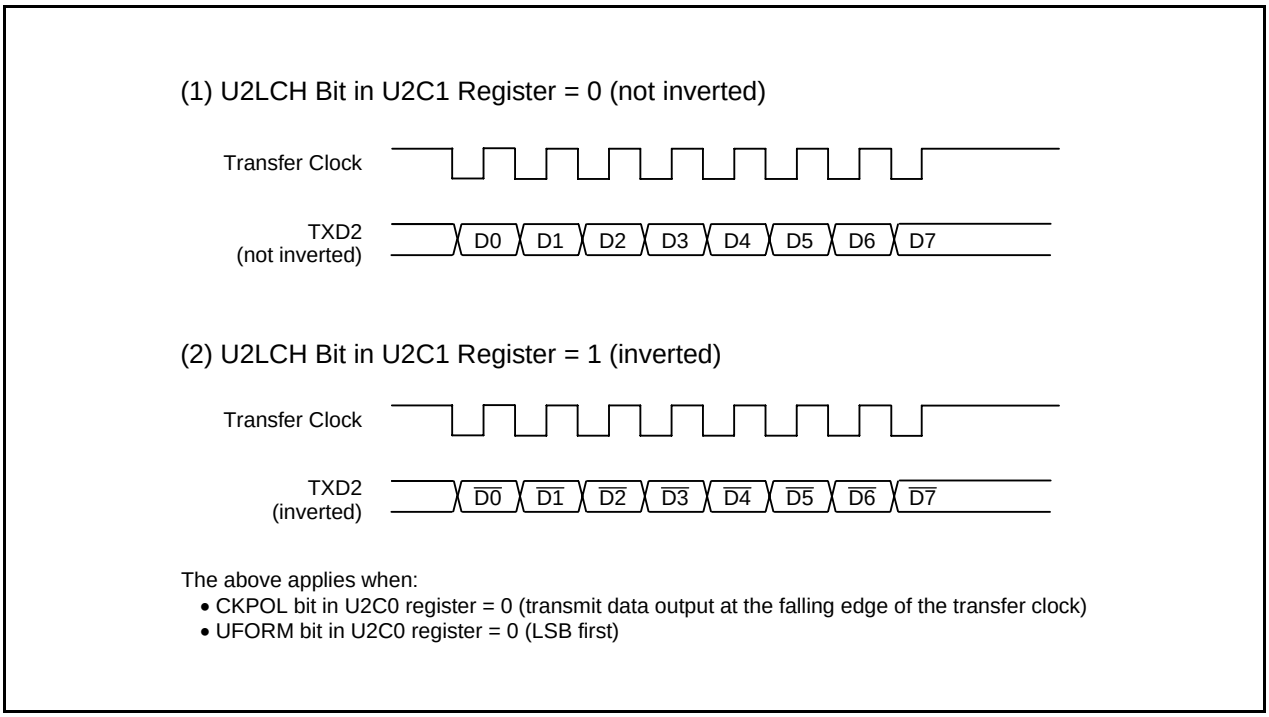


Figure 25.6 Serial Data Logic Switching

25.3.6 $\overline{\text{CTS}}/\overline{\text{RTS}}$ Function

The $\overline{\text{CTS}}$ function is used to start transmit and receive operation when "L" is applied to the $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin. Transmit and receive operation begins when the $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin is held low. If the "L" signal is switched to "H" during a transmit or receive operation, the operation stops before the next data.

For the $\overline{\text{RTS}}$ function, the $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin outputs "L" when the MCU is ready for a receive operation. The output level goes high at the first falling edge of the CLK2 pin.

- The CRD bit in the U2C0 register = 1 ($\overline{\text{CTS}}/\overline{\text{RTS}}$ function disabled)
  The $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin operates as the programmable I/O function.
- The CRD bit = 0, CRS bit = 0 ($\overline{\text{CTS}}$ function selected)
  The $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin operates as the $\overline{\text{CTS}}$ function.
- The CRD bit = 0, CRS bit = 1 ($\overline{\text{RTS}}$ function selected)
  The $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin operates as the $\overline{\text{RTS}}$ function.

25.4 Clock Asynchronous Serial I/O (UART) Mode

In UART mode, data is transmitted and received after setting the desired bit rate and transfer data format. Table 25.5 lists the UART Mode Specifications. Table 25.6 lists the Registers Used and Settings in UART Mode.

Table 25.5 UART Mode Specifications

Item	Specification
Transfer data format	• Character bits (transfer data): Selectable from 7, 8, or 9 bits • Start bit:1 bit • Parity bit: Selectable from odd, even, or none • Stop bits: Selectable from 1 bit or 2 bits
Transfer clock	• The CKDIR bit in the U2MR register is set to 0 (internal clock): fj/(16(n + 1)) fj = f1, f8, f32 n = setting value in the U2BRG register: 00h to FFh • The CKDIR bit is set to 1 (external clock): fEXT/(16(n + 1)) fEXT: Input from CLK2 pin n: Setting value in the U2BRG register: 00h to FFh
Transmit/receive control	Selectable from the $\overline{\text{CTS}}$ function, $\overline{\text{RTS}}$ function, or $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ function disabled.
Transmit start conditions	To start transmission, the following requirements must be met: • The TE bit in the U2C1 register is set to 1 (transmission enabled). • The TI bit in the U2C1 register is set to 0 (data present in the U2TB register). • If the $\overline{\text{CTS}}$ function is selected, input to the $\overline{\text{CTS2}}$ pin = “L”.
Receive start conditions	To start reception, the following requirements must be met: • The RE bit in the U2C1 register is set to 1 (reception enabled). • Start bit detection
Interrupt request generation timing	For transmission, one of the following conditions can be selected. • The U2IRS bit in the U2C1 register is set to 0 (transmit buffer empty): When data is transferred from the U2TB register to the UART2 transmit register (at start of transmission). • The U2IRS bit is set to 1 (transmission completed): When data transmission from the UART2 transmit register is completed. For reception • When data is transferred from the UART2 receive register to the U2RB register (at completion of reception).
Error detection	• Overrun error (1) This error occurs if the serial interface starts receiving the next unit of data before reading the U2RB register and receives the bit one before the last stop bit of the next unit of data. • Framing error (2) This error occurs when the set number of stop bits is not detected. • Parity error (2) This error occurs when if parity is enabled, the number of 1’s in the parity and character bits does not match the set number of 1’s. • Error sum flag This flag is set to 1 if an overrun, framing, or parity error occurs.
Selectable functions	• LSB first, MSB first selection Whether transmitting or receiving data begins with bit 0 or begins with bit 7 can be selected. • Serial data logic switching This function inverts the logic of the transmit/receive data. The start and stop bits are not inverted. • TXD, RXD I/O polarity switching This function inverts the polarities of the TXD pin output and RXD pin input. The logic levels of all I/O data are inverted. • RXD2 digital filter selection The RXD2 input signal can be enabled or disabled.

Notes:
1. If an overrun error occurs, the receive data in the U2RB register will be undefined.
2. The framing error flag and the parity error flag are set to 1 when data is transferred from the UART2 receive register to the U2RB register.

Table 25.6 Registers Used and Settings in UART Mode

Register	Bit	Function
U2TB	b0 to b8	Set transmit data. (1)
U2RB	b0 to b8	Receive data can be read. (1, 2)
	OER, FER, PER, SUM	Error flag
U2BRG	b0 to b7	Set a bit rate.
U2MR	SMD2 to SMD0	Set to 100b when transfer data is 7 bits long. Set to 101b when transfer data is 8 bits long. Set to 110b when transfer data is 9 bits long.
	CKDIR	Select the internal clock or external clock.
	STPS	Select the stop bit.
	PRY, PRYE	Select whether parity is included and whether odd or even.
	IOPOL	Select the TXD/RXD I/O polarity.
U2C0	CLK0, CLK1	Select the count source for the U2BRG register.
	CRS	Select $\overline{\text{CTS}}$ or $\overline{\text{RTS}}$ to use functions.
	TXEPT	Transmit register empty flag
	CRD	Enable or disable the $\overline{\text{CTS}}$ or $\overline{\text{RTS}}$ function.
	NCH	Select TXD2 pin output mode.
	CKPOL	Set to 0.
	UFORM	Select LSB first or MSB first when transfer data is 8 bits long. Set to 0 when transfer data is 7 or 9 bits long.
U2C1	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Receive complete flag
	U2IRS	Select the UART2 transmit interrupt source.
	U2RRM	Set to 0.
	U2LCH	Set to 1 to use inverted data logic.
	U2ERE	Set to 0.
U2SMR	b0 to b7	Set to 0.
U2SMR2	b0 to b7	Set to 0.
U2SMR3	b0 to b7	Set to 0.
U2SMR4	b0 to b7	Set to 0.
URXDF	DF2EN	Select the digital filter disabled or enabled.
U2SMR5	MP	Set to 0.

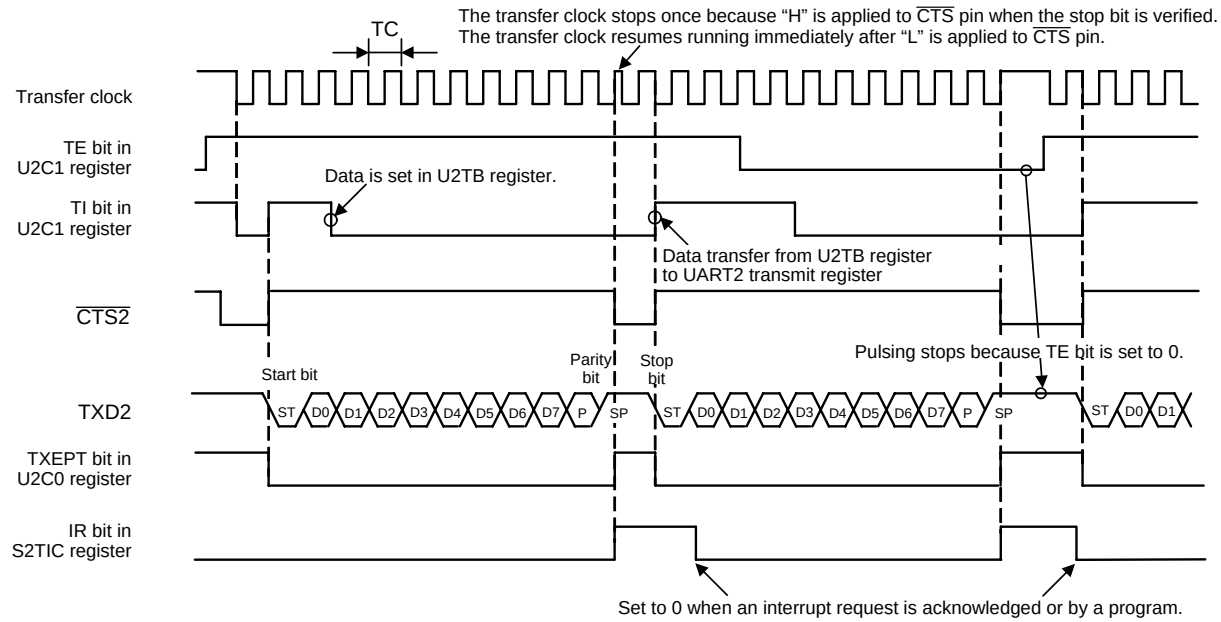
Notes:
1. The bits used for transmit/receive data are as follows:
   - Bits b0 to b6 when transfer data is 7 bits long
   - Bits b0 to b7 when transfer data is 8 bits long
   - Bits b0 to b8 when transfer data is 9 bits long
2. The contents of the following are undefined:
   - Bits b7 and b8 when transfer data is 7 bits long
   - Bit b8 when transfer data is 8 bits long

Table 25.7 lists the I/O Pin Functions in UART Mode.
Note that for a period from when the UART2 operating mode is selected to when transfer starts, the TXD2 pin outputs “H”. (When N-channel open-drain output is selected, this pin is in the high-impedance state.)
Figure 25.7 shows the Transmit Timing in UART Mode. Figure 25.8 shows the Receive Timing in UART Mode.

Table 25.7 I/O Pin Functions in UART Mode

Pin Name	Function	Selection Method
TXD2 (P3_4, P3_7 or P6_6)	Serial data output	• When TXD2 (P3_4) TXD2SEL2 to TXD2SEL0 bits in U2SR0 register =010b(P3_4) • When TXD2 (P3_7) TXD2SEL2 to TXD2SEL0 bits in U2SR0 register =001b(P3_7) • When TXD2 (P6_6) TXD2SEL2 to TXD2SEL0 bits in U2SR0 register =101b(P6_6) • For reception only: P3_4, P3_7, and P6_6 can be used as ports by setting bits TXD2SEL2 to TXD2SEL0 to 000b.
RXD2 (P3_4, P3_7 or P6_7)	Serial data input	• When RXD2 (P3_4) RXD2SEL2 to RXD2SEL0 bits in U2SR0 register =001b(P3_4) PD3_4 bit in PD3 register = 0 • When RXD2 (P3_7) RXD2SEL2 to RXD2SEL0 bits in U2SR0 register =010b(P3_7) PD3_7 bit in PD3 register =0 • When RXD2 (P6_7) RXD2SEL2 to RXD2SEL0 bits in U2SR0 register =101b(P6_7) PD6_7 bit in PD6 register =0 • For transmission only: P3_4, P3_7, and P6_7 can be used as ports by setting bits RXD2SEL1 to RXD2SEL0 to 000b.
CLK2 (P3_5 or P6_5)	I/O port	CLK2SEL1to CLK2SEL0 bits in U2SR1 register =00b
	Transfer clock input	• When CLK2 (P3_5) CLK2SEL1, CLK2SEL0 bit in U2SR1 register =01b(P3_5) CKDIR bit in U2MR register =1 PD3_5 bit in PD3 register =0 • When CLK2 (P6_5) CLK2SEL1, CLK2SEL0 bit in U2SR1 register =11b(P6_5) CKDIR bit in U2MR register =1 PD6_5 bit in PD6 register =0
$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$ (P3_3)	$\overline{\text{CTS}}$ input	CTS2SEL0 bit in U2SR1 register =1 CRD bit in U2C0 register =0 CRS bit in U2C0 register =0 PD3_3 bit in PD3 register =0
	$\overline{\text{RTS}}$ output	CTS2SEL0 bit in U2SR1 register =1 CRD bit in U2C0 register =0 CRS bit in U2C0 register =1
	I/O port	CTS2SEL0 bit in U2SR1 register =0

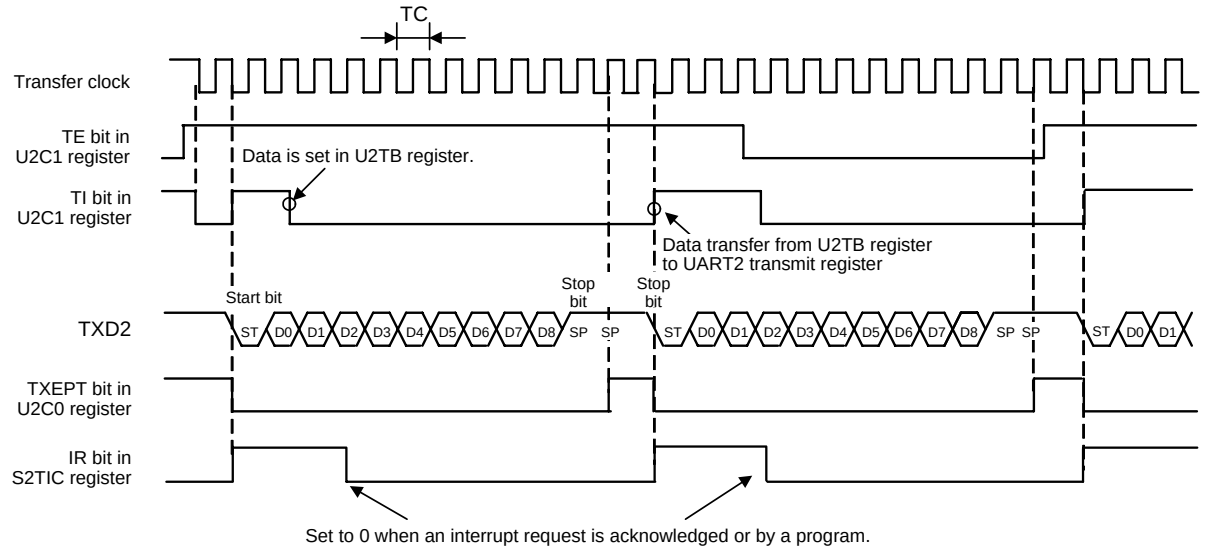
(1) Transmit Timing Example When Transfer Data is 8 Bits Long (Parity Enabled, One Stop Bit)



The above applies when:
- PRYE bit in U2MR register = 1 (parity enabled)
- STPS bit in U2MR register = 0 (one stop bit)
- CRD bit in U2C0 register = 0 (CTS/RTS function enabled), CRS bit = 0 (CTS function selected)
- U2IRS bit in U2C1 register = 1 (interrupt request generation when transmission is completed)

TC = 16(n + 1)/fj or 16(n + 1)/fEXT
fj: Frequency of U2BRG count source (f1, f8, f32)
fEXT: Frequency of U2BRG count source (external clock)
n: Setting value in U2BRG

(2) Transmit Timing Example When Transfer Data is 9 Bits Long (Parity Disabled, Two Stop Bits)

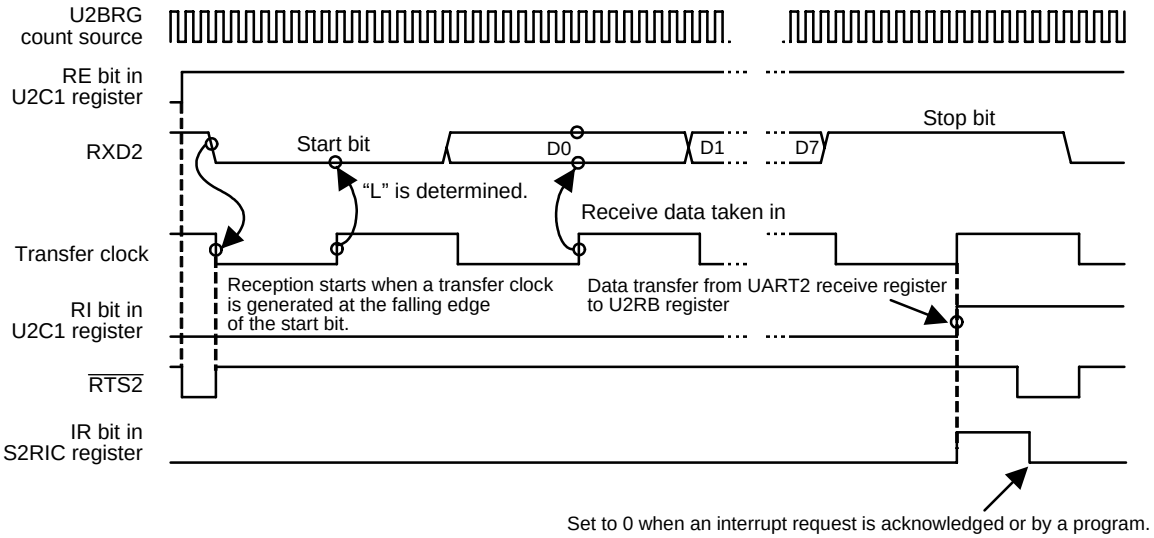


The above applies when:
- PRYE bit in U2MR register = 0 (parity disabled)
- STPS bit in U2MR register = 1 (two stop bits)
- CRD bit in U2C0 register = 1 (CTS/RTS function disabled)
- U2IRS bit in U2C1 register = 0 (interrupt request generation when the transmit buffer is empty)

TC = 16(n + 1)/fj or 16(n + 1)/fEXT
fj: Frequency of U2BRG count source (f1, f8, f32)
fEXT: Frequency of U2BRG count source (external clock)
n: Setting value in U2BRG

Figure 25.7 Transmit Timing in UART Mode

Receive Timing Example When Transfer Data is 8 Bits Long (Parity Disabled, One Stop Bit)



The above applies when:
- PRYE bit in U2MR register = 0 (parity disabled)
- STPS bit in U2MR register = 0 (one stop bit)
- CRD bit in U2C0 register = 0 ($\overline{CTS2}/\overline{RTS2}$ function enabled), CRS bit = 1 ($\overline{RTS2}$ function selected)

Figure 25.8 Receive Timing in UART Mode

25.4.1 Bit Rate

In UART mode, the bit rate is the frequency divided by the U2BRG register divided by 16. Table 25.8 lists the Bit Rate Setting Example in UART Mode (Internal Clock Selected).

Table 25.8 Bit Rate Setting Example in UART Mode (Internal Clock Selected)

Bit Rate (bps)	U2BRG Count Source	System Clock = 20 MHz			System Clock = 18.432 MHz (1)			System Clock = 8 MHz		
		U2BRG Setting Value	Actual Time (bps)	Setting Error (%)	U2BRG Setting Value	Actual Time (bps)	Setting Error (%)	U2BRG Setting Value	Actual Time (bps)	Setting Error (%)
1200	f8	129 (81h)	1201.92	0.16	119 (77h)	1200.00	0.00	51 (33h)	1201.92	0.16
2400	f8	64 (40h)	2403.85	0.16	59 (3Bh)	2400.00	0.00	25 (19h)	2403.85	0.16
4800	f8	32 (20h)	4734.85	-1.36	29 (1Dh)	4800.00	0.00	12 (0Ch)	4807.69	0.16
9600	f1	129 (81h)	9615.38	0.16	119 (77h)	9600.00	0.00	51 (33h)	9615.38	0.16
14400	f1	86 (56h)	14367.82	-0.22	79 (4Fh)	14400.00	0.00	34 (22h)	14285.71	-0.79
19200	f1	64 (40h)	19230.77	0.16	59 (3Bh)	19200.00	0.00	25 (19h)	19230.77	0.16
28800	f1	42 (2Ah)	29069.77	0.94	39 (27h)	28800.00	0.00	16 (10h)	29411.76	2.12
38400	f1	32 (20h)	37878.79	-1.36	29 (1Dh)	38400.00	0.00	12 (0Ch)	38461.54	0.16
57600	f1	21 (15h)	56818.18	-1.36	19 (13h)	57600.00	0.00	8 (08h)	55555.56	-3.55
115200	f1	10 (0Ah)	113636.36	-1.36	9 (09h)	115200.00	0.00	–	–	–

Note:
1. For the high-speed on-chip oscillator, the correction value in the FRA4 register should be written into the FRA1 register and the correction value in the FRA5 register should be written into the FRA3 register.
   This applies when the high-speed on-chip oscillator is selected as the system clock and bits FRA22 to FRA20 in the FRA2 register are set to 000b (divide-by-2 mode). For the precision of the high-speed on-chip oscillator, refer to **32. Electrical Characteristics**.

25.4.2 Measure for Dealing with Communication Errors

If communication is aborted or a communication error occurs while transmitting or receiving in UART mode, follow the procedures below:

(1) Set the TE bit in the U2C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
(2) Set bits SMD2 to SMD0 in the U2MR register to 000b (serial interface disabled).
(3) Set bits SMD2 to SMD0 in the U2MR register to 100b (UART mode, transfer data 7 bits long), 101b (UART mode, transfer data 8 bits long), or 110b (UART mode, transfer data 9 bits long).
(4) Set the TE bit in the U2C1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).

25.4.3 LSB First/MSB First Select Function

As shown in Figure 25.9, use the UFORM bit in the U2C0 register to select the transfer format. This function is enabled when transfer data is 8 bits long. Figure 25.9 shows the Transfer Format.

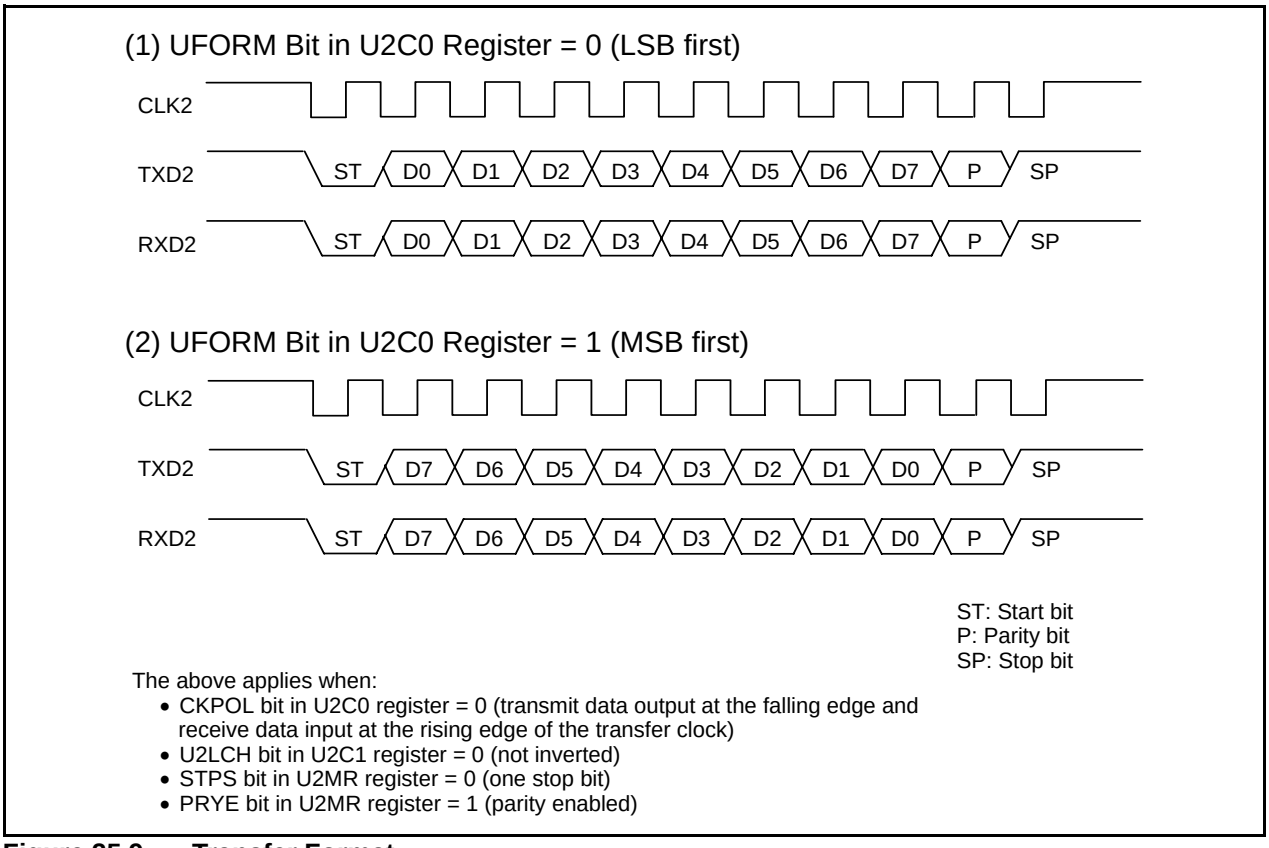


Figure 25.9 Transfer Format

25.4.4 Serial Data Logic Switching Function

The data written to the U2TB register has its logic inverted before being transmitted. Similarly, the received data has its logic inverted when read from the U2RB register. Figure 25.10 shows the Serial Data Logic Switching.

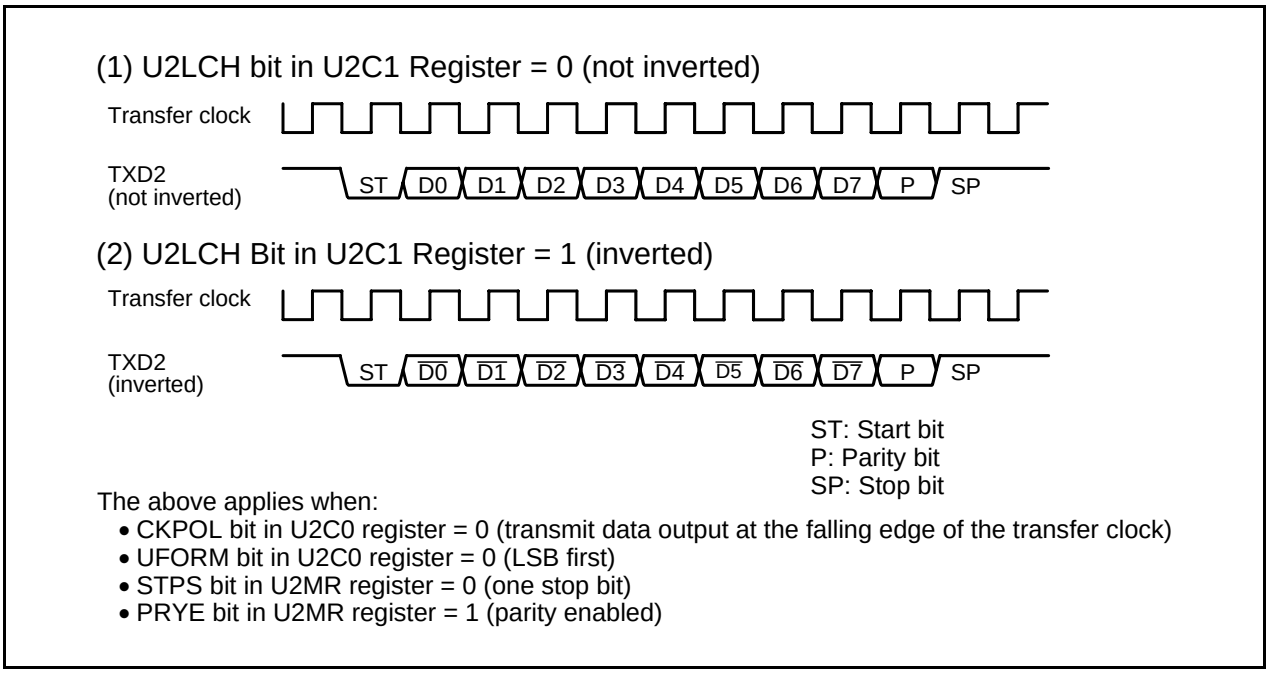


Figure 25.10 Serial Data Logic Switching

25.4.5 TXD and RXD I/O Polarity Inverse Function

This function inverts the polarities of the TXD2 pin output and RXD2 pin input. The logic levels of all I/O data (including bits for start, stop, and parity) are inverted. Figure 25.11 shows the TXD and RXD I/O Inversion.

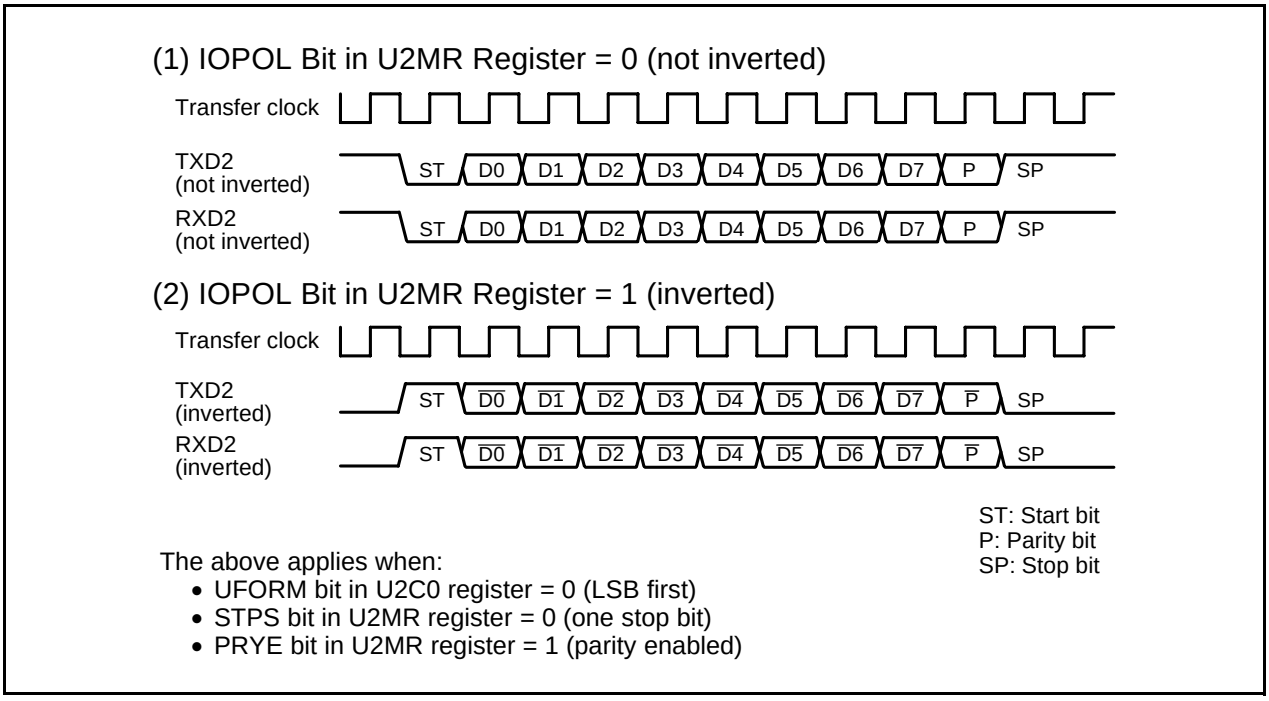


Figure 25.11 TXD and RXD I/O Inversion

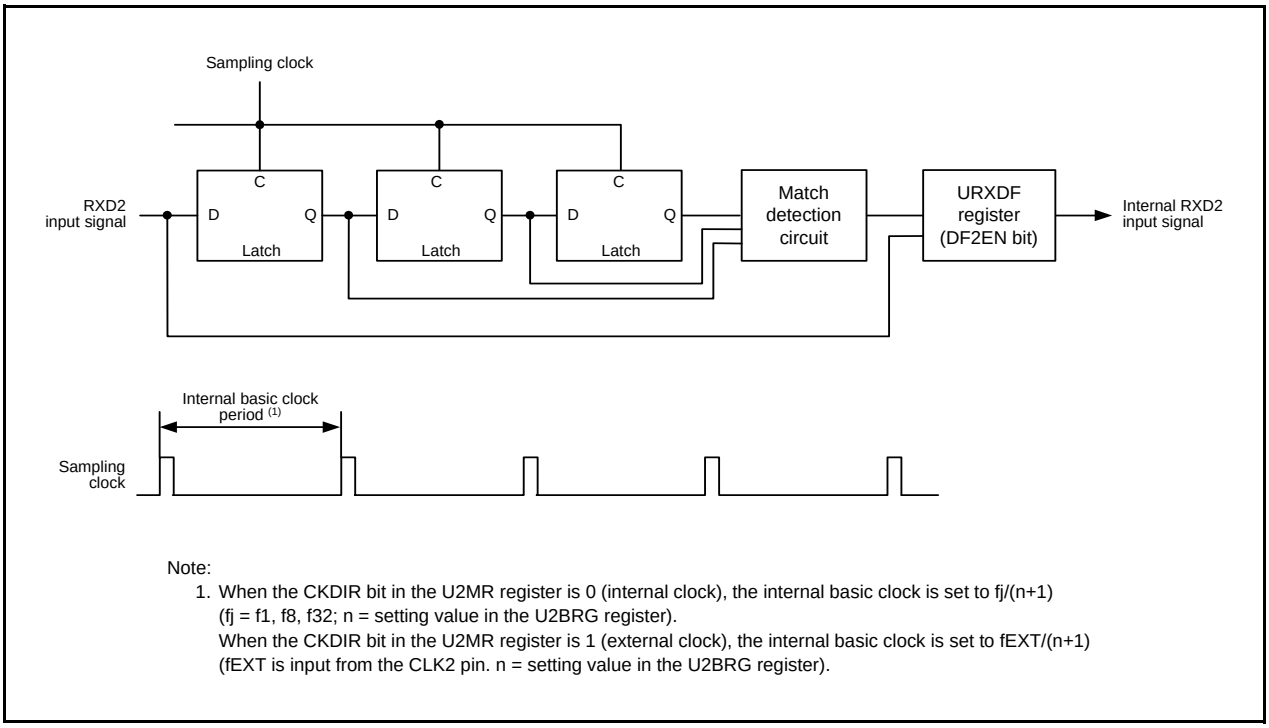
25.4.6 $\overline{\text{CTS}}/\overline{\text{RTS}}$ Function

The $\overline{\text{CTS}}$ function is used to start transmit operation when "L" is applied to the $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin. Transmit operation begins when the $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin is held low. If the "L" signal is switched to "H" during transmit operation, the operation stops after the ongoing transmit/receive operation is completed.
When the $\overline{\text{RTS}}$ function is used, the $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin outputs "L" when the MCU is ready for a receive operation.

- The CRD bit in the U2C0 register = 1 ($\overline{\text{CTS}}/\overline{\text{RTS}}$ function disabled)
  The $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin operates as the programmable I/O function.
- The CRD bit = 0, CRS bit = 0 ($\overline{\text{CTS}}$ function selected)
  The $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin operates as the $\overline{\text{CTS}}$ function.
- The CRD bit = 0, CRS bit = 1 ($\overline{\text{RTS}}$ function selected)
  The $\overline{\text{CTS2}}/\overline{\text{RTS2}}$ pin operates as the $\overline{\text{RTS}}$ function.

25.4.7 RXD2 Digital Filter Select Function

When the DF2EN bit in the URXDF register is set to 1 (RXD2 digital filer enabled), the RXD2 input signal is loaded internally via the digital filter circuit for noise reduction. The noise canceller consists of three cascaded latch circuits and a match detection circuit. The RXD2 input signal is sampled on the internal basic clock with a frequency 16 times the bit rate. It is recognized as a signal and the level is passed forward to the next circuit when three latch outputs match. When the outputs do not match, the previous value is retained.
In other words, when the level is changed within three clocks, the change is recognized as not a signal change but noise.
Figure 25.12 shows a Block Diagram of RXD2 Digital Filter Circuit.



Note:
1. When the CKDIR bit in the U2MR register is 0 (internal clock), the internal basic clock is set to fj/(n+1) (fj = f1, f8, f32; n = setting value in the U2BRG register).
   When the CKDIR bit in the U2MR register is 1 (external clock), the internal basic clock is set to fEXT/(n+1) (fEXT is input from the CLK2 pin. n = setting value in the U2BRG register).

Figure 25.12 Block Diagram of RXD2 Digital Filter Circuit

25.5 Special Mode 1 (I^2C Mode)

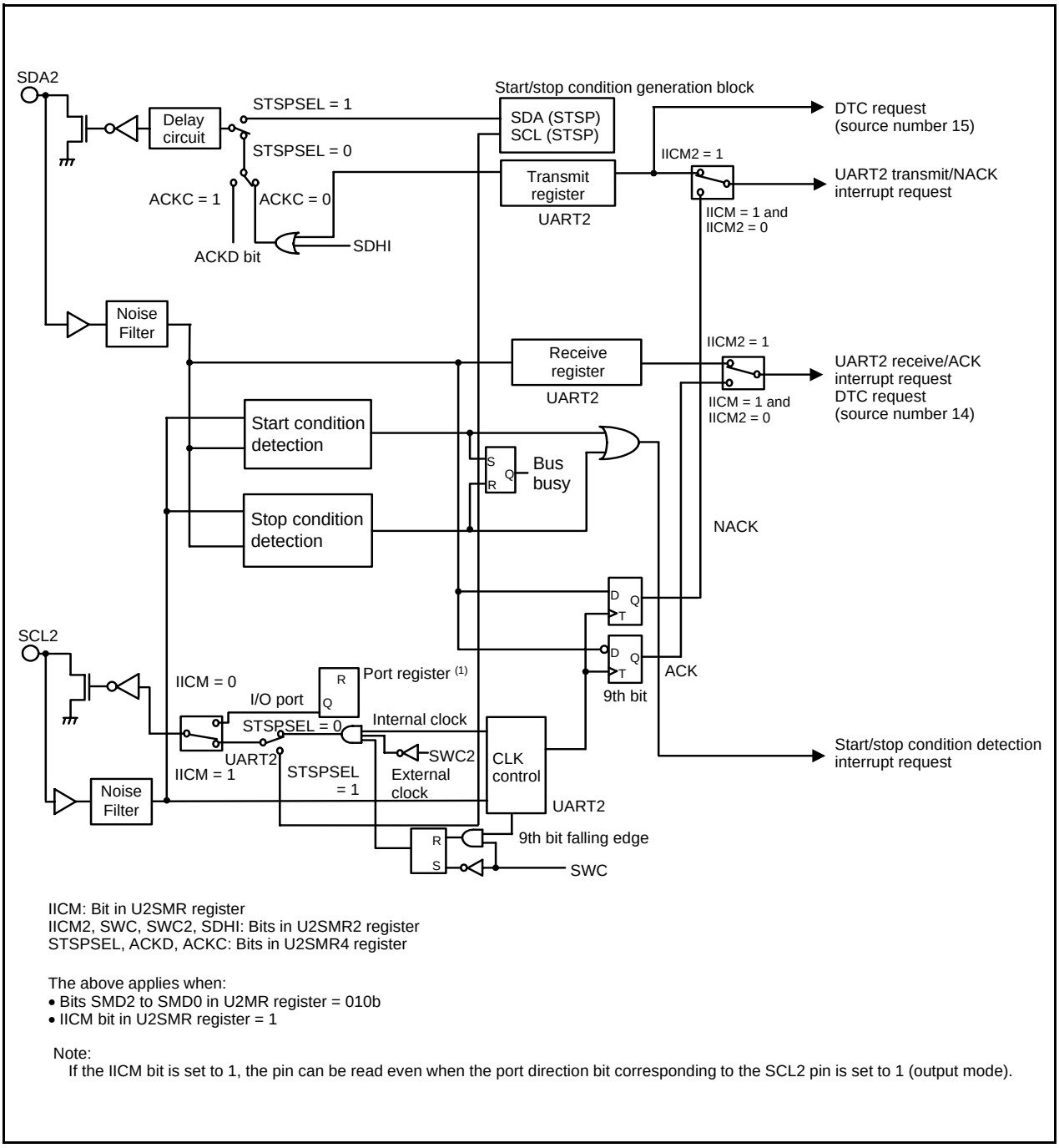
I^2C mode is provided for use as a simplified I^2C interface compatible mode. Table 25.9 lists the I^2C Mode Specifications. Tables 25.10 and 25.11 list the registers used in I^2C mode and the settings. Table 25.12 lists the I^2C Mode Functions, Figure 25.13 shows an I^2C Mode Block Diagram, and Figure 25.14 shows the Transfer to U2RB Register and Interrupt Timing.

As shown in Table 25.12, the MCU is placed in I^2C mode by setting bits SMD2 to SMD0 to 010b and the IICM bit to 1. Because SDA2 transmit output has a delay circuit attached, SDA2 output does not change state until SCL2 goes low and remains stably low.

Table 25.9 I^2C Mode Specifications

Item	Specification
Transfer data format	Transfer data length: 8 bits
Transfer clock	• Master mode The CKDIR bit in the U2MR register is set to 0 (internal clock): fj/(2(n+1)) fj = f1, f8, f32 n = setting value in the U2BRG register: 00h to FFh • Slave mode The CKDIR bit is set to 1 (external clock): Input from the SCL2 pin
Transmit start conditions	To start transmission, the following requirements must be met: (1) • The TE bit in the U2C1 register is set to 1 (transmission enabled). • The TI bit in the U2C1 register is set to 0 (data present in the U2TB register).
Receive start conditions	To start reception, the following requirements must be met: (1) • The RE bit in the U2C1 register is set to 1 (reception enabled). • The TE bit in the U2C1 register is set to 1 (transmission enabled). • The TI bit in the U2C1 register is set to 0 (data present in the U2TB register).
Interrupt request generation timing	Start/stop condition detection, no acknowledgement detection, or acknowledgement detection
Error detection	Overrun error (2) This error occurs if the serial interface starts receiving the next unit of data before reading the U2RB register and receives the 8th bit of the next unit of data.
Selectable functions	• SDA2 digital delay No digital delay or a delay of 2 to 8 U2BRG count source clock cycles can be selected. • Clock phase setting With or without clock delay can be selected.

Notes:
1. When an external clock is selected, the requirements must be met while the external clock is held high.
2. If an overrun error occurs, the received data in the U2RB register will be undefined. The IR bit in the S2RIC register remains unchanged.



IICM: Bit in U2SMR register
IICM2, SWC, SWC2, SDHI: Bits in U2SMR2 register
STSPSEL, ACKD, ACKC: Bits in U2SMR4 register

The above applies when:
- Bits SMD2 to SMD0 in U2MR register = 010b
- IICM bit in U2SMR register = 1

Note:
If the IICM bit is set to 1, the pin can be read even when the port direction bit corresponding to the SCL2 pin is set to 1 (output mode).

Figure 25.13 I²C Mode Block Diagram

Table 25.10 Registers Used and Settings in I²C Mode (1)

Register	Bit	Function	
		Master	Slave
U2TB (1)	b0 to b7	Set transmit data.	Set transmit data.
U2RB (1)	b0 to b7	Receive data can be read.	Receive data can be read.
	b8	ACK or NACK is set in this bit.	ACK or NACK is set in this bit.
	OER	Overrun error flag	Overrun error flag
U2BRG	b0 to b7	Set a bit rate.	Disabled
U2MR (1)	SMD2 to SMD0	Set to 010b.	Set to 010b.
	CKDIR	Set to 0.	Set to 1.
	IOPOL	Set to 0.	Set to 0.
U2C0	CLK1, CLK0	Select the count source for the U2BRG register.	Disabled
	CRS	Disabled because CRD = 1.	Disabled because CRD = 1.
	TXEPT	Transmit register empty flag	Transmit register empty flag
	CRD	Set to 1.	Set to 1.
	NCH	Set to 1.	Set to 1.
	CKPOL	Set to 0.	Set to 0.
	UFORM	Set to 1.	Set to 1.
U2C1	TE	Set to 1 to enable transmission.	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag	Transmit buffer empty flag
	RE	Set to 1 to enable reception.	Set to 1 to enable reception.
	RI	Receive complete flag	Receive complete flag
	U2IRS	Set to 1.	Set to 1.
	U2RRM, U2LCH, U2ERE	Set to 0.	Set to 0.
U2SMR	IICM	Set to 1.	Set to 1.
	BBS	Bus busy flag	Bus busy flag
	b1, b3, b5 to b7	Set to 0.	Set to 0.
U2SMR2	IICM2	Refer to **Table 25.12 I²C Mode Functions**.	Refer to **Table 25.12 I²C Mode Functions**.
	CSC	Set to 1 to enable clock synchronization.	Set to 0.
	SWC	Set to 1 to fix SCL2 output low at the falling edge of the 9th bit of clock.	Set to 1 to fix SCL2 output low at the falling edge of the 9th bit of clock.
	STAC	Set to 0.	Set to 1 to initialize UART2 at start condition detection
	SWC2	Set to 1 to forcibly pull SCL2 low.	Set to 1 to forcibly pull SCL2 output low.
	SDHI	Set to 1 to disable SDA2 output.	Set to 1 to disable SDA2 output.
	b7	Set to 0.	Set to 0.

Note:
1. Set the bits not listed in this table to 0 when writing to the above registers in I²C mode.

Table 25.11 Registers Used and Settings in I²C Mode (2)

Register	Bit	Function	
		Master	Slave
U2SMR3	b0, b2, b4, and NODC	Set to 0.	Set to 0.
	CKPH	Refer to **Table 25.12 I²C Mode Functions**.	Refer to **Table 25.12 I²C Mode Functions**.
	DL2 to DL0	Set the amount of SDA2 digital delay.	Set the amount of SDA2 digital delay.
U2SMR4	STAREQ	Set to 1 to generate a start condition.	Set to 0.
	RSTAREQ	Set to 1 to generate a restart condition.	Set to 0.
	STPREQ	Set to 1 to generate a stop condition.	Set to 0.
	STSPSEL	Set to 1 to output each condition.	Set to 0.
	ACKD	Select ACK or NACK.	Select ACK or NACK.
	ACKC	Set to 1 to output ACK data.	Set to 1 to output ACK data.
	SCLHI	Set to 1 to stop SCL2 output when a stop condition is detected.	Set to 0.
	SWC9	Set to 0.	Set to 1 to hold SCL2 low at the falling edge of the 9th bit of clock.
URXDF	DF2EN	Set to 0.	Set to 0.
U2SMR5	MP	Set to 0.	Set to 0.

Table 25.12 I²C Mode Functions

Function	Clock Synchronous Serial I/O Mode (SMD2 to SMD0 = 001b, IICM = 0)	I²C Mode (SMD2 to SMD0 = 010b, IICM = 1)			
		IICM2 = 0 (NACK/ACK interrupt)		IICM2 = 1 (UART transmit/receive interrupt)	
		CKPH = 0 (No Clock Delay)	CKPH = 1 (With Clock Delay)	CKPH = 0 (No Clock Delay)	CKPH = 1 (With Clock Delay)
Source of UART2 bus collision interrupt (1, 5)	-	Start condition detection or stop condition detection (Refer to **Table 25.13 STSPSEL Bit Functions**)			
Source of UART2 transmit/NACK2 (1, 6)	UART2 transmission Transmission started or completed (selectable by U2IRS bit)	No acknowledgment detection (NACK) Rising edge of SCL2 9th bit		UART2 transmission Rising edge of SCL2 9th bit	UART2 transmission Falling edge of SCL2 next to 9th bit
Source of UART2 receive/ACK2 (1, 6)	UART2 reception When 8th bit received CKPOL = 0 (rising edge) CKPOL = 1 (falling edge)	Acknowledgment detection (ACK) Rising edge of SCL2 9th bit		UART2 reception Falling edge of SCL2 9th bit	
Timing for transferring data from UART reception shift register to U2RB register	CKPOL = 0 (rising edge) CKPOL = 1 (falling edge)	Rising edge of SCL2 9th bit		Falling edge of SCL2 9th bit	Falling and rising edges of SCL2 9th bit
UART2 transmission output delay	No delay	With delay			
TXD2/SDA2 functions	TXD2 output	SDA2 I/O			
RXD2/SCL2 functions	RXD2 input	SCL2 I/O			
CLK2 functions	CLK2 input or output port selected	– (Cannot be used in I²C mode.)			
Noise filter width	15 ns	200 ns			
Read of RXD2 and SCL2 pin levels	Possible when the corresponding port direction bit = 0	Possible regardless of the content of the corresponding port direction bit.			
Initial value of TXD2 and SDA2 outputs	CKPOL = 0 (“H”) CKPOL = 1 (“L”)	The value set in the port register before setting I²C mode. (2)			
Initial and end values of SCL2	-	“H”	“L”	“H”	“L”
DTC source number 14 (6)	UART2 reception When 8th bit received CKPOL = 0 (rising edge) CKPOL = 1 (falling edge)	Acknowledgment detection (ACK)		UART2 reception Falling edge of SCL2 9th bit	
DTC source number 15 (6)	UART2 transmission Transmission started or completed (selectable by U2IRS bit)	UART2 transmission Rising edge of SCL2 9th bit	UART2 transmission Falling edge of SCL2 next to 9th bit	UART2 transmission Rising edge of SCL2 9th bit	UART2 transmission Falling edge of SCL2 next to 9th bit
Storage of receive data	1st to 8th bits of the received data are stored in bits b0 to b7 in the U2RB register.	1st to 8th bits of the received data are stored in bits b7 to b0 in the U2RB register.		1st to 7th bits of the received data are stored in bits b6 to b0 in the U2RB register. 8th bit is stored in bit b8 in the U2RB register.	
					1st to 8th bits are stored in bits b7 to b0 in the U2RB register. (3)
Read of receive data	The U2RB register status is read.				Bits b6 to b0 in the U2RB register are read as bits b7 to b1. Bit b8 in the U2RB register is read as bit b0. (4)

Notes:
1. If the source of any interrupt is changed, the IR bit in the interrupt control register for the changed interrupt may inadvertently be set to 1 (interrupt requested). (Refer to **11.8 Notes on Interrupts**.)
   If one of the bits listed below is changed, the interrupt source, the interrupt timing, and others change. Therefore, always be sure to set the IR bit to 0 (interrupt not requested) after changing these bits.
   Bits SMD2 to SMD0 in the U2MR register, the IICM bit in the U2SMR register, the IICM2 bit in the U2SMR2 register, and the CKPH bit in the U2SMR3 register.
2. Set the initial value of SDA2 output while bits SMD2 to SMD0 in the U2MR register are 000b (serial interface disabled).
3. Second data transfer to the U2RB register (rising edge of SCL2 9th bit)
4. First data transfer to the U2RB register (falling edge of SCL2 9th bit)
5. Refer to **Figure 25.16 STSPSEL Bit Functions**.
6. Refer to **Figure 25.14 Transfer to U2RB Register and Interrupt Timing**.

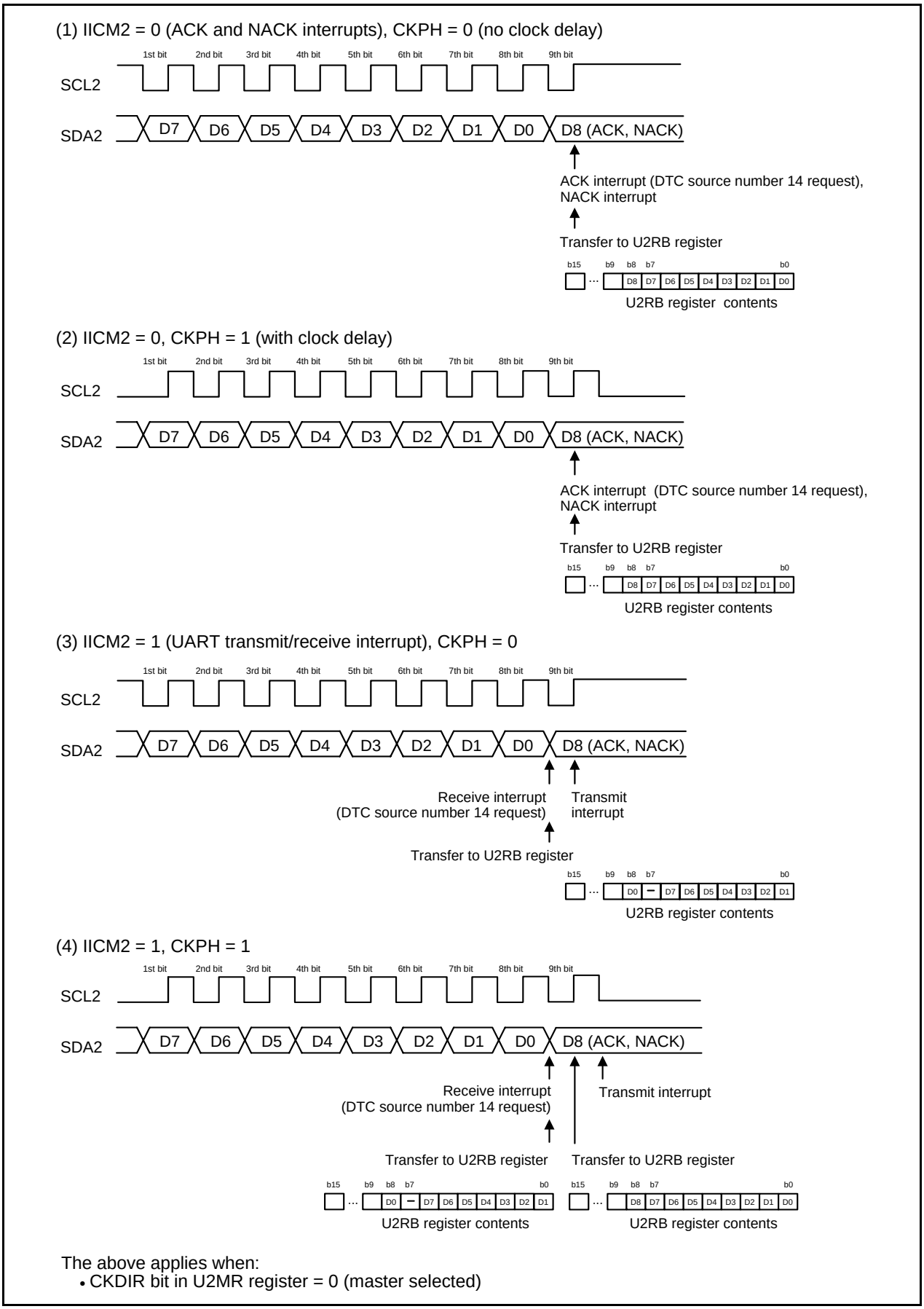


Figure 25.14 Transfer to U2RB Register and Interrupt Timing

25.5.1 Detection of Start and Stop Conditions

Whether a start or a stop condition has been detected is determined.
A start condition detect interrupt request is generated when the SDA2 pin changes state from high to low while the SCL2 pin is in the high state. A stop condition detect interrupt request is generated when the SDA2 pin changes state from low to high while the SCL2 pin is in the high state.
Because the start and stop condition detect interrupts share an interrupt control register and vector, check the BBS bit in the U2SMR register to determine which interrupt source is requesting the interrupt.
Figure 25.15 shows the Detection of Start and Stop Conditions.

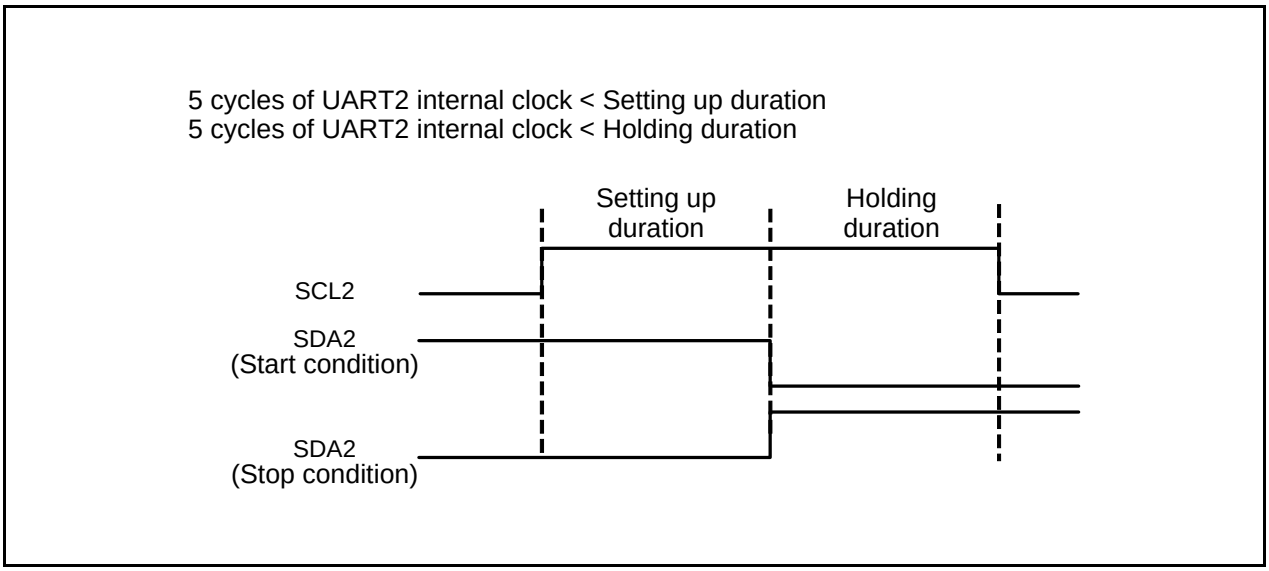


Figure 25.15 Detection of Start and Stop Conditions

25.5.2 Output of Start and Stop Conditions

A start condition is generated by setting the STAREQ bit in the U2SMR4 register to 1 (start).
A restart condition is generated by setting the RSTAREQ bit in the U2SMR4 register to 1 (start).
A stop condition is generated by setting the STPREQ bit in the U2SMR4 register to 1 (start).
The output procedure is as follows:
(1) Set the STAREQ bit, RSTAREQ bit or STPREQ bit to 1 (start).
(2) Set the STSPSEL bit in the U2SMR4 register to 1 (output).
Table 25.13 lists the STSPSEL Bit Functions. Figure 25.16 shows the STSPSEL Bit Functions.

Table 25.13 STSPSEL Bit Functions

Function	STSPSEL = 0	STSPSEL = 1
Output of pins SCL2 and SDA2	Output of transfer clock and data Output of start/stop conditions is accomplished by a program using ports (not automatically generated in hardware)	Output of start/stop conditions according to bits STAREQ, RSTAREQ, and STPREQ
Start/stop condition interrupt request generation timing	Detection of start/stop conditions	Completion of start/stop condition generation

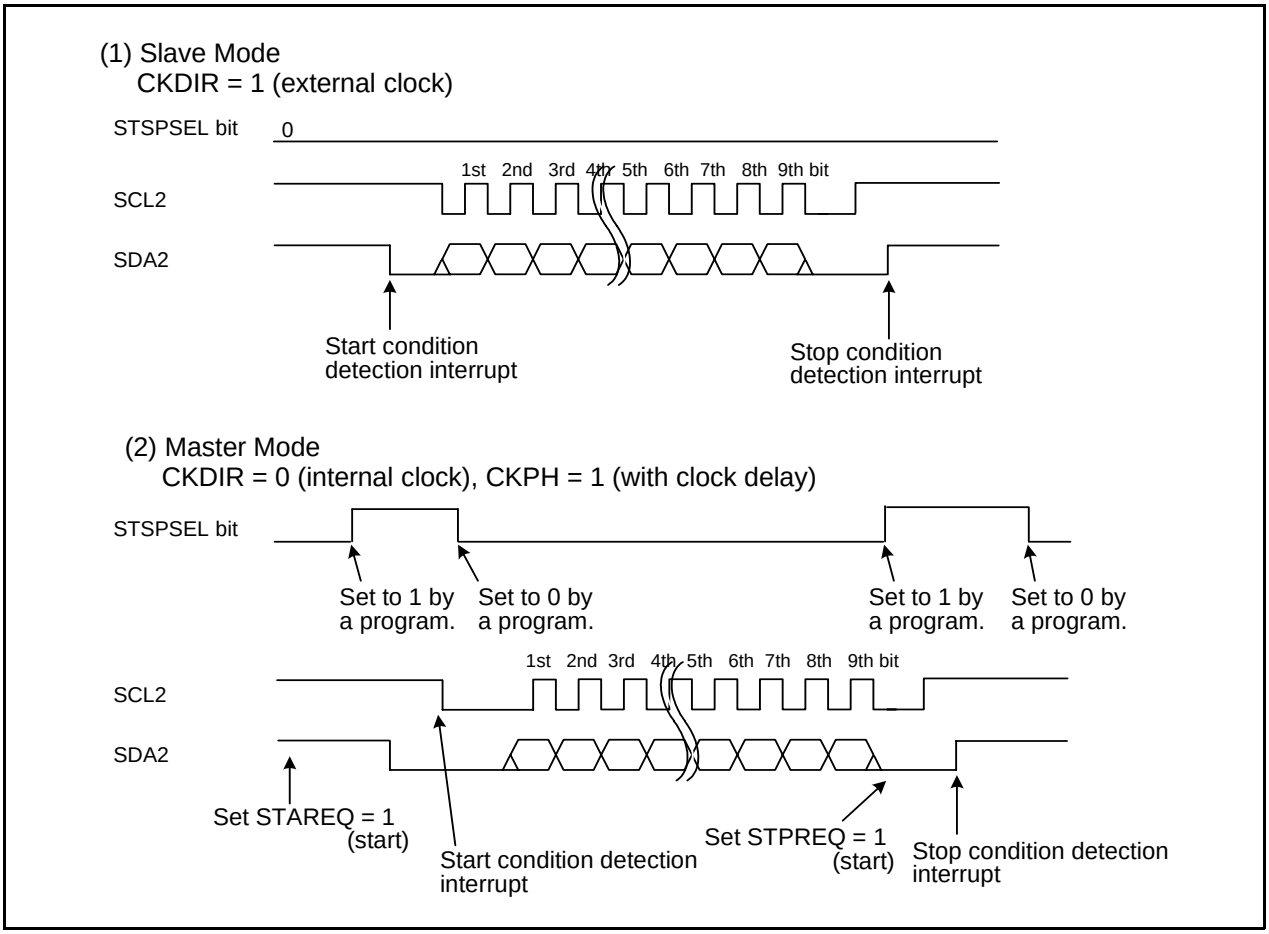


Figure 25.16 STSPSEL Bit Functions

25.5.3 Transfer Clock

The transfer clock is used to transmit and receive data as is shown in **Figure 25.14 Transfer to U2RB Register and Interrupt Timing**.

The CSC bit in the U2SMR2 register is used to synchronize an internally generated clock (internal SCL2) and an external clock supplied to the SCL2 pin. When the CSC bit is set to 1 (clock synchronization enabled), if a falling edge on the SCL2 pin is detected while the internal SCL2 is high, the internal SCL2 goes low. The value in the U2BRG register is reloaded and counting of the low-level intervals starts. If the internal SCL2 changes state from low to high while the SCL2 pin is low, counting stops. If the SCL2 pin goes high, counting restarts.

In this way, the UART2 transfer clock is equivalent to AND of the internal SCL2 and the clock signal applied to the SCL2 pin. The transfer clock works from a half cycle before the falling edge of the internal SCL2 1st bit to the rising edge of the 9th bit. To use this function, select an internal clock for the transfer clock.

The SWC bit in the U2SMR2 register determines whether the SCL2 pin is fixed low or freed from low-level output at the falling edge of the 9th clock pulse.

If the SCLHI bit in the U2SMR4 register is set to 1 (enabled), SCL2 output is turned off (placed in the high-impedance state) when a stop condition is detected.

Setting the SWC2 bit in the U2SMR2 register to 1 (“L” output) makes it possible to forcibly output a low-level signal from the SCL2 pin even while sending or receiving data. Setting the SWC2 bit to 0 (transfer clock) allows the transfer clock to be output from or supplied to the SCL2 pin, instead of outputting a low-level signal.

If the SWC9 bit in the U2SMR4 register is set to 1 (SCL “L” hold enabled) when the CKPH bit in the U2SMR3 register is 1, the SCL2 pin is fixed low at the falling edge of the clock pulse next to the 9th. Setting the SWC9 bit to 0 (SCL “L” hold disabled) frees the SCL2 pin from low-level output.

25.5.4 SDA Output

The data written to bits b7 to b0 (D7 to D0) in the U2TB register is output in descending order from D7.

The 9th bit (D8) is ACK or NACK.

Set the initial value of SDA2 transmit output when IICM is set to 1 (I^2C mode) and bits SMD2 to SMD0 in the U2MR register are set to 000b (serial interface disabled).

Bits DL2 to DL0 in the U2SMR3 register allow addition of no delays or a delay of 2 to 8 U2BRG count source clock cycles to the SDA2 output.

Setting the SDHI bit in the U2SMR2 register to 1 (SDA output disabled) forcibly places the SDA2 pin in the high-impedance state. Do not write to the SDHI bit at the rising edge of the UART2 transfer clock.

25.5.5 SDA Input

When the IICM2 bit is set to 0, the 1st to 8th bits (D7 to D0) of received data are stored in bits b7 to b0 in the U2RB register. The 9th bit (D8) is ACK or NACK.
When the IICM2 bit is set to 1, the 1st to 7th bits (D7 to D1) of received data are stored in bits b6 to b0 in the U2RB register and the 8th bit (D0) is stored in bit b8 in the U2RB register. Even when the IICM2 bit is set to 1, if the CKPH bit is 1, the same data as when the IICM2 bit is 0 can be read by reading the U2RB register after the rising edge of 9th bit of the clock.

25.5.6 ACK and NACK

If the STSPSEL bit in the U2SMR4 register is set to 0 (start and stop conditions not output) and the ACKC bit in the U2SMR4 register is set to 1 (ACK data output), the value of the ACKD bit in the U2SMR4 register is output from the SDA2 pin.
If the IICM2 bit is set to 0, a NACK interrupt request is generated if the SDA2 pin remains high at the rising edge of the 9th bit of transmit clock pulse. An ACK interrupt request is generated if the SDA2 pin is low at the rising edge of the 9th bit of the transmit clock.
If ACK2 (UART2 reception) is selected to generate a DTC request source, a DTC transfer can be activated by detection of an acknowledge.

25.5.7 Initialization of Transmission/Reception

If a start condition is detected while the STAC bit is set to 1 (UART2 initialization enabled), the serial interface operates as described below.

- The transmit shift register is initialized, and the contents of the U2TB register are transferred to the transmit shift register. In this way, the serial interface starts sending data when the next clock pulse is applied. However, the UART2 output value does not change state and remains the same as when a start condition was detected until the first bit of data is output in synchronization with the input clock.
- The receive shift register is initialized, and the serial interface starts receiving data when the next clock pulse is applied.
- The SWC bit is set to 1 (SCL wait output enabled). Consequently, the SCL2 pin is pulled low at the falling edge of the 9th clock pulse.

Note that when UART2 transmission/reception is started using this function, the TI bit does not change state. Select the external clock as the transfer clock to start UART2 transmission/reception with this setting.

25.6 Special Mode 3 (IE mode)

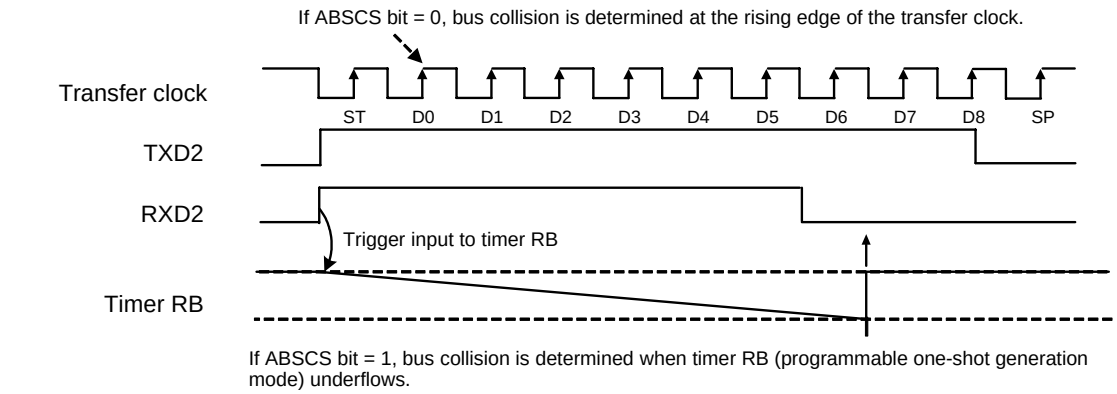
In IE mode, one bit of IEBus is approximated with one byte of UART mode waveform.
Table 25.14 lists the Registers Used and Settings in IE Mode. Figure 25.17 shows the Bits Associated with Bus Collision Detect Function.
If the TXD2 pin output level and RXD2 pin input level do not match, a UART2 bus collision detect interrupt request is generated.

Table 25.14 Registers Used and Settings in IE Mode

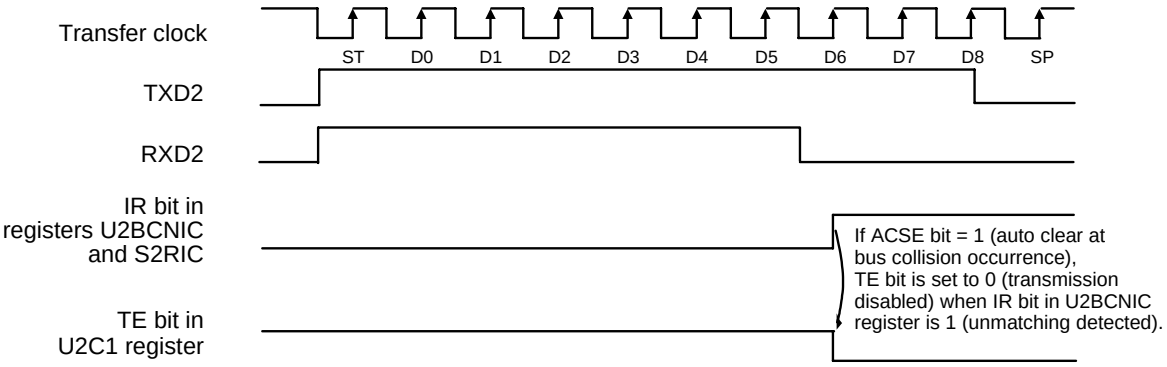
Register	Bit	Function
U2TB	b0 to b8	Set transmit data.
U2RB (1)	b0 to b8	Receive data can be read.
	OER, FER, PER, SUM	Error flag
U2BRG	b0 to b7	Set a bit rate.
U2MR	SMD2 to SMD0	Set to 110b.
	CKDIR	Select the internal clock or external clock.
	STPS	Set to 0.
	PRY	Disabled because PRYE = 0.
	PRYE	Set to 0.
	IOPOL	Select the TXD and RXD I/O polarity
U2C0	CLK1, CLK0	Select the count source for the U2BRG register.
	CRS	Disabled because CRD = 1.
	TXEPT	Transmit register empty flag
	CRD	Set to 1.
	NCH	Select the TXD2 pin output format.
	CKPOL	Set to 0.
	UFORM	Set to 0.
U2C1	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Receive complete flag
	U2IRS	Select the UART2 transmit interrupt source.
	U2RRM, U2LCH, U2ERE	Set to 0.
U2SMR	b0 to b3, b7	Set to 0.
	ABSCS	Select the sampling timing at which a bus collision is detected.
	ACSE	Set to 1 to use the auto clear function of the transmit enable bit.
	SSS	Select the transmit start condition.
U2SMR2	b0 to b7	Set to 0.
U2SMR3	b0 to b7	Set to 0.
U2SMR4	b0 to b7	Set to 0.
URXDF	DF2EN	Set to 0.
U2SMR5	MP	Set to 0.

Note:
1. Set the bits not listed in this table to 0 when writing to the above registers in IE mode.

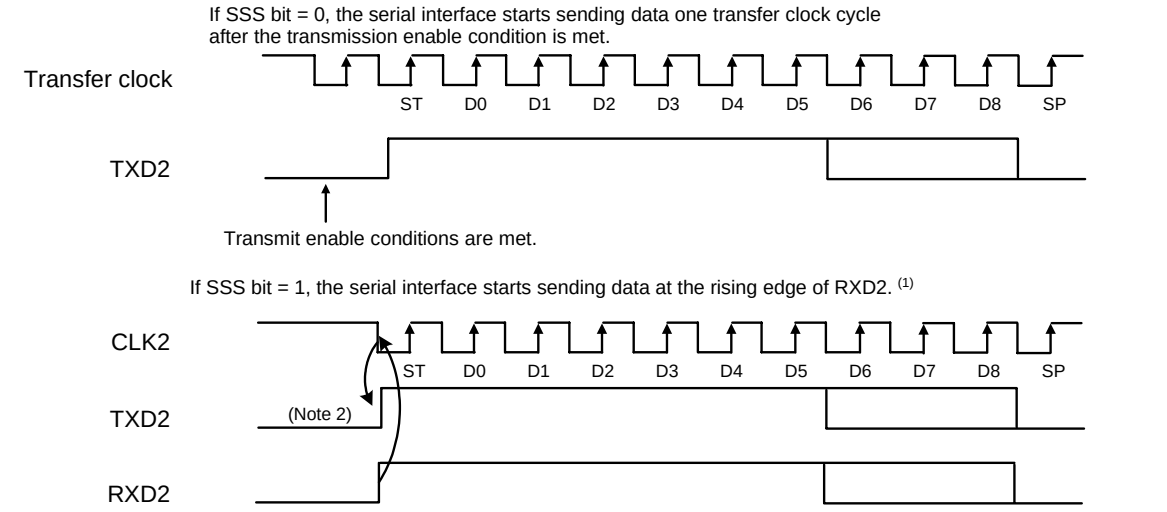
(1) ABSCS Bit in U2SMR Register (bus collision detect sampling clock select)



(2) ACSE Bit in U2SMR Register (auto clear of transmit enable bit)



(3) SSS Bit in U2SMR Register (transmit start condition select)



Notes:
1. The falling edge of RXD2 when IOPOL = 0; the rising edge of RXD2 when IOPOL = 1.
2. The transmit condition must be met before the falling edge of RXD. (1)

The above applies when:
- IOPOL = 1 (inverted)

Figure 25.17 Bits Associated with Bus Collision Detect Function

25.7 Multiprocessor Communication Function

When the multiprocessor communication function is used, data transmission/reception can be performed between a number of processors sharing communication lines by asynchronous serial communication, in which a multiprocessor bit is added to the data. For multiprocessor communication, each receiving station is addressed by a unique ID code. The serial communication cycle consists of two component cycles; an ID transmission cycle for specifying the receiving station, and a data transmission cycle for the specified receiving station. The multiprocessor bit is used to differentiate between the ID transmission cycle and the data transmission cycle. When the multiprocessor bit is set to 1, the cycle is an ID transmission cycle; when the multiprocessor bit is set to 0, the cycle is a data transmission cycle. Figure 25.18 shows an Inter-Processor Communication Example Using Multiprocessor Format (Data AAh Transmission to Receiving Station A).

The transmitting station first sends the ID code of the receiving station to perform communication as communication data with a 1 multiprocessor bit added. It then sends transmit data as communication data with a 0 multiprocessor bit added.

When communication data in which the multiprocessor bit is 1 is received, the receiving station compares that data with its own ID. If they match, the data to be sent next is received. If they do not match, the receive station continues to skip communication data until data in which the multiprocessor bit is 1 is again received.

UART2 uses the MPIE bit in the U2SMR5 register to implement this function. When the MPIE bit is set to 1, data transfer from the UART2 receive register to the U2RB register, receive error detection, and the settings of the status flags, the RI bit in the U2C1 register, bits FER and OER in the U2RB register, are disabled until data in which the multiprocessor bit is 1 is received. On receiving a receive character in which the multiprocessor bit is 1, the MPRB bit in the U2RB register is set to 1 and the MPIE in the U2SMR5 register bit is set to 0, thus normal reception is resumed.

When the multiprocessor format is specified, the parity bit specification is invalid. All other bit settings are the same as those in normal asynchronous mode (UART mode). The clock used for multiprocessor communication is the same as that in normal asynchronous mode (UART mode).

Figure 25.19 shows a Block Diagram of Multiprocessor Communication Function.

Table 25.15 lists the Registers and Settings in Multiprocessor Communication Function.

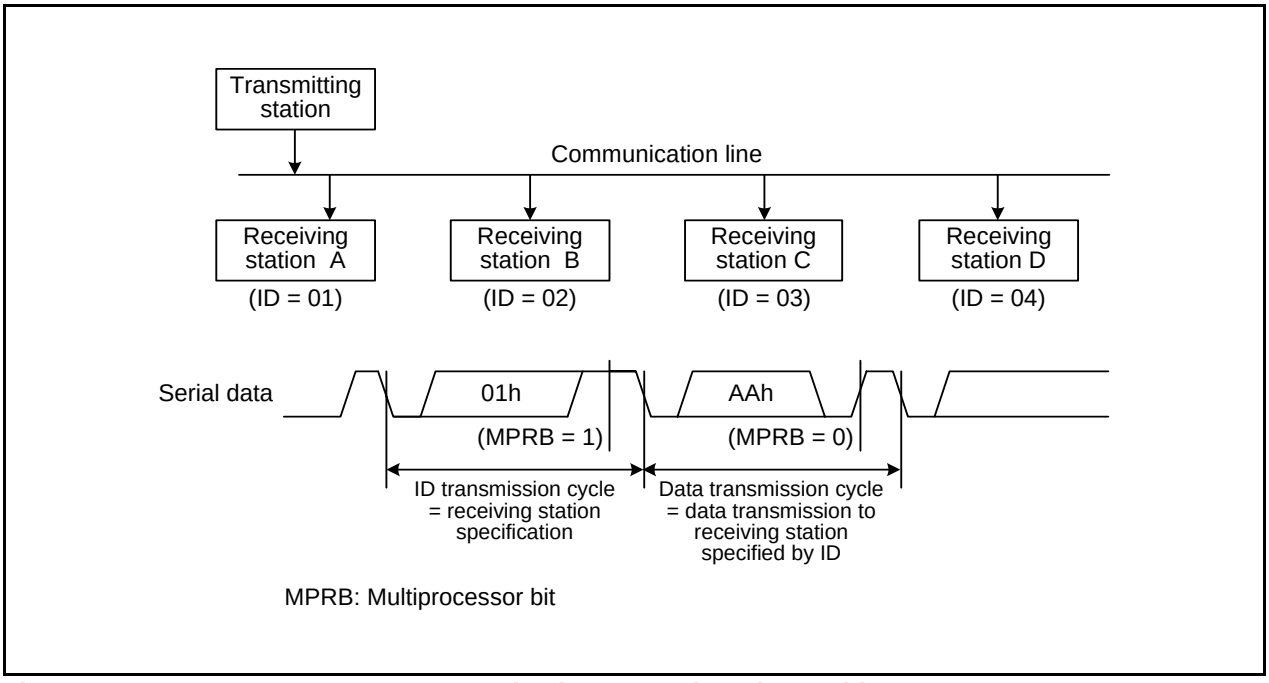


Figure 25.18 Inter-Processor Communication Example Using Multiprocessor Format (Data AAh Transmission to Receiving Station A)

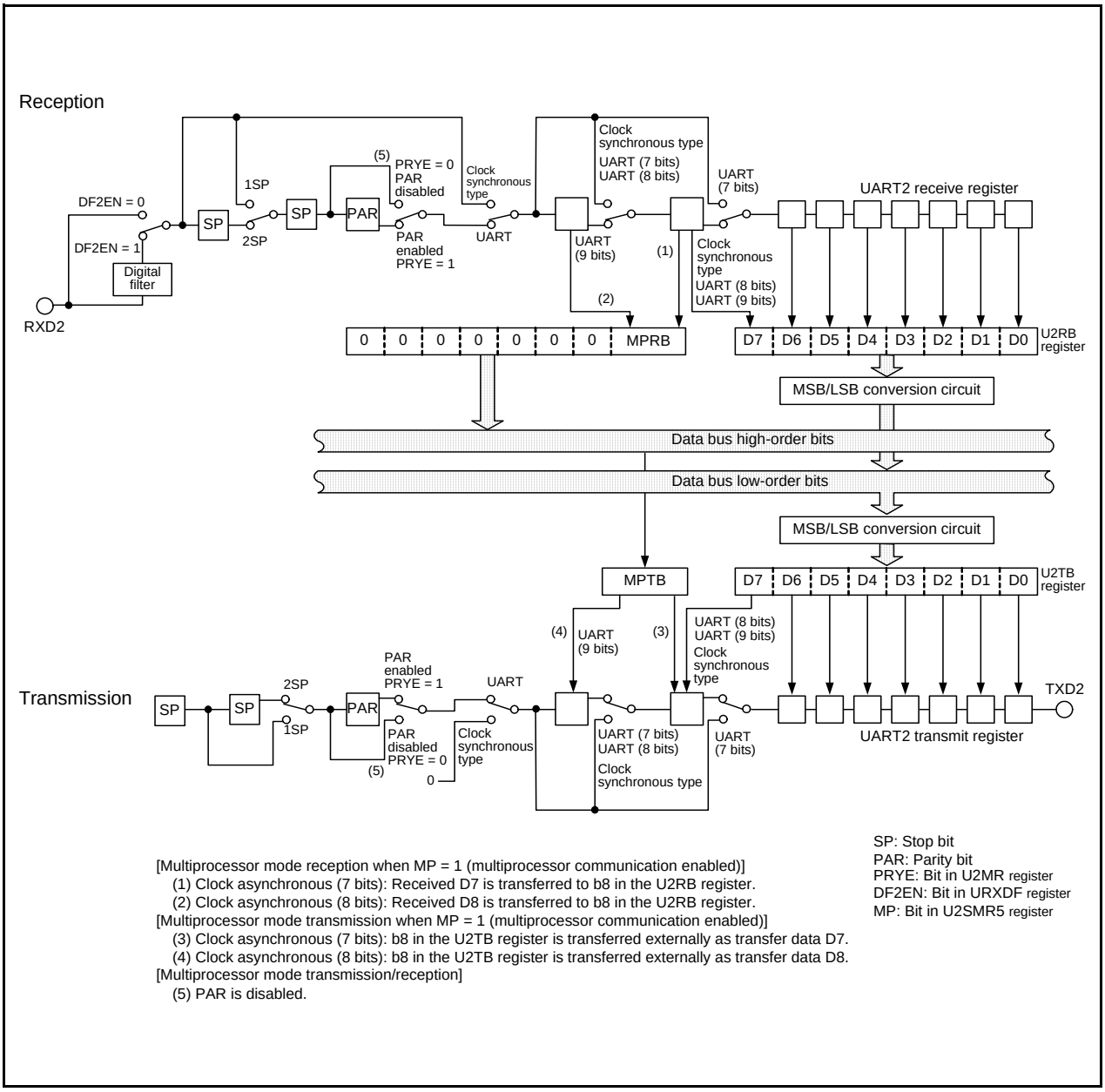


Figure 25.19 Block Diagram of Multiprocessor Communication Function

Table 25.15 Registers and Settings in Multiprocessor Communication Function

Register	Bit	Function
U2TB (1)	b0 to b7	Set transmit data.
	MPTB	Set to 0 or 1.
U2RB (2)	b0 to b7	Receive data can be read.
	MPRB	Multiprocessor bit
	OER, FER, SUM	Error flag
U2BRG	b0 to b7	Set the transfer rate.
U2MR	SMD2 to SMD0	Set to 100b when transfer data is 7 bits long.
		Set to 101b when transfer data is 8 bits long.
	CKDIR	Select the internal clock or external clock.
	STPS	Select the stop bit.
	PRY, PRYE	Parity detection function disabled
	IOPOL	Set to 0.
U2C0	CLK0, CLK1	Select the U2BRG count source.
	CRS	$\overline{\text{CTS}}$ or $\overline{\text{RTS}}$ function disabled
	TXEPT	Transmit register empty flag
	CRD	Set to 0.
	NCH	Select TXD2 pin output mode.
	CKPOL	Set to 0.
	UFORM	Set to 0.
U2C1	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Receive complete flag
	U2IRS	Select the UART2 transmit interrupt source.
	U2LCH	Set to 0.
	U2ERE	Set to 0.
U2SMR	b0 to b7	Set to 0.
U2SMR2	b0 to b7	Set to 0.
U2SMR3	b0 to b7	Set to 0.
U2SMR4	b0 to b7	Set to 0.
U2SMR5	MP	Set to 1.
	MPIE	Set to 1.
URXDF	DF2EN	Select the digital filter enabled or disabled.

Notes:
1. Set the MPTB bit to 1 when the ID data frame is transmitted. Set this bit to 0 when the data frame is transmitted.
2. If the MPRB bit is set to 1, received D7 to D0 are ID fields. If the MPRB bit is set to 0, received D7 to D0 are data fields.

25.7.1 Multiprocessor Transmission

Figure 25.20 shows a Sample Flowchart of Multiprocessor Data Transmission. Set the MPBT bit in the U2TB register to 1 for ID transmission cycles. Set the MPBT bit in the U2TB register to 0 for data transmission cycles. Other operations are the same as in universal asynchronous receiver/transmitter mode (UART mode).

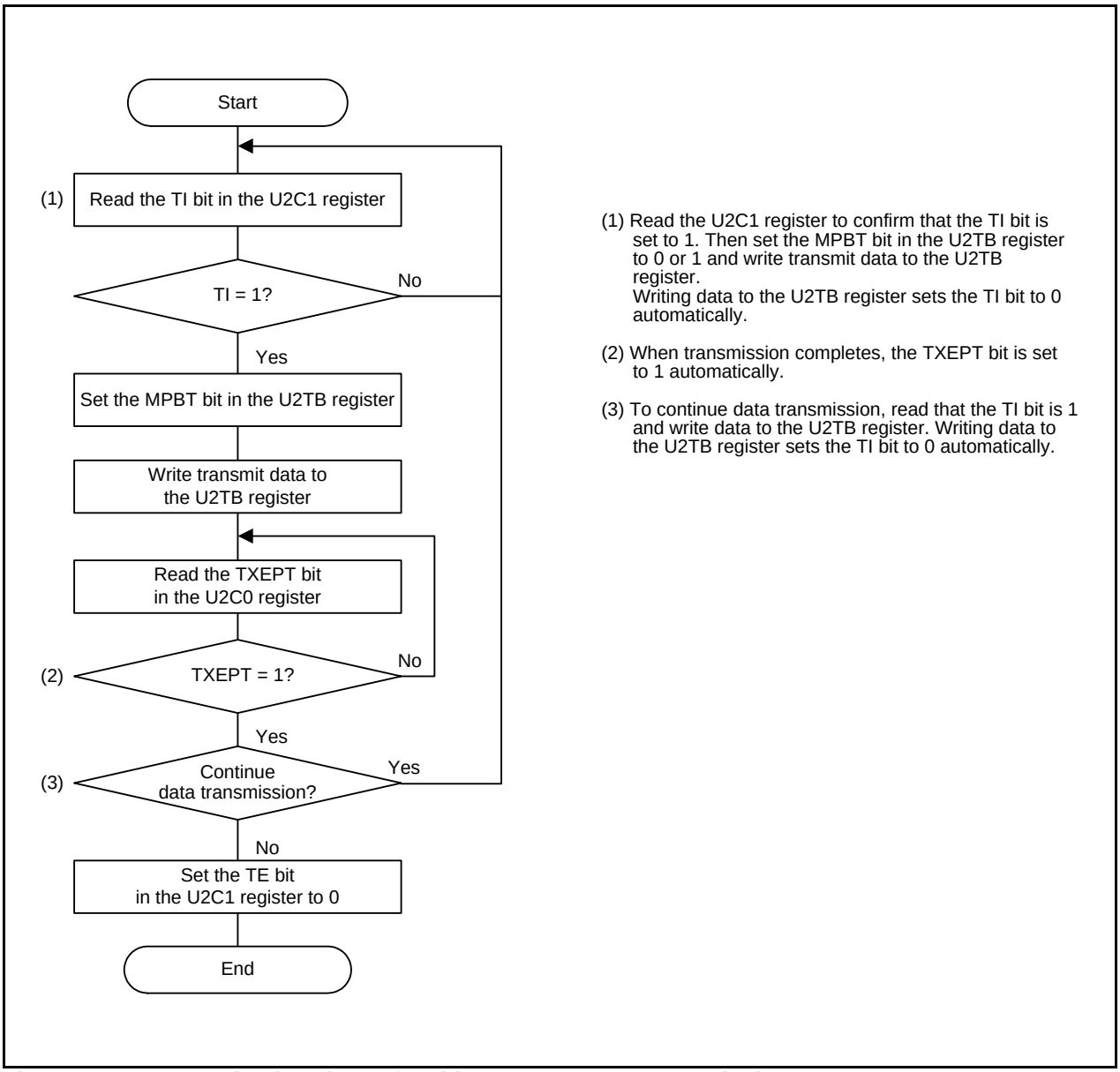


Figure 25.20 Sample Flowchart of Multiprocessor Data Transmission

25.7.2 Multiprocessor Reception

Figure 25.21 shows a Sample Flowchart of Multiprocessor Data Reception. When the MPIE bit in the U2SMR5 register is set to 1, communication data is ignored until data in which the multiprocessor bit is 1 is received. Communication data with a 1 multiprocessor bit added is transferred to the U2RB register as receive data. At this time, a reception complete interrupt request is generated. Other operations are the same as in universal asynchronous receiver/transmitter mode (UART mode). Figure 25.22 shows a Receive Operation Example during Multiprocessor Communication (with 8-Bit Data/Multiprocessor Bit/One-Stop Bit).

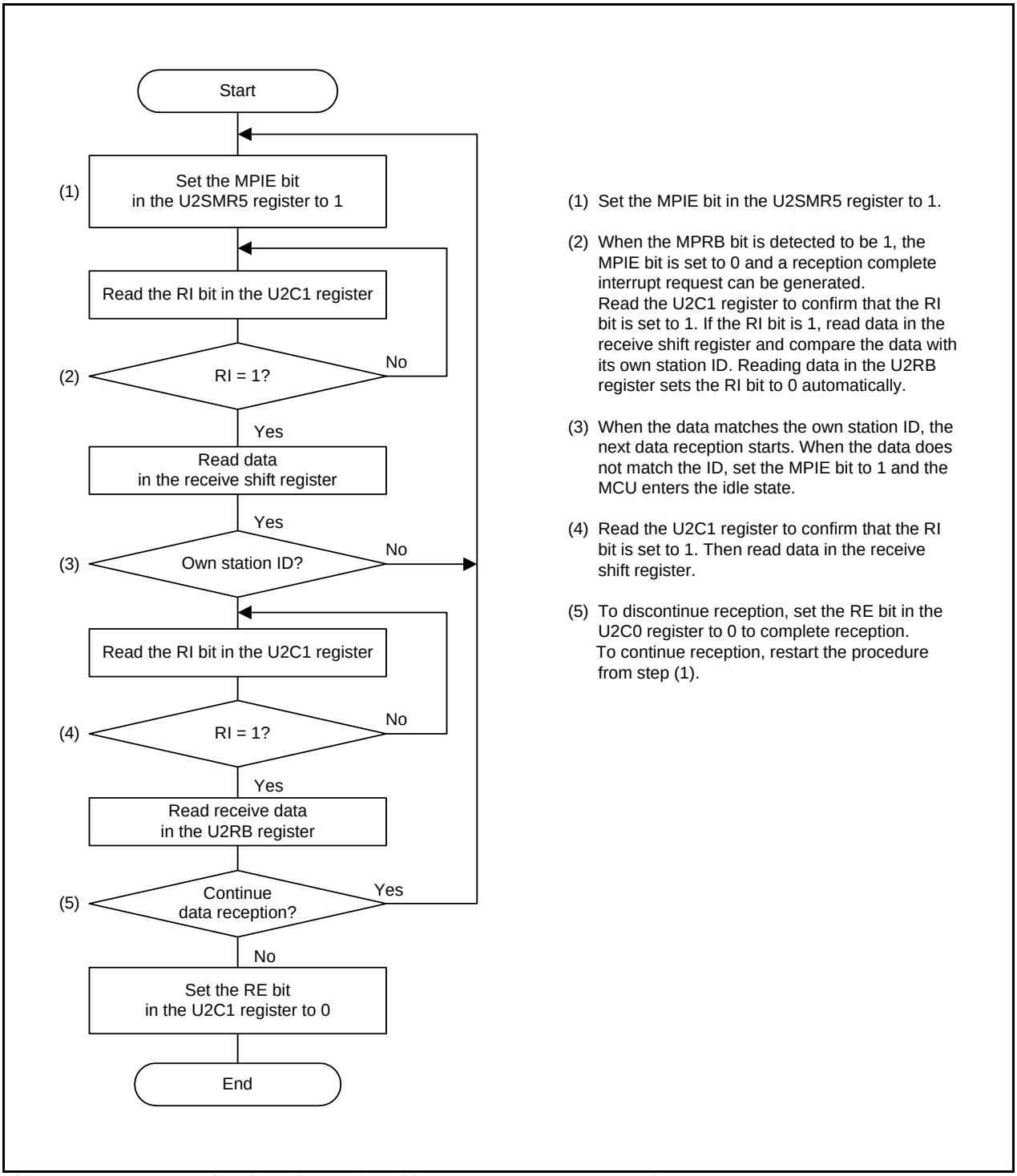


Figure 25.21 Sample Flowchart of Multiprocessor Data Reception

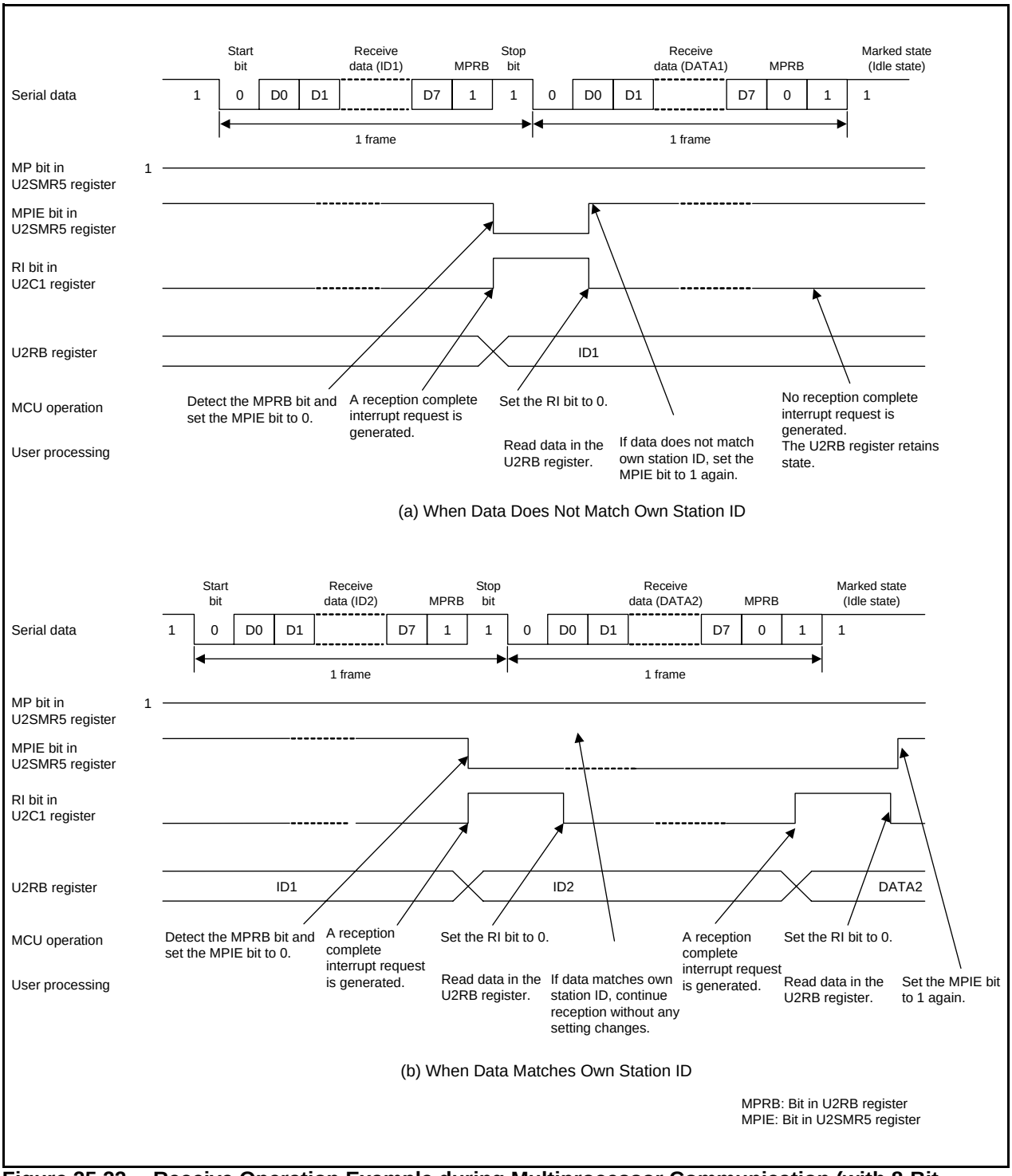
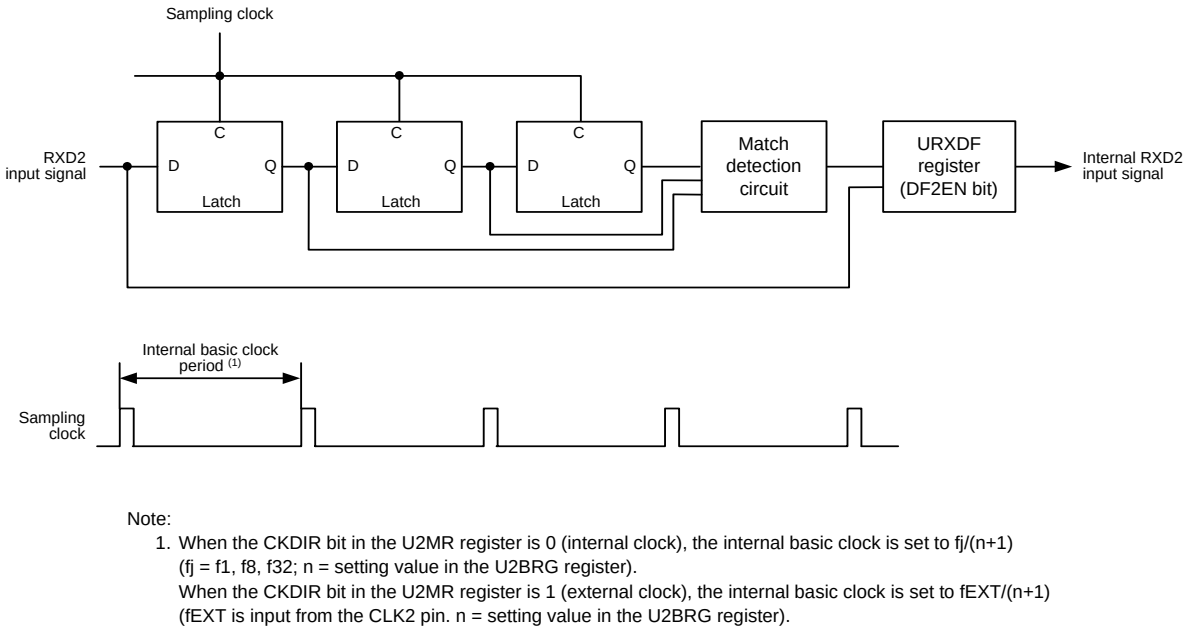


Figure 25.22 Receive Operation Example during Multiprocessor Communication (with 8-Bit Data/Multiprocessor Bit/One-Stop Bit)

25.7.3 RXD2 Digital Filter Select Function

When the DF2EN bit in the URXDF register is set to 1 (RXD2 digital filer enabled), the RXD2 input signal is loaded internally via the digital filter circuit for noise reduction. The noise canceller consists of three cascaded latch circuits and a match detection circuit. The RXD2 input signal is sampled on the internal basic clock with a frequency 16 times the bit rate. When three latch outputs match, the level is recognized as a signal and passed forward to the next circuit. When the outputs do not match, the previous value is retained.
In other words, when the level is changed within three clocks, the change is recognized as not a signal change but noise.
Figure 25.23 shows a Block Diagram of RXD2 Digital Filter Circuit.



Note:
1. When the CKDIR bit in the U2MR register is 0 (internal clock), the internal basic clock is set to fj/(n+1) (fj = f1, f8, f32; n = setting value in the U2BRG register).
When the CKDIR bit in the U2MR register is 1 (external clock), the internal basic clock is set to fEXT/(n+1) (fEXT is input from the CLK2 pin. n = setting value in the U2BRG register).

Figure 25.23 Block Diagram of RXD2 Digital Filter Circuit

25.8 Notes on Serial Interface (UART2)

25.8.1 Clock Synchronous Serial I/O Mode

25.8.1.1 Transmission/Reception

When the $\overline{\text{RTS}}$ function is used with an external clock, the $\overline{\text{RTS2}}$ pin outputs "L," which informs the transmitting side that the MCU is ready for a receive operation. The $\overline{\text{RTS2}}$ pin outputs "H" when a receive operation starts. Therefore, the transmit timing and receive timing can be synchronized by connecting the $\overline{\text{RTS2}}$ pin to the $\overline{\text{CTS2}}$ pin of the transmitting side. The $\overline{\text{RTS}}$ function is disabled when an internal clock is selected.

25.8.1.2 Transmission

If an external clock is selected, the following conditions must be met while the external clock is held high when the CKPOL bit in the U2C0 register is set to 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock), or while the external clock is held low when the CKPOL bit is set to 1 (transmit data output at the rising edge and receive data input at the falling edge of the transfer clock).

- The TE bit in the U2C1 register = 1 (transmission enabled)
- The TI bit in the U2C1 register = 0 (data present in the U2TB register)
- If the $\overline{\text{CTS}}$ function is selected, input on the $\overline{\text{CTS2}}$ pin = "L"

25.8.1.3 Reception

In clock synchronous serial I/O mode, the shift clock is generated by activating the transmitter. Set the UART2-associated registers for transmit operation even if the MCU is used for receive operation only. Dummy data is output from the TXD2 pin while receiving.

When an internal clock is selected, the shift clock is generated by setting the TE bit in the U2C1 register to 1 (transmission enabled) and placing dummy data in the U2TB register. When an external clock is selected, set the TE bit to 1 (transmission enabled), place dummy data in the U2TB register, and input an external clock to the CLK2 pin to generate the shift clock.

If data is received consecutively, an overrun error occurs when the RE bit in the U2C1 register is set to 1 (data present in the U2RB register) and the next receive data is received in the UART2 receive register. Then, the OER bit in the U2RB register is set to 1 (overrun error). At this time, the U2RB register value is undefined. If an overrun error occurs, the IR bit in the S2RIC register remains unchanged.

To receive data consecutively, set dummy data in the low-order byte in the U2TB register per each receive operation.

If an external clock is selected, the following conditions must be met while the external clock is held high when the CKPOL bit is set to 0, or while the external clock is held low when the CKPOL bit is set to 1.

- The RE bit in the U2C1 register = 1 (reception enabled)
- The TE bit in the U2C1 register = 1 (transmission enabled)
- The TI bit in the U2C1 register = 0 (data present in the U2TB register)

25.8.2 Special Mode 1 (I^2C Mode)

When generating start, stop, and restart conditions, set the STSPSEL bit in the U2SMR4 register to 0 and wait for more than half cycle of the transfer clock before changing each condition generation bit (STAREQ, RSTAREQ, and STPREQ) from 0 to 1.

25.8.3 UART2 Bit Rate Register (U2BRG)

Immediately after writing 00h to the U2BRG register, there may be a delay of up to 256 cycles of the count source when the following data transmission/reception starts (including the timing when the TI bit in the U2C1 register is set to 0 (data present in the U2TB register)) and when the start bit is detected during reception).

26. Synchronous Serial Communication Unit (SSU)

Synchronous serial communication unit (SSU) supports clock synchronous serial data communication.

26.1 Overview

Table 26.1 shows a Synchronous Serial Communication Unit Specifications and Figure 26.1 shows a Block Diagram of Synchronous Serial Communication Unit.

Table 26.1 Synchronous Serial Communication Unit Specifications

Item	Specification
Transfer data format	• Transfer data length: 8 to 16 bits Continuous transmission and reception of serial data are supported since both transmitter and receiver have buffer structures.
Operating modes	• Clock synchronous communication mode • 4-wire bus communication mode (including bidirectional communication)
Master/slave device	Selectable
I/O pins	SSCK (I/O): Clock I/O pin SSI (I/O): Data I/O pin SSO (I/O): Data I/O pin SCS (I/O): Chip-select I/O pin
Transfer clocks	• When the MSS bit in the SSCRH register is set to 0 (operates as slave device), external clock is selected (input from SSCK pin). • When the MSS bit in the SSCRH register is set to 1 (operates as master device), internal clock (selectable among f1/256, f1/128, f1/64, f1/32, f1/16, f1/8 and f1/4, output from SSCK pin) is selected. • Clock polarity and phase of SSCK can be selected.
Receive error detection	• Overrun error Overrun error occurs during reception and completes in error. While the RDRF bit in the SSSR register is set to 1 (data in the SSRDR register) and when next serial data receive is completed, the ORER bit is set to 1.
Multimaster error detection	• Conflict error When the SSUMS bit in the SSMR2 register is set to 1 (4-wire bus communication mode) and the MSS bit in the SSCRH register is set to 1 (operates as master device) and when starting a serial communication, the CE bit in the SSSR register is set to 1 if “L” applies to the SCS pin input. When the SSUMS bit in the SSMR2 register is set to 1 (4-wire bus communication mode), the MSS bit in the SSCRH register is set to 0 (operates as slave device) and the SCS pin input changes state from “L” to “H”, the CE bit in the SSSR register is set to 1.
Interrupt requests	5 interrupt requests (transmit-end, transmit-data-empty, receive-data-full, overrun error, and conflict error) (1).
Select functions	• Data transfer direction Selects MSB-first or LSB-first • SSCK clock polarity Selects “L” or “H” level when clock stops • SSCK clock phase Selects edge of data change and data download

Note:
1. Synchronous serial communication unit has only one interrupt vector table.

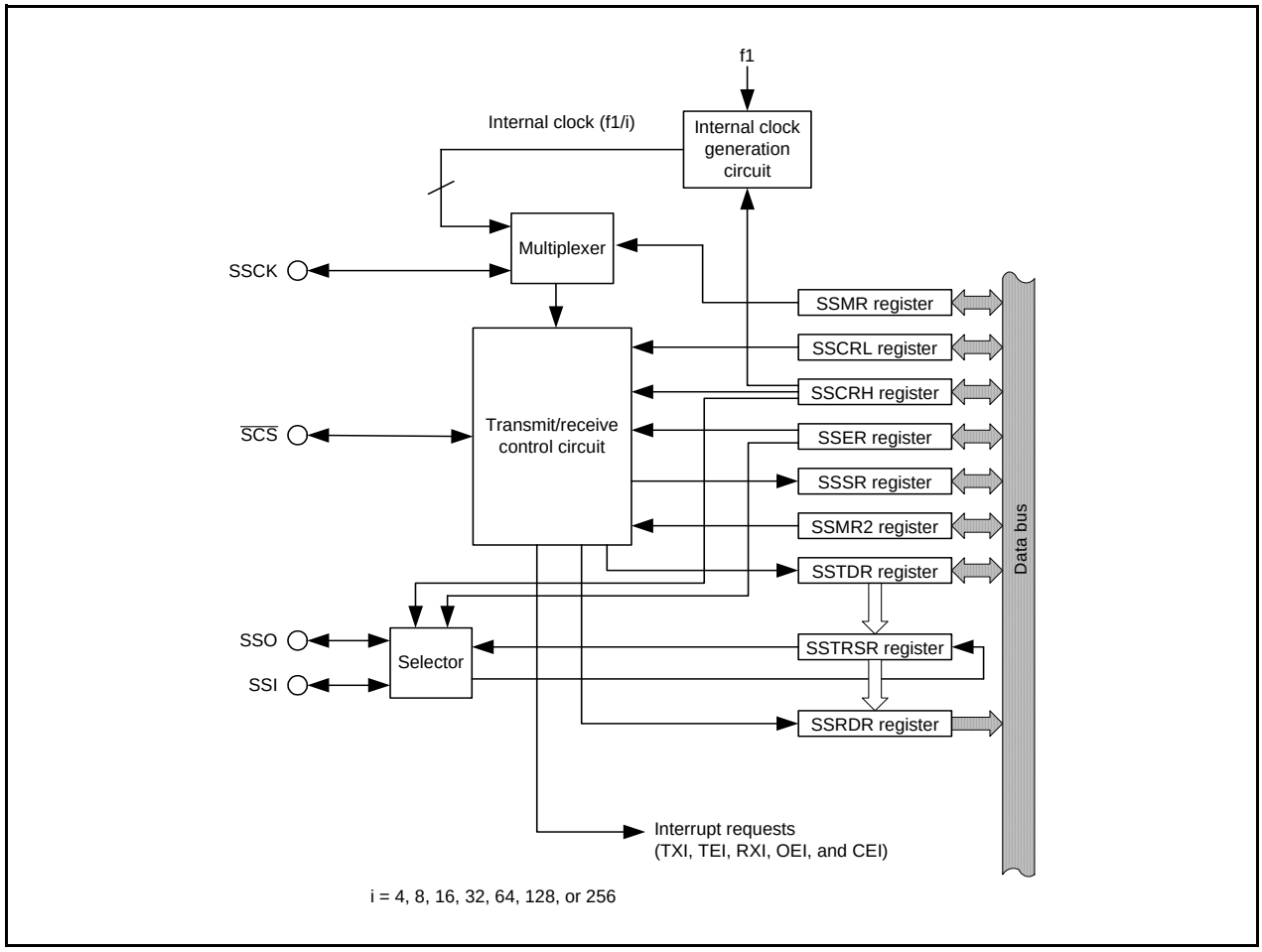


Figure 26.1 Block Diagram of Synchronous Serial Communication Unit

Table 26.2 Pin Configuration of Synchronous Serial Communication Unit

Pin Name	Assigned Pin	I/O	Function
SSI	P3_4 or P3_3	I/O	Data I/O pin
$\overline{\text{SCS}}$	P3_3 or P3_4	I/O	Chip-select signal I/O pin
SSCK	P3_5	I/O	Clock I/O pin
SSO	P3_7	I/O	Data I/O pin

26.2 Registers

26.2.1 Module Standby Control Register (MSTCR)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	MSTTRG	MSTTRC	MSTTRD	MSTIIC	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	MSTIIC	SSU standby bit	0: Active 1: Standby (1)	R/W
b4	MSTTRD	Timer RD standby bit	0: Active 1: Standby (2, 3)	R/W
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (4)	R/W
b6	MSTTRG	Timer RG standby bit	0: Active 1: Standby (5)	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. When the MSTIIC bit is set to 1 (standby), any access to the SSU associated registers (addresses 0193h to 019Dh) is disabled.
2. When the MSTTRD bit is set to 1 (standby), any access to the timer RD associated registers (addresses 0136h to 015Fh) is disabled.
3. To set the MSTTRD bit to 1 (standby), set bits TCK2 to TCK0 in the TRDCRi (i = 0 or 1) register to 000b (f1).
4. When the MSTTRC bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0120h to 0133h) is disabled.
5. When the MSTTRG bit is set to 1 (standby), any access to the timer RG associated registers (addresses 0170h to 017Fh) is disabled.

26.2.2 SSU Pin Select Register (SSUIICSR)

Address 018Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	SCSSEL0	—	SSISEL0	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	SSISEL0	SSI pin select bit	0: P3_4 assigned 1: P3_3 assigned	R/W
b5	—	Reserved bit	Set to 0.	R/W
b6	SCSSEL0	$\overline{SCS}$ pin select bit	0: P3_3 assigned 1: P3_4 assigned	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

SSISEL0 Bit (SSI pin select bit)

The SSISEL0 bit select which pin is assigned to the SSU I/O. To use the I/O pin for SSU, set this bit.
Set the SSUIICSR register setting the SSU associated registers. Also, do not change the setting value in this register during SSU operation.

SCSSEL0 Bit ($\overline{SCS}$ pin select bit)

The SCSSEL0 bit select which pin is assigned to the SSU I/O. To use the I/O pin for SSU, set this bit.
Set the SSUIICSR register setting the SSU associated registers. Also, do not change the setting value in this register during SSU operation.

26.2.3 SS Bit Counter Register (SSBR)

Address 0193h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	BS3	BS2	BS1	BS0
After Reset	1	1	1	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	BS0	SSU data transfer length set bit (1)	b3 b2 b1 b0 0 0 0 0: 16 bits 1 0 0 0: 8 bits 1 0 0 1: 9 bits 1 0 1 0: 10 bits 1 0 1 1: 11 bits 1 1 0 0: 12 bits 1 1 0 1: 13 bits 1 1 1 0: 14 bits 1 1 1 1: 15 bits	R/W
b1	BS1			R/W
b2	BS2			R/W
b3	BS3			R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	—			

Note:
1. Do not write to bits BS0 to BS3 during SSU operation.

To set the SSBR register, set the RE bit in the SSER register to 0 (reception disabled) and the TE bit to 0 (transmission disabled).

Bits BS0 to BS3 (SSU Data Transfer Length Set Bit)

As the SSU data transfer length, 8 to 16 bits can be used.

26.2.4 SS Transmit Data Register (SSTDR)

Address 0195h to 0194h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
b15 to b0	—	Store the transmit data. (1) The stored transmit data is transferred to the SSTRSR register and transmission is started when it is detected that the SSTRSR register is empty. When the next transmit data is written to the SSTDR register during the data transmission from the SSTRSR register, the data can be transmitted continuously. When the MLS bit in the SSMR register is set to 1 (transfer data with LSB-first), the data in which MSB and LSB are reversed is read, after writing to the SSTDR register.	R/W

Note:
1. When the SSU data transfer length is set to 9 bits or more with the SSBR register, access the SSTDR register in 16-bit units.

26.2.5 SS Receive Data Register (SSRDR)

Address 0197h to 0196h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
b15 to b0	—	Store the receive data. (1, 2) The receive data is transferred to the SSRDR register and the receive operation is completed when 1 byte of data has been received by the SSTRSR register. At this time, the next receive operation is possible. Continuous reception is possible using registers SSTRSR and SSRDR.	R

Notes:
1. The SSRDR register retains the data received before an overrun error occurs (ORER bit in the SSSR register set to 1 (overrun error)). When an overrun error occurs, the receive data may contain errors and therefore should be discarded.
2. When the SSU data transfer length is set to 9 bits or more with the SSBR register, access the SSRDR register in 16-bit units.

26.2.6 SS Control Register H (SSCRH)

Address 0198h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	RSSTP	MSS	—	—	CKS2	CKS1	CKS0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CKS0	Transfer clock select bit (1)	b2 b1 b0 0 0 0: f1/256 0 0 1: f1/128 0 1 0: f1/64 0 1 1: f1/32 1 0 0: f1/16 1 0 1: f1/8 1 1 0: f1/4 1 1 1: Do not set.	R/W
b1	CKS1			R/W
b2	CKS2			R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	MSS	Master/slave device select bit (2)	0: Operates as slave device 1: Operates as master device	R/W
b6	RSSTP	Receive single stop bit (3)	0: Maintains receive operation after receiving 1 byte of data 1: Completes receive operation after receiving 1 byte of data	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. The set clock is used when the MSS bit is set to 1 (operates as master device).
2. The SSCK pin functions as the transfer clock output pin when the MSS bit is set to 1 (operates as master device). The MSS bit is set to 0 (operates as slave device) when the CE bit in the SSSR register is set to 1 (conflict error occurs).
3. The RSSTP bit is disabled when the MSS bit is set to 0 (operates as slave device).

26.2.7 SS Control Register L (SSCRL)

Address 0199h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	SOL	SOLP	—	—	SRES	—
After Reset	0	1	1	1	1	1	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b1	SRES	SSU control unit reset bit	Writing 1 to this bit resets the SSU control unit and the SSTRSR register. The value in the SSU internal register (1) is retained.	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b3	—			
b4	SOLP	SOL write protect bit (2)	The output level can be changed by the SOL bit when this bit is set to 0. The SOLP bit remains unchanged even if 1 is written to it. When read, the content is 1.	R/W
b5	SOL	Serial data output value setting bit	When read 0: The serial data output is set to “L”. 1: The serial data output is set to “H”. When written (2, 3) 0: The data output is “L”. 1: The data output is “H”.	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. Registers SSBR, SSCRH, SSCRL, SSMR, SSER, SSSR, SSMR2, SSTDR, and SSRDR.
2. For the data output after serial data transmission, the last bit value of the transmitted serial data is retained.
   If the content of the SOL bit is rewritten before or after serial data transmission, the change is immediately reflected in the data output.
   When writing to the SOL bit, set the SOLP bit to 0 and the SOL bit to 0 or 1 simultaneously by the MOV instruction.
3. Do not write to the SOL bit during data transfer.

26.2.8 SS Mode Register (SSMR)

Address 019Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	MLS	CPOS	CPHS	—	BC3	BC2	BC1	BC0
After Reset	0	0	0	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	BC0	Bits counter 3 to 0	b3 b2 b1 b0 0 0 0 0: 16 bits left 0 0 0 1: 1 bit left 0 0 1 0: 2 bits left 0 0 1 1: 3 bits left 0 1 0 0: 4 bits left 0 1 0 1: 5 bits left 0 1 1 0: 6 bits left 0 1 1 1: 7 bits left 1 0 0 0: 8 bits left 1 0 0 1: 9 bits left 1 0 1 0: 10 bits left 1 0 1 1: 11 bits left 1 1 0 0: 12 bits left 1 1 0 1: 13 bits left 1 1 1 0: 14 bits left 1 1 1 1: 15 bits left	R
b1	BC1			R
b2	BC2			R
b3	BC3			R
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	CPHS	SSCK clock phase select bit (1)	0: Change data at odd edge (Download data at even edge) 1: Change data at even edge (Download data at odd edge)	R/W
b6	CPOS	SSCK clock polarity select bit (1)	0: “H” when clock stops 1: “L” when clock stops	R/W
b7	MLS	MSB first/LSB first select bit	0: Transfers data MSB first 1: Transfers data LSB first	R/W

Note:

1. Refer to **26.3.1.1 Association between Transfer Clock Polarity, Phase, and Data** for the settings of the CPHS and CPOS bits.
   When the SSUMS bit in the SSMR2 register is set to 0 (clock synchronous communication mode), set the CPHS bit to 0 and the CPOS bit to 0.

26.2.9 SS Enable Register (SSER)

Address 019Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIE	TEIE	RIE	TE	RE	—	—	CEIE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CEIE	Conflict error interrupt enable bit	0: Disables conflict error interrupt request 1: Enables conflict error interrupt request	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	RE	Receive enable bit	0: Disables receive 1: Enables receive	R/W
b4	TE	Transmit enable bit	0: Disables transmit 1: Enables transmit	R/W
b5	RIE	Receive interrupt enable bit	0: Disables receive data full and overrun error interrupt request 1: Enables receive data full and overrun error interrupt request	R/W
b6	TEIE	Transmit end interrupt enable bit	0: Disables transmit end interrupt request 1: Enables transmit end interrupt request	R/W
b7	TIE	Transmit interrupt enable bit	0: Disables transmit data empty interrupt request 1: Enables transmit data empty interrupt request	R/W

26.2.10 SS Status Register (SSSR)

Address 019Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TDRE	TEND	RDRF	—	—	ORER	—	CE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CE	Conflict error flag (1)	0: No conflict errors generated 1: Conflict errors generated (2)	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	ORER	Overrun error flag (1)	0: No overrun errors generated 1: Overrun errors generated (3)	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	RDRF	Receive data register full flag (1, 4)	0: No data in SSRDR register 1: Data in SSRDR register	R/W
b6	TEND	Transmit end flag (1, 5)	0: The TDRE bit is set to 0 when transmitting the last bit of transmit data 1: The TDRE bit is set to 1 when transmitting the last bit of transmit data	R/W
b7	TDRE	Transmit data empty flag (1, 5, 6)	0: Data is not transferred from registers SSTDR to SSTRSR 1: Data is transferred from registers SSTDR to SSTRSR	R/W

Notes:

1. Writing 1 to CE, ORER, RDRF, TEND, or TDRE bits is invalid. To set any of these bits to 0, first read 1 then write 0.
2. When the serial communication is started while the SSUMS bit in the SSMR2 register is set to 1 (four-wire bus communication mode) and the MSS bit in the SSCRH register is set to 1 (operates as master device), the CE bit is set to 1 if “L” is applied to the $\overline{\text{SCS}}$ pin input. Refer to **26.5.4 SCS Pin Control and Arbitration** for more information.
   When the SSUMS bit in the SSMR2 register is set to 1 (four-wire bus communication mode), the MSS bit in the SSCRH register is set to 0 (operates as slave device) and the $\overline{\text{SCS}}$ pin input changes the level from “L” to “H” during transfer, the CE bit is set to 1.
3. Indicates when overrun errors occur and receive completes by error reception. If the next serial data receive operation is completed while the RDRF bit is set to 1 (data in the SSRDR register), the ORER bit is set to 1.
   After the ORER bit is set to 1 (overrun error), receive operation is disabled while the bit remains 1.
4. The RDRF bit is set to 0 when reading out the data from the SSRDR register.
5. Bits TEND and TDRE are set to 0 when writing data to the SSTDR register.
6. The TDRE bit is set to 1 when the TE bit in the SSER register is set to 1 (transmit enabled).

If the SSSR register is accessed continuously, insert one or more NOP instructions between the instructions used for access.

26.2.11 SS Mode Register 2 (SSMR2)

Address 019Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BIDE	SCKS	CSS1	CSS0	SCKOS	SOOS	CSOS	SSUMS
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SSUMS	SSU mode select bit (1)	0: Clock synchronous communication mode 1: Four-wire bus communication mode	R/W
b1	CSOS	$\overline{SCS}$ pin open drain output select bit	0: CMOS output 1: N-channel open-drain output	R/W
b2	SOOS	Serial data pin open output drain select bit (1)	0: CMOS output (5) 1: N-channel open-drain output	R/W
b3	SCKOS	SSCK pin open drain output select bit	0: CMOS output 1: N-channel open-drain output	R/W
b4	CSS0	$\overline{SCS}$ pin select bit (2)	b5 b4 0 0: Functions as port 0 1: Functions as $\overline{SCS}$ input pin 1 0: Functions as $\overline{SCS}$ output pin (3) 1 1: Functions as $\overline{SCS}$ output pin (3)	R/W
b5	CSS1			R/W
b6	SCKS	SSCK pin select bit	0: Functions as port 1: Functions as serial clock pin	R/W
b7	BIDE	Bidirectional mode enable bit (1, 4)	0: Standard mode (communication using 2 pins of data input and data output) 1: Bidirectional mode (communication using 1 pin of data input and data output)	R/W

Notes:
1. Refer to **26.3.2.1 Association between Data I/O Pins and SS Shift Register** for information on combinations of data I/O pins.
2. The $\overline{SCS}$ pin functions as a port, regardless of the values of bits CSS0 and CSS1 when the SSUMS bit is set to 0 (clock synchronous communication mode).
3. This bit functions as the $\overline{SCS}$ input pin before starting transfer.
4. The BIDE bit is disabled when the SSUMS bit is set to 0 (clock synchronous communication mode).
5. When the SOOS bit is set to 0 (CMOS output), set the port direction register bits corresponding to pins SSI and SSO to 0 (input mode).

26.3 Common Items for Multiple Modes

26.3.1 Transfer Clock

The transfer clock can be selected from among seven internal clocks (f1/256, f1/128, f1/64, f1/32, f1/16, f1/8, and f1/4) and an external clock.
When using synchronous serial communication unit, set the SCKS bit in the SSMR2 register to 1 and select the SSCK pin as the serial clock pin.
When the MSS bit in the SSCRH register is set to 1 (operates as master device), an internal clock can be selected and the SSCK pin functions as output. When transfer is started, the SSCK pin outputs clocks of the transfer rate selected by bits CKS0 to CKS2 in the SSCRH register.
When the MSS bit in the SSCRH register is set to 0 (operates as slave device), an external clock can be selected and the SSCK pin functions as input.

26.3.1.1 Association between Transfer Clock Polarity, Phase, and Data

The association between the transfer clock polarity, phase and data changes according to the combination of the SSUMS bit in the SSMR2 register and bits CPHS and CPOS in the SSMR register.
Figure 26.2 shows the Association between Transfer Clock Polarity, Phase, and Transfer Data.
Also, the MSB-first transfer or LSB-first transfer can be selected by setting the MLS bit in the SSMR register. When the MLS bit is set to 1, transfer is started from the LSB and proceeds to the MSB. When the MLS bit is set to 0, transfer is started from the MSB and proceeds to the LSB.

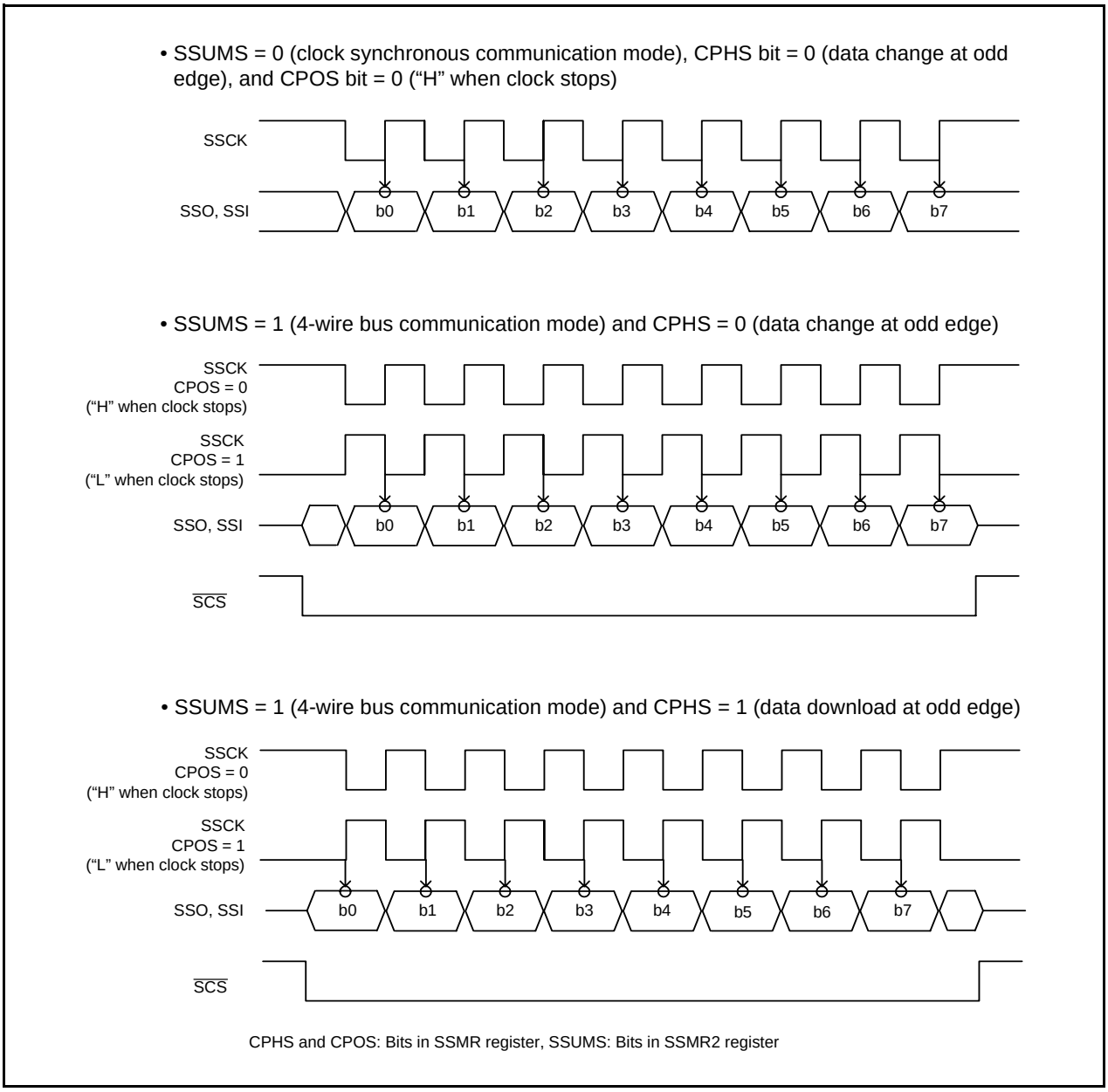


Figure 26.2 Association between Transfer Clock Polarity, Phase, and Transfer Data

26.3.2 SS Shift Register (SSTRSR)

The SSTRSR register is a shift register for transmitting and receiving serial data.
When transmit data is transferred from the SSTDR register to the SSTRSR register and the MLS bit in the SSMR register is set to 0 (MSB-first), the bit 0 in the SSTDR register is transferred to bit 0 in the SSTRSR register. When the MLS bit is set to 1 (LSB-first), bit 7 in the SSTDR register is transferred to bit 0 in the SSTRSR register.

26.3.2.1 Association between Data I/O Pins and SS Shift Register

The connection between the data I/O pins and SSTRSR register (SS shift register) changes according to a combination of the MSS bit in the SSCRH register and the SSUMS bit in the SSMR2 register. The connection also changes according to the BIDE bit in the SSMR2 register.
Figure 26.3 shows the Association between Data I/O Pins and SSTRSR Register.

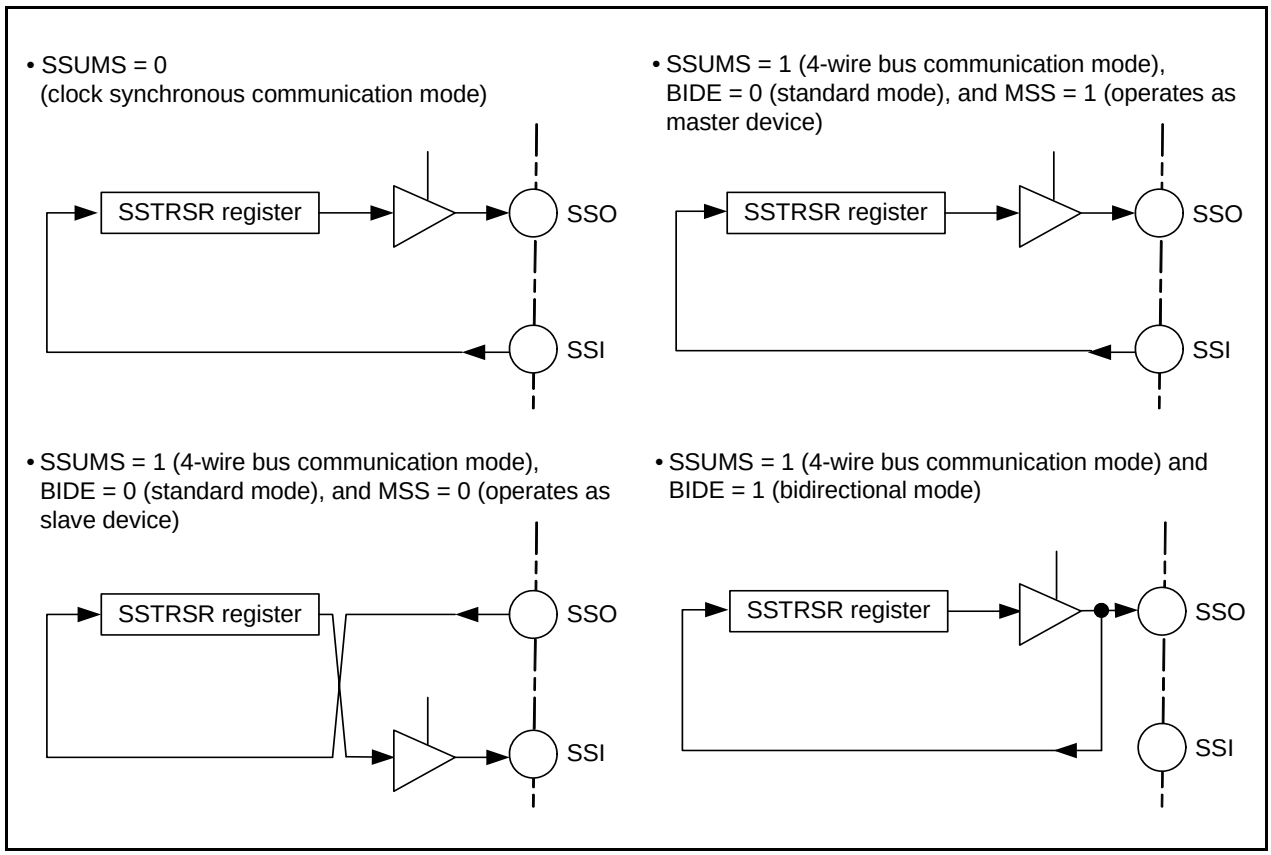


Figure 26.3 Association between Data I/O Pins and SSTRSR Register

26.3.3 Interrupt Requests

Synchronous serial communication unit has five interrupt requests: transmit data empty, transmit end, receive data full, overrun error, and conflict error. Since these interrupt requests are assigned to the synchronous serial communication unit interrupt vector table, determining interrupt sources by flags is required.
Table 26.3 shows the Synchronous Serial Communication Unit Interrupt Requests.

Table 26.3 Synchronous Serial Communication Unit Interrupt Requests

Interrupt Request	Abbreviation	Generation Condition
Transmit data empty	TXI	TIE = 1, TDRE = 1
Transmit end	TEI	TEIE = 1, TEND = 1
Receive data full	RXI	RIE = 1, RDRF = 1
Overrun error	OEI	RIE = 1, ORER = 1
Conflict error	CEI	CEIE = 1, CE = 1

CEIE, RIE, TEIE and TIE: Bits in SSER register
ORER, RDRF, TEND and TDRE: Bits in SSSR register

If the generation conditions in Table 26.3 are met, a synchronous serial communication unit interrupt request is generated. Set each interrupt source to 0 by a synchronous serial communication unit interrupt routine.

However, the TDRE and TEND bits are automatically set to 0 by writing transmit data to the SSTDR register and the RDRF bit is automatically set to 0 by reading the SSRDR register. In particular, the TDRE bit is set to 1 (data transmitted from registers SSTDR to SSTRSR) at the same time transmit data is written to the SSTDR register. Setting the TDRE bit to 0 (data not transmitted from registers SSTDR to SSTRSR) can cause an additional byte of data to be transmitted.

26.3.4 Communication Modes and Pin Functions

Synchronous serial communication unit switches the functions of the I/O pins in each communication mode according to the setting of the MSS bit in the SSCRH register and bits RE and TE in the SSER register. Table 26.4 shows the Association between Communication Modes and I/O Pins.

Table 26.4 Association between Communication Modes and I/O Pins

Communication Mode	Bit Setting					Pin State		
	SSUMS	BIDE	MSS	TE	RE	SSI	SSO	SSCK
Clock synchronous communication mode	0	Disabled	0	0	1	Input	– (1)	Input
				1	0	– (1)	Output	Input
					1	Input	Output	Input
			1	0	1	Input	– (1)	Output
				1	0	– (1)	Output	Output
					1	Input	Output	Output
4-wire bus communication mode	1	0	0	0	1	– (1)	Input	Input
				1	0	Output	– (1)	Input
					1	Output	Input	Input
			1	0	1	Input	– (1)	Output
				1	0	– (1)	Output	Output
					1	Input	Output	Output
4-wire bus (bidirectional) communication mode (2)	1	1	0	0	1	– (1)	Input	Input
				1	0	– (1)	Output	Input
			1	0	1	– (1)	Input	Output
				1	0	– (1)	Output	Output

Notes:
1. This pin can be used as a programmable I/O port.
2. Do not set both bits TE and RE to 1 in 4-wire bus (bidirectional) communication mode.

SSUMS and BIDE: Bits in SSMR2 register
MSS: Bit in SSCRH register
TE and RE: Bits in SSER register

26.4 Clock Synchronous Communication Mode

26.4.1 Initialization in Clock Synchronous Communication Mode

Figure 26.4 shows Initialization in Clock Synchronous Communication Mode. To initialize, set the TE bit in the SSER register to 0 (transmit disabled) and the RE bit to 0 (receive disabled) before data transmission or reception.
Set the TE bit to 0 and the RE bit to 0 before changing the communication mode or format.
Setting the RE bit to 0 does not change the contents of flags RDRF and ORER or the contents of the SSRDR register.

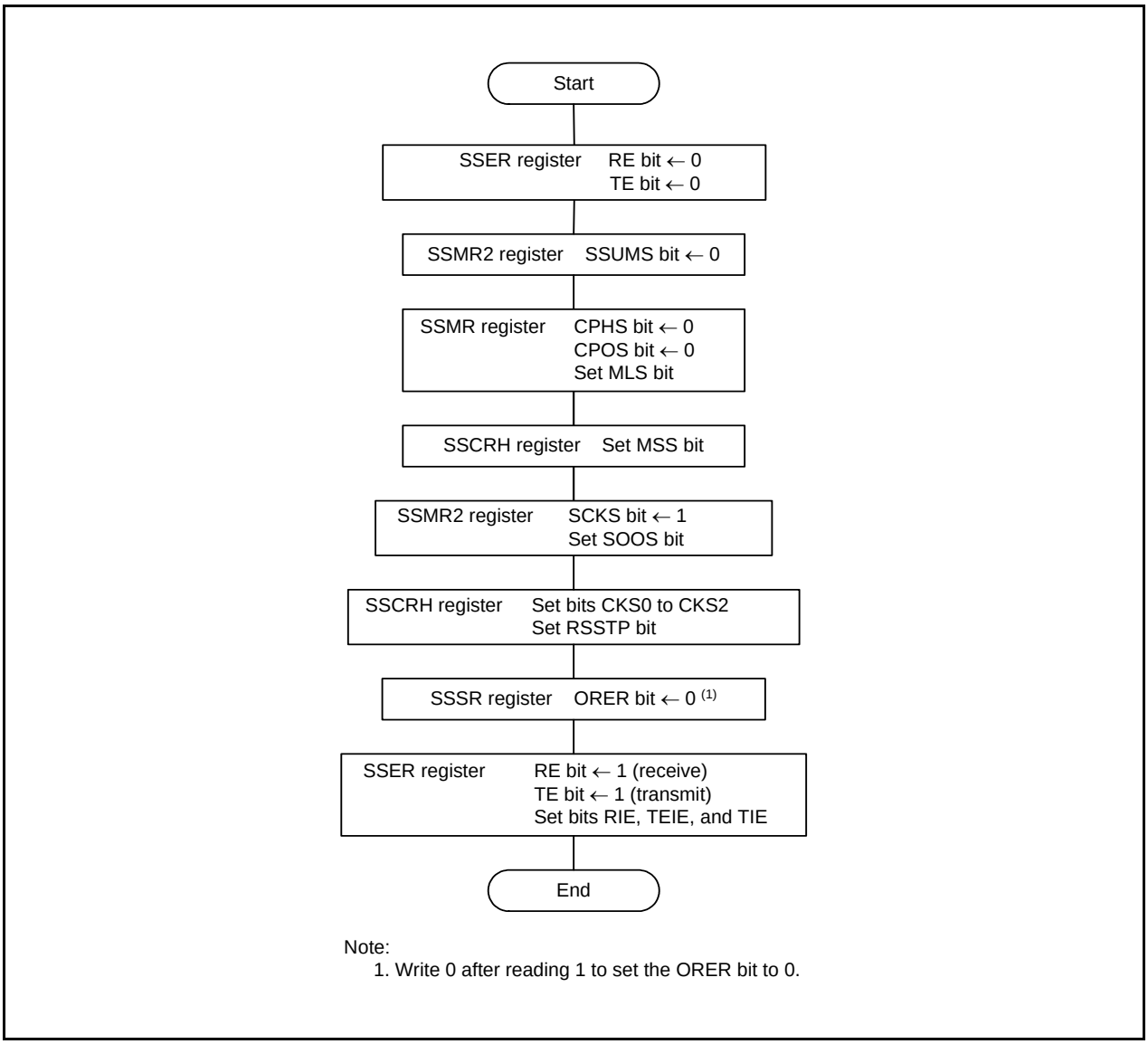


Figure 26.4 Initialization in Clock Synchronous Communication Mode

26.4.2 Data Transmission

Figure 26.5 shows an Example of Synchronous Serial Communication Unit Operation for Data Transmission (Clock Synchronous Communication Mode, 8-Bit SSU Data Transfer Length). During data transmission, the synchronous serial communication unit operates as described below. (The data transfer length can be set from 8 to 16 bits using the SSBR register).

When synchronous serial communication unit is set as a master device, it outputs a synchronous clock and data. When synchronous serial communication unit is set as a slave device, it outputs data synchronized with the input clock.

When the TE bit is set to 1 (transmit enabled) before writing the transmit data to the SSTDR register, the TDRE bit is automatically set to 0 (data not transferred from registers SSTDR to SSTRSR) and the data is transferred from registers SSTDR to SSTRSR.

After the TDRE bit is set to 1 (data transferred from registers SSTDR to SSTRSR), transmission starts. When the TIE bit in the SSER register is set to 1, the TXI interrupt request is generated. When one frame of data is transferred while the TDRE bit is set to 0, data is transferred from registers SSTDR to SSTRSR and transmission of the next frame is started. If the 8th bit is transmitted while the TDRE bit is set to 1, the TEND bit in the SSSR register is set to 1 (the TDRE bit is set to 1 when the last bit of the transmit data is transmitted) and the state is retained. The TEI interrupt request is generated when the TEIE bit in the SSER register is set to 1 (transmit-end interrupt request enabled). The SSCK pin is fixed “H” after transmit-end.

Transmission cannot be performed while the ORER bit in the SSSR register is set to 1 (overrun error). Confirm that the ORER bit is set to 0 before transmission.

Figure 26.6 shows a Sample Flowchart of Data Transmission (Clock Synchronous Communication Mode).

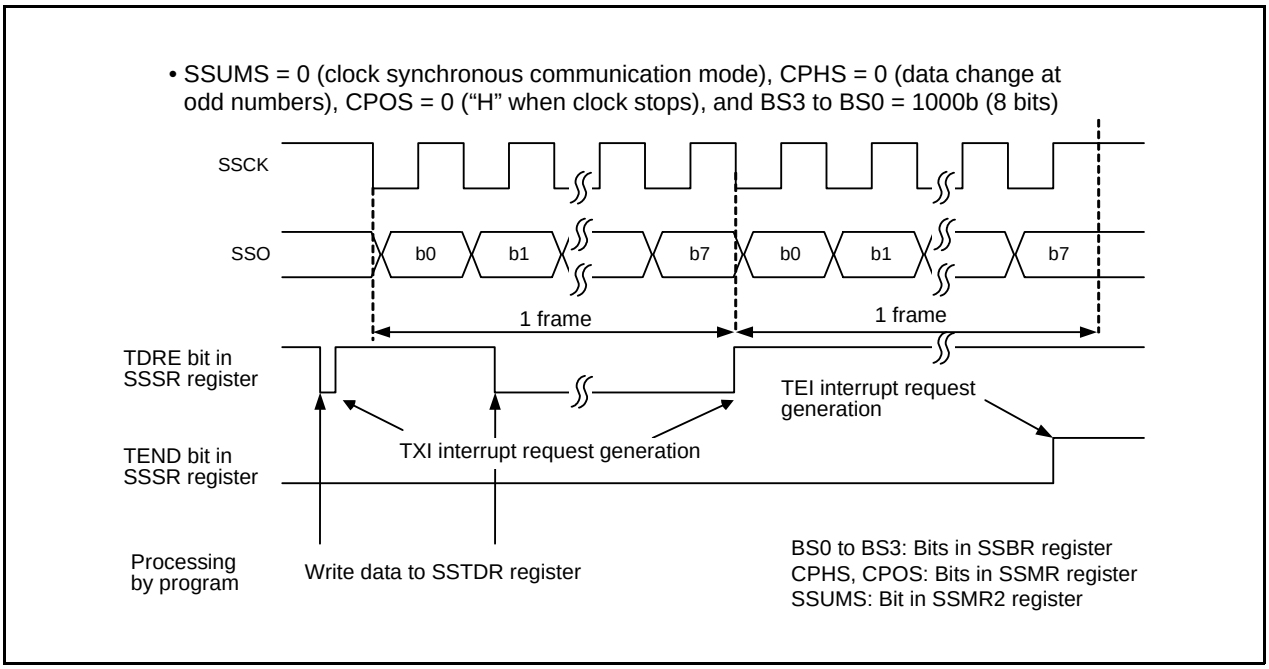


Figure 26.5 Example of Synchronous Serial Communication Unit Operation for Data Transmission (Clock Synchronous Communication Mode, 8-Bit SSU Data Transfer Length)

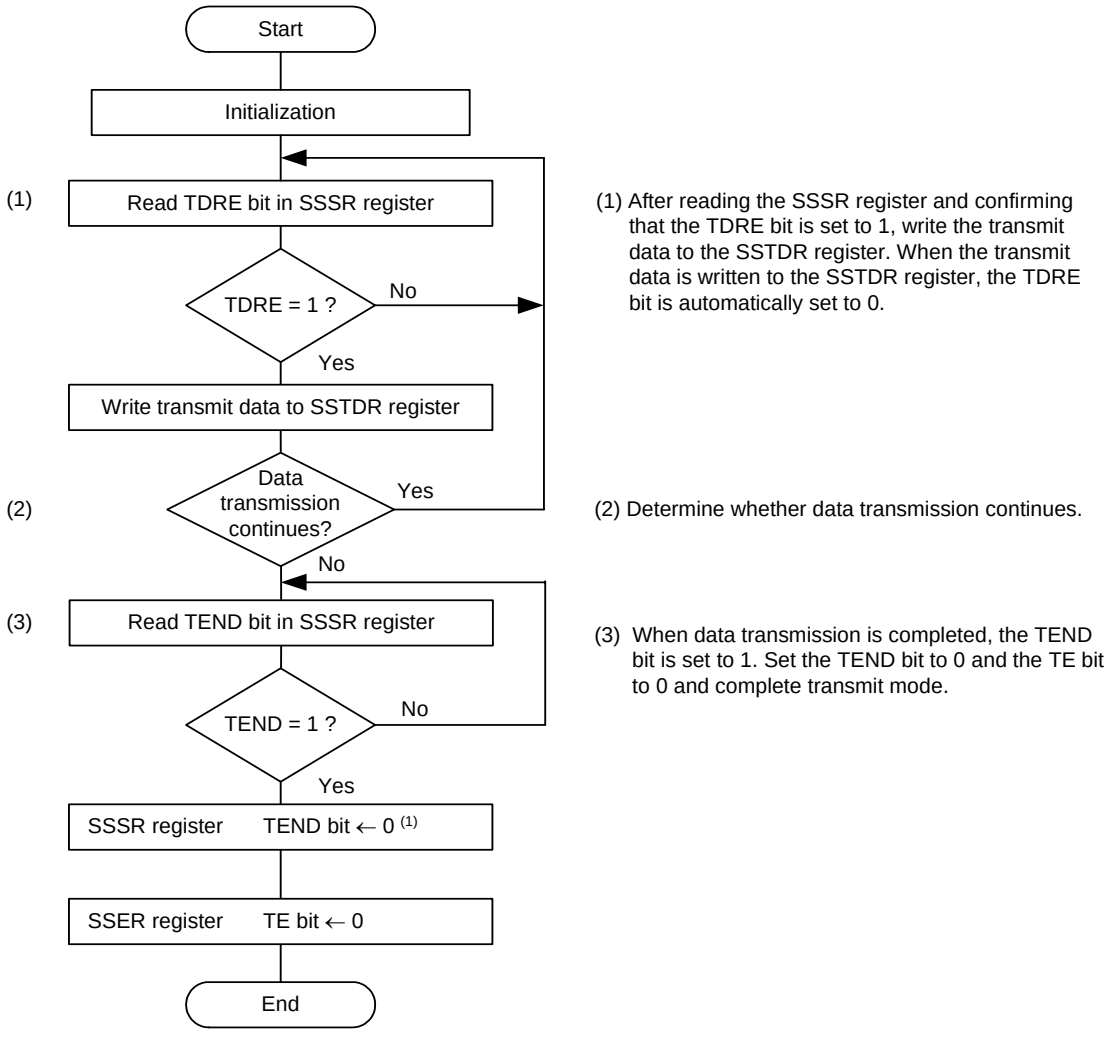


Figure 26.6 Sample Flowchart of Data Transmission (Clock Synchronous Communication Mode)

26.4.3 Data Reception

Figure 26.7 shows an Example of Synchronous Serial Communication Unit Operation for Data Reception (Clock Synchronous Communication Mode, 8-Bit SSU Data Transfer Length). During data reception, synchronous serial communication unit operates as described below. (The data transfer length can be set from 8 to 16 bits using the SSBR register).

When the synchronous serial communication unit is set as the master device, it outputs a synchronous clock and inputs data. When synchronous serial communication unit is set as a slave device, it inputs data synchronized with the input clock.

When synchronous serial communication unit is set as a master device, it outputs a receive clock and starts receiving by performing dummy read of the SSRDR register.

After 8 bits of data are received, the RDRF bit in the SSSR register is set to 1 (data in the SSRDR register) and receive data is stored in the SSRDR register. When the RIE bit in the SSER register is set to 1 (RXI and OEI interrupt requests enabled), the RXI interrupt request is generated. If the SSDR register is read, the RDRF bit is automatically set to 0 (no data in the SSRDR register).

Read the receive data after setting the RSSTP bit in the SSCRH register to 1 (after receiving 1 byte of data, the receive operation is completed). Synchronous serial communication unit outputs a clock for receiving 8 bits of data and stops. After that, set the RE bit in the SSER register to 0 (receive disabled) and the RSSTP bit to 0 (receive operation is continued after receiving the 1 byte of data) and read the receive data. If the SSRDR register is read while the RE bit is set to 1 (receive enabled), a receive clock is output again.

When the 8th clock rises while the RDRF bit is set to 1, the ORER bit in the SSSR register is set to 1 (overrun error: OEI) and the operation is stopped. When the ORER bit is set to 1, receive cannot be performed. Confirm that the ORER bit is set to 0 before restarting receive.

Figure 26.8 shows a Sample Flowchart of Data Reception (MSS = 1) (Clock Synchronous Communication Mode).

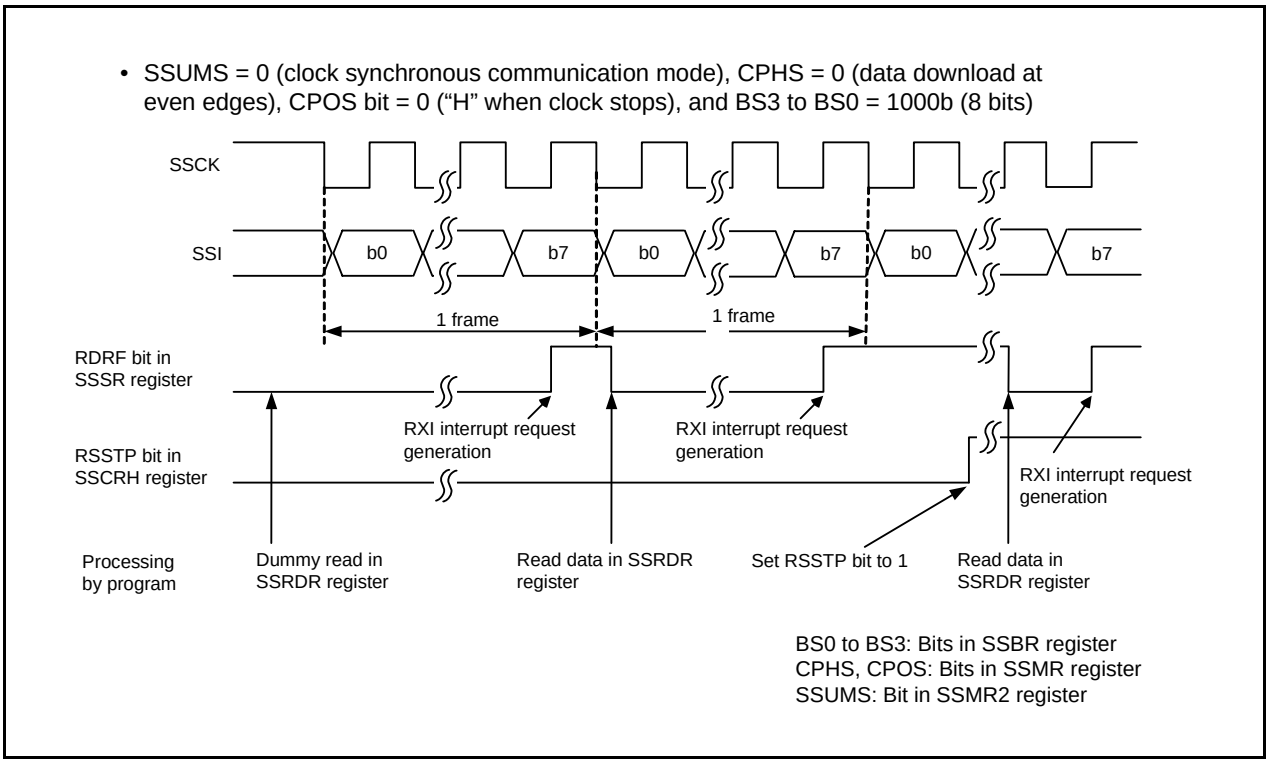


Figure 26.7 Example of Synchronous Serial Communication Unit Operation for Data Reception (Clock Synchronous Communication Mode, 8-Bit SSU Data Transfer Length)

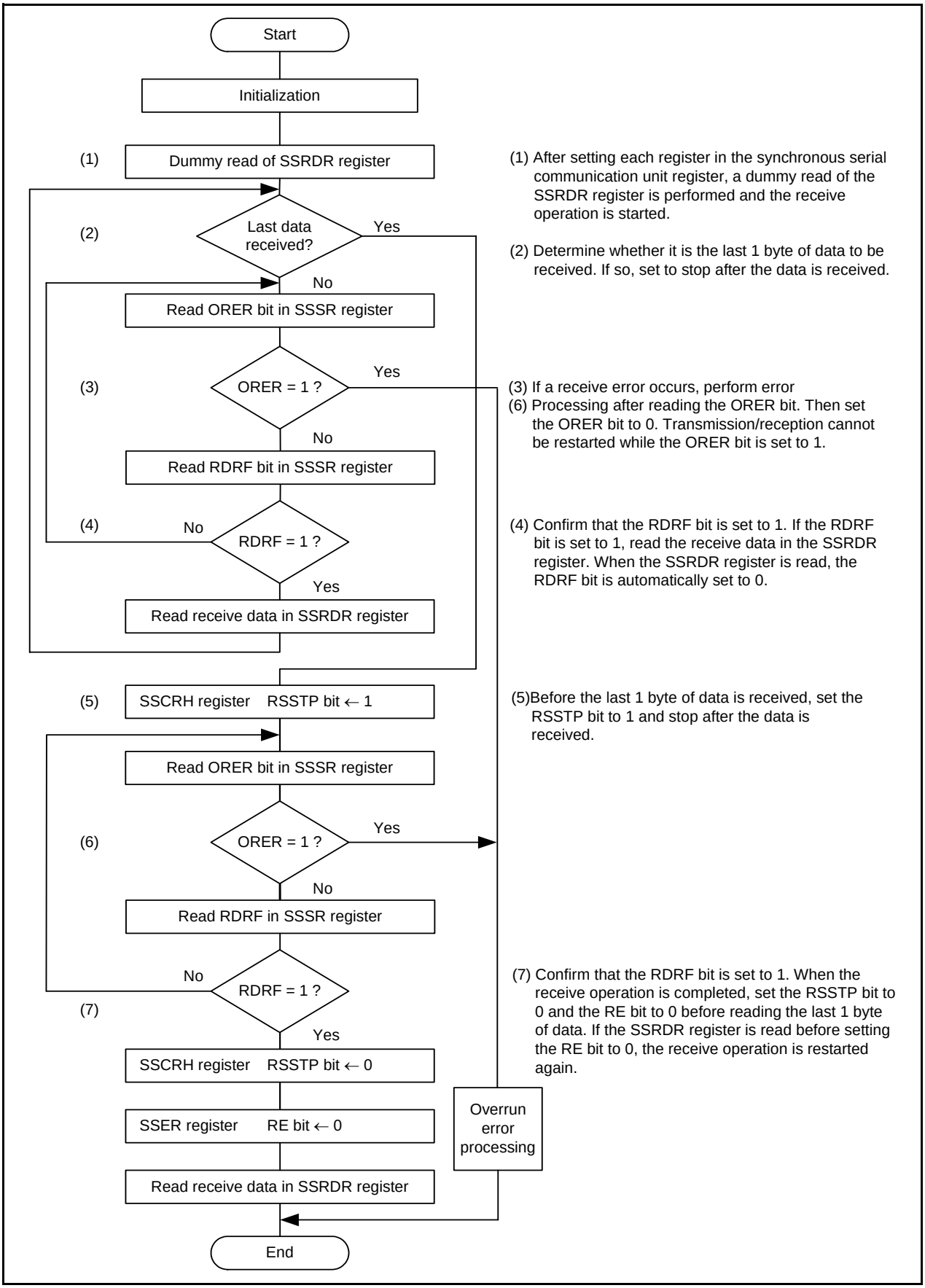


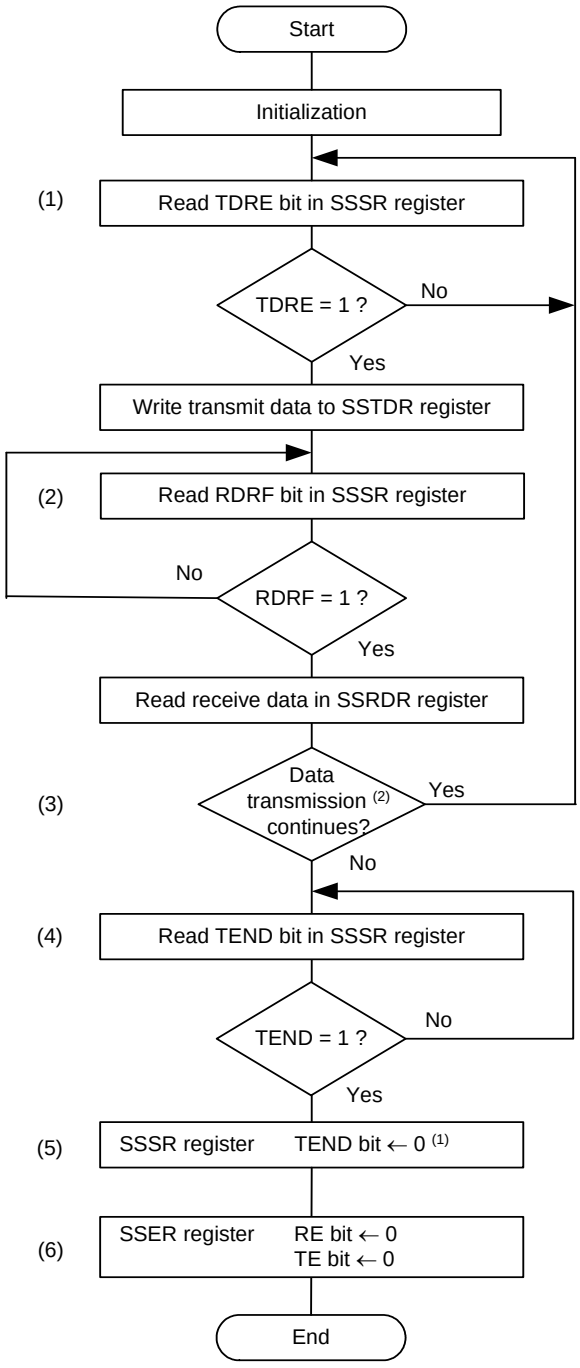
Figure 26.8 Sample Flowchart of Data Reception (MSS = 1) (Clock Synchronous Communication Mode)

26.4.3.1 Data Transmission/Reception

Data transmission/reception is an operation combining data transmission and reception which were described earlier. Transmission/reception is started by writing data to the SSTDR register.
When the last transfer clock (the data transfer length can be set from 8 to 16 bits using the SSBR register) rises or the ORER bit is set to 1 (overrun error) while the TDRE bit is set to 1 (data is transferred from registers SSTDR to SSTRSR), the transmit/receive operation is stopped.
When switching from transmit mode (TE = 1) or receive mode (RE = 1) to transmit/receive mode (TE = RE = 1), set the TE bit to 0 and RE bit to 0 before switching. After confirming that the TEND bit is set to 0 (the TDRE bit is set to 0 when the last bit of the transmit data is transmitted), the RDRF bit is set to 0 (no data in the SSRDR register), and the ORER bit is set to 0 (no overrun error), set bits TE and RE to 1.
Figure 26.9 shows a Sample Flowchart of Data Transmission/Reception (Clock Synchronous Communication Mode).
When exiting transmit/receive mode after this mode is used (TE = RE = 1), a clock may be output if transmit/receive mode is exited after reading the SSRDR register. To avoid any clock outputs, perform either of the following:

- First set the RE bit to 0, and then set the TE bit to 0.
- Set bits TE and RE at the same time.

When subsequently switching to receive mode (TE = 0 and RE = 1), first set the SRES bit to 1, and set this bit to 0 to reset the SSU control unit and the SSTRSR register. Then, set the RE bit to 1.



(1) After reading the SSSR register and confirming that the TDRE bit is set to 1, write the transmit data to the SSTDR register. When the transmit data is written to the SSTDR register, the TDRE bit is automatically set to 0.

(2) Confirm that the RDRF bit is set to 1. If the RDRF bit is set to 1, read the receive data in the SSRDR register. When the SSRDR register is read, the RDRF bit is automatically set to 0.

(3) Determine whether the data transmission continues

(4) When the data transmission is completed, the TEND bit in the SSSR register is set to 1.

(5) Set the TEND bit to 0 and bits RE and TE in
(6) the SSER register to 0 before ending transmit/ receive mode.

Note:
1. Write 0 after reading 1 to set the TEND bit to 0.

Figure 26.9 Sample Flowchart of Data Transmission/Reception (Clock Synchronous Communication Mode)

26.5 Operation in 4-Wire Bus Communication Mode

In 4-wire bus communication mode, a 4-wire bus consisting of a clock line, a data input line, a data output line, and a chip select line is used for communication. This mode includes bidirectional mode in which the data input line and data output line function as a single pin.

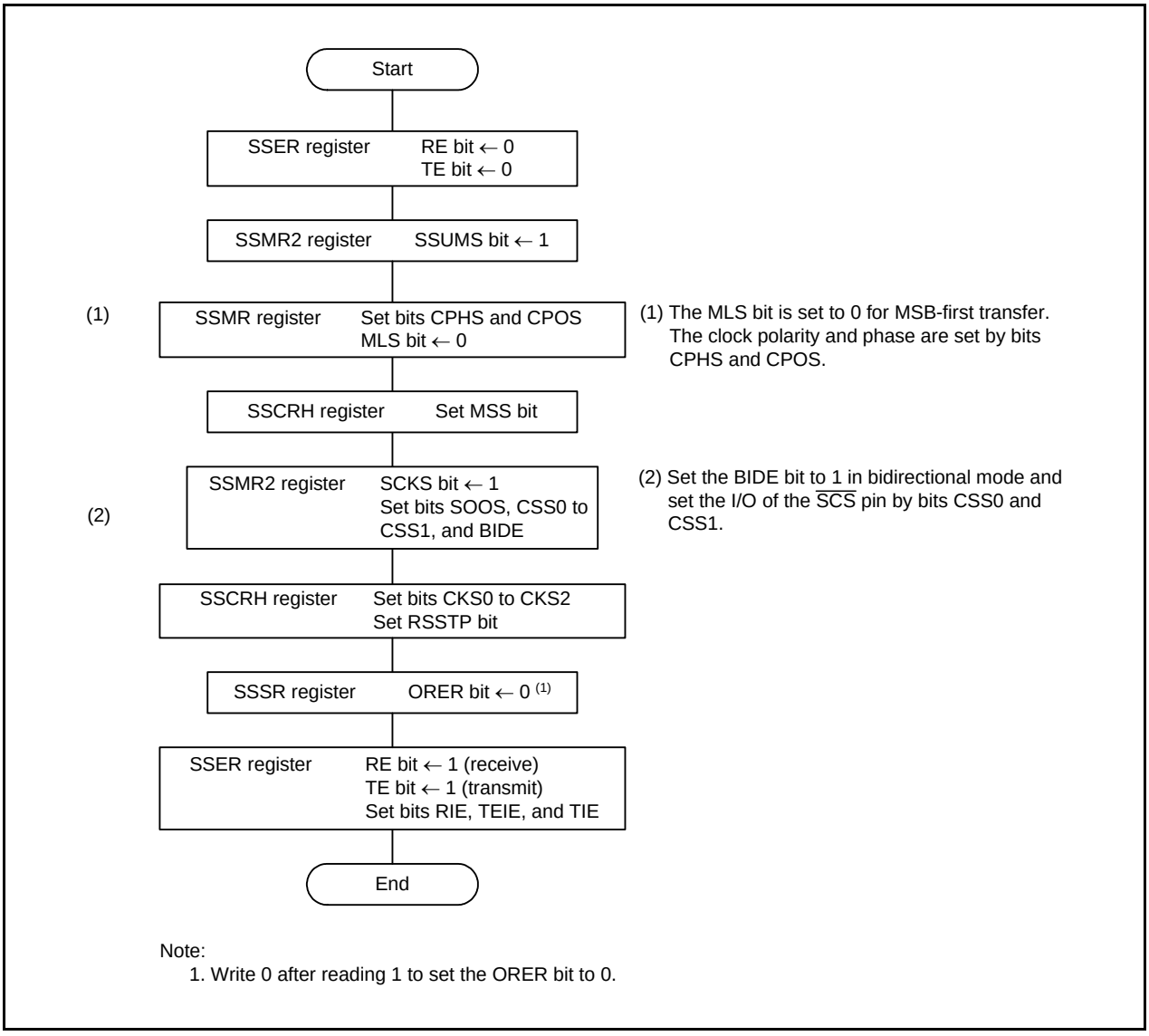
The data input line and output line change according to the settings of the MSS bit in the SSCRH register and the BIDE bit in the SSMR2 register. For details, refer to **26.3.2.1 Association between Data I/O Pins and SS Shift Register**. In this mode, clock polarity, phase, and data settings are performed by bits CPOS and CPHS in the SSMR register. For details, refer to **26.3.1.1 Association between Transfer Clock Polarity, Phase, and Data**.

When this MCU is set as the master device, the chip select line controls output. When synchronous serial communication unit is set as a slave device, the chip select line controls input. When it is set as the master device, the chip select line controls output of the $\overline{\text{SCS}}$ pin or controls output of a general port according to the setting of the CSS1 bit in the SSMR2 register. When the MCU is set as a slave device, the chip select line sets the $\overline{\text{SCS}}$ pin as an input pin by setting bits CSS1 and CSS0 in the SSMR2 register to 01b.

In 4-wire bus communication mode, the MLS bit in the SSMR register is set to 0 and communication is performed MSB-first.

26.5.1 Initialization in 4-Wire Bus Communication Mode

Figure 26.10 shows Initialization in 4-Wire Bus Communication Mode. Before the data transmit/receive operation, set the TE bit in the SSER register to 0 (transmit disabled), the RE bit in the SSER register to 0 (receive disabled), and initialize the synchronous serial communication unit.
To change the communication mode or format, set the TE bit to 0 and the RE bit to 0 before making the change. Setting the RE bit to 0 does not change the settings of flags RDRF and ORER or the contents of the SSRDR register.



Note:
1. Write 0 after reading 1 to set the ORER bit to 0.

Figure 26.10 Initialization in 4-Wire Bus Communication Mode

26.5.2 Data Transmission

Figure 26.11 shows an Example of Synchronous Serial Communication Unit Operation during Data Transmission (4-Wire Bus Communication Mode, 8-Bit SSU Data Transfer Length). During the data transmit operation, synchronous serial communication unit operates as described below. (The data transfer length can be set from 8 to 16 bits using the SSBR register).

When the MCU is set as the master device, it outputs a synchronous clock and data. When the MCU is set as a slave device, it outputs data in synchronization with the input clock while the $\overline{SCS}$ pin is "L".

When the transmit data is written to the SSTDR register after setting the TE bit to 1 (transmit enabled), the TDRE bit is automatically set to 0 (data has not been transferred from registers SSTDR to SSTRSR) and the data is transferred from registers SSTDR to SSTRSR. After the TDRE bit is set to 1 (data is transferred from registers SSTDR to SSTRSR), transmission starts. When the TIE bit in the SSER register is set to 1, a TXI interrupt request is generated.

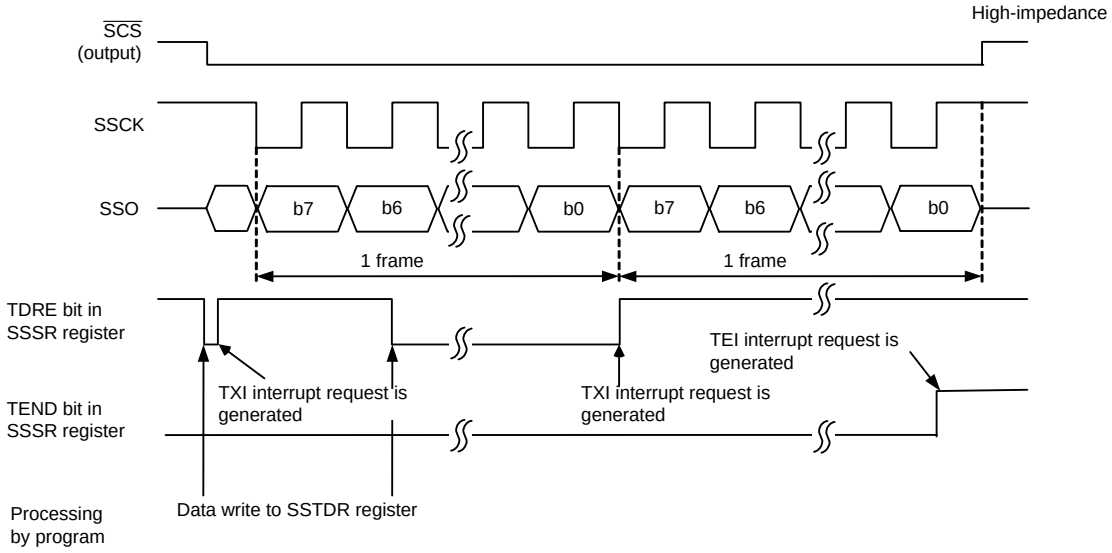
After 1 frame of data is transferred while the TDRE bit is set to 0, the data is transferred from registers SSTDR to SSTRSR and transmission of the next frame is started. If the 8th bit is transmitted while TDRE is set to 1, TEND in the SSSR register is set to 1 (when the last bit of the transmit data is transmitted, the TDRE bit is set to 1) and the state is retained. If the TEIE bit in the SSER register is set to 1 (transmit-end interrupt requests enabled), a TEI interrupt request is generated. The SSCK pin remains "H" after transmit-end and the $\overline{SCS}$ pin is held "H". When transmitting continuously while the $\overline{SCS}$ pin is held "L", write the next transmit data to the SSTDR register before transmitting the 8th bit.

Transmission cannot be performed while the ORER bit in the SSSR register is set to 1 (overrun error). Confirm that the ORER bit is set to 0 before transmission.

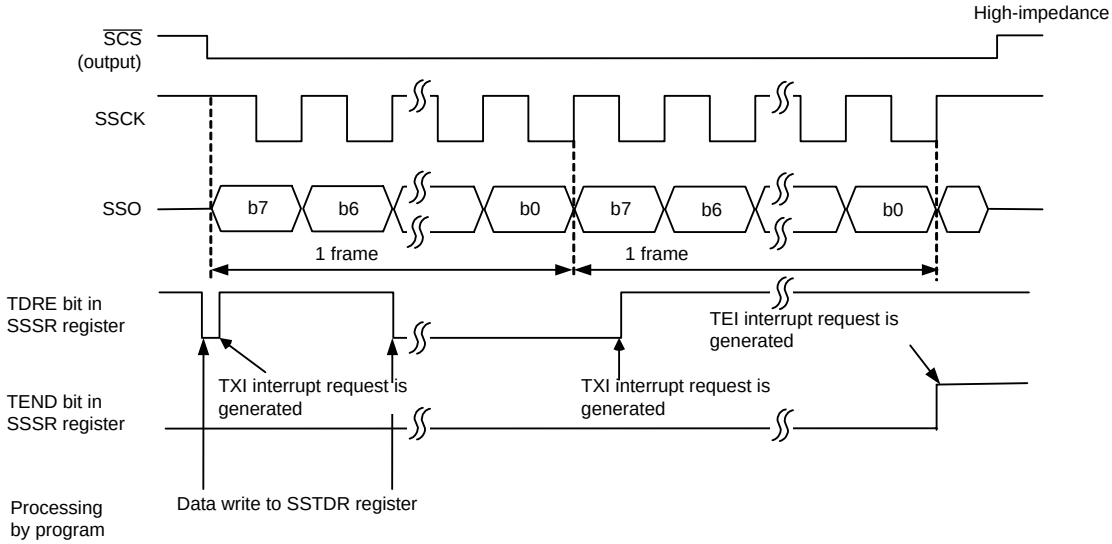
In contrast to the clock synchronous communication mode, the SSO pin is placed in high-impedance state while the $\overline{SCS}$ pin is placed in high-impedance state when operating as a master device and the SSI pin is placed in high-impedance state while the $\overline{SCS}$ pin is placed in "H" input state when operating as a slave device.

The sample flowchart is the same as that for the clock synchronous communication mode (refer to **Figure 26.6 Sample Flowchart of Data Transmission (Clock Synchronous Communication Mode)**).

• CPHS bit = 0 (data change at odd edges), CPOS bit = 0 (“H” when clock stops), and BS3 to BS0 = 1000b (8 bits)



• CPHS bit = 1 (data change at even edges). CPOS bit = 0 (“H” when clock stops), and BS3 to BS0 = 1000b (8 bits)



BS0 to BS3: Bits in SSBR register
CPHS, CPOS: Bits in SSMR register

Figure 26.11 Example of Synchronous Serial Communication Unit Operation during Data Transmission (4-Wire Bus Communication Mode, 8-Bit SSU Data Transfer Length)

26.5.3 Data Reception

Figure 26.12 shows an Example of Synchronous Serial Communication Unit Operation during Data Reception (4-Wire Bus Communication Mode, 8-Bit SSU Data Transfer Length). During data reception, synchronous serial communication unit operates as described below. (The data transfer length can be set from 8 to 16 bits using the SSBR register).

When the MCU is set as the master device, it outputs a synchronous clock and inputs data. When the MCU is set as a slave device, it outputs data synchronized with the input clock while the $\overline{SCS}$ pin receives “L” input. When the MCU is set as the master device, it outputs a receive clock and starts receiving by performing a dummy read of the SSRDR register.

After 8 bits of data are received, the RDRF bit in the SSSR register is set to 1 (data in the SSRDR register) and receive data is stored in the SSRDR register. When the RIE bit in the SSER register is set to 1 (RXI and OEI interrupt requests enabled), an RXI interrupt request is generated. When the SSRDR register is read, the RDRF bit is automatically set to 0 (no data in the SSRDR register).

Read the receive data after setting the RSSTP bit in the SSCRH register to 1 (after receiving 1-byte data, the receive operation is completed). Synchronous serial communication unit outputs a clock for receiving 8 bits of data and stops. After that, set the RE bit in the SSER register to 0 (receive disabled) and the RSSTP bit to 0 (receive operation is continued after receiving 1-byte data) and read the receive data. When the SSRDR register is read while the RE bit is set to 1 (receive enabled), a receive clock is output again.

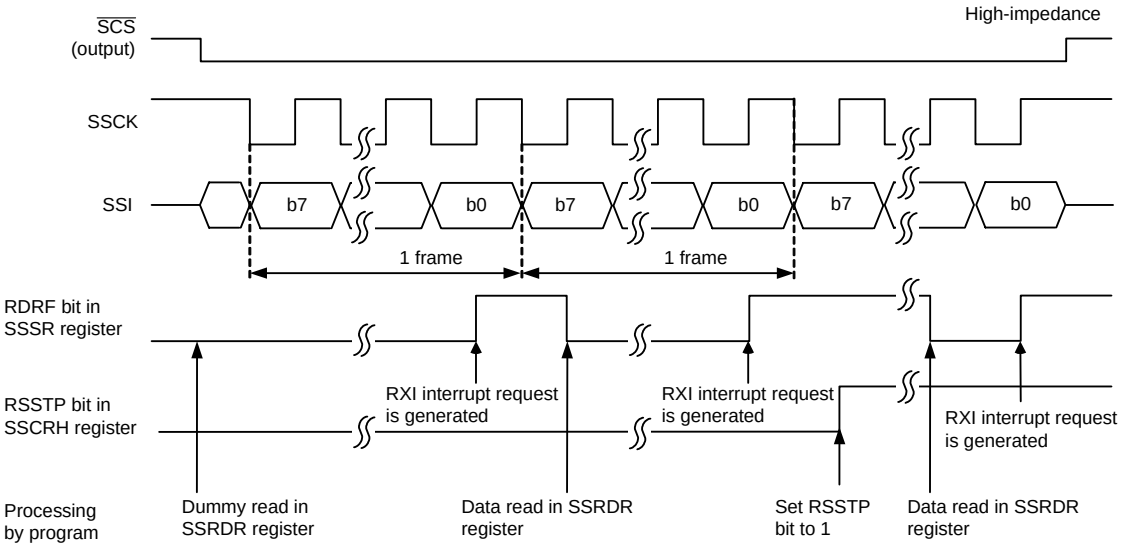
When the 8th clock rises while the RDRF bit is set to 1, the ORER bit in the SSSR register is set to 1 (overrun error: OEI) and the operation is stopped. When the ORER bit is set to 1, reception cannot be performed. Confirm that the ORER bit is set to 0 before restarting reception.

The timing with which bits RDRF and ORER are set to 1 varies depending on the setting of the CPHS bit in the SSMR register. Figure 26.12 shows when bits RDRF and ORER are set to 1.

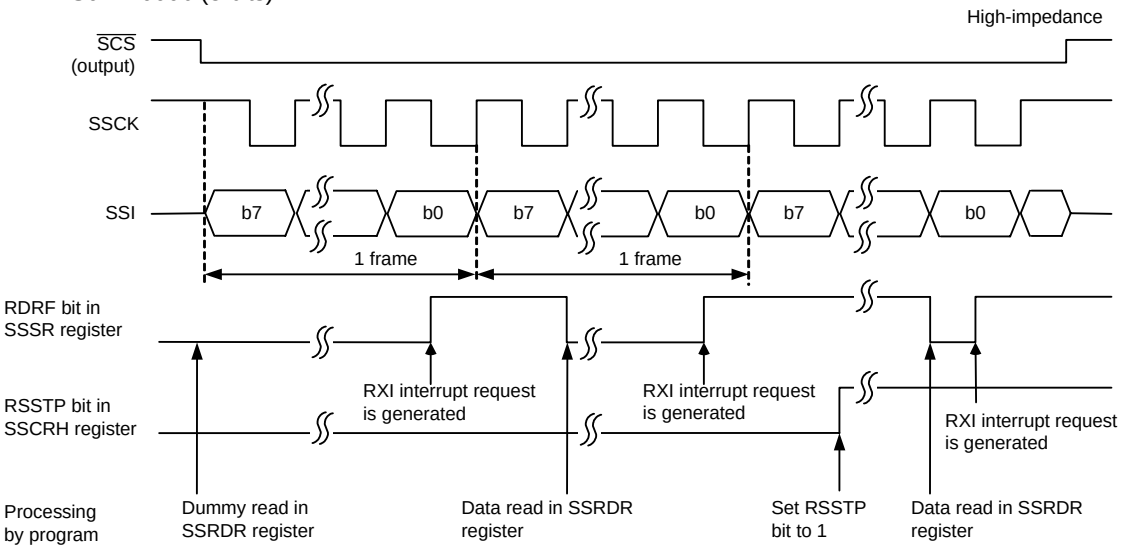
When the CPHS bit is set to 1 (data download at the odd edges), bits RDRF and ORER are set to 1 at some point during the frame.

The sample flowchart is the same as that for the clock synchronous communication mode (refer to **Figure 26.8 Sample Flowchart of Data Reception (MSS = 1) (Clock Synchronous Communication Mode)**).

• CPHS bit = 0 (data download at even edges), CPOS bit = 0 (“H” when clock stops), and BS3 to BS0 = 1000b (8 bits)



• CPHS bit = 1 (data download at odd edges), CPOS bit = 0 (“H” when clock stops), and BS3 to BS0 = 1000b (8 bits)



BS0 to BS3: Bits in SSBR register
CPHS and CPOS: Bit in SSMR register

Figure 26.12 Example of Synchronous Serial Communication Unit Operation during Data Reception (4-Wire Bus Communication Mode, 8-Bit SSU Data Transfer Length)

26.5.4 $\overline{\text{SCS}}$ Pin Control and Arbitration

When setting the SSUMS bit in the SSMR2 register to 1 (4-wire bus communication mode) and the CSS1 bit in the SSMR2 register to 1 (functions as $\overline{\text{SCS}}$ output pin), set the MSS bit in the SSCRH register to 1 (operates as the master device) and check the arbitration of the $\overline{\text{SCS}}$ pin before starting serial transfer. If synchronous serial communication unit detects that the synchronized internal $\overline{\text{SCS}}$ signal is held "L" in this period, the CE bit in the SSSR register is set to 1 (conflict error) and the MSS bit is automatically set to 0 (operates as a slave device).
Figure 26.13 shows the Arbitration Check Timing.

Future transmit operations are not performed while the CE bit is set to 1. Set the CE bit to 0 (no conflict error) before starting transmission.

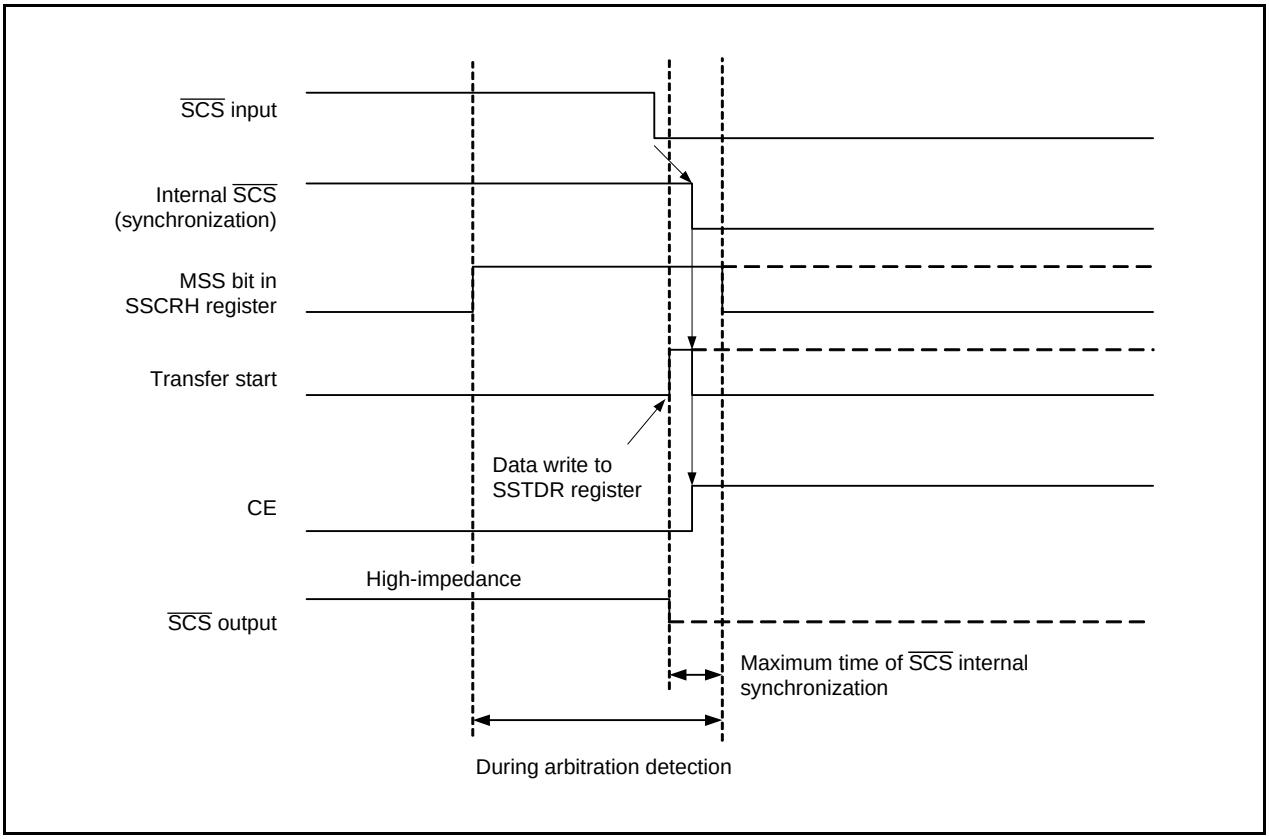


Figure 26.13 Arbitration Check Timing

26.6 Note on Synchronous Serial Communication Unit (SSU)

When using the SSU, a maximum of three cycles are required between writing to the SSTDR register and setting the TEND bit or TDRE bit in the SSSR register to 0. When reading the TEND bit or TDRE bit in the SSSR register immediately after writing to the SSTDR register, insert more than three NOP instructions between the write and read instructions.

27. Hardware LIN

The hardware LIN performs LIN communication in cooperation with timer RAi (i = 0 or 1) and UARTi (i = 0 or 1).

27.1 Overview

The hardware LIN has the features listed below.
Figure 27.1 shows a Hardware LIN Block Diagram.
The wake-up function for each mode is detected using $\overline{\text{INT1}}$.

Master mode
- Synch Break generation
- Bus collision detection

Slave mode
- Synch Break detection
- Synch Field measurement
- Control function for Synch Break and Synch Field signal inputs to UARTi
- Bus collision detection

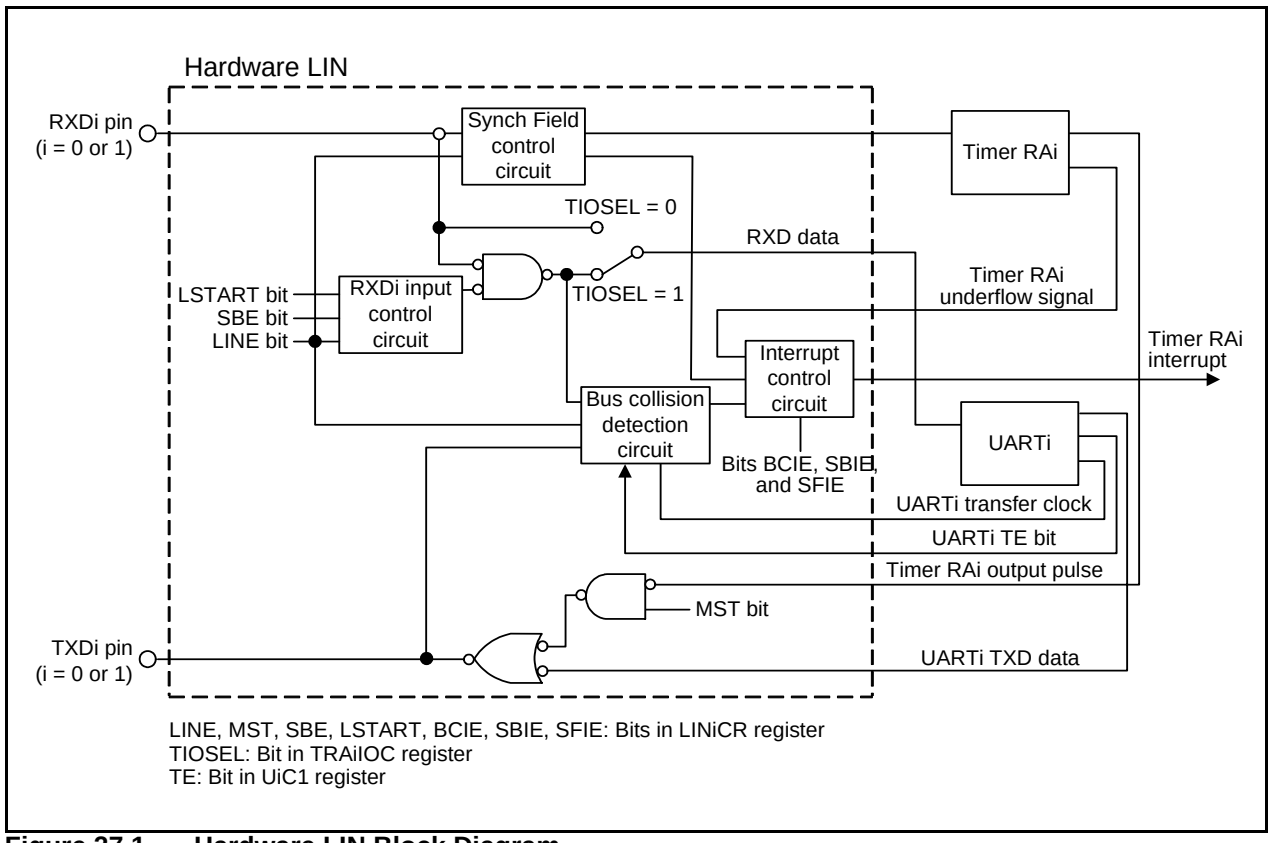


Figure 27.1 Hardware LIN Block Diagram

27.2 Input/Output Pins

The pin configuration for the hardware LIN is listed in Table 27.1.

Table 27.1 Hardware LIN Pin Configuration

Name	Pin Name	Assigned Pin	Input/Output	Function
Receive data input	RXD0	P1_5 (1)	Input	Receive data input pin for the hardware LIN0
Transmit data output	TXD0	P1_4 (2)	Output	Transmit data output pin for the hardware LIN0
Receive data input	RXD1	P6_4 (3)	Input	Receive data input pin for the hardware LIN1
Transmit data output	TXD1	P0_1 or P6_3 (4)	Output	Transmit data output pin for the hardware LIN1

Notes:
1. To use the hardware LIN0, refer to **Table 7.18**.
2. To use the hardware LIN0, set the TXD0SEL0 bit in the U0SR register to 1.
3. To use the hardware LIN1, refer to **Table 7.55**.
4. To use the hardware LIN1, set the bits TXD1SEL1 and TXD1SEL0 in the U1SR register to 01b or 10b.

27.3 Registers

The hardware LIN contains the following registers:

- LINi Control Register 2 (LINiCR2)
- LINi Control Register (LINiCR)
- LINi Status Register (LINiST)

27.3.1 LINi Control Register 2 (LINiCR2) (i = 0 or 1)

Address 0105h (LIN0CR2), 0115h (LIN1CR2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	BCE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	BCE	Bus collision detection during Sync Break transmission enable bit	0: Bus collision detection disabled 1: Bus collision detection enabled	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

27.3.2 LINi Control Register (LINiCR) (i = 0 or 1)

Address 0106h (LIN0CR), 0116h (LIN1CR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	LINE	MST	SBE	LSTART	RXDSF	BCIE	SBIE	SFIE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SFIE	Synch Field measurement-completed interrupt enable bit	0: Synch Field measurement-completed interrupt disabled 1: Synch Field measurement-completed interrupt enabled	R/W
b1	SBIE	Synch Break detection interrupt enable bit	0: Synch Break detection interrupt disabled 1: Synch Break detection interrupt enabled	R/W
b2	BCIE	Bus collision detection interrupt enable bit	0: Bus collision detection interrupt disabled 1: Bus collision detection interrupt enabled	R/W
b3	RXDSF	RXDi input status flag	0: RXDi input enabled 1: RXDi input disabled	R
b4	LSTART	Synch Break detection start bit (1)	When this bit is set to 1, timer RAi input is enabled and RXDi input is disabled. When read, the content is 0.	R/W
b5	SBE	RXDi input unmasking timing select bit (effective only in slave mode)	0: Unmasked after Synch Break detected 1: Unmasked after Synch Field measurement completed	R/W
b6	MST	LIN operation mode setting bit (2)	0: Slave mode (Synch Break detection circuit operation) 1: Master mode (timer RAi output OR'ed with TXDi)	R/W
b7	LINE	LIN operation start bit	0: LIN operation stops 1: LIN operation starts (3)	R/W

Notes:
1. After setting the LSTART bit, confirm that the RXDSF flag is set to 1 before Synch Break input starts.
2. Before switching LIN operation modes, stop the LIN operation (LINE bit = 0) once.
3. Inputs to timer RAi and UARTi are disabled immediately after the LINE bit is set to 1 (LIN operation starts). (Refer to **Figure 27.3 Header Field Transmission Flowchart Example (1)** and **Figure 27.7 Header Field Reception Flowchart Example (2)**.)

27.3.3 LINi Status Register (LINiST) (i = 0 or 1)

Address 0107h (LIN0ST), 0117h (LIN1ST)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	B2CLR	B1CLR	B0CLR	BCDCT	SBDCT	SFDCT
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SFDCT	Synch Field measurement-completed flag	When this bit is set to 1, Synch Field measurement is completed.	R
b1	SBDCT	Synch Break detection flag	when this bit is set to 1, Synch Break is detected or Synch Break generation is completed.	R
b2	BCDCT	Bus collision detection flag	When this bit is set to 1, bus collision is detected.	R
b3	B0CLR	SFDCT bit clear bit	When this bit is set to 1, the SFDCT bit is set to 0. When read, the content is 0.	R/W
b4	B1CLR	SBDCT bit clear bit	When this bit is set to 1, the SBDCT bit is set to 0. When read, the content is 0.	R/W
b5	B2CLR	BCDCT bit clear bit	When this bit is set to 1, the BCDCT bit is set to 0. When read, the content is 0.	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

27.4 Function Description

27.4.1 Master Mode

Figure 27.2 shows an Operating Example during Header Field Transmission in master mode. Figures 27.3 and 27.4 show Examples of Header Field Transmission Flowchart.
During header field transmission, the hardware LIN operates as follows:

(1) When 1 is written to the TSTART bit in the TRAiCR register for timer RAi, a “L” level is output from the TXDi pin for the period set in registers TRAiPRE and TRAi for timer RAi.
(2) When timer RAi underflows, the TXDi pin output is inverted and the SBDCT flag in the LINiST register is set to 1. If the SBIE bit in the LINiCR register is set to 1, a timer RAi interrupt is generated.
(3) The hardware LIN transmits “55h” via UARTi.
(4) After the hardware LIN completes transmitting “55h”, it transmits an ID field via UARTi.
(5) After the hardware LIN completes transmitting the ID field, it performs communication for a response field.

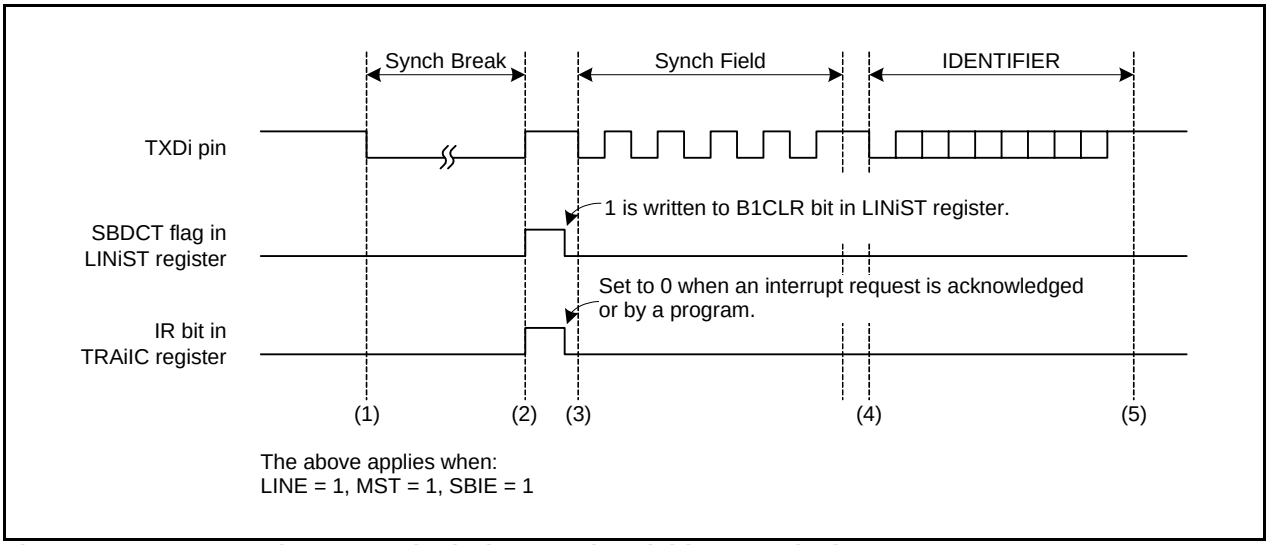
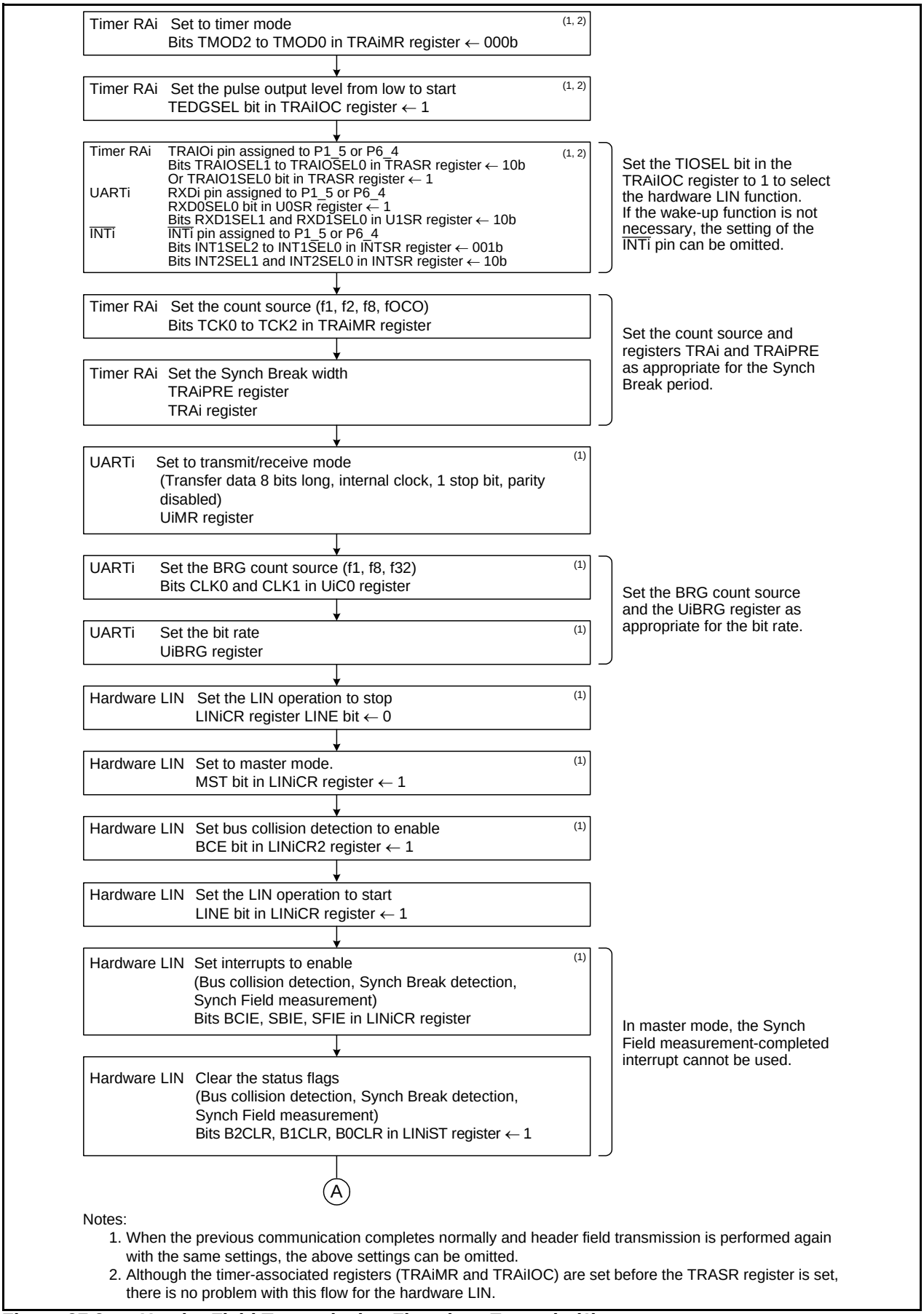


Figure 27.2 Operating Example during Header Field Transmission



Notes:
1. When the previous communication completes normally and header field transmission is performed again with the same settings, the above settings can be omitted.
2. Although the timer-associated registers (TRAiMR and TRAiIOC) are set before the TRASR register is set, there is no problem with this flow for the hardware LIN.

Figure 27.3 Header Field Transmission Flowchart Example (1)

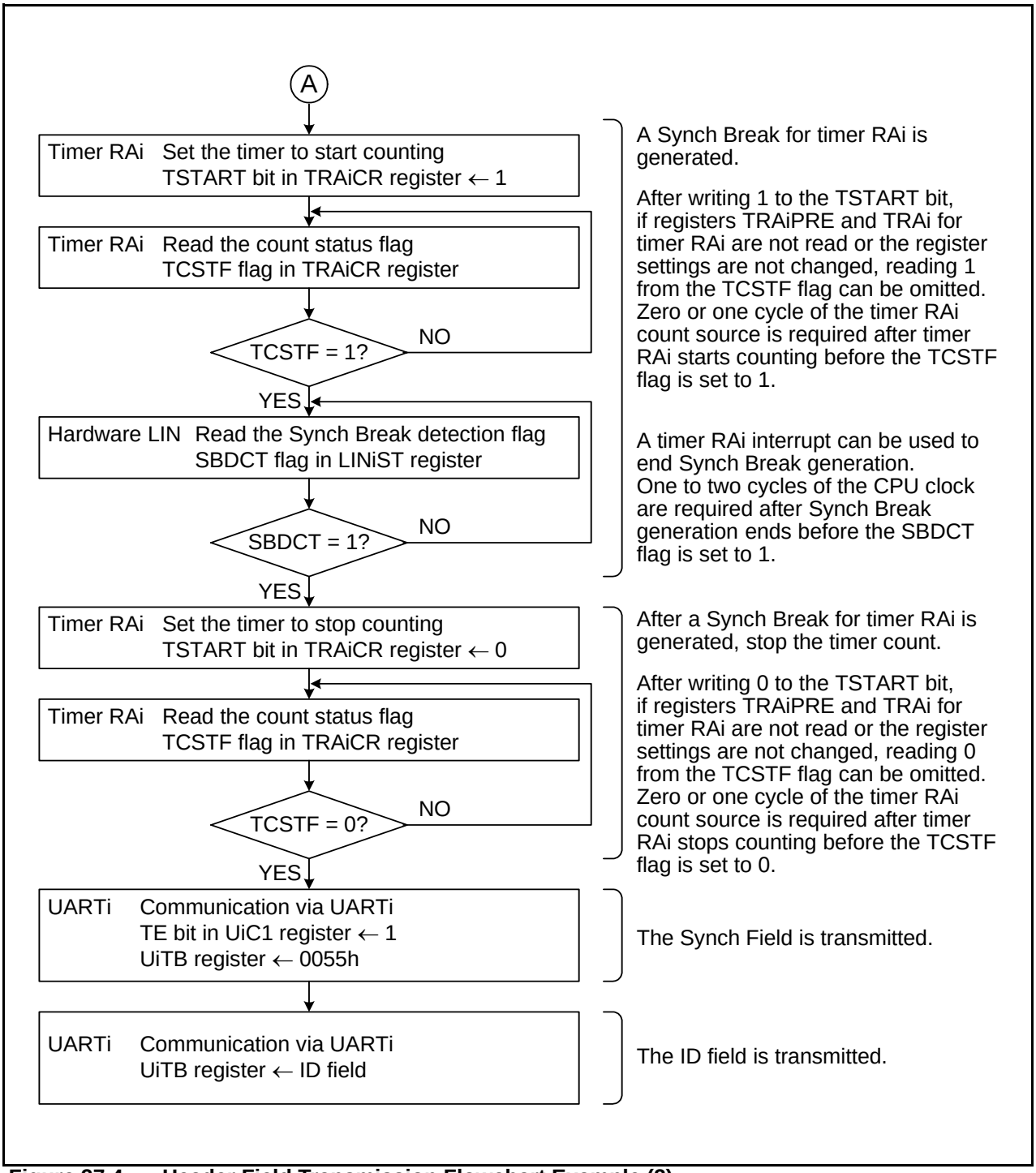


Figure 27.4 Header Field Transmission Flowchart Example (2)

27.4.2 Slave Mode

Figure 27.5 shows an Operating Example during Header Field Reception in slave mode. Figure 27.6 through Figure 27.8 show examples of Header Field Reception Flowchart.
During header field reception, the hardware LIN operates as follows:

(1) When 1 is written to the LSTART bit in the LINiCR register for the hardware LIN, Synch Break detection is enabled.
(2) If a “L” level is input for a duration equal to or longer than the period set in timer RAi, the hardware LIN detected it as a Synch Break. At this time, the SBDCT flag in the LINiST register is set to 1. If the SBIE bit in the LINiCR register is set to 1, a timer RAi interrupt is generated. Then the hardware LIN enters the Synch Field measurement.
(3) The hardware LIN receives a Synch Field (55h) and measures the period of the start bit and bits 0 to 6 is using timer RAi. At this time, whether to input the Synch Field signal to RXDi of UARTi can be selected by the SBE bit in the LINiCR register.
(4) When the Synch Field measurement is completed, the SFDCT flag in the LINiST register is set to 1. If the SFIE bit in the LINiCR register is set to 1, a timer RAi interrupt is generated.
(5) After the Synch Field measurement is completed, a transfer rate is calculated from the timer RAi count value. The rate is set in UARTi and registers TRAiPRE and TRAi for timer RAi are set again. Then the hardware LIN receives an ID field via UARTi.
(6) After the hardware LIN completes receiving the ID field is completed, it performs communication for a response field.

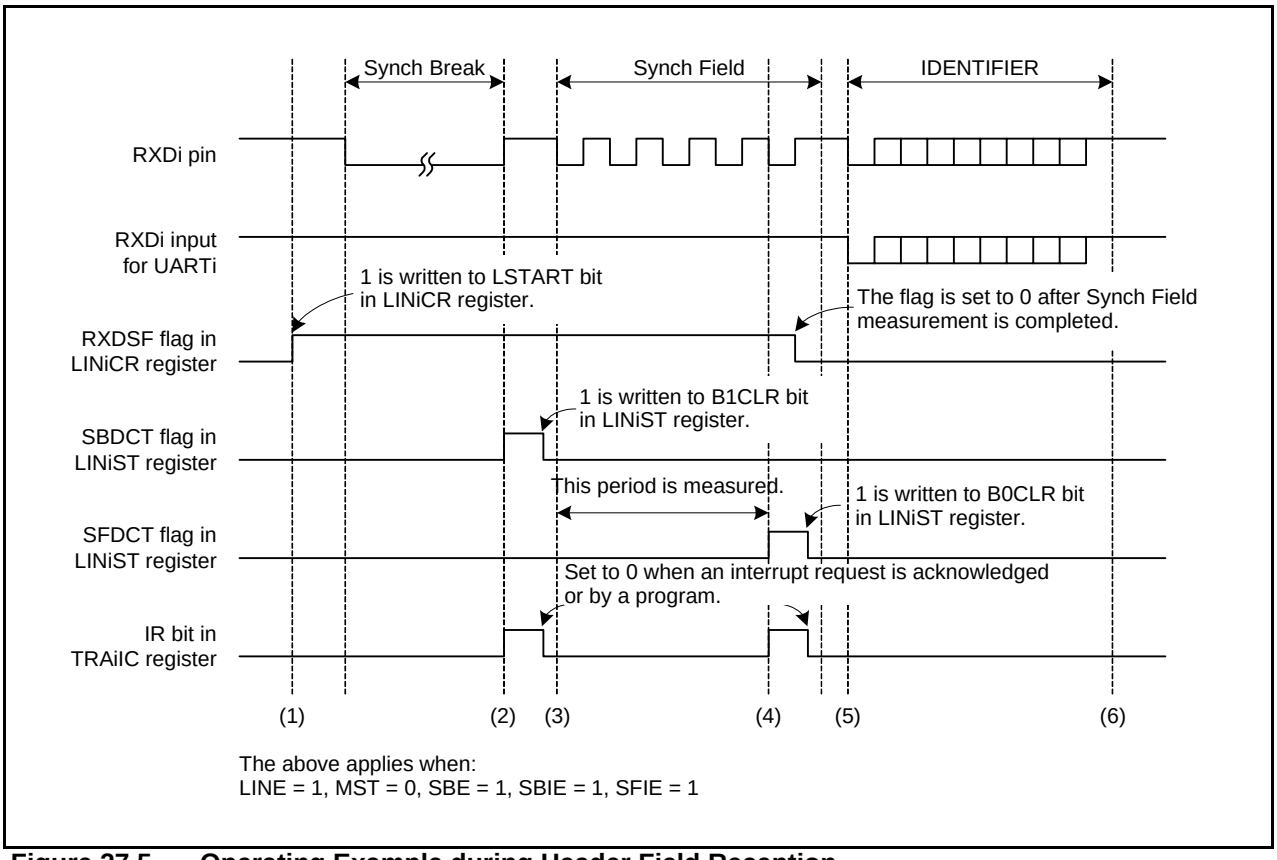
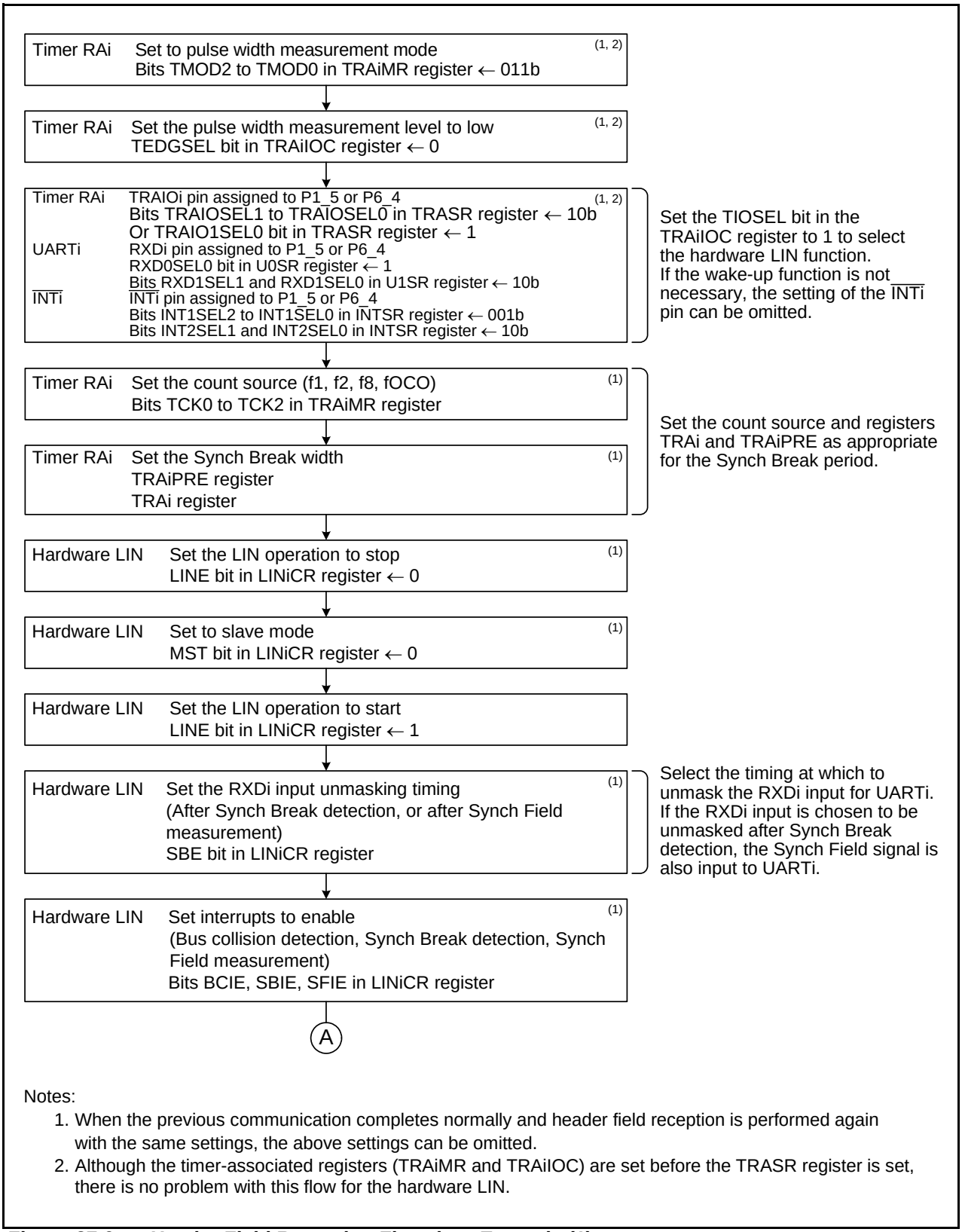


Figure 27.5 Operating Example during Header Field Reception



Notes:
1. When the previous communication completes normally and header field reception is performed again with the same settings, the above settings can be omitted.
2. Although the timer-associated registers (TRAiMR and TRAiIOC) are set before the TRASR register is set, there is no problem with this flow for the hardware LIN.

Figure 27.6 Header Field Reception Flowchart Example (1)

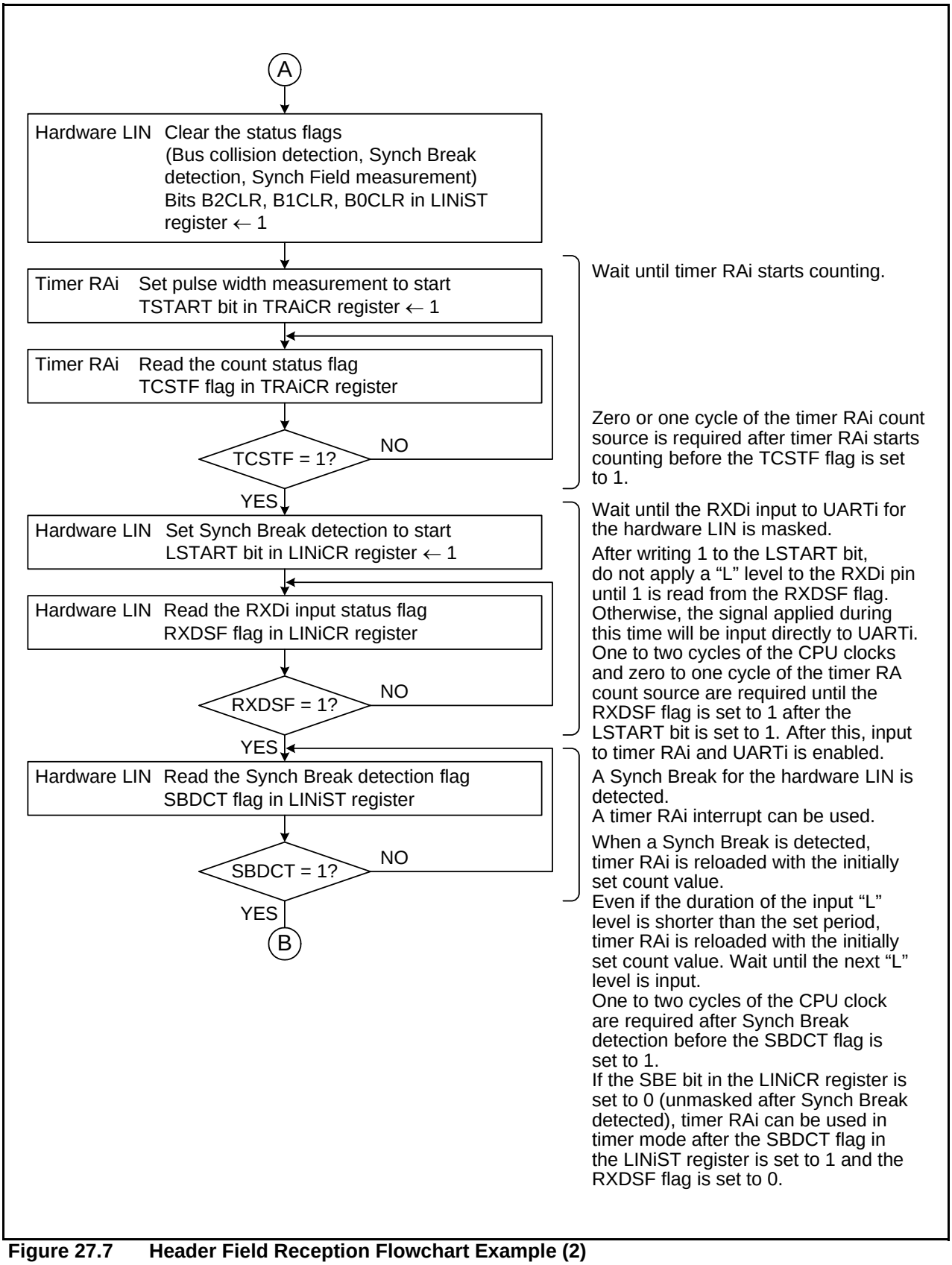


Figure 27.7 Header Field Reception Flowchart Example (2)

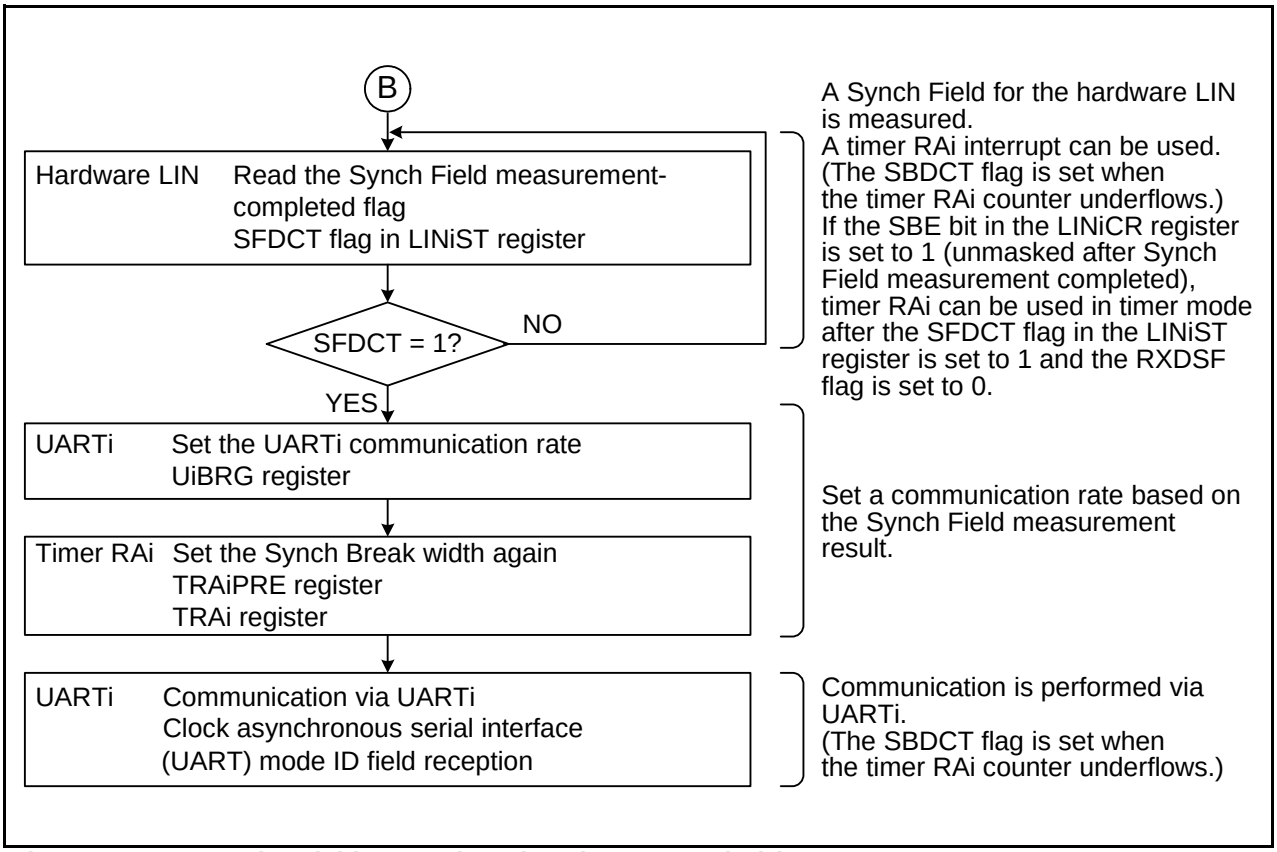


Figure 27.8 Header Field Reception Flowchart Example (3)

27.4.3 Bus Collision Detection Function

The bus collision detection function can be used if UARTi is enabled for transmission (TE bit in UiC1 register = 1). To detect a bus collision during Synch Break transmission, set the BCE bit in the LINiCR2 register to 1 (bus collision detection enabled).
Figure 27.9 shows an Operating Example When Bus Collision is Detected.

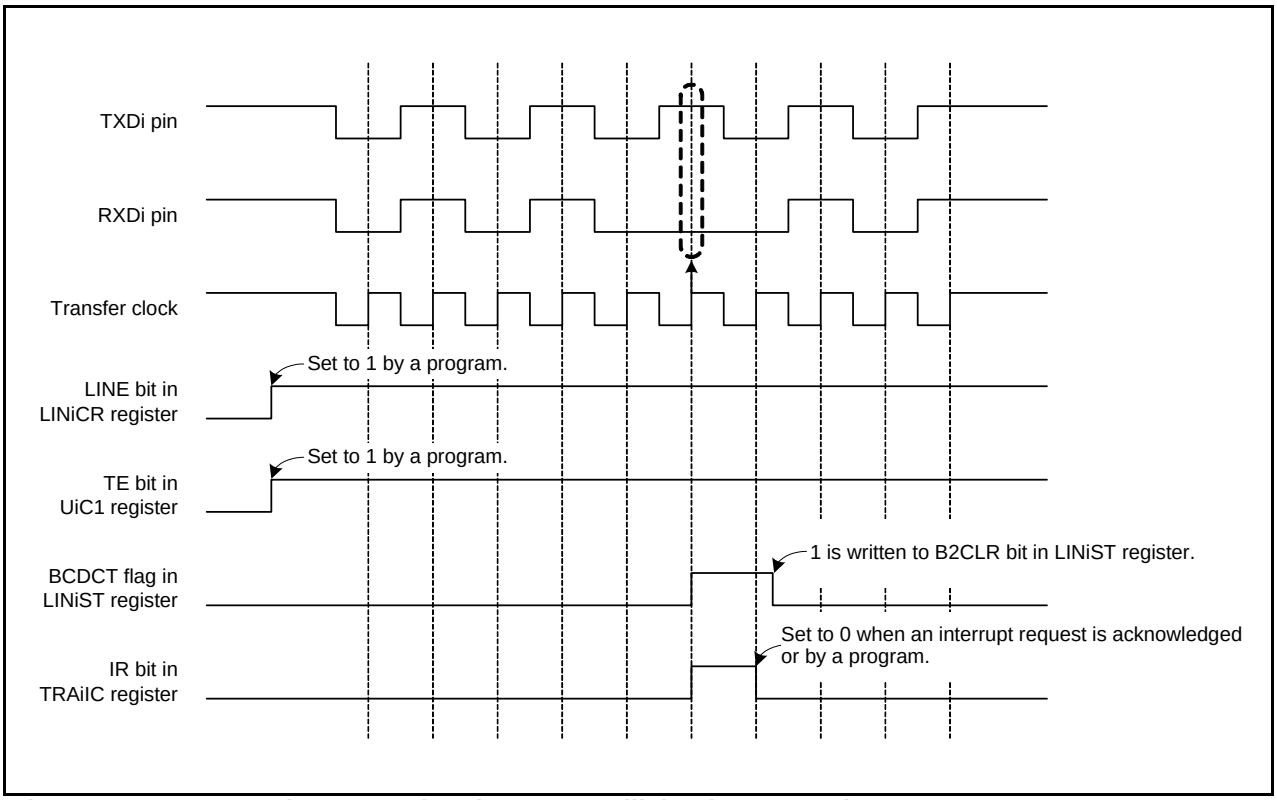


Figure 27.9 Operating Example When Bus Collision is Detected

27.4.4 Hardware LIN End Processing

Figure 27.10 shows an Example of Hardware LIN Communication Completion Flowchart.
Use the following timing for hardware LIN ending processing:

- If the hardware bus collision detection function is used
  Perform hardware LIN ending processing after checksum transmission completes.
- If the bus collision detection function is not used
  Perform hardware LIN end processing after header field transmission and reception complete.

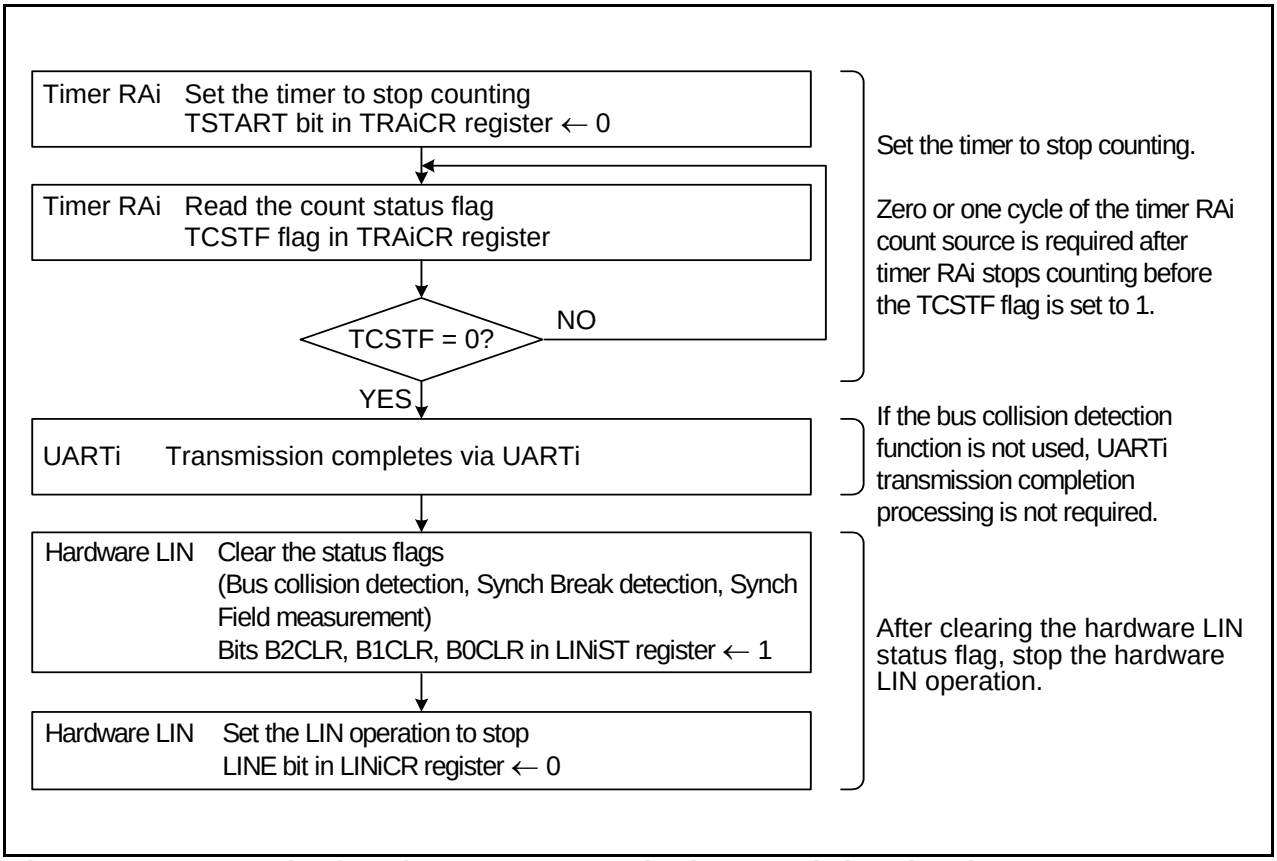


Figure 27.10 Example of Hardware LIN Communication Completion Flowchart

27.5 Interrupt Requests

There are four interrupt requests generated by the hardware LIN: Synch Break detection, Completion of Synch Break generation, Completion of Synch Field measurement, and bus collision detection. These interrupts are shared with timer RAi.
Table 27.2 lists the Hardware LIN Interrupt Requests.

Table 27.2 Hardware LIN Interrupt Requests

Interrupt Request	Status Flag	Interrupt Source
Synch Break detection	SBDCT	Generated when timer RAi underflows after the “L” level duration for the RXDi input is measured, or when a “L” level is input for a duration longer than the Synch Break period during communication.
Completion of Synch Break generation		Generated when a “L” level output to TXDi for the duration set by timer RAi is completed.
Completion of Synch Field measurement	SFDCT	Generated when measurement for 6 bits of the Lynch Field by timer RAi is completed.
Bus collision detection	BCDCT	Generated when the RXDi input and TXDi output values are different at data latch timing while UARTi is enabled for transmission.

27.6 Notes on Hardware LIN

For the time-out processing of the header and response fields, use another timer to measure the duration of time with a Synch Break detection interrupt as the starting point.

28. CAN Module

The R8C/38W Group and R8C/38X Group implement one channel (referred to as CAN0) of CAN (Controller Area Network) module that complies with the ISO11898-1 Specifications.

28.1 Overview

The CAN module transmits and receives both formats of messages, namely the standard identifier (11 bits) (identifier hereafter referred to as ID) and extended ID (29 bits).
Table 28.1 and Table 28.2 list the CAN Module Specifications and Figure 28.1 shows the CAN Module Block Diagram.
Connect the CAN bus transceiver externally.

Table 28.1 CAN Module Specifications (1)

Item	Specifications
Protocol	ISO11898-1 compliant
Bit rate	Up to 1 Mbps
Message boxes	16 mailboxes: Two selectable mailbox modes: • Normal mailbox mode All 16 mailboxes can be configured for transmission or reception. • FIFO mailbox mode: 8 mailboxes can be configured for transmission or reception. The remaining mailboxes can be configured as 4-stage FIFO for transmission and 4-stage FIFO for reception.
Reception	• Data frames and remote frames can be received • Selectable receiving ID format (only standard ID, only extended ID, or both ID) • Programmable one-shot reception function • Selectable overwrite mode (message overwritten) or overrun mode (message discarded) • The reception complete interrupt can be individually enabled or disabled for each mailbox
Acceptance filtering	4 acceptance masks: one mask every 4 mailboxes The mask can be individually enabled or disabled for each mailbox.
Transmission	• Data frame and remote frame can be transmitted • Selectable transmitting ID format (only standard ID, only extended ID, or both ID) • Programmable one-shot transmission function • Selectable ID priority transmit mode or mailbox number priority transmit mode • Transmission request can be aborted (The completion of abort can be confirmed with a flag) • The transmission complete interrupt can be individually enabled or disabled for each mailbox
Mode transition for bus-off recovery	Mode transition for the recovery from the bus-off state can be selected: • ISO11898-1 compliant • Automatic entry to CAN halt mode at bus-off entry • Automatic entry to CAN halt mode at bus-off end • Entry to CAN halt mode by a program • Transition to the error-active state by a program
Error status monitoring	• CAN bus errors (stuff error, form error, ACK error, CRC error, bit error, and ACK delimiter error) can be monitored • Transition to error states can be detected (error-warning, error-passive, bus-off entry, and bus-off recovery) • The error counters can be read.
Time stamp function	Time stamp function using a 16-bit counter The reference clock can be selected from either 1-, 2-, 4- or 8-bit time periods.
Interrupt sources	6 types: • Reception complete • Transmission complete • Receive FIFO • Transmit FIFO • Error • Wake-up
CAN sleep mode	Current consumption can be reduced by stopping the CAN clock.

Table 28.2 CAN Module Specifications (2)

Item	Specifications
Software support units	3 software support units: • Acceptance filter support • Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) • Channel search support
Test mode	3 test modes available for user evaluation: • Listen-only mode • Self-test mode 0 (external loop back) • Self-test mode 1 (internal loop back)

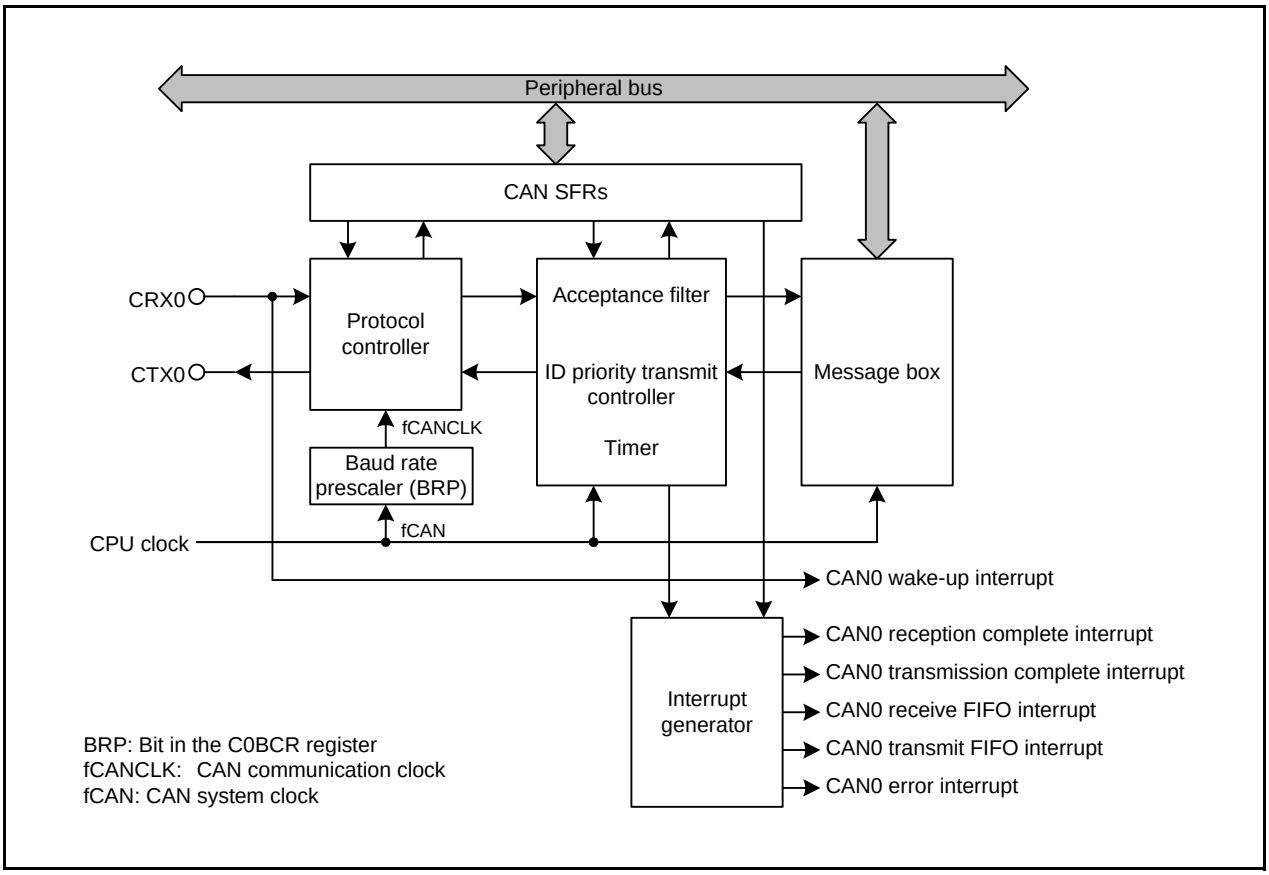


Figure 28.1 CAN Module Block Diagram

- CRX0/CTX0: CAN input/output pins
- Protocol controller: Handles CAN protocol processing such as bus arbitration, bit timing at transmission and reception, stuffing, and error handling, etc.
- Message box: Consists of 16 mailboxes which can be configured as either transmit or receive mailboxes. Each mailbox has an individual ID, data length code, a data field (8 bytes), and a time stamp.
- Acceptance filter: Performs filtering of received messages. Registers C0MKR0 to C0MKR3 are used for the filtering process.
- Timer: Used for the time stamp function. The timer value when storing a message into the mailbox is written as the time stamp value.
- Wake-up function: Generates a CAN0 wake-up interrupt request when a message is detected on the CAN bus.
- Interrupt generation function: Generates the following five types of interrupts:
  - CAN0 reception complete interrupt
  - CAN0 transmission complete interrupt
  - CAN0 receive FIFO interrupt
  - CAN0 transmit FIFO interrupt
  - CAN0 error interrupt
- CAN SFRs: CAN-associated registers. Refer to **28.2 Registers** for details.

28.2 Registers

28.2.1 CAN0 Control Register (C0CTLR)

Address 2F41h to 2F40h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CPE	—	RBOC	BOM		SLPM	CANM	
After Reset	0	0	0	0	0	1	0	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	TSPS		TSRC	TPM	MLM	IDFM		MBM
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b1-b0	CANM	CAN operating mode select bit (1)	b1 b0 0 0: CAN operation mode 0 1: CAN reset mode 1 0: CAN halt mode 1 1: Do not use this combination	R/W
b2	SLPM	CAN sleep mode bit (1, 2)	0: Other than CAN sleep mode 1: CAN sleep mode	R/W
b4-b3	BOM	Bus-off recovery mode bit (3)	b4 b3 0 0: Normal mode (ISO11898-1 compliant) 0 1: Entry to CAN halt mode automatically at bus-off entry 1 0: Entry to CAN halt mode automatically at bus-off end 1 1: Entry to CAN halt mode (during bus-off recovery period) by a program request	R/W
b5	RBOC	Forcible return from bus-off bit (4)	0: Nothing occurred 1: Forcible return from bus-off (5)	R/W
b6	—	Reserved bit	Should be written with 0	R/W
b7	CPE	CPE CAN port enable bit (3, 7)	0: Function as I/O ports 1: Function as CAN I/O	R/W
b8	MBM	CAN mailbox mode select bit (3)	0: Normal mailbox mode 1: FIFO mailbox mode	R/W
b10-b9	IDFM	ID format mode select bit (3)	b10 b9 0 0: Standard ID mode 0 1: Extended ID mode 1 0: Mixed ID mode 1 1: Do not use this combination	R/W
b11	MLM	Message lost mode select bit (3)	0: Overwrite mode 1: Overrun mode	R/W
b12	TPM	Transmit priority mode select bit (3)	0: ID priority transmit mode 1: Mailbox number priority transmit mode	R/W
b13	TSRC	Time stamp counter reset bit (6)	0: Nothing occurred 1: Reset (5)	R/W
b15-b14	TSPS	Time stamp prescaler select bit (3)	b15b14 0 0: Every bit time 0 1: Every 2-bit time 1 0: Every 4-bit time 1 1: Every 8-bit time	R/W

Notes:
1. When bits CANM and SLPM are changed, check the C0STR register to ensure that the mode has been switched. Do not change bits CANM and SLPM until the mode has been switched.
2. Write to the SLPM bit in CAN reset mode or CAN halt mode.
   When rewriting the SLPM bit, set only this bit to 0 or 1.

3. Write to bits BOM, CPE, MBM, IDFM, MLM, TPM, and TSPS in CAN reset mode.
4. Set the RBOC bit to 1 in bus-off state.
5. Bits RBOC and TSRC are automatically set back to 0 after being set to 1. It should be read as 0.
6. Set the TSRC bit to 1 in CAN operation mode.
7. To use a CAN wake-up interrupt, set the CPE bit to 1.

CANM Bit

The CANM bit selects one of the following modes for the CAN module: CAN operation mode, CAN reset mode or CAN halt mode. Refer to **28.3 Operational Mode** for detail.
CAN sleep mode is set by the SLPM bit.
Do not set the CANM bit to 11b.
When the CAN module enters CAN halt mode according to the setting of the BOM bit, the CANM bit is automatically set to 10b.

SLPM Bit

When the SLPM bit is set to 1, the CAN module enters CAN sleep mode.
When this bit is set to 0, the CAN module exits CAN sleep mode.
Refer to **28.3 Operational Mode** for detail.

BOM Bit

The BOM bit is used to select bus-off recovery mode.

When the BOM bit is 00b, the recovery from bus-off is compliant with ISO11898-1, i.e. the CAN module re-enters CAN communication (error-active state) after detecting 11 consecutive recessive bits 128 times. A bus-off recovery interrupt request is generated when recovering from bus-off.

When the BOM bit is 01b, as soon as the CAN module reaches the bus-off state, the CANM bit in the C0CTLR register is set to 10b (CAN halt mode) and the CAN module enters CAN halt mode. No bus-off recovery interrupt request is generated when recovering from bus-off and registers C0TECR and C0RECR are set to 00h.

When the BOM bit is 10b, the CANM bit is set to 10b as soon as the CAN module reaches the bus-off state. The CAN module enters CAN halt mode after the recovery from the bus-off state, i.e. after detecting 11 consecutive recessive bits 128 times. A bus-off recovery interrupt request is generated when recovering from bus-off and registers C0TECR and C0RECR are set to 00h.

When the BOM bit is 11b, the CAN module enters CAN halt mode by setting the CANM bit to 10b while the CAN module is still in bus-off state. No bus-off recovery interrupt request is generated when recovering from bus-off and registers C0TECR and C0RECR are set to 00h. However, if the CAN module recovers from bus-off after detecting 11 consecutive recessive bits 128 times before the CANM bit is set to10b, a bus-off recovery interrupt request is generated.

If the CPU requests an entry to CAN reset mode at the same time as the CAN module attempts to enter CAN halt mode (at bus-off entry when the BOM bit is 01b, or at bus-off end when the BOM bit is 10b), then the CPU request to enter CAN reset mode has higher priority.

RBOC Bit

When the RBOC bit is set to 1 (forcible return from bus-off) in bus-off state, the CAN module forcibly returns from the bus-off state. This bit is automatically set to 0. The error state changes from bus-off to error-active.

When the RBOC bit is set to 1, registers C0RECR and C0TECR are set to 00h and the BOST bit in the C0STR register is set to 0 (the CAN module is not in bus-off state). The other registers remain unchanged. No bus-off recovery interrupt request is generated by this recovery from the bus-off state.
Use the RBOC bit only when the BOM bit is 00b (normal mode).

CPE Bit

When the CPE bit is set to 1, the P62/CRX0 pin and the P61/CTX0 pin function as CAN I/O pins (CRX0 and CTX0), respectively. When the CPE bit is set to 0, the P62/CRX0 pin and the P61/CTX0 pin function as port I/O pins. To use the CAN module, set this bit to 1.

MBM Bit

When the MBM bit is 0 (normal mailbox mode), mailboxes [0] to [15] are configured as transmit or receive mailboxes.
When this bit is 1 (FIFO mailbox mode), mailboxes [0] to [7] are configured as transmit or receive mailboxes. Mailboxes [8] to [11] are configured as a transmit FIFO and mailboxes [8] to [11] as a receive FIFO.
Transmit data is written into mailbox [8] (mailbox [8] is a window mailbox for the transmit FIFO).
Receive data is read from mailbox [12] (mailbox [12] is a window mailbox for the receive FIFO).
Table 28.3 lists the mailbox configuration.

Table 28.3 Mailbox Configuration

Mailbox	MBM bit = 0 (Normal mailbox mode)	MBM bit = 1 (1) (FIFO mailbox mode)
Mailboxes [0] to [7]	Normal mailbox	Normal mailbox
Mailboxes [8] to [11]		Transmit FIFO
Mailboxes [12] to [15]		Receive FIFO

Note:
1. When the MBM bit is set to 1, note the following:
   - Transmit FIFO is controlled by the C0TFCR register.
     The C0MCTLj register (j = 0 to 15) for mailboxes [8] to [11] is disabled.
     Registers C0MCTL8 to C0MCTL11 cannot be used.
   - Receive FIFO is controlled by the C0RFCR register.
     The C0MCTLj register for mailboxes [12] to [15] is disabled.
     Registers C0MCTL12 to C0MCTL15 cannot be used.
   - Refer to the C0MIER register about the FIFO interrupts.
   - The corresponding bits in the C0MKIVLR register for mailboxes [8] to [15] are disabled. Set 0 to these bits.
   - Transmit/receive FIFOs can be used for both data frames and remote frames.

IDFM Bit

The IDFM bit specifies the ID format.
When this bit is 00b, all mailboxes (including FIFO mailboxes) handle only standard IDs.
When this bit is 01b, all mailboxes (including FIFO mailboxes) handle only extended IDs.
When this bit is 10b, all mailboxes (including FIFO mailboxes) handle both standard IDs and extended IDs. Standard IDs or extended IDs are specified by using the IDE bit in the corresponding mailbox in normal mail box mode. In FIFO mailbox mode, the IDE bit in the corresponding mailbox is used for mailboxes [0] to [7], the IDE bit in registers C0FIDCR0 and C0FIDCR1 is used for the receive FIFO, and the IDE bit in mailbox [8] is used for the transmit FIFO.
Do not set 11b to the IDFM bit.

MLM Bit

The MLM bit specifies the operation when a new message is captured in the unread mailbox.
Overwrite mode or overrun mode can be selected. All mailboxes (including the receive FIFO) are set to either overwrite mode or overrun mode.

When the MLM bit is 0, all mailboxes are set to overwrite mode and the new message is overwriting the old message.
When this bit is 1, all mailboxes are set to overrun mode and the new message is discarded.

TPM Bit

The TPM bit specifies the priority of modes when transmitting messages.
ID priority transmit mode or mailbox number transmit mode can be selected.
All mailboxes are set for either ID priority transmission or mailbox number priority transmission.

When the TPM bit is 0, ID priority transmit mode is selected and transmission priority complies with the CAN bus arbitration rule, as defined in the ISO 11898-1 Specifications. In ID priority transmit mode, mailboxes [0] to [15] (in normal mailbox mode), and mailboxes [0] to [7] (in FIFO mailbox mode), and the transmit FIFO are compared for the IDs of mailboxes configured for transmission. If two or more mailbox IDs are the same, the mailbox with the smaller number has higher priority.

Only the next message to be transmitted from the transmit FIFO is included in the transmission arbitration. If a transmit FIFO message is being transmitted, the next pending message within the transmit FIFO is included in the transmission arbitration.

When the TPM bit is 1, mailbox number transmit mode is selected and the transmit mailbox with the smallest mailbox number has the highest priority. In FIFO mailbox mode, the transmit FIFO has lower priority than normal mailboxes (mailboxes [0] to [7]).

TSRC Bit

The TSRC bit is used to reset the time stamp counter.
When this bit is set to 1, the C0TSR register is set to 0000h. It is automatically set to 0.

TSPS Bit

The TSPS bit selects the prescaler for the time stamp.
The reference clock for the time stamp can be selected to be either 1-, 2-, 4- or 8-bit time periods.

28.2.2 CAN0 Bit Configuration Register (C0BCR)

Address 2F46h to 2F44h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BRP							
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	TSEG1				—	—	BRP	
After Reset	0	0	0	0	0	0	0	0

Bit	b23	b22	b21	b20	b19	b18	b17	b16
Symbol	—	—	SJW		—	TSEG2		
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b9-b0	BRP	Prescaler division ratio set bit (10 bits)	If the setting value is P (0 to 1023), the baud rate prescaler divides fCAN by P + 1	R/W
b10	—	Reserved	Set to 0.	R/W
b11	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b15-b12	TSEG1	Time segment 1 control bit	b15b14b13b12 0 0 0 0: Do not use this combination 0 0 0 1: Do not use this combination 0 0 1 0: Do not use this combination 0 0 1 1: 4 Tq 0 1 0 0: 5 Tq 0 1 0 1: 6 Tq 0 1 1 0: 7 Tq 0 1 1 1: 8 Tq 1 0 0 0: 9 Tq 1 0 0 1: 10 Tq 1 0 1 0: 11 Tq 1 0 1 1: 12 Tq 1 1 0 0: 13 Tq 1 1 0 1: 14 Tq 1 1 1 0: 15 Tq 1 1 1 1: 16 Tq	R/W
b18-b16	TSEG2	Time segment 2 control bit	b18b17b16 0 0 0: Do not use this combination 0 0 1: 2 Tq 0 1 0: 3 Tq 0 1 1: 4 Tq 1 0 0: 5 Tq 1 0 1: 6 Tq 1 1 0: 7 Tq 1 1 1: 8 Tq	R/W
b19	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b21-b20	SJW	Resynchronization jump width control bit	b21b20 0 0: 1 Tq 0 1: 2 Tq 1 0: 3 Tq 1 1: 4 Tq	R/W
b23-b22	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Set the C0BCR register before entering CAN halt mode from CAN reset mode, or CAN operation mode from CAN reset mode. After the setting is made once, this register can be written to in CAN reset mode or CAN halt mode.
The C0BCR register consists of 24 bits.
Refer to **28.4 CAN Communication Speed Configuration** about the bit timing configuration.

BRP Bit

The BRP bit is used to set the frequency of the CAN communication clock (fCANCLK).
The cycle of the fCANCLK is set to be 1 Time Quantum (Tq).

TSEG1 Bit

The TSEG1 bit is used to specify the total length of the propagation time segment (PROP_SEG) and phase buffer segment 1 (PHASE_SEG1) with the value of Tq.
A value from 4 to 16 time quanta can be set.

TSEG2 Bit

The TSEG2 bit is used to specify the length of phase buffer segment TSEG2 (PHASE_SEG2) with the value of Tq.
A value from 2 to 8 time quanta can be set.
Set the value smaller than that of the TSEG1 bit.

SJW Bit

The SJW bit is used to specify the resynchronization jump width with the value of Tq.
A value from 1 to 4 time quanta can be set.
Set the value smaller than or equal to that of the TSEG2 bit.

28.2.3 CAN0 Mask Register k (C0MKRk) (k = 0 to 3)

Address 2F13h to 2F10h (C0MKR0), 2F17h to 2F14h (C0MKR1), 2F1Bh to 2F18h (C0MKR2), 2F1Fh to 2F1Ch (C0MKR3)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	EID							
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	EID							
After Reset	X	X	X	X	X	X	X	X

Bit	b23	b22	b21	b20	b19	b18	b17	b16
Symbol	SID						EID	
After Reset	X	X	X	X	X	X	X	X

Bit	b31	b30	b29	b28	b27	b26	b25	b24
Symbol	—	—	—	SID				
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b17-b0	EID	Extended ID bit	0: Corresponding EID bit is not compared 1: Corresponding EID bit is compared	R/W
b28-b18	SID	Standard ID bit	0: Corresponding SID bit is not compared 1: Corresponding SID bit is compared	R/W
b31-b29	—	Reserved bit	Set to 0.	R/W

Write to registers C0MKR0 to C0MKR3 in CAN reset mode or CAN halt mode.
Refer to **28.6 Acceptance Filtering and Masking Function** about the masking function in FIFO mailbox mode.

EID Bit

The EID bit is the filter mask bit corresponding to the CAN extended ID bit. This bit is used to receive extended ID messages.
When the EID bit is 0, the corresponding EID bit is not compared for the received ID and the mailbox ID.
When this bit is 1, the corresponding EID bit is compared for the received ID and the mailbox ID.

SID Bit

The SID bit is the filter mask bit corresponding to the CAN standard ID bit. This bit is used to receive both standard ID and extended ID messages.
When the SID bit is 0, the corresponding SID bit is not compared for the received ID and the mailbox ID.
When this bit is 1, the corresponding SID bit is compared for the received ID and the mailbox ID.

28.2.4 CAN0 FIFO Received ID Compare Register n (C0FIDCR0 and C0FIDCR1) (n= 0, 1)

Address 2F23h to 2F20h (C0FIDCR0), 2F27h to 2F24h (C0FIDCR1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	EID							
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	EID							
After Reset	X	X	X	X	X	X	X	X

Bit	b23	b22	b21	b20	b19	b18	b17	b16
Symbol	SID						EID	
After Reset	X	X	X	X	X	X	X	X

Bit	b31	b30	b29	b28	b27	b26	b25	b24
Symbol	IDE	RTR	—	SID				
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b17-b0	EID	Extended ID bit	0: Corresponding EID bit is 0 1: Corresponding EID bit is 1	R/W
b28-b18	SID	Standard ID bit	0: Corresponding SID bit is 0 1: Corresponding SID bit is 1	R/W
b29	—	Reserved bit	Set to 0.	R/W
b30	RTR	Remote frame request bit	0: Data frame 1: Remote frame	R/W
b31	IDE	ID extension bit (1)	0: Standard ID 1: Extended ID	R/W

Note:
1. The IDE bit is enabled when the IDFM bit in the C0CTLR register is 10b (mixed ID mode). When the IDFM bit is not 10b, the IDE bit should be written with 0.

Write to registers C0FIDCR0 and C0FIDCR1 in CAN reset mode or CAN halt mode.
Registers C0FIDCR0 and C0FIDCR1 are enabled when the MBM bit in the C0CTLR register is set to 1 (FIFO mailbox mode). Bits EID, SID, RTR, and IDE in registers C0MB to C0MB are disabled.
Refer to **28.6 Acceptance Filtering and Masking Function** about the usage of these registers.

EID Bit

The EID bit sets the extended ID of data frames and remote frames. This bit is used to receive extended ID messages.

SID Bit

The SID bit sets the standard ID of data frames and remote frames. This bit is used to receive both standard ID and extended ID messages.

RTR Bit

The RTR bit sets the specified frame format of data frames or remote frames.
This bit specifies the following operation:

- When both RTR bits in registers C0FIDCR0 and C0FIDCR1 are set to 0, only data frames can be received.
- When both RTR bits in registers C0FIDCR0 and C0FIDCR1 are set to 1, only remote frames can be received.
- When the RTR bits in registers C0FIDCR0 and C0FIDCR1 are set to 0 or 1 individually, both data frames and remote frames can be received.

IDE Bit

The IDE bit sets the ID format of standard ID or extended ID.
This bit is enabled when the IDFM bit in the C0CTLR register is 10b (mixed ID mode).
When the IDFM bit is 10b, the IDE bit specifies the following operation:

- When both IDE bits in registers C0FIDCR0 and C0FIDCR1 are set to 0, only standard ID frames can be received.
- When both IDE bits in registers C0FIDCR0 and C0FIDCR1 are set to 1, only extended ID frames can be received.
- When the IDE bits in registers C0FIDCR0 and C0FIDCR1 are set to 0 or 1 individually, both standard ID and extended ID frames can be received.

28.2.5 CAN0 Mask Invalid Register (C0MKIVLR)

Address 2F2Bh to 2F2Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Mode	Bit Name	Function	R/W
b15-b0	Normal mailbox mode	Mask invalid bit	0: Mask valid 1: Mask invalid	R/W
b7-b0	FIFO mailbox mode	Mask invalid bit	0: Mask valid 1: Mask invalid	R/W
b15-b8		Reserved bit	Set to 0.	R/W

Write to the C0MKIVLR register in CAN reset mode or CAN halt mode.
Each bit corresponds to the mailbox with the same number. When each bit is 1, the acceptance mask for the mailbox corresponding to the bit number is disabled. In this case, a receiving message is stored into the mailbox only if its ID matches bits SID and EID in the C0MBj register (j = 0 to 15).

28.2.6 CAN0 Mailbox (C0MBj) (j = 0 to 15)

Table 28.4 lists the CAN0 Mailbox Memory Mapping and Table 28.5 lists the CAN Data Frame Structure. The value after reset of CAN0 mailbox is undefined.

Table 28.4 CAN0 Mailbox Memory Mapping

Address	Message Content
CAN0	Memory Mapping
2E00h + j × 16 + 0	EID7 to EID0
2E00h + j × 16 + 1	EID15 to EID8
2E00h + j × 16 + 2	SID5 to SID0, EID17, EID16
2E00h + j × 16 + 3	IDE, RTR, SID10 to SID6
2E00h + j × 16 + 4	—
2E00h + j × 16 + 5	Data length code (DLC)
2E00h + j × 16 + 6	Data byte 0
2E00h + j × 16 + 6 : : : 2E00h + j × 16 + 13	Data byte 1 : : : Data byte 7
2E00h + j × 16 + 14	Time stamp lower byte
2E00h + j × 16 + 15	Time stamp upper byte

j: Mailbox number (j = 0 to 15)

Table 28.5 CAN Data Frame Structure

SID10 to SID6	SID5 to SID0	EID17 to EID16	EID15 to EID8	EID7 to EID0	DLC3 to DLC0	DATA0	DATA1	.....	DATA7

Address 2E00h to 2EFFh (C0MB0 to C0MB15)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	EID							
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	EID							
After Reset	X	X	X	X	X	X	X	X

Bit	b23	b22	b21	b20	b19	b18	b17	b16
Symbol	SID						EID	
After Reset	X	X	X	X	X	X	X	X

Bit	b31	b30	b29	b28	b27	b26	b25	b24
Symbol	IDE	RTR	—	SID				
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b17-b0	EID	Extended ID (1)	0: Corresponding EID bit is 0 1: Corresponding EID bit is 1	R/W
b28-b18	SID	Standard ID	0: Corresponding SID bit is 0 1: Corresponding SID bit is 1	R/W
b29	—	Reserved bit	Set to 0.	R/W
b30	RTR	Remote frame request bit	0: Data frame 1: Remote frame	R/W
b31	IDE	ID extension bit (2)	0: Standard ID 1: Extended ID	R/W

Address 2E00h to 2EFFh (C0MB0 to C0MB15)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	DLC			
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b7-b0	—	Reserved bit	Set to 0.	R/W
b11-b8	DLC	Data length code (3)	0h to Fh	R/W
b15-b12	—	Reserved bit	Set to 0.	R/W

Address 2E00h to 2EFFh (C0MB0 to C0MB15)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DATA0							
After Reset	X	X	X	X	X	X	X	X
	:							
	:							
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DATA7							
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b7-b0	DATA0 to DATA7	Data Bytes 0 to 7 (3, 4)	00h to FFh	R/W

Address 2E00h to 2EFFh (C0MB0 to C0MB15)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TSL							
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	TSH							
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b7-b0	TSL	Time stamp lower byte	00h to FFh	R/W
b15-b8	TSH	Time stamp higher byte	00h to FFh	R/W

Notes:
1. If the mailbox has received a standard ID message, the EID bit in the mailbox is undefined.
2. The IDE bit is enabled when the IDFM bit in the C0CTLR register is 10b (mixed ID mode).
   When the IDFM bit is not 10b, it should be written with 0.
3. If the mailbox has received a message with n bytes less than 8 bytes, the values of DATAn to DATA7 in the mailbox are undefined.
4. If the mailbox has received a remote frame, the previous values of DATA0 to DATA7 in the mailbox are retained.

Write to the C0MBj register only when the associated C0MCTLj register is 00h and the corresponding mailbox is not processing an abort request.
Refer to **Table 28.4 CAN0 Mailbox Memory Mapping** for detailed addresses.
The previous value of each mailbox is retained unless a new message is received.

EID Bit

The EID bit sets the extended ID of data frames and remote frames. This bit is used to transmit or receive extended ID messages.

SID Bit

The SID bit sets the standard ID of data frames and remote frames. This bit is used to transmit or receive both standard ID and extended ID messages.

RTR Bit

The RTR bit sets the frame format of data frames or remote frames.
This bit specifies the following operation:

- Receive mailbox receives only frames with the format specified by the RTR bit.
- Transmit mailbox transmits according to the frame format specified by the RTR bit.
- Receive FIFO mailbox receives the data frame, remote frame, or both frames specified by the RTR bit in registers C0FIDCR0 and C0FIDCR1.
- Transmit FIFO mailbox transmits the data frame or remote frame specified by the RTR bit in the relevant transmitting message.

IDE Bit

The IDE bit sets the ID format of standard ID or extended ID.
The IDE bit is enabled when the IDFM bit in the C0CTLR register is 10b (mixed ID mode).
When the IDFM bit is 10b, the IDE bit specifies the following operation.

- Receive mailbox receives only ID format specified by the IDE bit.
- Transmit mailbox transmits according to the ID format specified by the IDE bit.
- Receive FIFO mailbox receives messages with the standard ID, extended ID, or both IDs specified by the IDE bit in registers C0FIDCR0 and C0FIDCR1.
- Transmit FIFO mailbox transmits messages with the standard ID or extended ID specified by the IDE bit in the relevant transmitting message.

DLC (Data Length Code)

The DLC is used to set the number of data bytes to be transmitted in a data frame. When data is requested using a remote frame, the number of data bytes to be requested is set.
When a data frame is received, the number of received data bytes is stored. When a remote frame is received, the number of requested data bytes is stored.
Table 28.6 lists the Data Length Corresponding DLC.

Table 28.6 Data Length Corresponding DLC

DLC[3]	DLC[2]	DLC[1]	DLC[0]	Data Length
0	0	0	0	0 byte
0	0	0	1	1 byte
0	0	1	0	2 bytes
0	0	1	1	3 bytes
0	1	0	0	4 bytes
0	1	0	1	5 bytes
0	1	1	0	6 bytes
0	1	1	1	7 bytes
1	-	-	-	8 bytes

-: Any value

DATA0 to DATA7

DATA0 to DATA7 store the transmitted or received CAN message data. Transmission or reception starts from DATA0. The bit order on the CAN bus is MSB first, and transmission or reception starts from bit 7.

TSL and TSH

TSL and TSH store the counter value of the time stamp when received messages are stored in the mailbox.

28.2.7 CAN0 Mailbox Interrupt Enable Register (C0MIER)

Address 2F2Fh to 2F2Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Mode	Bit Name	Function	R/W
b15-b0	Normal mailbox mode	Interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	R/W
b7-b0	FIFO mailbox mode	Interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	R/W
b8		Transmit FIFO interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	R/W
b9		Transmit FIFO interrupt generation timing control bit	Transmit FIFO interrupt request is generated 0: Every time transmission is completed 1: When transmit FIFO becomes empty due to completion of transmission	R/W
b11-b10		Reserved bit	Set to 0.	R/W
b12		Receive FIFO interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	R/W
b13		Receive FIFO interrupt generation timing control bit	Receive FIFO interrupt request is generated 0: Every time reception is completed 1: When receive FIFO becomes buffer warning by completion of reception (1)	R/W
b15-b14		Reserved bit	Set to 0.	R/W

Note:
1. No interrupt request is generated when the receive FIFO becomes buffer warning from full.

Write to the C0MIER register only when the associated C0MCTLj register (j = 0 to 15) is 00h and the corresponding mailbox is not processing transmission or reception abort request.
In FIFO mailbox mode, change the bits in the C0MIER register for the associated FIFO only when:
- The TFE bit in the C0TFCR register is 0 and the TFEST bit is 1, and
- The RFE bit in the C0RFCR register is 0 and the RFEST bit is 1.

Interrupts can enabled individually for each mailbox.
In normal mailbox mode (bits 0 to 15) and in FIFO mailbox mode (bits 0 to 7), each bit corresponds to the mailbox with the same number. These bits enable or disable transmission/reception complete interrupts for the corresponding mailboxes.
In FIFO mailbox mode, bits 8, 9, 12, and 13 specify whether transmit/receive FIFO interrupts are enabled/disabled and timing when interrupt requests are generated.
“Buffer warning” indicates a state in which the third unread message is stored in the receive FIFO.

28.2.8 CAN0 Message Control Register j (C0MCTLj) (j = 0 to 15)

Address 2F30 to 2F3Fh (C0MCTL0 to C0MCTL15)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRMREQ	RECREQ	—	ONESHOT	—	MSGLOST / TRMABT	INVALDATA / TRMACTIVE	NEWDATA / SENTDATA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	NEWDATA	Reception complete flag (1, 2)	(Receiver mailbox setting enabled) 0: No data has been received or 0 is written to the NEWDATA bit 1: A new message is being stored or has been stored to the mailbox	R/W
	SENTDATA	Transmission complete flag (1, 2)	(Transmitter mailbox setting enabled) 0: Transmission is not completed (pending) 1: Transmission is completed (success)	R/W
b1	INVALDATA	Reception-in-progress status flag	(Receiver mailbox setting enabled) 0: Message valid 1: Message being updated	R
	TRMACTIVE	Transmission-in-progress status flag	(Transmitter mailbox setting enabled) 0: Transmission is pending or transmission is not requested 1: From acceptance of transmission request to completion of transmission, or error/arbitration lost	R
b2	MSGLOST	Message lost flag (1, 2)	(Receiver mailbox setting enabled) 0: Message is not overwritten or overrun 1: Message is overwritten or overrun	R/W
	TRMABT	Transmission abort complete flag (1, 2)	(Transmitter mailbox setting enabled) 0: Transmission has started, transmission abort failed because transmission is completed, or transmission abort is not requested 1: Transmission abort is completed	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	ONESHOT	One-shot enable bit (3)	0: One-shot reception or one-shot transmission disabled 1: One-shot reception or one-shot transmission enabled	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	RECREQ	Receive mailbox set bit (2, 4, 5)	0: Not configured for reception 1: Configured for reception	R/W
b7	TRMREQ	Transmit mailbox set bit (2, 4)	0: Not configured for transmission 1: Configured for transmission	R/W

Notes:
1. Write 0 only. Writing 1 has no effect.
2. When writing 0 to bits NEWDATA, SENTDATA, MSGLOST, TRMABT, RECREQ, and TREMREQ by a program, use the MOV instruction to ensure that only the specified bit is set to 0 and the other bits are set to 1.
3. To enter one-shot receive mode, write 1 to the ONESHOT bit at the same time as setting the RECREQ bit to 1. To exit one-shot receive mode, write 0 to the ONESHOT bit after writing 0 to the RECREQ bit and confirming it has been set to 0.
   To enter one-shot transmit mode, write 1 to the ONESHOT bit at the same time as setting the TRMREQ bit to 1. To exit one-shot transmit mode, write 0 to the ONESHOT bit after the message has been transmitted or aborted.
4. Do not set both the RECREQ and TRMREQ bits to 1.
5. When setting the RECREQ bit to 0, set bits MSGLOST, NEWDATA, RECREQ to 0 simultaneously.

Write to the C0MCTLj register in CAN operation mode or CAN halt mode.
Do not use registers C0MCTL8 to 15 in FIFO mailbox mode.

NEWDATA Bit

The NEWDATA bit is set to 1 when a new message is being stored or has been stored to the mailbox.
The timing for setting this bit to 1 is simultaneous with the INVALDATA bit.
The NEWDATA bit is set to 0 by writing 0 by a program.
This bit is not set to 0 by writing 0 by a program while the related INVALDATA bit is 1.

SENTDATA Bit

The SENTDATA bit is set to 1 when data transmission from the corresponding mailbox is completed.
This bit is set to 0 by writing 0 by a program.
To set the SENTDATA bit to 0, first set the TRMREQ bit to 0.
Bits SENTDATA and TRMREQ cannot be set to 0 simultaneously.
To transmit a new message from the corresponding mailbox, set the SENTDATA bit to 0.

INVALDATA Bit

After the completion of a message reception, the INVALDATA bit is set to 1 while the received message is being updated into the corresponding mailbox.
This bit is set to 0 immediately after the message has been stored. If the mailbox is read while this bit is 1, the data is undefined.

TRMACTIVE Bit

The TRMACTIVE bit is set to 1 when the corresponding mailbox of the CAN module begins transmitting a message.
This bit is set to 0 when the CAN module has lost CAN bus arbitration, a CAN bus error occurs, or data transmission is completed.

MSGLOST Bit

The MSGLOST bit is set to 1 when the mailbox is overwritten or overrun by a new received message while the NEWDATA bit is 1. The MSGLOST bit is set to 1 at the end of the 6th bit of EOF.
This bit is set to 0 by writing 0 by a program.
In both overwrite and overrun modes, this bit is not set to 0 by writing 0 by a program during five cycles of fCAN (CAN system clock) following the 6th bit of EOF.

TRMABT Bit

The TRMABT bit is set to 1 in the following cases:

- Following a transmission abort request, when the transmission abort is completed before starting transmission.
- Following a transmission abort request, when the CAN module detects CAN bus arbitration lost or a CAN bus error.
- In one-shot transmission mode (RECREQ bit = 0, TRMREQ bit = 1, and ONESHOT bit = 1), when the CAN module detects CAN bus arbitration lost or a CAN bus error.

The TRMABT bit is not set to 1 when data transmission is completed. In this case, the SENTDATA bit is set to 1.
The TRMABT bit is set to 0 by writing 0 by a program.

ONESHOT Bit

The ONESHOT bit can be used in the following two ways, receive mode and transmit mode:

(1) One-Shot Receive Mode

When the ONESHOT bit is set to 1 in receive mode (RECREQ bit = 1 and TRMREQ bit = 0), the mailbox receives a message only one time. The mailbox does not behave as a receive mailbox after having received a message one time. The behavior of bits NEWDATA and INVALDATA is the same as in normal reception mode. In one-shot receive mode, the MSGLOST bit is not set to 1.

To set the ONESHOT bit to 0, first write 0 to the RECREQ bit and ensure that it has been set to 0.

(2) One-shot Transmission Mode

When the ONESHOT bit is set to 1 in transmit mode (RECREQ bit = 0 and TRMREQ bit = 1), the CAN module transmits a message only one time. The CAN module does not transmit the message again if a CAN bus error or CAN bus arbitration lost occurs. When transmission is completed, the SENTDATA bit is set to 1. If transmission is not completed due to a CAN bus error or CAN bus arbitration lost, the TRMABT bit is set to 1.

Set the ONESHOT bit to 0 after the SENTDATA or TRMABT bit is set to 1.

RECREQ Bit

The RECREQ bit selects receive modes shown in Table 28.11.

When the RECREQ bit is set to 1, the corresponding mailbox is configured for reception of a data frame or a remote frame.

When this bit is set to 0, the corresponding mailbox is not configured for reception of a data frame or a remote frame.

Due to HW protection, the RECREQ bit cannot be set to 0 by writing 0 by a program during the following period

HW protection is started

- from the acceptance filter procedure (the beginning of CRC field)

HW protection is released

- for the mailbox that is specified to receive the incoming message, after the received data is stored into the mailbox or a CAN bus error occurs (i.e. a maximum period of HW protection is from the beginning of the CRC field to the end of the 7th bit of EOF).
- for the other mailboxes, after the acceptance filter procedure.
- if no mailbox is specified to receive the message, after the acceptance filter procedure.

When setting the RECREQ bit to 1, do not set 1 to the TRMREQ bit.

To change the configuration of a mailbox from transmission to reception, first abort the transmission and then set bits SENTDATA and TRMABT to 0 before changing to reception.

TRMREQ Bit

The TRMREQ bit selects transmit modes shown in Table 28.11.

When this bit is set to 1, the corresponding mailbox is configured for transmission of a data frame or a remote frame.

When this bit is set to 0, the corresponding mailbox is not configured for transmission of a data frame or a remote frame.

If the TRMREQ bit is changed from 1 to 0 to cancel the corresponding transmission request, either the TRMABT or SENTDATA bit is set to 1.

When setting the TRMREQ bit to 1, do not set the RECREQ bit to 1.

To change the configuration of a mailbox from reception to transmission, first abort the reception and then set bits NEWDATA and MSGLOST to 0 before changing to transmission.

28.2.9 CAN0 Receive FIFO Control Register (C0RFCR)

Address 2F48h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	RFEST	RFWST	RFFST	RFMLF	RFUST			RFE
After Reset	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	RFE	Receive FIFO enable bit (1)	0: Receive FIFO disabled 1: Receive FIFO enabled	R/W
b3-b1	RFUST	Receive FIFO unread message number status bit	b3 b2 b1 0 0 0: No unread message 0 0 1: 1 unread message 0 1 0: 2 unread messages 0 1 1: 3 unread messages 1 0 0: 4 unread messages 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved	R
b4	RFMLF	Receive FIFO message lost flag (2)	0: No receive FIFO message lost has occurred 1: Receive FIFO message lost has occurred	R/W
b5	RFFST	Receive FIFO full status bit	0: Receive FIFO is not full 1: Receive FIFO is full (4 unread messages)	R
b6	RFWST	Receive FIFO buffer warning status bit	0: Receive FIFO is not buffer warning 1: Receive FIFO is buffer warning (3 unread messages)	R
b7	RFEST	Receive FIFO empty status bit	0: Unread message in receive FIFO 1: No unread message in receive FIFO	R

Notes:
1. Write 0 to the RFE bit simultaneously with the RFMLF bit.
2. Write 0 only. Writing 1 has no effect.

Write to the C0RFCR register in CAN operation mode or CAN halt mode.

RFE Bit

When the RFE bit is set to 1, the receive FIFO is enabled.
When this bit is set to 0, the receive FIFO is disabled for reception and becomes empty (RFEST bit = 1).
Do not set this bit to 1 in normal mailbox mode (MBM bit in the C0CTLR register = 0).
Due to HW protection, the RFE bit is not set to 0 by writing 0 by a program during the following period:
HW protection is started

- from the acceptance filter procedure (the beginning of the CRC field)

HW protection is released

- if the receive FIFO is specified to receive the incoming message, after the received data is stored into the receive FIFO or a CAN bus error occurs. (i.e. a maximum period of HW protection is from the beginning of the CRC field to the end of the 7th bit of EOF.)
- if the receive FIFO is not specified to receive the message, after the acceptance filter procedure.

RFUST Bit

The RFUST bit indicates the number of unread messages in the receive FIFO.
The value of this bit is initialized to 000b when the RFE bit is set to 0.

RFMLF Bit

The RFMLF bit is set to 1 (receive FIFO message lost has occurred) when the receive FIFO receives a new message and the receive FIFO is full. The timing for setting this bit to 1 is at the end of the 6th bit of EOF.
The RFMLF bit is set to 0 by writing 0 by a program.
In both overwrite and overrun modes, this bit cannot be set to 0 (receive FIFO message lost has not occurred) by writing 0 by a program due to HW protection during the five cycles of fCAN following the 6th bit of EOF, if the receive FIFO is full and determined to receive the message.

RFFST Bit

The RFFST bit is set to 1 (receive FIFO is full) when the number of unread messages in the receive FIFO is 4. This bit is set to 0 (receive FIFO is not full) when the number of unread messages in the receive FIFO is less than 4. This bit is set to 0 when the RFE bit is 0.

RFWST Bit

The RFWST bit is set to 1 (receive FIFO is buffer warning) when the number of unread messages in the receive FIFO is 3. This bit is set to 0 (receive FIFO is not buffer warning) when the number of unread messages in the receive FIFO is less than 3 or equal to 4. This bit is set to 0 when the RFE bit is 0.

RFEST Bit

The RFEST bit is 1 (no unread message in receive FIFO) when the number of unread messages in the receive FIFO is 0. This bit is set to 1 when the RFE bit is set to 0. The RFEST bit is set to 0 (unread message in receive FIFO) when the number of unread messages in the receive FIFO is one or more.

Figure 28.2 shows the Receive FIFO Mailbox Operation (Bits 13 and 12 in C0MIER Register = 01b and 11b).

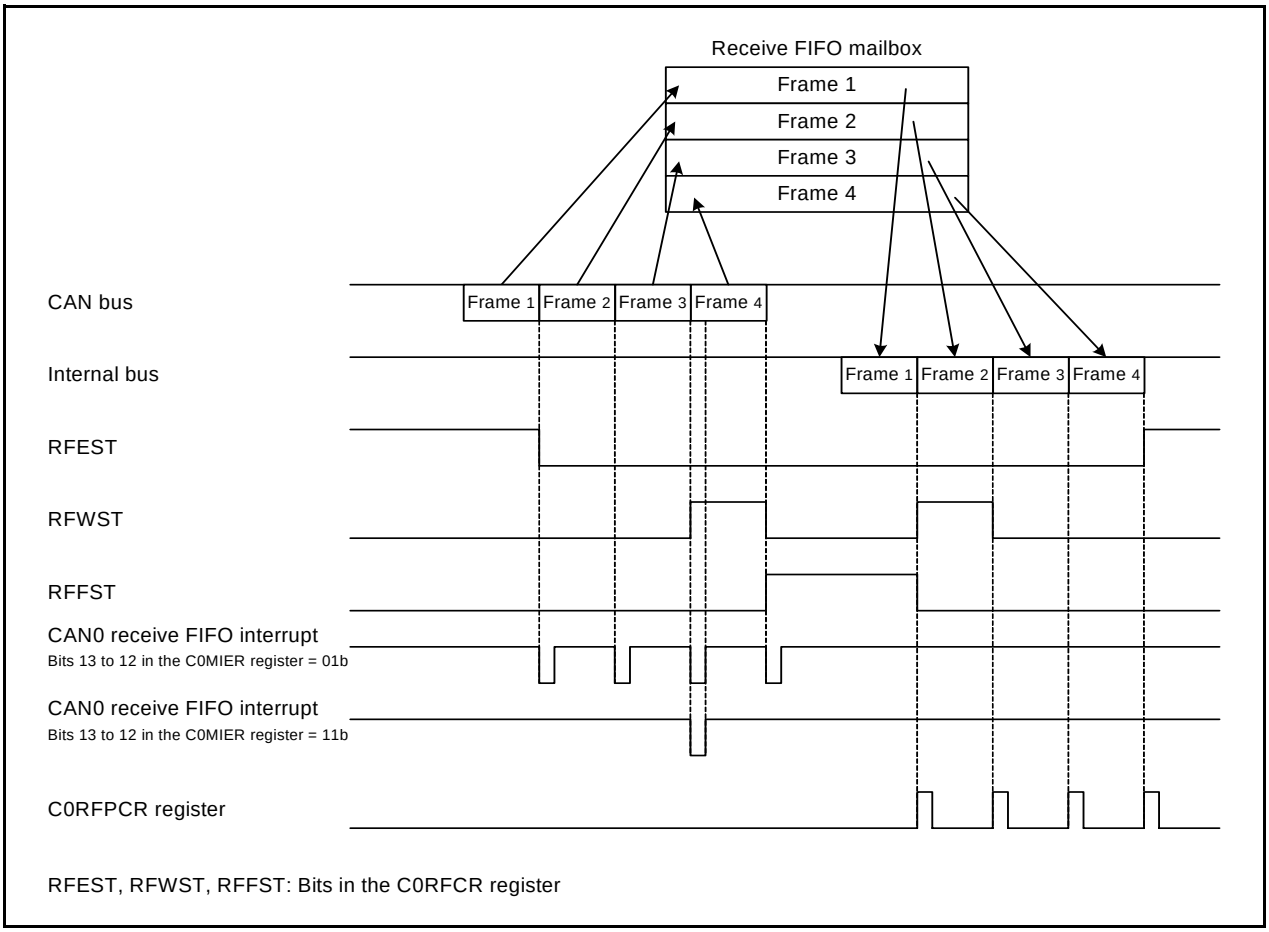


Figure 28.2 Receive FIFO Mailbox Operation (Bits 13 and 12 in C0MIER Register = 01b and 11b)

28.2.10 CAN0 Receive FIFO Pointer Control Register (C0RFPCR)

Address 2F49h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7-b0	The CPU-side pointer for the receive FIFO is incremented by writing FFh	FFh	W

When the receive FIFO is not empty, write FFh to the C0RFPCR register by a program to increment the CPU-side pointer for the receive FIFO to the next mailbox location.
Do not write to the C0RFPCR register when the RFE bit in the C0RFCR register is 0 (receive FIFO disabled).
Both the CAN-side pointer and the CPU-side pointer are incremented when a new message is received and the RFFST bit is 1 (receive FIFO is full) in overwrite mode. When the RFMLF bit is 1 in this condition, the CPU-side pointer cannot be incremented by writing to the C0RFPCR register by a program.

28.2.11 CAN0 Transmit FIFO Control Register (C0TFCR)

Address 2F4Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TFEST	TFFST	—	—	TFUST			TFE
After Reset	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TFE	Transmit FIFO enable bit	0: Transmit FIFO disabled 1: Transmit FIFO enabled	R/W
b3-b1	TFUST	Transmit FIFO unsent message number status bit	b3 b2 b1 0 0 0: No unsent message 0 0 1: 1 unsent message 0 1 0: 2 unsent messages 0 1 1: 3 unsent messages 1 0 0: 4 unsent messages 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved	R
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—	Reserved bit	If necessary, set to 0. When read, the content is undefined.	R
b6	TFFST	Transmit FIFO full status bit	0: Transmit FIFO is not full 1: Transmit FIFO is full (4 unsent messages)	R
b7	TFEST	Transmit FIFO empty status bit	0: Unsent message in transmit FIFO 1: No unsent message in transmit FIFO	R

Write to the C0TFCR register in CAN operation mode or CAN halt mode.

TFE Bit

When the TFE bit is set to 1, the transmit FIFO is enabled.
When this bit is set to 0, the transmit FIFO becomes empty (TFEST bit = 1) and then unsent messages from the transmit FIFO are lost as described below:

- If a message from the transmit FIFO is not scheduled for the next transmission or during transmission.
- Following the completion of transmission, a CAN bus error, CAN bus arbitration lost, or entry to CAN halt mode if a message from the transmit FIFO is scheduled for the next transmission or already during transmission.

Before setting the TFE bit to set to 1 again, ensure that the TFEST bit has been set to 1.
After setting the TFE bit to 1, write transmit data into the C0MB8 register.
Do not set this bit to 1 in normal mailbox mode (MBM bit in the C0CTLR register = 0).

TFUST Bit

The TFUST bit indicates the number of unsent messages in the transmit FIFO.
After the TFE bit is set to 0, the value of the TFUST bit is initialized to 000b (no unsent message) when transmission abort or transmission is completed.

TFFST Bit

The TFFST bit is set to 1 (transmit FIFO is full) when the number of unsent messages in the transmit FIFO is 4. This bit is set to 0 (transmit FIFO is not full) when the number of unsent messages in the transmit FIFO is less than 4. This bit is set to 0 when transmission from the transmit FIFO has been aborted.

TFEST Bit

The TFEST bit is set to 1 (no message in transmit FIFO) when the number of unsent messages in the transmit FIFO is 0. This bit is set to 1 when transmission from the transmit FIFO has been aborted.
The TFEST bit is set to 0 (message in transmit FIFO) when the number of unsent messages in the transmit FIFO is not 0.

Figure 28.3 shows the Transmit FIFO Mailbox Operation (Bits 9 and 8 in C0MIER Register = 01b and 11b).

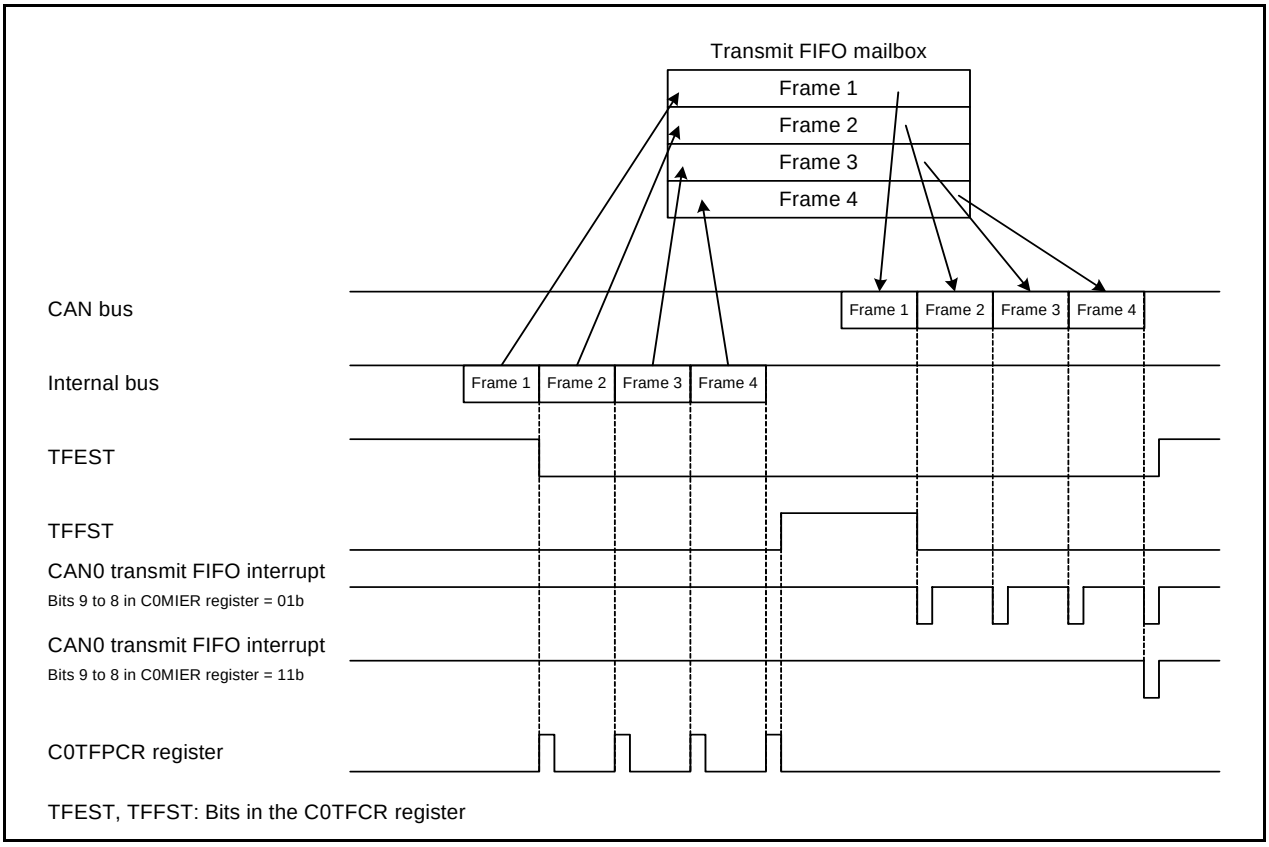


Figure 28.3 Transmit FIFO Mailbox Operation (Bits 9 and 8 in C0MIER Register = 01b and 11b)

28.2.12 CAN0 Transmit FIFO Pointer Control Register (C0TFPCR)

Address 2F4Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7-b0	The CPU-side pointer for the transmit FIFO is incremented by writing FFh	FFh	W

When the transmit FIFO is not full, write FFh to the C0TFPCR register by a program to increment the CPU-side pointer for the transmit FIFO to the next mailbox location.
Do not write to the C0TFPCR register when the TFE bit in the C0TFPCR register is 0 (transmit FIFO disabled).

28.2.13 CAN0 Status Register (C0STR)

Address 2F43h to 2F42h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	RECST	TRMST	BOST	EPST	SLPST	HITST	RSTST
After Reset	0	0	0	0	0	1	0	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	EST	TABST	FMLST	NMLST	TFST	RFST	SDNT	NDST
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	RSTST	CAN reset status flag	0: Not in CAN reset mode 1: In CAN reset mode	R
b1	HITST	CAN halt status flag	0: Not in CAN halt mode 1: In CAN halt mode	R
b2	SLPST	CAN sleep status flag	0: Not in CAN sleep mode 1: In CAN sleep mode	R
b3	EPST	Error-passive status flag	0: Not in error-passive state 1: In error-passive state	R
b4	BOST	Bus-off status flag	0: Not in bus-off state 1: In bus-off state	R
b5	TRMST	Transmit status flag (transmitter)	0: Bus idle or reception in progress 1: Transmission in progress or in bus-off state	R
b6	RECST	Receive status flag (receiver)	0: Bus idle or transmission in progress 1: Reception in progress	R
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b8	NDST	NEWDATA status flag	0: No mailbox with NEWDATA bit = 1 1: Mailbox(es) with NEWDATA bit = 1	R
b9	SDNT	SENTDATA status flag	0: No mailbox with SENTDATA bit = 1 1: Mailbox(es) with SENTDATA bit = 1	R
b10	RFST	Receive FIFO status flag	0: No message in receive FIFO 1: Message in receive FIFO	R
b11	TFST	Transmit FIFO status flag	0: Transmit FIFO is full 1: Transmit FIFO is not full	R
b12	NMLST	Normal mailbox message lost status flag	0: No mailbox with MSGLOST bit = 1 1: Mailbox(es) with MSGLOST bit = 1	R
b13	FMLST	FIFO mailbox message lost status flag	0: RFMLF bit = 0 1: RFMLF bit = 1	R
b14	TABST	Transmission abort status flag	0: No mailbox with TRMABT bit = 1 1: Mailbox(es) with TRMABT bit = 1	R
b15	EST	Error status flag	0: No error occurred 1: Error occurred	R

RSTST Bit

The RSTST bit is set to 1 when the CAN module is in CAN reset mode.
This bit is set to 0 when the CAN module is not in CAN reset mode.
Even when the state is changed from CAN reset mode to CAN sleep mode, the RSTST bit remains 1.

HLTST Bit

The HLTST bit is set to 1 when the CAN module is in CAN halt mode.
This bit is set to 0 when the CAN module is not in CAN halt mode.
Even when the state is changed from CAN halt mode to CAN sleep mode, the HLTST bit remains 1.

SLPST Bit

The SLPST bit is set to 1 when the CAN module is in CAN sleep mode.
This bit is set to 0 when the CAN module is not in CAN sleep mode.

EPST Bit

The EPST bit is set to 1 when the value of the C0TECR or C0RECR register exceeds 127 and the CAN module is in error-passive state (128 ≤ TEC < 256 or 128 ≤ REC < 256). This bit is set to 0 when the CAN module is not in error-passive state.
TEC indicates the value of the transmit error counter (C0TECR register) and REC indicates the value of the receive error counter (C0RECR register).

BOST Bit

The BOST bit is set to 1 when the value of the C0TECR register exceeds 255 and the CAN module is in bus-off state (TEC ≥ 256). This bit is set to 0 when the CAN module is not in bus-off state.

TRMST Bit

The TRMST bit is set to 1 when the CAN module performs as a transmitter node or is in bus-off state.
This bit is set to 0 when the CAN module performs as a receiver node or is in bus-idle state.

RECST Bit

The RECST bit is set to 1 when the CAN module performs as a receiver node.
This bit is set to 0 when the CAN module performs as a transmitter node or is in bus-idle state.

NDST Bit

The NDST bit is set to 1 when at least one NEWDATA bit in the C0MCTLj register (j = 0 to 15) is 1 regardless of the value of the C0MIER register.
The NDST bit is set to 0 when all NEWDATA bits are 0.

SDST Bit

The SDST bit is set to 1 when at least one SENTDATA bit in the C0MCTLj register (j = 0 to 15) is 1 regardless of the value of the C0MIER register.
The SDST bit is set to 0 when all SENTDATA bits are 0.

RFST Bit

The RFST bit is set to 1 when the receive FIFO is not empty.
This bit is set to 0 when the receive FIFO is empty.
This bit is set to 0 when normal mailbox mode is selected.

TFST Bit

The TFST bit is set to 1 when the transmit FIFO is not full.
This bit is set to 0 when the transmit FIFO is full.
This bit is set to 0 when normal mailbox mode is selected.

NMLST Bit

The NMLST bit is set to 1 when at least one MSGLOST bit in the C0MCTLj register is 1 regardless of the value of the C0MIER register.
The NMLST bit is set to 0 when all MSGLOST bits are 0.

FMLST Bit

The FMLST bit is set to 1 when the RFMLF bit in the C0RFCR register is 1 regardless of the value of the C0MIER register.
The FMLST bit is set to 0 when the RFMLF bit is 0.

TABST Bit

The TABST bit is set to 1 when at least one TRMABT bit in the C0MCTLj register is 1 regardless of the value of the C0MIER register.
The TABST bit is set to 0 when all TRMABT bits are 0.

EST Bit

The EST bit is 1 when at least one error is detected by the C0EIFR register regardless of the value of the C0EIER register.
This bit is set to 0 when no error is detected by the C0EIFR register.

28.2.14 CAN0 Mailbox Search Mode Register (C0MSMR)

Address 2F53h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	MBSM	
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b1-b0	MBSM	Mailbox search mode select bit	b1 b0 0 0: Receive mailbox search mode 0 1: Transmit mailbox search mode 1 0: Message lost search mode 1 1: Channel search mode	R/W
b7-b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Write to the C0MSMR register in CAN operation mode or CAN halt mode.

MBSM Bit

The MBSM bit selects the search mode for the mailbox search function.
When this bit is 00b, receive mailbox search mode is selected. In this mode, the search targets are the NEWDATA bit in the C0MCTLj register (j = 0 to 15) for the normal mailbox and the RFESF bit in the C0RFCR register.
When the MBSM bit is 01b, transmit mailbox search mode is selected. In this mode, the search target is the SENTDATA bit in the C0MCTLj register.
When the MBSM bit is 10b, message lost search mode is selected. In this mode, the search targets are the MSGLOST bit in the C0MCTLj register for the normal mailbox and the RFMLF bit in the C0RFCR register.
When the MBSM bit is 11b, channel search mode is selected. In this mode, the search target is the C0CSSR register. Refer to **28.2.16 CAN0 Channel Search Support Register (C0CSSR)**.

28.2.15 CAN0 Mailbox Search Status Register (C0MSSR)

Address 2F52h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SEST	—	—	—	MBNST			
After Reset	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b3-b0	MBNST	Search result mailbox number status bit	Output of search result in each search mode. Output number: 0 to 15	R
b6-b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	SEST	Search result status bit	0: Search result found 1: No search result	R

MBNST Bit

The MBNST bit outputs the smallest mailbox number that is searched in each mode of the C0MSMR register. In receive mailbox, transmit mailbox, and message lost search modes, the value of the mailbox i.e.,the search result to be output, is updated as described below:

- When the NEWDATA, SENTDATA, or MSGLOST bit for the output mailbox is set to 0.
- When the NEWDATA, SENTDATA, or MSGLOST bit for a higher-priority mailbox is set to 1.

In receive mailbox search and message lost search modes, the receive FIFO (mailbox [12]) is output when the receive FIFO is not empty and there are no unread received messages or no lost messages in any of the normal mailboxes (mailboxes [0] to [7]).
In transmit mailbox search mode, the transmit FIFO (mailbox [8]) is not output.
Table 28.7 lists the Behavior of MBNST Bit in FIFO Mailbox Mode.

Table 28.7 Behavior of MBNST Bit in FIFO Mailbox Mode

MBSM bit	Mailbox [8] (Transmit FIFO)	Mailbox [12] (Receive FIFO)
00b	Mailbox [8] is not output.	Mailbox [12] is output when no NEWDATA bit for the normal mailbox is set to 1 and the receive FIFO is not empty.
01b		Mailbox [12] is not output.
10b		Mailbox [12] is output when no MSGLOST bit for the normal mailbox is set to 1 and the RFMLF bit is set to 1 in the receive FIFO.
11b		Mailbox [12] is not output.

In channel search mode, the MBNST bit outputs the corresponding channel number. After the C0MSSR register is read by a program, the next target channel number is output.

SEST Bit

The SEST bit is set to 1 when no corresponding mailbox is found after searching all mailboxes.
For example, in transmit mailbox search mode, the SEST bit is set to 1 when no SENTDATA bit for mailboxes is 1. The SEST bit is set to 0 when at least one SENTDATA bit is 1.
When the SEST bit is 1, the value of the MBNST bit is undefined.

28.2.16 CAN0 Channel Search Support Register (C0CSSR)

Address 2F51h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7-b0	When the value of the channel search is input, the channel number is output to theC0MSSR register	Channel value	R/W

Write to the C0CSSR register only when the MBSM bit in the C0MSMR register is 11b (channel search mode).
Write to the C0CSSR register in CAN operation mode or CAN halt mode.
The bits in the C0CSSR register, which are set to 1, are encoded by an 8/3 encoder (the lower bit position, the higher priority) and output to the MBNST bits in the C0MSSR register.
The C0MSSR register outputs the updated value whenever the C0MSSR register is read by a program.
Figure 28.4 shows the Write and Read of Registers C0CSSR and C0MSSR.

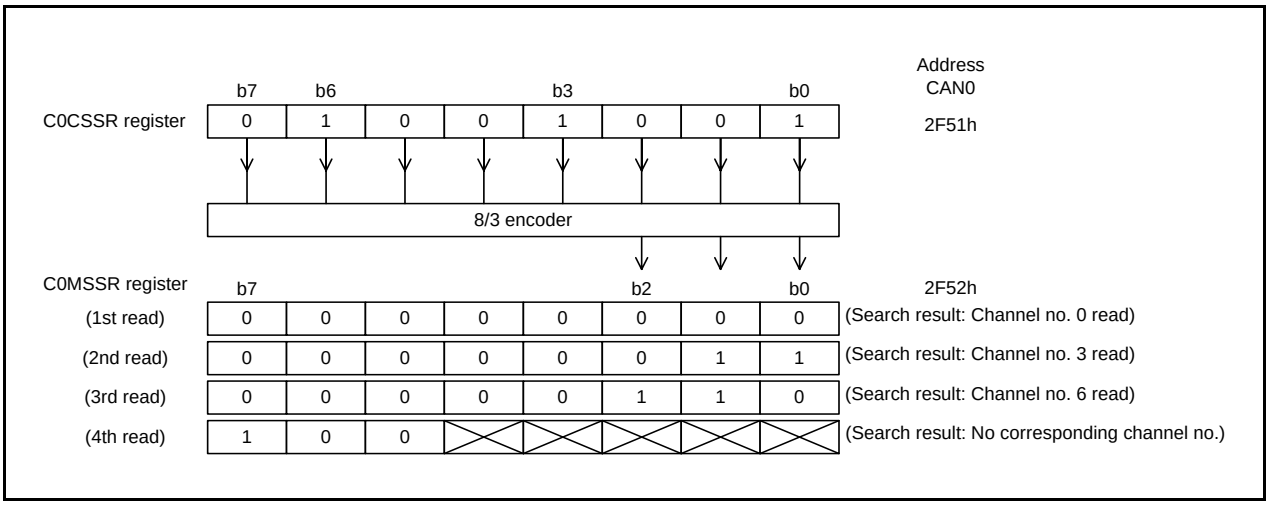


Figure 28.4 Write and Read of Registers C0CSSR and C0MSSR

The value of the C0CSSR register is also updated whenever the C0MSSR register is read. When the C0CSSR register is read, the value before the 8/3 encoder conversion read.

28.2.17 CAN0 Acceptance Filter Support Register (C0AFSR)

Address 2F57h to 2F56h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

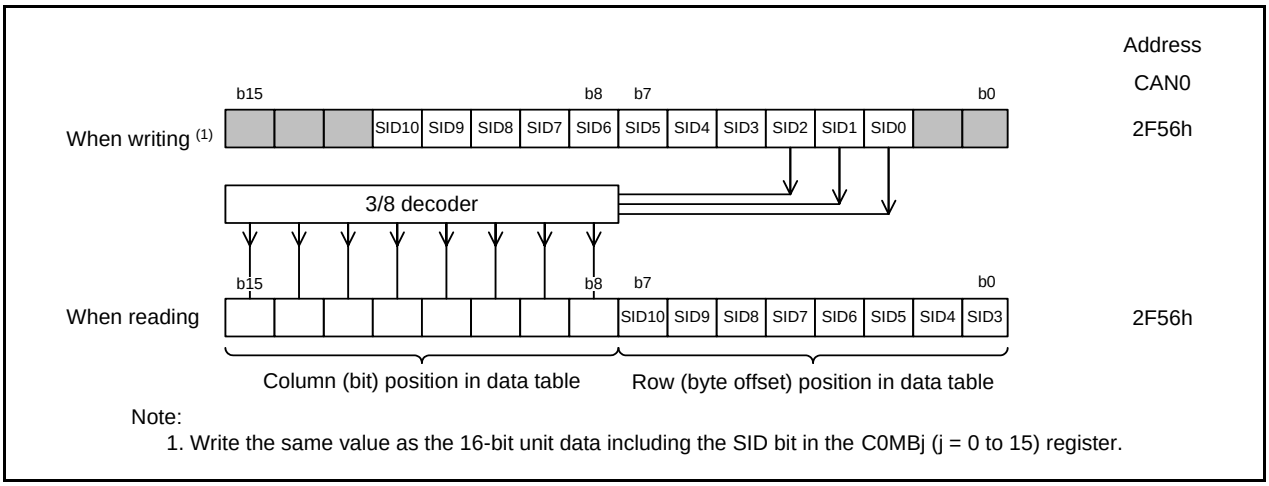
Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b15-b0	After the standard ID of a received message is written, the value converted for data table search can be read	Standard ID/ converted value	R/W

Write to the C0AFSR register in CAN operation mode or CAN halt mode.
The acceptance filter support unit (ASU) can be used for data table (8 bits × 256) search. In the data table, all standard IDs created by the user are set to be valid/invalid in bit units. When the C0AFSR register is written with the 16-bit unit data including the SID bit in the C0MBj register (j = 0 to 15), in which a received ID is stored, a decoded row (byte offset) position and column (bit) position for data table search can be read. The ASU can be used for standard (11-bit) IDs only.
The ASU is enabled in the following cases:

- When the ID to receive cannot be masked by the acceptance filter.
  Example) IDs to receive: 078h, 087h, 111h
- When there are too many IDs to receive and software filtering time is expected to be shortened.

Figure 28.5 shows the Write and Read of C0AFSR Register.



Note:
1. Write the same value as the 16-bit unit data including the SID bit in the C0MBj (j = 0 to 15) register.

Figure 28.5 Write and Read of C0AFSR Register

28.2.18 CAN0 Error Interrupt Enable Register (C0EIER)

Address 2F4Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BLIE	OLIE	ORIE	BORIE	BOEIE	EPIE	EWIE	BEIE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	BEIE	Bus error interrupt enable bit	0: Bus error interrupt disabled 1: Bus error interrupt enabled	R/W
b1	EWIE	Error warning interrupt enable bit	0: Error warning interrupt disabled 1: Error warning interrupt enabled	R/W
b2	EPIE	Error passive interrupt enable bit	0: Error passive interrupt disabled 1: Error passive interrupt enabled	R/W
b3	BOEIE	Bus-off entry interrupt enable bit	0: Bus-off entry interrupt disabled 1: Bus-off entry interrupt enabled	R/W
b4	BORIE	Bus-off recovery interrupt enable bit	0: Bus-off recovery interrupt disabled 1: Bus-off recovery interrupt enabled	R/W
b5	ORIE	Reception overrun interrupt enable bit	0: Receive overrun interrupt disabled 1: Receive overrun interrupt enabled	R/W
b6	OLIE	Overload frame transmit interrupt enable bit	0: Overload frame transmit interrupt disabled 1: Overload frame transmit interrupt enabled	R/W
b7	BLIE	Bus lock interrupt enable bit	0: Bus lock interrupt disabled 1: Bus lock interrupt enabled	R/W

Write to the C0EIER register in CAN reset mode.
The C0EIER register is used to set the error interrupt enabled/disabled individually for each error interrupt source in the C0EIFR register.

BEIE Bit

When the BEIE bit is 0, no error interrupt request is generated even if the BEIF bit in the C0EIFR register is set to 1.
When the BEIE bit is 1, an error interrupt request is generated if the BEIF bit is set to 1.

EWIE Bit

When the EWIE bit is 0, no error interrupt request is generated even if the EWIF bit in the C0EIFR register is set to 1.
When the EWIE bit is 1, an error interrupt request is generated if the EWIF bit is set to 1.

EPIE Bit

When the EPIE bit is 0, no error interrupt request is generated even if the EPIF bit in the C0EIFR register is set to 1.
When the EPIE bit is 1, an error interrupt request is generated if the EPIF bit is set to 1.

BOEIE Bit

When the BOEIE bit is 0, no error interrupt request is generated even if the BOEIF bit in the C0EIFR register is set to 1.
When the BOEIE bit is 1, an error interrupt request is generated if the BOEIF bit is set to 1.

BORIE Bit

When the BORIE bit is 0, an error interrupt request is not generated even if the BORIF bit in the C0EIFR register is set to 1.
When the BORIE bit is 1, an error interrupt request is generated if the BORIF bit is set to 1.

ORIE Bit

When the ORIE bit is 0, no error interrupt request is generated even if the ORIF bit in the C0EIFR register is set to 1.
When the ORIE bit is 1, an error interrupt request is generated if the ORIF bit is set to 1.

OLIE Bit

When the OLIE bit is 0, no error interrupt request is generated even if the OLIF bit in the C0EIFR register is set to 1.
When the OLIE is 1, an error interrupt request is generated if the OLIF bit is set to 1.

BLIE Bit

When the BLIE bit is 0, no error interrupt request is generated even if the BLIF bit in the C0EIFR register is set to 1.
When the BLIE bit is 1, an error interrupt request is generated if the BLIF bit is set to 1.

28.2.19 CAN0 Error Interrupt Factor Judge Register (C0EIFR)

Address 2F4Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BLIF	OLIF	ORIF	BORIF	BOEIF	EPIF	EWIF	BEIF
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	BEIF	Bus error detect flag	0: No bus error detected 1: Bus error detected	R/W
b1	EWIF	Error warning detect flag	0: No error warning detected 1: Error warning detected	R/W
b2	EPIF	Error passive detect flag	0: No error passive detected 1: Error passive detected	R/W
b3	BOEIF	Bus-off entry detect flag	0: No bus-off entry detected 1: Bus-off entry detected	R/W
b4	BORIF	Bus-off recovery detect flag	0: No bus-off recovery detected 1: Bus-off recovery detected	R/W
b5	ORIF	Receive overrun detect flag	0: No receive overrun detected 1: Receive overrun detected	R/W
b6	OLIF	Overload frame transmission detect flag	0: No overload frame transmission detected 1: Overload frame transmission detected	R/W
b7	BLIF	Bus lock detect flag	0: No bus lock detected 1: Bus lock detected	R/W

If an event corresponding to each bit occurs, the corresponding bit in the C0EIFR register is set to 1 regardless of the setting of the C0EIER register.
When writing 0 to these bits by a program, use the MOV instruction to ensure that only the specified bit is set to 0 and the other bits are set to 1. Writing 1 has no effect to these bit values. If the set timing occurs simultaneously with the clear timing by the program, the bit becomes 1.

BEIF Bit

The BEIF bit is set to 1 when a bus error is detected.

EWIF Bit

The EWIF bit is set to 1 when the value of the receive error counter (REC) or transmit error counter (TEC) exceeds 95.
This bit is set to 1 only when the REC or TEC initially exceeds 95. Thus, if 0 is written to the EWIF bit by a program while the REC or TEC remains greater than 95, this bit is not set to 1 until the REC and the TEC go below 95 and then exceeds 95 again.

EPIF Bit

The EPIF bit is set to 1 when the CAN error state becomes error-passive (the REC or TEC value exceeds 127).
This bit is set to 1 only when the REC or TEC initially exceeds 127. Thus, if 0 is written to the EPIF bit by a program while the REC or TEC remains greater than 127, this bit is not set to 1 until the REC and the TEC go below 127 and then exceeds 127 again.

BOEIF Bit

The BOEIF bit is set to 1 when the CAN error state becomes bus-off (the TEC value exceeds 255).
This bit is also set to 1 when the BOM bit in the C0CTLR register is 01b (entry to CAN halt mode automatically at bus-off entry) and the CAN module becomes the bus-off state.

BORIF Bit

The BORIF bit is set to 1 when the CAN module recovers from the bus-off state normally by detecting 11 consecutive bits 128 times in the following conditions:
(1) When the BOM bit in the C0CTLR register is 00b.
(2) When the BOM bit is 10b.
(3) When the BOM bit is 11b.

The BORIF bit is not set to 1 if the CAN module recovers from the bus-off state in the following conditions:
(1) When the CANM bit in the C0CTLR register is set to 01b (CAN reset mode).
(2) When the RBOC bit in the C0CTLR register is set to 1 (forcible return from bus-off).
(3) When the BOM bit is 01b.
(4) When the BOM bit is 11b and the CANM bit is set to 10b (CAN halt mode) before normal recovery occurs.

Table 28.8 lists the Behavior of Bits BOEIF and BORIF according to BOM Bit Setting Value.

Table 28.8 Behavior of Bits BOEIF and BORIF according to BOM Bit Setting Value

BOM bit	BOEIF bit	BORIF bit
00b	Set to 1 on entry to the bus-off state.	Set to 1 on exit from the bus-off state.
01b		Do not set to 1.
10b		Set to 1 on exit from the bus-off state.
11b		Set to 1 if normal bus-off recovery occurs before the CANM bit is set to 10b (CAN halt mode).

ORIF Bit

The ORIF bit is set to 1 when a receive overrun occurs.
This bit is not to set to 1 in overwrite mode. In overwrite mode, a reception complete interrupt request is generated if an overwrite condition occurs and this bit is not set to 1.
In normal mailbox mode, if an overrun occurs in any of mailboxes [0] to [15] in overrun mode, this bit is set to 1.
In FIFO mailbox mode, if an overrun occurs in any of mailboxes [0] to [7] or the receive FIFO in overrun mode, this bit is set to 1.

OLIF Bit

The OLIF bit is set to 1 if the transmitting condition of an overload frame is detected when the CAN module performs transmission or reception.

BLIF Bit

The BLIF bit becomes 1 if 32 consecutive dominant bits are detected on the CAN bus while the CAN module is in CAN operation mode.
After the BLIF bit becomes 1, bus lock can be detected again after either of the following conditions is satisfied:
- After this bit is set to 0 from 1, recessive bits are detected (bus lock is resolved).
- After this bit is set to 0 from 1, the CAN module enters CAN reset mode and then enters CAN operation mode again (internal reset).

28.2.20 CAN0 Receive Error Count Register (C0RECR)

Address 2F4Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b7-b0	Receive error count function The C0RECR register increments or decrements the counter value according to the error status of the CAN module during reception	00h to FFh (1)	R

Note:
1. The value in bus-off state is undefined.

The C0RECR register indicates the value of the receive error counter.
Refer to the CAN Specifications (ISO11898-1) about the increment/decrement conditions of the receive error counter.

28.2.21 CAN0 Transmit Error Count Register (C0TECR)

Address 2F4Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b7-b0	Transmit error count function The C0TECR register increments or decrements the counter value according to the error status of the CAN module during transmission	00h to FFh (1)	R

Note:
1. The value in bus-off state is undefined.

The C0TECR register indicates the value of the TEC error counter.
Refer to the CAN Specifications (ISO11898-1) about the increment/decrement conditions of the transmit error counter.

28.2.22 CAN0 Error Code Store Register (C0ECSR)

Address 2F50h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	EDPM	ADEF	BE0F	BE1F	CEF	AEF	FEF	SEF
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SEF	Stuff error flag (1, 2)	0: No stuff error detected 1: Stuff error detected	R/W
b1	FEF	Form error flag (1, 2)	0: No form error detected 1: Form error detected	R/W
b2	AEF	ACK error flag (1, 2)	0: No ACK error detected 1: ACK error detected	R/W
b3	CEF	CRC error flag (1, 2)	0: No CRC error detected 1: CRC error detected	R/W
b4	BE1F	Bit error (recessive) flag (1, 2)	0: No bit error detected 1: Bit error (recessive) detected	R/W
b5	BE0F	Bit error (dominant) flag (1, 2)	0: No bit error detected 1: Bit error (dominant) detected	R/W
b6	ADEF	ACK delimiter error bit (1, 2)	0: No ACK delimiter error detected 1: ACK delimiter error detected	R/W
b7	EDPM	Error display mode select bit (3, 4)	0: Output of first detected error code 1: Output of accumulated error code	R/W

Notes:
1. Writing 1 has no effect to these bit values.
2. When writing 0 to bits SEF, FEF, AEF, CEF, BE1F, BE0F, and ADEF by a program, use the MOV instruction to ensure that only the specified bit is set to 0 and the other bits are set to 1.
3. Write to the EDPM bit in CAN reset mode or CAN halt mode.
4. If more than one error condition is detected simultaneously, all related bits are set to 1.

The C0ECSR register can be used to monitor whether an error has occurred on the CAN bus. Refer to the CAN Specifications (ISO11898-1) to check the generation conditions of each error.
To set each bit except the EDPM bit to 0, write 0 by a program. If the timing at which each bit is set to 1 and the timing at which is written by a program are the same, the relevant bit is set to 1.

SEF Bit

The SEF bit is set to 1 when a stuff error is detected.

FEF Bit

The FEF bit is set to 1 when a form error is detected.

AEF Bit

The AEF bit is set to 1 when an ACK error is detected.

CEF Bit

The CEF bit is set to 1 when a CRC error is detected.

BE1F Bit

The BE1F bit is set to 1 when a recessive bit error is detected.

BE0F Bit

The BE0F bit is set to 1 when a dominant bit error is detected.

ADEF Bit

The ADEF bit is set to 1 when a form error is detected with the ACK delimiter during transmission.

EDPM Bit

The EDPM bit selects the output mode of the C0ECSR register.
When this bit is set to 0, the C0ECSR register outputs the first error code.
When this bit is set to 1, the C0ECSR register outputs the accumulated error code.

28.2.23 CAN0 Time Stamp Register (C0TSR)

Address 2F55h to 2F54h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15-b0	Free-running counter value for the time stamp function	0000h to FFFFh	R

When the C0TSR register is read, the value of the time stamp counter (16-bit free-running counter) at that moment is read.
The value of the time stamp counter reference clock is a multiple of 1 bit time, as configured by the TSPS bit in the C0CTLR register.
The time stamp counter stops in CAN sleep mode and CAN halt mode, and is initialized in CAN reset mode.
The time stamp counter value is stored to TSL and TSH in the C0MBj register (j = 0 to 15) when a received message is stored in a receive mailbox.

28.2.24 CAN0 Test Control Register (C0TCR)

Address 2F58h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	TSTM		TSTE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTE	CAN test mode enable bit	0: CAN test mode disabled 1: CAN test mode enabled	R/W
b2-b1	TSTM	CAN test mode select bit	b2 b1 0 0: Other than CAN test mode 0 1: Listen-only mode 1 0: Self-test mode 0 (external loop back) 1 1: Self-test mode 1 (internal loop back)	R/W
b7-b3	—	Reserved	Set to 0.	R/W

Write to the C0TCR register only in CAN halt mode.

TSTE Bit

When the TSTE bit is set to 0, CAN test mode is disabled.
When this bit is set to 1, CAN test mode is enabled.

TSTM Bit

The TSTM bit selects the CAN test mode.
The details of each CAN test mode is described below.

28.2.24.1 Listen-only Mode

The ISO 11898-1 recommends an optional bus monitoring mode. In listen-only mode, the CAN node is able to receive valid data frames and valid remote frames. It sends only recessive bits on the CAN bus, and the protocol controller is not required to send the ACK bit, overload flag, or active error flag.
Listen-only mode can be used for baud rate detection.
Do not request transmission from any mailboxes in this mode.
Figure 28.6 shows the Connection when Listen-Only Mode is Selected.

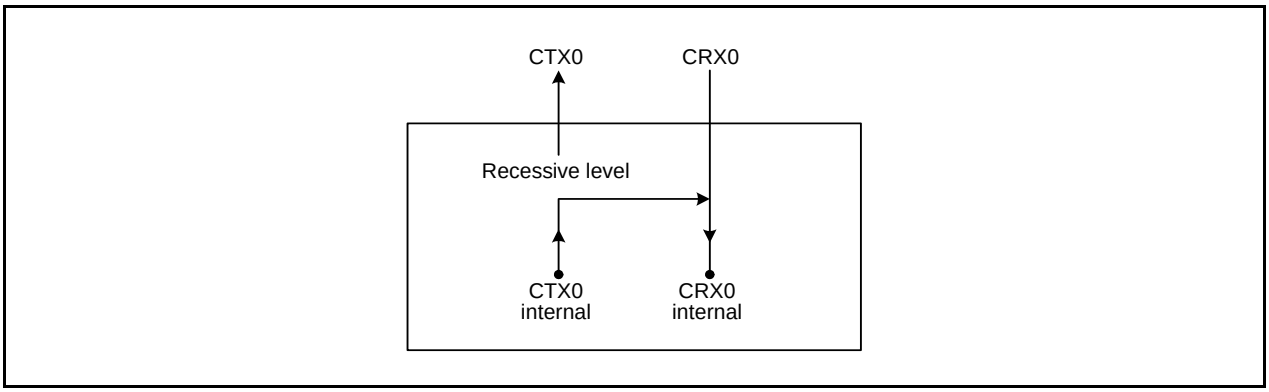


Figure 28.6 Connection when Listen-Only Mode is Selected

28.2.24.2 Self-Test Mode 0 (External Loop Back)

Self-test mode 0 is provided for CAN transceiver tests.
In this mode, the protocol controller treats its own transmitted messages as messages received via the CAN transceiver and stores them into the receive mailbox. To be independent from external stimulation, the protocol controller generates the ACK bit.
Connect the CTX0/CRX0 pins to the transceiver.
Figure 28.7 shows the Connection when Self-Test Mode 0 is Selected.

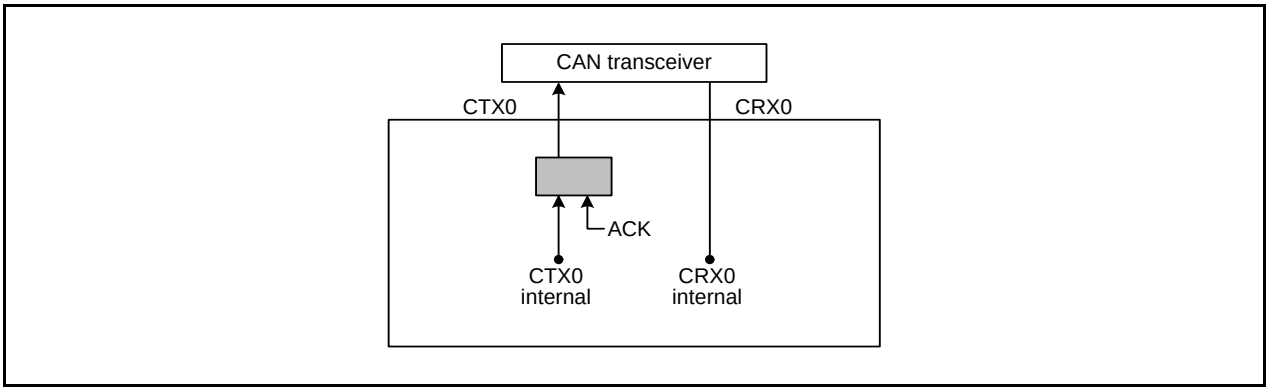


Figure 28.7 Connection when Self-Test Mode 0 is Selected

28.2.24.3 Self-Test Mode 1 (Internal Loop Back)

Self-test mode 1 is provided for self-test functions.
In this mode, the protocol controller treats its transmitted messages as received messages and stores them into the receive mailbox. To be independent from external stimulation, the protocol controller generates the ACK bit.
In self-test mode 1, the protocol controller performs an internal feedback from the internal CTX0 pin to the internal CRX0 pin. The input value of the external CRX0 pin is ignored. The external CTX0 pin outputs only recessive bits. The CTX0/CRX0 pins do not need to be connected to the CAN bus or any external device.
Figure 28.8 shows the Connection when Self-Test Mode 1 is Selected.

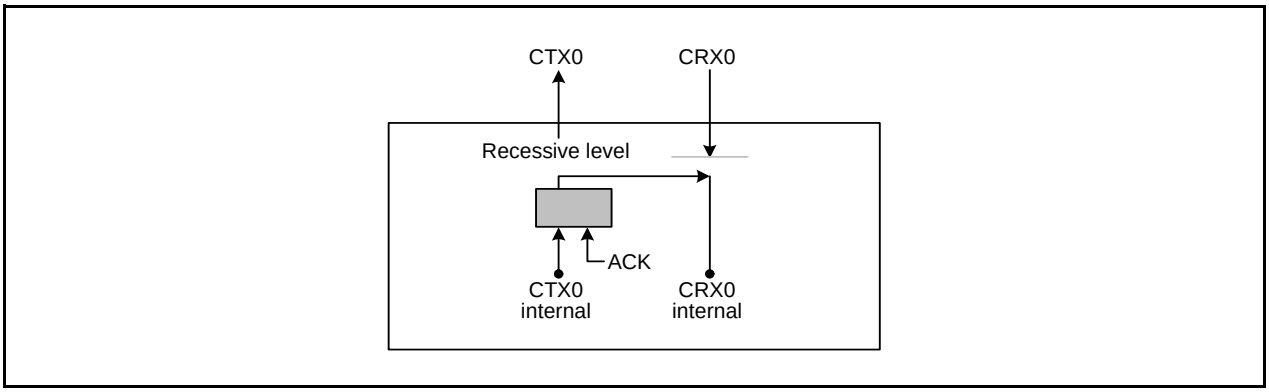


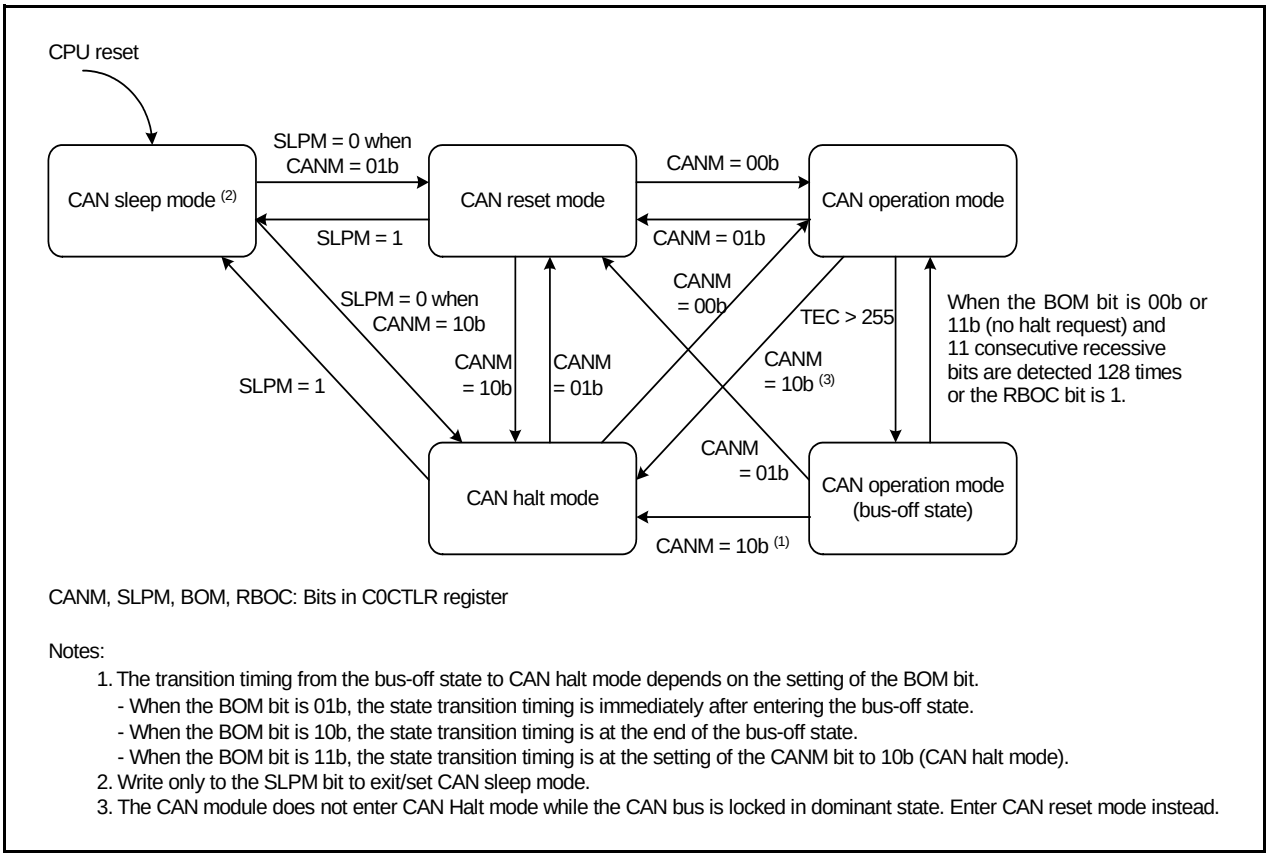
Figure 28.8 Connection when Self-Test Mode 1 is Selected

28.3 Operational Mode

The CAN module has the following four operating modes.

- CAN reset mode
- CAN halt mode
- CAN operation mode
- CAN sleep mode

Figure 28.9 shows the Transition between CAN Operating Modes.



CANM, SLPM, BOM, RBOC: Bits in C0CTLR register

Notes:

1. The transition timing from the bus-off state to CAN halt mode depends on the setting of the BOM bit.
   - When the BOM bit is 01b, the state transition timing is immediately after entering the bus-off state.
   - When the BOM bit is 10b, the state transition timing is at the end of the bus-off state.
   - When the BOM bit is 11b, the state transition timing is at the setting of the CANM bit to 10b (CAN halt mode).
2. Write only to the SLPM bit to exit/set CAN sleep mode.
3. The CAN module does not enter CAN Halt mode while the CAN bus is locked in dominant state. Enter CAN reset mode instead.

Figure 28.9 Transition between CAN Operating Modes

28.3.1 CAN Reset Mode

CAN reset mode is provided for CAN communication configuration.
When the CANM bit in the C0CTLR register is set to 01b, the CAN module enters CAN reset. Then the RSTST bit in the C0STR register is set to 1. Do not change the CANM bit until the RSTST bit is set to 1.
Configure the C0BCR register before exiting CAN reset mode to any other modes.

The following registers are initialized to their reset values after entering CAN reset mode and their initialized values are retained during CAN reset mode:

- C0MCTLj register (j = 0 to 15)
- C0STR register (except bits SLPST and TFST)
- C0EIFR register
- C0RECR register
- C0TECR register
- C0TSR register
- C0MSSR register
- C0MSMR register
- C0RFCR register
- C0TFCR register
- C0TCR register
- C0ECSR register (except EDPM bit)

The previous values of the following registers are retained after entering CAN reset mode.

- C0CTLR register
- C0STR register (bits SLPST and TFST)
- C0MIER register
- C0EIER register
- C0BCR register
- C0CSSR register
- C0ECSR register (EDPM bit only)
- C0MBj register
- Registers C0MKR0 to C0MKR3
- Registers C0FIDCR0 and C0FIDCR1
- C0MKIVLR register
- C0AFSR register
- C0RFPCR register
- C0TFPCR register

28.3.2 CAN Halt Mode

CAN halt mode is used for mailbox configuration and test mode setting.
When the CANM bit in the C0CTLR register is set to 10b, CAN halt mode is selected. Then the HLTST bit in the C0STR register is set to 1. Do not change the CANM bit until the HLTST bit is set to 1.
Refer to **Table 28.9 Operation in CAN Reset Mode and CAN Halt Mode** regarding the state transition conditions when transmitting or receiving.
All registers except bits RSTST, HLTST, and SLPST in the C0STR register remain unchanged when the CAN module enters CAN halt mode.
Do not change registers C0CLKR, C0CTLR (except bits CANM and SLPM,) and C0EIER in CAN halt mode.
The C0BCR register can be changed in CAN halt mode only when listen-only mode is selected to use for automatic bit rate detection.

Table 28.9 Operation in CAN Reset Mode and CAN Halt Mode

Mode	Receiver	Transmitter	Bus-off
CAN reset mode	CAN module enters CAN reset mode without waiting for the end of message reception.	CAN module enters CAN reset mode after waiting for the end of message transmission. (1, 4)	CAN module enters CAN reset mode without waiting for the end of bus-off recovery.
CAN halt mode	CAN module enters CAN halt mode after waiting for the end of message reception. (2, 3)	CAN module enters CAN halt mode after waiting for the end of message transmission. (1, 2, 4)	[When the BOM bit is 00b] A halt request from a program will be acknowledged only after bus-off recovery. [When the BOM bit is 01b] CAN module enters automatically to CAN halt mode without waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the BOM bit is 10b] CAN module enters automatically to CAN halt mode after waiting for the end of bus-off recovery (regardless of a halt request from a program). [When the BOM bit is 11b] CAN module enters CAN halt mode (without waiting for the end of bus-off recovery) if a halt is requested by a program during bus-off.

BOM bit: Bit in the C0CTLR register
Notes:
1. If several messages are requested to be transmitted, mode transition occurs after the completion of the first message transmission. When CAN reset mode is being requested during suspend transmission, mode transition occurs when the bus is idle, the next transmission ends, or the CAN module becomes a receiver.
2. If the CAN bus is locked in dominant state, the program can detect this state by monitoring the BLIF bit in the C0EIFR register. The CAN module does not enter CAN Halt mode while the CAN bus is locked in dominant state. Enter CAN reset mode instead.
3. If a CAN bus error occurs during reception after CAN halt mode is requested, the CAN module enters CAN halt mode. However, the CAN module does not enter CAN Halt mode when the CAN bus is locked in dominant state.
4. If a CAN bus error or arbitration lost occurs during transmission after CAN reset mode or CAN halt mode is requested, the CAN module enters the requested operating mode. However, the CAN module does not enter CAN Halt mode when the CAN bus is locked in dominant state.

28.3.3 CAN Sleep Mode

CAN sleep mode is used for reducing current consumption by stopping the clock supply to the CAN module. After MCU hardware reset or software reset, the CAN module starts from CAN module sleep mode.
When the SLPM bit in the C0CTLR register is set to 1, the CAN module enters CAN sleep mode. Then the SLPST bit in the C0STR register is set to 1. Do not change the value of the SLPM bit until the bit is set to 1. The other registers remain unchanged when the MCU enters CAN sleep mode.
Write to the SLPM bit in CAN reset mode and CAN halt mode. Do not change any other registers (except the SLPM bit) during CAN sleep mode. Read operation is still allowed.
When the SLPM bit is set to 0, the CAN module is released from CAN sleep mode. When the CAN module exits CAN sleep mode, the other registers remain unchanged.

28.3.4 CAN Operation Mode (Excluding Bus-Off State)

CAN operation mode is used for CAN communication.
When the CANM bit in the C0CTLR register is set to 00b, the CAN module enters CAN operation mode. Then bits RSTST and HLTST in the C0STR register are set to 0. Do not change the value of the CANM bit until these bits are set to 0.
If 11 consecutive recessive bits are detected after entering CAN operation mode, the CAN module is in the following states:

- The CAN module becomes an active node on the network that enables transmission and reception of CAN messages.
- Error monitoring of the CAN bus, such as receive and transmit error counters, is performed.

During CAN operation mode, the CAN module may be in one of the following three sub-modes, depending on the status of the CAN bus:

- Idle mode: Transmission or reception is not being performed.
- Receive mode: A CAN message sent by another node is being received.
- Transmit mode: A CAN message is being transmitted. The CAN module may receive its own message simultaneously when self-test mode 0 (TSTM bit in the C0STR register = 10b) or self-test mode 1 (TSTM bit = 11b) is selected.

Figure 28.10 shows the Sub Mode in CAN Operation Mode.

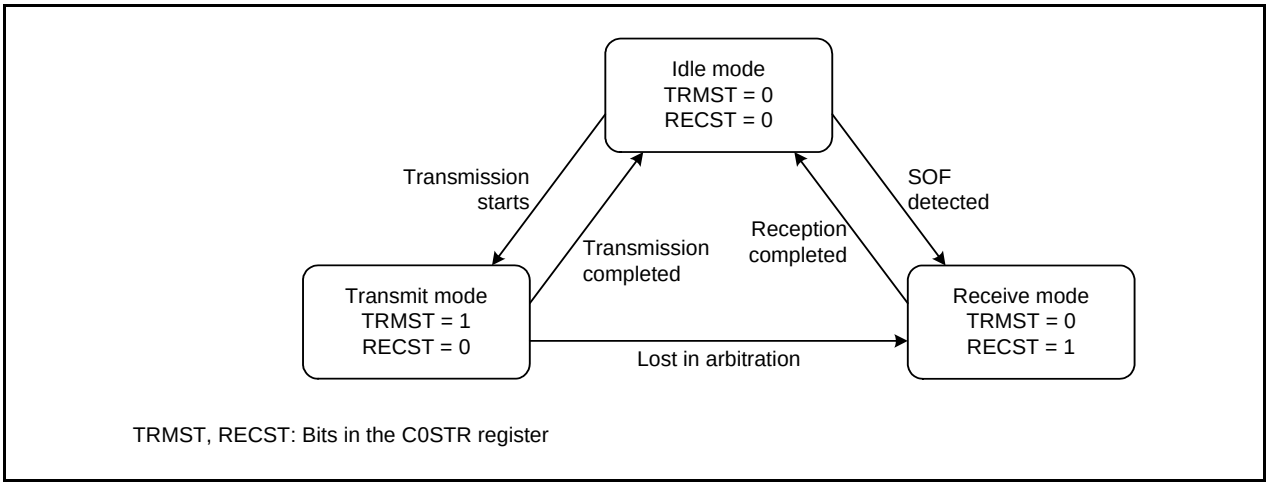


Figure 28.10 Sub Mode in CAN Operation Mode

28.3.5 CAN Operation Mode (Bus-Off State)

The CAN module enters the bus-off state according to the increment/decrement rules for the transmit/ error counters in the CAN Specifications.
The following cases apply when recovering from the bus-off state. When the CAN module is in bus-off state, the values of the associated registers, except registers C0STR, C0EIFR, C0RECR, C0TECR and C0TSR, remain unchanged.

(1) When the BOM bit in the C0CTLR register is 00b (normal mode)
The CAN module enters the error-active state after it has completed the recovery from the bus-off state and CAN communication is enabled. The BORIF bit in the C0EIFR register is set to 1 (bus-off recovery detected) at this time.

(2) When the RBOC bit in the C0CTLR register is set to 1 (forcible return from bus-off)
The CAN module enters the error-active state when it is in bus-off state and the RBOC bit is set to 1. CAN communication is enabled again after 11 consecutive recessive bits are detected. The BORIF bit is not set to 1 at this time.

(3) When the BOM bit is 01b (entry to CAN halt mode automatically at bus-off entry)
The CAN module enters CAN halt mode when it reaches the bus-off state. The BORIF bit is not set to 1 at this time.

(4) When the BOM bit is 10b (entry to CAN halt mode automatically at bus-off end)
The CAN module enters CAN halt mode when it has completed the recovery from bus-off. The BORIF bit is set to 1 at this time.

(5) When the BOM bit is 11b (entry to CAN halt mode by a program) and the CANM bit in the C0CTLR register is set to 10b (CAN halt mode) during the bus-off state
The CAN module enters CAN halt mode when it is in bus-off state and the CANM bit is set to 10b (CAN halt mode). The BORIF bit is not set to 1 at this time.
If the CANM bit is not set to 10b during bus-off, the same behavior as (1) applies.

28.4 CAN Communication Speed Configuration

The following description explains about the CAN communication speed configuration.

28.4.1 CAN Clock Configuration

The CAN clock can be configured by setting the BRP bit in the C0BCR register.
Figure 28.11 shows the Block Diagram of CAN Clock Generator.

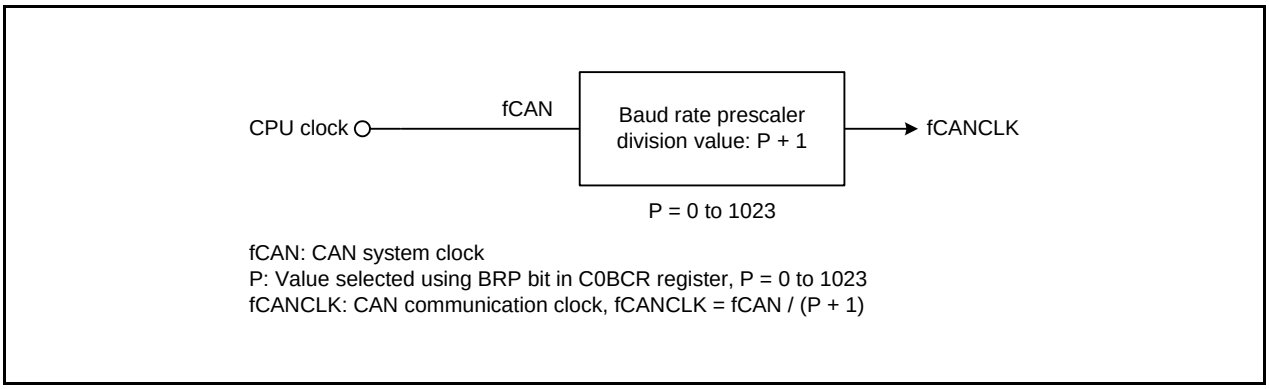


Figure 28.11 Block Diagram of CAN Clock Generator

28.4.2 Bit Timing Configuration

The bit time is a single bit time for transmitting/receiving a message and consists of the following three segments.
Figure 28.12 shows the Bit Timing.

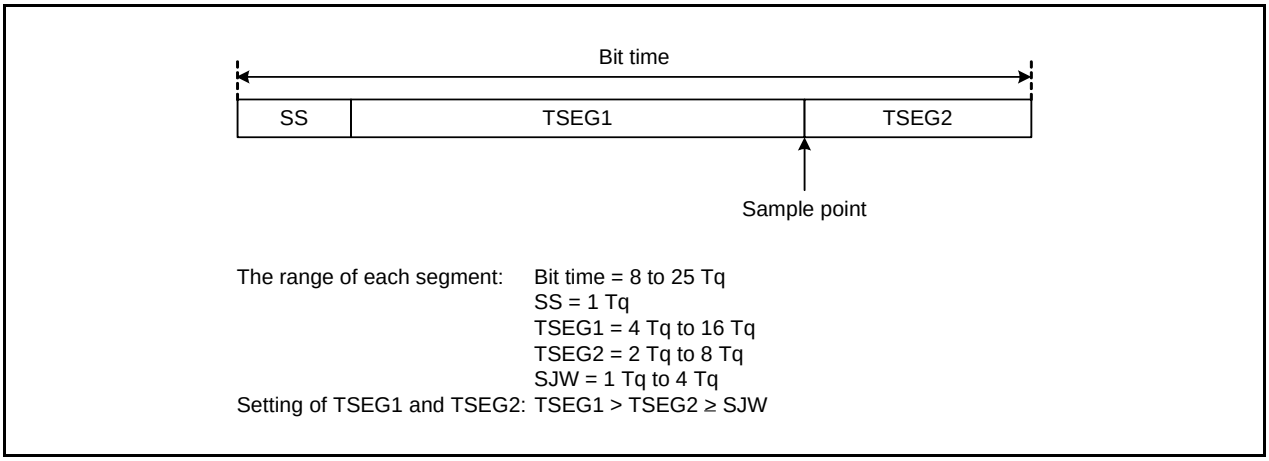


Figure 28.12 Bit Timing

28.4.3 Bit-rate

The bit rate depends on the CAN system clock (fCAN), the division value of the baud rate prescaler, and the number of Tq of one bit time.

$$\text{Bit rate[bps]} = \frac{fCAN}{\text{Baud rate prescaler division value}\ (1) \times \text{number of Tq of one bit time}} = \frac{\text{fCANCLK}}{\text{Number of Tq of one bit time}}$$

Note:
1. Division value of the baud rate prescaler = P + 1 (P = 0 to 1023)
   P: Setting value of the BRP bit in the C0BCR register

Table 28.10 lists the Bit Rate Examples.

Table 28.10 Bit Rate Examples

fCAN	20 MHz		16 MHz		8 MHz	
Bit Rate	No. of Tq	P+1	No. of Tq	P+1	No. of Tq	P+1
1 Mbps	10 Tq	2	8 Tq	2	8 Tq	1
	20 Tq	1	16 Tq	1		
500 kbps	10 Tq	4	8 Tq	4	8 Tq	2
	20 Tq	2	16 Tq	2	16 Tq	1
250 kbps	10 Tq	8	8 Tq	8	8 Tq	4
	20 Tq	4	16 Tq	4	16 Tq	2
83.3 kbps	8 Tq	30	8 Tq	24	8 Tq	12
	10 Tq	24	16 Tq	12	16 Tq	6
	16 Tq	15				
	20 Tq	12				
33.3 kbps	8 Tq	75	8 Tq	60	8 Tq	30
	10 Tq	60	10 Tq	48	10 Tq	24
	20 Tq	30	16 Tq	30	16 Tq	15
			20 Tq	24	20 Tq	12

28.5 Mailbox and Mask Register Structure

There are 16 mailboxes with the same structure.
Figure 28.13 shows the Structure of C0MBj Register (j = 0 to 15).

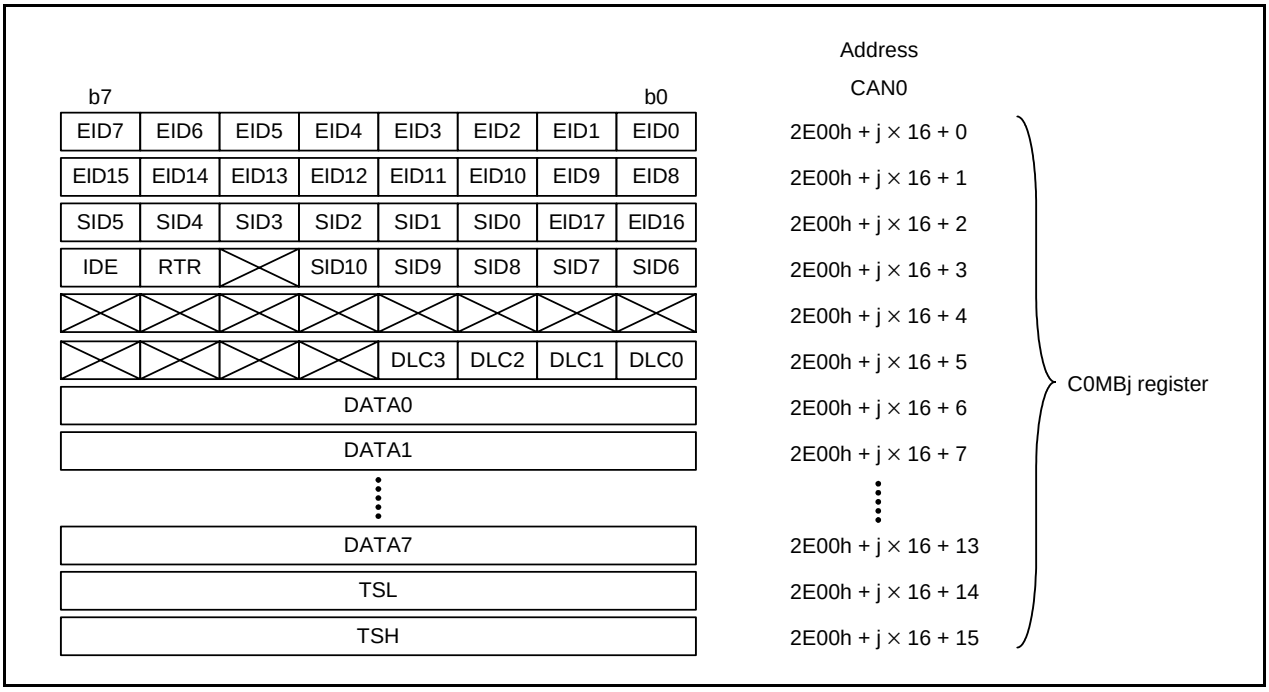


Figure 28.13 Structure of C0MBj Register (j = 0 to 15)

There are 4 mask registers with the same structure.
Figure 28.14 shows the Structure of C0MKRk Register (k = 0 to 3).

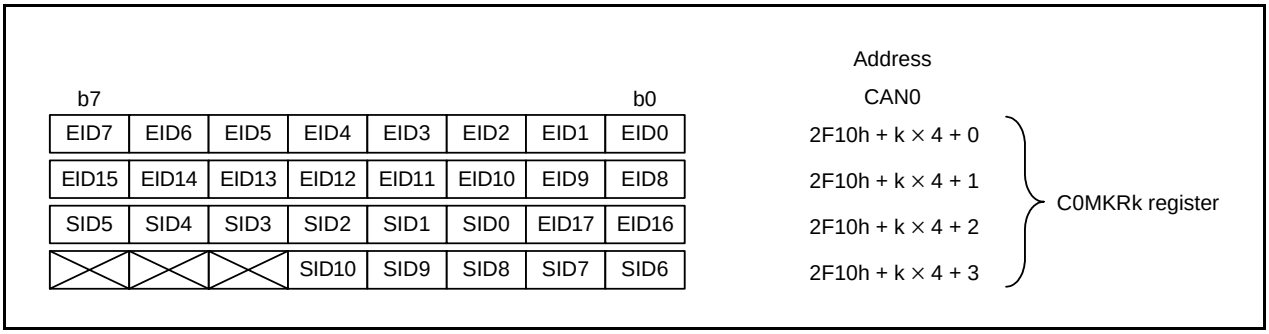


Figure 28.14 Structure of C0MKRk Register (k = 0 to 3)

There are 4 FIFO received ID compare registers with the same structure.
Figure 28.15 shows the Structure of C0FIDCRn Register (n = 0, 1).

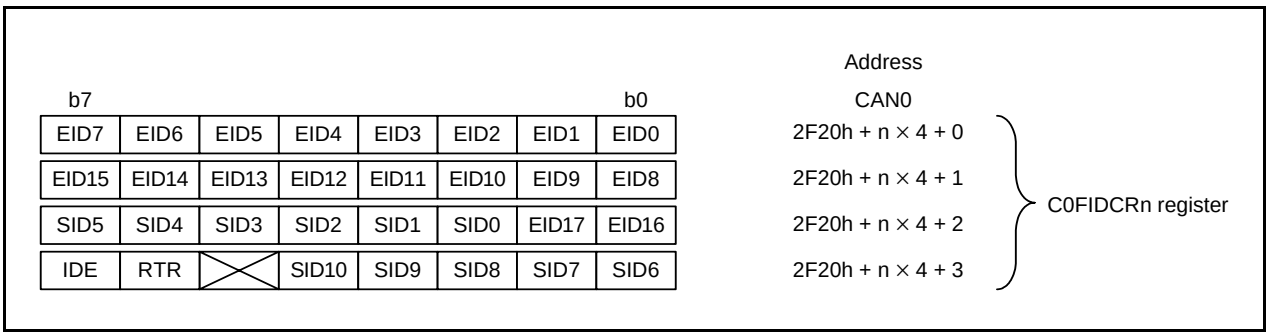


Figure 28.15 Structure of C0FIDCRn Register (n = 0, 1)

28.6 Acceptance Filtering and Masking Function

Acceptance filtering allows the user to receive messages with a specified range of multiple IDs for mailboxes.
Registers C0MKR0 to C0MKR3 can perform masking of the standard ID and the extended ID of 29 bits.

- The C0MKR0 register corresponds to mailboxes [0] to [3].
- The C0MKR1 register corresponds to mailboxes [4] to [7].
- The C0MKR2 register corresponds to mailboxes [8] to [11] in normal mailbox mode, and receive FIFO mailboxes [12] to [15] in FIFO mailbox mode.
- The C0MKR3 register corresponds to mailboxes [12] to [15] in normal mailbox mode, and receive FIFO mailboxes [12] to [15] in FIFO mailbox mode.

The C0MKIVLR register disables acceptance filtering individually for each mailbox.

The IDE bit in the C0MBj register (j = 0 to 15) is enabled when the IDFM bit in the C0CTLR register is 10b (mixed ID mode).
The RTR bit in the C0MBj register selects a data frame or a remote frame.

In FIFO mailbox mode, normal mailboxes (mailboxes [0] to [7]) use the single corresponding register among registers C0MKR0 and C0MKR1 for acceptance filtering. Receive FIFO mailboxes (mailboxes [12] to [15]) use two registers C0MKR2 and C0MKR3 for the acceptance filtering.
Also, the receive FIFO uses two registers C0FIDCR0 and C0FIDCR1 for ID comparison. Bits EID, SID, RTR, and IDE in registers C0MB12 to C0MB15 for the receive FIFO are disabled. As acceptance filtering depends on the result of two ID-mask sets, two ranges of IDs can be received into the receive FIFO.
The C0MKIVLR register is disabled for the receive FIFO.

If both setting of standard ID and extended ID are set in the IDE bits in registers C0FIDCR0 and C0FIDCR1 individually, both ID formats are received.
If both setting of data frame and remote frame are set in the RTR bits in registers C0FIDCR0 and C0FIDCR1 individually, both data and remote frames are received.
When combination with two ranges of IDs is not necessary, set the same mask value and the same ID into both of the FIFO ID/mask register sets.

Figure 28.16 shows the Correspondence of Mask Registers to Mailboxes, and Figure 28.17 shows the Acceptance Filtering.

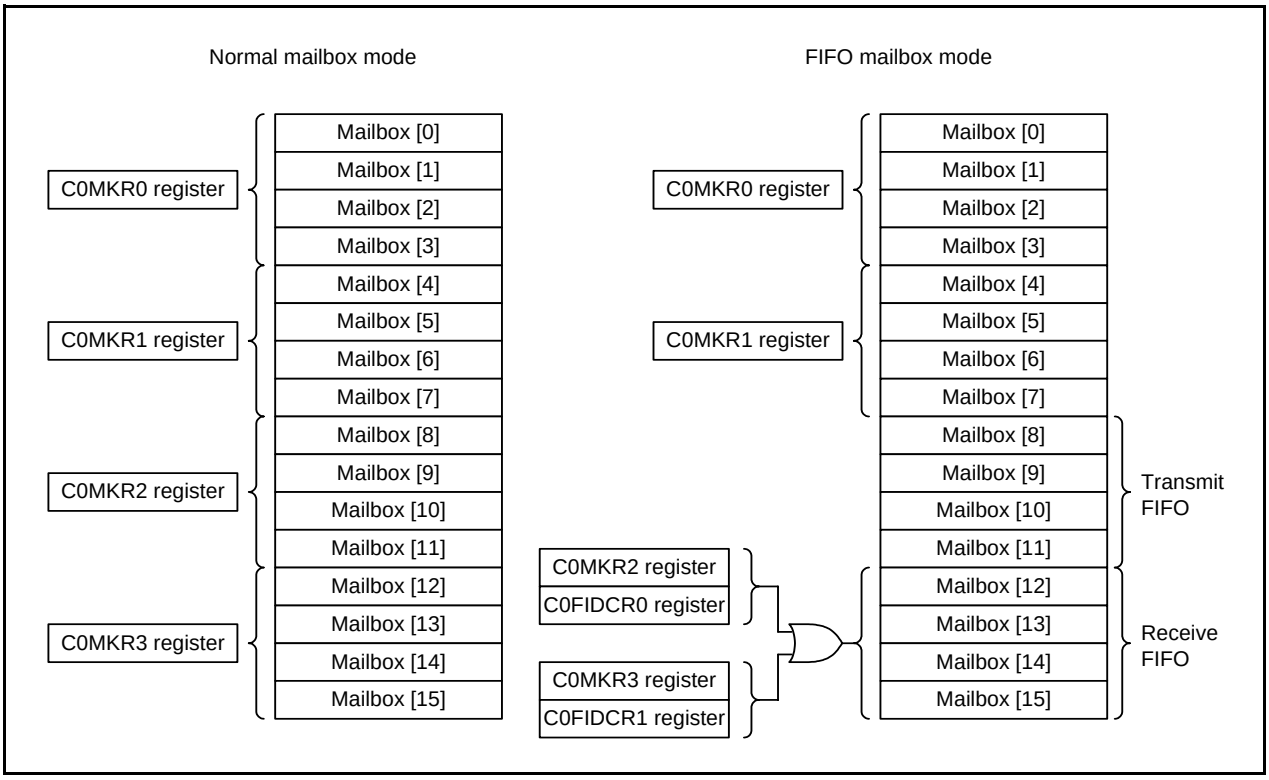


Figure 28.16 Correspondence of Mask Registers to Mailboxes

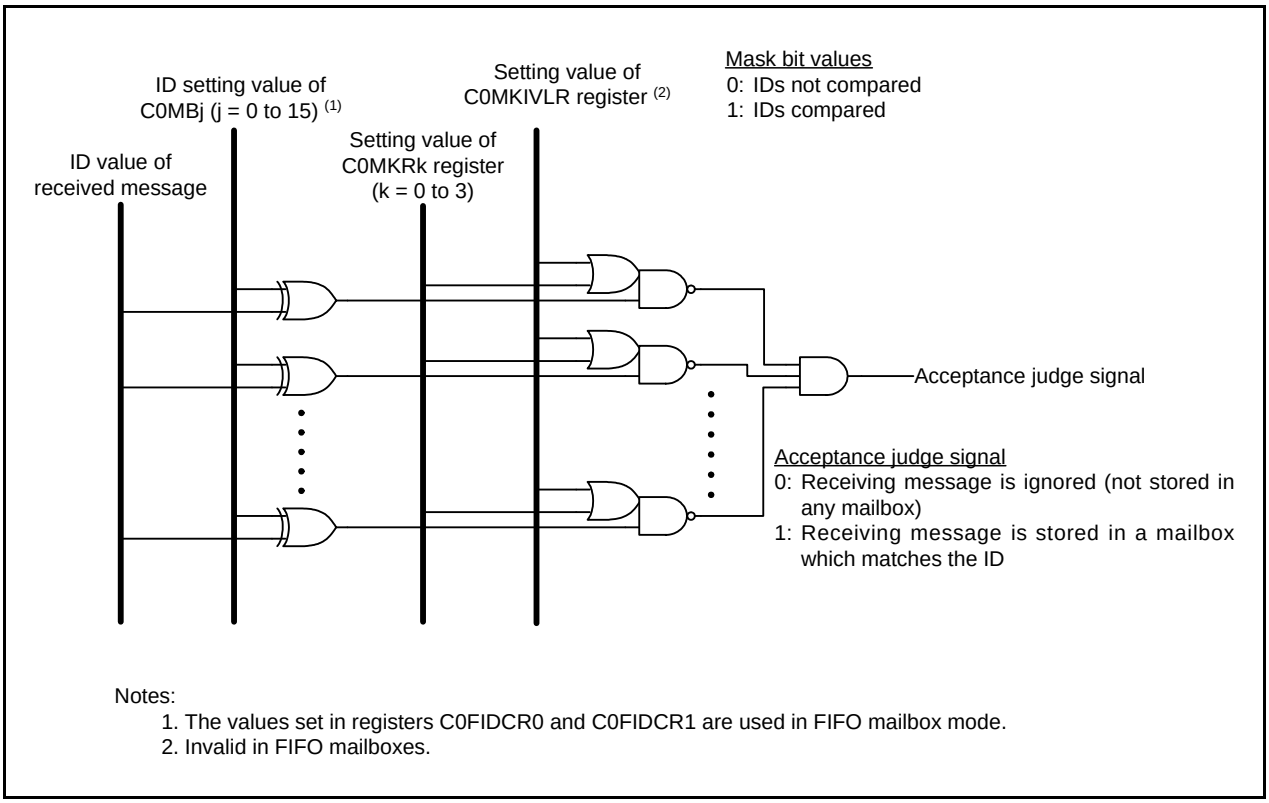


Figure 28.17 Acceptance Filtering

28.7 Reception and Transmission

Table 28.11 list the Configuration for CAN Reception Mode and Transmission Mode.

Table 28.11 Configuration for CAN Reception Mode and Transmission Mode

TRMREQ	RECREQ	ONESHOT	Communication mode of mailbox
0	0	0	Mailbox disabled or transmission being aborted.
0	0	1	Configurable only when transmission or reception from a mailbox (programmed in one-shot mode) is aborted.
0	1	0	Configured as a receive mailbox for a data frame or a remote frame.
0	1	1	Configured as a one-shot receive mailbox for a data frame or a remote frame.
1	0	0	Configured as a transmit mailbox for a data frame or a remote frame.
1	0	1	Configured as a one-shot transmit mailbox for a data frame or a remote frame.
1	1	0	Do not set.
1	1	1	Do not set.

TRMREQ, RECREQ, ONESHOT: Bits in C0MCTLj register (j = 0 to 15)

When a mailbox is configured as a receive mailbox or a one-shot receive mailbox, note the following:

(1) Before a mailbox is configured as a receive mailbox or a one-shot receive mailbox, set the C0MCTLj register (j = 0 to 15) to 00h.

(2) A received message is stored into the first mailbox that matches the condition according to the result of receive mode configuration and acceptance filtering. Upon deciding a mailbox which stores the received message, the mailbox with the smaller number has higher priority.

(3) In CAN operation mode, when a CAN module transmits a message whose ID matches with the ID/ mask set of a mailbox configured to receive messages, the CAN module never receives the transmitted data. In self-test mode, however, the CAN module may receive its transmitted data. In this case, the CAN module sends an ACK.

When configuring a mailbox as a transmit mailbox or a one-shot transmit mailbox, note the following:

(1) Before a mailbox is configured as a transmit mailbox or one-shot transmit mailbox, ensure that the C0MCTLj register is 00h and that there is no pending abort process.

28.7.1 Reception

Figure 28.18 shows the Operation Example of Data Frame Reception in Overwrite Mode.
This example shows the operation of overwriting the first message when the CAN module receives two consecutive CAN messages that matches the receiving conditions of the C0MCTL0 register.

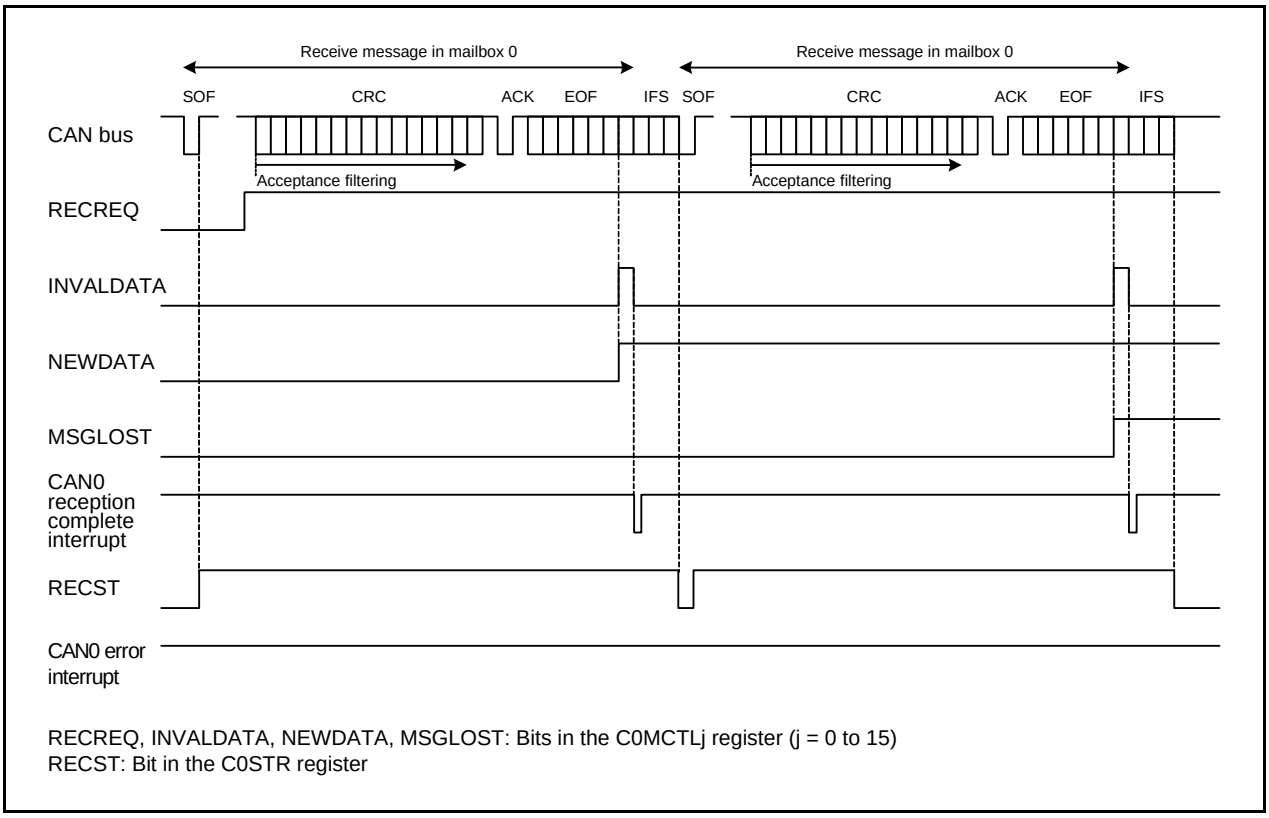


Figure 28.18 Operation Example of Data Frame Reception in Overwrite Mode

(1) When a SOF is detected on the CAN bus, the RECST bit in the C0STR registers set to 1 (reception in progress) if the CAN module has no message ready to start transmission.
(2) The acceptance filter procedure starts at the beginning of the CRC field to select the receive mailbox.
(3) After a message has been received, the NEWDATA bit in the C0MCTLj register (j = 0 to 15) for the receive mailbox is set to 1 (new data being updated/stored in the mailbox). The INVALDATA bit in the C0MCTLj register is set to 1 (message is being updated) at the same time, and then the INVALDATA bit is set to 0 (message valid) again after the complete message is transferred to the mailbox.
(4) When the interrupt enable bit in the C0MIER register for the receive mailbox is 1 (interrupt enabled), the CAN0 reception complete interrupt request is generated. This interrupt is generated when the INVALDATA bit is set to 0.
(5) After reading the message from the mailbox, the NEWDATA bit needs to be set to 0 by a program.
(6) In overwrite mode, if the next CAN message has been received into a mailbox whose NEWDATA bit is still set to 1, the MSGLOST bit in the C0MCTLj register is set to 1 (message has been overwritten). The new received message is transferred to the mailbox. The CAN0 reception complete interrupt request is generated the same as in (4).

Figure 28.19 shows the Operation Example of Data Frame Reception in Overrun Mode.
This example shows the operation of overrunning the second message when the CAN module receives two consecutive CAN messages that matches the receiving conditions of the C0MCTL0 register.

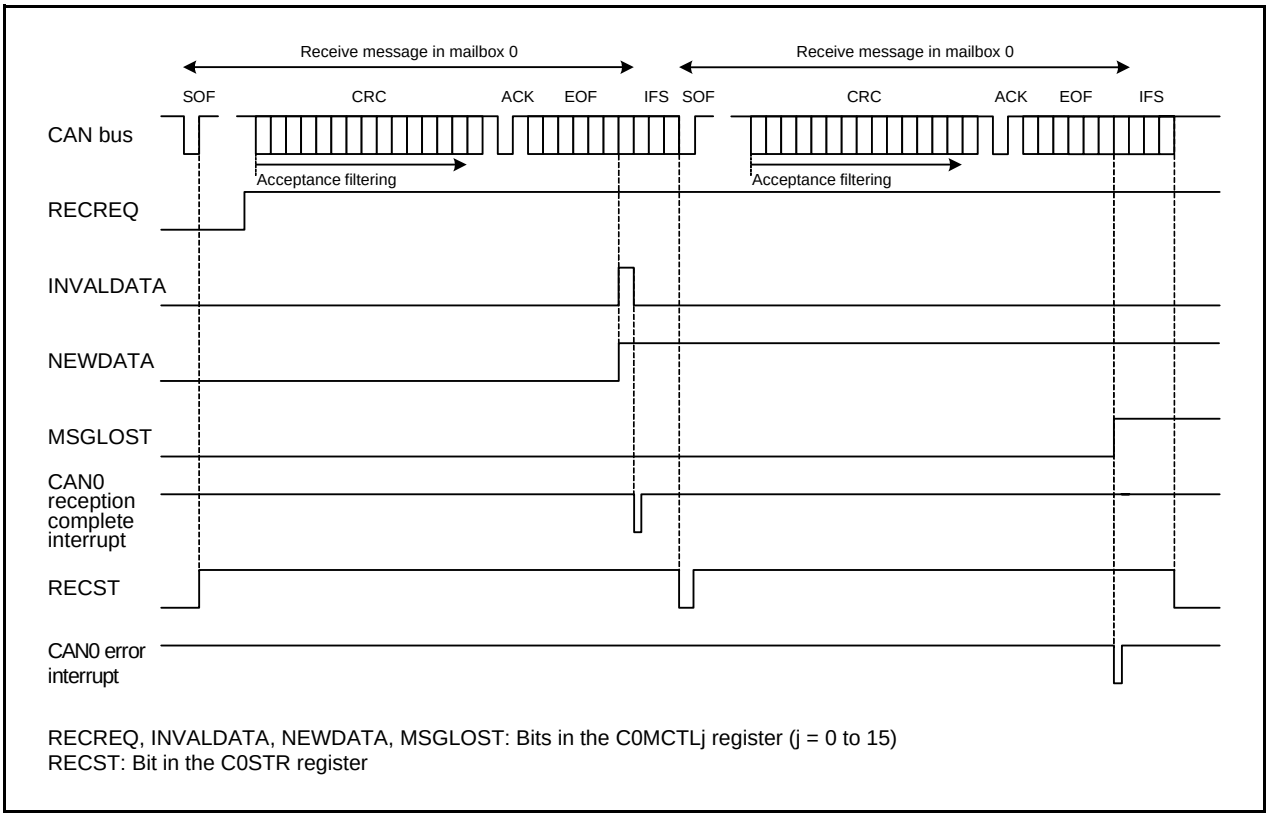


Figure 28.19 Operation Example of Data Frame Reception in Overrun Mode

(1) to (5) are same as overwrite mode.

(6) In overrun mode, if the next message has been received before the NEWDATA bit is set to 0, the MSGLOST bit in the C0MCTLj register (j = 0 to 15) is set to 1 (message has been overrun). The new received message is discarded and a CAN0 error interrupt request is generated if the corresponding interrupt enable bit in the C0EIER register is set to 1 (interrupt enabled).

28.7.2 Transmission

Figure 28.20 shows the Operation Example of Data Frame Transmission. This example shows the operation of transmitting messages that has been set in registers C0MCTL0 and C0MCTL1.

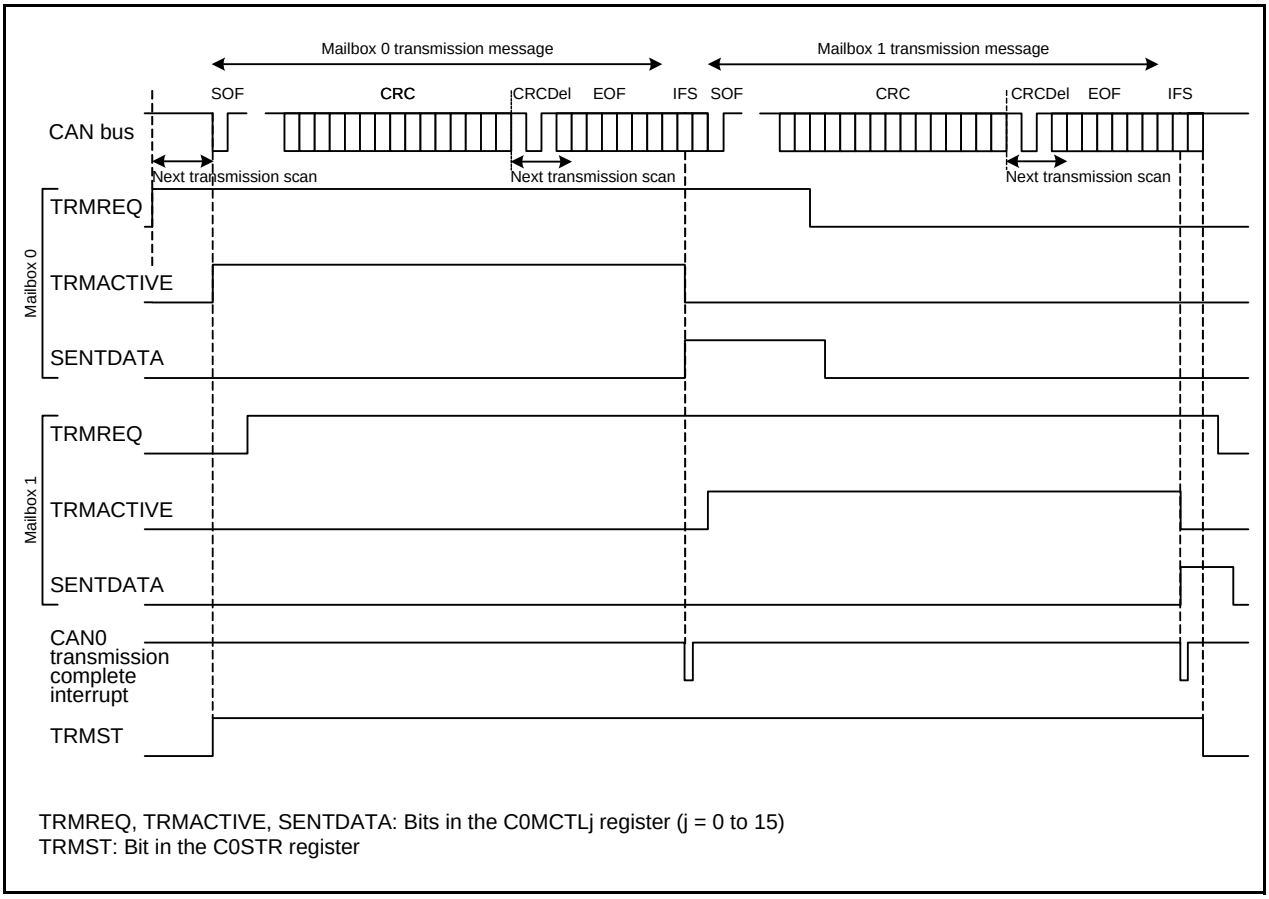


Figure 28.20 Operation Example of Data Frame Transmission

(1) When a TRMREQ bit in the C0MCTLj register (j = 0 to 15) is set to 1 (transmit mailbox) in bus-idle state, the mailbox scan procedure starts to decide the highest-priority mailbox for transmission. Once the transmit mailbox is decided, the TRMACTIVE bit in the C0MCTLj register is set to 1 (from when a transmission request is received until transmission is completed, or an error/arbitration lost has occurred), the TRMST bit in the C0STR register is set to 1 (transmission in progress), and the CAN module starts transmission. (1)

(2) If other TRMREQ bits are set, the transmission scan procedure starts with the CRC delimiter for the next transmission.

(3) If transmission is completed without losing arbitration, the SENTDATA bit in the C0MCTLj register is set to 1 (transmission completed) and the TRMACTIVE bit is set to 0 (transmission is pending, or no transmission request). If the interrupt enable bit in the C0MIER register is 1 (interrupt enabled), the CAN0 transmission complete interrupt request is generated.

(4) When requesting the next transmission from the same mailbox, set bits SENDTDATA and TRMREQ to 0, then set the TRMREQ bit to 1 after checking that bits SENDTDATA and TRMREQ have been set to 0.

Note:

1. If arbitration is lost after the CAN module starts transmission, the TRMACTIVE bit is set to 0. The transmission scan procedure is performed again to search for the highest-priority transmit mailbox from the beginning of the CRC delimiter. If an error occurs either during transmission or following the loss of arbitration, the transmission scan procedure is performed again from the start of the error delimiter to search for the highest-priority transmit mailbox.

28.8 CAN Interrupt

The CAN module provides the following CAN interrupts:

- CAN0 reception complete interrupt
- CAN0 transmission complete interrupt
- CAN0 receive FIFO interrupt
- CAN0 transmit FIFO interrupt
- CAN0 error interrupt
  There are eight types of interrupt sources for the CAN0 error interrupts. These sources can be determined by checking the C0EIFR register.
  - Bus error
  - Error warning
  - Error passive
  - Bus-off entry
  - Bus-off recovery
  - Reception overrun
  - Overload frame transmission
  - Bus lock
- CAN0 wake-up interrupt

29. A/D Converter

The A/D converter consists of one 10-bit successive approximation A/D converter circuit with a capacitive coupling amplifier. The analog input shares pins P0_0 to P0_7, P1_0 to P1_3, and P7_0 to P7_7.

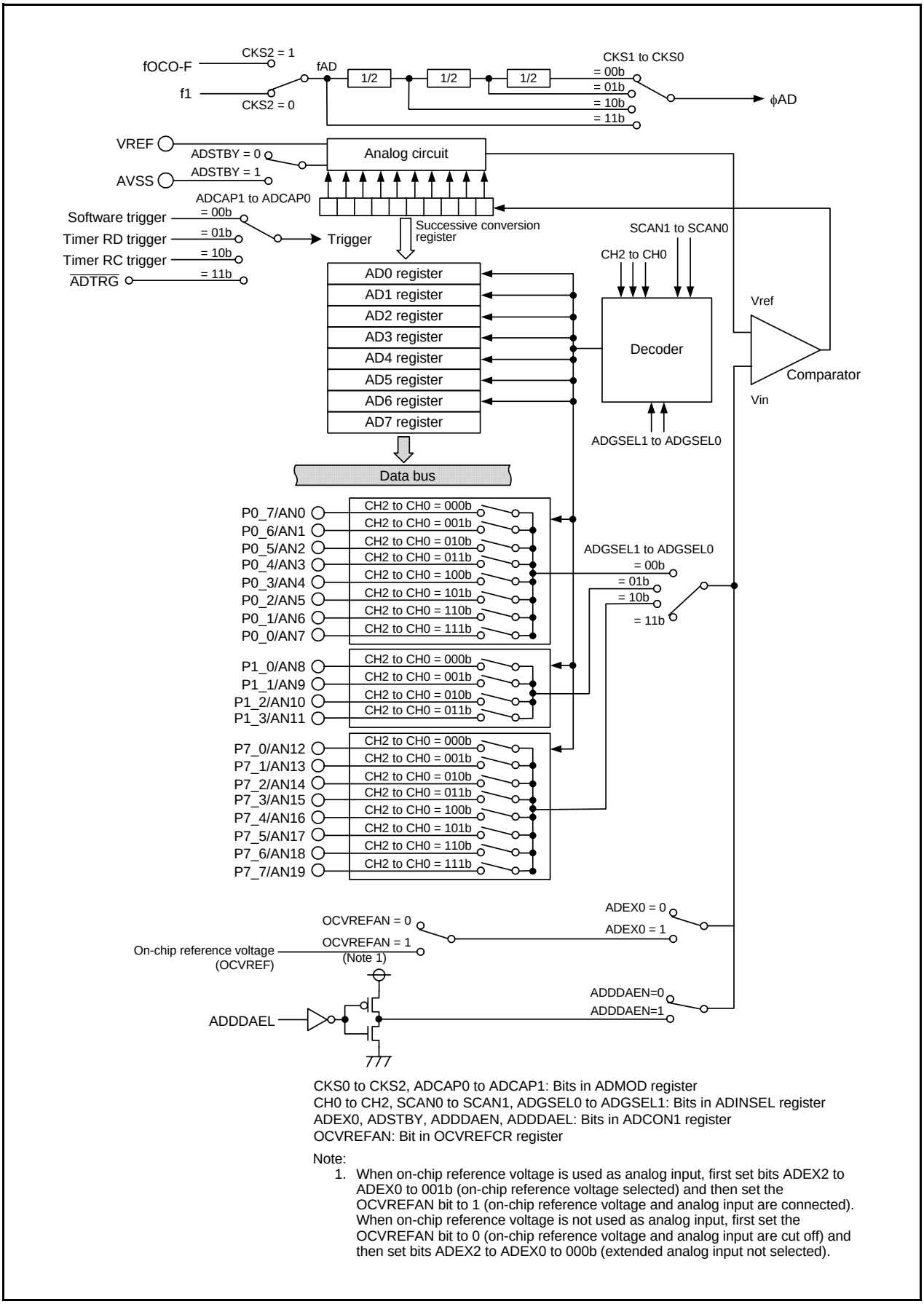
29.1 Overview

Table 29.1 lists the A/D Converter Performance. Figure 29.1 shows a Block Diagram of A/D Converter.

Table 29.1 A/D Converter Performance

Item	Performance
A/D conversion method	Successive approximation (with capacitive coupling amplifier)
Analog input voltage (1)	0 V to AVCC
Operating clock ϕAD (2)	fAD, fAD divided by 2, fAD divided by 4, fAD divided by 8 (fAD=f1 or fOCO-F)
Resolution	8 bits or 10 bits selectable
Absolute accuracy	AVCC = Vref = 5 V, ϕAD = 20 MHz • 8-bit resolution ±2 LSB • 10-bit resolution ±3 LSB AVCC = Vref = 3.0 V, ϕAD = 10 MHz • 8-bit resolution ±2 LSB • 10-bit resolution ±5 LSB
Operating mode	One-shot mode, repeat mode 0, repeat mode 1, single sweep mode, and repeat sweep mode
Analog input pin	20 pins (AN0 to AN19)
A/D conversion start condition	• Software trigger • Timer RD • Timer RC • External trigger (Refer to **29.3.3 A/D Conversion Start Condition**.)
Conversion rate per pin (3) (ϕAD = fAD)	Minimum 44 ϕAD cycles

Notes:
1. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.
2. Refer to **Table 32.4 A/D Converter Characteristics** for the operating clock ϕAD.
3. Conversion rate per pin is minimum 44 ϕAD cycles for both 8-bit resolution and 10-bit resolution.



CKS0 to CKS2, ADCAP0 to ADCAP1: Bits in ADMOD register
CH0 to CH2, SCAN0 to SCAN1, ADGSEL0 to ADGSEL1: Bits in ADINSEL register
ADEX0, ADSTBY, ADDDAEN, ADDDAEL: Bits in ADCON1 register
OCVREFAN: Bit in OCVREFCR register

Note:
1. When on-chip reference voltage is used as analog input, first set bits ADEX2 to ADEX0 to 001b (on-chip reference voltage selected) and then set the OCVREFAN bit to 1 (on-chip reference voltage and analog input are connected). When on-chip reference voltage is not used as analog input, first set the OCVREFAN bit to 0 (on-chip reference voltage and analog input are cut off) and then set bits ADEX2 to ADEX0 to 000b (extended analog input not selected).

Figure 29.1 Block Diagram of A/D Converter

29.2 Registers

29.2.1 On-Chip Reference Voltage Control Register (OCVREFCR)

Address 0026h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	OCVREFAN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	OCVREFAN	On-chip reference voltage to analog input connect bit (1)	0: On-chip reference voltage and analog input are cut off 1: On-chip reference voltage and analog input are connected	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

Note:

1. When on-chip reference voltage is used as analog input, first set bits ADEX2 to ADEX0 in the ADCON1 register to 001b (on-chip reference voltage selected) and then set the OCVREFAN bit to 1 (on-chip reference voltage and analog input are connected).
   When on-chip reference voltage is not used as analog input, first set the OCVREFAN bit to 0 (on-chip reference voltage and analog input are cut off) and then set bits ADEX2 to ADEX0 to 000b (extended analog input not selected).

   Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the OCVREFCR register.
   If the contents of the OCVREFCR register are rewritten during A/D conversion, the conversion result is undefined.

29.2.2 A/D Register i (ADi) (i = 0 to 7)

Address 00C1h to 00C0h (AD0), 00C3h to 00C2h (AD1), 00C5h to 00C4h (AD2), 00C7h to 00C6h (AD3), 00C9h to 00C8h (AD4), 00CBh to 00CAh (AD5), 00CDh to 00CCh (AD6), 00CFh to 00CEh (AD7)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	X	X

Bit	Function		R/W
	10-Bit Mode (BITS Bit in ADCON1 Register = 1)	8-Bit Mode (BITS Bit in ADCON1 Register = 0)	
b0	8 low-order bits in A/D conversion result	A/D conversion result	R
b1			
b2			
b3			
b4			
b5			
b6			
b7			
b8	2 high-order bits in A/D conversion result	When read, the content is 0.	R
b9			
b10	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b11			
b12			
b13			
b14			
b15	Reserved bit	When read, the content is undefined.	R

If the contents of the ADCON1, ADMOD, ADINSEL, or OCVREFCR register are written during A/D conversion, the conversion result is undefined.

When using the A/D converter in 10-bit mode, repeat mode 0, repeat mode 1, or repeat sweep mode, access the ADi register in 16-bit units. Do not access it in 8-bit units.

29.2.3 A/D Mode Register (ADMOD)

Address 00D4h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADCAP1	ADCAP0	MD2	MD1	MD0	CKS2	CKS1	CKS0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CKS0	Division select bit	b1 b0 0 0: fAD divided by 8 0 1: fAD divided by 4 1 0: fAD divided by 2 1 1: fAD divided by 1 (no division)	R/W
b1	CKS1			R/W
b2	CKS2	Clock source select bit (1)	0: Selects f1 1: Selects fOCO-F	R/W
b3	MD0	A/D operating mode select bit	b5 b4 b3 0 0 0: One-shot mode 0 0 1: Do not set. 0 1 0: Repeat mode 0 0 1 1: Repeat mode 1 1 0 0: Single sweep mode 1 0 1: Do not set. 1 1 0: Repeat sweep mode 1 1 1: Do not set.	R/W
b4	MD1			R/W
b5	MD2			R/W
b6	ADCAP0	A/D conversion trigger select bit	b7 b6 0 0: A/D conversion starts by software trigger (ADST bit in ADCON0 register) 0 1: A/D conversion starts by conversion trigger from timer RD 1 0: A/D conversion starts by conversion trigger from timer RC 1 1: A/D conversion starts by external trigger ($\overline{\text{ADTRG}}$)	R/W
b7	ADCAP1			R/W

Note:
1. When the CKS2 bit is changed, wait for 3 ϕAD cycles or more before starting A/D conversion.

If the ADMOD register is rewritten during A/D conversion, the conversion result is undefined.

29.2.4 A/D Input Select Register (ADINSEL)

Address 00D5h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADGSEL1	ADGSEL0	SCAN1	SCAN0	—	CH2	CH1	CH0
After Reset	1	1	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CH0	Analog input pin select bit	Refer to **Table 29.2 Analog Input Pin Selection**	R/W
b1	CH1			R/W
b2	CH2			R/W
b3	—	Reserved bit	Set to 0.	R/W
b4	SCAN0	A/D sweep pin count select bit	b5 b4 0 0: 2 pins 0 1: 4 pins 1 0: 6 pins 1 1: 8 pins	R/W
b5	SCAN1			R/W
b6	ADGSEL0	A/D input group select bit	b7 b6 0 0: Port P0 group selected 0 1: Port P1 group selected 1 0: Port P7 group selected 1 1: Port group not selected	R/W
b7	ADGSEL1			R/W

If the ADINSEL register is rewritten during A/D conversion, the conversion result is undefined.

Table 29.2 Analog Input Pin Selection

Bits CH2 to CH0	Bits ADGSEL1, ADGSEL0 = 00b	Bits ADGSEL1, ADGSEL0 = 01b	Bits ADGSEL1, ADGSEL0 = 10b
000b	AN0	AN8	AN12
001b	AN1	AN9	AN13
010b	AN2	AN10	AN14
011b	AN3	AN11	AN15
100b	AN4	Do not set.	AN16
101b	AN5		AN17
110b	AN6		AN18
111b	AN7		AN19

29.2.5 A/D Control Register 0 (ADCON0)

Address 00D6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	ADST
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADST	A/D conversion start flag	0: Stop A/D conversion 1: Start A/D conversion	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

ADST Bit (A/D conversion start flag)

[Conditions for setting to 1]
When A/D conversion starts and while A/D conversion is in progress.
[Condition for setting to 0]
When A/D conversion stops.

29.2.6 A/D Control Register 1 (ADCON1)

Address 00D7h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADDDAEL	ADDDAEN	ADSTBY	BITS	—	—	—	ADEX0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADEX0	Extended analog input select bit (1)	0: Extended analog input not selected 1: On-chip reference voltage selected (2, 6, 7)	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			R/W
b3	—			R/W
b4	BITS	8/10-bit mode select bit	0: 8-bit mode 1: 10-bit mode	R/W
b5	ADSTBY	A/D standby bit (3)	0: A/D operation stops (standby) (4) 1: A/D operation enabled	R/W
b6	ADDDAEN	A/D open-circuit detection assist function enable bit (5, 7)	0: Disabled 1: Enabled	R/W
b7	ADDDAEL	A/D open-circuit detection assist method select bit (5)	0: Discharge before conversion 1: Precharge before conversion	R/W

Notes:

1. When on-chip reference voltage is used as analog input, first set bits ADEX2 to ADEX0 in the ADCON1 register to 001b (on-chip reference voltage selected) and then set the OCVREFAN bit to 1 (on-chip reference voltage and analog input are connected).
   When on-chip reference voltage is not used as analog input, first set the OCVREFAN bit to 0 (on-chip reference voltage and analog input are cut off) and then set bits ADEX2 to ADEX0 to 000b (extended analog input not selected).
2. Do not set to 1 (A/D conversion using comparison reference voltage as input) in single sweep mode or repeat sweep mode.
3. When the ADSTBY bit is changed from 0 (A/D operation stops) to 1 (A/D operation enabled), wait for 1 ϕAD cycle or more before starting A/D conversion.
4. Stop the A/D function before setting to standby. When the ADSTBY bit is set to 0 (standby), any access to the A/D associated registers (addresses 00C0h to 00CFh, and 00D4h to 00D7h) is disabled.
   However, only the ADSTBY bit can be accessed in the ADCON1 register at address 00D7h.
5. To enable the A/D open-circuit detection assist function, select the conversion start state with the ADDDAEL bit after setting the ADDDAEN bit to 1 (enabled).
   The conversion result with an open circuit varies with external circuits. Careful evaluation should be performed according to the system before using this function.
6. When on-chip reference voltage is used (ADEX0 = 1), set bits CH2 to CH0 in the ADINSEL register to 000b.
7. When on-chip reference voltage is used (ADEX0 = 1), set the ADDDAEN bit to 0 (A/D open-circuit detection assist function disabled).

If the ADCON1 register is rewritten during A/D conversion, the conversion result is undefined.

29.3 Common Items for Multiple Modes

29.3.1 Input/Output Pins

The analog input shares pins P0_0 to P0_7, P1_0 to P1_3, and P7_0 to P7_7 in AN0 to AN19.
When using the ANi (i = 0 to 19) pin as input, set the corresponding port direction bit to 0 (input mode).
After changing the A/D operating mode, select an analog input pin again.

29.3.2 A/D Conversion Cycles

Figure 29.2 shows a Timing Diagram of A/D Conversion. Figure 29.3 shows the A/D Conversion Cycles (ϕAD = fAD).

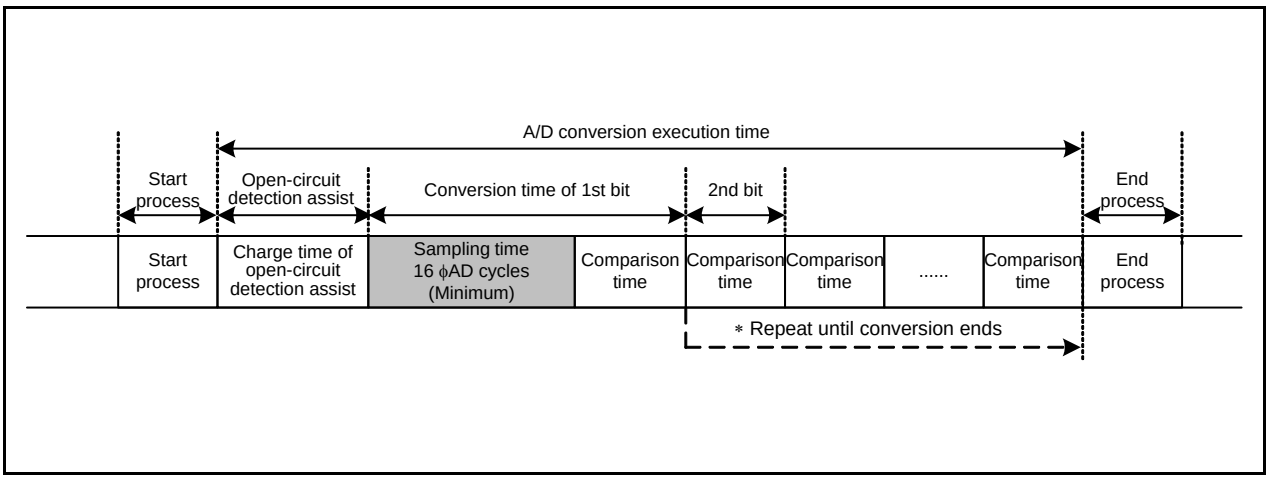
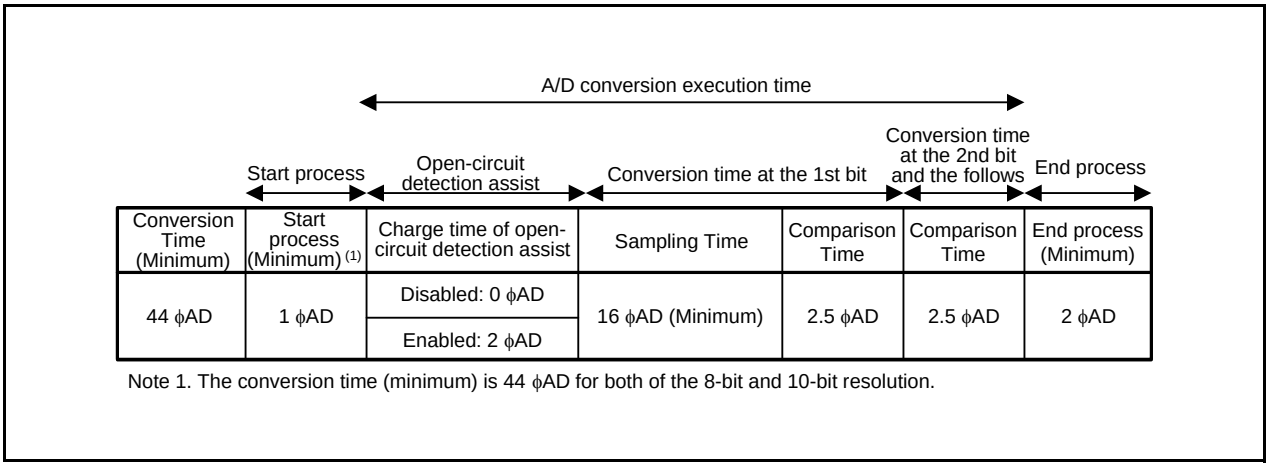


Figure 29.2 Timing Diagram of A/D Conversion



Conversion Time (Minimum)	Start process (Minimum) (1)	Charge time of open-circuit detection assist	Sampling Time	Comparison Time	Comparison Time	End process (Minimum)
44 ϕAD	1 ϕAD	Disabled: 0 ϕAD	16 ϕAD (Minimum)	2.5 ϕAD	2.5 ϕAD	2 ϕAD
		Enabled: 2 ϕAD				

Note 1. The conversion time (minimum) is 44 ϕAD for both of the 8-bit and 10-bit resolution.

Figure 29.3 A/D Conversion Cycles (ϕAD = fAD)

Table 29.3 shows the Number of Cycles for A/D Conversion Items. The A/D conversion time is defined as follows.
The start process time varies depending on which ϕAD is selected.
When 1 (A/D conversion starts) is written to the ADST bit in the ADCON0 register, an A/D conversion starts after the start process time has elapsed. Reading the ADST bit before the A/D conversion returns 0 (A/D conversion stops).
In the modes where an A/D conversion is performed on multiple pins or multiple times, the between-execution process time is inserted between the A/D conversion execution time for one pin and the next A/D conversion time.
In one-shot mode and single sweep mode, the ADST bit is set to 0 during the end process time and the last A/D conversion result is stored in the ADi register.

- In on-shot mode
  Start process time + A/D conversion execution time + end process time

- When two pins are selected in single sweep mode
  Start process time + (A/D conversion execution time + between-execution process time + A/D conversion execution time) + end process time

Table 29.3 Number of Cycles for A/D Conversion Items

A/D Conversion Item		Number of Cycles
Start process time	ϕAD = fAD	1 or 2 fAD cycles
	ϕAD = fAD divided by 2	2 or 3 fAD cycles
	ϕAD = fAD divided by 4	3 or 4 fAD cycles
	ϕAD = fAD divided by 8	5 or 6 fAD cycles
A/D conversion execution time	Disabled open-circuit detection assist	40 ϕAD cycles + 1 to 3 fAD cycles
	Enabled open-circuit detection assist	42 ϕAD cycles + 1 to 3 fAD cycles
Between-execution process time		1 ϕAD cycle
End process time		2 or 3 fAD cycles

29.3.3 A/D Conversion Start Condition

A software trigger, trigger from timer RD or timer RC, and external trigger are used as A/D conversion start triggers.
Figure 29.4 shows the Block Diagram of A/D Conversion Start Control Unit.

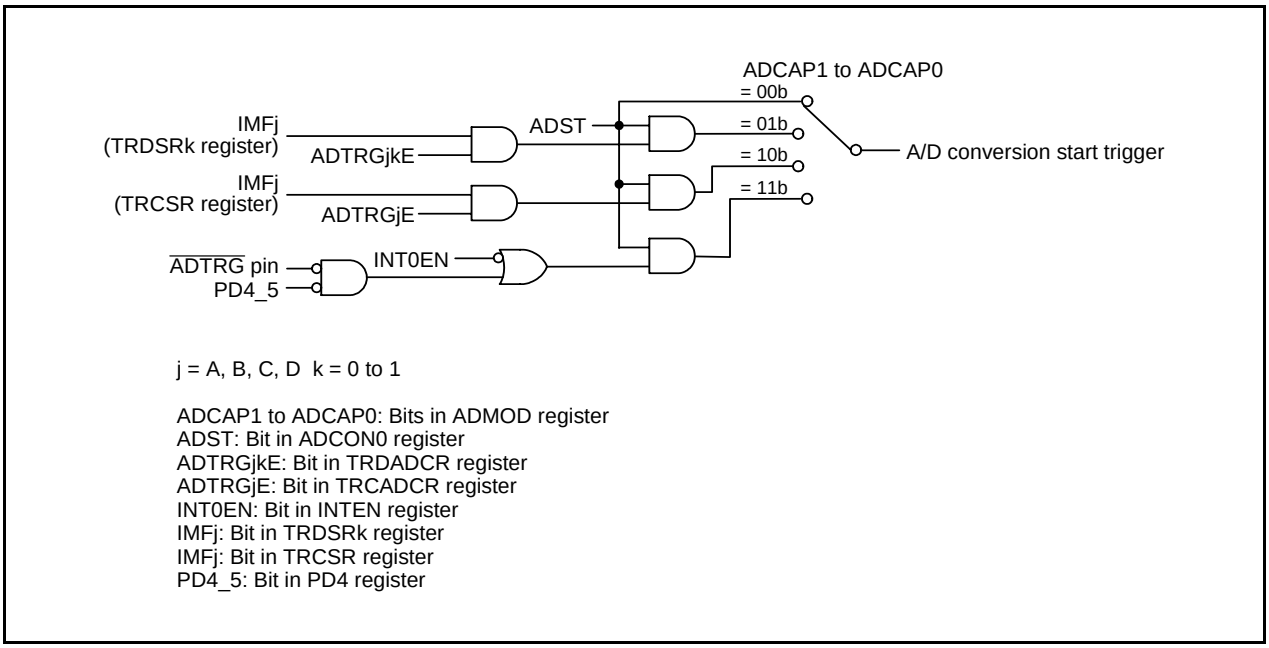


Figure 29.4 Block Diagram of A/D Conversion Start Control Unit

29.3.3.1 Software Trigger

A software trigger is selected when bits ADCAP1 to ADCAP0 in the ADMOD register are set to 00b (software trigger).
The A/D conversion starts when the ADST bit in the ADCON0 register is set to 1 (A/D conversion starts).

29.3.3.2 Trigger from Timer RD

This trigger is selected when bits ADCAP1 to ADCAP0 in the ADMOD register are set to 01b (timer RD).
To use this function, make sure the following conditions are met.

- Bits ADCAP1 to ADCAP0 in the ADMOD register are set to 01b (timer RD).
- Timer RD is used in the output compare function (timer mode, PWM mode, reset synchronous PWM mode, complementary PWM mode, and PWM3 mode).
- The ADTRGjkE bit (j = A, B, C, D, k = 0 or 1) in the TRDADCR register is set to 1 (A/D trigger occurs at compare match with TRDGRjk register).
- The ADST bit in the ADCON0 register is set to 1 (A/D conversion starts).

When the IMFj bit in the TRDSRk register is changed from 0 to 1, A/D conversion starts.
Refer to **20. Timer RD**, **20.4 Timer Mode (Output Compare Function)**, **20.5 PWM Mode**, **20.6 Reset Synchronous PWM Mode**, **20.7 Complementary PWM Mode**, **20.8 PWM3 Mode** for the details of timer RD and the output compare function (timer mode, PWM mode, reset synchronous PWM mode, complementary PWM mode, and PWM3 mode).

29.3.3.3 Trigger from Timer RC

This trigger is selected when bits ADCAP1 to ADCAP0 in the ADMOD register are set to 10b (timer RC).
To use this function, make sure the following conditions are met.

- Bits ADCAP1 to ADCAP0 in the ADMOD register are set to 10b (timer RC).
- Timer RC is used in the output compare function (timer mode, PWM mode, PWM2 mode).
- The ADTRGjE bit (j = A, B, C, D) in the TRCADCR register is set to 1 (A/D trigger occurs at compare match with TRCGRj register).
- The ADST bit in the ADCON0 register is set to 1 (A/D conversion starts).

When the IMFj bit in the TRCSR register is changed from 0 to 1, A/D conversion starts.
Refer to **19. Timer RC**, **19.5 Timer Mode (Output Compare Function)**, **19.6 PWM Mode**, **19.7 PWM2 Mode** for the details of timer RC and the output compare function (timer mode, PWM mode, and PWM2 mode).

29.3.3.4 External Trigger

This trigger is selected when bits ADCAP1 to ADCAP0 in the ADMOD register are set to 11b (external trigger ($\overline{\text{ADTRG}}$)).
To use this function, make sure the following conditions are met.

- Bits ADCAP1 to ADCAP0 in the ADMOD register are set to 11b (external trigger ($\overline{\text{ADTRG}}$)).
- Set the INT0EN bit in the INTEN register to 1 ($\overline{\text{INT0}}$ input enabled) and the INT0PL bit to 0 (one edge), and set the POL bit in the INT0IC register to 0 (falling edge selected).
- The PD4_5 bit in the PD4 register is set to 0 (input mode).
- Select the $\overline{\text{INT0}}$ digital filter by bits INT0F1 to INT0F0 in the INTF register.
- The ADST bit in the ADCON0 register is set to 1 (A/D conversion starts).

The IR bit in the INT0IC register is set to 1 (interrupt request) in accordance with the setting of the POL bit in the INT0IC register and the INT0PL bit in the INTEN register and a change in the $\overline{\text{ADTRG}}$ pin input (refer to **11.8 Notes on Interrupts**).
For details on interrupts, refer to **11. Interrupts**.

When the $\overline{\text{ADTRG}}$ pin input is changed from high to low under the above conditions, A/D conversion starts.

29.3.4 A/D Conversion Result

The A/D conversion result is stored in the ADi register (i = 0 to 7). The register where the result is stored varies depending on the A/D operating mode used. The contents of the ADi register are undefined after a reset. Values cannot be written to the ADi register.

In repeat mode 0, no interrupt request is generated. After the first AD conversion is completed, determine if the A/D conversion time has elapsed by a program.
In one-shot mode, repeat mode 1, single sweep mode, and repeat sweep mode, an interrupt request is generated at certain times, such as when an A/D conversion completes (the IR bit in the ADIC register is set to 1).
However, in repeat mode 1 and repeat sweep mode, A/D conversion continues after an interrupt request is generated. Read the ADi register before the next A/D conversion is completed, since at completion the ADi register is rewritten with the new value.

In one-shot mode and single sweep mode, when bits ADCAP1 to ADCAP0 in the ADMOD register is set to 00b (software trigger), the ADST bit in the ADCON0 register is used to determine whether the A/D conversion or sweep has completed.

During an A/D conversion operation, if the ADST bit in the ADCON0 register is set to 0 (A/D conversion stops) by a program to forcibly terminate A/D conversion, the conversion result of the A/D converter is undefined and no interrupt is generated. The value of the ADi register before A/D conversion may also be undefined.
If the ADST bit is set to 0 by a program, do not use the value of all the ADi register.

29.3.5 Low Current Consumption Function

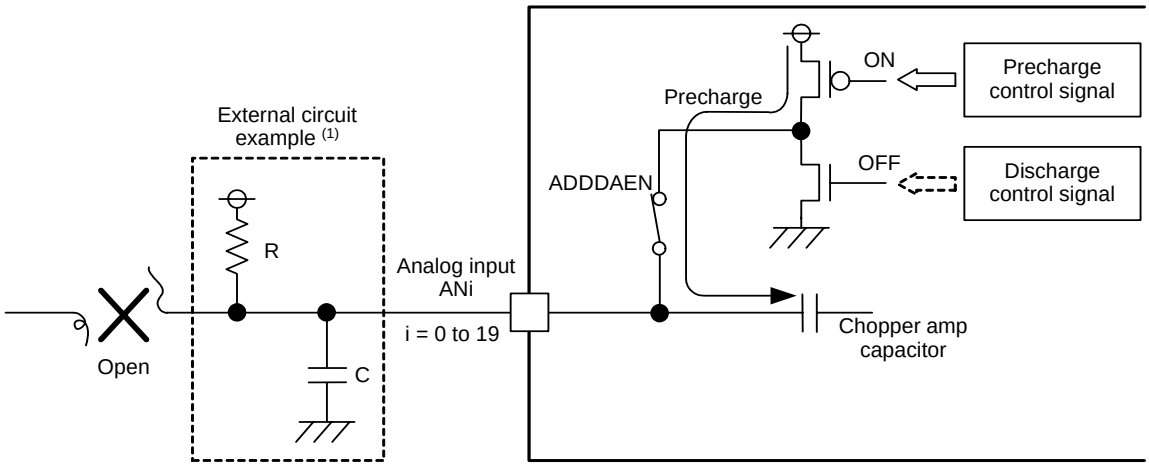
When the A/D converter is not used, power consumption can be reduced by setting the ADSTBY bit in the ADCON1 register to 0 (A/D operation stops (standby)) to shut off any analog circuit current flow.
To use the A/D converter, set the ADSTBY bit to 1 (A/D operation enabled) and wait for 1 ϕAD cycle or more before setting the ADST bit in the ADCON0 register to 1 (A/D conversion starts). Do not write 1 to bits ADST and ADSTBY at the same time.
Also, do not set the ADSTBY bit to 0 (A/D operation stops (standby)) during A/D conversion.

29.3.6 Extended Analog Input

In one-shot mode, repeat mode 0, and repeat mode 1, the on-chip reference voltage (OCVREF) can be used as analog input.
Any variation in VREF can be confirmed using the on-chip reference voltage. Use the ADEX0 bit in the ADCON1 register and the OCVREFAN bit in the OCVREFCR register to select the on-chip reference voltage.
The A/D conversion result of the on-chip reference voltage in one-shot mode or in repeat mode 0 is stored in the AD0 register.

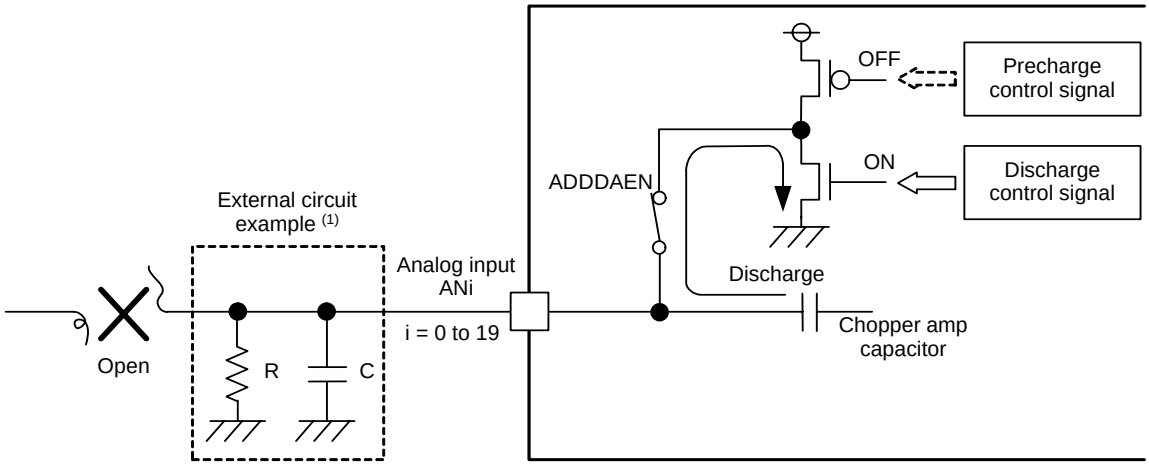
29.3.7 A/D Open-Circuit Detection Assist Function

To suppress influences of the analog input voltage leakage from the previously converted channel during A/D conversion operation, a function is incorporated to fix the electric charge on the chopper amp capacitor to the predetermined state (AVCC or GND) before starting conversion.
This function enables more reliable detection of an open circuit in the wiring connected to the analog input pins.
Figure 29.5 shows the A/D Open-Circuit Detection Example on AVCC Side (Precharge before Conversion Selected) and Figure 29.6 shows the A/D Open-Circuit Detection Example on AVSS Side (Discharge before Conversion Selected).



Note:
1. The conversion result for an open circuit varies with external circuits. Careful evaluation should be performed before using this function.

Figure 29.5 A/D Open-Circuit Detection Example on AVCC Side (Precharge before Conversion Selected)



Note:
1. The conversion result for an open circuit varies with external circuits. Careful evaluation should be performed before using this function.

Figure 29.6 A/D Open-Circuit Detection Example on AVSS Side (Discharge before Conversion Selected)

29.4 One-Shot Mode

In one-shot mode, the input voltage to one pin selected from among AN0 to AN19 or OCVREF is A/D converted once.
Table 29.4 lists the One-Shot Mode Specifications.

Table 29.4 One-Shot Mode Specifications

Item	Specification
Function	The input voltage to the pin selected by bits CH2 to CH0 and bits ADGSEL1 to ADGSEL0 in the ADINSEL register or the ADEX0 bit in the ADCON1 register is A/D converted once.
Resolution	8 bits or 10 bits
A/D conversion start condition	• Software trigger • Timer RD • Timer RC • External trigger (Refer to **29.3.3 A/D Conversion Start Condition)**
A/D conversion stop condition	• A/D conversion completes (If bits ADCAP1 to ADCAP0 in the ADMOD register are set to 00b (software trigger), the ADST bit in the ADCON0 register is set to 0.) • Set the ADST bit to 0
Interrupt request generation timing	When A/D conversion completes
Analog input pin	One pin selectable from among AN0 to AN19, or OCVREF.
Storage resister for A/D conversion result	AD0 register: AN0, AN8, AN12 OCVREF AD1 register: AN1, AN9, AN13 AD2 register: AN2, AN10, AN14 AD3 register: AN3, AN11, AN15 AD4 register: AN4, AN16 AD5 register: AN5, AN17 AD6 register: AN6, AN18 AD7 register: AN7, AN19
Reading of result of A/D converter	Read register AD0 to AD7 corresponding to the selected pin.

29.5 Repeat Mode 0

In repeat mode 0, the input voltage to one pin selected from among AN0 to AN19 or OCVREF is A/D converted repeatedly.
Table 29.5 lists the Repeat Mode 0 Specifications.

Table 29.5 Repeat Mode 0 Specifications

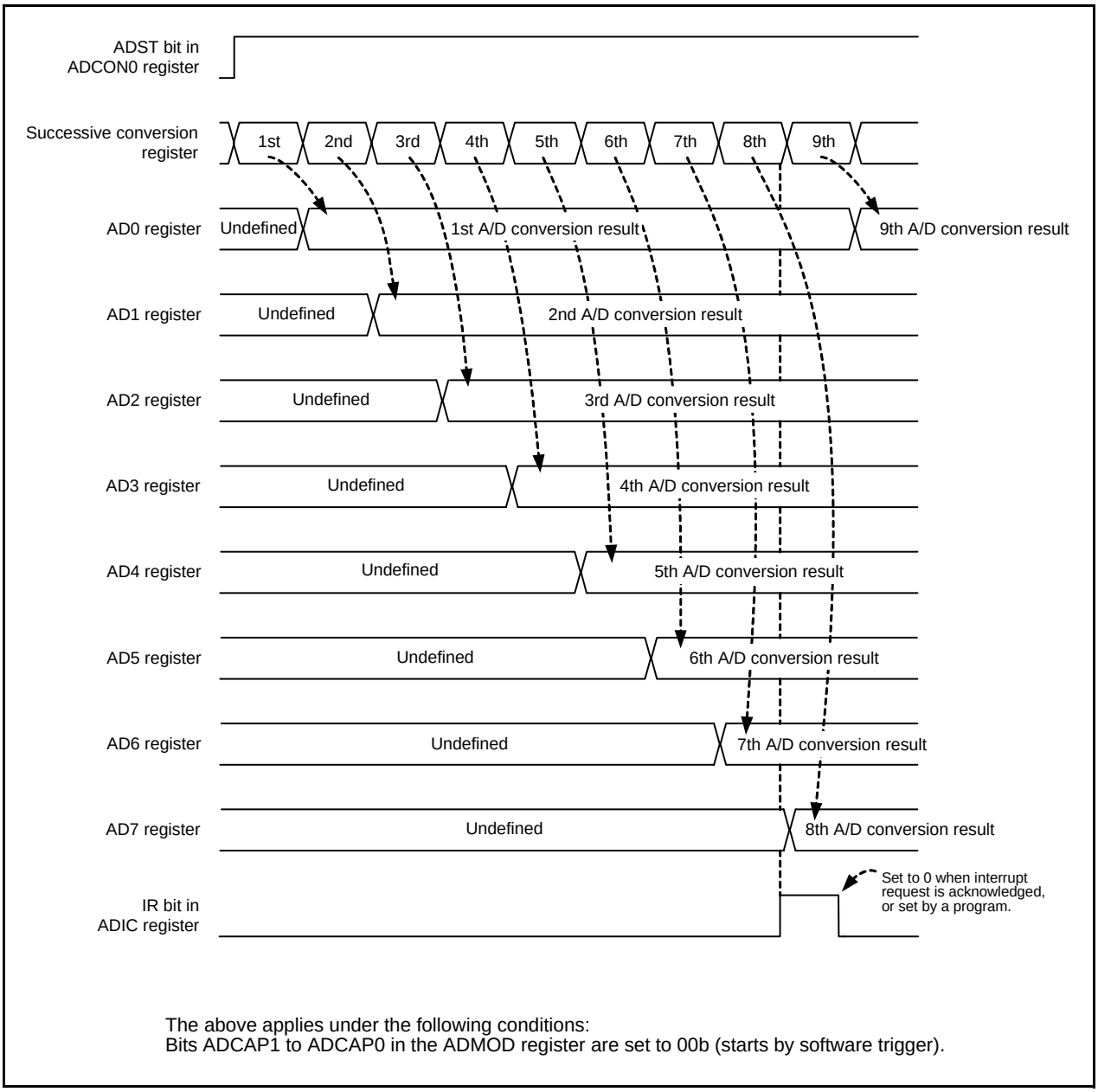
Item	Specification
Function	The input voltage to the pin selected by bits CH2 to CH0 and bits ADGSEL1 to ADGSEL0 in the ADINSEL register or the ADEX0 bit in the ADCON1 register is A/D converted repeatedly.
Resolution	8 bits or 10 bits
A/D conversion start condition	• Software trigger • Timer RD • Timer RC • External trigger (Refer to **29.3.3 A/D Conversion Start Condition)**
A/D conversion stop condition	Set the ADST bit in the ADCON0 register to 0
Interrupt request generation timing	Not generated
Analog input pin	One pin selectable from among AN0 to AN19, or OCVREF.
Storage resister for A/D conversion result	AD0 register: AN0, AN8, AN12 OCVREF AD1 register: AN1, AN9, AN13 AD2 register: AN2, AN10, AN14 AD3 register: AN3, AN11, AN15 AD4 register: AN4, AN16 AD5 register: AN5, AN17 AD6 register: AN6, AN18 AD7 register: AN7, AN19
Reading of result of A/D converter	Read register AD0 to AD7 corresponding to the selected pin.

29.6 Repeat Mode 1

In repeat mode 1, the input voltage to one pin selected from among AN0 to AN19 or OCVREF is A/D converted repeatedly.
Table 29.6 lists the Repeat Mode 1 Specifications. Figure 29.7 shows the Operating Example of Repeat Mode 1.

Table 29.6 Repeat Mode 1 Specifications

Item	Specification
Function	The input voltage to the pin selected by bits CH2 to CH0 and bits ADGSEL1 to ADGSEL0 in the ADINSEL register or the ADEX0 bit in the ADCON1 register is A/D converted repeatedly.
Resolution	8 bits or 10 bits
A/D conversion start condition	• Software trigger • Timer RD • Timer RC • External trigger (Refer to **29.3.3 A/D Conversion Start Condition)**
A/D conversion stop condition	Set the ADST bit in the ADCON0 register to 0
Interrupt request generation timing	When the A/D conversion result is stored in the AD7 register.
Analog input pin	One pin selectable from among AN0 to AN19, or OCVREF.
Storage resister for A/D conversion result	AD0 register: 1st A/D conversion result, 9th A/D conversion result... AD1 register: 2nd A/D conversion result, 10th A/D conversion result... AD2 register: 3rd A/D conversion result, 11th A/D conversion result... AD3 register: 4th A/D conversion result, 12th A/D conversion result... AD4 register: 5th A/D conversion result, 13th A/D conversion result... AD5 register: 6th A/D conversion result, 14th A/D conversion result... AD6 register: 7th A/D conversion result, 15th A/D conversion result... AD7 register: 8th A/D conversion result, 16th A/D conversion result...
Reading of result of A/D converter	Read registers AD0 to AD7



The above applies under the following conditions:
Bits ADCAP1 to ADCAP0 in the ADMOD register are set to 00b (starts by software trigger).

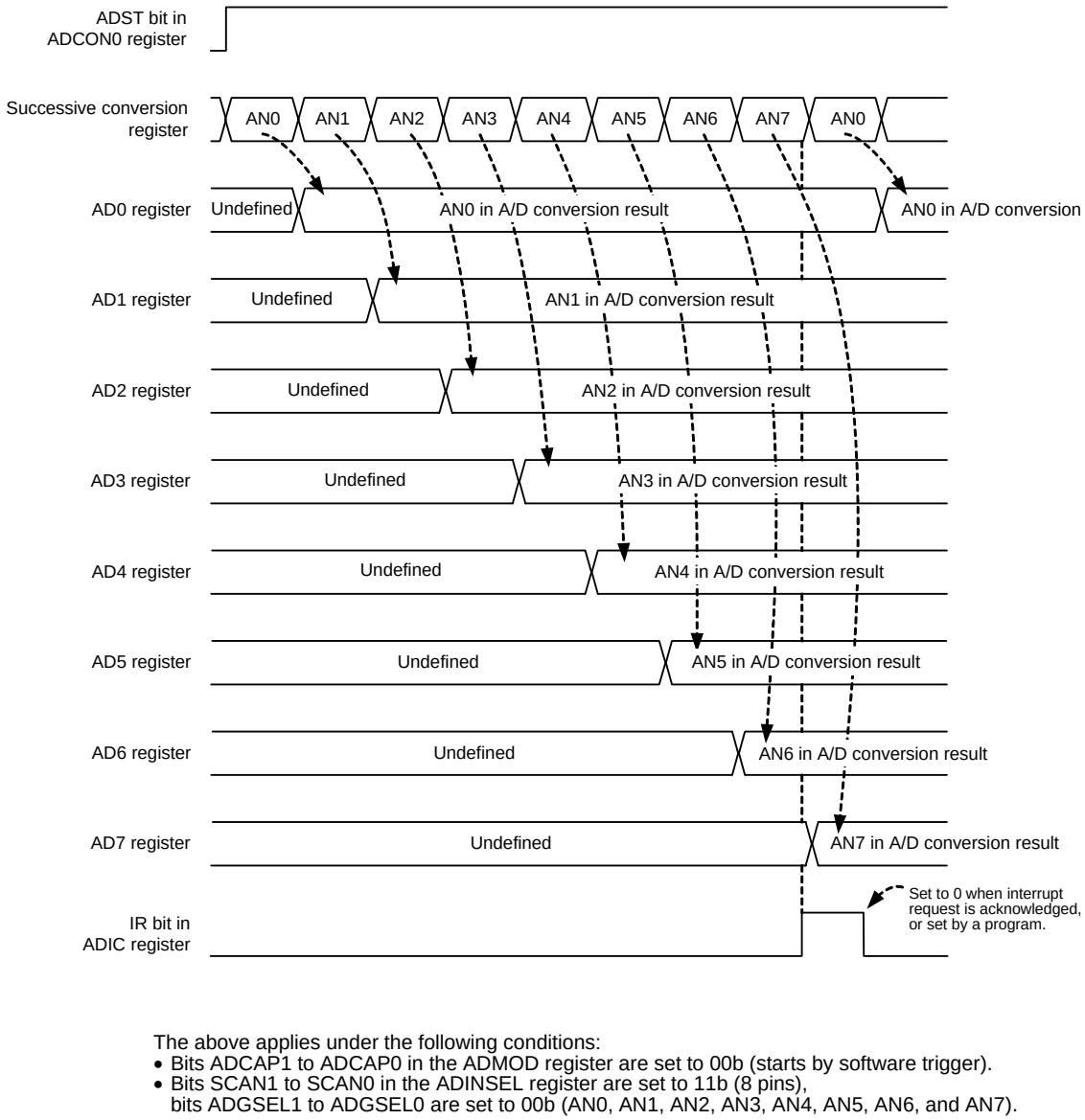
Figure 29.7 Operating Example of Repeat Mode 1

29.7 Single Sweep Mode

In single sweep mode, the input voltage to two, four, six, or eight pins selected from among AN0 to AN19 are A/D converted once.
Table 29.7 lists the Single Sweep Mode Specifications. Figure 29.8 shows the Operating Example of Single Sweep Mode.

Table 29.7 Single Sweep Mode Specifications

Item		Specification
Function		The input voltage to the pins selected by bits ADGSEL1 to ADGSEL0 and bits SCAN1 to SCAN0 in the ADINSEL register is A/D converted once.
Resolution		8 bits or 10 bits
A/D conversion start condition		• Software trigger • Timer RD • Timer RC • External trigger (Refer to **29.3.3 A/D Conversion Start Condition)**
A/D conversion stop condition	Software trigger	• If two pins are selected, when A/D conversion of the two selected pins completes (the ADST bit in the ADCON0 register is set to 0). • If four pins are selected, when A/D conversion of the four selected pins completes (the ADST bit is set to 0). • If six pins are selected, when A/D conversion of the six selected pins completes (the ADST bit is set to 0). • If eight pins are selected, when A/D conversion of the eight selected pins completes (the ADST bit is set to 0). • Set the ADST bit to 0.
	Timer RD	Set the ADST bit to 0.
	Timer RC	
	External trigger	
Interrupt request generation timing		• If two pins are selected, when A/D conversion of the two selected pins completes. • If four pins are selected, when A/D conversion of the four selected pins completes. • If six pins are selected, when A/D conversion of the six selected pins completes. • If eight pins are selected, when A/D conversion of the eight selected pins completes.
Analog input pin		AN0 to AN1(2 pins), AN8 to AN9(2 pins), AN12 to AN13(2 pins) AN0 to AN3(4 pins), AN8 to AN11(4 pins), AN12 to AN15(4 pins) AN0 to AN5(6 pins), AN12 to AN17(6 pins) AN0 to AN7(8 pins), AN12 to AN19(8 pins) (Selectable by bits SCAN1 to SCAN0 and bits ADGSEL1 to ADGSEL0.)
Storage resister for A/D conversion result		AD0 register: AN0, AN8, AN12 AD1 register: AN1, AN9, AN13 AD2 register: AN2, AN10, AN14 AD3 register: AN3, AN11, AN15 AD4 register: AN4, AN16 AD5 register: AN5, AN17 AD6 register: AN6, AN18 AD7 register: AN7, AN19
Reading of result of A/D converter		Read the registers from AD0 to AD7 corresponding to the selected pin.



The above applies under the following conditions:
- Bits ADCAP1 to ADCAP0 in the ADMOD register are set to 00b (starts by software trigger).
- Bits SCAN1 to SCAN0 in the ADINSEL register are set to 11b (8 pins), bits ADGSEL1 to ADGSEL0 are set to 00b (AN0, AN1, AN2, AN3, AN4, AN5, AN6, and AN7).

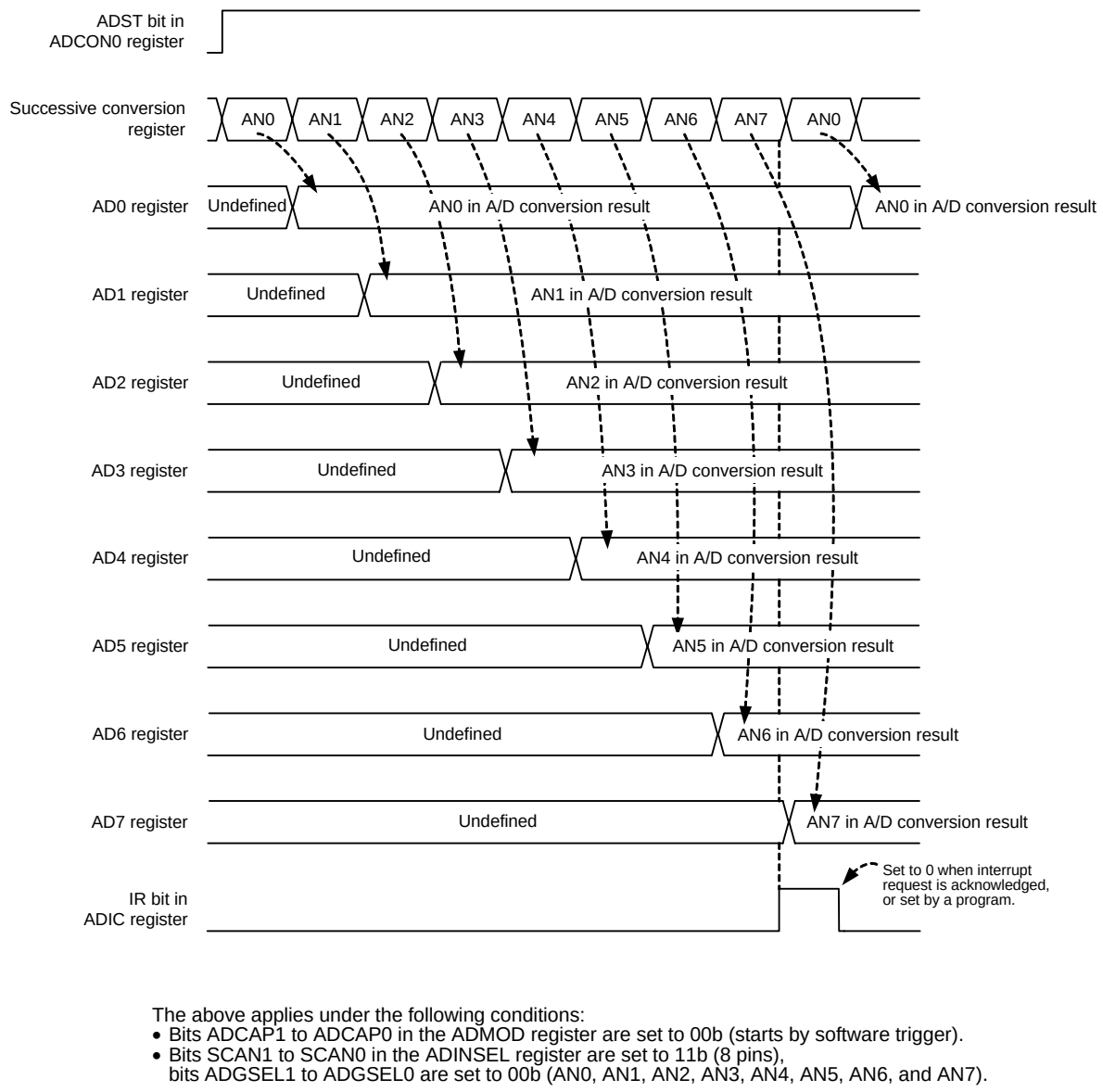
Figure 29.8 Operating Example of Single Sweep Mode

29.8 Repeat Sweep Mode

In repeat sweep mode, the input voltage to two, four, six, or eight pins selected from among AN0 to AN19 are A/D converted repeatedly.
Table 29.8 lists the Repeat Sweep Mode Specifications. Figure 29.9 shows the Operating Example of Repeat Sweep Mode.

Table 29.8 Repeat Sweep Mode Specifications

Item	Specification
Function	The input voltage to the pins selected by bits ADGSEL1 to ADGSEL0 and bits SCAN1 to SCAN0 in the ADINSEL register are A/D converted repeatedly.
Resolution	8 bits or 10 bits
A/D conversion start condition	• Software trigger • Timer RD • Timer RC • External trigger (Refer to **29.3.3 A/D Conversion Start Condition)**
A/D conversion stop condition	Set the ADST bit in the ADCON0 register to 0
Interrupt request generation timing	• If two pins are selected, when A/D conversion of the two selected pins completes. • If four pins are selected, when A/D conversion of the four selected pins completes. • If six pins are selected, when A/D conversion of the six selected pins completes. • If eight pins are selected, when A/D conversion of the eight selected pins completes.
Analog input pin	AN0 to AN1(2 pins), AN8 to AN9(2 pins), AN12 to AN13(2 pins) AN0 to AN3(4 pins), AN8 to AN11(4 pins), AN12 to AN15(4 pins) AN0 to AN5(6 pins), AN12 to AN17(6 pins) AN0 to AN7(8 pins), AN12 to AN19(8 pins) (Selectable by bits SCAN1 to SCAN0 and bits ADGSEL1 to ADGSEL0.)
Storage resister for A/D conversion result	AD0 register: AN0, AN8, AN12 AD1 register: AN1, AN9, AN13 AD2 register: AN2, AN10, AN14 AD3 register: AN3, AN11, AN15 AD4 register: AN4, AN16 AD5 register: AN5, AN17 AD6 register: AN6, AN18 AD7 register: AN7, AN19
Reading of result of A/D converter	Read the registers from AD0 to AD7 corresponding to the selected pin.



The above applies under the following conditions:
- Bits ADCAP1 to ADCAP0 in the ADMOD register are set to 00b (starts by software trigger).
- Bits SCAN1 to SCAN0 in the ADINSEL register are set to 11b (8 pins), bits ADGSEL1 to ADGSEL0 are set to 00b (AN0, AN1, AN2, AN3, AN4, AN5, AN6, and AN7).

Figure 29.9 Operating Example of Repeat Sweep Mode

29.9 Output Impedance of Sensor under A/D Conversion

To carry out A/D conversion properly, charging the internal capacitor C shown in Figure 29.10 has to be completed within a specified period of time. T (sampling time) as the specified time. Let output impedance of sensor equivalent circuit be R0, internal resistance of microcomputer be R, precision (error) of the A/D converter be X, and the resolution of A/D converter be Y (Y is 1024 in the 10-bit mode, and 256 in the 8-bit mode).

VC is generally $VC = VIN\left\{1 - e^{-\frac{1}{C(R0+R)}t}\right\}$

And when t = T, $VC = VIN - \frac{X}{Y}VIN = VIN\left(1 - \frac{X}{Y}\right)$

$$e^{-\frac{1}{C(R0+R)}T} = \frac{X}{Y}$$

$$-\frac{1}{C(R0+R)}T = \ln\frac{X}{Y}$$

Hence, $R0 = -\frac{T}{C \bullet \ln\frac{X}{Y}} - R$

Figure 29.10 shows the Analog Input Pin and External Sensor Equivalent Circuit. When the difference between VIN and VC becomes 0.1LSB, we find impedance R0 when voltage between pins VC changes from 0 to VIN-(0.1/1024) VIN in time T. (0.1/1024) means that A/D precision drop due to insufficient capacitor charge is held to 0.1LSB at time of A/D conversion in the 10-bit mode. Actual error however is the value of absolute precision added to 0.1LSB.
T = 0.8 µs when ϕAD = 20 MHz. Output impedance R0 for sufficiently charging capacitor C within time T is determined as follows.

T = 0.8 µs, R = 10 kΩ, C = 6.0 pF, X = 0.1, and Y = 1024. Hence,

$$R0 = -\frac{0.8 \times 10^{-6}}{6.0 \times 10^{-12} \bullet \ln\frac{0.1}{1024}} - 10 \times 10^{3} \approx 4.4 \times 10^{3}$$

Thus, the allowable output impedance of the sensor equivalent circuit, making the precision (error) 0.1LSB or less, is approximately 4.4 kΩ maximum.

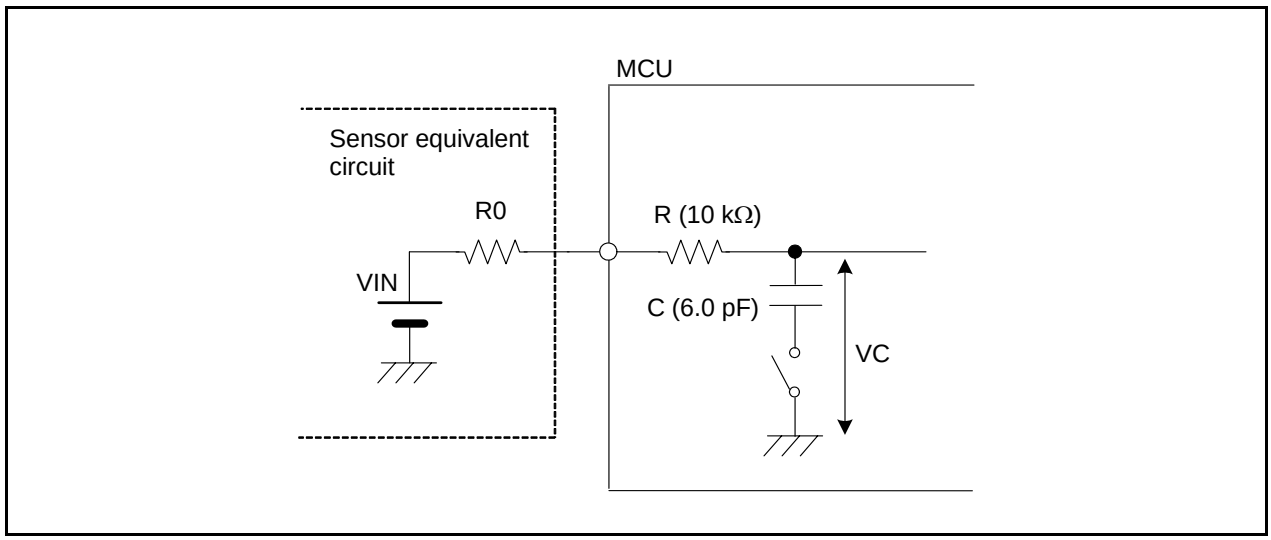


Figure 29.10 Analog Input Pin and External Sensor Equivalent Circuit

29.10 Notes on A/D Converter

- Write to the ADMOD register, the ADINSEL register, the ADCON0 register (other than ADST bit), the ADCON1 register, the OCVREFCR register when A/D conversion is stopped (before a trigger occurs).
- To use the A/D converter in repeat mode 0, repeat mode 1, or repeat sweep mode, select the frequency of the A/D converter operating clock ϕAD or more for the CPU clock during A/D conversion.
  Do not select fOCO-F as ϕAD.
- Connect 0.1 μF capacitor between the VREF pin and AVSS pin.
- Do not enter stop mode during A/D conversion.
- Do not enter wait mode during A/D conversion regardless of the state of the CM02 bit in the CM0 register (1: Peripheral function clock stops in wait mode or 0: Peripheral function clock does not stop in wait mode).
- Do not set the FMSTP bit in the FMR0 register to 1 (flash memory stops) or the FMR27 bit to 1 (low-consumption-current read mode enabled) during A/D conversion. Otherwise, the A/D conversion result will be undefined.
- Do not change the CKS2 bit in the ADMOD register while fOCO-F is stopped.
- During an A/D conversion operation, if the ADST bit in the ADCON0 register is set to 0 (A/D conversion stops) by a program to forcibly terminate A/D conversion, the conversion result of the A/D converter is undefined and no interrupt is generated. The value of the ADi register before A/D conversion may also be undefined.
  If the ADST bit is set to 0 by a program, do not use the value of all the ADi register.

30. Flash Memory

The flash memory can perform in the following three rewrite modes: CPU rewrite mode, standard serial I/O mode, and parallel I/O mode.

30.1 Overview

Table 30.1 lists the Flash Memory Version Performance (R8C/38W Group, R8C/38Y Group) (Refer to **Table 1.1** and **Table 1.2 Specifications for R8C/38W Group** and **Table 1.3** and **Table 1.4 Specifications for R8C/38X Group** and **Table 1.5** and **Table 1.6 Specifications for R8C/38Y Group** and **Table 1.7** and **Table 1.8 Specifications for R8C/38Z Group**, for the items other than listed in Table 30.1).
The R8C/38W Group and the R8C/38Y Group have data flash (1 KB × 4 blocks) with the background operation (BGO) function.

Table 30.1 Flash Memory Version Performance (R8C/38W Group, R8C/38Y Group)

Item		Specification
Flash memory operating mode		3 modes (CPU rewrite, standard serial I/O, and parallel I/O)
Division of erase blocks		Refer to **Figure 30.1**.
Programming method		Byte units or word units (program ROM only)
Erasure method		Block erase
Programming and erasure control method (1)		Program and erase control by software commands
Rewrite control method	Blocks 0 to 8 (3) (Program ROM)	Rewrite protect control in block units by the lock bit
	Blocks A, B, C, and D (Data flash)	Individual rewrite protect control on blocks A, B, C, and D by bits FMR14, FMR15, FMR16, and FMR17 in the FMR1 register
Number of commands		7 commands
Programming and erasure endurance (2)	Blocks 0 to 8 (3) (Program ROM)	1,000 times
	Blocks A, B, C, and D (Data flash)	10,000 times
ID code check function		Standard serial I/O mode supported
ROM code protection		Parallel I/O mode supported

Notes:
1. To perform programming and erasure, use VCC = 2.7 V to 5.5 V as the supply voltage. Do not perform programming and erasure at less than 2.7 V.
2. Definition of programming and erasure endurance
   The programming and erasure endurance is defined on a per-block basis. If the programming and erasure endurance is n (n = 1,000 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1-Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. When performing 100 or more rewrites, the actual erase count can be reduced by executing program operations in such a way that all blank areas are used before performing an erase operation. Avoid rewriting only particular blocks and try to average out the programming and erasure endurance of the blocks. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
3. The number of blocks and block division vary with the MCU. Refer to **Figure 30.1 Flash Memory Block Diagram of this MCU** for details.

Table 30.2 Flash Memory Version Performance (R8C/38X Group, R8C/38Z Group)

Item		Specification
Flash memory operating mode		3 modes (CPU rewrite, standard serial I/O, and parallel I/O)
Division of erase blocks		Refer to **Figure 30.1**.
Programming method		Byte units or word units
Erasure method		Block erase
Programming and erasure control method (1)		Program and erase control by software commands
Rewrite control method	Blocks 0 to 8 (3) (Program ROM)	Rewrite protect control in block units by the lock bit
Number of commands		7 commands
Programming and erasure endurance (2)	Blocks 0 to 8 (3) (Program ROM)	100 times
ID code check function		Standard serial I/O mode supported
ROM code protection		Parallel I/O mode supported

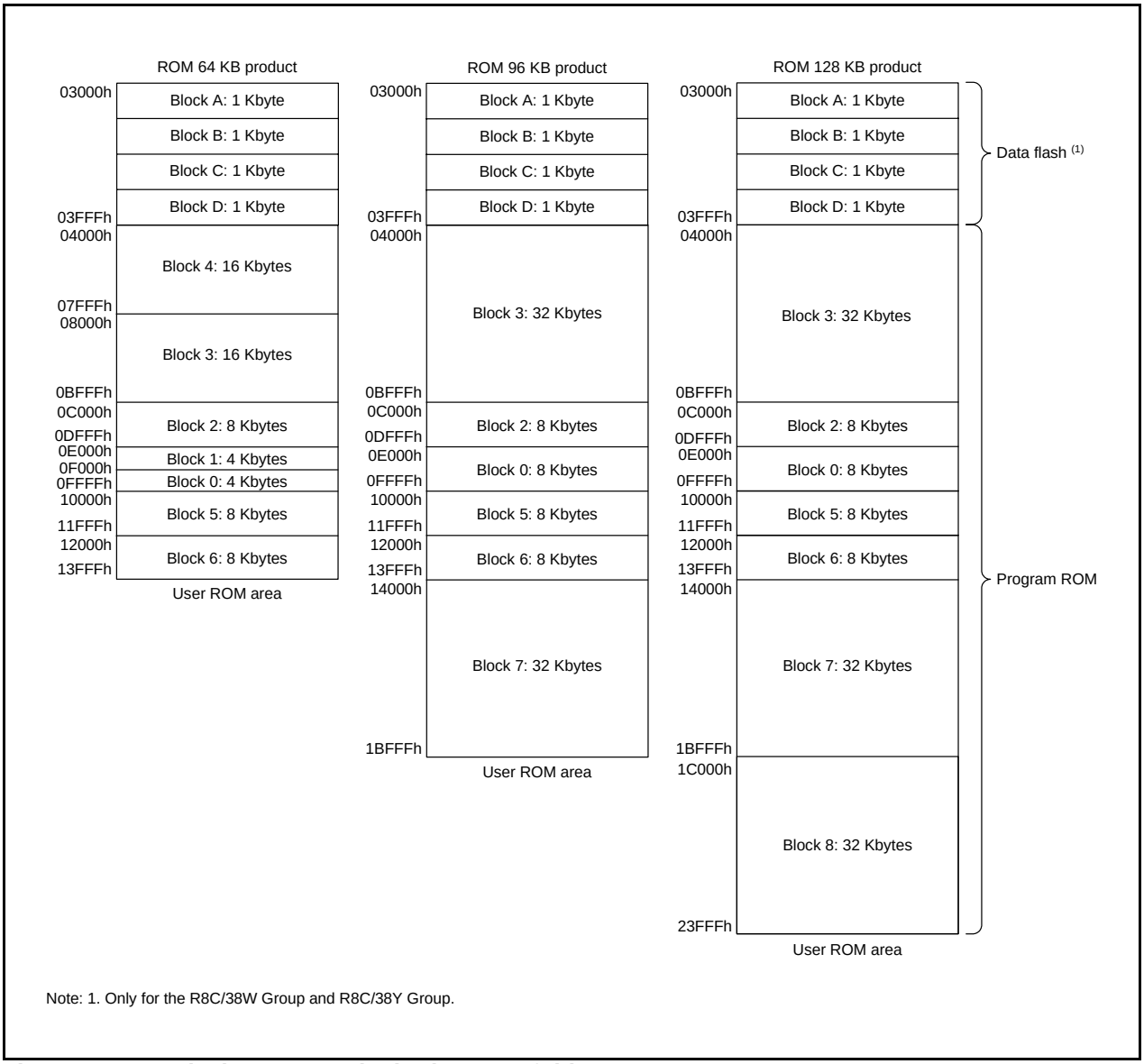
Notes:
1. To perform programming and erasure, use VCC = 2.7 V to 5.5 V as the supply voltage. Do not perform programming and erasure at less than 2.7 V.
2. Definition of programming and erasure endurance
   The programming and erasure endurance is defined on a per-block basis. If the programming and erasure endurance is 100, each block can be erased 100 times. For example, if 4,096 1-byte writes are performed to different addresses in block, a 4-Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. The actual erase count can be reduced by executing program operations in such a way that all blank areas are used before performing an erase operation. Avoid rewriting only particular blocks and try to average out the programming and erasure endurance of the blocks. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
3. The number of blocks and block division vary with the MCU. Refer to **Figure 30.1 Flash Memory Block Diagram of this MCU** for details.

Table 30.3 Flash Memory Rewrite Mode

Flash Memory Rewrite Mode	CPU Rewrite Mode	Standard Serial I/O Mode	Parallel I/O Mode
Function	User ROM area is rewritten by executing software commands from the CPU.	User ROM area is rewritten using a dedicated serial programmer.	User ROM area is rewritten using a dedicated parallel programmer.
Rewritable area	User ROM	User ROM	User ROM
Rewrite programs	User program	Standard boot program	–

30.2 Memory Map

The flash memory contains a user ROM area and a boot ROM area (reserved area).
Figure 30.1 shows the Flash Memory Block Diagram of this MCU.
The user ROM area contains program ROM and data flash (only for R8C/38W Group and R8C/38Y Group).
Program ROM: Flash memory mainly used for storing programs
Data flash: Flash memory mainly used for storing data to be rewritten
The user ROM area is divided into several blocks. The user ROM area can be rewritten in CPU rewrite mode, standard serial I/O mode, or parallel I/O mode.
The rewrite control program (standard boot program) for standard serial I/O mode is stored in the boot ROM area before shipment. The boot ROM area is allocated separately from the user ROM area.



Note: 1. Only for the R8C/38W Group and R8C/38Y Group.

Figure 30.1 Flash Memory Block Diagram of this MCU

30.3 Functions to Prevent Flash Memory from being Rewritten

Standard serial I/O mode has an ID code check function, and parallel I/O mode has a ROM code protect function to prevent the flash memory from being read or rewritten easily.

30.3.1 ID Code Check Function

The ID code check function is used in standard serial I/O mode. Unless 3 bytes (addresses 0FFFCh to 0FFFEh) of the reset vector are set to FFFFFFh, the ID codes sent from the serial programmer or the on-chip debugging emulator and the 7-byte ID codes written in the flash memory are checked to see if they match. If the ID codes do not match, the commands sent from the serial programmer or the on-chip debugging emulator are not accepted. For details of the ID code check function, refer to **12. ID Code Areas**.

30.3.2 ROM Code Protect Function

The ROM protect function prevents the contents of the flash memory from being read, rewritten, or erased using the OFS register in parallel I/O mode.
Refer to **13. Option Function Select Area** for details of the option function select area.

The ROM code protect function is enabled by writing 1 to the ROMCR bit and writing 0 to the ROMCP1 bit. This prevents the contents of the on-chip flash memory from being read or rewritten.
Once ROM code protection is enabled, the content of the internal flash memory cannot be rewritten in parallel I/O mode. To disable ROM code protection, erase the block including the OFS register using CPU rewrite mode or standard serial I/O mode.

30.3.3 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	—	—	ROMCP1	ROMCR	—	WDTON
After Reset	User Setting Value (Note 1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset. 1: Watchdog timer is stopped after reset.	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	—	Reserved bits	Set to 1.	R/W
b5	—			
b6	LVDAS	Voltage detection 0 circuit start bit (2)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protect mode enabled after reset 1: Count source protect mode disabled after reset	R/W

Notes:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS register. If the block including the OFS register is erased, the OFS register is set to FFh.
   When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.
2. To use power-on reset and voltage monitor 0 reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

For a setting example of the OFS register, refer to **13.3.1 Setting Example of Option Function Select Area**.

30.4 CPU Rewrite Mode

In CPU rewrite mode, the user ROM area can be rewritten by executing software commands from the CPU. Therefore, the user ROM area can be rewritten directly while the MCU is mounted on a board without using a ROM programmer. Execute the software command only to blocks in the user ROM area.
The flash module has an erase-suspend function which halts the erase operation temporarily during an erase operation in CPU rewrite mode. During erase-suspend, the flash memory can be read or programmed.
Erase-write 0 mode (EW0 mode) and erase-write 1 mode (EW1 mode) are available in CPU rewrite mode.
Table 30.4 lists the Differences between EW0 Mode and EW1 Mode.

Table 30.4 Differences between EW0 Mode and EW1 Mode

Item	EW0 Mode	EW1 Mode
Operating mode	Single-chip mode	Single-chip mode
Rewrite control program allocatable area	User ROM	User ROM
Rewrite control program executable areas (1)	RAM (The rewrite control program must be transferred before being executed.) However, the program can be executed in the program ROM area when rewriting the data flash area.	User ROM or RAM
Rewritable area	User ROM	User ROM However, blocks which contain the rewrite control program are excluded.
Software command restrictions (1)	—	Program and block erase commands cannot be executed to any block which contains the rewrite control program.
Mode after programming or block erasure or after entering erase-suspend	Read array mode	Read array mode
CPU and DTC state during programming and block erasure (1)	The CPU operates.	• The CPU or DTC operates while the data flash area is being programmed or block erased. • The CPU or DTC is put in a hold state while the program ROM area is being programmed or block erased. (I/O ports retain the state before the command execution).
Flash memory status detection	Read bits FST7, FMT5, and FMT4 in the FST register by a program.	Read bits FST7, FMT5, and FMT4 in the FST register by a program.
Conditions for entering erase-suspend (1)	• Set bits FMR20 and FMR21 in the FMR2 register to 1 by a program. • Set bits FMR20 and FMR22 in the FMR2 register to 1 and the enabled maskable interrupt is generated.	• Set bits FMR20 and FMR21 in the FMR2 register to 1 by a program (while rewriting the data flash area). • Set bits FMR20 and FMR22 in the FMR2 register to 1 and the enabled maskable interrupt is generated.
CPU clock	Max. 20 MHz	Max. 20 MHz

Note:
1. The R8C/38W Group and R8C/38Y Group have data flash.

30.4.1 Flash Memory Status Register (FST)

Address 01B2h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	FST7	FST6	FST5	FST4	—	LBDATA	BSYAEI	RDYSTI
After Reset	1	0	0	0	0	X	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	RDYSTI	Flash ready status interrupt request flag (1, 4)	0: No flash ready status interrupt request 1: Flash ready status interrupt request	R/W
b1	BSYAEI	Flash access error interrupt request flag (2, 4)	0: No flash access error interrupt request 1: Flash access error interrupt request	R/W
b2	LBDATA	LBDATA monitor flag	0: Locked 1: Not locked	R
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	FST4	Program error flag (3)	0: No program error 1: Program error	R
b5	FST5	Erase error/blank check error flag (3)	0: No erase error/blank check error 1: Erase error/blank check error	R
b6	FST6	Erase-suspend status flag	0: Other than erase-suspend 1: During erase-suspend	R
b7	FST7	Ready/busy status flag	0: Busy 1: Ready	R

Notes:
1. The RDYSTI bit cannot be set to 1 (flash ready status interrupt request) by a program.
   When writing 0 (no flash ready status interrupt request) to the RDYSTI bit, read this bit (dummy read) before writing to it.
   Make sure the DTC is not activated by the flash ready status source between reading and writing.
   To confirm this bit, set the RDYSTIE bit in the FMR0 register to 1 (flash ready status interrupt enabled).
2. The BSYAEI bit cannot be set to 1 (flash access error interrupt request) by a program.
   When writing 0 (no flash access error interrupt request) to the BSYAEI bit, read this bit (dummy read) before writing to it.
   To confirm this bit, set the BSYAEIE bit in the FMR0 register to 1 (flash access error interrupt enabled) or set the CMDERIE bit in the FMR0 register to 1 (erase/write error interrupt enabled).
3. This bit is also set to 1 (error) when a command error occurs.
4. When this bit is set to 1, do not set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled).

RDYSTI Bit (Flash Ready Status Flag Interrupt Request Flag)

When the RDYSTIE bit in the FMR0 register is set to 1 (flash ready status interrupt enabled) and auto-programming or auto-erasure completes, or erase-suspend mode is entered, the RDYSTI bit is set to 1 (flash ready status interrupt request).
During interrupt handling, set the RDYSTI bit to 0 (no flash ready status interrupt request).

[Condition for setting to 0]
Set to 0 by an interrupt handling program.
[Condition for setting to 1]
When the flash memory status changes from busy to ready while the RDYSTIE bit in the FRMR0 register is set to 1, the RDYSTI bit is set to 1.
The status is changed from busy to ready in the following states:

- Completion of erasing/programming the flash memory
- Suspend acknowledgement
- Completion of forcible termination
- Completion of the lock bit program
- Completion of the read lock bit status
- Completion of the block blank check
- When the flash memory can be read after it has been stopped.

BSYAEI Bit (Flash Access Error Interrupt Request Flag)

The BYSAEI bit is set to 1 (flash access error interrupt request) when the BSYAEIE bit in the FMR0 register is set to 1 (flash access error interrupt enabled) and the block during auto-programming/auto-erasure is accessed. This bit is also set to 1 if an erase or program error occurs when the CMDERIE bit in the FMR0 register is set to 1 (erase/write error interrupt enabled).
During interrupt handling, set the BSYAEI bit to 0 (no flash access error interrupt request).

[Conditions for setting to 0]
(1) Set to 0 by an interrupt handling program.
(2) Execute the clear status register command.
[Conditions for setting to 1]
(1) Read or write the area that is being erased/written when the BSYAEIE bit in the FRMR0 register is set to 1 and while the flash memory is busy.
Or, read the data flash area (only for R8C/38W Group and R8C/38Y Group) while erasing/writing to the program ROM area. (Note that the read value is undefined in both cases. Writing has no effect.)
(2) If a command sequence error, erase error, blank check error, or program error occurs when the CMDERIE bit in the FMR0 register is set to 1 (erase/write error interrupt enabled).

LBDATA Bit (LBDATA Monitor Flag)

This is a read-only bit indicating the lock bit status. To confirm the lock bit status, execute the read lock bit status command and read the LBDATA bit after the FST7 bit is set to 1 (ready).
The condition for updating this bit is when the program, erase, read lock bit status commands are generated.
When the read lock bit status command is input, the FST7 bit is set to 0 (busy). At the time when the FST7 bit is set to 1 (ready), the lock bit status is stored in the LBDATA bit. The data in the LBDATA bit is retained until the next command is input.

FST4 Bit (Program Error Flag)

This is a read-only bit indicating the auto-programming status. The bit is set to 1 if a program error occurs; otherwise, it is set to 0. For details, refer to the description in **30.4.14 Full Status Check**.

FST5 Bit (Erase Error/blank check error Flag)

This is a read-only bit indicating the status of auto-programming or the block blank check command. The bit is set to 1 if an erase error or blank check error occurs; otherwise, it is set to 0. Refer to **30.4.14 Full Status Check** for details.

FST6 Bit (Erase Suspend Status Flag)

This is a read-only bit indicating the suspend status. The bit is set to 1 when an erase-suspend request is acknowledged and a suspend status is entered; otherwise, it is set to 0.

FST7 Bit (Ready/Busy Status Flag)

When the FST7 bit is set to 0 (busy), the flash memory is in one of the following states:

- During programming
- During erasure
- During the lock bit program
- During the read lock bit status
- During the block blank check
- During forced stop operation
- The flash memory is being stopped
- The flash memory is being activated

Otherwise, the FST7 bit is set to 1 (ready).

30.4.2 Flash Memory Control Register 0 (FMR0)

Address 01B4h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	RDYSTIE	BSYAEIE	CMDERIE	CMDRST	FMSTP	FMR02	FMR01	FMR00
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FMR00	Program unit select bit (1, 5)	0: Byte units 1: Word units	R/W
b1	FMR01	CPU rewrite mode select bit (1, 4)	0: CPU rewrite mode disabled 1: CPU rewrite mode enabled	R/W
b2	FMR02	EW1 mode select bit (1)	0: EW0 mode 1: EW1 mode	R/W
b3	FMSTP	Flash memory stop bit (2)	0: Flash memory operates 1: Flash memory stops (Low-power consumption state, flash memory initialization)	R/W
b4	CMDRST	Erase/write sequence reset bit (3)	When the CMDRST bit is set to 1, the erase/write sequence is reset and erasure/writing can be forcibly stopped. When read, the content is 0.	R/W
b5	CMDERIE	Erase/write error interrupt enable bit	0: Erase/write error interrupt disabled 1: Erase/write error interrupt enabled	R/W
b6	BSYAEIE	Flash access error interrupt enable bit	0: Flash access error interrupt disabled 1: Flash access error interrupt enabled	R/W
b7	RDYSTIE	Flash ready status interrupt enable bit	0: Flash ready status interrupt disabled 1: Flash ready status interrupt enabled	R/W

Notes:
1. To set this bit to 1, first write 0 and then 1 immediately. Disable interrupts and DTC activation between writing 0 and writing 1.
2. Write to the FMSTP bit by a program transferred to the RAM. The FMSTP bit is enabled when the FMR01 bit is set to 1 (CPU rewrite mode enabled). To set the FMSTP bit to 1 (flash memory stops), set it when the FST7 bit in the FST register is set to 1 (ready).
3. The CMDRST bit is enabled when the FMR01 bit is set to 1 (CPU rewrite mode enabled) and the FST7 bit in the FST register is set to 0 (busy).
4. To set the FMR01 bit to 0 (CPU rewrite mode disabled), set it when the RDYSTI bit in the FST register is set to 0 (no flash ready status interrupt request) and the BSYAEI bit is set to 0 (no flash access error interrupt request).
5. Valid for the program ROM area only.

FMR00 bit (program unit selection bit)

The program unit to program ROM area can be selected from 8-bit (byte) units or 16-bit (word) units. When this bit is set to 1 (word units), use the word command for writing the software command.

FMR01 Bit (CPU Rewrite Mode Select Bit)

When the FMR01 bit is set to 1 (CPU rewrite mode enabled), the MCU is made ready to accept software commands.

FMR02 Bit (EW1 Mode Select Bit)

When the FMR02 bit is set to 1 (EW1 mode), EW1 mode is selected.

FMSTP Bit (Flash Memory Stop Bit)

This bit is used to initialize the flash memory control circuits, and also to reduce the amount of current consumed by the flash memory. Access to the flash memory is disabled by setting the FMSTP bit to 1.
Write to the FMSTP bit by a program transferred to the RAM.
To reduce the power consumption further in high-speed on-chip oscillator mode, low-speed on-chip oscillator mode (XIN clock stopped), and low-speed clock mode (XIN clock stopped), set the FMSTP bit to 1. Refer to **31.2.10 Stopping Flash Memory** for details.
When entering stop mode or wait mode while CPU rewrite mode is disabled, the FMR0 register does not need to be set because the power for the flash memory is automatically turned off and is turned back on when exiting stop or wait mode.
When the FMSTP bit is set to 1 (including during the busy status (the period while the FST7 bit is 0) immediately after the FMSTP bit is changed from 1 to 0), do not set to low-consumption-current read mode at the same time.

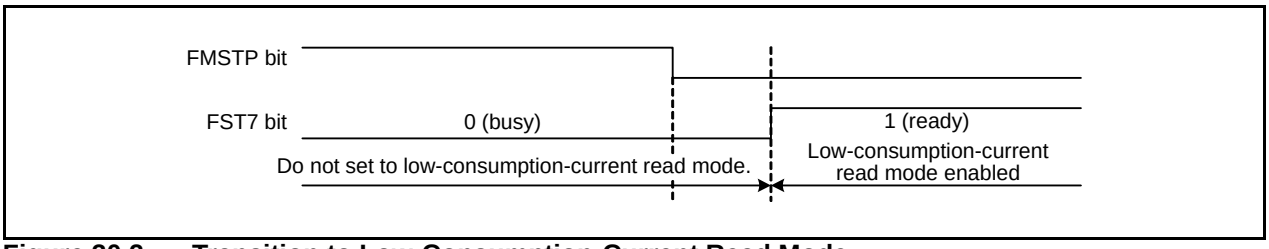


Figure 30.2 Transition to Low-Consumption-Current Read Mode

CMDRST Bit (Erase/Write Sequence Reset Bit)

This bit is used to initialize the flash memory sequence and forcibly stop a program or erase command. The program ROM area can be read when resetting the sequence of programming/erasing the data flash area.
If the program or erase command is forcibly stopped using the CMDRST bit in the FMR0 register, execute the clear status register command after the FST7 bit in the FST register is changed to 1 (ready). To program to the same address again, execute the block erase command again and ensure it has been completed normally before programming. If the addresses and blocks which the program or block erase command is forcibly stopped are allocated in the program area, set the FMR13 bit in the FMR1 register to 1 (lock bit disabled) before executing the block erasure command again.
When the CMDRST bit is set to 1 (erasure/writing stopped) during erase-suspend, the suspend status is also initialized. Thus execute block erasure again to the block which the block erasure is being suspended.
When td(CMDRST-READY) has elapsed after the CMDRST bit is set to 1 (erasure/writing stopped), the executing command is forcibly terminated and reading from the flash memory is enabled.

CMDERIE Bit (Erase/Write Error Interrupt Enable Bit)

This bit enables a flash command error interrupt to be generated if the following errors occur:

- Program error
- Block erase error
- Command sequence error
- Block blank check error

If the CMDERIE bit is set to 1 (erase/write error interrupt enabled) and erasure/writing is performed, an interrupt is generated if the above errors occur.
If a flash command error interrupt is generated, execute the clear status register command during interrupt handling.

To change the CMDERIE bit from 0 (erase/write error interrupt disabled) to 1 (erase/write error interrupt enabled), make the setting as follows:
(1) Execute the clear status register command.
(2) Set the CMDERIE bit to 1.

BSYAEIE Bit (Flash Access Error Interrupt Enable Bit)

This bit enables a flash access error interrupt to be generated if the flash memory during rewriting is accessed.

To change the BSYAEIE bit from 0 (flash access error interrupt disabled) to 1 (flash access error interrupt enabled), make the setting as follows:
(1) Read the BSYAEI bit in the FST register (dummy read).
(2) Write 0 (no flash access error interrupt) to the BSYAEI bit.
(3) Set the BSYAEIE bit to 1 (flash access error interrupt enabled).

RDYSTIE Bit (Flash Ready Status Interrupt Enable Bit)

This bit enables a flash ready status error interrupt to be generated when the status of the flash memory sequence changes from the busy to ready status.

To change the RDYSTIE bit from 0 (flash ready status interrupt disabled) to 1 (flash ready status interrupt enabled), make the setting as follows:
(1) Read the RDYSTI bit in the FST register (dummy read).
(2) Write 0 (no flash ready status interrupt) to the RDYSTI bit.
(3) Set the RDYSTIE bit to 1 (flash ready status interrupt enabled).

30.4.3 Flash Memory Control Register 1 (FMR1) [R8C/38W Group, R8C/38Y Group]

Address 01B5h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	FMR17	FMR16	FMR15	FMR14	FMR13	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			—
b2	—			—
b3	FMR13	Lock bit disable select bit (1)	0: Lock bit enabled 1: Lock bit disabled	R/W
b4	FMR14	Data flash block A rewrite disable bit (2, 3)	0: Rewrite enabled (software command acceptable) 1: Rewrite disabled (software command not acceptable, no error occurred)	R/W
b5	FMR15	Data flash block B rewrite disable bit (2, 3)	0: Rewrite enabled (software command acceptable) 1: Rewrite disabled (software command not acceptable, no error occurred)	R/W
b6	FMR16	Data flash block C rewrite disable bit (2, 3)	0: Rewrite enabled (software command acceptable) 1: Rewrite disabled (software command not acceptable, no error occurred)	R/W
b7	FMR17	Data flash block D rewrite disable bit (2, 3)	0: Rewrite enabled (software command acceptable) 1: Rewrite disabled (software command not acceptable, no error occurred)	R/W

Notes:
1. To set the FMR13 bit to 1, first write 0 and then 1 immediately. Disable interrupts and DTC activation between writing 0 and writing 1.
2. To set this bit to 0, first write 1 and then 0 immediately. Disable interrupts and DTC activation between writing 1 and writing 0.
3. This bit is set to 0 when the FMR01 bit in the FMR0 register is set to 0 (CPU rewrite mode disabled).

FMR13 Bit (Lock Bit Disable Select Bit)

When the FMR13 bit is set to 1 (lock bit disabled), the lock bit is disabled. When the FMR13 bit is set to 0, the lock bit is enabled. Refer to **30.4.12 Data Protect Function** for the details of the lock bit.
The FMR13 bit enables the lock bit function only and the lock bit data does not change. However, when a block erase command is executed while the FMR13 bit is set to 1, the lock bit data set to 0 (locked) changes to 1 (not locked) after erasure completes.

[Conditions for setting to 0]
The FMR13 bit is set to 0 when one of the following conditions is met.
- Completion of the program command
- Completion of the erase command
- Transition to erase-suspend
- Generation of a command sequence error
- If the FMR01 bit in the FMR0 register is set to 0 (CPU rewrite mode disabled).
- If the FMSTP bit in the FMR0 register is set to 1 (flash memory stops).
- If the CMDRST bit in the FMR0 register is set to 1 (erasure/writing stopped).

[Condition for setting to 1]
Set to 1 by a program.

FMR14 Bit (Data Flash Block A Rewrite Disable Bit)

When the FMR 14 bit is set to 0, data flash block A accepts program and block erase commands.

FMR15 Bit (Data Flash Block B Rewrite Disable Bit)

When the FMR 15 bit is set to 0, data flash block B accepts program and block erase commands.

FMR16 Bit (Data Flash Block C Rewrite Disable Bit)

When the FMR 16 bit is set to 0, data flash block C accepts program and block erase commands.

FMR17 Bit (Data Flash Block D Rewrite Disable Bit)

When the FMR 17 bit is set to 0, data flash block D accepts program and block erase commands.

30.4.4 Flash Memory Control Register 1 (FMR1) [R8C/38X Group, R8C/38Z Group]

Address 01B5h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	FMR13	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			—
b2	—			—
b3	FMR13	Lock bit disable select bit (1)	0: Lock bit enabled 1: Lock bit disabled	R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

Note:
1. To set the FMR13 bit to 1, first write 0 and then 1 immediately. Disable interrupts and DTC activation between writing 0 and writing 1.

FMR13 Bit (Lock Bit Disable Select Bit)

When the FMR13 bit is set to 1 (lock bit disabled), the lock bit is disabled. When the FMR13 bit is set to 0, the lock bit is enabled. Refer to **30.4.12 Data Protect Function** for the details of the lock bit.
The FMR13 bit enables the lock bit function only and the lock bit data does not change. However, when a block erase command is executed while the FMR13 bit is set to 1, the lock bit data set to 0 (locked) changes to 1 (not locked) after erasure completes.

[Conditions for setting to 0]
The FMR13 bit is set to 0 when one of the following conditions is met.
- Completion of the program command
- Completion of the erase command
- Transition to erase-suspend
- Generation of a command sequence error
- If the FMR01 bit in the FMR0 register is set to 0 (CPU rewrite mode disabled).
- If the FMSTP bit in the FMR0 register is set to 1 (flash memory stops).
- If the CMDRST bit in the FMR0 register is set to 1 (erasure/writing stopped).

[Condition for setting to 1]
Set to 1 by a program.

30.4.5 Flash Memory Control Register 2 (FMR2) [R8C/38W Group, R8C/38Y Group]

Address 01B6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	FMR27	—	—	—	FMR23	FMR22	FMR21	FMR20
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FMR20	Erase-suspend enable bit (1)	0: Erase-suspend disabled 1: Erase-suspend enabled	R/W
b1	FMR21	Erase-suspend request bit (2)	0: Erase restart 1: Erase-suspend request	R/W
b2	FMR22	Interrupt request suspend request enable bit (1)	0: Erase-suspend request disabled by interrupt request 1: Erase-suspend request enabled by interrupt request	R/W
b3	FMR23	Data flash access cycle selection bit (3)	0: 2 cycles of CPU clock 1: 4 cycles of CPU clock	R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	FMR27	Low-consumption-current read mode enable bit (1, 4)	0: Low-consumption-current read mode disabled 0: Low-consumption-current read mode enabled	R/W

Notes:
1. To set this bit to 1, first write 0 and then 1 immediately. Disable interrupts and DTC activation between writing 0 and writing 1.
2. To set the FMR21 bit to 0 (erase restart), set it when the FMR01 bit in the FMR0 register is set to 1 (CPU rewrite mode enabled).
3. To use the data flash with more than 16 MHz CPU clock, set this bit to 1 (4 cycles of the CPU clock).
4. After setting the CPU clock to the low-speed on-chip oscillator clock divided by 4, 8, or 16, set the FMR27 bit to 1. When divided by 1 (no division) or divided by 2 is set, do not use low-consumption-current read mode.
   Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).
   Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

FMR20 Bit (Erase-Suspend Enable Bit)

When the FMR20 bit is set to 1 (enabled), the erase-suspend function is enabled.

FMR21 Bit (Erase-Suspend Request Bit)

When the FMR21 bit is set to 1, erase-suspend mode is entered. If the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request) when an interrupt request for the enabled interrupt is generated, and erase-suspend mode is entered. To restart auto-erasure, set the FMR21 bit to 0 (erase restart).

[Condition for setting to 0]
Set to 0 by a program.
[Conditions for setting to 1]
- When the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request) at the time an interrupt is generated.
- Set to 1 by a program.

FMR22 Bit (Interrupt Request Suspend-Request Enable Bit)

When the FMR 22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request) at the time an interrupt request is generated during auto-erasure. Set the FMR22 bit to 1 when using erase-suspend while rewriting the user ROM area in EW1 mode.

FMR23 bit (data flash access cycle selection bit)

When the FMR23 bit is set to 1, the read timing of the data flash is changed from 2 cycles of CPU clock usually to four cycles. The access to program ROM area, SFR, and the RAM area is not changed.
To use the data flash with more than 16 MHz CPU clock, set this bit to 1 (4 cycles of the CPU clock).

FMR27 Bit (Low-Power-Current Read Mode Enable Bit)

When the FMR 27 bit is set to 1 (low-consumption-current read mode enabled) in low-speed on-chip oscillator mode (XIN clock stopped), power consumption when reading the flash memory can be reduced. Refer to **31.2.11 Low-Current-Consumption Read Mode** for details.
When the CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16, low-consumption-current read mode can be used. When divided by 1 (no division) or divided by 2 is set, do not use low-consumption-current read mode. After setting the divide ratio of the CPU clock, set the FMR27 bit to 1.
Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).
Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).
When the FMR27 bit is set to 1 (low-consumption-current read mode enabled), do not execute the program, block erase, or lock bit program command. To change the FMSTP bit from 1 (flash memory stops) to 0 (flash memory operates), make the setting when the FMR27 bit is set to 0 (low-consumption-current read mode disabled).

30.4.6 Flash Memory Control Register 2 (FMR2)[R8C/38X Group, R8C/38Z Group]

Address 01B6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	FMR27	—	—	—	—	FMR22	FMR21	FMR20
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FMR20	Erase-suspend enable bit (1)	0: Erase-suspend disabled 1: Erase-suspend enabled	R/W
b1	FMR21	Erase-suspend request bit (2)	0: Erase restart 1: Erase-suspend request	R/W
b2	FMR22	Interrupt request suspend request enable bit (1)	0: Erase-suspend request disabled by interrupt request 1: Erase-suspend request enabled by interrupt request	R/W
b3	—	Reserved bits	Set to 0.	R/W
b4	—			
b5	—			
b6	—			
b7	FMR27	Low-consumption-current read mode enable bit (1, 3)	0: Low-consumption-current read mode disabled 0: Low-consumption-current read mode enabled	R/W

Notes:
1. To set this bit to 1, first write 0 and then 1 immediately. Disable interrupts and DTC activation between writing 0 and writing 1.
2. To set the FMR21 bit to 0 (erase restart), set it when the FMR01 bit in the FMR0 register is set to 1 (CPU rewrite mode enabled).
3. After setting the CPU clock to the low-speed on-chip oscillator clock divided by 4, 8, or 16, set the FMR27 bit to 1. When divided by 1 (no division) or divided by 2 is set, do not use low-consumption-current read mode.
   Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).
   Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

FMR20 Bit (Erase-Suspend Enable Bit)

When the FMR20 bit is set to 1 (enabled), the erase-suspend function is enabled.

FMR21 Bit (Erase-Suspend Request Bit)

When the FMR21 bit is set to 1, erase-suspend mode is entered. If the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request) when an interrupt request for the enabled interrupt is generated, and erase-suspend mode is entered. To restart auto-erasure, set the FMR21 bit to 0 (erase restart).

[Condition for setting to 0]
Set to 0 by a program.
[Conditions for setting to 1]
- When the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request) at the time an interrupt is generated.
- Set to 1 by a program.

FMR22 Bit (Interrupt Request Suspend-Request Enable Bit)

When the FMR 22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request) at the time an interrupt request is generated during auto-erasure. Set the FMR22 bit to 1 when using erase-suspend while rewriting the user ROM area in EW1 mode.

FMR27 Bit (Low-Power-Current Read Mode Enable Bit)

When the FMR 27 bit is set to 1 (low-consumption-current read mode enabled) in low-speed on-chip oscillator mode (XIN clock stopped), power consumption when reading the flash memory can be reduced. Refer to **31.2.11 Low-Current-Consumption Read Mode** for details.

When the CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16, low-consumption-current read mode can be used. When divided by 1 (no division) or divided by 2 is set, do not use low-consumption-current read mode. After setting the divide ratio of the CPU clock, set the FMR27 bit to 1.

Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled). Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

When the FMR27 bit is set to 1 (low-consumption-current read mode enabled), do not execute the program, block erase, or lock bit program command. To change the FMSTP bit from 1 (flash memory stops) to 0 (flash memory operates), make the setting when the FMR27 bit is set to 0 (low-consumption-current read mode disabled).

30.4.7 EW0 Mode

When the FMR01 bit in the FMR0 register is set to 1 (CPU rewrite mode enabled), the MCU enters CPU rewrite mode and software commands can be accepted. At this time, the FMR02 bit in the FMR0 register is set to 0 so that EW0 mode is selected.

Software commands are used to control program and erase operations. The FST register can be used to confirm whether programming or erasure has completed.

To enter erase-suspend during auto-erasure, set the FMR20 bit to 1 (erase-suspend enabled) and the FMR21 bit to 1 (erase-suspend request). Next, verify the FST7 bit in the FST register is set to 1 (ready), then verify the FST6 bit is set to 1 (during erase-suspend) before accessing the flash memory. When the FST6 bit is set to 0, erasure completes.

When the FMR21 bit in the FMR2 register is set to 0 (erase restart), auto-erasure restarts. To confirm whether auto-erasure has restarted, verify the FST7 bit in the FST register is set to 0, then verify the FST6 bit is set to 0 (other than erase-suspend).

30.4.8 EW1 Mode

After the FMR01 bit in the FMR0 register is set to 1 (CPU rewrite mode enabled), EW1 mode is selected by setting the FMR02 bit is set to 1.

The FST register can be used to confirm whether programming and erasure has completed.

To enable the erase-suspend function during auto-erasure, execute the block erase command after setting the FMR20 bit in the FMR2 register to 1 (suspend enabled). To enter erase-suspend while auto-erasing the user ROM area, set the FMR22 bit in the FMR2 register to 1 (erase-suspend request enabled by interrupt request). Also, the interrupt to enter erase-suspend must be enabled beforehand.

When an interrupt request is generated, the FMR21 bit in the FMR2 register is automatically set to 1 (erase-suspend request) and auto-erasure suspends after td(SR-SUS). After interrupt handling completes, set the FMR21 bit to 0 (erase restart) to restart auto-erasure.

30.4.9 Suspend Operation

The suspend function halts the auto-erase operation temporarily during auto-erasure.
When auto-erasure is suspended, the next operation can be executed. (Refer to **Table 30.5 Executable Operation during Suspend**.)

- When suspending the auto-erasure of any block in data flash (only for R8C/38W Group and R8C/38Y Group), auto-programming and reading another block can be executed.
- When suspending the auto-erasure of data flash, auto-programming and reading program ROM can be executed.
- When suspending the auto-erasure of any block in program ROM, auto-programming and reading another block can be executed.
- When suspending the auto-erasure of program ROM, auto-programming and reading data flash can be executed.
- To check the suspend, verify the FST7 bit is set to 1 (ready), then verify the FST6 bit is set to 1 (during erase-suspend) to confirm whether erasure has been suspended. When the FST6 bit is set to 0 (other than erase suspend), erasure completes.

Figure 30.3 shows the Suspend Operation Timing.

Table 30.5 Executable Operation during Suspend

		Operation during Suspend											
		Data flash (Block during erasure execution before entering suspend)			Data flash (Block during no erasure execution before entering suspend)			Program ROM (Block during erasure execution before entering suspend)			Program ROM (Block during no erasure execution before entering suspend)		
		Erase	Program	Read	Erase	Program	Read	Erase	Program	Read	Erase	Program	Read
Areas during erasure execution before entering suspend	Data flash	D	D	D	D	E	E	N/A	N/A	N/A	D	E	E (5)
	Program ROM	N/A	N/A	N/A	D	E	E	D	D	D	D	E	E

Notes:
1. E indicates operation is enabled by using the suspend function, D indicates operation is disabled, and N/A indicates no combination is available.
2. Operation cannot be suspended during programming.
3. The block erase command can be executed for erasure. The program, lock bit program, and read lock bit status commands can be executed for programming.
   The clear status register command can be executed when the FST7 bit in the FST register is set to 1 (ready).
   The operation of block blank check is disabled during suspend.
4. The MCU enters read array mode immediately after entering erase-suspend.
5. The program ROM area can be read with the BGO function while programming or block erasing data flash.
6. The R8C/38W Group and R8C/38Y Group have data flash.

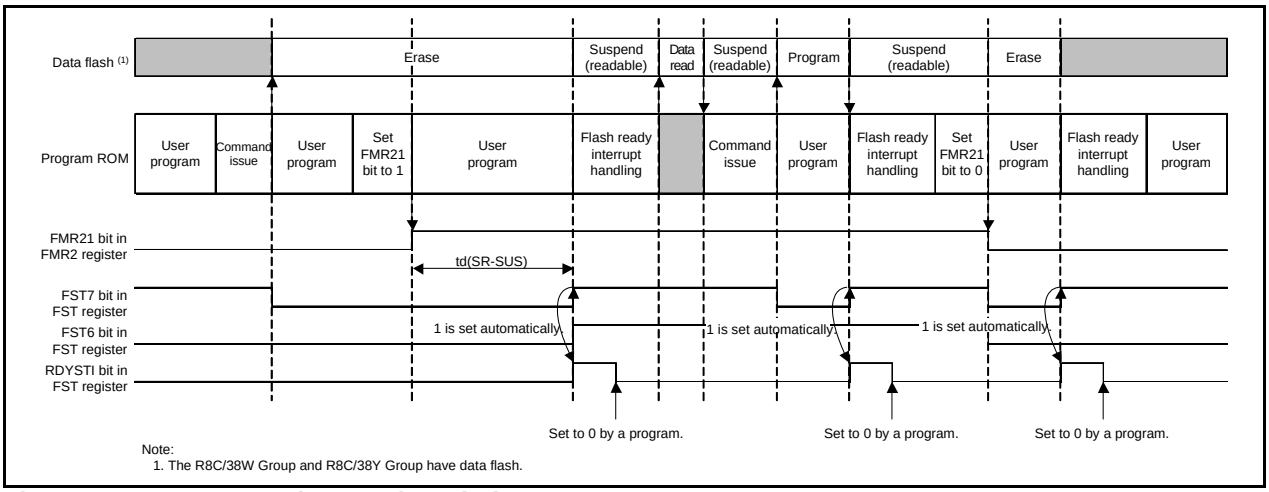


Figure 30.3 Suspend Operation Timing

30.4.10 How to Set and Exit Each Mode

Figure 30.4 shows How to Set and Exit EW0 Mode and Figure 30.5 shows How to Set and Exit EW0 Mode (When Rewriting Data Flash) and EW1 Mode.

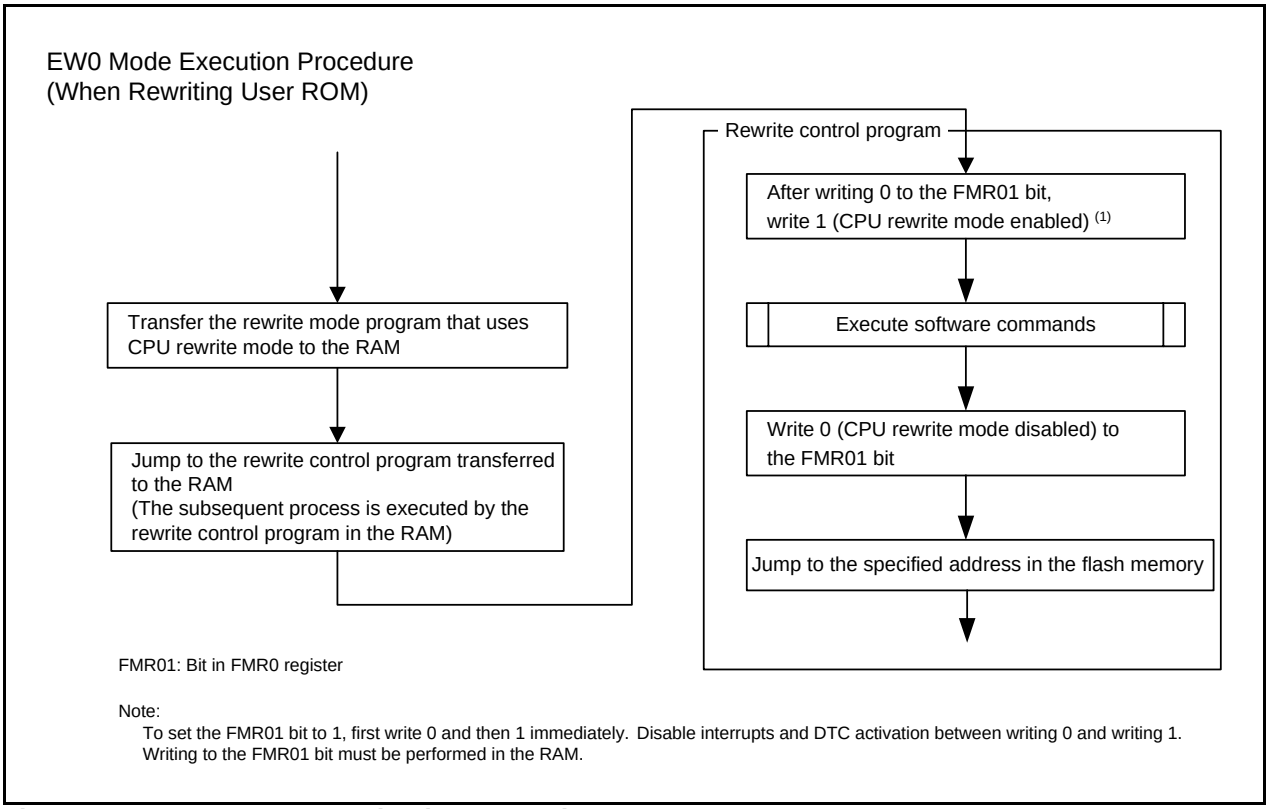


Figure 30.4 How to Set and Exit EW0 Mode

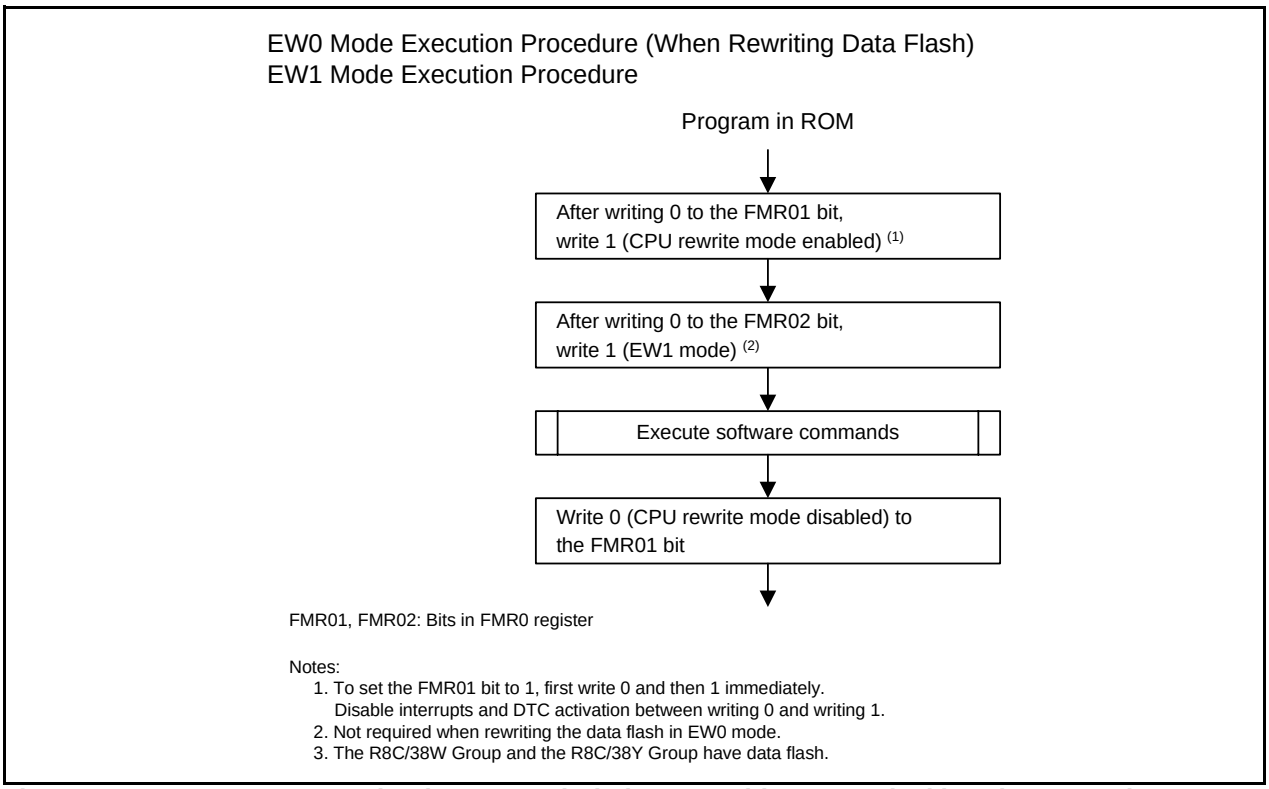


Figure 30.5 How to Set and Exit EW0 Mode (When Rewriting Data Flash) and EW1 Mode

30.4.11 BGO (BackGround Operation) Function [R8C/38W Group, R8C/38Y Group]

When the program ROM area is specified while a program or block erase operation to the data flash, array data can be read. This eliminates the need for writing software commands. Access time is the same as for normal read operations.
Any other block of the data flash cannot read during a program or block erase operation to the data flash.
Figure 30.6 shows the BGO Function.

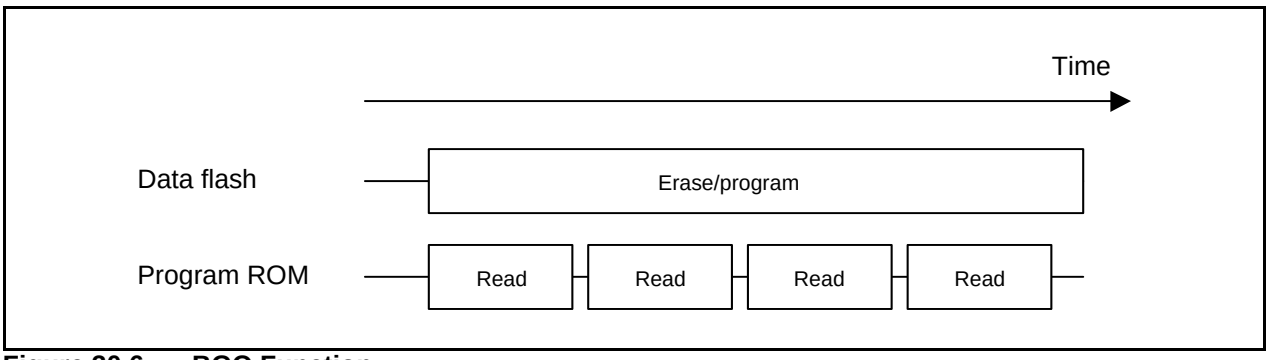


Figure 30.6 BGO Function

30.4.12 Data Protect Function

Each block in the flash memory has a nonvolatile lock bit. The lock bit is enabled by setting the FMR13 bit in the FMR1 register is set to 0 (lock bit enabled). The lock bit can be used to disable (lock) programming or erasing each block. This prevents data from being written or erased inadvertently. A block status changes according to the lock bit as follows:

- When the lock bit data is set to 0: locked (the block cannot be programmed or erased)
- When the lock bit data is set to 1: not locked (the block can be programmed and erased)

The lock bit data is set to 0 (locked) by executing the lock bit program command and to 1 (not locked) by erasing the block. No commands can be used to set only the lock bit data to 1.
The lock bit data can be read using the read lock bit status command.

When the FMR13 bit is set to 1 (lock bit disabled), the lock bit function is disabled and all blocks are not locked (each lock bit data remains unchanged). The lock bit function is enabled by setting the FMR13 bit to 0 (the lock bit data is retained).
When the block erase command is executed while the FMR13 bit is set to 1, the target block is erased regardless of the lock bit status. The lock bit of the erase target block is set to 1 after auto-erasure completes.
Refer to **30.4.13 Software Commands** for the details of individual commands.
The FMR13 bit is set to 0 after auto-erasure completes. This bit is also set to 0 if one of the following conditions is met. To erase or program a different locked block, set the FMR 13 bit to 1 again and execute the block erase or program command.

- If the FST7 bit in the FST register is changed from 0 (busy) to 1 (ready).
- If a command sequence error occurs.
- If the FMR01 bit in the FMR0 register is set to 0 (CPU mode disabled).
- If the FMSTP bit in the FM0 register is set to 1 (flash memory stops).
- If the CMDRST bit in the FMR0 register is set to 1 (erasure/writing stopped).

Figure 30.7 shows the FMR13 Bit Operation Timing.

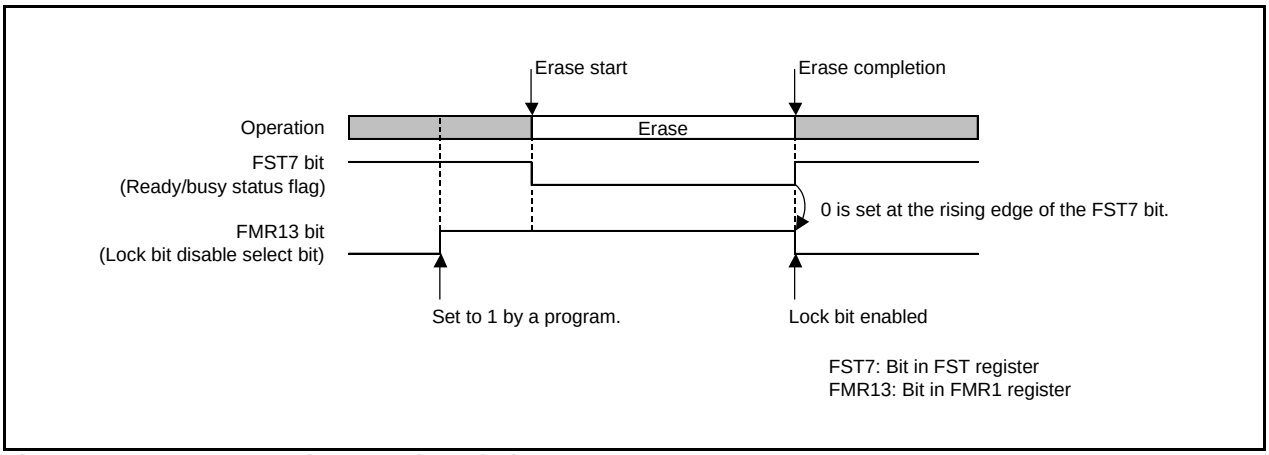


Figure 30.7 FMR13 Bit Operation Timing

30.4.13 Software Commands

The software commands are described below. Read or write commands and data in 8-bit units. However, write the program (word units) command and data in 16-bit units.
Do not input any command other than those listed in the table below.

Table 30.6 Software Commands

Command	First Bus Cycle			Second Bus Cycle		
	Mode	Address	Data	Mode	Address	Data
Read array	Write	×	FFh			
Clear status register	Write	×	50h			
Program (byte units)	Write	WA	40h	Write	WA	WD_8
Program (word units)	Write	WA	××40h	Write	WA	WD_{16}
Block erase	Write	×	20h	Write	BA	D0h
Lock bit program	Write	BT	77h	Write	BT	D0h
Read lock bit status	Write	×	71h	Write	BT	D0h
Block blank check	Write	×	25h	Write	BA	D0h

WA: Write address (Specify an even address when performing programming in word units.)
WD_8: Write data (8 bits)
WD_{16}: Write data (16 bits)
BA: Any block address
BT: Starting block address
×: Any address in the user ROM area
××: 8 high-order bits of command code (ignored)

30.4.13.1 Read Array Command

The read array command is used to read the flash memory.
When FFh is written in the first bus cycle, the MCU enters read array mode. When the read address is input in the following bus cycles, the content of the specified address can be read in 8-bit units.
Since read array mode remains until another command is written, the contents of multiple addresses can be read continuously.
In addition, after a reset, the MCU enters read array mode after a program, block erase, block blank check, read lock bit status, or clear status register command, or after entering erase-suspend.

30.4.13.2 Clear Status Register Command

The clear status register command is used to set bits FST4 and FST5 in the FST register to 0.
When 50h is written in the first bus cycle, bits FST4 and FST5 in the FST register are set to 0.

30.4.13.3 Program Command

The program command is used to write data to the flash memory in 1-byte or 1-word units.
When 40h (or xx40h) is written in the first bus cycle and data is written in the second bus cycle to the write address, auto-programming (data program and verify operation) starts. Make sure the address value specified in the first bus cycle is the same address as the write address specified in the second bus cycle. When performing programming in word units, set the address value to an even address.
The FST7 bit in the FST register can be used to confirm whether auto-programming has completed. The FST7 bit is set to 0 during auto-programming and is set to 1 when auto-programming completes.
After auto-programming has completed, the auto-program result can be confirmed by the FST4 bit in the FST register (refer to **30.4.14 Full Status Check**).
Do not write additions to the already programmed addresses.

The program command targeting each block in the program ROM can be disabled using the lock bit.
As for the R8C/38W Group and R8C/38Y Group, following commands are not accepted under the following conditions:

- Block erase commands targeting data flash block A when the FMR14 bit in the FMR1 register is set to 1 (rewrite disabled).
- Block erase commands targeting data flash block B when the FMR15 bit is set to 1 (rewrite disabled).
- Block erase commands targeting data flash block C when the FMR16 bit is set to 1 (rewrite disabled).
- Block erase commands targeting data flash block D when the FMR17 bit is set to 1 (rewrite disabled).

Figure 30.8 shows a Program Flowchart (Flash Ready Status Interrupt Disabled) and Figure 30.9 shows a Program Flowchart (Flash Ready Status Interrupt Enabled).

In EW1 mode, do not execute this command to any address where a rewrite control program is allocated.

When the RDYSTIE bit in the FMR0 register is set to 1 (flash ready status interrupt enabled), a flash ready status interrupt can be generated upon completion of auto-programming. The auto-program result can be confirmed by reading the FST register during the interrupt routine.

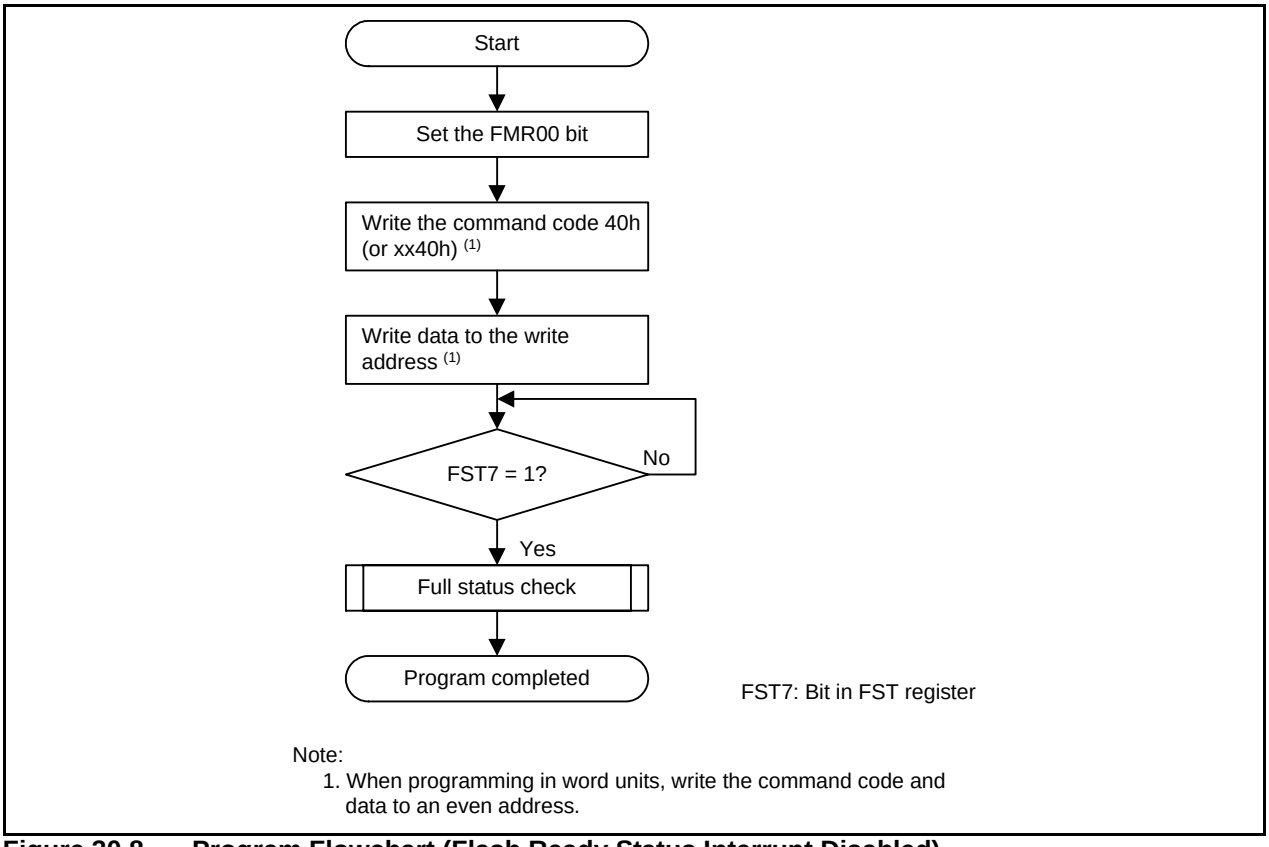


Figure 30.8 Program Flowchart (Flash Ready Status Interrupt Disabled)

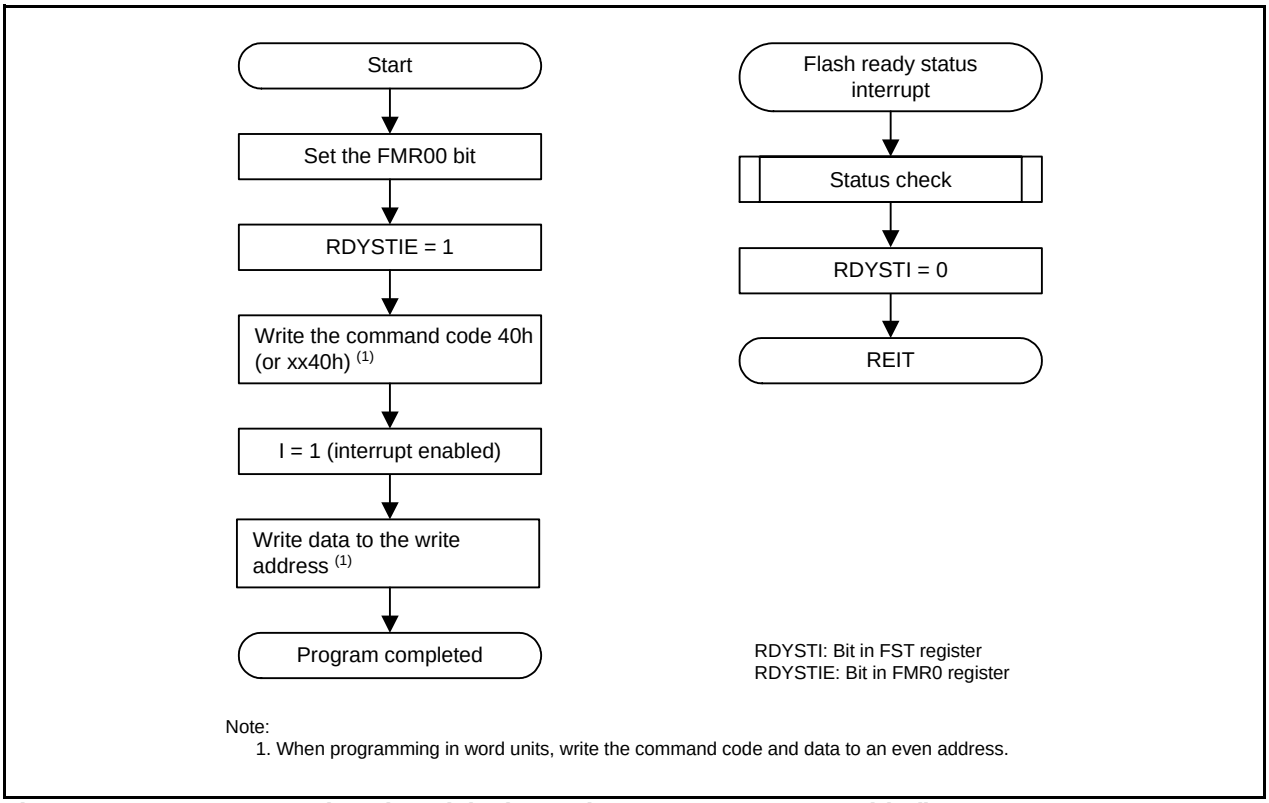


Figure 30.9 Program Flowchart (Flash Ready Status Interrupt Enabled)

30.4.13.4 Block Erase Command

When 20h is written in the first bus cycle and then D0h is written in the second bus cycle to any block address, auto-erasure (erase and erase verify operation) starts in the specified block.
The FST7 bit in the FST register can be used to confirm whether auto-erasure has completed. The FST7 bit is set to 0 during auto-erasure and is set to 1 when auto-erasure completes. After auto-erasure completes, all data in the block is set to FFh.
After auto-erasure has completed, the auto-erase result can be confirmed by the FST5 bit in the FST register. (Refer to **30.4.14 Full Status Check**).

The block erase command targeting each block in the program ROM can be disabled using the lock bit.
As for the R8C/38W Group and R8C/38Y Group, following commands are not accepted under the following conditions:

- Block erase commands targeting data flash block A when the FMR14 bit in the FMR1 register is set to 1 (rewrite disabled).
- Block erase commands targeting data flash block B when the FMR15 bit is set to 1 (rewrite disabled).
- Block erase commands targeting data flash block C when the FMR16 bit is set to 1 (rewrite disabled).
- Block erase commands targeting data flash block D when the FMR17 bit is set to 1 (rewrite disabled).

Figure 30.10 shows a Block Erase Flowchart (Flash Ready Status Interrupt Disabled), Figure 30.11 shows a Block Erase Flowchart (Flash Ready Status Interrupt Disabled and Suspend Enabled), and Figure 30.12 shows a Block Erase Flowchart (Flash Ready Status Interrupt Enabled and Suspend Enabled).

In EW1 mode, do not execute this command to any block where a rewrite control program is allocated.

While the RDYSTIE bit in the FMR0 register is set to 1 (flash ready status interrupt enabled), a flash ready status interrupt can be generated upon completion of auto-erasure. While the RDYSTIE bit is set to 1 and the FMR20 bit in the FMR2 register is set to 1 (erase-suspend enabled), a flash ready status interrupt is generated when the FMR21 bit is set to 1 (erase-suspend request) and auto-erasure suspends. The auto-erase result can be confirmed by reading the FST register during the interrupt routine.

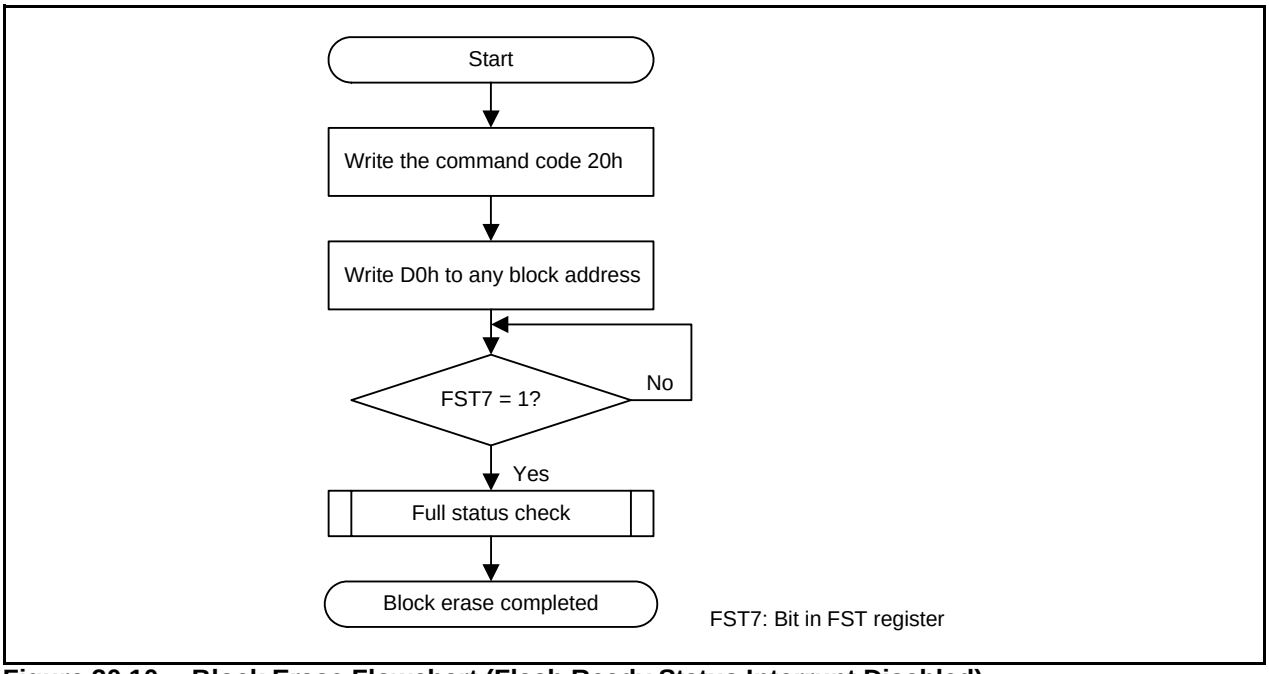
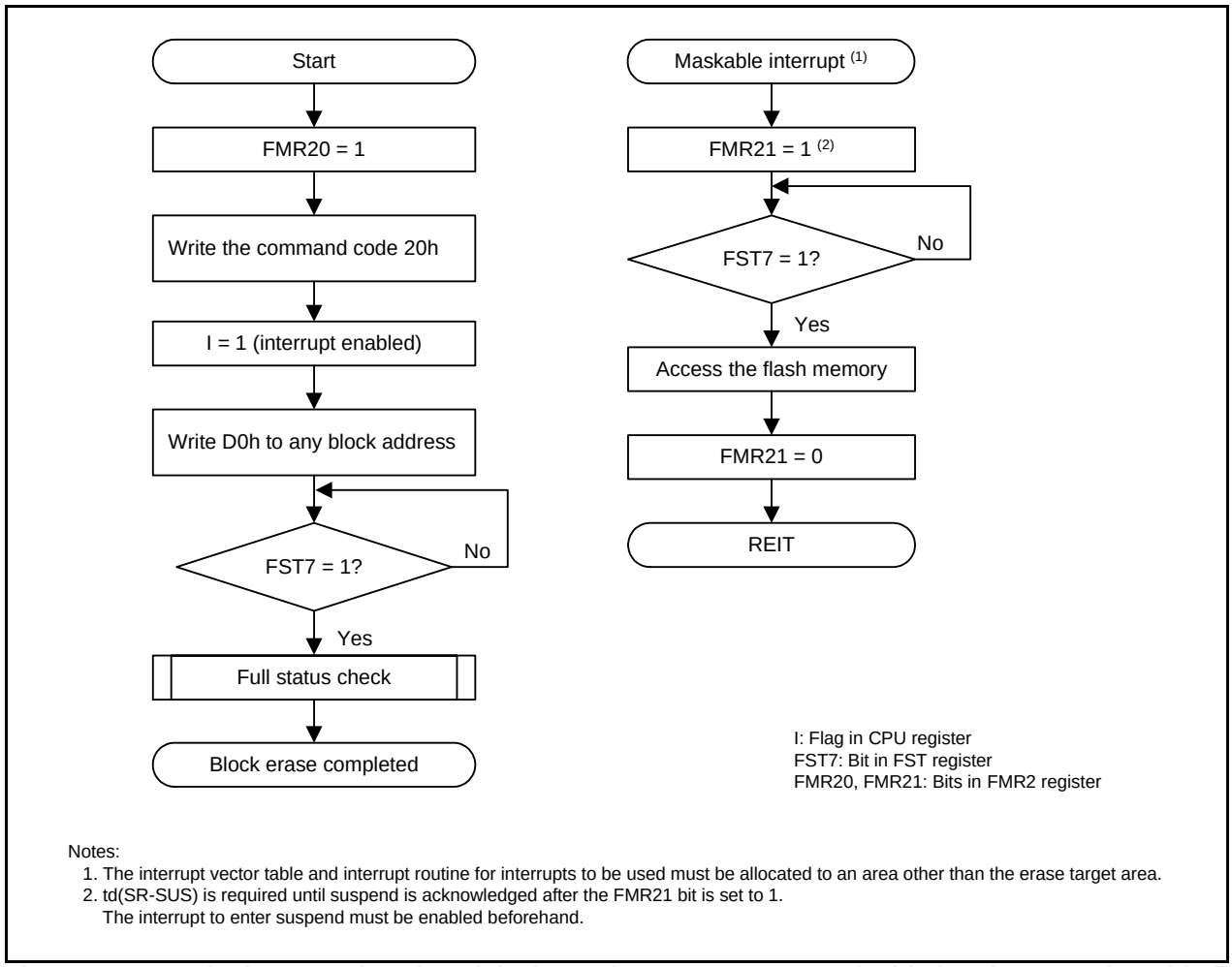
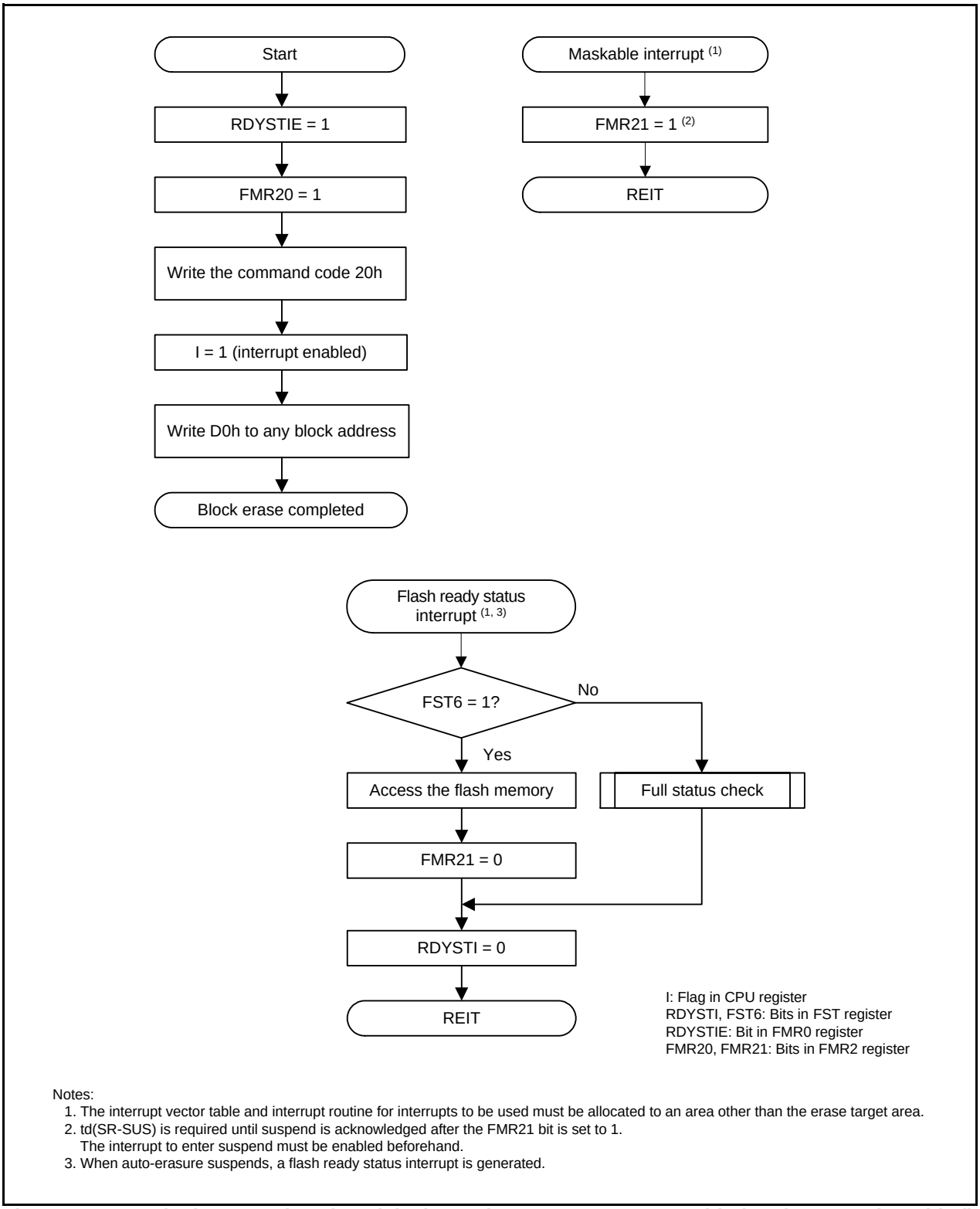


Figure 30.10 Block Erase Flowchart (Flash Ready Status Interrupt Disabled)



Notes:
1. The interrupt vector table and interrupt routine for interrupts to be used must be allocated to an area other than the erase target area.
2. td(SR-SUS) is required until suspend is acknowledged after the FMR21 bit is set to 1.
   The interrupt to enter suspend must be enabled beforehand.

Figure 30.11 Block Erase Flowchart (Flash Ready Status Interrupt Disabled and Suspend Enabled)



Notes:
1. The interrupt vector table and interrupt routine for interrupts to be used must be allocated to an area other than the erase target area.
2. td(SR-SUS) is required until suspend is acknowledged after the FMR21 bit is set to 1.
   The interrupt to enter suspend must be enabled beforehand.
3. When auto-erasure suspends, a flash ready status interrupt is generated.

Figure 30.12 Block Erase Flowchart (Flash Ready Status Interrupt Enabled and Suspend Enabled)

30.4.13.5 Lock Bit Program Command

This command is used to set the lock bit of any block in the program ROM area to 0 (locked).
When 77h is written in the first bus cycle and D0h is written in the second bus cycle to the starting block address, 0 is written to the lock bit of the specified block. Make sure the address value in the first bus cycle is the same address as the starting block address specified in the second bus cycle.
Figure 30.13 shows a Lock Bit Program Flowchart. The lock bit status (lock bit data) can be read using the read lock bit status command.
The FST7 bit in the FST register can be used to confirm whether writing to the lock bit has completed.
Refer to **30.4.12 Data Protect Function** for the lock bit function and how to set the lock bit to 1 (not locked).

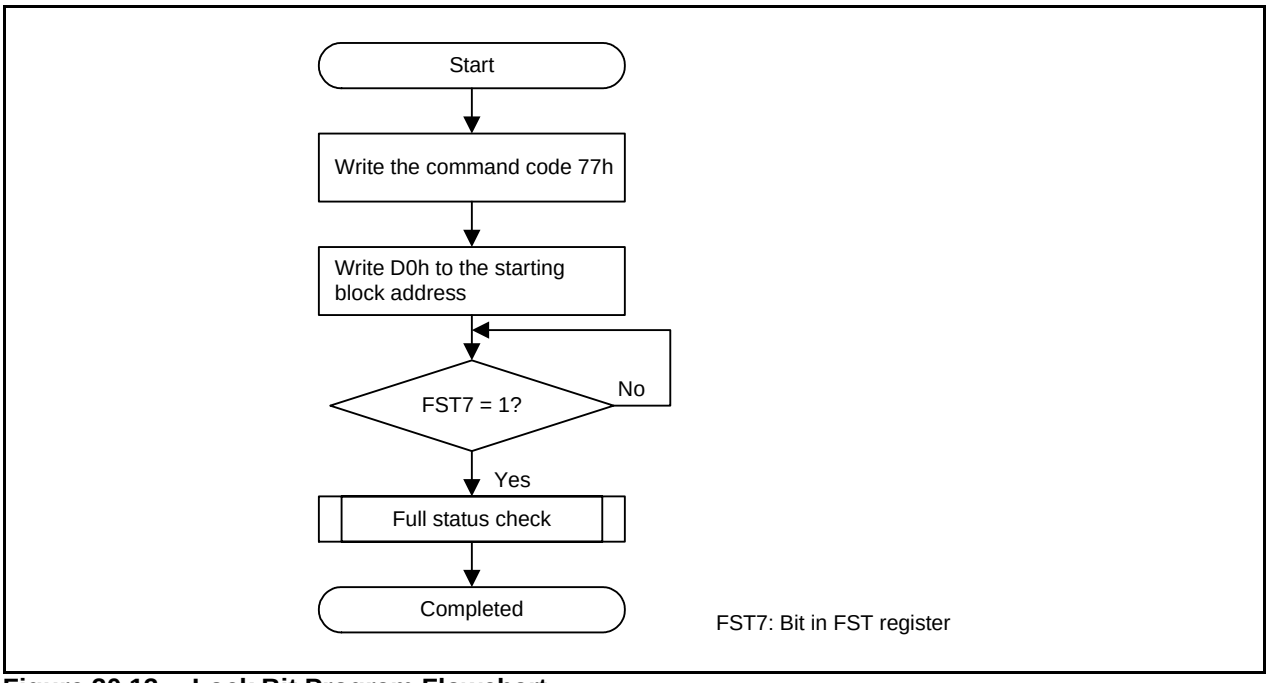


Figure 30.13 Lock Bit Program Flowchart

30.4.13.6 Read Lock Bit Status Command

This command is used to read the lock bit status of any address in the program ROM area.
When 71h written in the first bus cycle and D0h is written in the second cycle to the starting block address, the lock bit status of the specified block is stored in the LBDATA bit in the FST register. After the FST7 bit in the FST register has been set to 1 (ready), read the LBDATA bit.
Figure 30.14 shows a Read Lock Bit Status Flowchart.

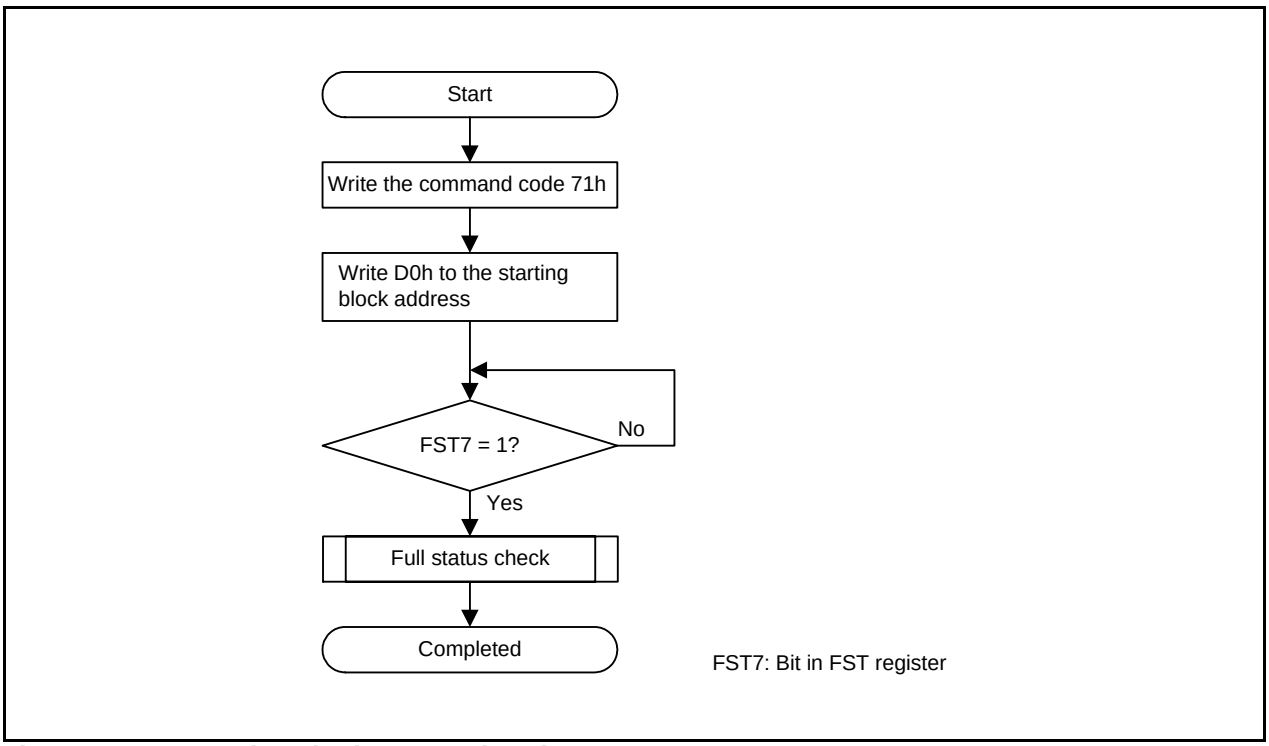


Figure 30.14 Read Lock Bit Status Flowchart

30.4.13.7 Block Blank Check Command

This command is used to confirm that all addresses in any block are blank data FFh.
When 25h is written in the first bus cycle and D0h is written in the second bus cycle to any block address, blank checking starts in the specified block. The FST7 bit in the FST register can be used to confirm whether blank checking has completed. The FST7 bit is set to 0 during the blank-check period and set to 1 when blank checking completes.
After blank checking has completed, the blank-check result can be confirmed by the FST5 bit in the FST register. (Refer to **30.4.14 Full Status Check**.). This command is used to verify the target block has not been written to. To confirm whether erasure has completed normally, execute the full status check.

Do not execute the block blank check command when the FST6 bit is set to 1 (during erase-suspend).
Figure 30.15 shows a Block Blank Check Flowchart.

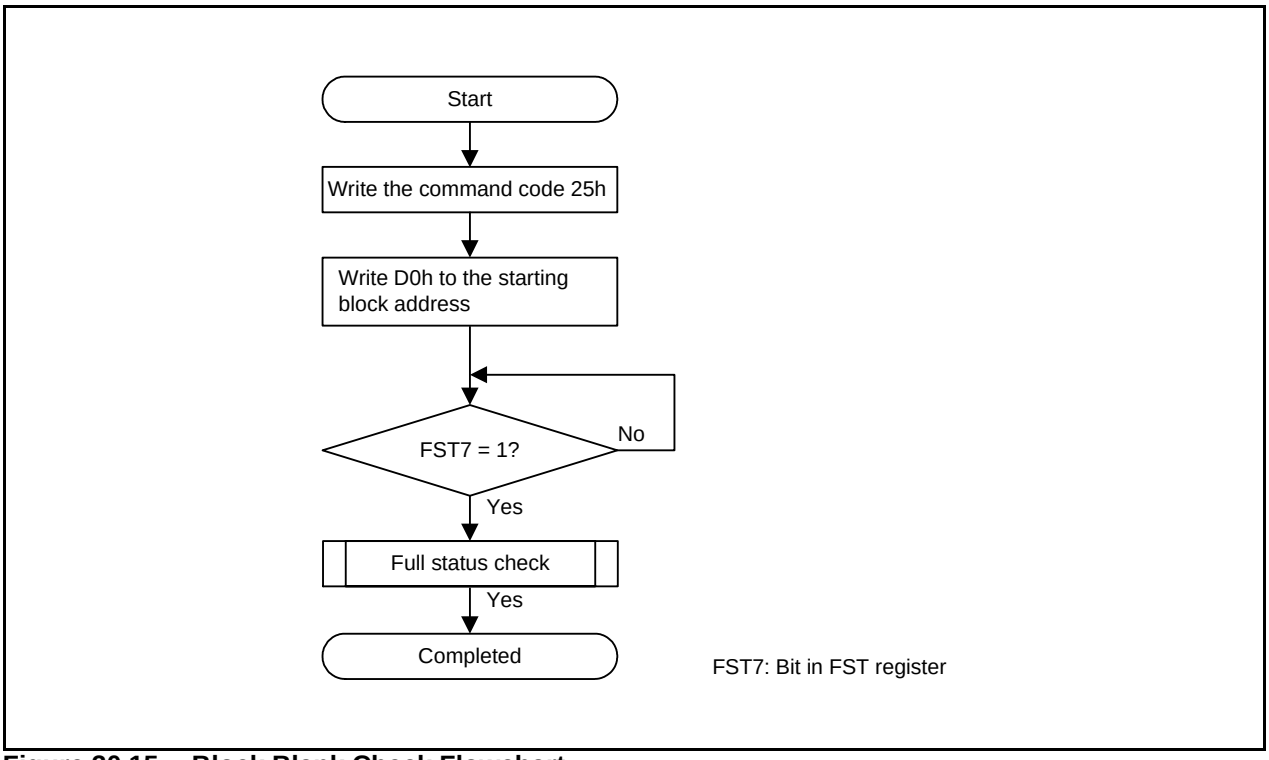


Figure 30.15 Block Blank Check Flowchart

This command is intended for programmer manufactures, not for general users.

30.4.14 Full Status Check

If an error occurs, bits FST4 and FST5 in the FST register are set to 1, indicating the occurrence of an error. The execution result can be confirmed by checking these status bits (full status check).
Table 30.7 lists the Errors and FST Register Status. Figure 30.16 shows the Full Status Check and Handling Procedure for Individual Errors.

Table 30.7 Errors and FST Register Status

FST Register Status		Error	Error Occurrence Condition
FST5	FST4		
1	1	Command sequence error	• When a command is not written correctly. • When data other than valid data (i.e., D0h or FFh) is written in the second bus cycle of the block erase command (1). • The erase command is executed during suspend • The command is executed to the block during suspend
1	0	Erase error	When the block erase command is executed, but auto-erasure does not complete correctly.
		Blank check error	When the block blank check command is executed and data other than blank data FFh is read.
0	1	Program error/ lock bit program error	When the program command is executed, but auto-programming does not complete correctly.

Note:
1. When FFh is written in the second bus cycle of these commands, the MCU enters read array mode. At the same time, the command code written in the first bus cycle is invalid.

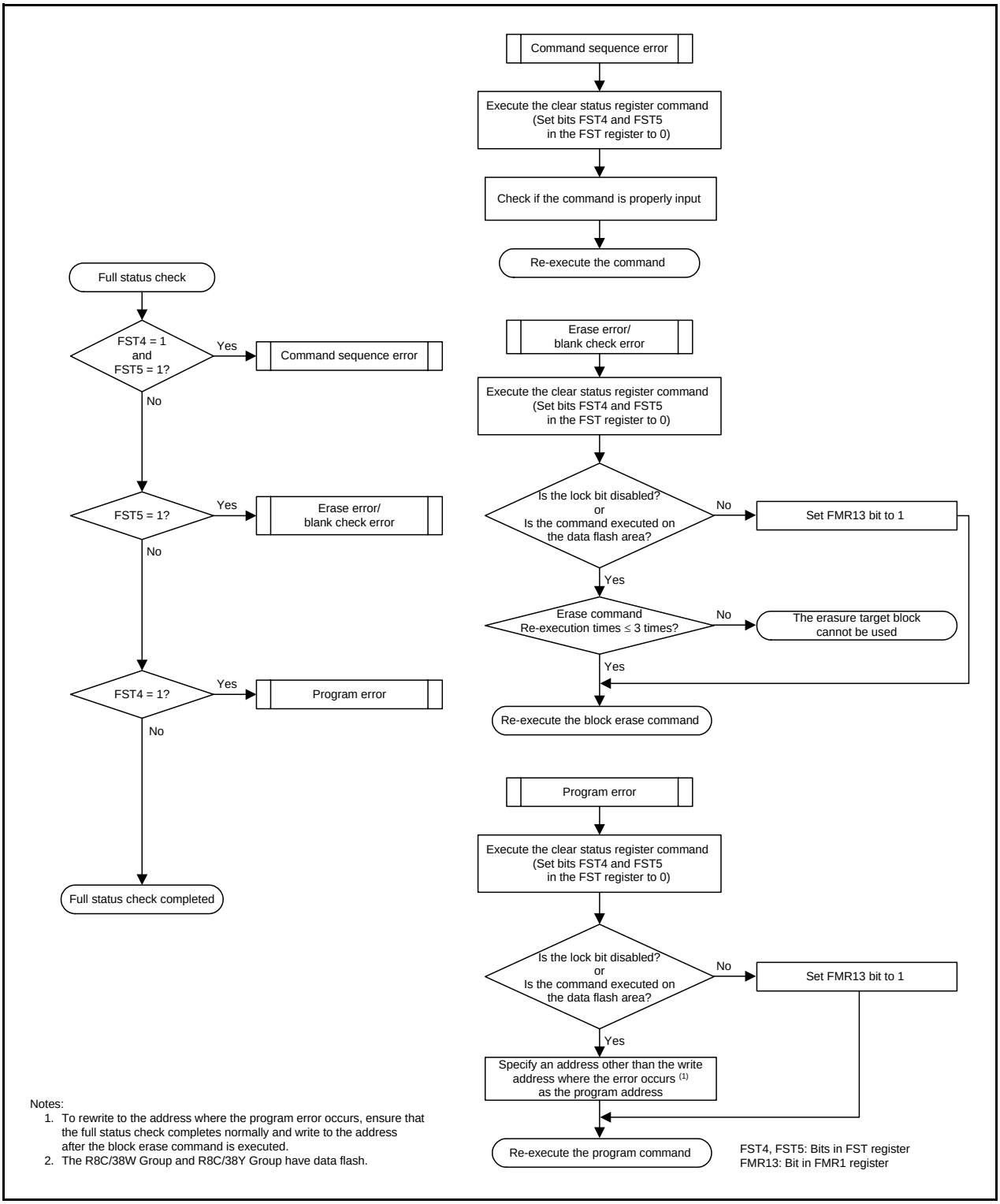


Figure 30.16 Full Status Check and Handling Procedure for Individual Errors

30.5 Standard Serial I/O Mode

In standard serial I/O mode, a serial programmer which supports the MCU can be used to rewrite the user ROM area while the MCU is mounted on-board.
There are three types of standard serial I/O modes:

- Standard serial I/O mode 1 .....Clock synchronous serial I/O used to connect to a serial programmer
- Standard serial I/O mode 2 .....Clock asynchronous serial I/O used to connect to a serial programmer
- Standard serial I/O mode 3 .....Special clock asynchronous serial I/O used to connect to a serial programmer

Standard serial I/O mode 2 and standard serial I/O mode 3 can be used for the MCU.

Refer to **Appendix 2. Connection Examples between Serial Programmer and On-Chip Debugging Emulator** for examples of connecting to a serial programmer. Contact the serial programmer manufacturer for more information. Refer to the user's manual included with your serial programmer for instructions.

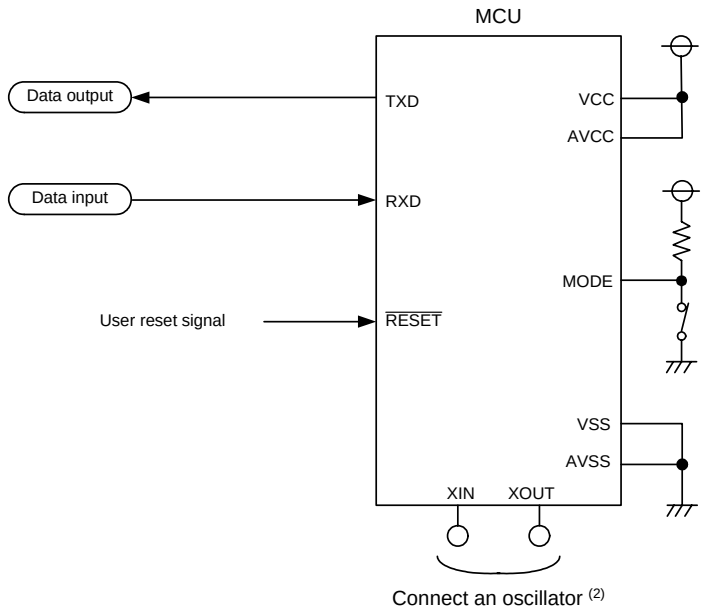
Table 30.8 lists the Pin Functions (Flash Memory Standard Serial I/O Mode 2) and Figure 30.17 shows Pin Handling in Standard Serial I/O Mode 2. Table 30.9 lists the Pin Functions (Flash Memory Standard Serial I/O Mode 3) and Figure 30.18 shows Pin Handling in Standard Serial I/O Mode 3.
After handling the pins shown in Table 30.9 and rewriting the flash memory using the programmer, apply a "H" level signal to the MODE pin and reset the hardware to run a program in the flash memory in single-chip mode.

30.5.1 ID Code Check Function

The ID code check function determines whether the ID codes sent from the serial programmer and those written in the flash memory match.
Refer to **12. ID Code Areas** for details of the ID code check.

Table 30.8 Pin Functions (Flash Memory Standard Serial I/O Mode 2)

Pin	Name	I/O	Description
VCC, VSS	Power supply input		Apply the guaranteed programming and erasure voltage to the VCC pin and 0 V to the VSS pin.
$\overline{\text{RESET}}$	Reset input	I	Reset input pin
P4_6/XIN	P4_6 input/clock input	I	Connect a ceramic resonator or crystal oscillator between pins XIN and XOUT.
P4_7/XOUT	P4_7 input/clock output	I/O	
P0_0 to P0_7	Input port P0	I	Input a “H” or “L” level signal or leave open.
P1_0 to P1_3, P1_6, P1_7	Input port P1	I	Input a “H” or “L” level signal or leave open.
P2_0 to P2_7	Input port P2	I	Input a “H” or “L” level signal or leave open.
P3_0 to P3_7	Input port P3	I	Input a “H” or “L” level signal or leave open.
P4_2/VREF, P4_3 to P4_5	Input port P4	I	Input a “H” or “L” level signal or leave open.
P5_0 to P5_7	Input port P5	I	Input a “H” or “L” level signal or leave open.
P6_0 to P6_7	Input port P6	I	Input a “H” or “L” level signal or leave open.
P7_0 to P7_7	Input port P7	I	Input a “H” or “L” level signal or leave open.
P8_0 to P8_7	Input port P8	I	Input a “H” or “L” level signal or leave open.
P9_0 to P9_5	Input port P9	I	Input a “H” or “L” level signal or leave open.
MODE	MODE	I/O	Input a “L” level signal.
P1_4	TXD output	O	Serial data output pin
P1_5	RXD input	I	Serial data input pin

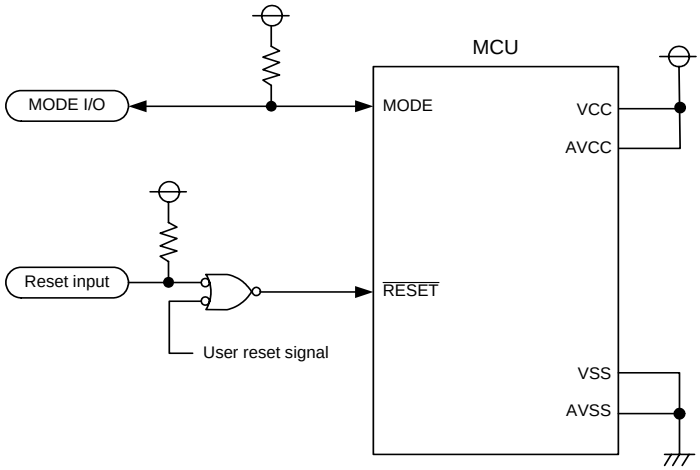


Notes:
1. In this example, modes are switched between single-chip mode and standard serial I/O mode by controlling the MODE input with a switch.
2. When operating with the on-chip oscillator clock, it is not necessary to connect an oscillation circuit. Refer to **Appendix Figure 2.1 Connection Example with M16C Flash Starter (M3A-0806)**.

Figure 30.17 Pin Handling in Standard Serial I/O Mode 2

Table 30.9 Pin Functions (Flash Memory Standard Serial I/O Mode 3)

Pin	Name	I/O	Description
VCC, VSS	Power supply input		Apply the guaranteed programming and erasure voltage to the VCC pin and 0 V to the VSS pin.
$\overline{\text{RESET}}$	Reset input	I	Reset input pin
P4_6/XIN	P4_6 input/clock input	I	If an external oscillator is connected, connect a ceramic resonator or crystal oscillator between pins XIN and XOUT. To use as an input port, input a “H” or “L” level signal or leave the pin open.
P4_7/XOUT	P4_7 input/clock output	I/O	
P0_0 to P0_7	Input port P0	I	Input a “H” or “L” level signal or leave open.
P1_0 to P1_7	Input port P1	I	Input a “H” or “L” level signal or leave open.
P2_0 to P2_7	Input port P2	I	Input a “H” or “L” level signal or leave open.
P3_0 to P3_7	Input port P3	I	Input a “H” or “L” level signal or leave open.
P4_2/VREF, P4_3 to P4_5	Input port P4	I	Input a “H” or “L” level signal or leave open.
P5_0 to P5_7	Input port P5	I	Input a “H” or “L” level signal or leave open.
P6_0 to P6_7	Input port P6	I	Input a “H” or “L” level signal or leave open.
P7_0 to P7_7	Input port P7	I	Input a “H” or “L” level signal or leave open.
P8_0 to P8_7	Input port P8	I	Input a “H” or “L” level signal or leave open.
P9_0 to P9_5	Input port P9	I	Input a “H” or “L” level signal or leave open.
MODE	MODE	I/O	Serial data I/O pin. Connect the pin to a programmer.



Notes:
1. Controlled pins and external circuits vary depending on the programmer. Refer to the programmer manual for details.
2. In this example, modes are switched between single-chip mode and standard serial I/O mode by connecting a programmer.
3. When operating with the on-chip oscillator clock, it is not necessary to connect an oscillation circuit.

Figure 30.18 Pin Handling in Standard Serial I/O Mode 3

30.6 Parallel I/O Mode

Parallel I/O mode is used to input and output software commands, addresses and data necessary to control (read, program, and erase) the on-chip flash memory.
Use a parallel programmer which supports the MCU. Contact the parallel programmer manufacturer for more information. Refer to the user's manual included with your parallel programmer for instructions.
In parallel I/O mode, the user ROM areas shown in Figure 30.1 can be rewritten.

30.6.1 ROM Code Protect Function

The ROM code protect function prevents the flash memory from being read and rewritten. (Refer to the **30.3.2 ROM Code Protect Function**.)

30.7 Notes on Flash Memory

30.7.1 CPU Rewrite Mode

30.7.1.1 Prohibited Instructions

The following instructions cannot be used while the program ROM area is being rewritten in EW0 mode because they reference data in the flash memory: UND, INTO, and BRK.

30.7.1.2 Interrupts

Tables 30.10 to 30.12 show CPU Rewrite Mode Interrupts (1), (2) and (3), respectively.

Table 30.10 CPU Rewrite Mode Interrupts (1)

Mode	Erase/ Write Target	Status	Maskable Interrupt
EW0	Data flash (1)	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request). The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0 (erase-suspend request disabled by interrupt request), set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit to 0 (erase restart).
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.
		During auto-programming	
	Program ROM	During auto-erasure (suspend enabled)	Usable by allocating a vector in RAM.
		During auto-erasure (suspend disabled)	
		During auto-programming	
EW1	Data flash (1)	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1, the FMR21 bit is automatically set to 1. The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0, set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit to 0.
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.
		During auto-programming	
	Program ROM	During auto-erasure (suspend enabled)	Auto-erasure suspends after td(SR-SUS) and interrupt handling is executed. Auto-erasure can be restarted by setting the FMR21 bit to 0 after interrupt handling completes. While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written.
		During auto-erasure (suspend disabled or FMR22 = 0)	Auto-erasure and auto-programming have priority and interrupt requests are put on standby. Interrupt handling is executed after auto-erase and auto-program complete.
		During auto-programming	

FMR21, FMR22: Bits in FMR2 register

Note:

1. The R8C/38W Group and R8C/38Y Group have data flash.

Table 30.11 CPU Rewrite Mode Interrupts (2)

<table>
<tr><td>Mode</td><td>Erase/ Write Target</td><td>Status</td><td>• Watchdog Timer
• Oscillation Stop Detection
• Voltage Monitor 2
• Voltage Monitor 1</td><td>• Undefined Instruction
• INTO Instruction
• BRK Instruction
• Single Step
• Address Match
• Address Break (Note 1)</td></tr>
<tr><td rowspan="5">EW0</td><td rowspan="3">Data flash (2)</td><td>During auto-erasure (suspend enabled)</td><td>When an interrupt request is acknowledged, interrupt handling is executed.
If the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request). The flash memory suspends auto-erasure after td(SR-SUS).
If erase-suspend is required while the FMR22 bit is set to 0 (erase-suspend request disabled by interrupt request), set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS).
While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit is set to 0 (erase restart).</td><td>When an interrupt request is acknowledged, interrupt handling is executed.
If erase-suspend is required, set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS).
While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written.
Auto-erasure can be restarted by setting the FMR21 bit in the FMR2 register is set to 0 (erase restart).</td></tr>
<tr><td>During auto-erasure (suspend disabled or FMR22 = 0)</td><td colspan="2" rowspan="2">Interrupt handling is executed while auto-erasure or auto-programming is being performed.</td></tr>
<tr><td>During auto-programming</td></tr>
<tr><td rowspan="3">Program ROM</td><td>During auto-erasure (suspend enabled)</td><td rowspan="3">When an interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts when the flash memory restarts after the fixed period.
Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. After the flash memory restarts, execute auto-erasure again and ensure it completes normally.
The watchdog timer does not stop during the command operation, so interrupt requests may be generated. Initialize the watchdog timer regularly using the erase-suspend function.</td><td rowspan="3">Not usable during auto-erasure or auto-programming.</td></tr>
<tr><td>During auto-erasure (suspend disabled)</td></tr>
<tr><td>During auto-programming</td></tr>
</table>

FMR21, FMR22: Bits in FMR2 register

Notes:
1. Do not use a non-maskable interrupt while block 0 is being auto-erased because the fixed vector is allocated in block 0.
2. The R8C/38W Group and R8C/38Y Group have data flash.

Table 30.12 CPU Rewrite Mode Interrupts (3)

Mode	Erase/ Write Target	Status	• Watchdog Timer • Oscillation Stop Detection • Voltage Monitor 2 • Voltage Monitor 1	• Undefined Instruction • INTO Instruction • BRK Instruction • Single Step • Address Match • Address Break (Note 1)
EW1	Data flash (2)	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1, the FMR21 bit is automatically set to 1. The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0, set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-programming after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit is set to 0.	When an interrupt request is acknowledged, interrupt handling is executed. If erase-suspend is required, set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit in the FMR2 register is set to 0 (erase restart).
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.	
		During auto-programming		
	Program ROM	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts when the flash memory restarts after the fixed period. Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. After the flash memory restarts, execute auto-erasure again and ensure it completes normally. The watchdog timer does not stop during the command operation, so interrupt requests may be generated. Initialize the watchdog timer regularly using the erase-suspend function.	Not usable during auto-erasure or auto-programming.
		During auto-erasure (suspend disabled or FMR22 = 0)		
		During auto-programming		

FMR21, FMR22: Bits in FMR2 register

Notes:
1. Do not use a non-maskable interrupt while block 0 is being auto-erased because the fixed vector is allocated in block 0.
2. The R8C/38W Group and R8C/38Y Group have data flash.

30.7.1.3 How to Access

To set one of the following bits to 1, first write 0 and then 1 immediately. Disable interrupts and DTC activation between writing 0 and writing 1.

- The FMR01 bit or FMR02 bit in the FMR0 register
- The FMR13 bit in the FMR1 register
- The FMR20 bit, FMR22 bit, or FMR 27 bit in the FMR2 register

To set one of the following bits to 0, first write 1 and then 0 immediately. Disable interrupts and DTC activation between writing 0 and writing 1.

- The FMR14 bit, FMR15 bit, FMR16 bit, or FMR17 bit in the FMR1 register

30.7.1.4 Rewriting User ROM Area

In EW0 mode, if the supply voltage drops while rewriting any block in which a rewrite control program is stored, it may not be possible to rewrite the flash memory because the rewrite control program cannot be rewritten correctly. In this case, use standard serial I/O mode.

30.7.1.5 Programming

Do not write additions to the already programmed address.

30.7.1.6 Entering Stop Mode or Wait Mode

Do not enter stop mode or wait mode during erase-suspend.
If the FST7 bit in the FST register is set to 0 (busy (during programming or erasure execution), do not enter to stop mode or wait mode.
Do not enter stop mode or wait mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

30.7.1.7 Note when data flash is used [R8C/38W Group, R8C/38Y Group]

To use data flash with more than 16 MHz CPU clock, set the FMR23 bit in the FMR2 register to 1 (4 cycles of the CPU clock).

30.7.1.8 Block Blank Check

Do not execute the block blank check command during erase-suspend.

30.7.1.9 Low-Current-Consumption Read Mode

In low-speed on-chip oscillator mode, the current consumption when reading the flash memory can be reduced by setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled).
When the CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16, low-consumption-current read mode can be used. When divided by 1 (no division) or divided by 2 is set, do not use low-consumption-current read mode. After setting the divide ratio of the CPU clock, set the FMR27 bit to 1 (low-current-consumption read mode enabled).
To reduce the power consumption, refer to **31. Reducing Power Consumption**.
Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).
Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

31. Reducing Power Consumption

31.1 Overview

This chapter describes key points and processing methods for reducing power consumption.

31.2 Key Points and Processing Methods for Reducing Power Consumption

Key points for reducing power consumption are shown below. They should be referred to when designing a system or creating a program.

31.2.1 Voltage Detection Circuit

If voltage monitor 1 is not used, set the VCA26 bit in the VCA2 register to 0 (voltage detection 1 circuit disabled). If voltage monitor 2 is not used, set the VCA27 bit in the VCA2 register to 0 (voltage detection 2 circuit disabled).
If the power-on reset and voltage monitor 0 reset are not used, set the VCA25 bit in the VCA2 register to 0 (voltage detection 0 circuit disabled).

31.2.2 Ports

Even after the MCU enters wait mode or stop mode, the states of the I/O ports are retained. Current flows into the output ports in the active state, and shoot-through current flows into the input ports in the high-impedance state. Unnecessary ports should be set to input and fixed to a stable electric potential before the MCU enters wait mode or stop mode.

31.2.3 Clocks

Power consumption generally depends on the number of the operating clocks and their frequencies. The fewer the number of operating clocks or the lower their frequencies, the more power consumption decreases.
Unnecessary clocks should be stopped accordingly.

Stopping low-speed on-chip oscillator oscillation: CM14 bit in CM1 register
Stopping high-speed on-chip oscillator oscillation: FRA00 bit in FRA0 register

31.2.4 Wait Mode, Stop Mode

Power consumption can be reduced in wait mode and stop mode. Refer to **9.6 Power Control** for details.

31.2.5 Stopping Peripheral Function Clocks

If the peripheral function f1, f2, f4, f8, and f32 clocks are not necessary in wait mode, set the CM02 bit in the CM0 register to 1 (peripheral function clock stops in wait mode). This will stop the f1, f2, f4, f8, and f32 clocks in wait mode.

31.2.6 Timers

If timer RAi (i = 0 or 1) is not used, set the TCKCUT bit in the TRAiMR (i = 0 or 1) register to 1 (count source cutoff).
If timer RB is not used, set the TCKCUT bit in the TRBMR register to 1 (count source cutoff).
If timer RC is not used, set the MSTTRC bit in the MSTCR register to 1 (standby).
If timer RD is not used, set bits TCK2 to TCK0 in the TRDCRi (i = 0 to 1) register to 000b and the MSTTRD bit in the MSTCR register to 1 (standby).
If timer RG is not used, set the MSTTRG bit in the MSTCR register to 1 (standby).

31.2.7 A/D Converter

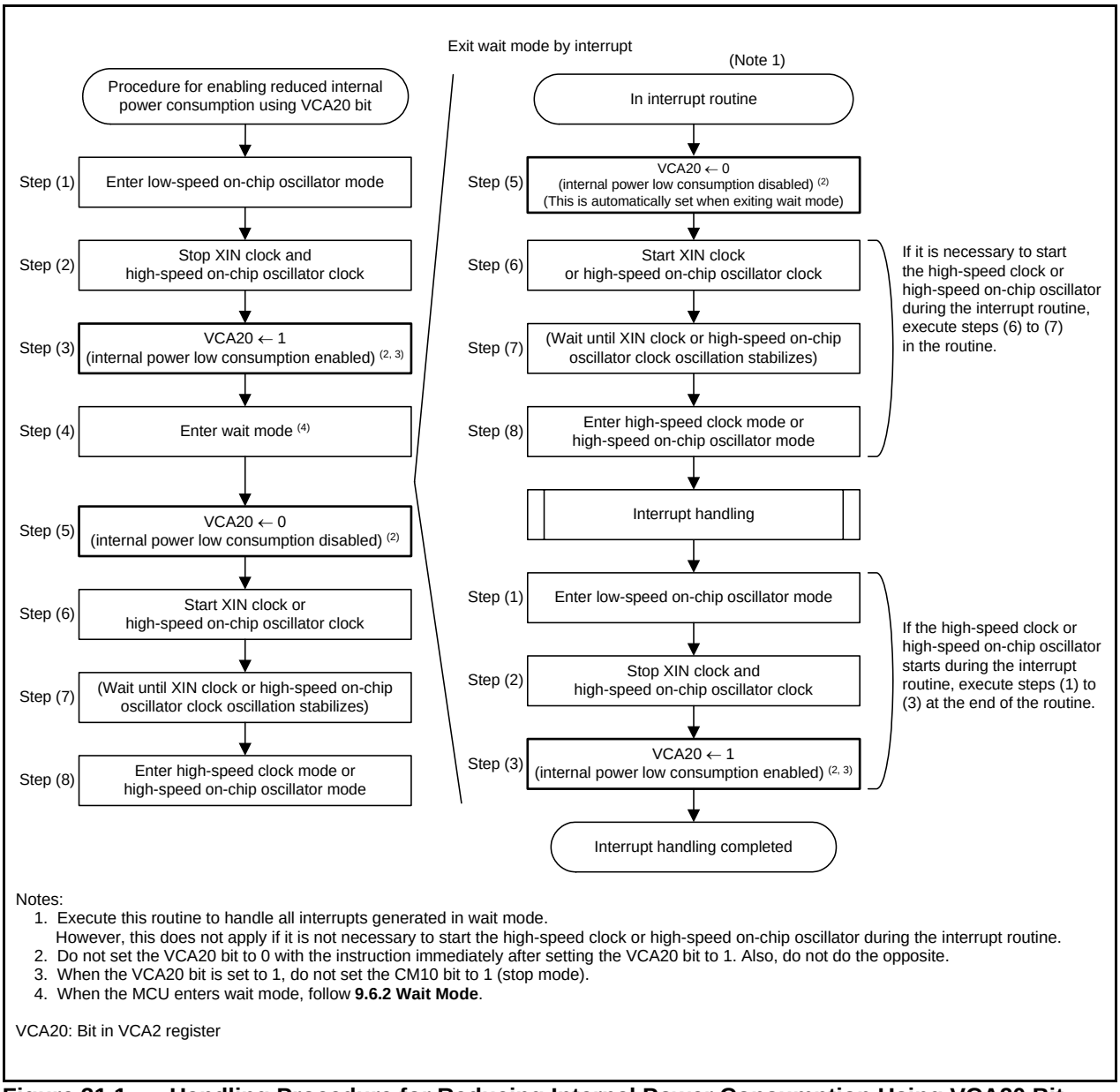
When the A/D converter is not used, power consumption can be reduced by setting the ADSTBY bit in the ADCON1 register to 0 (A/D operation stops (standby)) to shut off any analog circuit current flow.

31.2.8 Clock Synchronous Serial Interface

When the SSU or the I^2C bus is not used, set the MSTIIC bit in the MSTCR register to 1 (standby).

31.2.9 Reducing Internal Power Consumption

When the MCU enters wait mode using low-speed on-chip oscillator mode, internal power consumption can be reduced by using the VCA20 bit in the VCA2 register. Figure 31.1 shows the Handling Procedure for Reducing Internal Power Consumption Using VCA20 Bit. To enable reduced internal power consumption by the VCA20 bit, follow Figure 31.1 Handling Procedure for Reducing Internal Power Consumption Using VCA20 Bit.



Notes:
1. Execute this routine to handle all interrupts generated in wait mode.
   However, this does not apply if it is not necessary to start the high-speed clock or high-speed on-chip oscillator during the interrupt routine.
2. Do not set the VCA20 bit to 0 with the instruction immediately after setting the VCA20 bit to 1. Also, do not do the opposite.
3. When the VCA20 bit is set to 1, do not set the CM10 bit to 1 (stop mode).
4. When the MCU enters wait mode, follow **9.6.2 Wait Mode**.

VCA20: Bit in VCA2 register

Figure 31.1 Handling Procedure for Reducing Internal Power Consumption Using VCA20 Bit

31.2.10 Stopping Flash Memory

In low-speed on-chip oscillator mode, power consumption can be further reduced by stopping the flash memory using the FMSTP bit in the FMR0 register.

Access to the flash memory is disabled by setting the FMSTP bit to 1 (flash memory stops). The FMSTP bit must be written to by a program transferred to RAM.

When the MCU enters stop mode or wait mode while CPU rewrite mode is disabled, the power for the flash memory is automatically turned off. It is turned back on again after the MCU exits stop mode or wait mode. This eliminates the need to set the FMR0 register.

Figure 31.2 shows the Handling Procedure Example for Reducing Power Consumption Using FMSTP Bit.

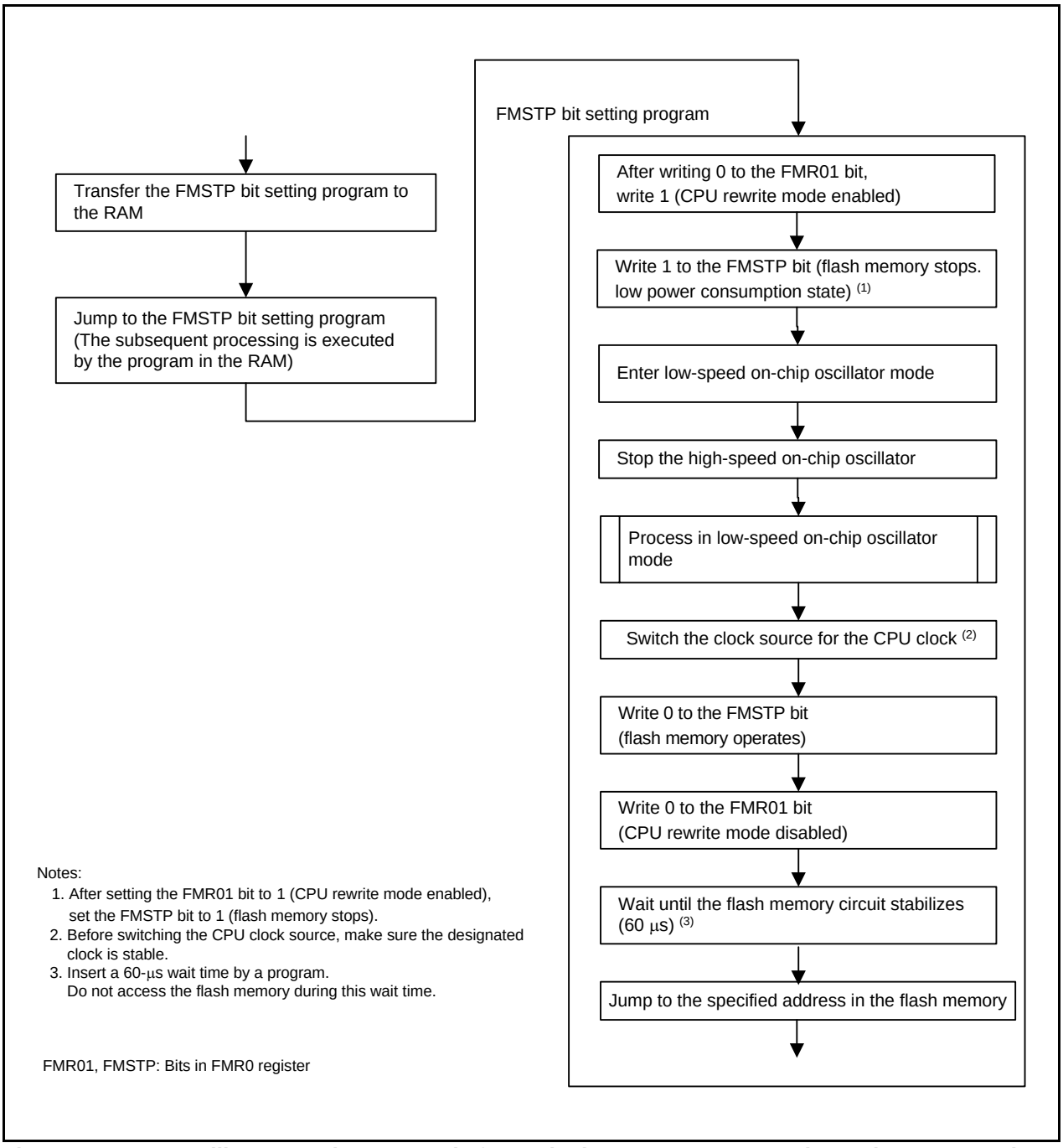
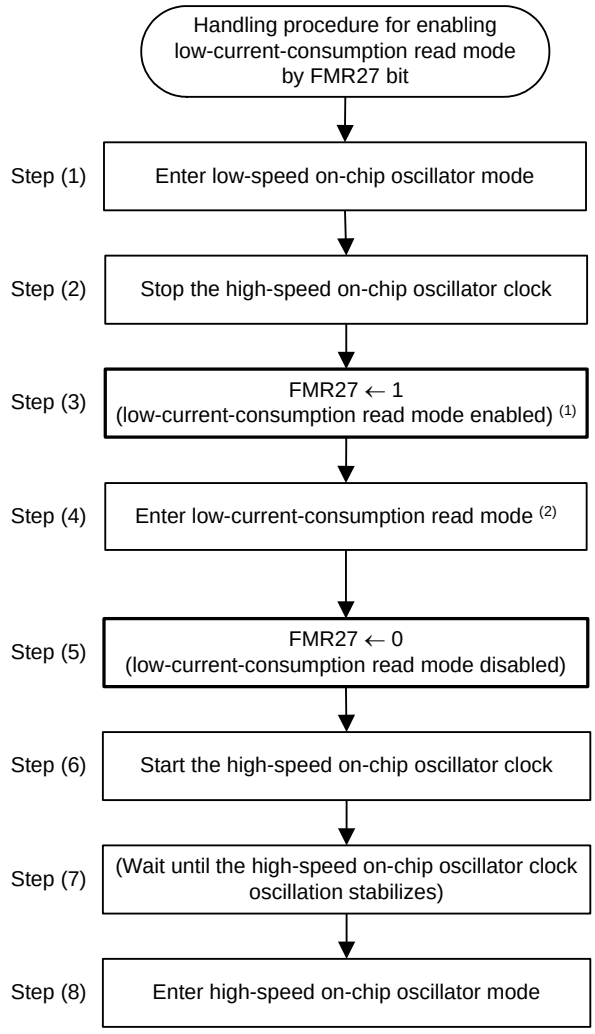


Figure 31.2 Handling Procedure Example for Reducing Power Consumption Using FMSTP Bit

31.2.11 Low-Current-Consumption Read Mode

In low-speed on-chip oscillator mode, the current consumption when reading the flash memory can be reduced by setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled).
When the CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16, low-consumption-current read mode can be used. When divided by 1 (no division) or divided by 2 is set, do not use low-consumption-current read mode. After setting the divide ratio of the CPU clock, set the FMR27 bit to 1 (low-current-consumption read mode enabled).
Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).
Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).
Figure 31.3 shows the Handling Procedure Example of Low-Current-Consumption Read Mode.



Notes:
1. To set the FMR27 bit to 1, first write 0 and then write 1 immediately.
   Disable interrupts and DTC activation between writing 0 and writing 1.
2. In low-current-consumption read mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled).
   Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).
   Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

FMR27: Bit in FMR2 register

Figure 31.3 Handling Procedure Example of Low-Current-Consumption Read Mode

32. Electrical Characteristics

Table 32.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V_{CC}/AV_{CC}	Supply voltage		–0.3 to 6.5	V
V_I	Input voltage (1)		–0.3 to V_{CC} + 0.3	V
IIN	Input current (1)	(2, 3, 4)	–4 to 4	mA
V_O	Output voltage		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation	–40 °C ≤ T_{opr} < 85 °C	300	mW
		85 °C ≤ T_{opr} < 125 °C	125	mW
T_{opr}	Operating ambient temperature		–40 to 85 (J version) / –40 to 125 (K version)	°C
T_{stg}	Storage temperature		–65 to 150	°C

Notes:
1. Meet the specified range for the input voltage or the input current.
2. Applicable ports: P0 to P3, P4_3 to P4_5, P5 to P8, P9_0 to P9_5
3. The total input current must be 12 mA or less.
4. Even if no voltage is supplied to Vcc, the input current may cause the MCU to be powered on and operate. When a voltage is supplied to Vcc, the input current may cause the supply voltage to rise. Since operations in any cases other than above are not guaranteed, use the power supply circuit in the system to ensure the supply voltage for the MCU is stable within the specified range.

Table 32.2 Recommended Operating Conditions (1)

Symbol	Parameter				Conditions	Standard			Unit
						Min.	Typ.	Max.	
V_{CC}/AV_{CC}	Supply voltage					2.7	–	5.5	V
V_{SS}/AV_{SS}	Supply voltage					–	0	–	V
V_{IH}	Input “H” voltage	Other than CMOS input				0.8 V_{CC}	–	V_{CC}	V
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0.5 V_{CC}	–	V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0.55 V_{CC}	–	V_{CC}	V
				Input level selection : 0.5 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0.65 V_{CC}	–	V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0.7 V_{CC}	–	V_{CC}	V
				Input level selection : 0.7 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0.85 V_{CC}	–	V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0.85 V_{CC}	–	V_{CC}	V
		External clock input (XOUT)				1.2	–	V_{CC}	V
V_{IL}	Input “L” voltage	Other than CMOS input				0	–	0.2 V_{CC}	V
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0	–	0.2 V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0	–	0.2 V_{CC}	V
				Input level selection : 0.5 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0	–	0.4 V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0	–	0.3 V_{CC}	V
				Input level selection : 0.7 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0	–	0.55 V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0	–	0.45 V_{CC}	V
		External clock input (XOUT)				0	–	0.4	V
$I_{OH(sum)}$	Peak sum output “H” current	Sum of all pins $I_{OH(peak)}$				–	–	–80	mA
$I_{OH(sum)}$	Average sum output “H” current	Sum of all pins $I_{OH(avg)}$				–	–	–40	mA
$I_{OH(peak)}$	Peak output “H” current					–	–	–10	mA
$I_{OH(avg)}$	Average output “H” current					–	–	–5	mA
$I_{OL(sum)}$	Peak sum output “L” current	Sum of all pins $I_{OL(peak)}$				–	–	80	mA
$I_{OL(sum)}$	Average sum output “L” current	Sum of all pins $I_{OL(avg)}$				–	–	40	mA
$I_{OL(peak)}$	Peak output “L” current					–	–	10	mA
$I_{OL(avg)}$	Average output “L” current					–	–	5	mA
$f_{(XIN)}$	XIN clock input oscillation frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	20	MHz
fOCO40M	Count source for timer RC, timer RD, or timer RG				2.7 V ≤ V_{CC} ≤ 5.5 V	32	–	40	MHz
fOCO-F	fOCO-F frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	20	MHz
–	System clock frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	20	MHz
$f_{(BCLK)}$	CPU clock frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	20	MHz

Notes:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = –40 to 85°C (J version) / –40 to 125°C (K version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

Table 32.3 Recommended Operating Conditions (2)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
$I_{IC(H)}$	High input injection current	P0 to P3, P4_3 to P4_5, P5 to P8, P9_0 to P9_5	$V_I > V_{CC}$	–	–	2	mA
$I_{IC(L)}$	Low input injection current	P0 to P3, P4_3 to P4_5, P5 to P8, P9_0 to P9_5	$V_I < V_{SS}$	–	–	–2	mA
$\Sigma\|I_{IC}\|$	Total injection current			–	–	8	mA

Note:
1. V_{CC} = 4.5 to 5.5 V at T_{opr} = –40 to 85°C (J version) / –40 to 125°C (K version), unless otherwise specified.

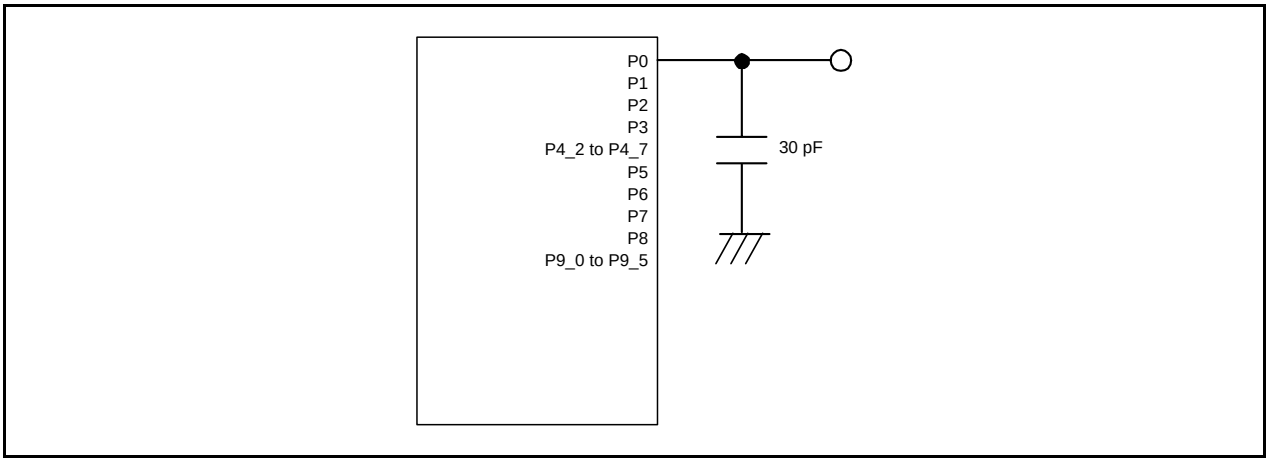


Figure 32.1 Ports P0 to P3, P4_2 to P4_7, P5 to P8, and P9_0 to P9_5 Timing Measurement Circuit

Table 32.4 A/D Converter Characteristics

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
–	Resolution		V_{ref} = AV_{CC}		–	–	10	Bit
–	Absolute accuracy	10-bit mode	V_{ref} = AV_{CC} = 5.0 V	AN0 to AN7 input, AN8 to AN11 input, AN12 to AN19 input	–	–	±3	LSB
			V_{ref} = AV_{CC} = 3.0 V	AN0 to AN7 input, AN8 to AN11 input, AN12 to AN19 input	–	–	±5	LSB
		8-bit mode	V_{ref} = AV_{CC} = 5.0 V	AN0 to AN7 input, AN8 to AN11 input, AN12 to AN19 input	–	–	±2	LSB
			V_{ref} = AV_{CC} = 3.0 V	AN0 to AN7 input, AN8 to AN11 input, AN12 to AN19 input	–	–	±2	LSB
ϕAD	A/D conversion clock		4.0 ≤ V_{ref} = AV_{CC} = ≤ 5.5 (2)		2	–	20	MHz
			2.7 ≤ V_{ref} = AV_{CC} = ≤ 5.5 (2)		2	–	10	MHz
–	Tolerance level impedance				–	3	–	kΩ
I_{vref}	V_{ref} current		V_{CC} = 5.0 V, XIN = f1 = ϕAD = 20 MHz		–	45	–	µA
t_{CONV}	Conversion time	10-bit mode	V_{ref} = AV_{CC} = 5.0 V, ϕAD = 20 MHz		2.2	–	–	µs
		8-bit mode	V_{ref} = AV_{CC} = 5.0 V, ϕAD = 20 MHz		2.2	–	–	µs
t_{SAMP}	Sampling time		ϕAD = 20 MHz		0.8	–	–	µs
V_{ref}	Reference voltage				2.7	–	AV_{CC}	V
V_{IA}	Analog input voltage (3)				0	–	V_{ref}	V
OCVREF	On-chip reference voltage		2 MHz ≤ ϕAD ≤ 4 MHz		1.14	1.34	1.54	V

Notes:
1. V_{CC}/AV_{CC} = V_{ref} = 2.7 to 5.5 V, V_{SS} = 0 V at T_{opr} = –40 to 85°C (J version) / –40 to 125°C (K version), unless otherwise specified.
2. The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-consumption current mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 32.5 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance (2)	R8C/38X, R8C/38Z Group	100 (3)	–	–	times
		R8C/38W, R8C/38Y Group	1,000 (3)	–	–	times
–	Byte program time (program/erase endurance ≤ 100 times)		–	60	300	µs
–	Byte program time (program/erase endurance > 100 times)		–	60	500	µs
–	Word program time (program/erase endurance ≤ 100 times)		–	100	400	µs
–	Word program time (program/erase endurance > 100 times)		–	100	650	µs
–	Block erase time		–	0.3	4	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	5+CPU clock × 3 cycles	ms
–	Interval from erase start/restart until following suspend request		0	–	–	µs
–	Time from suspend until erase restart		–	–	30+CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly terminated until reading is enabled		–	–	30+CPU clock × 1 cycle	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.7	–	5.5	V
–	Program, erase temperature		–40	–	85 (J version) 125 (K version)	°C
–	Data hold time (7)	Ambient temperature = 55°C (8)	20	–	–	year

Notes:
1. VCC = 2.7 to 5.5 V at Topr = -40 to 85°C (J version) / -40 to 125°C (K version) (under consideration), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100, 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.
8. This data hold time includes 3,000 hours in Ta = 125°C and 7,000 hours in Ta = 85°C.

Table 32.6 Flash Memory (Data flash Block A to Block D) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance (2)		10,000 (3)	–	–	times
–	Byte program time (program/erase endurance ≤ 1,000 times)		–	160	950	µs
–	Byte program time (program/erase endurance > 1,000 times)		–	300	950	µs
–	Block erase time (program/erase endurance ≤ 1,000 times)		–	0.2	1	s
–	Block erase time (program/erase endurance > 1,000 times)		–	0.3	1	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	3+CPU clock × 3 cycles	ms
–	Interval from erase start/restart until following suspend request		0	–	–	µs
–	Time from suspend until erase restart		–	–	30+CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly terminated until reading is enabled		–	–	30+CPU clock × 1 cycle	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.7	–	5.5	V
–	Program, erase temperature		–40	–	85 (J version) 125 (K version)	°C
–	Data hold time (7)	Ambient temperature = 55 °C (8)	20	–	–	year

Notes:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = –40 to 85°C (J version) / –40 to 125°C (K version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100, 1,000, 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.
8. This data hold time includes 3,000 hours in Ta = 125°C and 7,000 hours in Ta = 85°C.

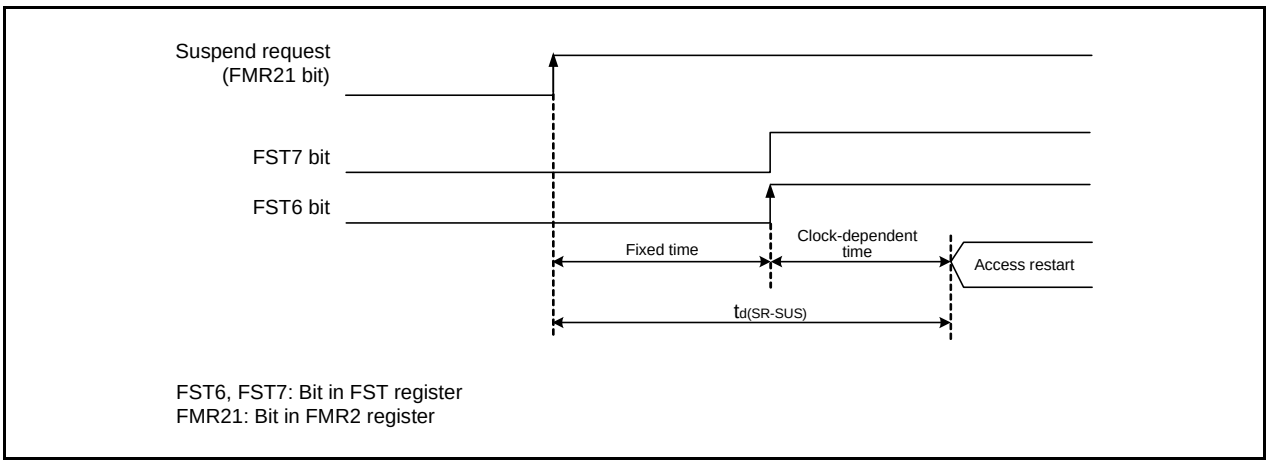


Figure 32.2 Time delay until Suspend

Table 32.7 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level	At the falling of V_{CC}	2.70	2.85	3.00	V
–	Voltage detection 0 circuit response time (3)	At the falling of Vcc from 5 V to (Vdet0 – 0.1) V	–	6	150	µs
–	Voltage detection circuit self power consumption	VCA25 = 1, V_{CC} = 5.0 V	–	1.5	–	µA
$t_{d(E-A)}$	Wait time until voltage detection circuit operation starts (2)		–	–	100	µs

Notes:
1. The measurement condition is V_{CC} = 2.7 V to 5.5 V and T_{opr} = –40 to 85°C (J version) / –40 to 125°C (K version).
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
3. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.

Table 32.8 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level Vdet1_7 (2)	At the falling of V_{CC}	3.05	3.25	3.45	V
	Voltage detection level Vdet1_8 (2)	At the falling of V_{CC}	3.20	3.40	3.60	V
	Voltage detection level Vdet1_9 (2)	At the falling of V_{CC}	3.35	3.55	3.75	V
	Voltage detection level Vdet1_A (2)	At the falling of V_{CC}	3.50	3.70	3.90	V
	Voltage detection level Vdet1_B (2)	At the falling of V_{CC}	3.65	3.85	4.05	V
	Voltage detection level Vdet1_C (2)	At the falling of V_{CC}	3.80	4.00	4.20	V
	Voltage detection level Vdet1_D (2)	At the falling of V_{CC}	3.95	4.15	4.35	V
	Voltage detection level Vdet1_E (2)	At the falling of V_{CC}	4.10	4.30	4.50	V
–	Hysteresis width at the rising of Vcc in voltage detection 1 circuit		–	0.1	–	V
–	Voltage detection 1 circuit response time (3)	At the falling of Vcc from 5 V to (Vdet1_7 – 0.1) V	–	60	150	µs
–	Voltage detection circuit self power consumption	VCA26 = 1, V_{CC} = 5.0 V	–	1.7	–	µA
$t_{d(E-A)}$	Wait time until voltage detection circuit operation starts (4)		–	–	100	µs

Notes:
1. The measurement condition is V_{CC} = 2.7 V to 5.5 V and T_{opr} = –40 to 85°C (J version) / –40 to 125°C (K version).
2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 32.9 Voltage Detection 2 Circuit Electrical Characteristics

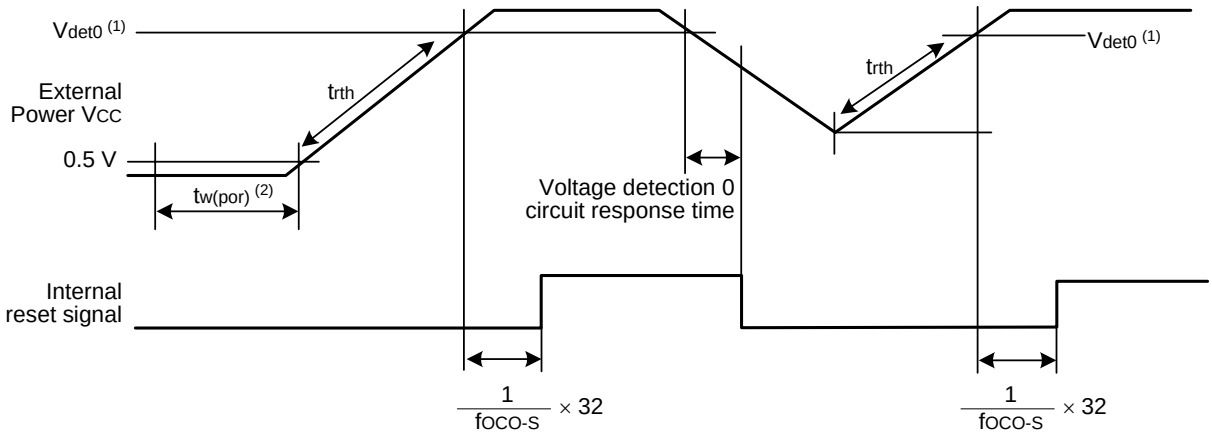
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage detection level Vdet2	At the falling of V_{CC}	3.80	4.00	4.20	V
–	Hysteresis width at the rising of Vcc in voltage detection 2 circuit		–	0.1	–	V
–	Voltage detection 2 circuit response time (2)	At the falling of Vcc from 5 V to (Vdet2 – 0.1) V	–	20	150	µs
–	Voltage detection circuit self power consumption	VCA26 = 1, V_{CC} = 5.0 V	–	1.7	–	µA
$t_{d(E-A)}$	Wait time until voltage detection circuit operation starts (3)		–	–	100	µs

Notes:
1. The measurement condition is V_{CC} = 2.7 V to 5.5 V and T_{opr} = –40 to 85°C (J version) / –40 to 125°C (K version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 32.10 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics(2)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{rth}	External power V_{CC} rise gradient	(1)	0	–	50000	mV/msec

Notes:
1. The measurement condition is V_{CC} = 2.7 V to 5.5 V and T_{opr} = –40 to 85°C (J version) / –40 to 125°C (K version).
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.



Notes:
1. Vdet0 indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** for details.
2. tw(por) indicates the duration the external power VCC must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain tw(por) for 1 ms or more.

Figure 32.3 Power-on Reset Circuit Electrical Characteristics

Table 32.11 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
–	High-speed on-chip oscillator frequency after reset	V_{CC} = 2.7 to 5.5 V, –40°C ≤ T_{opr} ≤ 85°C (J version) / –40°C ≤ T_{opr} ≤ 125°C (K version)	–	40	–	MHz
	High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register (3)		–	36.864	–	MHz
	High-speed on-chip oscillator frequency when the FRA6 register correction value is written into the FRA1 register and the FRA7 register correction value into the FRA3 register		–	32	–	MHz
	High-speed on-chip oscillator frequency temperature • supply voltage dependence (2)		–5	–	5	%
–	Oscillation stabilization time		–	200	–	µs
–	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25°C	–	400	–	µA

Notes:
1. The measurement condition is V_{CC} = 2.7 to 5.5 V and T_{opr} = –40 to 85°C (J version) / –40 to 125°C (K version).
2. This indicates the precision error for the oscillation frequency of the high-speed on-chip oscillator.
3. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 32.12 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		112.5	125	137.5	kHz
fOCO-WDT	Low-speed on-chip oscillator frequency for watchdog timer		112.5	125	137.5	kHz
–	Oscillation stabilization time	V_{CC} = 5.0 V, T_{opr} = 25°C	–	30	100	µs
–	Self power consumption at oscillation	V_{CC} = 5.0 V, T_{opr} = 25°C	–	3	–	µA

Note:
1. The measurement condition is V_{CC} = 2.7 to 5.5 V and T_{opr} = –40 to 85°C (J version) / –40 to 125°C (K version).

Table 32.13 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on (2)		–	–	2000	µs

Notes:
1. The measurement condition is V_{CC} = 2.7 to 5.5 V and T_{opr} = –40 to 85°C (J version) / –40 to 125°C (K version).
2. Wait time until the internal power supply generation circuit stabilizes during power-on.

Table 32.14 Timing Requirements of SSU (1)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	–	–	t_{CYC} (2)
t_{HI}	SSCK clock “H” width			0.4	–	0.6	t_{SUCYC}
t_{LO}	SSCK clock “L” width			0.4	–	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		–	–	1	t_{CYC} (2)
		Slave		–	–	1	µs
t_{FALL}	SSCK clock falling time	Master		–	–	1	t_{CYC} (2)
		Slave		–	–	1	µs
t_{SU}	SSO, SSI data input setup time			100	–	–	ns
t_{H}	SSO, SSI data input hold time			1	–	–	t_{CYC} (2)
t_{LEAD}	$\overline{SCS}$ setup time	Slave		$1t_{CYC}$ + 50	–	–	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		$1t_{CYC}$ + 50	–	–	ns
t_{OD}	SSO, SSI data output delay time			–	–	1	t_{CYC} (2)
t_{SA}	SSI slave access time		2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	$1.5t_{CYC}$ + 100	ns
t_{OR}	SSI slave out open time		2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	$1.5t_{CYC}$ + 100	ns

Notes:
1. The measurement condition is V_{CC} = 2.7 to 5.5 V and T_{opr} = –40 to 85°C (J version) / –40 to 125°C (K version).
2. $1t_{CYC}$ = 1/f1(s)

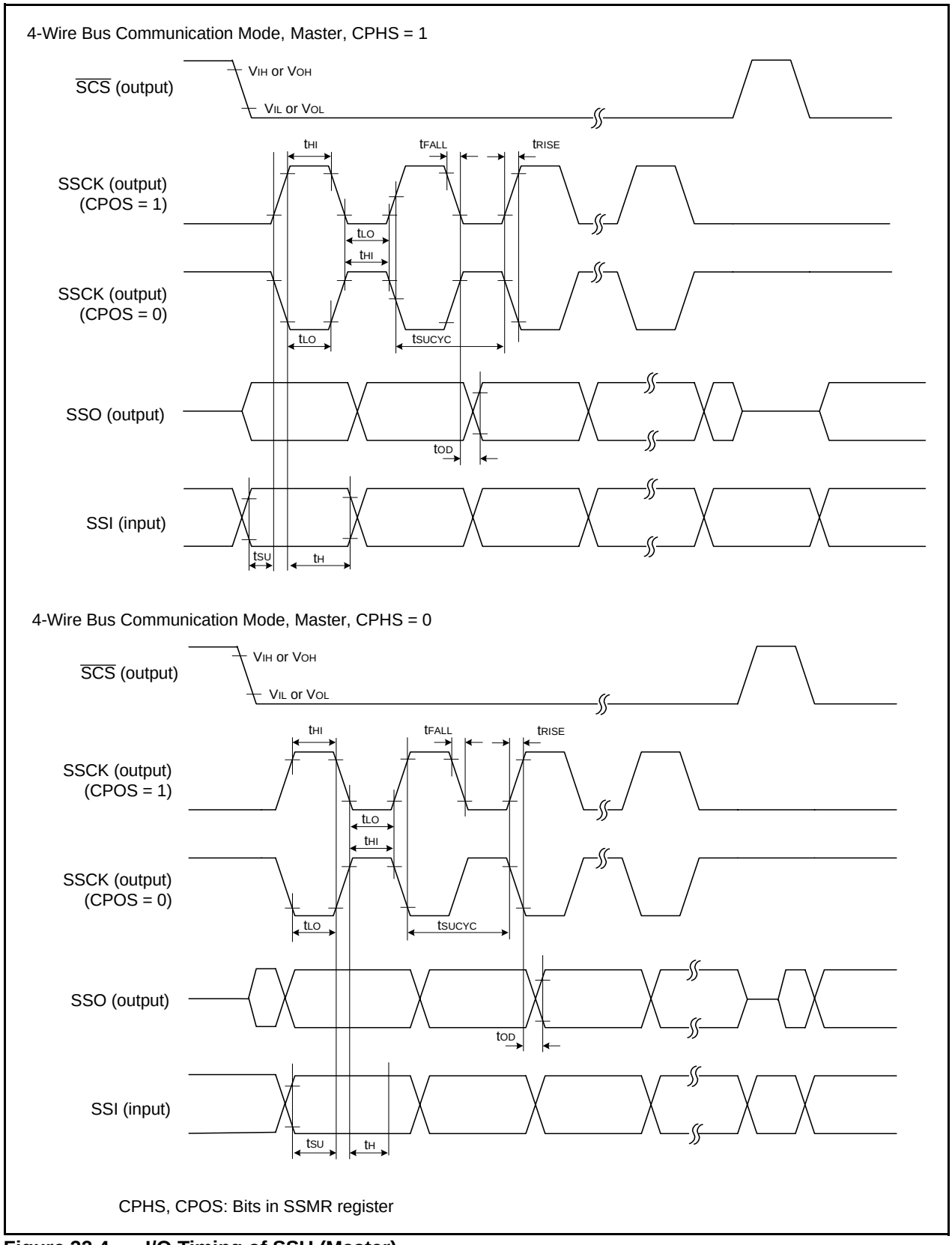
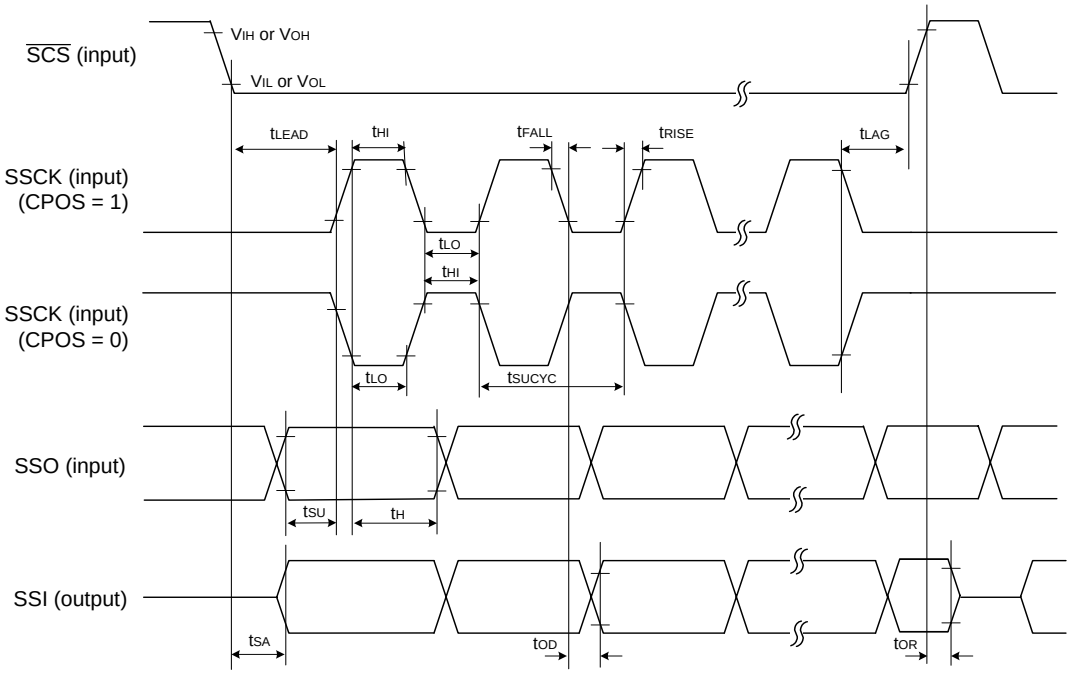
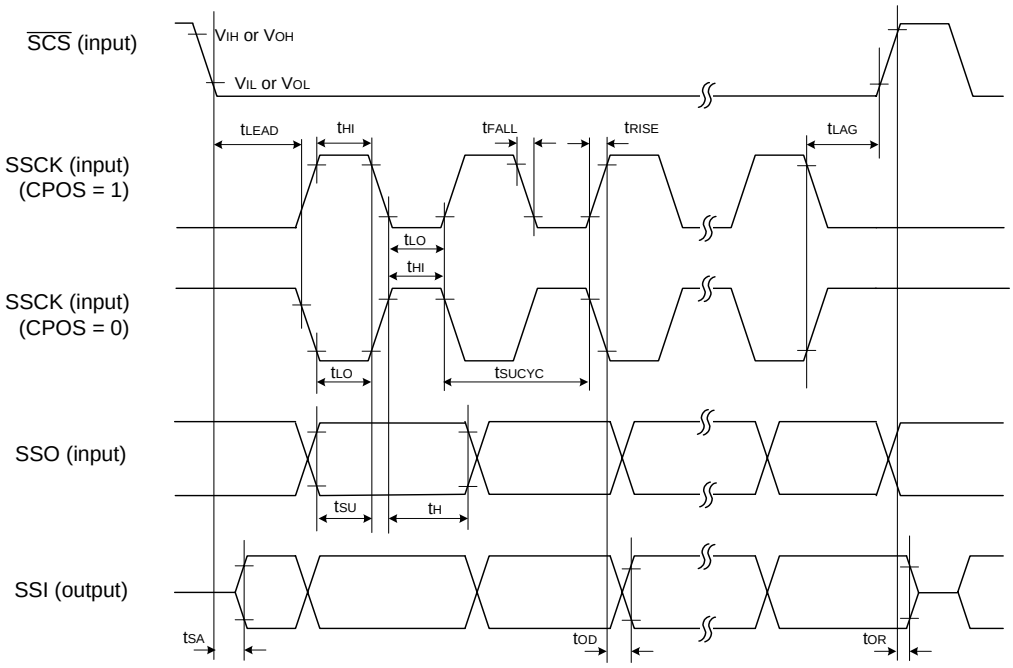


Figure 32.4 I/O Timing of SSU (Master)

4-Wire Bus Communication Mode, Slave, CPHS = 1



4-Wire Bus Communication Mode, Slave, CPHS = 0



CPHS, CPOS: Bits in SSMR register

Figure 32.5 I/O Timing of SSU (Slave)

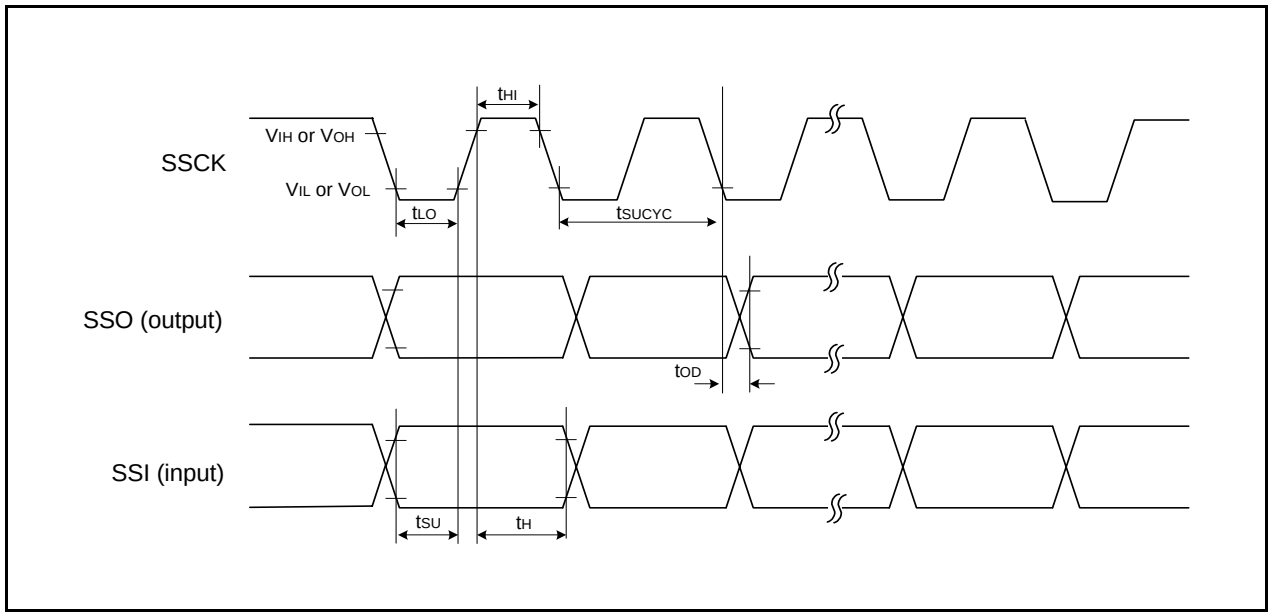


Figure 32.6 I/O Timing of SSU (Clock Synchronous Communication Mode)

Table 32.15 Electrical Characteristics (1) [4.2 V ≤ Vcc ≤ 5.5 V]

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Other than XOUT	I_{OH} = –5 mA	V_{CC} – 2.0	–	V_{CC}	V
			I_{OH} = –200 μA	V_{CC} – 0.3	–	V_{CC}	V
		XOUT	I_{OH} = –200 μA	1.0	–	V_{CC}	V
V_{OL}	Output “L” voltage	Other than XOUT	I_{OL} = 5 mA	–	–	2.0	V
			I_{OL} = 200 μA	–	–	0.45	V
		XOUT	I_{OH} = –200 μA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$ to $\overline{INT4}$, $\overline{KI0}$ to $\overline{KI3}$, TRAIO0, TRAIO1, TRBO, TRCIOA to TRCIOD, TRDIOA0 to TRDIOD0, TRDIOA1 to TRDIOD1, TRFI, TRGIOA, TRGIOB, TRCCLK, TRDCLK, TRGCLKA, $\overline{TRGCLKB}$, TRCTRG, $\overline{ADTRG}$, RXD0 to RXD2, CLK0 to CLK2, SSI, SCL2, SDA2, SSO		0.1	1.2	–	V
		$\overline{RESET}$		0.1	1.2	–	V
I_{IH}	Input “H” current		VI = 5 V, V_{CC} = 5.0 V	–	–	1.0	μA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 5.0 V	–	–	–1.0	μA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 5.0 V	25	50	100	kΩ
R_{fXIN}	Feedback resistance	XIN		–	0.3	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode	2.0	–	–	V

Note:
1. 4.2 V ≤ V_{CC} ≤ 5.5 V at T_{opr} = –40 to 85°C (J version) / –40 to 125°C (K version), f(XIN) = 20 MHz, unless otherwise specified.

Table 32.16 Electrical Characteristics (2) [3.3 V ≤ Vcc ≤ 5.5 V] (Topr = −40 to 85°C (J version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
ICC	Power supply current (VCC = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are VSS	High-speed clock mode (1)	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	7.0	15	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	5.6	12.5	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	3.6	–	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.0	–	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.2	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
		High-speed on-chip oscillator mode (1)	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	7.0	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.0	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	–	90	180	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	15	110	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	5	100	µA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	2.0	5.0	µA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	15.0	–	µA

Note:
1. The typical value (Typ.) indicates the current value when the CPU and the memory operate.
The maximum value (Max.) indicates the current when the CPU, the memory, and the peripheral functions operate and the flash memory is programmed/erased.

Table 32.17 Electrical Characteristics (3) [3.3 V ≤ Vcc ≤ 5.5 V] (Topr = −40 to 125°C (K version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
ICC	Power supply current (VCC = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are VSS	High-speed clock mode (1)	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	7.0	15	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	5.6	12.5	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	3.6	–	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.0	–	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.2	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
		High-speed on-chip oscillator mode (1)	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	7.0	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.0	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	–	90	400	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	15	330	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	5	320	µA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	2.0	5.0	µA
			XIN clock off, Topr = 125°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	60.0	–	µA

Note:
1. The typical value (Typ.) indicates the current value when the CPU and the memory operate.
The maximum value (Max.) indicates the current when the CPU, the memory, and the peripheral functions operate and the flash memory is programmed/erased.

Timing Requirements
(Unless Otherwise Specified: Vcc = 5 V, Vss = 0 V at Topr = –40°C to 85°C (J ver)/–40°C to 125°C (K ver))

Table 32.18 External clock input (XOUT)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	50	–	ns
$t_{WH(XOUT)}$	XOUT input “H” width	24	–	ns
$t_{WL(XOUT)}$	XOUT input “L” width	24	–	ns

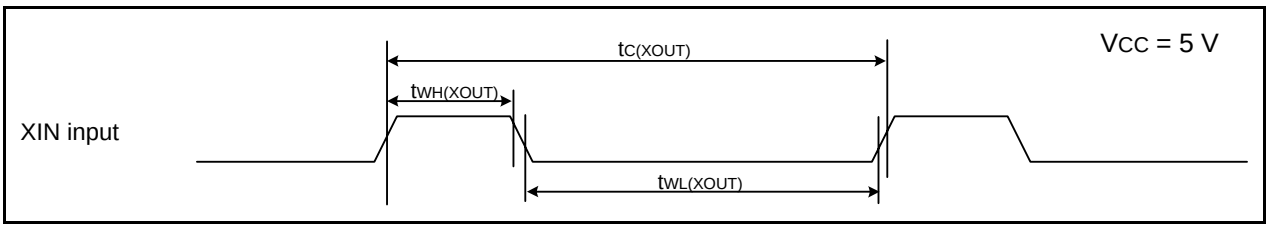


Figure 32.7 External Clock Input Timing Diagram when VCC = 5 V

Table 32.19 TRAIOi (i = 0 to 1) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIOi (i = 0 to 1) input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIOi (i = 0 to 1) input “H” width	40	–	ns
$t_{WL(TRAIO)}$	TRAIOi (i = 0 to 1) input “L” width	40	–	ns

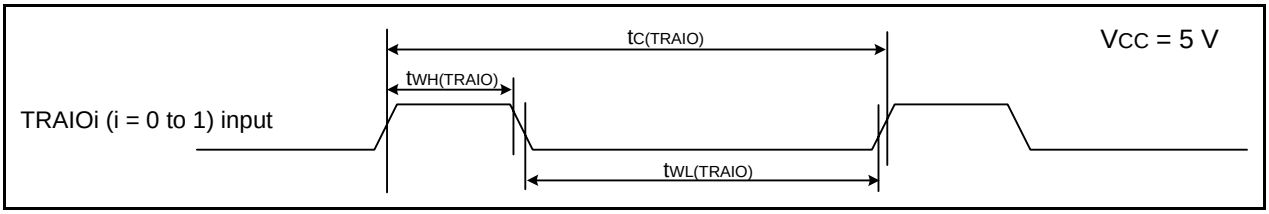


Figure 32.8 TRAIOi (i = 0 to 1) Input Timing Diagram when Vcc = 5 V

Table 32.20 TRFI Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRFI)}$	TRFI input cycle time	1200 (1)	–	ns
$t_{WH(TRFI)}$	TRFI input “H” width	600 (2)	–	ns
$t_{WL(TRFI)}$	TRFI input “L” width	600 (2)	–	ns

Notes:
1. When using timer RF input capture mode, adjust the cycle time to (1/timer RF count source frequency × 3) or above.
2. When using timer RF input capture mode, adjust the pulse width to (1/timer RF count source frequency × 1.5) or above.

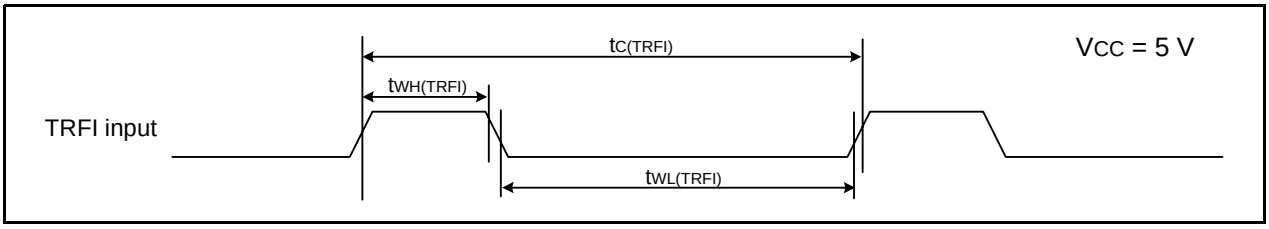


Figure 32.9 TRFI Input Timing Diagram when Vcc = 5 V

Table 32.21 Serial Interface

Symbol	Parameter	Condition	Standard		Unit
			Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	When external clock selected	200	–	ns
$t_{W(CKH)}$	CLKi input “H” width		100	–	ns
$t_{W(CKL)}$	CLKi input “L” width		100	–	ns
$t_{d(C-Q)}$	TXDi output delay time		–	90	ns
$t_{h(C-Q)}$	TXDi hold time		0	–	ns
$t_{su(D-C)}$	RXDi input setup time		10	–	ns
$t_{h(C-D)}$	RXDi input hold time		90	–	ns
$t_{d(C-Q)}$	TXDi output delay time	When internal clock selected	–	10	ns
$t_{su(D-C)}$	RXDi input setup time		90	–	ns
$t_{h(C-D)}$	RXDi input hold time		90	–	ns

i = 0 to 2

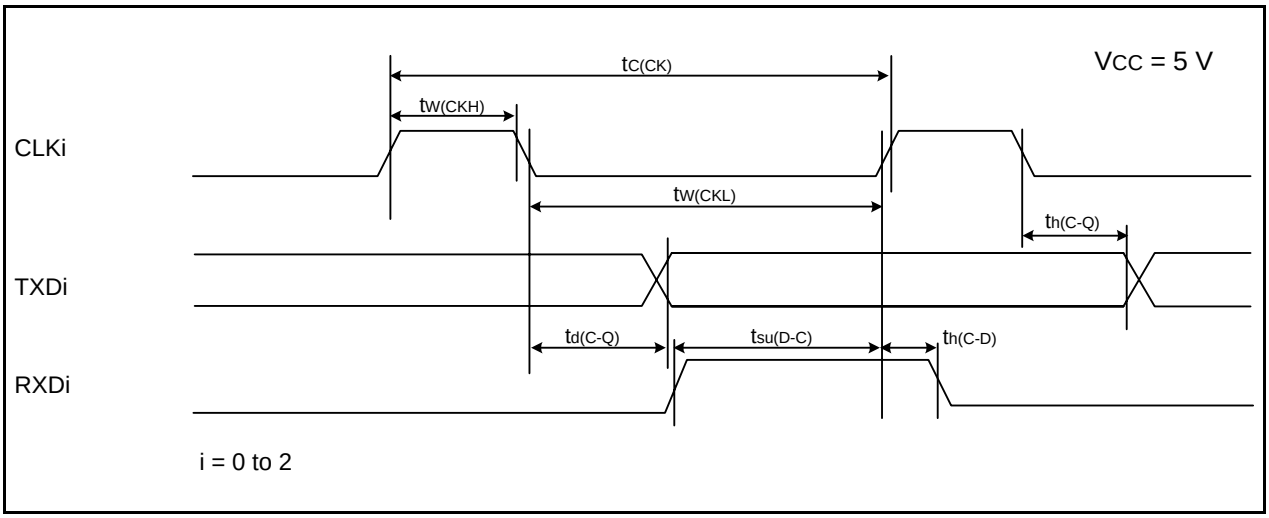


Figure 32.10 Serial Interface Timing Diagram when Vcc = 5 V

Table 32.22 External Interrupt $\overline{INTi}$ (i = 0 to 4) Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width	250 (1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width	250 (2)	–	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

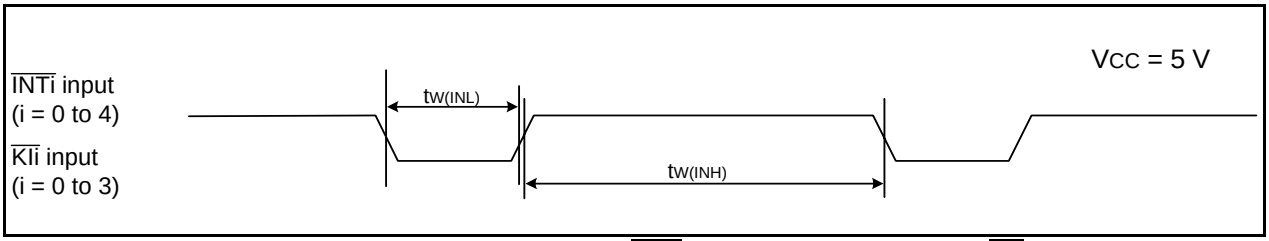


Figure 32.11 Input Timing for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIi}$ when Vcc = 5 V

Table 32.23 Electrical Characteristics (4) [2.7 V ≤ Vcc < 4.2 V]

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Other than XOUT	I_{OH} = –1 mA	V_{CC} – 0.5	–	V_{CC}	V
		XOUT	I_{OH} = –200 μA	1.0	–	V_{CC}	V
V_{OL}	Output “L” voltage	Other than XOUT	I_{OL} = 1 mA	–	–	0.5	V
		XOUT	I_{OL} = 200 μA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$ to $\overline{INT4}$, $\overline{KI0}$ to $\overline{KI3}$, TRAIO0, TRAIO1, TRBO, TRCIOA to TRCIOD, TRDIOA0 to TRDIOD0, TRDIOA1 to TRDIOD1, TRFI, TRGIOA, TRGIOB, TRCCLK, TRDCLK, TRGCLKA, $\overline{TRGCLKB}$, TRCTRG, $\overline{ADTRG}$, RXD0 to RXD2, CLK0 to CLK2, SSI, SCL2, SDA2, SSO		0.1	0.4	–	V
		$\overline{RESET}$		0.1	0.5	–	V
I_{IH}	Input “H” current		VI = 3 V, V_{CC} = 3.0 V	–	–	1.0	μA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 3.0 V	–	–	–1.0	μA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 3.0 V	42	84	168	kΩ
R_{fXIN}	Feedback resistance	XIN		–	0.3	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode	2.0	–	–	V

Note:
1. 2.7 V ≤ V_{CC} < 4.2 V at T_{opr} = –40 to 85°C (J version) / –40 to 125°C (K version), f(XIN) = 20 MHz, unless otherwise specified.

Table 32.24 Electrical Characteristics (5) [2.7 V ≤ Vcc < 3.3 V] (Topr = −40 to 85°C (J version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
ICC	Power supply current (VCC = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are VSS	High-speed clock mode (1)	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	7.0	14.5	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	5.6	12.0	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	3.6	–	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.0	–	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.2	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
		High-speed on-chip oscillator mode (1)	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	7.0	14.5	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.0	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	–	85	180	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	15	110	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	5	100	µA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	2.0	5.0	µA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	13.0	–	µA

Note:
1. The typical value (Typ.) indicates the current value when the CPU and the memory operate.
The maximum value (Max.) indicates the current when the CPU, the memory, and the peripheral functions operate and the flash memory is programmed/erased.

Table 32.25 Electrical Characteristics (6) [2.7 V ≤ Vcc < 3.3 V] (Topr = −40 to 125°C (K version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
ICC	Power supply current (VCC = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are VSS	High-speed clock mode (1)	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	7.0	14.5	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	5.6	12.0	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	3.6	–	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.0	–	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.2	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
		High-speed on-chip oscillator mode (1)	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	7.0	14.5	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.0	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	–	85	390	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	15	320	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	5	310	µA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	2.0	5.0	µA
			XIN clock off, Topr = 125°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	55.0	–	µA

Note:
1. The typical value (Typ.) indicates the current value when the CPU and the memory operate.
The maximum value (Max.) indicates the current when the CPU, the memory, and the peripheral functions operate and the flash memory is programmed/erased.

Timing requirements
(Unless Otherwise Specified: Vcc = 3 V, Vss = 0 V at Topr = –40°C to 85°C (J ver)/–40°C to 125°C (K ver))

Table 32.26 External clock input (XOUT)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	50	–	ns
$t_{WH(XOUT)}$	XOUT input “H” width	24	–	ns
$t_{WL(XOUT)}$	XOUT input “L” width	24	–	ns

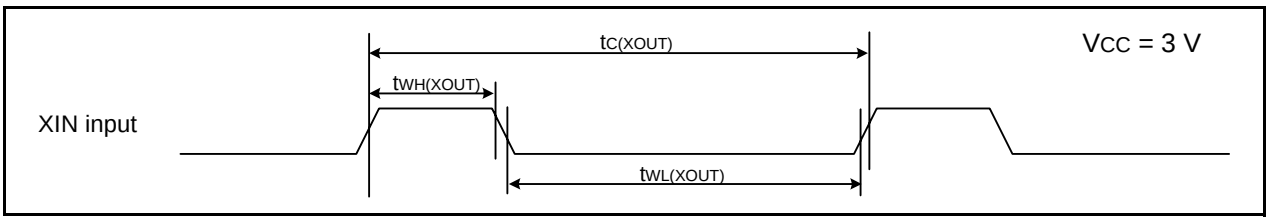


Figure 32.12 External Clock Input Timing Diagram when VCC = 3 V

Table 32.27 TRAIOi (i = 0 to 1) Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIOi (i = 0 to 1) input cycle time	300	–	ns
$t_{WH(TRAIO)}$	TRAIOi (i = 0 to 1) input “H” width	120	–	ns
$t_{WL(TRAIO)}$	TRAIOi (i = 0 to 1) input “L” width	120	–	ns

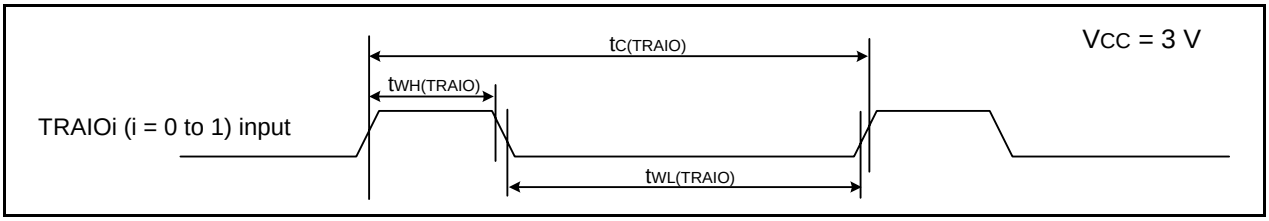


Figure 32.13 TRAIOi (i = 0 to 1) Input Timing Diagram when Vcc = 3 V

Table 32.28 TRFI Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRFI)}$	TRFI input cycle time	400 (1)	–	ns
$t_{WH(TRFI)}$	TRFI input “H” width	200 (2)	–	ns
$t_{WL(TRFI)}$	TRFI input “L” width	200 (2)	–	ns

Notes:
1. When using timer RF input capture mode, adjust the cycle time to (1/timer RF count source frequency × 3) or above.
2. When using timer RF input capture mode, adjust the pulse width to (1/timer RF count source frequency × 1.5) or above.

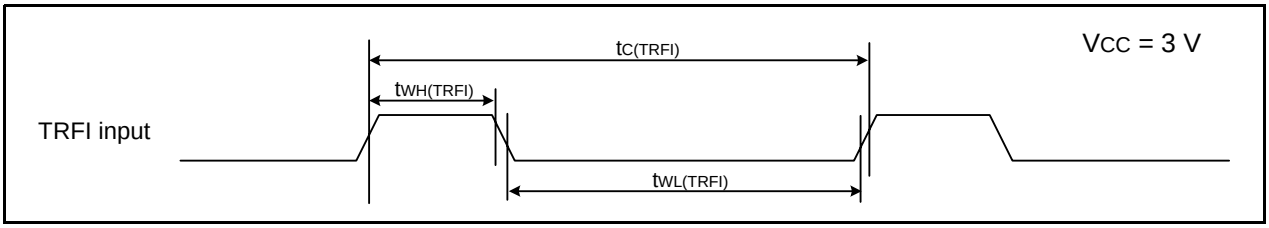


Figure 32.14 TRFI Input Timing Diagram when Vcc = 3 V

Table 32.29 Serial Interface

Symbol	Parameter	Condition	Standard		Unit
			Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	When external clock selected	300	–	ns
$t_{W(CKH)}$	CLKi input “H” width		150	–	ns
$t_{W(CKL)}$	CLKi Input “L” width		150	–	ns
$t_{d(C-Q)}$	TXDi output delay time		–	120	ns
$t_{h(C-Q)}$	TXDi hold time		0	–	ns
$t_{su(D-C)}$	RXDi input setup time		30	–	ns
$t_{h(C-D)}$	RXDi input hold time		90	–	ns
$t_{d(C-Q)}$	TXDi output delay time	When internal clock selected	–	30	ns
$t_{su(D-C)}$	RXDi input setup time		120	–	ns
$t_{h(C-D)}$	RXDi input hold time		90	–	ns

i = 0 to 2

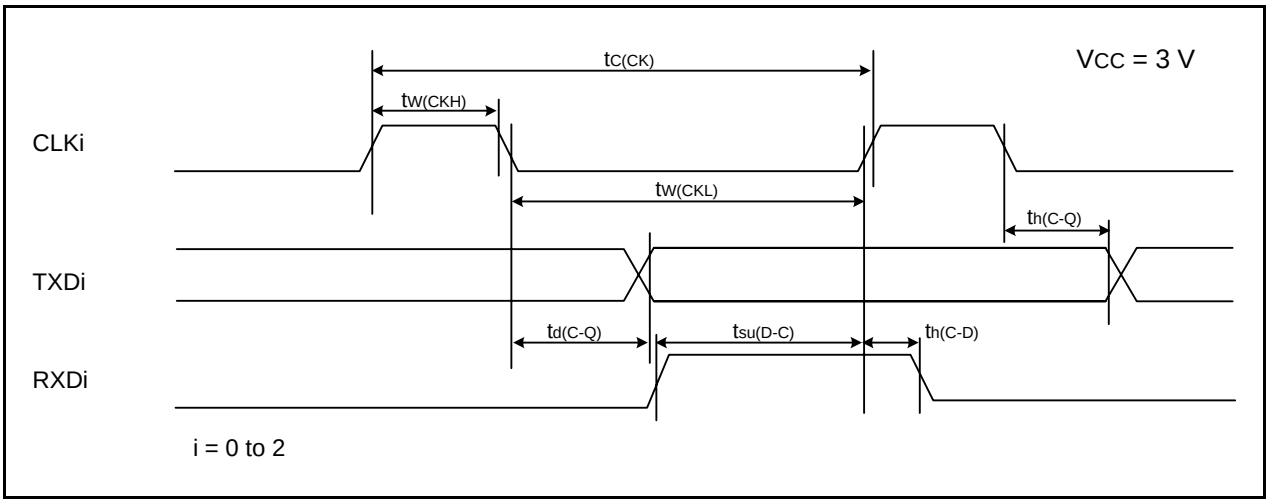


Figure 32.15 Serial Interface Timing Diagram when VCC = 3 V

Table 32.30 External Interrupt $\overline{INTi}$ (i = 0 to 4) Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width	380 (1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width	380 (2)	–	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

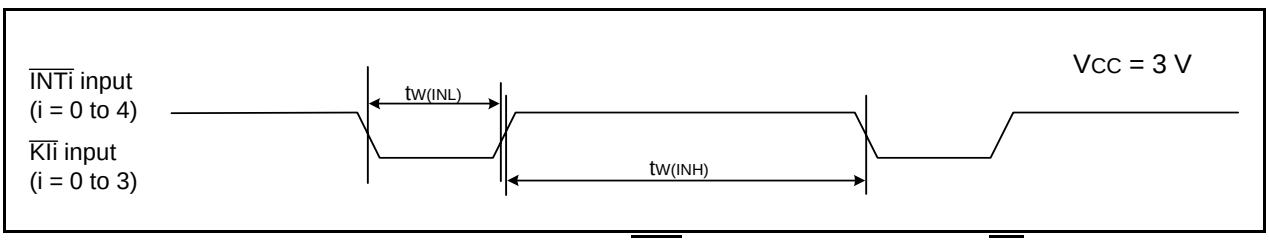


Figure 32.16 Input Timing for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIi}$ when Vcc = 3 V

33. Usage Notes

33.1 Notes on Clock Generation Circuit

33.1.1 Stop Mode

To enter stop mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and then the CM10 bit in the CM1 register to 1 (stop mode). An instruction queue pre-reads 4 bytes from the instruction which sets the CM10 bit to 1 (stop mode) and the program stops.
Insert at least four NOP instructions following the JMP.B instruction after the instruction which sets the CM10 bit to 1.

• Program example to enter stop mode

```
        BCLR    1,FMR0      ; CPU rewrite mode disabled
        BCLR    7,FMR2      ; Low-current-consumption read mode disabled
        BSET    0,PRCR      ; Writing to CM1 register enabled
        FSET    I           ; Enable interrupt
        BSET    0,CM1       ; Stop mode
        JMP.B   LABEL_001
LABEL_001:
        NOP
        NOP
        NOP
        NOP
```

33.1.2 Wait Mode

When setting bits CM37 and CM36 to values other than 00b to enter wait mode from high-speed clock mode, set the XIN clock frequency to 28 kHz or more.
To enter wait mode by setting the CM30 bit to 1, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) before setting the CM30 bit to 1.
To enter wait mode with the WAIT instruction, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and then execute the WAIT instruction. An instruction queue pre-reads 4 bytes from the instruction to set the CM30 bit to 1 (MCU enters wait mode) or the WAIT instruction, and then the program stops. Insert at least four NOP instructions after the instruction to set the CM30 bit to 1 (MCU enters wait mode) or these instructions.

• Program example to execute the WAIT instruction

```
        BCLR    1,FMR0      ; CPU rewrite mode disabled
        BCLR    7,FMR2      ; Low-current-consumption read mode disabled
        FSET    I           ; Enable interrupt
        WAIT                ; Wait mode
        NOP
        NOP
        NOP
        NOP
```

• Program example to execute the instruction to set the CM30 bit to 1

```
        BCLR    1, FMR0     ; CPU rewrite mode disabled
        BCLR    7,FMR2      ; Low-current-consumption read mode disabled
        BSET    0, PRCR     ; Writing to CM3 register enabled
        FCLR    I           ; Interrupt disabled
        BSET    0, CM3      ; Wait mode
        NOP
        NOP
        NOP
        NOP
        BCLR    0, PRCR     ; Writing to CM3 register enabled
        FSET    I           ; Interrupt enabled
```

33.1.3 Oscillation Stop Detection Function

Since the oscillation stop detection function cannot be used if the XIN clock frequency is below 2 MHz, set bits OCD1 to OCD0 to 00b.

33.1.4 Oscillation Circuit Constants

Consult the oscillator manufacturer to determine the optimal oscillation circuit constants for the user system.

33.2 Notes on Interrupts

33.2.1 Reading Address 00000h

Do not read address 00000h by a program. When a maskable interrupt request is acknowledged, the CPU reads interrupt information (interrupt number and interrupt request level) from 00000h in the interrupt sequence. At this time, the IR bit for the acknowledged interrupt is set to 0.
If address 00000h is read by a program, the IR bit for the interrupt which has the highest priority among the enabled interrupts is set to 0. This may cause the interrupt to be canceled, or an unexpected interrupt to be generated.

33.2.2 SP Setting

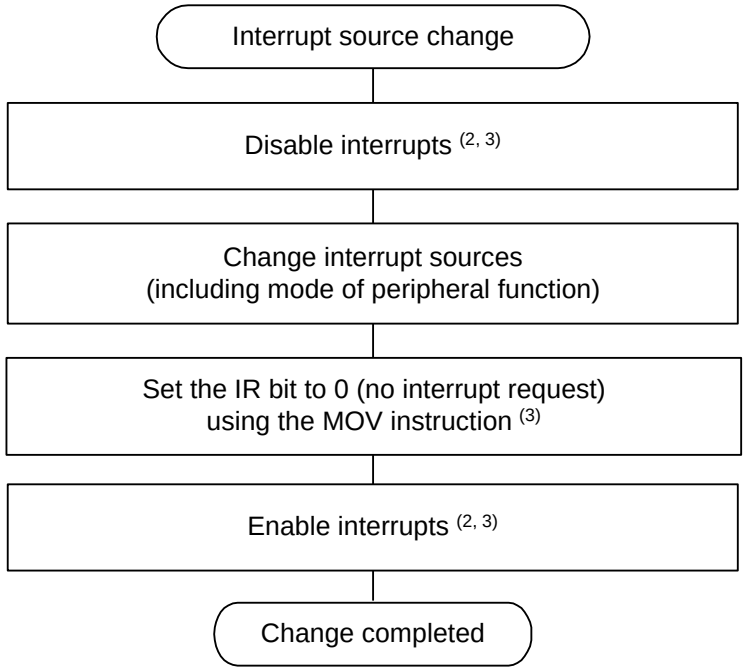
Set a value in the SP before an interrupt is acknowledged. The SP is set to 0000h after a reset. If an interrupt is acknowledged before setting a value in the SP, the program may run out of control.

33.2.3 External Interrupt and Key Input Interrupt

Either the “L” level width or “H” level width shown in the Electrical Characteristics is required for the signal input to pins $\overline{\text{INT0}}$ to $\overline{\text{INT4}}$ and pins $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$, regardless of the CPU clock.
For details, refer to **Table 32.22** (VCC = 5 V), **Table 32.30** (VCC = 3 V) **External Interrupt $\overline{\text{INTi}}$ (i = 0 to 4) Input, Key Input Interrupt $\overline{\text{KIi}}$ (i = 0 to 3)**.

33.2.4 Changing Interrupt Sources

The IR bit in the interrupt control register may be set to 1 (interrupt requested) when the interrupt source changes. To use an interrupt, set the IR bit to 0 (no interrupt requested) after changing interrupt sources.
Changing interrupt sources as referred to here includes all factors that change the source, polarity, or timing of the interrupt assigned to a software interrupt number. Therefore, if a mode change of a peripheral function involves the source, polarity, or timing of an interrupt, set the IR bit to 0 (no interrupt requested) after making these changes. Refer to the descriptions of the individual peripheral functions for related interrupts.
Figure 33.1 shows a Procedure Example for Changing Interrupt Sources.



IR bit: The interrupt control register bit for the interrupt whose source is to be changed

Notes:
1. The above settings must be executed individually. Do not execute two or more settings simultaneously (using one instruction).
2. To prevent interrupt requests from being generated disable the peripheral function before changing the interrupt source. In this case, use the I flag if all maskable interrupts can be disabled.
   If all maskable interrupts cannot be disabled, use bits ILVL0 to ILVL2 for the interrupt whose source is to be changed.
3. To change the interrupt source to the input with the digital filter used, wait for three or more cycles of the sampling clock of the digital filter before setting the IR bit to 0 (no interrupt request). Refer to **33.2.5 Rewriting Interrupt Control Register** for the instructions to use and related notes.

Figure 33.1 Procedure Example for Changing Interrupt Sources

33.2.5 Rewriting Interrupt Control Register

(a) The contents of the interrupt control register can be rewritten only while no interrupt requests corresponding to that register are generated. If an interrupt request may be generated, disable the interrupt before rewriting the contents of the interrupt control register.

(b) When rewriting the contents of the interrupt control register after disabling the interrupt, be careful to choose appropriate instructions.
Changing any bit other than the IR bit
If an interrupt request corresponding to the register is generated while executing the instruction, the IR bit may not be set to 1 (interrupt requested), and the interrupt may be ignored. If this causes a problem, use one of the following instructions to rewrite the contents of the register: AND, OR, BCLR, and BSET.

Changing the IR bit
Depending on the instruction used, the IR bit may not be set to 0 (no interrupt requested).
Use the MOV instruction to set the IR bit to 0.

(c) When using the I flag to disable an interrupt, set the I flag as shown in the sample programs below. Refer to (b) regarding rewriting the contents of interrupt control registers using the sample programs.

Examples 1 to 3 shows how to prevent the I flag from being set to 1 (interrupts enabled) before the contents of the interrupt control register are rewritten for the effects of the internal bus and the instruction queue buffer.

Example 1: Use the NOP instructions to pause program until the interrupt control register is rewritten

```
INT_SWITCH1:
    FCLR    I               ; Disable interrupts
    AND.B   #00H,0056H      ; Set the TRA0IC register to 00h
    NOP                     ;
    NOP
    FSET    I               ; Enable interrupts
```

Example 2: Use a dummy read to delay the FSET instruction

```
INT_SWITCH2:
    FCLR    I               ; Disable interrupts
    AND.B   #00H,0056H      ; Set the TRA0IC register to 00h
    MOV.W   MEM,R0          ; Dummy read
    FSET    I               ; Enable interrupts
```

Example 3: Use the POPC instruction to change the I flag

```
INT_SWITCH3:
    PUSHC   FLG
    FCLR    I               ; Disable interrupts
    AND.B   #00H,0056H      ; Set the TRA0IC register to 00h
    POPC    FLG             ; Enable interrupts
```

33.3 Notes on ID Code Areas

33.3.1 Setting Example of ID Code Areas

The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

- To set 55h in all of the ID code areas

```
.org 00FFDCH
.lword dummy | (55000000h)    ; UND
.lword dummy | (55000000h)    ; INTO
.lword dummy ; BREAK
.lword dummy | (55000000h)    ; ADDRESS MATCH
.lword dummy | (55000000h)    ; SET SINGLE STEP
.lword dummy | (55000000h)    ; WDT
.lword dummy | (55000000h)    ; ADDRESS BREAK
.lword dummy | (55000000h)    ; RESERVE
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

33.4 Notes on Option Function Select Area

33.4.1 Setting Example of Option Function Select Area

The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

- To set FFh in the OFS register

```
.org 00FFFCH
.lword reset | (0FF000000h)      ; RESET
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

- To set FFh in the OFS2 register

```
.org 00FFDBH
.byte 0FFh
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

33.5 Notes on DTC

33.5.1 DTC activation source

- Do not generate any DTC activation sources before entering wait mode or during wait mode.
- Do not generate any DTC activation sources before entering stop mode or during stop mode.

33.5.2 DTCENi (i = 0 to 6) Registers

- Modify bits DTCENi0 to DTCENi7 only while an interrupt request corresponding to the register is not generated.
- When the interrupt source flag in the status register for the peripheral function is 1, do not modify the corresponding activation source bit among bits DTCENi0 to DTCENi7.
- Do not access the DTCENi registers using DTC transfers.

33.5.3 Peripheral Modules

- Do not set the status register bit for the peripheral function to 0 using a DTC transfer.
- When the DTC activation source is SSU receive data full, read the SSRDR register using a DTC transfer. The RDRF bit in the SSSR register is set to 0 (no data in SSRDR register) by reading the SSRDR register. However, the RDRF bit is not set to 0 by reading the SSRDR register when the DTC data transfer setting is either of the following:
  - Transfer causing the DTCCTj (j = 0 to 23) register value to change from 1 to 0 in normal mode
  - Transfer causing the DTCCRj register value to change from 1 to 0 while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled) in repeat mode.
- When the DTC activation source is SSU transmit data empty, write to the SSTDR register using a DTC transfer. The TDRE bit in the SSSR register is set to 0 (data is not transferred from registers SSTDR to SSTRSR) by writing to the SSTDR register.

33.5.4 Interrupt Request

- When the DTC activation source is either SSU transmit data empty or flash ready status, no interrupt request is generated for the CPU in either of the following cases:
  - When the DTC performs a data transfer that causes the DTCCTj register value to change to 0 in normal mode.
  - When the DTC performs a data transfer that causes the DTCCRj register value to change to 0 while the RPTINT bit in the DTCCRj register is 1 in repeat mode.

33.5.5 DTC Activation

- When the DTC is activated, operation may be shifted for one cycle before reading a vector.

33.5.6 Chain transfer

When performing chain transfers using several control data, the number of transfers set to the first control data is enabled and the number of transfers proceeded after the first control data is disabled.

Examples: When DTCCT0 = 5 and DTCCT1 = 10, chain transfers are performed as DTCCT0 = DTCCT1 = 5.
When DTCCT0 = 10 and DTCCT1 = 5, chain transfers are performed as DTCCT0 = DTCCT1 = 10.
When DTCCT0 = 10, DTCCT1 = 5, and DTCCT2 = 2, chain transfers are performed as DTCCT0 = DTCCT1 = DTCCT2 = 10.

33.6 Notes on Timer RA

- Timer RA stops counting after a reset. Set the values in the timer RA and timer RA prescalers before the count starts.
- Even if the prescaler and timer RA are read out in 16-bit units, these registers are read 1 byte at a time by the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In pulse width measurement mode and pulse period measurement mode, bits TEDGF and TUNDF in the TRAiCR register can be set to 0 by writing 0 to these bits by a program. However, these bits remain unchanged if 1 is written. When using the READ-MODIFY-WRITE instruction for the TRAiCR register, the TEDGF or TUNDF bit may be set to 0 although these bits are set to 1 while the instruction is being executed. In this case, write 1 to the TEDGF or TUNDF bit which is not supposed to be set to 0 with the MOV instruction.
- When changing to pulse period measurement mode from another mode, the contents of bits TEDGF and TUNDF are undefined. Write 0 to bits TEDGF and TUNDF before the count starts.
- The TEDGF bit may be set to 1 by the first timer RA prescaler underflow generated after the count starts.
- When using the pulse period measurement mode, leave two or more periods of the timer RA prescaler immediately after the count starts, then set the TEDGF bit to 0.
- The TCSTF bit retains 0 (count stops) for 0 to 1 cycle of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.
  Do not write to the TRAiCR register until the TCSTF bit is set to 1. Also, do not access other registers associated with timer RA (1).
  Timer RA starts counting at the first valid edge of the count source after the TCSTF bit is set to 1 (during count).
  The TCSTF bit remains 1 for 0 to 1 cycle of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RA counting is stopped when the TCSTF bit is set to 0.
  Do not write to the TRAiCR register until the TCSTF bit is set to 0. Also, do not access other registers associated with timer RA (1).

  Note:
  1. Registers associated with timer RA: TRAiIOC, TRAiMR, TRAiPRE, and TRAi.

- When the TRAiPRE register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the count source clock for each write interval.
- When the TRAi register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the prescaler underflow for each write interval.
- Do not set 00h to the TRAi register in pulse width measurement mode and pulse period measurement mode.

33.7 Notes on Timer RB

- Timer RB stops counting after a reset. Set the values in the timer RB and timer RB prescalers before the count starts.
- Even if the prescaler and timer RB is read out in 16-bit units, these registers are read 1 byte at a time by the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In programmable one-shot generation mode and programmable wait one-shot generation mode, when setting the TSTART bit in the TRBCR register to 0 (stops counting) or setting the TOSSP bit in the TRBOCR register to 1 (stops one-shot), the timer reloads the value of reload register and stops. Therefore, in programmable one-shot generation mode and programmable wait one-shot generation mode, read the timer count value before the timer stops.
- The TCSTF bit remains 0 (count stops) for 1 to 2 cycles of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.
  During this time, do not access registers associated with timer RB (1) other than the TCSTF bit. Timer RB starts counting at the first valid edge of the count source after the TCSTF bit is set to 1 (during count).
  The TCSTF bit remains 1 for 1 to 2 cycles of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RB counting is stopped when the TCSTF bit is set to 0.
  During this time, do not access registers associated with timer RB (1) other than the TCSTF bit.

  Note:
  1. Registers associated with timer RB: TRBCR, TRBOCR, TRBIOC, TRBMR, TRBPRE, TRBSC, and TRBPR.

- If the TSTOP bit in the TRBCR register is set to 1 during timer operation, timer RB stops immediately.
- If 1 is written to the TOSST or TOSSP bit in the TRBOCR register, the value of the TOSSTF bit changes after one or two cycles of the count source have elapsed. If the TOSSP bit is written to 1 during the period between when the TOSST bit is written to 1 and when the TOSSTF bit is set to 1, the TOSSTF bit may be set to either 0 or 1 depending on the content state. Likewise, if the TOSST bit is written to 1 during the period between when the TOSSP bit is written to 1 and when the TOSSTF bit is set to 0, the TOSSTF bit may be set to either 0 or 1.
- To use the underflow signal of timer RA as the count source for timer RB, set timer RA in timer mode, pulse output mode, or event count mode.

33.7.1 Timer Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

33.7.2 Programmable Waveform Generation Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

33.7.3 Programmable One-shot Generation Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRE register is written continuously during count operation (TCSTF bit is set to 1), allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously during count operation (TCSTF bit is set to 1), allow three or more cycles of the prescaler underflow for each write interval.

33.7.4 Programmable Wait One-shot Generation Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

33.8 Notes on Timer RC

33.8.1 TRC Register

- The following note applies when the CCLR bit in the TRCCR1 register is set to 1 (clear TRC register at compare match with TRCGRA register).
  When using a program to write a value to the TRC register while the TSTART bit in the TRCMR register is set to 1 (count starts), ensure that the write does not overlap with the timing with which the TRC register is set to 0000h.
  If the timing of the write to the TRC register and the setting of the TRC register to 0000h coincide, the write value will not be written to the TRC register and the TRC register will be set to 0000h.

- Reading from the TRC register immediately after writing to it can result in the value previous to the write being read out. To prevent this, execute the JMP.B instruction between the read and the write instructions.

```
Program Example     MOV.W   #XXXXh, TRC    ;Write
                    JMP.B   L1             ;JMP.B instruction
                L1: MOV.W   TRC,DATA       ;Read
```

33.8.2 TRCSR Register

Reading from the TRCSR register immediately after writing to it can result in the value previous to the write being read out. To prevent this, execute the JMP.B instruction between the read and the write instructions.

```
Program Example     MOV.B   #XXh, TRCSR    ;Write
                    JMP.B   L1             ;JMP.B instruction
                L1: MOV.B   TRCSR,DATA     ;Read
```

33.8.3 TRCCR1 Register

To set bits TCK2 to TCK0 in the TRCCR1 register to 111b (fOCO-F), set fOCO-F to the clock frequency higher than the CPU clock frequency.

33.8.4 Count Source Switching

- Stop the count before switching the count source.

Switching procedure
(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.

- When changing the count source from fOCO40M to another clock other than fOCO-F and stopping fOCO40M, wait 2 cycles of f1 or more after setting the clock switch, and then stop fOCO40M.

Switching procedure
(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change bits TCK2 to TCK0 in the TRCCR1 register.
(3) Wait 2 or more cycles of f1.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

- After switching the count source from fOCO-F to a clock other than fOCO40M, allow a minimum of one cycle of fOCO-F + fOCO40M to elapse after changing the clock setting before stopping fOCO-F.

Switching procedure

(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.
(3) Wait for a minimum of one cycle of fOCO-F + fOCO40M.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

33.8.5 Input Capture Function

- Set the pulse width of the input capture signal as follows:
  [When the digital filter is not used]
  Three or more cycles of the timer RC operation clock (refer to **Table 19.1 Timer RC Operation Clock**)
  [When the digital filter is used]
  Five cycles of the digital filter sampling clock + three cycles of the timer RC operating clock, minimum (refer to **Figure 19.5 Digital Filter Block Diagram**)
- The value of the TRC register is transferred to the TRCGRj register one or two cycles of the timer RC operation clock after the input capture signal is input to the TRCIOj (j = A, B, C, or D) pin (when the digital filter function is not used).

33.8.6 TRCMR Register in PWM2 Mode

When the CSEL bit in the TRCCR2 register is set to 1 (count stops at compare match with the TRCGRA register), do not set the TRCMR register at compare match timing of registers TRC and TRCGRA.

33.9 Notes on Timer RD

33.9.1 TRDSTR Register

- Set the TRDSTR register using the MOV instruction.

- When the CSELi (i = 0 to 1) bit is set to 0 (the count stops at compare match of registers TRDi and TRDGRAi), the count does not stop and the TSTARTi bit remains unchanged even if 0 (count stops) is written to the TSTARTi bit.
  Therefore, set the TSTARTi bit to 0 to change other bits without changing the TSTARTi bit when the CSELi bit is se to 0.
  To stop counting by a program, set the TSTARTi bit after setting the CSELi bit to 1. Although the CSELi bit is set to 1 and the TSTARTi bit is set to 0 at the same time (with 1 instruction), the count cannot be stopped.

- Table 33.1 lists the TRDIOji (j = A, B, C, or D) Pin Output Level when Count Stops to use the TRDIOji (j = A, B, C, or D) pin with the timer RD output.

Table 33.1 TRDIOji (j = A, B, C, or D) Pin Output Level when Count Stops

Count Stop	TRDIOji Pin Output when Count Stops
When the CSELi bit is set to 1, set the TSTARTi bit to 0 and the count stops.	The pin holds the output level immediately before the count stops. (The pin outputs the initial output level selected by bits OLS0 and OLS1 in the TRDFCR register in complementary and reset synchronous PWM modes.)
When the CSELi bit is set to 0, the count stops at compare match of registers TRDi and TRDGRAi.	The pin holds the output level after the output changes by compare match. (The pin outputs the initial output level selected by bits OLS0 and OLS1 in the TRDFCR register in complementary and reset synchronous PWM modes.)

33.9.2 TRDi Register (i = 0 or 1)

- When writing the value to the TRDi register by a program while the TSTARTi bit in the TRDSTR register is set to 1 (count starts), avoid overlapping with the timing for setting the TRDi register to 0000h, and then write. If the timing for setting the TRDi register to 0000h overlaps with the timing for writing the value to the TRDi register, the value is not written and the TRDi register is set to 0000h.
  These precautions are applicable when selecting the following by bits CCLR2 to CCLR0 in the TRDCRi register.
  - 001b (Clear the TRDi register by input capture/compare match in the TRDGRAi register.)
  - 010b (Clear the TRDi register by input capture/compare match in the TRDGRBi register.)
  - 011b (Synchronous clear)
  - 101b (Clear the TRDi register by input capture/compare match in the TRDGRCi register.)
  - 110b (Clear the TRDi register by input capture/compare match in the TRDGRDi register.)

- When writing the value to the TRDi register and continuously reading the same register, the value before writing may be read. In this case, execute the JMP.B instruction between the writing and reading.

```
Program example     MOV.W   #XXXXh, TRD0     ;Writing
                    JMP.B   L1               ;JMP.B
                L1: MOV.W   TRD0,DATA        ;Reading
```

33.9.3 TRDSRi Register (i = 0 or 1)

When writing the value to the TRDSRi register and continuously reading the same register, the value before writing may be read. In this case, execute the JMP.B instruction between the writing and reading.

```
Program example     MOV.B   #XXh, TRDSR0     ;Writing
                    JMP.B   L1               ;JMP.B
                L1: MOV.B   TRDSR0,DATA      ;Reading
```

33.9.4 TRDCRi Register (i = 0 or 1)

To set bits TCK2 to TCK0 in the TRDCRi register to 111b (fOCO-F), set fOCO-F to the clock frequency higher than the CPU clock frequency.

33.9.5 Count Source Switching

• Switch the count source after the count stops.

Switching procedure

(1) Set the TSTARTi (i = 0 or 1) bit in the TRDSTR register to 0 (count stops).
(2) Change bits TCK2 to TCK0 in the TRDCRi register.

• When changing the count source from fOCO40M to another clock other than fOCO-F and stopping fOCO40M, wait 2 cycles of f1 or more after setting the clock switch, and then stop fOCO40M.

Switching procedure

(1) Set the TSTARTi (i = 0 or 1) bit in the TRDSTR register to 0 (count stops).
(2) Change bits TCK2 to TCK0 in the TRDCRi register.
(3) Wait 2 or more cycles of f1.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

• After switching the count source from fOCO-F to a clock other than fOCO40M, allow a minimum of one cycle of fOCO-F + fOCO40M to elapse after changing the clock setting before stopping fOCO-F.

Switching procedure

(1) Set the TSTARTi (i = 0 to 1) bit in the TRDSTR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRDCRi register.
(3) Wait for a minimum of one cycle of fOCO-F + fOCO40M.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

33.9.6 Input Capture Function

• Set the pulse width of the input capture signal to 3 or more cycles of the timer RD operation clock (refer to **Table 20.1 Timer RD Operation Clocks**).
• The value in the TRDi register is transferred to the TRDGRji register 2 to 3 cycles of the timer RD operation clock after the input capture signal is applied to the TRDIOji pin (i = 0 or 1, j = either A, B, C, or D) (no digital filter).

33.9.7 Reset Synchronous PWM Mode

• When reset synchronous PWM mode is used for motor control, make sure OLS0 = OLS1.
• Set to reset synchronous PWM mode by the following procedure:

Switching procedure

(1) Set the TSTART0 bit in the TRDSTR register to 0 (count stops).
(2) Set bits CMD1 to CMD0 in the TRDFCR register to 00b (timer mode, PWM mode, and PWM3 mode).
(3) Set bits CMD1 to CMD0 to 01b (reset synchronous PWM mode).
(4) Set the other registers associated with timer RD again.

33.9.8 Complementary PWM Mode

- When complementary PWM mode is used for motor control, make sure OLS0 = OLS1.
- Change bits CMD1 to CMD0 in the TRDFCR register in the following procedure.

Switching procedure: When setting to complementary PWM mode (including re-set), or changing the transfer timing from the buffer register to the general register in complementary PWM mode.

(1) Set both the TSTART0 and TSTART1 bits in the TRDSTR register to 0 (count stops).
(2) Set bits CMD1 to CMD0 in the TRDFCR register to 00b (timer mode, PWM mode, and PWM3 mode).
(3) Set bits CMD1 to CMD0 to 10b or 11b (complementary PWM mode).
(4) Set the registers associated with other timer RD again.

Switching procedure: When stopping complementary PWM mode

(1) Set both the TSTART0 and TSTART1 bits in the TRDSTR register to 0 (count stops).
(2) Set bits CMD1 to CMD to 00b (timer mode, PWM mode, and PWM3 mode).

- Do not write to TRDGRA0, TRDGRB0, TRDGRA1, or TRDGRB1 register during operation.
  When changing the PWM waveform, transfer the values written to registers TRDGRD0, TRDGRC1, and TRDGRD1 to registers TRDGRB0, TRDGRA1, and TRDGRB1 using the buffer operation.
  However, to write data to the TRDGRD0, TRDGRC1, or TRDGRD1 register, set bits BFD0, BFC1, and BFD1 to 0 (general register). After this, bits BFD0, BFC1, and BFD1 may be set to 1 (buffer register).
  The PWM period cannot be changed.
- If the value in the TRDGRA0 register is assumed to be m, the TRD0 register counts m-1, m, m+1, m, m-1, in that order, when changing from increment to decrement operation.
  When changing from m to m+1, the IMFA bit is set to 1. Also, bits CMD1 to CMD0 in the TRDFCR register are set to 11b (complementary PWM mode, buffer data transferred at compare match between registers TRD0 and TRDGRA0), the content in the buffer registers (TRDGRD0, TRDGRC1, and TRDGRD1) is transferred to the general registers (TRDGRB0, TRDGRA1, and TRDGRB1).
  During m+1, m, and m-1 operation, the IMFA bit remains unchanged and data are not transferred to registers such as the TRDGRA0 register.

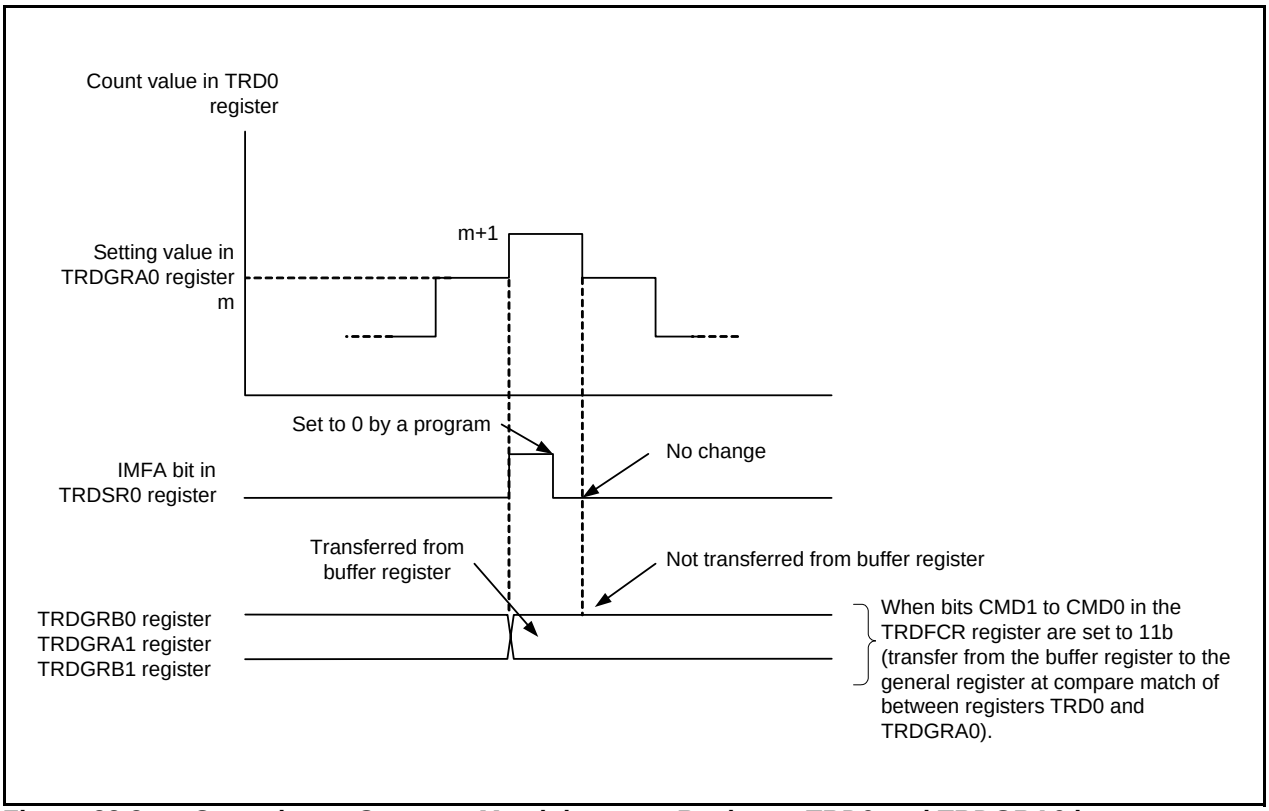


Figure 33.2 Operation at Compare Match between Registers TRD0 and TRDGRA0 in Complementary PWM Mode

- The TRD1 register counts 1, 0, FFFFh, 0, 1, in that order, when changing from decrement to increment operation.
  The UDF bit is set to 1 when changing between 1, 0, and FFFFh operation. Also, when bits CMD1 to CMD0 in the TRDFCR register are set to 10b (complementary PWM mode, buffer data transferred at underflow in the TRD1 register), the content in the buffer registers (TRDGRD0, TRDGRC1, and TRDGRD1) is transferred to the general registers (TRDGRB0, TRDGRA1, and TRDGRB1). During FFFFh, 0, 1 operation, data are not transferred to registers such as the TRDGRB0 register. Also, at this time, the OVF bit remains unchanged.

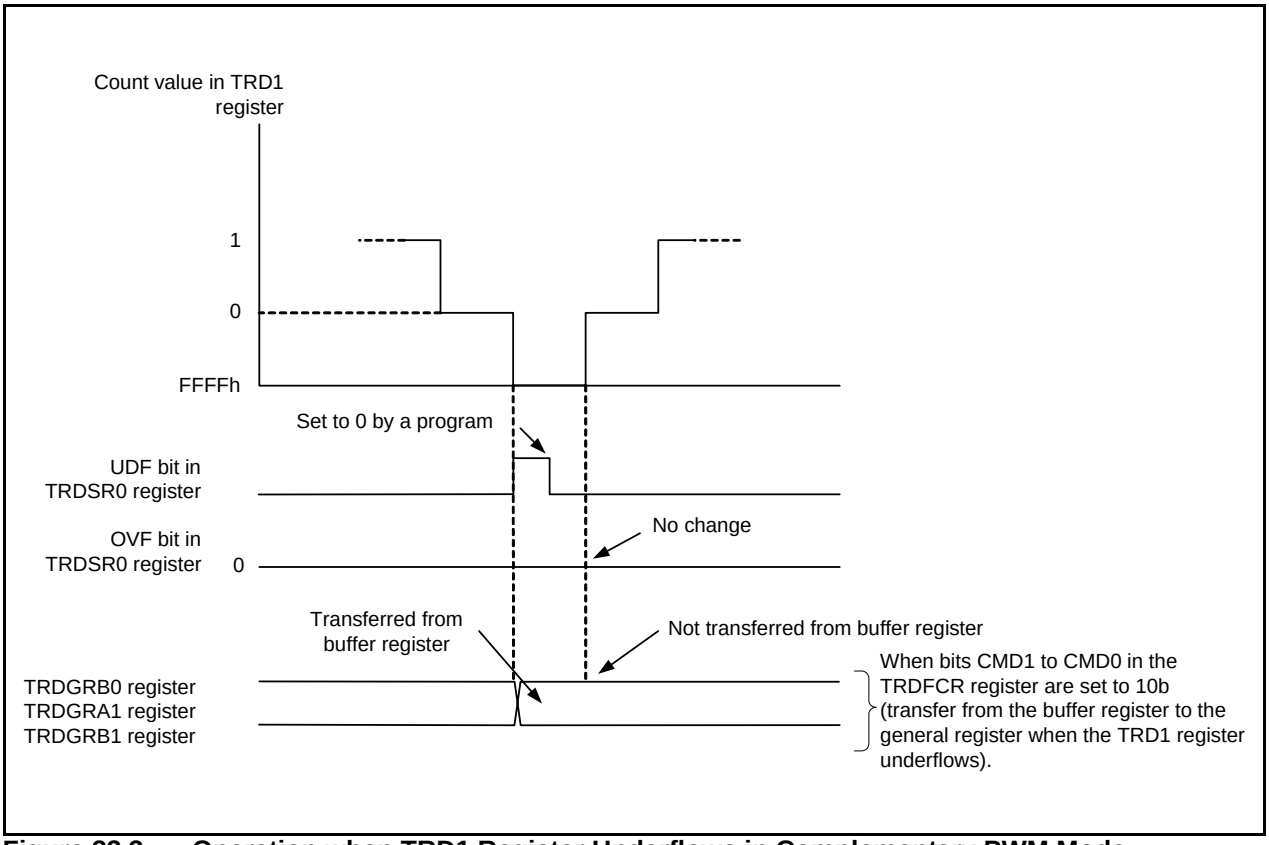
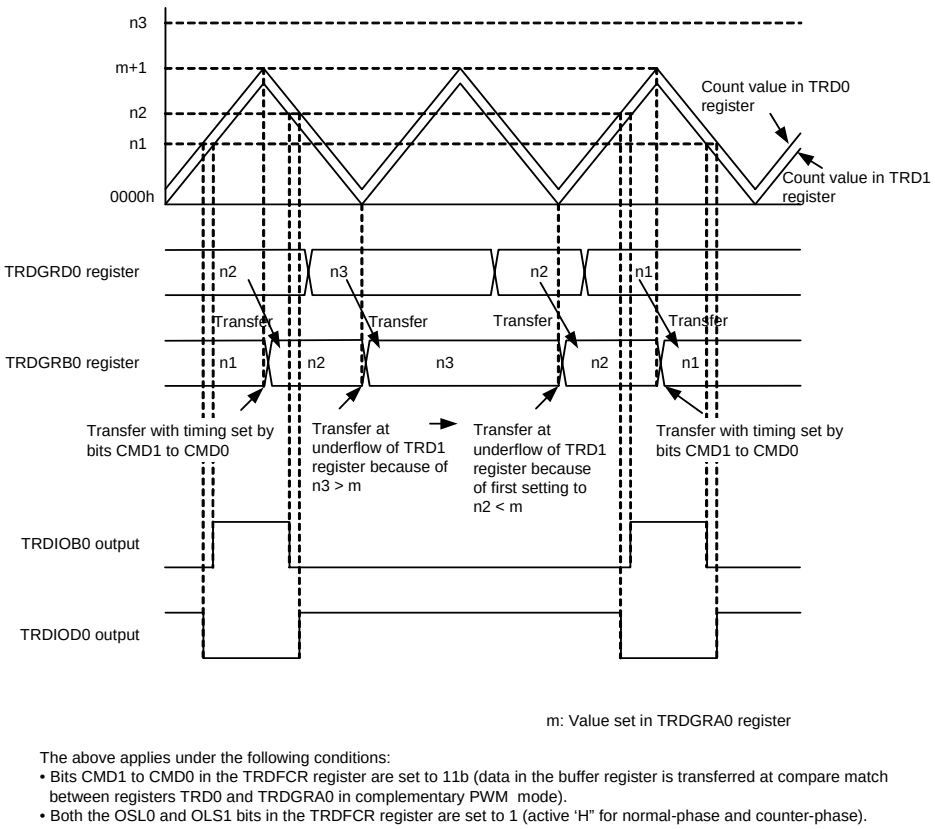


Figure 33.3 Operation when TRD1 Register Underflows in Complementary PWM Mode

- Select with bits CMD1 to CMD0 the timing of data transfer from the buffer register to the general register. However, transfer takes place with the following timing in spite of the value of bits CMD1 to CMD0 in the following cases:

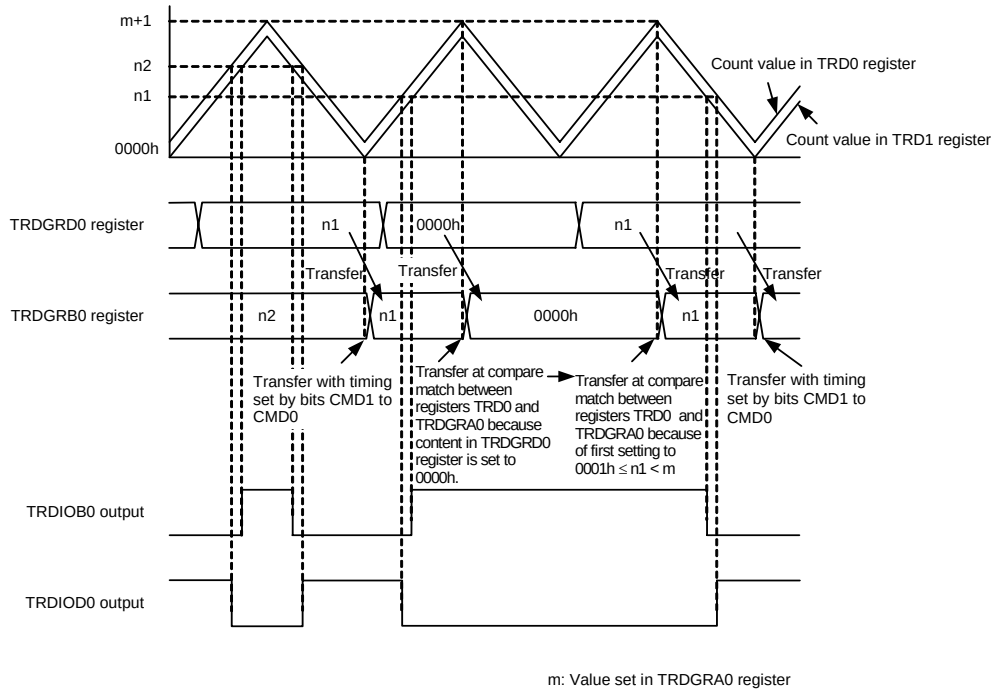
  Value in buffer register ≥ value in TRDGRA0 register:
  Transfer take place at underflow of the TRD1 register.
  After this, when the buffer register is set to 0001h or above and a smaller value than the value of the TRDGRA0 register, and the TRD1 register underflows for the first time after setting, the value is transferred to the general register. After that, the value is transferred with the timing selected by bits CMD1 to CMD0.



The above applies under the following conditions:
- Bits CMD1 to CMD0 in the TRDFCR register are set to 11b (data in the buffer register is transferred at compare match between registers TRD0 and TRDGRA0 in complementary PWM mode).
- Both the OSL0 and OLS1 bits in the TRDFCR register are set to 1 (active ‘H” for normal-phase and counter-phase).

Figure 33.4 Operation when Value in Buffer Register ≥ Value in TRDGRA0 Register in Complementary PWM Mode

When the value in the buffer register is set to 0000h:
Transfer takes place at compare match between registers TRD0 and TRDGRA0.
After this, when the buffer register is set to 0001h or above and a smaller value than the value of the TRDGRA0 register, and a compare match occurs between registers TRD0 and TRDGRA0 for the first time after setting, the value is transferred to the general register. After that, the value is transferred with the timing selected by bits CMD1 to CMD0.



The above applies under the following conditions:
- Bits CMD1 to CMD0 in the TRDFCR register are set to 10b (data in the buffer register is transferred at underflow of the TRD1 register in PWM mode).
- Both the OLS0 and OLS1 bits in the TRDFCR register are set to 1 (active “H” for normal-phase and counter-phase).

Figure 33.5 Operation when Value in Buffer Register Is Set to 0000h in Complementary PWM Mode

33.10 Notes on Timer RE

33.10.1 Starting and Stopping Count

Timer RE has the TSTART bit for instructing the count to start or stop, and the TCSTF bit, which indicates count start or stop. Bits TSTART and TCSTF are in the TRECR1 register.
Timer RE starts counting and the TCSTF bit is set to 1 (count starts) when the TSTART bit is set to 1 (count starts). It takes up to 2 cycles of the count source until the TCSTF bit is set to 1 after setting the TSTART bit to 1. During this time, do not access registers associated with timer RE (1) other than the TCSTF bit.
Also, timer RE stops counting when setting the TSTART bit to 0 (count stops) and the TCSTF bit is set to 0 (count stops). It takes the time for up to 2 cycles of the count source until the TCSTF bit is set to 0 after setting the TSTART bit to 0. During this time, do not access registers associated with timer RE other than the TCSTF bit.

Note:
1. Registers associated with timer RE: TREMIN, TRECR1, TRECR2, and TRECSR.

33.10.2 Register Setting

Write to the following registers or bits when timer RE is stopped.
- Registers TRESEC, TREMIN, and TRECR2
- Bits RCS0 to RCS3 in TRECSR register

Timer RE is stopped when bits TSTART and TCSTF in the TRECR1 register are set to 0 (timer RE stopped).

Also, set all above-mentioned registers and bits (immediately before timer RE count starts) before setting the TRECR2 register.

33.11 Notes on Timer RF

- Access registers TRF, TRFM0, and TRFM1 in 16-bit units.

Example of reading timer RF:

```
MOV.W    0090H,R0    ; Read out timer RF
```

- In input capture mode, a capture interrupt request is generated by inputting an edge selected by bits TRFC03 and TRFC04 in the TRFCR0 register even when the TSTART bit in the TRFCR0 register is set to 0 (count stops).

33.12 Notes on Timer RG

33.12.1 Phase Difference, Overlap, and Pulse Width in Phase Counting Mode

The phase difference and overlap between external input signals from pins TRGCLKA and TRGCLKB should be 1.5 f1 or more, respectively. The pulse width should be 2.5 f1 or more. Figure 33.6 shows the Phase Difference, Overlap, and Pulse Width in Phase Counting Mode.

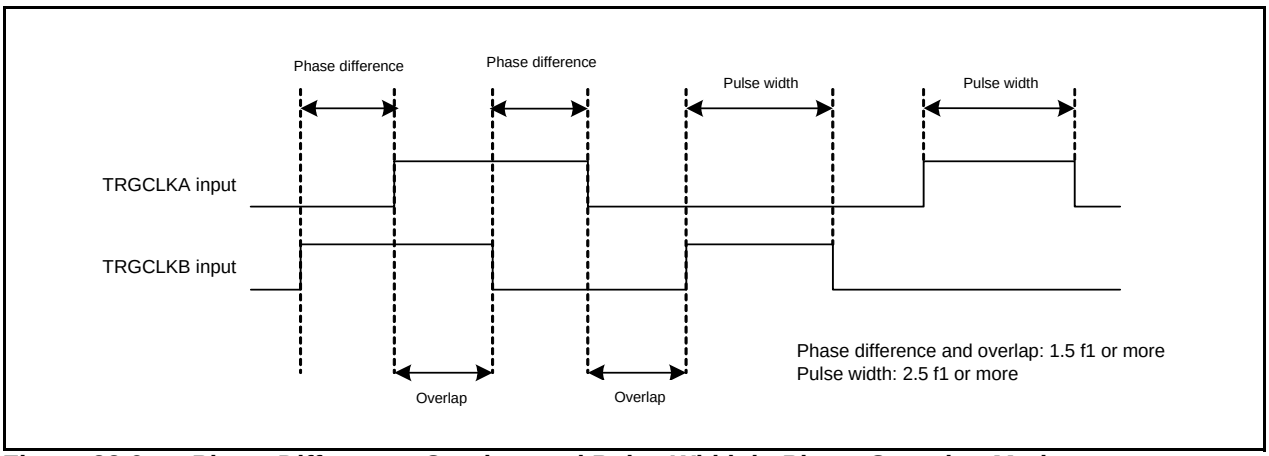


Figure 33.6 Phase Difference, Overlap, and Pulse Width in Phase Counting Mode

33.12.2 Timer RG Counter (TRG)

When writing to the TRG register or TRGCR register, make sure the TSTART bit in the TRGMR register is set to 0 (count stops).

33.12.3 Timer Mode

When using the output compare function in timer mode, use the TRGIOR register to select the compare match output from the following three: low-level output, high-level output, or toggle output. When waveform output mode is selected, the port functions as the compare match output pin (TRGIOA or TRGIOB) while the TRGIOASEL0 bit or the TRGIOBSEL0 bit in the TRGPSR register is 1. The output level of these pins depend on the settings of bits IOA0 and IOA1, or bits IOB0 and IOB1 in the TRGIOR register until the first compare match occurs.

After setting the TRGIOR register, the output level is undefined for one cycle of the timer RG operating clock, and the corresponding level to bits IOA0 and IOA1 or bits IOB0 and IOB1 is output.

33.12.4 PWM Mode

When using PWM mode, the TRGIOA pin becomes the PWM output pin by setting the PWM bit in the TRGMR register to 1 (PWM mode) while the TRGIOASEL0 bit in the TRGPSR register is 1. The output level of the PWM output pin depends on the settings of bits CCLR0 and CCLR1 in the TRGCR register until the first compare match occurs.

After setting the PWM bit, the output level is undefined for one cycle of the timer RG operating clock, and the corresponding level to bits CCLR0 and CCLR1 is output.

33.13 Notes on Serial Interface (UARTi (i = 0 or 1))

- When reading data from the UiRB (i = 0 or 1) register either in clock synchronous serial I/O mode or in clock asynchronous serial I/O mode, always read data in 16-bit units.
  When the high-order byte of the UiRB register is read, bits PER and FER in the UiRB register and the RI bit in the UiC1 register are set to 0.
  To check receive errors, read the UiRB register and then use the read data.

  Program example to read the receive buffer register:
  ```
  MOV.W    00A6H,R0    ; Read the U0RB register
  ```

- When writing data to the UiTB register in clock asynchronous serial I/O mode with 9-bit transfer data length, write data to the high-order byte first and then the low-order byte, in 8-bit units.

  Program example to write to the transmit buffer register:
  ```
  MOV.B    #XXH,00A3H  ; Write to the high-order byte of the U0TB register
  MOV.B    #XXH,00A2H  ; Write to the low-order byte of the U0TB register
  ```

33.14 Notes on Serial Interface (UART2)

33.14.1 Clock Synchronous Serial I/O Mode

33.14.1.1 Transmission/Reception

When the $\overline{\text{RTS}}$ function is used with an external clock, the $\overline{\text{RTS2}}$ pin outputs “L,” which informs the transmitting side that the MCU is ready for a receive operation. The $\overline{\text{RTS2}}$ pin outputs “H” when a receive operation starts. Therefore, the transmit timing and receive timing can be synchronized by connecting the $\overline{\text{RTS2}}$ pin to the $\overline{\text{CTS2}}$ pin of the transmitting side. The $\overline{\text{RTS}}$ function is disabled when an internal clock is selected.

33.14.1.2 Transmission

If an external clock is selected, the following conditions must be met while the external clock is held high when the CKPOL bit in the U2C0 register is set to 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock), or while the external clock is held low when the CKPOL bit is set to 1 (transmit data output at the rising edge and receive data input at the falling edge of the transfer clock).

- The TE bit in the U2C1 register = 1 (transmission enabled)
- The TI bit in the U2C1 register = 0 (data present in the U2TB register)
- If the $\overline{\text{CTS}}$ function is selected, input on the $\overline{\text{CTS2}}$ pin = “L”

33.14.1.3 Reception

In clock synchronous serial I/O mode, the shift clock is generated by activating the transmitter. Set the UART2-associated registers for transmit operation even if the MCU is used for receive operation only. Dummy data is output from the TXD2 pin while receiving.

When an internal clock is selected, the shift clock is generated by setting the TE bit in the U2C1 register to 1 (transmission enabled) and placing dummy data in the U2TB register. When an external clock is selected, set the TE bit to 1 (transmission enabled), place dummy data in the U2TB register, and input an external clock to the CLK2 pin to generate the shift clock.

If data is received consecutively, an overrun error occurs when the RE bit in the U2C1 register is set to 1 (data present in the U2RB register) and the next receive data is received in the UART2 receive register. Then, the OER bit in the U2RB register is set to 1 (overrun error). At this time, the U2RB register value is undefined. If an overrun error occurs, the IR bit in the S2RIC register remains unchanged.

To receive data consecutively, set dummy data in the low-order byte in the U2TB register per each receive operation.

If an external clock is selected, the following conditions must be met while the external clock is held high when the CKPOL bit is set to 0, or while the external clock is held low when the CKPOL bit is set to 1.

- The RE bit in the U2C1 register = 1 (reception enabled)
- The TE bit in the U2C1 register = 1 (transmission enabled)
- The TI bit in the U2C1 register = 0 (data present in the U2TB register)

33.14.2 Special Mode 1 (I^2C Mode)

When generating start, stop, and restart conditions, set the STSPSEL bit in the U2SMR4 register to 0 and wait for more than half cycle of the transfer clock before changing each condition generation bit (STAREQ, RSTAREQ, and STPREQ) from 0 to 1.

33.14.3 UART2 Bit Rate Register (U2BRG)

Immediately after writing 00h to the U2BRG register, there may be a delay of up to 256 cycles of the count source when the following data transmission/reception starts (including the timing when the TI bit in the U2C1 register is set to 0 (data present in the U2TB register)) and when the start bit is detected during reception).

33.15 Note on Synchronous Serial Communication Unit (SSU)

When using the SSU, a maximum of three cycles are required between writing to the SSTDR register and setting the TEND bit or TDRE bit in the SSSR register to 0. When reading the TEND bit or TDRE bit in the SSSR register immediately after writing to the SSTDR register, insert more than three NOP instructions between the write and read instructions.

33.16 Notes on Hardware LIN

For the time-out processing of the header and response fields, use another timer to measure the duration of time with a Synch Break detection interrupt as the starting point.

33.17 Notes on A/D Converter

- Write to the ADMOD register, the ADINSEL register, the ADCON0 register (other than ADST bit), the ADCON1 register, the OCVREFCR register when A/D conversion is stopped (before a trigger occurs).
- To use the A/D converter in repeat mode 0, repeat mode 1, or repeat sweep mode, select the frequency of the A/D converter operating clock ϕAD or more for the CPU clock during A/D conversion.
  Do not select fOCO-F as ϕAD.
- Connect 0.1 μF capacitor between the VREF pin and AVSS pin.
- Do not enter stop mode during A/D conversion.
- Do not enter wait mode during A/D conversion regardless of the state of the CM02 bit in the CM0 register (1: Peripheral function clock stops in wait mode or 0: Peripheral function clock does not stop in wait mode).
- Do not set the FMSTP bit in the FMR0 register to 1 (flash memory stops) or the FMR27 bit to 1 (low-consumption-current read mode enabled) during A/D conversion. Otherwise, the A/D conversion result will be undefined.
- Do not change the CKS2 bit in the ADMOD register while fOCO-F is stopped.
- During an A/D conversion operation, if the ADST bit in the ADCON0 register is set to 0 (A/D conversion stops) by a program to forcibly terminate A/D conversion, the conversion result of the A/D converter is undefined and no interrupt is generated. The value of the ADi register before A/D conversion may also be undefined.
  If the ADST bit is set to 0 by a program, do not use the value of all the ADi register.

33.18 Notes on Flash Memory

33.18.1 CPU Rewrite Mode

33.18.1.1 Prohibited Instructions

The following instructions cannot be used while the program ROM area is being rewritten in EW0 mode because they reference data in the flash memory: UND, INTO, and BRK.

33.18.1.2 Interrupts

Tables 33.2 to 33.4 show CPU Rewrite Mode Interrupts (1), (2) and (3), respectively.

Table 33.2 CPU Rewrite Mode Interrupts (1)

Mode	Erase/ Write Target	Status	Maskable Interrupt
EW0	Data flash (1)	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request). The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0 (erase-suspend request disabled by interrupt request), set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit to 0 (erase restart).
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.
		During auto-programming	
	Program ROM	During auto-erasure (suspend enabled)	Usable by allocating a vector in RAM.
		During auto-erasure (suspend disabled)	
		During auto-programming	
EW1	Data flash (1)	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1, the FMR21 bit is automatically set to 1. The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0, set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit to 0.
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.
		During auto-programming	
	Program ROM	During auto-erasure (suspend enabled)	Auto-erasure suspends after td(SR-SUS) and interrupt handling is executed. Auto-erasure can be restarted by setting the FMR21 bit to 0 after interrupt handling completes. While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written.
		During auto-erasure (suspend disabled or FMR22 = 0)	Auto-erasure and auto-programming have priority and interrupt requests are put on standby. Interrupt handling is executed after auto-erase and auto-program complete.
		During auto-programming	

FMR21, FMR22: Bits in FMR2 register

Note:

1. The R8C/38W Group and R8C/38Y Group have data flash.

Table 33.3 CPU Rewrite Mode Interrupts (2)

Mode	Erase/ Write Target	Status	• Watchdog Timer • Oscillation Stop Detection • Voltage Monitor 2 • Voltage Monitor 1	• Undefined Instruction • INTO Instruction • BRK Instruction • Single Step • Address Match • Address Break (Note 1)
EW0	Data flash (2)	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request). The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0 (erase-suspend request disabled by interrupt request), set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit is set to 0 (erase restart).	When an interrupt request is acknowledged, interrupt handling is executed. If erase-suspend is required, set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit in the FMR2 register is set to 0 (erase restart).
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.	
		During auto-programming		
	Program ROM	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts when the flash memory restarts after the fixed period. Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. After the flash memory restarts, execute auto-erasure again and ensure it completes normally. The watchdog timer does not stop during the command operation, so interrupt requests may be generated. Initialize the watchdog timer regularly using the erase-suspend function.	Not usable during auto-erasure or auto-programming.
		During auto-erasure (suspend disabled)		
		During auto-programming		

FMR21, FMR22: Bits in FMR2 register

Notes:
1. Do not use a non-maskable interrupt while block 0 is being auto-erased because the fixed vector is allocated in block 0.
2. The R8C/38W Group and R8C/38Y Group have data flash.

Table 33.4 CPU Rewrite Mode Interrupts (3)

Mode	Erase/ Write Target	Status	• Watchdog Timer • Oscillation Stop Detection • Voltage Monitor 2 • Voltage Monitor 1	• Undefined Instruction • INTO Instruction • BRK Instruction • Single Step • Address Match • Address Break (Note 1)
EW1	Data flash (2)	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1, the FMR21 bit is automatically set to 1. The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0, set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-programming after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit is set to 0.	When an interrupt request is acknowledged, interrupt handling is executed. If erase-suspend is required, set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit in the FMR2 register is set to 0 (erase restart).
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.	
		During auto-programming		
	Program ROM	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts when the flash memory restarts after the fixed period. Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. After the flash memory restarts, execute auto-erasure again and ensure it completes normally. The watchdog timer does not stop during the command operation, so interrupt requests may be generated. Initialize the watchdog timer regularly using the erase-suspend function.	Not usable during auto-erasure or auto-programming.
		During auto-erasure (suspend disabled or FMR22 = 0)		
		During auto-programming		

FMR21, FMR22: Bits in FMR2 register

Notes:
1. Do not use a non-maskable interrupt while block 0 is being auto-erased because the fixed vector is allocated in block 0.
2. The R8C/38W Group and R8C/38Y Group have data flash.

33.18.1.3 How to Access

To set one of the following bits to 1, first write 0 and then 1 immediately. Disable interrupts and DTC activation between writing 0 and writing 1.
- The FMR01 bit or FMR02 bit in the FMR0 register
- The FMR13 bit in the FMR1 register
- The FMR20 bit, FMR22 bit, or FMR 27 bit in the FMR2 register

To set one of the following bits to 0, first write 1 and then 0 immediately. Disable interrupts and DTC activation between writing 0 and writing 1.
- The FMR14 bit, FMR15 bit, FMR16 bit, or FMR17 bit in the FMR1 register

33.18.1.4 Rewriting User ROM Area

In EW0 mode, if the supply voltage drops while rewriting any block in which a rewrite control program is stored, it may not be possible to rewrite the flash memory because the rewrite control program cannot be rewritten correctly. In this case, use standard serial I/O mode.

33.18.1.5 Programming

Do not write additions to the already programmed address.

33.18.1.6 Entering Stop Mode or Wait Mode

Do not enter stop mode or wait mode during erase-suspend.
If the FST7 bit in the FST register is set to 0 (busy (during programming or erasure execution), do not enter to stop mode or wait mode.
Do not enter stop mode or wait mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

33.18.1.7 Note when data flash is used [R8C/38W Group, R8C/38Y Group]

To use data flash with more than 16 MHz CPU clock, set the FMR23 bit in the FMR2 register to 1 (4 cycles of the CPU clock).

33.18.1.8 Block Blank Check

Do not execute the block blank check command during erase-suspend.

33.18.1.9 Low-Current-Consumption Read Mode

In low-speed on-chip oscillator mode, the current consumption when reading the flash memory can be reduced by setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled).
When the CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16, low-consumption-current read mode can be used. When divided by 1 (no division) or divided by 2 is set, do not use low-consumption-current read mode. After setting the divide ratio of the CPU clock, set the FMR27 bit to 1 (low-current-consumption read mode enabled).
To reduce the power consumption, refer to **31. Reducing Power Consumption**.
Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).
Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

33.19 Notes on Noise

33.19.1 Inserting a Bypass Capacitor between VCC and VSS Pins as a Countermeasure against Noise and Latch-up

Connect a bypass capacitor (approximately 0.1 μF) using the shortest and thickest wire possible.

33.19.2 Countermeasures against Noise Error of Port Control Registers

During rigorous noise testing or the like, external noise (mainly power supply system noise) can exceed the capacity of the MCU's internal noise control circuitry. In such cases the contents of the port related registers may be changed.

As a firmware countermeasure, it is recommended that the port registers, port direction registers, and pull-up control registers be reset periodically. However, examine the control processing fully before introducing the reset routine as conflicts may be created between the reset routine and interrupt routines.

33.20 Note on Supply Voltage Fluctuation

After reset is deasserted, the supply voltage applied to the VCC pin must meet either or both the allowable ripple voltage Vr (vcc) or ripple voltage falling gradient dVr (vcc)/dt shown in Figure 33.7.

Symbol	Parameter	Standard			Unit
		Min.	Typ.	Max.	
Vr (vcc)	Allowable ripple voltage			0.1 VCC	V
dVr (vcc)/dt	Ripple voltage falling gradient			10	V/ms

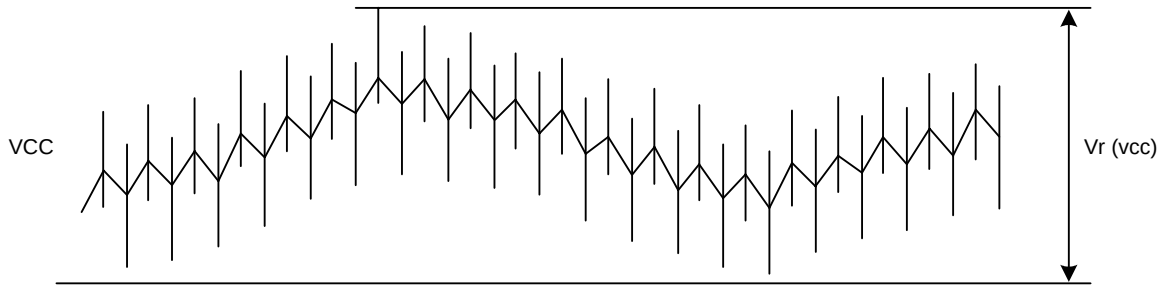


Figure 33.7 Definition of ripple voltage

34. Notes on On-Chip Debugging Emulator

When using the on-chip debugging emulator to develop and debug programs for the this MCU take note of the following.

(1) Some of the user flash memory and RAM areas are used by the on-ship debugger. These areas cannot be accessed by the user.
Refer to the on-chip debugging emulator manual for which areas are used.
(2) Do not set the address match interrupt (registers AIER0, AIER1, RMAD0, and RMAD1 and fixed vector tables) in a user system.
(3) Do not use the BRK instruction in a user system.

Connecting and using the on-chip debugging emulator has some special restrictions. Refer to the on-chip debugging emulator manual for details.

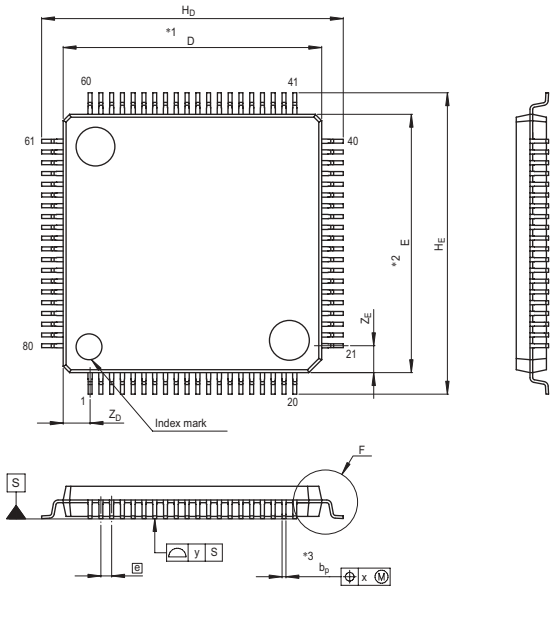
35. Notes on Emulator Debugger

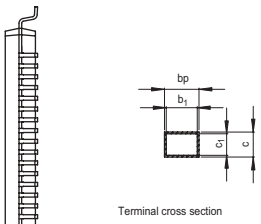
Connecting and using the emulator debugger has some special restrictions. Refer to the emulator debugger manual for details.

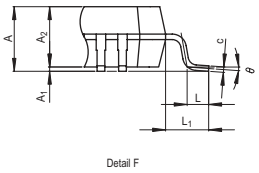
Appendix 1. Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP80-12x12-0.50	PLQP0080KB-A	80P6Q-A	0.5g





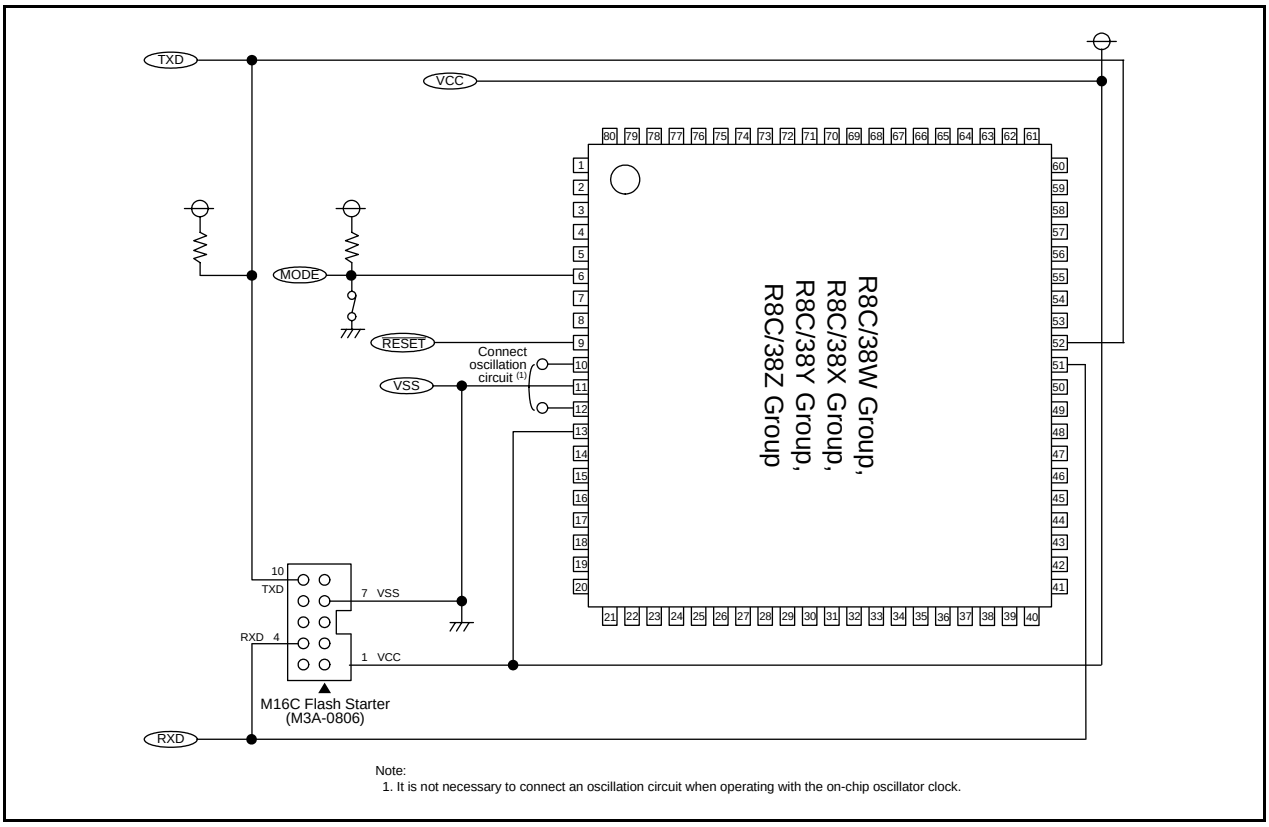


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

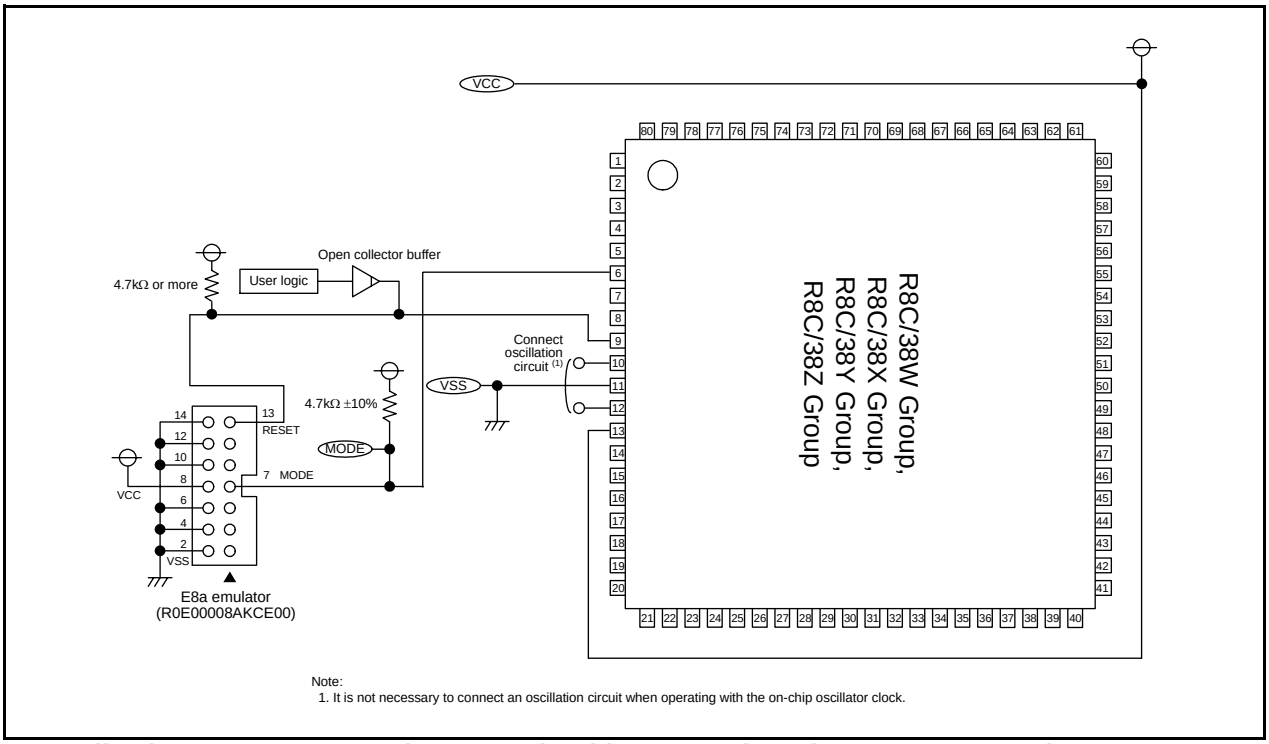
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	10°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.3	0.5	0.7
L_1	—	1.0	—

Appendix 2. Connection Examples between Serial Programmer and On-Chip Debugging Emulator

Appendix Figure 2.1 shows a Connection Example with M16C Flash Starter (M3A-0806) and Appendix Figure 2.2 shows a Connection Example with E8a Emulator (R0E00008AKCE00).



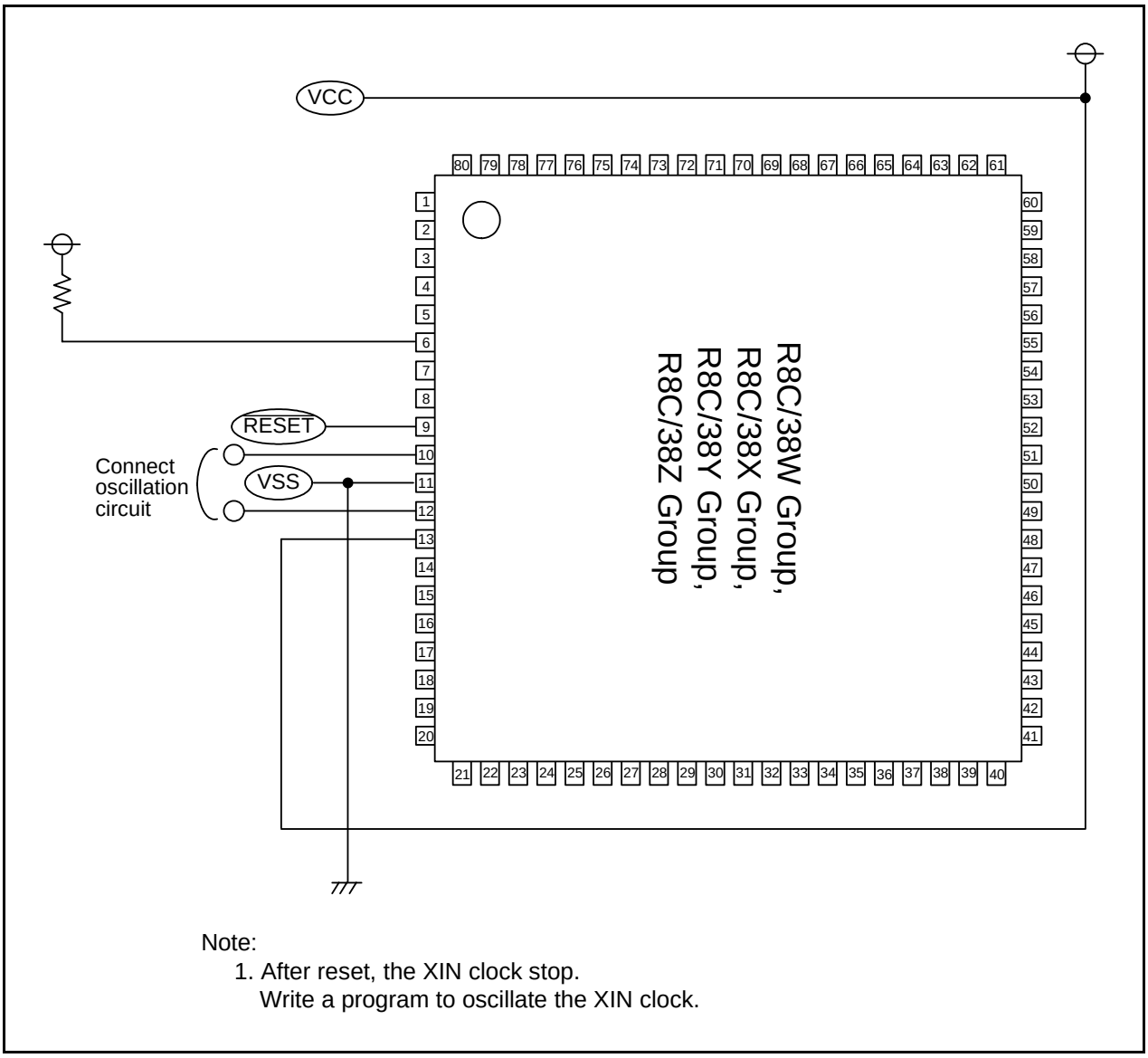
Appendix Figure 2.1 Connection Example with M16C Flash Starter (M3A-0806)



Appendix Figure 2.2 Connection Example with E8a Emulator (R0E00008AKCE00)

Appendix 3. Example of Oscillation Evaluation Circuit

Appendix Figure 3.1 shows an Example of Oscillation Evaluation Circuit.



Note:
1. After reset, the XIN clock stop.
   Write a program to oscillate the XIN clock.

Appendix Figure 3.1 Example of Oscillation Evaluation Circuit

Index

REVISION HISTORY	R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group User's Manual: Hardware

Rev.	Date	Description	
		Page	Summary
0.10	May 31, 2010	—	First Edition issued
1.00	Jun 03, 2013	All	"Preliminary" and "Under development" deleted
		B-1	006Ch, 006Dh, 0072h and 0073h revised
		14	Figure 1.5 "Voltage detection circuit" added
		28	Table 4.2 006Ch, 006Dh, 0072h and 0073h revised
		32, 38 to 43	Table 4.6, Tables 4.12 to 4.17 "After Reset" notation revised
		110	7.4.23 After reset revised
		138	Table 8.3 revised
		139	Table 9.1 Note 3 revised
		144	9.2.3 Note 4 revised
		294	Table 19.7 Count period revised
		324, 768	19.9.7 and 33.8.7 deleted
		434, 772	Figures 20.26 and 33.3 "Count value in TRD0 register" → "Count value in TRD1 register"
		532	Table 25.5 Note 1 revised
		539	25.4.6 "The output level goes high... the CLK2 pin." deleted
		657	Figure 28.17 revised
		674	29.3.3.4 revised
		685	29.9 revised
		736	Table 32.3 "VI > VSS" → "VI < VSS", Note 1 revised
		737	Table 32.4 tSAMP revised
		738	Table 32.5 "1,000 times" → "100 times"
		747	Table 32.15 "VCC = 5.0 V" added
		750	Figure 32.9 revised
		751	Table 32.21 revised
		752	Table 32.23 "[2.7 V ≤ Vcc ≤ 4.2 V]" → "[2.7 V ≤ Vcc < 4.2 V]", "VCC = 3.0 V" added
		753, 754	Tables 32.24 and 32.25 "[2.7 V ≤ Vcc ≤ 3.3 V]" → "[2.7 V ≤ Vcc < 3.3 V]"
		755	Figure 32.14 revised
		756	Table 30.29 revised
		789	Appendix Figure 2.1 Note 1 revised
1.10	Jun 03, 2013	120	Table 7.33 revised
		121	Table 7.36 revised
		127	Table 7.58 revised
		161	9.6.3.2 revised
		162	9.6.3.3 revised
		168, 758	9.8.2, 33.1.2 revised
		232	15.3.8 revised
		236, 764	15.4.2, 15.4.4 revised, "15.4.5 DTC Activation", "15.4.6 Chain transfer", added, 33.5.2, 33.5.4 revised, "33.5.5 DTC Activation", "33.5.6 Chain transfer" added
		255, 765	17.8, 33.6 revised
		466	23.2.7 revised
		467	23.2.8 revised
		516	25.2.3 revised
		538	Figure 25.10 revised
		546	Figure 25.15 revised

REVISION HISTORY	R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group User's Manual: Hardware

Rev.	Date	Description	
		Page	Summary
1.10	Jun 03, 2013	560, 780	"25.8.3 UART2 Bit Rate Register (U2BRG)", "33.14.3 UART2 Bit Rate Register (U2BRG)" added
		591, 780	"26.6 Note on synchronous serial communication unit (SSU)", "33.15 Note on synchronous serial communication unit (SSU)" added
		642	BLIF Bit revised
		649	Figure 28.9 revised
		651	Table 28.9, Note 1 to Note 4 revised
		671	29.2.6 Note 4 added
		682	Table 29.7 revised

R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group
User's Manual: Hardware

Publication Date: Rev.0.10 May 31, 2010
Rev.1.10 Jun 03, 2013

Published by: Renesas Electronics Corporation

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