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R8C/2H Group, R8C/2J Group RENESAS MCU

REJ03B0217-0100 Rev.1.00 Mar 28, 2008

1. Overview

1.1 Features

The R8C/2H Group and R8C/2J Group of single-chip MCUs incorporate the R8C/Tiny Series CPU core, employing sophisticated instructions for a high level of efficiency. With 1 Mbyte of address space, and it is capable of executing instructions at high speed. In addition, the CPU core boasts a multiplier for high-speed operation processing.

Power consumption is low, and the supported operating modes allow additional power control. These MCUs also use an anti-noise configuration to reduce emissions of electromagnetic noise and are designed to withstand EMI. Integration of many peripheral functions, including multifunction timer and serial interface, reduces the number of system components.

1.1.1 Applications

Electric power meters, electronic household appliances, office equipment, audio equipment, consumer equipment, etc.

1.1.2 Specifications

Table 1.1 outlines the Specifications for R8C/2H Group and Table 1.2 outlines the Specifications for R8C/2J Group.

Table 1.1 Specifications for R8C/2H Group

	opecinications to	•			
Item	Function	Specification			
CPU	Central processing	R8C/Tiny series core			
	unit	Number of fundamental instructions: 89			
		Minimum instruction execution time:			
		125 ns (System clock = 8 MHz, VCC = 2.7 to 5.5 V)			
		250 ns (System clock = 4 MHz, VCC = 2.2 to 5.5 V)			
		 Multiplier: 16 bits x 16 bits → 32 bits 			
		 Multiply-accumulate instruction: 16 bits x 16 bits + 32 bits → 32 bits 			
		Operation mode: Single-chip mode (address space: 1 Mbyte)			
Memory	ROM, RAM	Refer to Table 1.3 Product List for R8C/2H Group.			
Power Supply	Voltage detection	Power-on reset			
Voltage	circuit	Voltage detection 3			
Detection					
Comparator		2 circuits (shared with voltage monitor 1 and voltage monitor 2)			
		External reference voltage input is available			
I/O Ports		Output-only: 1			
		CMOS I/O ports: 15, selectable pull-up resistor			
Clock	Clock generation	2 circuits: On-chip oscillator (high-speed, low-speed)			
	circuits	(high-speed on-chip oscillator has a frequency adjustment function),			
		XCIN clock oscillation circuit (32 kHz)			
		• Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16			
		• Low power consumption modes:			
		Standard operating mode (low-speed clock, high-speed on-chip oscillator,			
		low-speed on-chip oscillator), wait mode, stop mode			
		Real-time clock (timer RE)			
Interrupts		External: 3 sources, Internal: 17 sources, Software: 4 sources			
menupis		Priority levels: 7 levels			
Watchdog Time	or .	15 bits × 1 (with prescaler), reset start selectable			
Timer	Timer RA	8 bits × 1 (with 8-bit prescaler)			
Tilliei	TIMETICA	Timer mode (period timer), pulse output mode (output level inverted every			
		period), event counter mode, pulse width measurement mode, pulse period			
		measurement mode			
	Timer RB	8 bits × 1 (with 8-bit prescaler)			
	Tilliel IVD	Timer mode (period timer), programmable waveform generation mode (PWM			
		output), programmable one-shot generation mode, programmable wait one-			
		shot generation mode			
	Timer RE	8 bits × 1			
	Timer KE				
		Real-time clock mode (count seconds, minutes, hours, days of week), output			
	Timer DE	compare mode			
	Timer RF	16 bits × 1 (with capture/compare register pin and compare register pin)			
Coriol	LIADTO LIADTO	Input capture mode, output compare mode			
Serial	UART0, UART2	Clock synchronous serial I/O/UART x 2			
Interface		Harabara HALA (Garan DA HADTO)			
LIN Module		Hardware LIN: 1 (timer RA, UARTO)			
Flash Memory		Programming and erasure voltage: VCC = 2.7 to 5.5 V			
		Programming and erasure endurance: 100 times			
		Program security: ROM code protect, ID code check			
		Debug functions: On-chip debug, on-board flash rewrite function			
Operating Fred	quency/Supply	System clock = 8 MHz (VCC = 2.7 to 5.5 V)			
Voltage		System clock = 4 MHz (VCC = 2.2 to 5.5 V)			
Current consur	mption	5 mA (VCC = 5 V, system clock = 8 MHz)			
		23 µA (VCC = 3 V, wait mode (low-speed on-chip oscillator on))			
		0.7 μA (VCC = 3 V, stop mode, BGR trimming circuit disabled)			
Operating Amb	pient Temperature	-20 to 85°C (N version)			
		-40 to 85°C (D version) ⁽¹⁾			
Package		20-pin LSSOP			
		Package code: PLSP0020JB-A (previous code: 20P2F-A)			
		· · · · · · · · · · · · · · · · · · ·			

NOTE:
1. Specify the D version if D version functions are to be used.



Table 1.2 Specifications for R8C/2J Group

Remain					
unit Number of fundamental instructions: 89 Minimum instruction execution time: 125 ns (System clock = 8 MHz, VCC = 2.7 to 5.5 V) 250 ns (System clock = 4 MHz, VCC = 2.2 to 5.5 V) 250 ns (S					
Minimum instruction execution time: 125 ns (System clock = 8 MHz, VCC = 2.7 to 5.5 V) 250 ns (System clock = 4 MHz, VCC = 2.2 to 5.5 V) Multiplier: 16 bits × 16 bits → 32 bits Multiplier: 16 bits × 16 bits → 32 bits Operation mode: Single-chip mode (address space: 1 Mbyte)					
125 ns (System clock = 8 MHz, VCC = 2.7 to 5.5 V) 250 ns (System clock = 4 MHz, VCC = 2.7 to 5.5 V) 4 Multiplier: 16 bits > 15 bits > 32 bits 6 Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits 6 Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits 7 Operation mode: Single-chip mode (address space: 1 Mbyte) 8 Memory					
250 ns (System clock = 4 MHz, VCC = 2.2 to 5.5 V) • Multiplier: 16 bits x 16 bits x 32 bits • Multiply-accumulate instruction: 16 bits x 16 bits x 20 bits • Multiply-accumulate instruction: 16 bits x 16 bits x 32 bits • Operation mode: Single-chip mode (address space: 1 Mbyte) Memory					
Multiplier: 16 bits × 16 bits → 32 bits					
Multiply-accumulate instruction: 16 bits x 16 bits → 32 bits → 0peration mode: Single-chip mode (address space: 1 Mbyte) Memory ROM, RAM Refer to Table 1.4 Product List for R8C/2J Group.					
Power Supply Voltage detection	S				
Refer to Table 1.4 Product List for R8C/2J Group.	-				
Power Supply Voltage Power-on reset					
Voltage Detection					
Detection Comparator * 2 circuits (shared with voltage monitor 1 and voltage monitor 2) * External reference voltage input is available I/O Ports Clock Clock generation circuits Clock generation circuits * 1 circuits: On-chip oscillator (high-speed, low-speed) (high-speed on-chip oscillator has a frequency adjustment for this power consumption modes: Standard operating mode (high-speed on-chip oscillator, low-speed oscillator), wait mode, stop mode Interrupts * External: 3 sources, Internal: 14 sources, Software: 4 sources * Priority levels: 7 levels Watchdog Timer Timer RA * B bits × 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted operiod), event counter mode, pulse width measurement mode, pulse measurement mode Timer RB * B bits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode output), programmable one-shot generation mode, programmable washot generation mode Timer RE Not implemented Timer RE Not implemented Timer RF 16 bits × 1 (with capture/compare register pin and compare register pin Input capture mode, output compare mode Serial UARTO Clock synchronous serial I/O/UART × 1 Interface LIN Module Hardware LIN: 1 (timer RA, UARTO) * Programming and erasure voltage: VCC = 2.7 to 5.5 V * Programming and erasure voltage: VCC = 2.7 to 5.5 V * Programming and erasure endurance: 100 times * Program security: ROM code protect, ID code check					
External reference voltage input is available					
External reference voltage input is available					
Clock Clock generation circuits Clock generation circuits Clock Clock generation circuits Clock generation goscillator (high-speed on-chip oscillator has a frequency adjustment for prequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 Low power consumption modes: Standard operating mode (high-speed on-chip oscillator, low-speed oscillator), wait mode, stop mode External: 3 sources, Internal: 14 sources, Software: 4 sources Priority levels: 7 levels Priority levels: 7 levels					
Clock circuits Clock generation circuits Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 Low power consumption modes: Standard operating mode (high-speed on-chip oscillator, low-speed oscillator), wait mode, stop mode External: 3 sources, Internal: 14 sources, Software: 4 sources Priority levels: 7 levels Timer RA Timer RA Timer RA Sits × 1 (with 8-bit prescaler), reset start selectable Timer mode (period timer), pulse output mode (output level inverted operiod), event counter mode, pulse width measurement mode, pulse measurement mode Timer RB Sits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode output), programmable one-shot generation mode, programmable waveform generation mode output), programmable one-shot generation mode, programmable waveform generation mode Timer RE Not implemented Timer RF Io bits × 1 (with capture/compare register pin and compare register pin Input capture mode, output compare mode Clock synchronous serial I/O/UART × 1 Interface LIN Module Hardware LIN: 1 (timer RA, UARTO) Programming and erasure voltage: VCC = 2.7 to 5.5 V Programming and erasure endurance: 100 times Program security: ROM code protect, ID code check					
Circuits					
Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 Low power consumption modes: Standard operating mode (high-speed on-chip oscillator, low-speed oscillator), wait mode, stop mode Interrupts	nt function)				
Low power consumption modes: Standard operating mode (high-speed on-chip oscillator, low-speed oscillator), wait mode, stop mode Interrupts	,				
Interrupts External: 3 sources, Internal: 14 sources, Software: 4 sources Priority levels: 7 levels Watchdog Timer Timer RA Timer RA B bits x 1 (with prescaler), reset start selectable Timer mode (period timer), pulse output mode (output level inverted of period), event counter mode, pulse width measurement mode, pulse measurement mode Timer RB B bits x 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode output), programmable one-shot generation mode, programmable washot generation mode Timer RE Not implemented Timer RF I 6 bits x 1 (with apture/compare register pin and compare register pin Input capture mode, output compare mode Clock synchronous serial I/O/UART x 1 Interface LIN Module Hardware LIN: 1 (timer RA, UARTO) Programming and erasure voltage: VCC = 2.7 to 5.5 V Programming and erasure endurance: 100 times Program security: ROM code protect, ID code check					
External: 3 sources, Internal: 14 sources, Software: 4 sources	ed on-chip				
Watchdog Timer Timer RA B bits x 1 (with prescaler), reset start selectable Timer RA B bits x 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted of period), event counter mode, pulse width measurement mode, pulse measurement mode Timer RB B bits x 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode output), programmable one-shot generation mode, programmable wayshot generation mode Timer RE Not implemented Timer RF Input capture mode, output compare register pin and compare register pin Input capture mode, output compare mode Serial UARTO Clock synchronous serial I/O/UART x 1 Interface LIN Module Hardware LIN: 1 (timer RA, UARTO) Programming and erasure voltage: VCC = 2.7 to 5.5 V Programming and erasure endurance: 100 times Program security: ROM code protect, ID code check					
Timer RA					
Timer RA S bits x 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted of period), event counter mode, pulse width measurement mode, pulse measurement mode Timer RB					
Timer mode (period timer), pulse output mode (output level inverted of period), event counter mode, pulse width measurement mode, pulse measurement mode Timer RB 8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode output), programmable one-shot generation mode, programmable was shot generation mode Timer RE Not implemented Timer RF 16 bits × 1 (with capture/compare register pin and compare register pin Input capture mode, output compare mode Clock synchronous serial I/O/UART × 1 Interface LIN Module Hardware LIN: 1 (timer RA, UARTO) Programming and erasure voltage: VCC = 2.7 to 5.5 V Programming and erasure endurance: 100 times Program security: ROM code protect, ID code check					
period), event counter mode, pulse width measurement mode, pulse measurement mode Timer RB 8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode output), programmable one-shot generation mode, programmable washot generation mode Timer RE Not implemented Timer RF 16 bits × 1 (with capture/compare register pin and compare register pin Input capture mode, output compare mode Serial Interface UARTO Clock synchronous serial I/O/UART × 1 Interface LIN Module Hardware LIN: 1 (timer RA, UARTO) Programming and erasure voltage: VCC = 2.7 to 5.5 V Programming and erasure endurance: 100 times Program security: ROM code protect, ID code check					
measurement mode Timer RB 8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode output), programmable one-shot generation mode, programmable washot generation mode Timer RE Not implemented Timer RF 16 bits × 1 (with capture/compare register pin and compare register pin Input capture mode, output compare mode Serial Interface UARTO Clock synchronous serial I/O/UART × 1 Interface LIN Module Hardware LIN: 1 (timer RA, UARTO) Programming and erasure voltage: VCC = 2.7 to 5.5 V Programming and erasure endurance: 100 times Program security: ROM code protect, ID code check	d every				
Timer RB 8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode output), programmable one-shot generation mode, programmable washot generation mode Timer RE Not implemented Timer RF 16 bits × 1 (with capture/compare register pin and compare register pin Input capture mode, output compare mode Serial Interface UARTO Clock synchronous serial I/O/UART × 1 Interface LIN Module Hardware LIN: 1 (timer RA, UARTO) Programming and erasure voltage: VCC = 2.7 to 5.5 V Programming and erasure endurance: 100 times Program security: ROM code protect, ID code check	se period				
Timer mode (period timer), programmable waveform generation mode output), programmable one-shot generation mode, programmable washot generation mode Timer RE Not implemented Timer RF 16 bits × 1 (with capture/compare register pin and compare register pin Input capture mode, output compare mode Serial Interface LIN Module Hardware LIN: 1 (timer RA, UARTO) Flash Memory Programming and erasure voltage: VCC = 2.7 to 5.5 V Programming and erasure endurance: 100 times Program security: ROM code protect, ID code check					
output), programmable one-shot generation mode, programmable washot generation mode Timer RE Not implemented Timer RF 16 bits x 1 (with capture/compare register pin and compare register pin Input capture mode, output compare mode Serial Interface LIN Module Hardware LIN: 1 (timer RA, UARTO) Flash Memory Programming and erasure voltage: VCC = 2.7 to 5.5 V Programming and erasure endurance: 100 times Program security: ROM code protect, ID code check					
shot generation mode Timer RE Not implemented Timer RF 16 bits × 1 (with capture/compare register pin and compare register pin Input capture mode, output compare mode Serial Interface LIN Module Hardware LIN: 1 (timer RA, UARTO) Flash Memory Programming and erasure voltage: VCC = 2.7 to 5.5 V Programming and erasure endurance: 100 times Program security: ROM code protect, ID code check					
Timer RE Timer RF Tim	wait one-				
Timer RF 16 bits × 1 (with capture/compare register pin and compare register pin Input capture mode, output compare mode Serial Interface LIN Module Flash Memory Programming and erasure voltage: VCC = 2.7 to 5.5 V Programming and erasure endurance: 100 times Program security: ROM code protect, ID code check					
Input capture mode, output compare mode Serial UARTO Clock synchronous serial I/O/UART x 1 Interface IIN Module Hardware LIN: 1 (timer RA, UARTO) Flash Memory Programming and erasure voltage: VCC = 2.7 to 5.5 V Programming and erasure endurance: 100 times Program security: ROM code protect, ID code check					
Serial UARTO Clock synchronous serial I/O/UART x 1 Interface LIN Module Hardware LIN: 1 (timer RA, UARTO) Flash Memory • Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 100 times • Program security: ROM code protect, ID code check	pin)				
Interface LIN Module Hardware LIN: 1 (timer RA, UART0) Flash Memory • Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 100 times • Program security: ROM code protect, ID code check					
LIN Module Hardware LIN: 1 (timer RA, UART0) Programming and erasure voltage: VCC = 2.7 to 5.5 V Programming and erasure endurance: 100 times Program security: ROM code protect, ID code check					
 Programming and erasure voltage: VCC = 2.7 to 5.5 V Programming and erasure endurance: 100 times Program security: ROM code protect, ID code check 					
 Programming and erasure endurance: 100 times Program security: ROM code protect, ID code check 					
Program security: ROM code protect, ID code check					
Debug functions: On-chip debug, on-board flash rewrite function					
	System clock = 8 MHz (VCC = 2.7 to 5.5 V)				
	System clock = 4 MHz (VCC = 2.2 to 5.5 V)				
Current consumption 5 mA (VCC = 5 V, system clock = 8 MHz)					
23 μ A (VCC = 3 V, wait mode (low-speed on-chip oscillator on))					
$0.7 \mu A \text{ (VCC} = 3 \text{ V, stop mode, BGR trimming circuit disabled)}$					
Operating Ambient Temperature -20 to 85°C (N version)					
-40 to 85°C (D version) ⁽¹⁾					
Package 20-pin LSSOP					
Package code: PLSP0020JB-A (previous code: 20P2F-A)					

NOTE:

1. Specify the D version if D version functions are to be used.



1.2 Product List

Table 1.3 lists Product List for R8C/2H Group, Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/2H Group. Table 1.4 lists Product List for R8C/2J Group, Figure 1.2 shows a Part Number, Memory Size, and Package of R8C/2J Group.

Table 1.3 Product List for R8C/2H Group

Current of Mar. 2008

Part No.	ROM Capacity	RAM Capacity	Package Type	Remarks
R5F212H1SNSP	4 Kbytes	256 bytes	PLSP0020JB-A	N version
R5F212H2SNSP	8 Kbytes	384 bytes	PLSP0020JB-A	
R5F212H1SDSP	4 Kbytes	256 bytes	PLSP0020JB-A	D version
R5F212H2SDSP	8 Kbytes	384 bytes	PLSP0020JB-A	

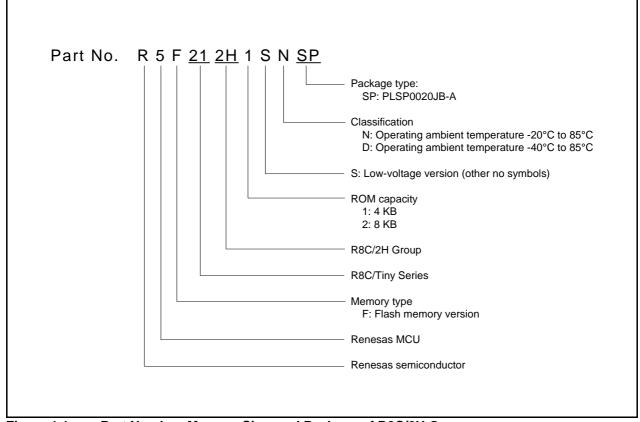
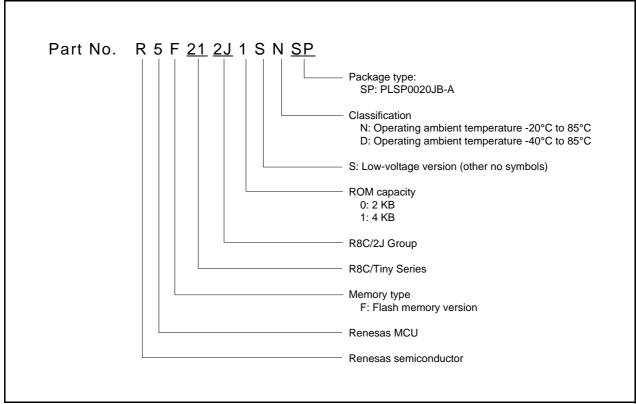


Figure 1.1 Part Number, Memory Size, and Package of R8C/2H Group

Table 1.4 **Product List for R8C/2J Group**

Current of Mar. 2008

Part No.	ROM Capacity	RAM Capacity	Package Type	Remarks
R5F212J0SNSP	2 Kbytes	256 bytes	PLSP0020JB-A	N version
R5F212J1SNSP	4 Kbytes	384 bytes	PLSP0020JB-A	
R5F212J0SDSP	2 Kbytes	256 bytes	PLSP0020JB-A	D version
R5F212J1SDSP	4 Kbytes	384 bytes	PLSP0020JB-A	



Part Number, Memory Size, and Package of R8C/2J Group Figure 1.2

1.3 Block Diagram

Figure 1.3 shows a Block Diagram of R8C/2H Group and Figure 1.4 shows a Block Diagram of R8C/2J Group.

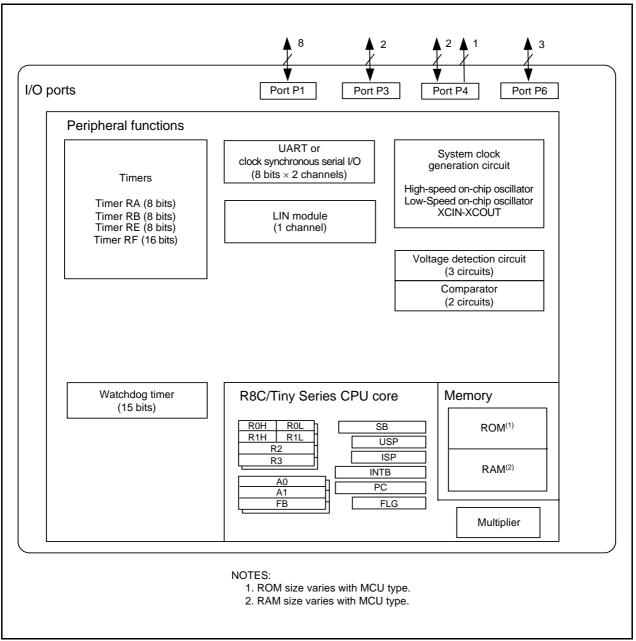


Figure 1.3 Block Diagram of R8C/2H Group

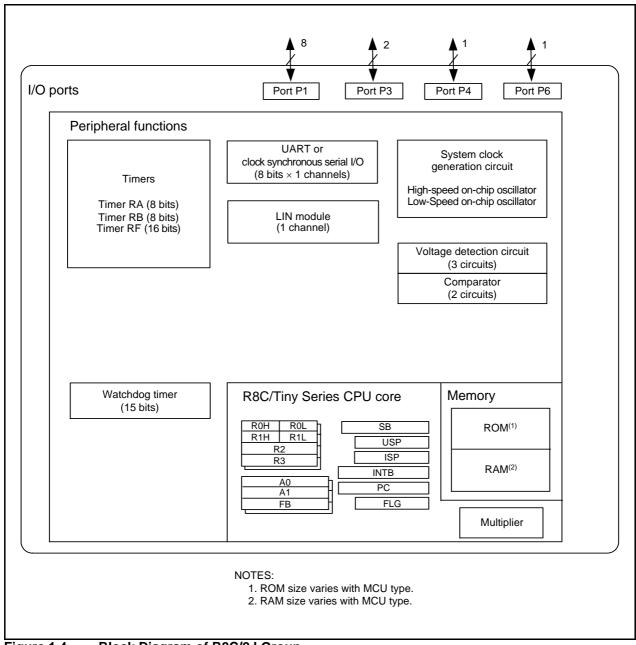


Figure 1.4 Block Diagram of R8C/2J Group

1.4 Pin Assignment

Figure 1.5 shows Pin Assignment (Top View) of R8C/2H Group. Table 1.5 outlines the Pin Name Information by Pin Number of R8C/2H Group.

Figure 1.6 shows Pin Assignment (Top View) of R8C/2J Group. Table 1.6 outlines the Pin Name Information by Pin Number of R8C/2J Group.

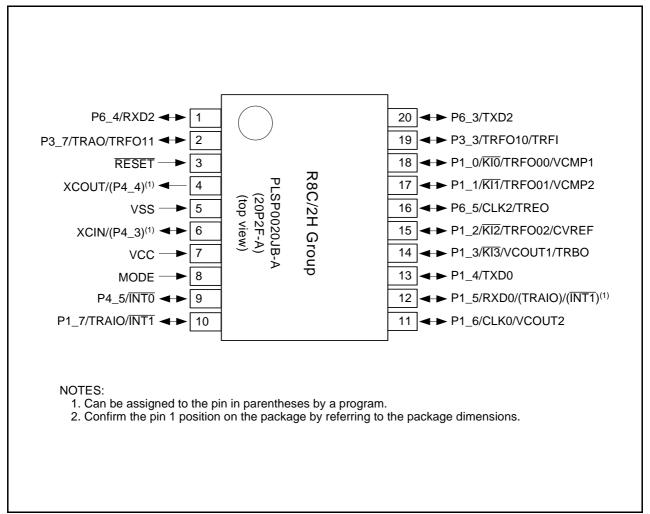


Figure 1.5 Pin Assignment (Top View) of R8C/2H Group

Pin Name Information by Pin Number of R8C/2H Group Table 1.5

Pin	Control Pin	Port	I/O Pin Functions for of Peripheral Modules			
Number	Control Fill	Foit	Interrupt	Timer	Serial Interface	Comparator
1		P6_4			RXD2	
2		P3_7		TRAO/TRFO11		
3	RESET					
4	XCOUT	(P4_4)				
5	VSS					
6	XCIN	(P4_3)				
7	VCC					
8	MODE					
9		P4_5	ĪNT0			
10		P1_7	ĪNT1	TRAIO		
11		P1_6			CLK0	VCOUT2
12		P1_5	(INT1) ⁽¹⁾	(TRAIO) ⁽¹⁾	RXD0	
13		P1_4			TXD0	
14		P1_3	KI3	TRBO		VCOUT1
15		P1_2	KI2	TRFO02		CVREF
16		P6_5		TREO	CLK2	
17		P1_1	KI1	TRFO01		VCMP2
18		P1_0	KI0	TRFO00		VCMP1
19		P3_3		TRFO10/TRFI		
20		P6_3			TXD2	

NOTE:

1. Can be assigned to the pin in parentheses by a program.

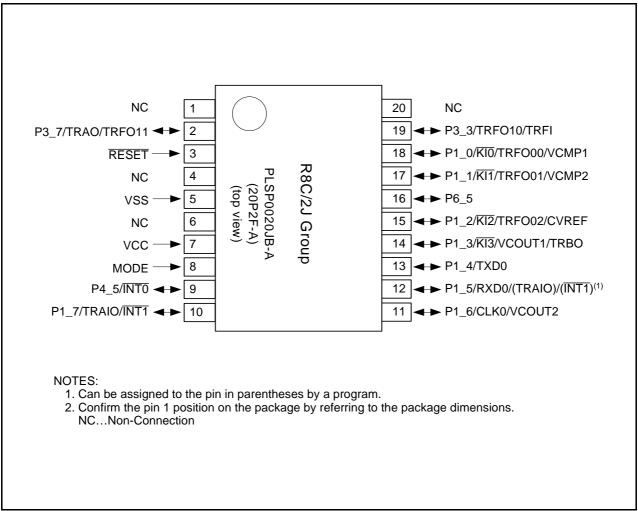


Figure 1.6 Pin Assignment (Top View) of R8C/2J Group

Table 1.6 Pin Name Information by Pin Number of R8C/2J Group

Pin	Control Pin	Port	I/O Pin Functions for of Peripheral Modules			
Number	Control Pill	Poit	Interrupt	Timer	Serial Interface	Comparator
1	NC ⁽²⁾					
2		P3_7		TRAO/TRFO11		
3	RESET					
4	NC ⁽²⁾					
5	VSS					
6	NC ⁽²⁾					
7	VCC					
8	MODE					
9		P4_5	ĪNT0			
10		P1_7	ĪNT1	TRAIO		
11		P1_6			CLK0	VCOUT2
12		P1_5	(INT1) ⁽¹⁾	(TRAIO) ⁽¹⁾	RXD0	
13		P1_4			TXD0	
14		P1_3	KI3	TRBO		VCOUT1
15		P1_2	KI2	TRFO02		CVREF
16		P6_5				
17		P1_1	KI1	TRFO01		VCMP2
18		P1_0	KI0	TRFO00		VCMP1
19		P3_3		TRFO10/TRFI		
20	NC ⁽²⁾					

- 1. Can be assigned to the pin in parentheses by a program.
- 2. NC(Non-Connection)

1.5 **Pin Functions**

Table 1.7 lists Pin Functions of R8C/2H Group and Table 1.8 lists Pin Functions of R8C/2J Group.

Table 1.7 Pin Functions of R8C/2H Group

Туре	Symbol	I/O Type	Description
Power supply input	VCC, VSS	_	Apply 2.2 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Reset input	RESET	I	Input "L" on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XCIN clock input	XCIN	I	These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between the XCIN and XCOUT
XCIN clock output	XCOUT	0	pins. ⁽¹⁾ To use an external clock, input it to the XCIN pin and leave the XCOUT pin open.
INT interrupt input	ĪNTO, ĪNT1	I	INT interrupt input pins
Key input interrupt	KI0 to KI3	I	Key input interrupt input pins
Timer RA	TRAIO	I/O	Timer RA I/O pin
	TRAO	0	Timer RA output pin
Timer RB	TRBO	0	Timer RB output pin
Timer RE	TREO	0	Divided clock output pin
Timer RF	TRFI	I	Timer RF input pin
	TRFO00 to TRFO02, TRFO10 to TRFO11	0	Timer RF output pins
Serial interface	CLK0, CLK2	I/O	Clock I/O pin
	RXD0, RXD2	I	Serial data input pin
	TXD0, TXD2	0	Serial data output pin
Comparator	VCMP1, VCMP2	I	Analog input pins to comparator
	CVREF	I	Reference voltage input pin to comparator
	VCOUT1, VCOUT2	0	Comparator output pins
I/O port	P1_0 to P1_7, P3_3, P3_7, P4_3, P4_5, P6_3 to P6_5	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program.
Output port	P4_4	0	Output-only port

I: Input NOTE:

O: Output

I/O: Input and output

1. Refer to the oscillator manufacturer for oscillation characteristics.

Pin Functions of R8C/2J Group Table 1.8

Type	Symbol	I/O Type	Description
Power supply input	VCC, VSS	_	Apply 2.2 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Reset input	RESET	I	Input "L" on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
INT interrupt input	ĪNTO, ĪNT1	I	INT interrupt input pins
Key input interrupt	KI0 to KI3	I	Key input interrupt input pins
Timer RA	TRAIO	I/O	Timer RA I/O pin
	TRAO	0	Timer RA output pin
Timer RB	TRBO	0	Timer RB output pin
Timer RF	TRFI	I	Timer RF input pin
	TRFO00 to TRFO02, TRFO10 to TRFO11	0	Timer RF output pins
Serial interface	CLK0	I/O	Clock I/O pin
	RXD0	I	Serial data input pin
	TXD0	0	Serial data output pin
Comparator	VCMP1, VCMP2	I	Analog input pins to comparator
	CVREF	I	Reference voltage input pin to comparator
	VCOUT1, VCOUT2	0	Comparator output pins
I/O port	P1_0 to P1_7, P3_3, P3_7, P4_5, P6_5	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program.

I: Input

O: Output

I/O: Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.

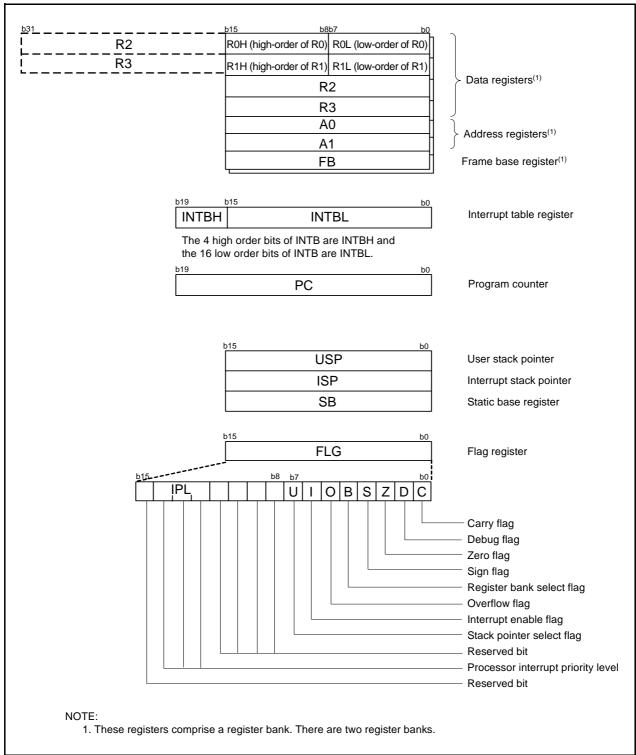


Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 to be used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 **Zero Flag (Z)**

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 **Sign Flag (S)**

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.



2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.

Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.

The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7. If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.



3. Memory

Figure 3.1 is a Memory Map of R8C/2H Group and Figure 3.2 is a Memory Map of R8C/2J Group. The R8C/2H group has 1 Mbyte of address space from addresses 00000h to FFFFFh.

The internal ROM is allocated lower addresses, beginning with address 0FFFFh. For example, a 4-Kbyte internal ROM area is allocated addresses 0F000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal RAM is allocated higher addresses beginning with address 00400h. For example, a 256-bytes internal RAM area is allocated addresses 00400h to 004FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.

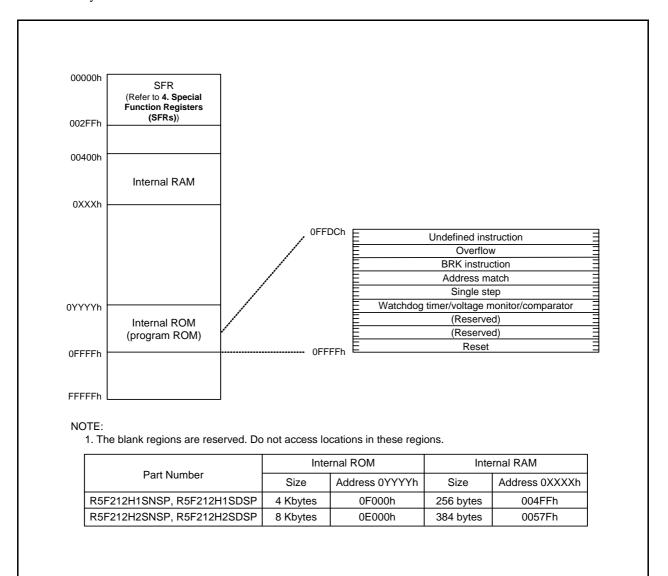


Figure 3.1 Memory Map of R8C/2H Group

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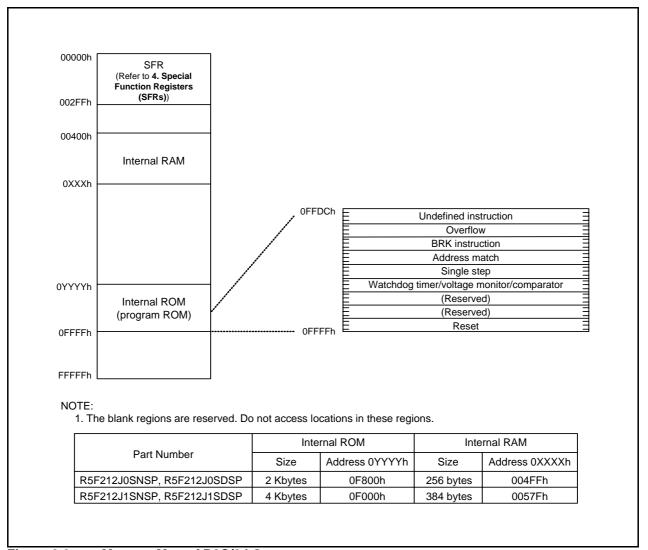


Figure 3.2 Memory Map of R8C/2J Group

Special Function Registers (SFRs) 4.

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.12 list the special function registers.

Table 4.1 SFR Information (1)⁽¹⁾

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01011000b
0007h	System Clock Control Register 1	CM1	00h
0008h			
0009h			
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	System Clock Select Register ⁽³⁾	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00X11111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			00h
0013h	Address Match Interrupt Enable Register	AIER	00h
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			00h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b ⁽²⁾
001Dh		+	100000000
001Eh			
001En		+	
0020h	High-Speed On-Chip Oscillator Control Register 0	HRA0	00h
0020h	High-Speed On-Chip Oscillator Control Register 1	HRA1	When Shipping
0021h	High-Speed On-Chip Oscillator Control Register 2	HRA2	00h
0022h	Thigh opoda on only oscillator control register 2	111012	3311
0023h			
002411 0025h			
0026h			
0027h			1
0028h	Clock Prescaler Reset Flag ⁽³⁾	CPSRF	00h
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	When Shipping
0023h	- ing.: Open and only obstitute of the region of	11001	Titlett Cimpping
002An	High-Speed On-Chip Oscillator Control Register 6	FRA6	When Shipping
002Dh	Thigh opoda on only oscillator control register o	11010	Titlett Ottipping
002Dh			
002Eh	BGR Trimming Auxiliary Register A	BGRTRMA	When Shipping
	BGR Trimming Auxiliary Register B	BGRTRMB	When Shipping

X: Undefined

- NOTES:

 1. The blank regions are reserved. Do not access locations in these regions.

 2. The CSPROINI bit in the OFS register is set to 0.

 3. This register is not implemented in the R8C/2J Group.

SFR Information (2)⁽¹⁾ Table 4.2

A dalraga	Desistes	Cumple of	After recet
Address	Register	Symbol	After reset
0030h			
0031h	Voltage Detection Register 1 ⁽²⁾	VCA1	00001000b
0032h	Voltage Detection Register 2 ⁽²⁾	VCA2	00h ⁽³⁾
000211	Vollage Detection Register 21-7	10/12	
			00100000b ⁽⁴⁾
0033h			
0034h			
0035h		+	- -
	(-)		
0036h	Voltage Monitor 1 Circuit Control Register ⁽⁵⁾	VW1C	00001010b
0037h	Voltage Monitor 2 Circuit Control Register ⁽⁵⁾	VW2C	00000010b
0038h	Voltage Monitor 0 Circuit Control Register ⁽²⁾	VW0C	1000X010b ⁽³⁾
003011	Voltage Monitor o Circuit Control Register(=)	******	
			1100X011b ⁽⁴⁾
0039h			
003Ah			
003Bh	Voltage Detection Circuit Futernal Innut Control Devictor	VCAB	00h
	Voltage Detection Circuit External Input Control Register		
003Ch	Comparator Mode Register	ALCMR	00h
003Dh	Voltage Monitor Circuit Edge Select Register	VCAC	00h
003Eh	BGR Control Register	BGRCR	00h
003Fh		BGRTRM	
	BGR Trimming Register	DUKTKIVI	When Shipping
0040h			
0041h	Comparator 1 Interrupt Control Register	VCMP1IC	XXXXX000b
0042h	Comparator 2 Interrupt Control Register	VCMP2IC	XXXXX000b
0043h		. 5 2.5	
0044h			
0045h			
0046h			
0047h			
1			
0048h			
0049h			
004Ah	Timer RE Interrupt Control Register ⁽⁶⁾	TREIC	XXXXX000b
004Bh	UART2 Transmit Interrupt Control Register ⁽⁶⁾	S2TIC	XXXXX000b
004Ch	UART2 Receive Interrupt Control Register ⁽⁶⁾	S2RIC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	., , , ,		
1			
004Fh			
0050h	Compare 1 Interrupt Control Register	CMP1IC	XXXXX000b
0051h	UART0 Transmit Interrupt Control Register	SOTIC	XXXXX000b
0052h	UARTO Receive Interrupt Control Register	SORIC	XXXXX000b
0053h	Office receive interrupt control register	001110	700000000
0054h			
0055h			
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h	Timor to timorrapt control register	110.00	700000000
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah			
005Bh	Timer RF Interrupt Control Register	TRFIC	XXXXX000b
005Ch	Compare 0 Interrupt Control Register	CMP0IC	XXXXX000b
005Dh	INT0 Interrupt Control Register	INTOIC	XX00X000b
005Eh			
005Fh	Capture Interrupt Control Register	CAPIC	XXXXX000b
	Saprano minimpri control regional	0,1110	70000000
0060h			
0061h			
0062h			
0063h			
			+
0064h			
0065h			
0066h			<u> </u>
0067h			
0068h			+
1			
0069h			
006Ah			
006Bh			
			
006Ch			
006Dh			
006Eh			
006Fh			-
	i e e e e e e e e e e e e e e e e e e e		

X: Undefined

- The blank regions are reserved. Do not access locations in these regions.
- Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect this register. The LVD0ON bit in the OFS register is set to 1 and hardware reset. Power-on reset, voltage monitor 0 reset, or the LVD0ON bit in the OFS register is set to 0 and hardware reset. Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect b2 and b3. This register is not implemented in the R8C/2J Group.

SFR Information (3)⁽¹⁾ Table 4.3

0079h 0079	Address	Register	Symbol	After reset
0071h 0073h 0073h 0073h 0073h 0073h 0073h 0073h 0073h 0075h 0075h 0075h 0077h 0077		· · · · · · · · · · · · · · · · · · ·		
0072h 0074h 0074h 0075h 0076h 0076h 0076h 0077h 0077				
9079h 9079h 9077h 9077h 9077h 9077h 9077h 9077h 9079h				
0074h				
0076h				
0076h 0078h 00078h 00078h 0008h 00				
007th 008th 008t				
0079h				
0078h 008h 00				
007Ah 007Ch 007Ch 007Ch 007Eh 007Eh 007Fh 008Dh 008th 008th 008th 008th 008th 008th 008th 009th 009th 000th 004th <td></td> <td></td> <td></td> <td></td>				
008th				
007Ch	007Ah			
007Eh 007Fh 007Fh 007Fh 0080h 0081h 0082h 0082h 0082h 0088h 0082h 0088h 0082h 0088h 0082h 0088h 0083h 0088h 0084h 0086h 0085h 0086h 0086h 0086h 0087h 0080h 0088h 0096h 0089h 0096h 0089h 0097h 0099h 0099h 0093h 0099h 0099h 0099h 0099h 0099h 0099h 0099h 0099h 0099h 0099h 0099h 0091h 0090h 0092h 0091h 0093h 0093h 0093h 0096h 0097h 0097h 0098h 0096h 0097h 0097h 0098h 0097h 0097h <td>007Bh</td> <td></td> <td></td> <td></td>	007Bh			
007Eh 0080h 0081h 0081h 0082h 0082h 0083h 0083h 0086h 0086h 0087h 0086h 0087h 0086h 0087h 0086h 0087h 0086h 0087h 0086h 0087h 0087h 0087h 0087h 0087h 0097h 0097h 0097h 0097h 0097h 0098h 0098h 0098h 0098h 0098h 0098h 0098h 0098h 0098h 0098h 0098h 0098h 0097h 0098h 0098h 0099h 0098h 0099h 0097h 0098h 0098h 0099h 0098h 0099h 0097h 0098h 0098h 0099h 0097h 0098h 0097h 0099h 0097h <td>007Ch</td> <td></td> <td></td> <td></td>	007Ch			
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0086h				
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0088h 0080h 008ch 008ch 008eh 008eh 008eh 009eh 0091h 0091h 0092h 0093h 0093h 0094h 0095h 0096h 0097h 0097h 0098h 0099h 0099h 0090h 0091h 0090h 0092h <td>0088h</td> <td></td> <td></td> <td></td>	0088h			
0088h 0080h 008ch 008ch 008eh 008eh 008eh 009eh 0091h 0091h 0092h 0093h 0093h 0094h 0095h 0096h 0097h 0097h 0098h 0099h 0099h 0090h 0091h 0090h 0092h <td>0089h</td> <td></td> <td></td> <td></td>	0089h			
OBBR OBBCh OBBCh				
008Ch 008Dh 008Eh 008Fh 0090h 0090h 0091h 0091h 0092h 0093h 0093h 0094h 0095h 0096h 0097h 0097h 0098h 0099h 0098h 0099h 0090h 009Ch 009Ch 009Ch 009Fh 009Fh 009Ch 009Fh 009Ch 009Ch 009Fh 009Ch 009Ch 0040h UARTO Transmit/Receive Mode Register UOMR 00h 0041h UARTO Transmit Usefer Register UOBRG XXh 00A3h UARTO Transmit/Receive Control Register 0 UOC0 00001000b 00A5h UARTO Transmit/Receive Control Register 1 UOC1 00000010b 00A6h UARTO Transmit/Receive Control Register 1 UOC1 00000010b 00A6h UARTO Receive Buffer Register UORB XXh 00A8h 00A9h 00A8h 00ABh 00ACh 00ACh 00ABh 00ACh <				
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008Eh				
008Fh 0090h 0091h 0092h 0093h 0093h 0094h 0095h 0096h 0097h 0098h 0099h 0099h 0098h 0099h 0090h 0090h 0090h 0091h 0090h 0092h 0090h 0095h 0090h 0096h 0090h 0097h 0090h 0098h 0090h 0091h 0091h 0092h 0092h 0095h 0096h 0097h 0097h 0098h 0097h 0097h 0097h 0098h 0098h 0040h UARTO Transmit/Receive Mode Register UOMR 00A1h UARTO Transmit/Receive Control Register UOTB XXh 00A3h UARTO Transmit/Receive Control Register UOC0 00001000b 00A6h UARTO Transmit/Receive Control Register UORB XXh 00A9h 00A9h <				
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0091h 0092h 0093h 0094h 0094h 0095h 0096h 0097h 0098h 0099h 0090h 0000h 0000				
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0096h 0097h 0098h 0099h 009Ah 009Bh 009Ch 009Ph 009Fh 00A0h UARTO Transmit/Receive Mode Register UOMR 00A0h UARTO Bit Rate Register UOBRG XXh 00A2h UARTO Transmit Buffer Register UOTB XXh 00A3h UARTO Transmit/Receive Control Register 0 UOC0 00001000b 00A5h UARTO Transmit/Receive Control Register 1 UOC1 00000010b 00A6h UARTO Receive Buffer Register UORB XXh 00A8h XXh 00A9h 00ABh 00ACh 00ACh 00ACh 00ACh				
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0098h 0099h 009Ah 009Bh 009Ch 009Dh 009Eh 009Fh 004Ah 000 004Bh 000 00ACh 000 00ABh 00ABh	0096h			
0099h 009Ah 009Bh 009Ch 009Dh 009Eh 009Fh 004 00A0h UARTO Transmit/Receive Mode Register UOMR 00h 00A0h UARTO Bit Rate Register UOBRG XXh 00A2h UARTO Transmit Buffer Register UOTB XXh 00A3h UARTO Transmit/Receive Control Register 0 UOC0 00001000b 00A5h UARTO Transmit/Receive Control Register 1 UOC1 00000010b 00A6h UARTO Receive Buffer Register UORB XXh 00A7h 00A8h 00A9h 00A9h 00ABh 00ACh 00ABh 00ACh 00ABh 00ACh 00ABh 00ABh 00AEh 00AEh 00AEh 00AEh	0097h			
009Ah 009Bh 009Ch 009Dh 009Eh 009Fh 00A0h UARTO Transmit/Receive Mode Register U0MR 00h 00A1h UARTO Bit Rate Register U0BRG XXh 00A2h UARTO Transmit Buffer Register U0TB XXh 00A3h UARTO Transmit/Receive Control Register 0 U0C0 00001000b 00A5h UARTO Transmit/Receive Control Register 1 U0C1 00000010b 00A6h UARTO Receive Buffer Register U0RB XXh 00A7h XXh XXh 00A8h 00A9h 00AAh 00ACh 00ACh 00ACh 00AEh 00AEh 00AEh	0098h			
009Ah 009Bh 009Ch 009Dh 009Eh 009Fh 00A0h UARTO Transmit/Receive Mode Register U0MR 00h 00A1h UARTO Bit Rate Register U0BRG XXh 00A2h UARTO Transmit Buffer Register U0TB XXh 00A3h UARTO Transmit/Receive Control Register 0 U0C0 00001000b 00A5h UARTO Transmit/Receive Control Register 1 U0C1 00000010b 00A6h UARTO Receive Buffer Register U0RB XXh 00A7h XXh XXh 00A8h 00A9h 00AAh 00ACh 00ACh 00ACh 00AEh 00AEh 00AEh	0099h			
009Bh 009Ch 009Dh				
009Ch 009Dh 009Eh 009Fh 00A0h UARTO Transmit/Receive Mode Register U0MR 00h 00A1h UARTO Bit Rate Register U0BRG XXh 00A2h UARTO Transmit Buffer Register U0TB XXh 00A3h UARTO Transmit/Receive Control Register 0 U0C0 00001000b 00A5h UARTO Transmit/Receive Control Register 1 U0C1 00000010b 00A6h UARTO Receive Buffer Register U0RB XXh 00A9h 00A9h 00AAh 00ABh 00ACh 00ADh 00AEh 00AEh				
009Dh 009Eh 009Fh 0040h 00A0h UART0 Transmit/Receive Mode Register U0MR 00h 00A1h UART0 Bit Rate Register U0BRG XXh 00A2h UART0 Transmit Buffer Register U0TB XXh 00A3h UART0 Transmit/Receive Control Register 0 U0C0 00001000b 00A5h UART0 Transmit/Receive Control Register 1 U0C1 00000010b 00A6h UART0 Receive Buffer Register U0RB XXh 00A7h 00A8h 00A9h 00A9h 00AAh 00ACh 00ACh 00ACh 00ACh 00ACh 00ACh 00ACh 00AEh 00AEh 00AEh 00AEh				
009Eh 009Fh 00A0h UART0 Transmit/Receive Mode Register U0MR 00h 00A1h UART0 Bit Rate Register U0BRG XXh 00A2h UART0 Transmit Buffer Register U0TB XXh 00A3h UART0 Transmit/Receive Control Register 0 U0C0 00001000b 00A5h UART0 Transmit/Receive Control Register 1 U0C1 00000010b 00A6h UART0 Receive Buffer Register U0RB XXh 00A7h 00A8h 00A9h 00A9h 00AAh 00AAh 00ACh 00ACh 00ADh 00ACh 00AEh 00AEh 00AEh				
009Fh 00A0h UART0 Transmit/Receive Mode Register U0MR 00h 00A1h UART0 Bit Rate Register U0BRG XXh 00A2h UART0 Transmit Buffer Register U0TB XXh 00A3h UART0 Transmit/Receive Control Register 0 U0C0 00001000b 00A5h UART0 Transmit/Receive Control Register 1 U0C1 00000010b 00A6h UART0 Receive Buffer Register U0RB XXh 00A7h VART0 Receive Buffer Register U0RB XXh 00A9h 00A9h 00A9h 00A9h 00ACh 00ACh 00ADh 00AEh 00ACh 00ACh				
00A0h UART0 Transmit/Receive Mode Register U0MR 00h 00A1h UART0 Bit Rate Register U0BRG XXh 00A2h UART0 Transmit Buffer Register U0TB XXh 00A3h UART0 Transmit/Receive Control Register 0 U0C0 00001000b 00A5h UART0 Transmit/Receive Control Register 1 U0C1 00000010b 00A6h UART0 Receive Buffer Register U0RB XXh 00A7h VART0 Receive Buffer Register U0RB XXh 00A9h 00A9h 00A9h 00A9h 00ABh 00ACh 00A0h 00ACh 00ADh 00ACh 00AEh 00AEh 00ACh				
00A1h UART0 Bit Rate Register U0BRG XXh 00A2h UART0 Transmit Buffer Register U0TB XXh 00A3h UART0 Transmit/Receive Control Register 0 U0C0 00001000b 00A5h UART0 Transmit/Receive Control Register 1 U0C1 00000010b 00A6h UART0 Receive Buffer Register U0RB XXh 00A7h VART0 Receive Buffer Register VART0 Receive Buffer Register VART0 Receive Buffer Register 00A9h VART0 Receive Buffer Register VART0 Receive Buffer Register VART0 Receive Buffer Register		LIADTO Terrore in Description Made Description	LIOMP	004
00A2h UART0 Transmit Buffer Register U0TB XXh 00A3h UART0 Transmit/Receive Control Register 0 U0C0 00001000b 00A5h UART0 Transmit/Receive Control Register 1 U0C1 00000010b 00A6h UART0 Receive Buffer Register U0RB XXh 00A7h XXh XXh 00A8h 00A9h 00AAh 00ABh 00ABh 00ACh 00ACh 00ADh 00ABh 00AEh 00AEh 00AEh		UAKTU Transmit/Receive Mode Register		
00A3h XXh 00A4h UART0 Transmit/Receive Control Register 0 U0C0 00001000b 00A5h UART0 Transmit/Receive Control Register 1 U0C1 00000010b 00A6h UART0 Receive Buffer Register U0RB XXh 00A7h XXh XXh 00A8h 00A9h 00A9h 00AAh 00ABh 00ACh 00ACh 00ADh 00ADh 00AEh 00AEh 00AEh		UAKTU Bit Rate Register		
00A4h UART0 Transmit/Receive Control Register 0 U0C0 00001000b 00A5h UART0 Transmit/Receive Control Register 1 U0C1 00000010b 00A6h UART0 Receive Buffer Register U0RB XXh 00A7h XXh XXh 00A9h 00A9h 00AAh 00ABh 00ACh 00ACh 00ACh 00ADh 00AEh	00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A5h UART0 Transmit/Receive Control Register 1 U0C1 00000010b 00A6h UART0 Receive Buffer Register U0RB XXh 00A7h XXh XXh 00A8h 00A9h 00AAh 00ABh 00ACh 00ACh 00ADh 00AEh 00AEh	00A3h			
00A5h UART0 Transmit/Receive Control Register 1 U0C1 00000010b 00A6h UART0 Receive Buffer Register U0RB XXh 00A7h XXh XXh 00A8h 00A9h 00AAh 00ABh 00ACh 00ACh 00ADh 00AEh 00AEh	00A4h	UART0 Transmit/Receive Control Register 0		00001000b
00A6h UART0 Receive Buffer Register U0RB XXh 00A7h XXh XXh 00A8h XXh XXh 00A9h XXh XXh 00AAh XXh XXh 00ABh XXh XXh 00ACh XXh XXh 00ADh XXh XXh 00ACh XXh XXh 00AEh XXh XXh 00AEh XXh XXh XXh XXh XXh <t< td=""><td>00A5h</td><td>UART0 Transmit/Receive Control Register 1</td><td>U0C1</td><td></td></t<>	00A5h	UART0 Transmit/Receive Control Register 1	U0C1	
00A7h 00A8h 00A9h 00A0h 00AAh 00ABh 00ACh 00ACh 00ACh	00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A8h 00A9h 00AAh 00ABh 00ACh 00ACh 00ADh	00A7h			
00A9h 00AAh 00ABh 00ACh 00ADh 00AEh	00A8h			
00AAh 00ABh 00ACh 00ADh 00AEh	00A9h			
00ABh 00ACh 00ADh 00AEh	00AAh			
00ACh 00ADh 00AEh				
00ADh 00AEh				
00AEh				
	OUADN			
UUAFn				
	UUAFh			

SFR Information (4)⁽¹⁾ Table 4.4

Address	Register	Symbol	After reset
00B0h	-5		
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh			
00BCh			
00BDh 00BEh			
00BEN 00BFh			
00C0h			
00C0H			
00C1fi			
00C2h			
00C3f1			
00C5h			
00C6h			
00C7h			
00C8h			
00C9h			
00CAh			
00CBh			
00CCh			
00CDh			
00CEh			
00CFh			
00D0h			
00D1h			
00D2h			
00D3h			
00D4h			
00D5h			
00D6h			
00D7h			
00D8h			
00D9h			
00DAh			
00DBh			
00DCh 00DDh			
00DDh 00DEh			
00DEH			
00E0h			
00E1h	Port P1 Register	P1	00h
00E1h			55.7
00E3h	Port P1 Direction Register	PD1	00h
00E4h	· · · · • • • · · · · · · · · · · · · ·		
00E5h	Port P3 Register	P3	00h
00E6h			
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	00h
00E9h	-		
00EAh	Port P4 Direction Register	PD4	00h
00EBh			
00ECh	Port P6 Register	P6	00h
00EDh			
00EEh	Port P6 Direction Register	PD6	00h
00EFh			
V: Undofined			

SFR Information (5)⁽¹⁾ Table 4.5

Address	Register	Symbol	After reset
00F0h	-		
00F1h			
00F2h			
00F3h			
00F4h			
00F5h			
00F6h	Pin Select Register 2	PINSR2	00h
00F7h			†
00F8h	Port Mode Register	PMR	00h
00F9h	External Input Enable Register	INTEN	00h
00FAh	INT Input Filter Select Register	INTF	00h
00FBh	Key Input Enable Register	KIEN	00h
00FCh	Pull-Up Control Register 0	PUR0	00h
00FDh	Pull-Up Control Register 1	PUR1	00h
00FEh			
00FFh			
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0102h	Timer RA Prescaler Register	TRAPRE	FFh
0103h	Timer RA Register	TRAPRE	FFh
0104h 0105h	Hiller IVV IVediater	IRA	11111
		LINOD	100
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			1
0111h			1
0112h			†
0113h			†
0114h			+
0115h			
0116h			+
0117h			+
	Time of DE Constant Data Desistant (Constant Data Desistant (2)	TRESEC	XXh
0118h	Timer RE Second Data Register / Counter Data Register ⁽²⁾		
0119h	Timer RE Minute Data Register / Compare Data Register(2)	TREMIN	XXh
011Ah	Timer RE Hour Data Register ⁽²⁾	TREHR	X0XXXXXb
011Bh	Timer RE Day of Week Data Register ⁽²⁾	TREWK	X0000XXXb
011Ch	Timer RE Control Register 1 ⁽²⁾	TRECR1	XXX0X0X0b
011Dh	Timer RE Control Register 2 ⁽²⁾	TRECR2	00XXXXXXb
011Eh	Timer RE Count Source Select Register ⁽²⁾	TRECSR	00001000b
011Fh	Timer RE Real-Time Clock Precision Adjust Register ⁽²⁾	TREOPR	00h
	Timer RE Real-Time Clock Precision Adjust Register(=)	INLOFK	0011
0120h		+	
0121h			
0122h		1	
0123h		1	
0124h		1	
0125h			
0126h			
0127h			
0128h			
0129h			
012Ah			
012Bh			1
012Ch			
012Dh		†	†
012Eh			+
012Fh		+	†
J i i i			

- X: Undefined
 NOTES:

 1. The blank regions are reserved. Do not access locations in these regions
 2. This register is not implemented in the R8C/2J Group.

SFR Information (6)⁽¹⁾ Table 4.6

Address	Register	Symbol	After reset
0130h			
0131h			
0132h			
0133h			
0134h			
0135h			
0136h			
0137h			
0138h			
0139h			
013Ah			
013Bh			
013Ch			
013Dh			
013Eh			
013Fh			
0140h			
0141h			
0142h			
0143h			
0144h			
0145h			
0146h			
0147h			
0148h			
0149h			
014Ah			
014Bh			
014Ch 014Dh			
014DII 014Eh			
014EH			
0150h			
0151h			
0152h			
0153h			
0154h			
0155h			
0156h			
0157h			
0158h			
0159h			
015Ah			
015Bh			
015Ch			
015Dh			
015Eh			
015Fh		LIOMD	006
0160h	UART2 Transmit/Receive Mode Register ⁽²⁾	U2MR	00h
0161h	UART2 Bit Rate Register ⁽²⁾	U2BRG	XXh
0162h	UART2 Transmit Buffer Register ⁽²⁾	U2TB	XXh
0163h		11000	XXh
0164h	UART2 Transmit/Receive Control Register 0 ⁽²⁾	U2C0	00001000b
0165h	UART2 Transmit/Receive Control Register 1(2)	U2C1	00000010b
0166h	UART2 Receive Buffer Register ⁽²⁾	U2RB	XXh
0167h			XXh
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			i

- X: Undefined
 NOTES:

 1. The blank regions are reserved. Do not access locations in these regions.
 2. This register is not implemented in the R8C/2J Group.

SFR Information (7)⁽¹⁾ Table 4.7

Address	Register	Symbol	After reset
0170h	ÿ	•	
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Eh			
0180h			
0180H			
0182h			
0183h 0184h			
0184N			
0185h			
0186h			
0187h			
0188h			
0189h			
018Ah			
018Bh			
018Ch			
018Dh			
018Eh			
018Fh			
0190h			
0191h			
0192h			
0193h			
0194h			
0195h			
0196h			
0197h			
0198h			
0199h			
019Ah			
019Bh			
019Ch			
019Dh			
019Eh			
019Fh			
01A0h			
01A011			
01A111			
01AZII			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			

SFR Information (8)⁽¹⁾ Table 4.8

0180h <th>Address</th> <th>Register</th> <th>Symbol</th> <th>After reset</th>	Address	Register	Symbol	After reset
0181h (183h) Flash Memory Control Register 4 FMR4 01000000b 0183h Flash Memory Control Register 4 FMR4 01000000b 0183h Flash Memory Control Register 1 FMR1 10000000b 0183h Flash Memory Control Register 0 FMR0 00000000b 0183h Flash Memory Control Register 0 FMR0 00000000b 0184h Flash Memory Control Register 0 FMR0 00000000b 0185h FMR0 00000000b 0186h FMR0 0000000b	01B0h		-,	
6182h Flash Memory Control Register 4 FMR4 0100000b 6183h Flash Memory Control Register 1 FMR1 1000000xb 6186h Flash Memory Control Register 0 FMR0 00000001b 6187h FMR0 00000001b 6187h FMR0 00000001b FMR0 6187h FMR0 00000001b FMR0 00000001b FMR0 6187h FMR1 FMR0 FMR0 00000001b FMR0 00000001b FMR0 000000000000000000000000000000000000				
01B3h Flash Memory Control Register 4 FMR4 01000000b 01B3h Flash Memory Control Register 1 FMR1 1000000xb 01B3h Flash Memory Control Register 0 FMR0 00000001b 01B3h FMR0 00000001b 01B3h FMR0 00000001b 01B3h FMR0 00000001b 01B4h FMR0 000000001b 01C4h FMR0 000000000000000000000000000000000000	01B2h			
0188h O188h Flash Memory Control Register 1 FMR1 1000000Xb 0188h O188h Flash Memory Control Register 0 FMR0 0000001b 0188h O188h Flash Memory Control Register 0 FMR0 0000001b 0188h O188h Flash Memory Control Register 0 FMR0 0000001b 0188h Flash Memory Control Register 0 FMR0 0000001b 0102h Flash Flash Memory Control Register 0 FMR0 0000001b 0102h Flash Flash Memory Control Register 0 FMR0 00000001b 0102h Flash Flash Memory Control	01B3h	Flash Memory Control Register 4	FMR4	01000000b
01BBh Flash Memory Control Register 1 FMR1 1000000Xb 01B7h Flash Memory Control Register 0 FMR0 00000001b 01BBh FMR0 000000000000000000000000000000000000	01B4h	The same of the sa		0.0000000
01BSh Flash Memory Control Register 0 FMRO 00000001b 01BSh 0000001b 00000001b 01BSh 0000001b 00000001b 01BSh 00000001b 0000001b 01BSh 00000001b 000000000000000000000000000000000000	01B5h	Flash Memory Control Register 1	FMR1	1000000Xb
OHBTh Flash Memory Control Register 0 FMRO 00000001b OHBSh 0 <t< td=""><td></td><td>The same of the sa</td><td></td><td></td></t<>		The same of the sa		
0188h 018Ah 018Ah 018Ah 018Ch 018Ch 018Ch 018Eh	01B7h	Flash Memory Control Register 0	FMR0	00000001b
01B9h 01BBh 01BCh 01BCh 01BCh 01BCh 01BCh 01BCh 01BCh 01Ch 01COh 01Ch 01COh 01Ch 01C2h 01CSh 01C3h 01CSh 01C6h 01CFh 01C8h 01CSh 01CSh 01CCh 01CCh 01CCh 01CCh 01CCh 01CFh 01CFh 01CPh 01CPh 01CPh	01B/h	That Memory Control Register C	TWITTO	00000015
01BAh 01BCh 01BCh 01BDh 01BCh 01BCh 01BFh 01Ch 01Ch 01Ch 01C2h 01Ch 01C2h 01Ch 01C4h 01Ch 01C5h 01Ch 01Ch 01Ch 01CR 01Ch 01CBh 01Ch 01CCh 01Ch 01CCh 01Ch 01CCh 01Ch 01CCh 01Ch 01CCh 01Ch 01Ch 01Ch	01B9h			
018Bh 018Ch 018Ch 018Ch 018Fh 01Ch 01Ch 01Ch 01Dh 01Ch 01Dh 01Ch 01Dh 01Ch 01	01BAh	!		
018Ch 018Eh 018Eh 018Eh 01Ch 01Ch 01Ch 01Ch 01Ch 01Ch 01Ch 01C	01BRh			
018Dh 018Fh 016Th 016Th 01C0h 01C1h 01C3h 01C3h 01C3h 01C5h 01C5h 01C6h 01C6h 01C6h 01C6h 01C6h 01C6h 01C6h 01C6h 01C8h 01C9h 01C9h 01Ch 01Ch 01Ch 01Ch 01Ch 01Ch 01Ch 01C	01BDh			
OHBER OTISH OTICOR OTIC	01B0h			
OTESPH OTCOM	01BBh			
01C0h 01C2h 01C2h 01C2h 01C3h 01C4h 01C5h 01C6h 01C6h 01C6h 01C6h 01C8h 01C0h 01CAh 01CBh 01CCh 01CDh 01CDh 01CDh 01CDh 01CDh 01CDh 01Dh 01Dh 01Dh 01Dh 01Dsh 01Ds	01BEh			
01C1h 01C2h 01C3h 01C3h 01C5h 01C5h 01C5h 01C6h 01C7h 01C8h 01C7h 01C8h 01C9h 01C9h 01C0h 01Ch 01Ch 01Ch 01Ch 01Ch 01Ch 01				
01C2h 01C3h 01C4h 01C5h 01C6h 01C7h 01C7h 01C8h 01C8h 01C8h 01C8h 01C8h 01C8h 01C9h 01C1b 01C1b 01C1ch	01C0h			
01C3h 01C5h 01C5h 01C7h 01C7h 01C8h 01C9h 01C9h 01C8h 01C9h 01C8h 01C8h 01C8h 01C8h 01C8h 01C8h 01C8h 01C8h 01C9h 01C8h 01C9h 01C8h 01C9h 01C9h 01C9h 01C9h 01C9h 01C9h 01C9h 01D9h 01D9h 01D1h 01D1h 01D2h 01D2h 01D8h 01D8h 01D8h 01D8h 01D9h	01C1h			
01C4h 01C6h 01C6h 01C8h 01C7h 01C8h 01C9h 01C8h 01C9h 01C6h 01CCh 01CCh 01CCh 01CPh 01Dh 01Dh 01Dh 01Dh 01Dh 01Dh 01Dh 01D	0102H			
01C5h 01C7h 01C8h 01C7h 01C8h 01C9h 01CAh 01CAh 01CBh 01CCCh 01CBh 01CCCh 01CBh 01CPh 01Dh 01CEh 01Dh 01Dh 01Dh 01Dh 01Dh 01Dh 01Dh 01D	01C4h			
01C8h 01C9h 01C9h 01C9h 01C9h 01C8h 01C8h 01C6h 01CCh 01CCh 01CCh 01CCh 01Ch 01Ch 01Ch	01C5h			
01C7h 01C8h 01C8h 01CAh 01CAh 01CCh 01CCh 01CCh 01CEh 01CFh 01Dh 01Dh 01Dh 01Dh 01Dh 01Dh 01Dh 01D	010311 0106h			
01C8h 01CAh 01CBh 01CCh 01CCCh 01CCCCh 01CCCC 01CCCCCCCCCC				
0103h 0102h 0102h 0102h 0102h 0102h 0102h 0102h 0102h 0101h 0101h 0101h 0102h 0103h 0104h 0105h 0108h	01C711			
01CAh 01CCh 01CCh 01CDh 01CEh 01CFh 01DOh 01DIh 01DIh 01DIh 01D3h 01D3h 01D3h 01D3h 01D8h 01D8h 01D8h 01D7h 01D8h 01D8h 01D8h 01D8h 01DBh 01DCh 01DCh 01DCh 01DEh 01DFh 01Eh 01DFh 01Eth 01Eth 01E3h 01E4h 01E3h 01E8h 01E8h 01E8h	01C0h			
01CBh 01CCh 01CDh 01CEh 01CFh 01Dh 01Dh 01Dh 01Dh 01Dh 01Dh 01Dh 01D	01C9H			
01Ch	01CAII			
01Cbh 01CFh 01Doh 01Doh 01Doh 01Dbh 01Dbh 01Dsh	01CBH			
01CFh 01CFh 01Dh 01Dh 01Dth 01Dh 01Dh 01Dh 01Dsh				
01CFh 01D0h 01D1h 01D2h 01D3h 01D3h 01D4h 01D5h 01D6h 01D7h 01D8h 01D9h 01D8h 01D9h 01DBh 01DBh 01DBh 01DBh 01DCh 01DBh 01DCh 01DBh 01DEh 01DCh 01DEh 01ESh				
01Dh	01CEh			
01D1h 01D2h 01D3h 01D3h 01D4h 01D5h 01D5h 01D6h 01D7h 01D8h 01D9h 01D9h 01DAh 01DBh 01DCh 01DDh 01DDh 01DEh 01DEh 01DEh 01DFh 01DFh 01Eh 01Eh 01Eh 01Eh 01Eh 01E3h 01E3h 01E5h 01E8h				
01D2h 01D3h 01D4h 01D5h 01D6h 01D6h 01D7h 01D8h 01D9h 01D9h 01DBh 01DDh 01DCh 01DDh 01DEh 01DEh 01DEh 01DEh 01DEh 01DEh 01DEh 01DEh 01Eh 01Eh 01Eh 01Eh 01E1h 01E2h 01E3h 01E3h 01E3h 01E3h 01E3h 01E3h 01E3h 01E3h 01E5h 01E6h 01E5h 01E6h 01E7h 01E8h 01E9h 01E8h 01E9h	01D0H			
01D3h 01D4h 01D5h 01D6h 01D7h 01D8h 01D9h 01D9h 01DAh 01DBh 01DCh 01DDh 01DEh 01DEh 01DEh 01DEh 01DEh 01EOh 01E1h 01E2h 01E3h 01E3h 01E4h 01E5h 01E5h 01E5h 01E6h 01E7h 01E8h 01E7h 01E8h 01E9h 01E8h 01E9h 01E9h 01E8h 01E9h 01E8h 01E9h 01E8h 01E9h 01E8h 01E9h 01EBh 01EBh 01EBh				
01D4h 01D5h 01D6h 01D7h 01D8h 01D9h 01DAh 01DBh 01DCh 01DCh 01DCh 01DDh 01DEh 01DEh 01DEh 01Eh 01Eh 01EOh 01El 01El 01El 01E2h 01E3h 01E4h 01E5h 01E5h 01E6h 01E7h 01E8h 01E9h 01E9h 01ERh 01EBh 01EBh				
01D5h 01D6h 01D7h 01D8h 01D9h 01D9h 01DAh 01DBh 01DCh 01DDh 01DEh 01DEh 01Eh 01ESh	01D3H			
01D6h 01D7h 01D8h 01D9h 01DAh 01DBh 01DCh 01DCh 01DDh 01DEh 01DEh 01Eh 01EGh 01ESh 01E3h 01E4h 01E5h 01E6h 01E8h 01E8h 01E8h 01E8h 01E9h 01E8h 01E9h 01E8h 01E9h 01E8h 01E9h 01E8h 01E9h 01E9h 01E8h 01E9h 01E8h 01E9h 01EBh 01ECh 01ECh				
01D7h 01D8h 01D9h 01DAh 01DBh 01DCh 01DDh 01DEh 01DFh 01DEh 01DFh 01ESh	01D3II			
01D8h 01DAh 01DBh 01DCh 01DCh 01DDh 01DFh 01DFh 01E0h 01E3h 01E3h 01E4h 01E5h 01E6h 01E8h 01E9h 01E9h 01E9h 01E9h 01E9h 01E9h 01EN	01D0H			
01D9h 01DAh 01DBh 01DCh 01DDh 01DEh 01DFh 01DFh 01Eh 01Eh 01ESh 01E3h 01E4h 01E5h 01E6h 01E8h 01E9h 01E8h 01E9h 01EAh				
01DAh 01DBh 01DCh 01DCh 01DCh 01DFh 01DFh 01Eh 01E0h 01E1h 01E2h 01E3h 01E3h 01E4h 01E5h 01E6h 01E6h 01E6h 01E7h 01E8h 01E8h 01E8h 01E8h 01E8h 01E9h 01E9h 01E9h 01E9h 01EOH	01D0H			
01DBh 01DCh 01DDh 01DBh 01DFh 01DFh 01E0h 01E0h 01E1h 01E2h 01E3h 01E4h 01E5h 01E6h 01E6h 01E7h 01E8h 01E9h 01EAh 01EBh 01ECh 01ECh 01EOh 01EDh				
01DCh 01DDh 01DFh 01DFh 01E0h 01E0h 01E1h 01E2h 01E3h 01E4h 01E6h 01E6h 01E7h 01E8h 01E9h 01E9h 01EAh 01EBh 01ECh 01ECh 01ECh 01EDh				
01DDh 01DEh 01DFh 01E0h 01E0h 01E1h 01E2h 01E3h 01E4h 01E6h 01E6h 01E6h 01E7h 01E8h 01E8h 01E8h 01E9h 01E8h 01E9h 01EOH	01DDH			
01DEh 01DFh 01E0h 01E0h 01E1h 01E2h 01E3h 01E4h 01E5h 01E6h 01E7h 01E8h 01E9h 01E9h 01EAh 01EBh 01ECh 01ECh 01EOh 01EDh	010011			
01DFh 01E0h 01E1h 01E2h 01E3h 01E4h 01E5h 01E6h 01E7h 01E8h 01E9h 01EAh 01EBh 01ECh 01ECh 01EDh				
01E0h 01E1h 01E2h 01E3h 01E4h 01E5h 01E6h 01E7h 01E8h 01E9h 01EAh 01EBh 01ECh 01EDh	01DEN			
01E1h 01E2h 01E3h 01E4h 01E5h 01E6h 01E7h 01E8h 01E9h 01EAh 01EBh 01ECh 01ECh 01EDh				
01E2h 01E3h 01E4h 01E5h 01E6h 01E6h 01E7h 01E8h 01E9h 01EAh 01EAh 01EBh 01ECh 01ECh 01EDh 01EDh	01500			
01E3h 01E4h 01E5h 01E6h 01E7h 01E8h 01E9h 01E9h 01EAh 01EBh 01EBh 01ECh 01ECh	015111			
01E4h 01E5h 01E6h 01E7h 01E8h 01E9h 01EAh 01EBh 01ECh 01EDh	01EZII			
01E5h 01E6h 01E7h 01E8h 01E9h 01EAh 01EBh 01EBh 01ECh 01ECh				
01E6h 01E7h 01E8h 01E9h 01E9h 01EAh 01EBh 01ECh 01EDh 01EDh				
01E7h 01E8h 01E9h 01EAh 01EBh 01ECh 01ECh				
01E8h 01E9h 01EAh 01EBh 01ECh 01ECh				
01E9h 01EAh 01EBh 01ECh 01EDh	015/0			
01EAh 01EBh 01ECh 01EDh	UTE8N			
01EBh 01ECh 01EDh				
01ECh				
01EDh				
U1EDN				
	01EDh			
VIEEN	01EEh			
01EFh	01EFh			

SFR Information (9)⁽¹⁾ Table 4.9

Address	Register	Symbol	After reset
01F0h		-,	
01F1h			
01F2h			
01F3h			
01F4h			
01F5h			
01F6h			
01F7h			
01F8h			
01F9h			
01FAh			
01FBh			
01FCh			
01FDh			
01FEh			
01FFh			
0200h			
0201h			
0202h			
0203h			
0204h			
0205h			
0206h			
0207h			
0208h			
0209h			
020Ah			
020Bh			
020Ch			
020Dh			
020Eh			
020Fh			
0210h			
0211h			
0212h			
0213h			
0214h			
0215h			
0216h			
0217h			
0218h			
0219h			
021Ah			
021Bh			
021Ch			
021Dh			
021Eh			
021Fh			
0220h			
0220h			
0221h			
0222h			
	<u> </u>		
0224h 0225h			
0226h			
0227h			
0228h			
0229h			
022Ah			
022Bh	<u> </u>		
022Ch			
0000			
022Dh			
022Dh 022Eh 022Fh			

SFR Information (10)⁽¹⁾ **Table 4.10**

Address	Register	Symbol	After reset
0230h	1.0gioto.	Cymso.	7 11101 10001
0231h			
0232h			
0233h			
0234h			
0235h			
0236h			
0237h			
0238h			
0239h			
023Ah			
023Bh			
023Ch			
023Dh			
023Eh			
023Fh			
0231 H			
0240H			
024111 0242h			
0242h 0243h			
0243h 0244h			
024411			
0245h			
0246h			
0247h			
0248h			
0249h			
024Ah			
024Bh			
024Ch			
024Dh			
024Eh			
024Fh			
0250h			
0251h			
0252h			
0253h			
0254h			
0255h			
0256h			
0257h			
0258h			
0259h			
025Ah			
025Bh			
025Ch			
025Dh			
025Eh			
025Fh			
0260h			
0261h			
0262h			
0263h			
0264h			
0265h			
0266h			
0267h			
0267h			
0269h			
0269h			
026An			
026Bh 026Ch			
026Ch 026Dh			
UZDIJII			l
026Eh 026Fh			

SFR Information (11)⁽¹⁾ **Table 4.11**

Address	Register	Symbol	After reset
0270h	register	Cymbol	Alter reset
0270H			
0271h			
0272h			
0274h			
0275h			
0276h			
0277h			
0277H			
0279h			
027Ah			
027Rh			
027Ch			
027Dh			
027Eh			
027Eh			
0280h			
0281h			
0282h			
0283h			
0284h			
0285h			
0286h			
0287h			
0288h			
0289h			
028Ah			
028Bh			
028Ch			
028Dh			
028Eh			
028Fh			
0290h	Timer RF Register	TRF	00h
0291h	····· · · · · · · · · · · · · · · · ·		00h
0292h			
0293h			
0294h			
0295h			
0296h			
0297h			
0298h			
0299h	Timer RF Control Register 2 ⁽⁴⁾	TRFCR2	00h
029Ah	Timer RF Control Register 2 ⁽⁴⁾ Timer RF Control Register 0	TRFCR0	00h
029Bh	Timer RF Control Register 1	TRFCR1	00h
029Ch	Capture and Compare 0 Register	TRFM0	0000h ⁽²⁾
029Dh			FFFFh ⁽³⁾
029Eh			1 1 1 1 IN ⁻⁷
029En	Compare 1 Register	TREM1	l FFh
029FII 02A0h	Compare 1 Register	TRFM1	FFh FFh
02A011 02A1h	Compare 1 Register	TRFM1	FFh FFh
	Compare 1 Register	TRFM1	FFh FFh
11/4/0	Compare 1 Register	TRFM1	FFh FFh
02A2h 02A3h	Compare 1 Register	TRFM1	FFh FFh
02A3h	Compare 1 Register	TRFM1	FFh FFh
02A3h 02A4h	Compare 1 Register	TRFM1	FFh FFh
02A3h 02A4h 02A5h	Compare 1 Register	TRFM1	FFh FFh
02A3h 02A4h 02A5h 02A6h	Compare 1 Register	TRFM1	FFh FFh
02A3h 02A4h 02A5h 02A6h 02A7h	Compare 1 Register	TRFM1	FFh FFh
02A3h 02A4h 02A5h 02A6h 02A7h 02A8h	Compare 1 Register	TRFM1	FFh FFh
02A3h 02A4h 02A5h 02A6h 02A7h 02A8h 02A9h	Compare 1 Register	TRFM1	FFh FFh
02A3h 02A4h 02A5h 02A6h 02A7h 02A8h 02A9h 02AAh	Compare 1 Register	TRFM1	FFh FFh
02A3h 02A4h 02A5h 02A6h 02A7h 02A8h 02A8h 02A9h 02AAh	Compare 1 Register	TRFM1	FFh FFh
02A3h 02A4h 02A5h 02A6h 02A7h 02A8h 02A9h 02A9h 02AAh 02ABh	Compare 1 Register	TRFM1	FFh FFh
02A3h 02A4h 02A5h 02A6h 02A7h 02A8h 02A9h 02A9h 02AAh 02ABh 02ACh	Compare 1 Register	TRFM1	FFh FFh
02A3h 02A4h 02A5h 02A6h 02A7h 02A8h 02A9h 02A9h 02AAh 02ABh	Compare 1 Register	TRFM1	FFh FFh

X: Undefined

- NOTES:

 1. The blank regions are reserved. Do not access locations in these regions.
 2. After input capture mode.
 3. After output compare mode.
 4. This register is not implemented in the R8C/2J Group.

SFR Information (12)⁽¹⁾ **Table 4.12**

Address	Register	Symbol	After reset
02B0h	g		1
02B1h			
02B2h			
02B3h			
02B4h			
02B5h			
02B6h			
02B7h			
02B8h			
02B9h			
02BAh			
02BBh			
02BCh			
02BDh			
02BEh			
02BFh			
02C0h			
02C1h			
02C2h			
02C3h			
02C4h			
02C5h			
02C6h			
02C7h			
02C8h			
02C9h			
02C9fi 02CAh			
02CAN			
02CBh			
02CCh			
02CDh			
02CEh			
02CFh			
02D0h			
02D1h			
02D111			
02D2H			
02D3h			
02D4h			
02D5h			
02D6h			
02D7h			
02D8h			
02D9h			
02DAh			
02DBh			
02DCh			
02DDh			
02DEh			
02DFh			
02E0h			
02EFh			
02F0h			
021 011			
02F1h			
02F2h			
02F3h			
02F4h			
02F5h			
02F6h			
02F7h			
02F8h			
02F9h			
021 311			
02FAh		DINIODA	
02FBh	Pin Select Register 4	PINSR4	00h
02FCh			
02FDh			
02FEh			
02FFh	Timer RF Output Control Register	TRFOUT	00h
	· · · · · · · · · · · · · · · · · · ·		
FFFFh	Option Function Select Register	OFS	(Note 2)
	Topilon Familian Colock Regional	J. J	(

- X: Undefined
 NOTES:

 1. The blank regions are reserved. Do not access locations in these regions.
 2. The OFS register cannot be changed by a program. Use a flash programmer to write to it.

Electrical Characteristics 5.

R8C/2H Group 5.1

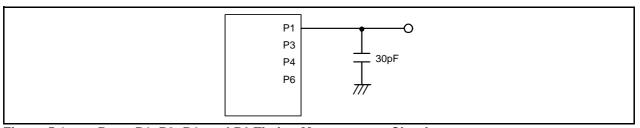
Absolute Maximum Ratings Table 5.1

Symbol	Parameter	Condition	Rated Value	Unit
Vcc	Supply voltage		-0.3 to 6.5	V
Vı	Input voltage		-0.3 to Vcc + 0.3	V
Vo	Output voltage		-0.3 to Vcc + 0.3	V
Pd	Power dissipation	Topr = 25°C	500	mW
Topr	Operating ambient temperature		-20 to 85 (N version) / -40 to 85 (D version)	°C
Tstg	Storage temperature		-65 to 150	°C

Table 5.2 **Recommended Operating Conditions**

Courselle sel	Davam		Canditions		Standard		Llait
Symbol	Param	neter	Conditions	Min.	Тур.	Max.	Unit
Vcc	Supply voltage			2.2	-	5.5	V
Vss	Supply voltage			-	0	-	V
ViH	Input "H" voltage			0.8 Vcc	=	Vcc	V
VIL	Input "L" voltage			0	=	0.2 Vcc	V
IOH(sum)	Peak sum output "H" current	Sum of all pins IOH(peak)		-	-	-160	mA
IOH(sum)	Average sum output "H" current	Sum of all pins IOH(avg)		-	_	-80	mA
IOH(peak)	Peak output "H" current	All pins		_	-	-10	mA
IOH(avg)	Average output "H" current	All pins		-	=	- 5	mA
IOL(sum)	Peak sum output "L" currents	Sum of all pins IOL(peak)		-	=	160	mA
IOL(sum)	Average sum output "L" currents	Sum of all pins IOL(avg)		-	=	80	mA
IOL(peak)	Peak output "L" currents	All pins		_	-	10	mA
IOL(avg)	Average output "L" current	All pins		-	-	5	mA
f(XCIN)	XCIN clock input oscillation	frequency	2.2 V ≤ Vcc ≤ 5.5 V	0	=	70	kHz
_	System clock	OCD2 = 0 XCIN clock selected	2.2 V ≤ Vcc ≤ 5.5 V	0	_	70	kHz
		OCD2 = 1 On-chip oscillator clock selected	HRA01 = 0 Low-speed on-chip oscillator selected	=	125	_	kHz
			HRA01 = 1 High-speed on-chip oscillator selected 2.7 V ≤ Vcc ≤ 5.5 V	-	=	8	MHz
			HRA01 = 1 High-speed on-chip oscillator selected 2.2 V ≤ Vcc ≤ 5.5 V	_	-	4	MHz

- 1. Vcc = 2.2 to 5.5 V at Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
- 2. The average output current indicates the average value of current measured during 100 ms.



Ports P1, P3, P4, and P6 Timing Measurement Circuit Figure 5.1

Table 5.3 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions		Unit		
Symbol	Faiametei	Conditions	Min.	Тур.	Max.	Offic
_	Program/erase endurance ⁽²⁾		100 ⁽³⁾	_	-	times
-	Byte program time		-	50	400	μS
_	Block erase time		=	0.4	9	S
_	Program, erase voltage		2.7	-	5.5	V
_	Read voltage		2.2	-	5.5	V
-	Program, erase temperature		0	=	60	°C
-	Data hold time ⁽⁷⁾	Ambient temperature = 55°C	20	-	-	year

- 1. Vcc = 2.7 to 5.5 V at Topr = 0 to 60°C, unless otherwise specified.
- 2. Definition of programming/erasure endurance
 - The programming and erasure endurance is defined on a per-block basis.
 - If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
 - However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
- 3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- 4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
- 5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- 6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- 7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.4 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
Symbol	Farameter	Condition	Min.	Тур.	Max.	Offic
Vdet0	Voltage detection level		2.2	2.3	2.4	V
=	Voltage detection circuit self power consumption	VCA25 = 1, Vcc = 5.0 V	_	0.9	-	μΑ
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽²⁾		-	=	300	μS
Vccmin	MCU operating voltage minimum value		2.2	-	-	V

- 1. The measurement condition is Vcc = 2.2 to 5.5 V and Topr = -20 to $85^{\circ}C$ (N version) / -40 to $85^{\circ}C$ (D version).
- 2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

Table 5.5 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Тур.	Max.	Offic
Vdet1	Voltage detection level ⁽⁴⁾		2.70	2.85	3.00	V
_	Voltage monitor 1 interrupt request generation time ⁽²⁾		_	40	_	μS
=	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V	=	0.6	-	μΑ
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾		-	_	100	μS

NOTES:

- 1. The measurement condition is Vcc = 2.2 to 5.5 V and $T_{opr} = -20$ to 85°C (N version) / -40 to 85°C (D version).
- 2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes Vdet1.
- 3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
- 4. This parameter shows the voltage detection level when the power supply drops. The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.

Table 5.6 Voltage Detection 2 Circuit Electrical Characteristics

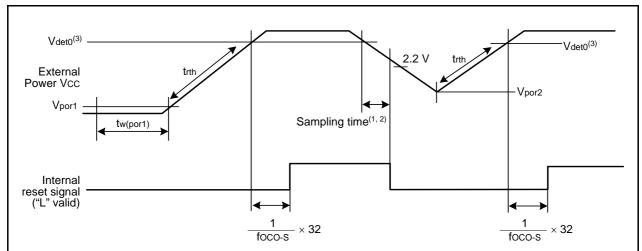
Symbol	Parameter	Condition	Standard			Unit
			Min.	Тур.	Max.	Offic
Vdet2	Voltage detection level		3.3	3.6	3.9	V
=	Voltage monitor 2 interrupt request generation time(2)		-	40	-	μS
=	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0 V	=	0.6	=	μΑ
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾		=	=	100	μS

- 1. The measurement condition is Vcc = 2.2 to 5.5 V and Topr = -20 to 85°C (N version) / -40 to 85°C (D version).
- 2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes Vdet2.
- 3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.7	Power-on Reset Circuit.	Voltage Monitor 0 Reset Electrical Characteristics ⁽³⁾
		Total go mornion o morot = mornion o management

Symbol	Parameter	Condition	Standard			Unit
			Min.	Тур.	Max.	Ullit
Vpor1	Power-on reset valid voltage ⁽⁴⁾		-	_	0.1	V
Vpor2	Power-on reset or voltage monitor 0 reset valid voltage		0	-	Vdet0	V
trth	External power Vcc rise gradient(2)		20	=	=	mV/msec

- 1. The measurement condition is Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
- 2. This condition (external power Vcc rise gradient) does not apply if Vcc ≥ 1.0 V.
- 3. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVD0ON bit in the OFS register to 0, the VW0C0 and VW0C6 bits in the VW0C register to 1 respectively, and the VCA25 bit in the VCA2 register to 1.
- 4. tw(por1) indicates the duration the external power Vcc must be held below the effective voltage (Vpor1) to enable a power on reset. When turning on the power for the first time, maintain tw(por1) for 30 s or more if $-20^{\circ}C \le T_{opr} \le 85^{\circ}C$, maintain tw(por1) for 3,000 s or more if $-40^{\circ}C \le T_{opr} < -20^{\circ}C$.



- 1. When using the voltage monitor 0 digital filter, ensure that the voltage is within the MCU operation voltage range (2.2 V or above) during the sampling time.
- 2. The sampling clock can be selected. Refer to **6. Voltage Detection Circuit** of Hardware Manual for details.
- V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to 6. Voltage Detection Circuit of Hardware Manual for details.

Figure 5.2 Reset Circuit Electrical Characteristics

Table 5.8 **Comparator Electrical Characteristics**

Symbol	Parameter	Condition		Standard		
Symbol	Farameter	Condition	Min.	Тур.	Max.	Unit
Vref	Internal reference voltage	Vcc = 2.2 V to 5.5 V, Topr = 25°C	1.15	1.25	1.35	V
		VCC = 2.2 V to 5.5 V, $Topr = -40 \text{ to } 85^{\circ}\text{C}$	-	1.25	_	V
Vcref	External input reference voltage	Vcc = 2.2 V to 4.0 V	0.5	=	Vcc - 1.1	V
		Vcc = 4.0 V to 5.5 V	0.5	=	Vcc - 1.5	V
Vcin	External comparison voltage input range		-0.3	_	Vcc + 0.3	V
Vofs	Input offset voltage		=	20	120	mV
Tcrsp	Response time		=	4	=	μS

Table 5.9 **High-speed On-Chip Oscillator Circuit Electrical Characteristics**

Symbol	Parameter	Condition		Standard		Unit
Symbol	Farameter	Condition	Min.	Тур.	Max.	Offic
fOCO-F	High-speed on-chip oscillator frequency temperature • supply voltage dependence	Vcc = 4.75 V to 5.25 V $Topr = 0 \text{ to } 60^{\circ}C^{(2)}$	7.76	8	8.24	MHz
		Vcc = 2.7 V to 5.5 V $Topr = -20 \text{ to } 85^{\circ}C^{(2)}$	7.68	8	8.32	MHz
		VCC = 2.7 V to 5.5 V $T_{\text{Opr}} = -40 \text{ to } 85^{\circ}C^{(2)}$	7.44	8	8.32	MHz
		Vcc = 2.2 V to 5.5 V $Topr = -20 \text{ to } 85^{\circ}C^{(3)}$	7.04	8	8.96	MHz
		VCC = 2.2 V to 5.5 V $Topr = -40 \text{ to } 85^{\circ}C^{(3)}$	6.8	8	9.2	MHz

NOTES:

- 1. The measurement condition is Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
- 2. These standard values show when the HRA1 register is set to the value before shipment and the HRA2 register is set to 00h.
- 3. These standard values show when the correction value in the FRA6 register is written into the HRA1 register.

Table 5.10 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard Min. Typ. 30 125 - 10 - 15		Unit	
Symbol	Falametei	Condition	Min.	Тур.	Max.	Offic
fOCO-S	Low-speed on-chip oscillator frequency		30	125	250	kHz
_	Oscillation stability time		-	10	100	μS
_	Self power consumption at oscillation	VCC = 5.0 V, Topr = 25°C	_	15	_	μΑ

NOTE:

1. Vcc = 2.2 to 5.5 V, Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.11 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition		Standard		Unit
Symbol	Falametei	Condition	Min.	Тур.	Max.	Offic
td(P-R)	Time for internal power supply stabilization during power-on ⁽²⁾		1	=	2000	μS
td(R-S)	STOP exit time ⁽³⁾		ı	-	150	μS

- 1. The measurement condition is Vcc = 2.2 to 5.5 V and T_{opr} = 25°C.
- 2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
- 3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.



^{1.} The measurement condition is Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.12 Electrical Characteristics (1) [Vcc = 5 V]

Symbol	Doro	meter	Condition	S	tandard		Unit
Symbol	Faia	inetei	Condition	Min.	Тур.	Max.	Offic
Voн	Output "H" voltage		Iон = −5 mA	Vcc - 2.0	_	Vcc	V
			IOH = −200 μA	Vcc - 0.5	-	Vcc	V
Vol	Output "L" voltage		IoL = 5 mA	=	-	2.0	V
			IoL = 200 μA	=	-	0.45	V
VT+-VT-	Hysteresis	NT0, NT1, KI0, KI1, KI2, KI3, RXD0, RXD2, CLK0, CLK2		0.1	0.5	-	V
		RESET		0.1	1.0	-	V
Іін	Input "H" current		VI = 5 V, Vcc = 5 V	-	_	5.0	μА
lı∟	Input "L" current		VI = 0 V, Vcc = 5 V	-	_	-5.0	μА
RPULLUP	Pull-up resistance		VI = 0 V, Vcc = 5 V	30	50	167	kΩ
RfXCIN	Feedback resistance	XCIN		-	18	-	МΩ
VRAM	RAM hold voltage		During stop mode	2.0	_	-	V

NOTE

^{1.} Vcc = 4.2 to 5.5 V at Topr = -20 to $85^{\circ}C$ (N version) / -40 to $85^{\circ}C$ (D version), unless otherwise specified.

Table 5.13 Electrical Characteristics (2) [Vcc = 5 V] (Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Condition		Standar		Unit
•				Min.	Тур.	Max.	
CC	Power supply current (Vcc = 3.3 to 5.5 V)	High-speed on-chip oscillator mode	High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz No division	_	5	8	mA
	Single-chip mode, output pins are open, other pins are Vss		High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	_	2	=	mA
	culci pino die vee	Low-speed on-chip oscillator mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	-	130	300	μА
		Low-speed clock mode	High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) FMR47 = 1	=	130	300	μА
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) Program operation on RAM Flash memory off, FMSTP = 1	-	30	-	μА
		Wait mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	25	75	μА
			High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	23	60	μА
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 BGR trimming circuit disabled (BGRCR0 = 1)	-	4	-	μА
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 BGR trimming circuit disabled (BGRCR0 = 1)	-	2.2	-	μА
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 BGR trimming circuit enabled (BGRCR0 = 0)	-	8	_	μА
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 BGR trimming circuit enabled (BGRCR0 = 0)	-	6	_	μА
		Stop mode	XCIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1)	-	0.8	3	μА
		XCIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1)	-	1.2	-	μА	
			XCIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0)	-	5	8	μА
			XCIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	-	5.5	=	μА

Timing Requirements

(Unless Otherwise Specified: Vcc = 5 V, Vss = 0 V at Topr = 25°C) [Vcc = 5 V]

Table 5.14 XCIN Input

Symbol Parametric(XCIN) XCIN input cycle time	Doromotor	Stan	Unit	
	Farameter	Min.	Max.	Offic
tc(XCIN)	XCIN input cycle time	14	=	μS
twh(xcin)	XCIN input "H" width	7	=	μS
twl(xcin)	XCIN input "L" width	7	-	μS

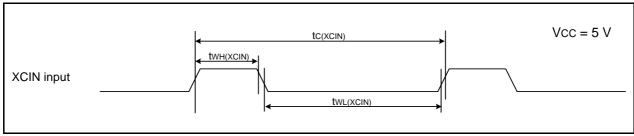


Figure 5.3 XCIN Input Timing Diagram when Vcc = 5 V

Table 5.15 TRAIO Input

Symbol Parameter tc(TRAIO) TRAIO input cycle time twh(TRAIO) TRAIO input "H" width	Standard		Unit	
	raidilletei	Min.	Max.	Offic
tc(TRAIO)	TRAIO input cycle time	100	=	ns
twh(traio)	TRAIO input "H" width	40	=	ns
twl(traio)	TRAIO input "L" width	40	Ī	ns

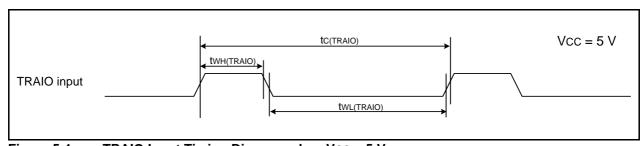


Figure 5.4 TRAIO Input Timing Diagram when Vcc = 5 V

Table 5.16 Serial Interface

Symbol	Parameter	Stan	dard	Unit
Symbol	Falanietei	Min.	Max.	Offic
tc(CK)	CLKi input cycle time	200	=	ns
tW(CKH)	CLKi input "H" width	100	-	ns
tW(CKL)	CLKi input "L" width	100	-	ns
td(C-Q)	TXDi output delay time	=	50	ns
th(C-Q)	TXDi hold time	0	-	ns
tsu(D-C)	RXDi input setup time	50	=	ns
th(C-D)	RXDi input hold time	90	_	ns

i = 0 or 2

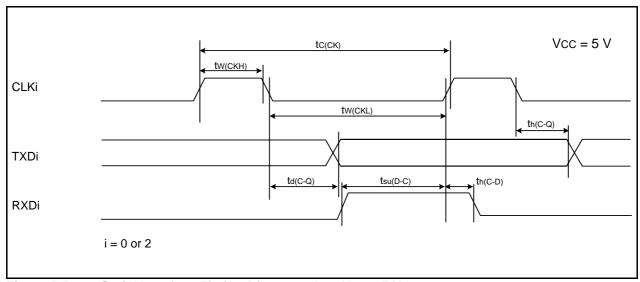


Figure 5.5 Serial Interface Timing Diagram when Vcc = 5 V

Table 5.17 External Interrupt \overline{INTi} (i = 0 or 1) Input

Symbol	Parameter		Standard Unit Min. Max. 250(1) - ns 250(2) - ns	Unit
Symbol	<u></u>	Min.	Max.	Offic
tW(INH)	ĪNTi input "H" width	250 ⁽¹⁾	-	ns
tW(INL)	INTi input "L" width	250 ⁽²⁾	-	ns

- 1. When selecting the digital filter by the $\overline{\text{INTi}}$ input filter select bit, use an $\overline{\text{INTi}}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
- 2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

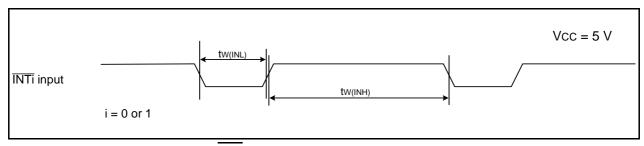


Figure 5.6 External Interrupt INTi Input Timing Diagram when Vcc = 5 V

Electrical Characteristics (3) [Vcc = 3 V] **Table 5.18**

Symbol	Doros	matar	Condition	5	Standard		Unit	
Symbol	Parameter		Condition	Min.	Тур.	Max.	Offile	
Vон	Output "H" voltage		Iон = −1 mA	Vcc - 0.5	=	Vcc	V	
Vol	Output "L" voltage		IoL = 1 mA	=	=	0.5	V	
VT+-VT-	Hysteresis	NT0, NT1, KI0, KI1, KI2, KI3, RXD0, RXD2, CLK0, CLK2		0.1	0.3	_	>	
		RESET		0.1	0.4	_	V	
Iн	Input "H" current		VI = 3 V, Vcc = 3 V	-	-	4.0	μА	
lı∟	Input "L" current		VI = 0 V, Vcc = 3 V	-	-	-4.0	μА	
RPULLUP	Pull-up resistance		VI = 0 V, Vcc = 3 V	66	160	500	kΩ	
RfXCIN	Feedback resistance	XCIN		-	18	-	MΩ	
VRAM	RAM hold voltage		During stop mode	1.8	-	_	V	

NOTE:

1. Vcc =2.7 to 3.3 V at Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.19 Electrical Characteristics (4) [Vcc = 3 V] (Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Cymbal	Parameter		Condition	Standard		l la:	
Symbol	Parameter		Condition	Min.	Тур.	Max.	Uni
СС	Power supply current (Vcc = 2.7 to 3.3 V)	High-speed on-chip oscillator mode	High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz No division	-	5	_	mA
	Single-chip mode, output pins are open, other pins are Vss		High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	2	=	mA
	other pins are vss	Low-speed on-chip oscillator mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	=	130	300	μΑ
		Low-speed clock mode	High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) FMR47 = 1	-	130	300	μА
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) Program operation on RAM Flash memory off, FMSTP = 1	=	30	_	μА
		Wait mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	=	25	70	μА
			High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	23	55	μА
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 BGR trimming circuit disabled (BGRCR0 = 1)	-	3.8	=	μА
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 BGR trimming circuit disabled (BGRCR0 = 1)		2	_	μА
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 BGR trimming circuit enabled (BGRCR0 = 0)	-	8	-	μА
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 BGR trimming circuit enabled (BGRCR0 = 0)	-	6	-	μΑ
		Stop mode	XCIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1)	-	0.7	3	μА
			XCIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1)	-	1.1	-	μА
			XCIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0)	-	5	7	μА
			XCIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0)	-	5.5	-	μА

Timing requirements

(Unless Otherwise Specified: Vcc = 3 V, Vss = 0 V at Topr = 25°C) [Vcc = 3 V]

Table 5.20 XCIN Input

Symbol	Parameter		Standard		
			Max.	Unit	
tc(XCIN)	XCIN input cycle time	14	=	μS	
twh(xcin)	XCIN input "H" width	7	=	μS	
tWL(XCIN)	XCIN input "L" width	7	=	μS	

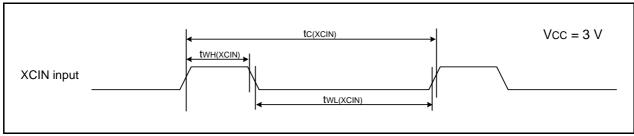


Figure 5.7 XCIN Input Timing Diagram when Vcc = 3 V

Table 5.21 TRAIO Input

Symbol	Parameter		Standard		
			Max.	Unit	
tc(TRAIO)	TRAIO input cycle time	300	-	ns	
twh(traio)	TRAIO input "H" width	120	-	ns	
twl(traio)	TRAIO input "L" width	120	Ī	ns	

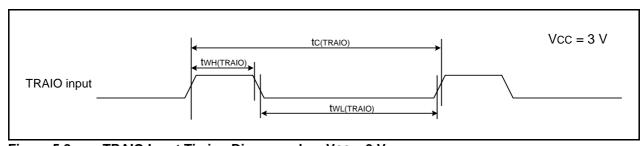


Figure 5.8 TRAIO Input Timing Diagram when Vcc = 3 V

Table 5.22 Serial Interface

Symbol	Parameter		Standard		
Symbol	raianietei	Min.	Max.	Unit	
tc(CK)	CLKi input cycle time	300	-	ns	
tW(CKH)	CLKi input "H" width	150	=	ns	
tW(CKL)	CLKi Input "L" width	150	-	ns	
td(C-Q)	TXDi output delay time	-	80	ns	
th(C-Q)	TXDi hold time	0	=	ns	
tsu(D-C)	RXDi input setup time	70	=	ns	
th(C-D)	RXDi input hold time	90	=	ns	

i = 0 or 2

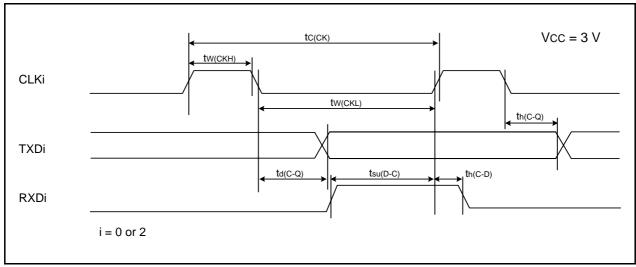


Figure 5.9 Serial Interface Timing Diagram when Vcc = 3 V

Table 5.23 External Interrupt \overline{INTi} (i = 0 or 1) Input

Symbol	Parameter		Standard		
Symbol	raidilletei	Min.	Max.	Unit	
tw(INH)	ĪNTi input "H" width	380 ⁽¹⁾	-	ns	
tW(INL)	INTi input "L" width	380(2)	-	ns	

- 1. When selecting the digital filter by the INTi input filter select bit, use an INTi input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
- 2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.

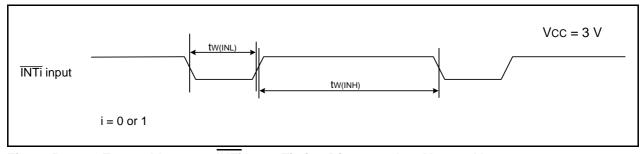


Figure 5.10 External Interrupt INTi Input Timing Diagram when Vcc = 3 V

Electrical Characteristics (5) [Vcc = 2.2 V] **Table 5.24**

Symbol	Parameter	Condition	5		Unit		
	Palai	meter	Condition	Min.	Тур.	Max.	Unit
Vон	Output "H" voltage		IOH = −1 mA	Vcc - 0.5	-	Vcc	V
Vol	Output "L" voltage		IoL = 1 mA	_	-	0.5	V
VT+-VT-	Hysteresis	NT0, NT1, KI0, KI1, KI2, KI3, RXD0, RXD2, CLK0, CLK2		0.05	0.3	-	V
		RESET		0.05	0.15	_	V
Iн	Input "H" current		VI = 2.2 V	-	_	4.0	μА
lıL	Input "L" current		VI = 0 V	-	-	-4.0	μΑ
RPULLUP	Pull-up resistance		VI = 0 V	100	200	600	kΩ
RfXCIN	Feedback resistance	XCIN		-	35	-	ΜΩ
VRAM	RAM hold voltage	•	During stop mode	1.8	=	_	V

NOTE: 1. Vcc = 2.2 V at $T_{opr} = -20 \text{ to } 85^{\circ}\text{C}$ (N version) / $-40 \text{ to } 85^{\circ}\text{C}$ (D version), unless otherwise specified.

Table 5.25 Electrical Characteristics (6) [Vcc = 2.2 V] (Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit	
Icc				Min. Typ.		Max.		
Icc	Power supply current (Vcc = 2.2 to 2.7 V)	High-speed on-chip oscillator mode	High-speed on-chip oscillator on = 4 MHz Low-speed on-chip oscillator on = 125 kHz No division	_	3.5	-	mA	
Single-chip mode, output pins are open, other pins are Vss		High-speed on-chip oscillator on = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	1.5	=	mA		
	other pins are vss	Low-speed on-chip oscillator mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	-	100	230	μА	
		Low-speed clock mode	High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) FMR47 = 1	_	100	230	μА	
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) Program operation on RAM Flash memory off, FMSTP = 1	-	25	_	μА	
		Wait mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	22	60	μА	
			High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	20	55	μА	
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 BGR trimming circuit disabled (BGRCR0 = 1)	-	3	_	μА	
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 BGR trimming circuit disabled (BGRCR0 = 1)	-	1.8	_	μА	
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 BGR trimming circuit enabled (BGRCR0 = 0)	-	7	_	μА	
			High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 BGR trimming circuit enabled (BGRCR0 = 0)	-	6	-	μА	
		Stop mode	XCIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1)	-	0.7	3	μА	
			XCIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1)	-	1.1	-	μА	
			XCIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0)	-	5	7	μА	
			XCIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0)	_	5.5	-	μА	

Timing requirements

(Unless Otherwise Specified: Vcc = 2.2 V, Vss = 0 V at Topr = 25°C) [Vcc = 2.2 V]

Table 5.26 XCIN Input

Symbol	Parameter		Standard		
Symbol			Max.	Unit	
tc(XCIN)	XCIN input cycle time	14	-	μS	
twh(xcin)	XCIN input "H" width	7	-	μS	
twl(xcin)	XCIN input "L" width	7	_	μS	

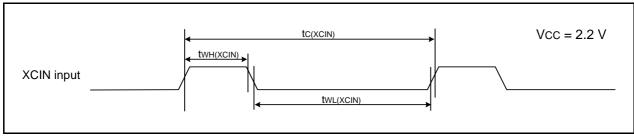
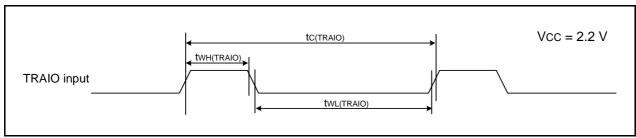


Figure 5.11 XCIN Input Timing Diagram when Vcc = 2.2 V

Table 5.27 TRAIO Input

Symbol	Parameter		Standard		
			Max.	Unit	
tc(TRAIO)	TRAIO input cycle time	500	=	ns	
twh(traio)	TRAIO input "H" width	200	=	ns	
twl(traio)	TRAIO input "L" width	200	Ī	ns	



TRAIO Input Timing Diagram when Vcc = 2.2 V Figure 5.12

Table 5.28 Serial Interface

Symbol	Parameter		Standard		
Symbol	raidilletei	Min.	Max.	Unit	
tc(CK)	CLKi input cycle time	800	-	ns	
tW(CKH)	CLKi input "H" width	400	=	ns	
tW(CKL)	CLKi input "L" width	400	-	ns	
td(C-Q)	TXDi output delay time	=	200	ns	
th(C-Q)	TXDi hold time	0	-	ns	
tsu(D-C)	RXDi input setup time	150	=	ns	
th(C-D)	RXDi input hold time	90	=	ns	

i = 0 or 2

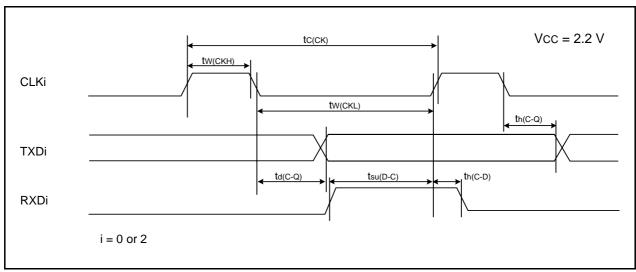


Figure 5.13 Serial Interface Timing Diagram when Vcc = 2.2 V

Table 5.29 External Interrupt INTi (i = 0 or 1) Input

Symbol	Parameter		Standard		
	Faranielei	Min.	Max.	Unit	
tW(INH)	ĪNTi input "H" width	1000(1)	-	ns	
tw(INL)	INTi input "L" width	1000(2)	1	ns	

- 1. When selecting the digital filter by the INTi input filter select bit, use an INTi input HIGH width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.
- 2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

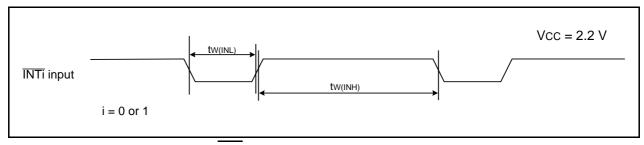


Figure 5.14 External Interrupt INTi Input Timing Diagram when Vcc = 2.2 V

5.2 **R8C/2J Group**

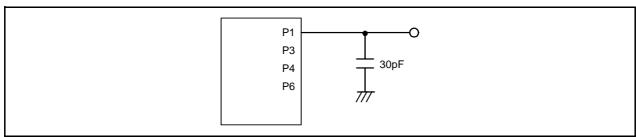
Table 5.30 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
Vcc	Supply voltage		-0.3 to 6.5	V
Vı	Input voltage		-0.3 to Vcc + 0.3	V
Vo	Output voltage		-0.3 to Vcc + 0.3	V
Pd	Power dissipation	Topr = 25°C	500	mW
Topr	Operating ambient temperature		-20 to 85 (N version) / -40 to 85 (D version)	°C
Tstg	Storage temperature		-65 to 150	°C

Recommended Operating Conditions Table 5.31

Symbol	Parameter		Conditions		Unit		
Symbol			Conditions	Min.	Тур.	Max.	Unit
Vcc	Supply voltage			2.2	=	5.5	V
Vss	Supply voltage			-	0	-	V
VIH	Input "H" voltage			0.8 Vcc	-	Vcc	V
VIL	Input "L" voltage			0	=	0.2 Vcc	V
IOH(sum)	Peak sum output "H" current	Sum of all pins IOH(peak)		_	_	-160	mA
IOH(sum)	Average sum output "H" current	Sum of all pins IOH(avg)		-	_	-80	mA
IOH(peak)	Peak output "H" current	All pins		-	-	-10	mA
IOH(avg)	Average output "H" current	All pins		-	_	- 5	mA
IOL(sum)	Peak sum output "L" currents	Sum of all pins IOL(peak)		-	=	160	mA
IOL(sum)	Average sum output "L" currents	Sum of all pins IOL(avg)		-	=	80	mA
IOL(peak)	Peak output "L" currents	All pins		-	-	10	mA
IOL(avg)	Average output "L" current	All pins		_	-	5	mA
=	System clock		HRA01 = 0 Low-speed on-chip oscillator selected	-	125	_	kHz
			HRA01 = 1 High-speed on-chip oscillator selected 2.7 V ≤ Vcc ≤ 5.5 V	-	-	8	MHz
			HRA01 = 1 High-speed on-chip oscillator selected 2.2 V ≤ Vcc ≤ 5.5 V	_	-	4	MHz

- 1. Vcc = 2.2 to 5.5 V at $T_{opr} = -20$ to $85^{\circ}C$ (N version) / -40 to $85^{\circ}C$ (D version), unless otherwise specified.
- 2. The average output current indicates the average value of current measured during 100 ms.



Ports P1, P3, P4, and P6 Timing Measurement Circuit Figure 5.15

Table 5.32 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions		Unit		
Symbol	Faiailletei	Conditions	Min.	Тур.	Max.	Offic
-	Program/erase endurance ⁽²⁾		100(3)	-	-	times
=	Byte program time		-	50	400	μS
_	Block erase time		-	0.4	9	S
_	Program, erase voltage		2.7	_	5.5	V
_	Read voltage		2.2	_	5.5	V
-	Program, erase temperature		0	=	60	°C
_	Data hold time ⁽⁷⁾	Ambient temperature = 55°C	20	_	_	year

- 1. Vcc = 2.7 to 5.5 V at Topr = 0 to 60°C, unless otherwise specified.
- 2. Definition of programming/erasure endurance
 - The programming and erasure endurance is defined on a per-block basis.

If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.

However, the same address must not be programmed more than once per erase operation (overwriting prohibited).

- 3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- 4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
- 5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- 6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- 7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.33 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition		Unit		
Syllibol	Falameter	Condition	Min.	Тур.	Max.	Offic
Vdet0	Voltage detection level		2.2	2.3	2.4	V
_	Voltage detection circuit self power consumption	VCA25 = 1, Vcc = 5.0 V	-	0.9	-	μΑ
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽²⁾		=	=	300	μS
Vccmin	MCU operating voltage minimum value		2.2	_	-	V

- 1. The measurement condition is Vcc = 2.2 to 5.5 V and Topr = -20 to $85^{\circ}C$ (N version) / -40 to $85^{\circ}C$ (D version).
- 2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

Table 5.34 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition		Unit		
Symbol	Farameter	Condition	Min.	Тур.	Max.	Offic
Vdet1	Voltage detection level ⁽⁴⁾		2.70	2.85	3.00	V
-	Voltage monitor 1 interrupt request generation time ⁽²⁾		_	40	_	μS
=	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V	=	0.6	=	μΑ
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾		=	=	100	μS

NOTES:

- 1. The measurement condition is Vcc = 2.2 to 5.5 V and Topr = -20 to 85°C (N version) / -40 to 85°C (D version).
- 2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes Vdet1.
- 3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
- 4. This parameter shows the voltage detection level when the power supply drops. The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.

Table 5.35 Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition		Unit		
Symbol	Farameter	Condition	Min.	Тур.	Max.	Offic
Vdet2	Voltage detection level		3.3	3.6	3.9	V
_	Voltage monitor 2 interrupt request generation time ⁽²⁾		_	40	_	μS
_	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0 V	-	0.6	_	μΑ
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾		=	=	100	μS

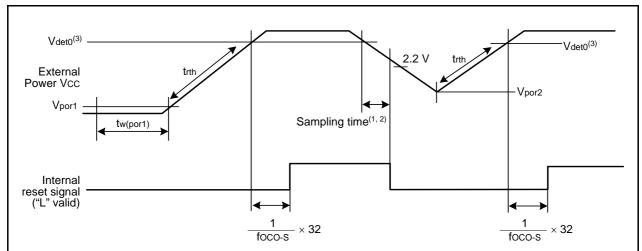
- 1. The measurement condition is Vcc = 2.2 to 5.5 V and Topr = -20 to 85°C (N version) / -40 to 85°C (D version).
- 2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes Vdet2.
- 3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.



Table 5.36 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristic	Table 5.36	Table 5.36 Power-on Reset Circuit, Voltage Monitor (0 Reset Electrical Characteristics
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Symbol	Parameter	Condition		Unit		
Symbol	Falametei	Condition	Min.	Тур.	Max.	Offic
Vpor1	Power-on reset valid voltage ⁽⁴⁾		_	_	0.1	V
Vpor2	Power-on reset or voltage monitor 0 reset valid voltage		0	-	Vdet0	V
trth	External power Vcc rise gradient(2)		20	_	_	mV/msec

- 1. The measurement condition is Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
- 2. This condition (external power Vcc rise gradient) does not apply if Vcc ≥ 1.0 V.
- 3. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVD0ON bit in the OFS register to 0, the VW0C0 and VW0C6 bits in the VW0C register to 1 respectively, and the VCA25 bit in the VCA2 register to 1.
- 4. tw(por1) indicates the duration the external power Vcc must be held below the effective voltage (Vpor1) to enable a power on reset. When turning on the power for the first time, maintain tw(por1) for 30 s or more if $-20^{\circ}C \le T_{opr} \le 85^{\circ}C$, maintain tw(por1) for 3,000 s or more if $-40^{\circ}C \le T_{opr} < -20^{\circ}C$.



- 1. When using the voltage monitor 0 digital filter, ensure that the voltage is within the MCU operation voltage range (2.2 V or above) during the sampling time.
- 2. The sampling clock can be selected. Refer to **6. Voltage Detection Circuit** of Hardware Manual for details.
- Vdet0 indicates the voltage detection level of the voltage detection 0 circuit. Refer to 6. Voltage Detection Circuit of Hardware Manual for details.

Figure 5.16 Reset Circuit Electrical Characteristics

Table 5.37 Comparator Electrical Characteristics

Symbol	Parameter	Condition			Unit		
Symbol	Farameter	Condition	Min.	Тур.	Max.	Offic	
Vref	Internal reference voltage	Vcc = 2.2 V to 5.5 V, Topr = 25°C	1.15	1.25	1.35	V	
		Vcc = 2.2 V to 5.5 V, Topr = -40 to 85°C	_	1.25	_	V	
Vcref	External input reference voltage	Vcc = 2.2 V to 4.0 V	0.5	=	Vcc - 1.1	V	
		Vcc = 4.0 V to 5.5 V	0.5	=	Vcc - 1.5	V	
Vcin	External comparison voltage input range		-0.3	_	Vcc + 0.3	V	
Vofs	Input offset voltage		-	20	120	mV	
Tcrsp	Response time		=	4	=	μS	

Table 5.38 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Cumbal	Parameter	Condition		Standard			
Symbol	Farameter	Condition	Min.	Тур.	Max.	Unit	
fOCO-F	High-speed on-chip oscillator frequency temperature • supply voltage dependence	VCC = 4.75 V to 5.25 V $T_{\text{Opr}} = 0 \text{ to } 60^{\circ}\text{C}^{(2)}$	7.76	8	8.24	MHz	
		Vcc = 2.7 V to 5.5 V $Topr = -20 \text{ to } 85^{\circ}C^{(2)}$	7.68	8	8.32	MHz	
		Vcc = 2.7 V to 5.5 V $Topr = -40 \text{ to } 85^{\circ}C^{(2)}$	7.44	8	8.32	MHz	
		Vcc = 2.2 V to 5.5 V $Topr = -20 \text{ to } 85^{\circ}C^{(3)}$	7.04	8	8.96	MHz	
		Vcc = 2.2 V to 5.5 V $Topr = -40 \text{ to } 85^{\circ}C^{(3)}$	6.8	8	9.2	MHz	

NOTES:

- 1. The measurement condition is Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
- 2. These standard values show when the HRA1 register is set to the value before shipment and the HRA2 register is set to 00h.
- 3. These standard values show when the correction value in the FRA6 register is written into the HRA1 register.

Table 5.39 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition		Unit		
Symbol	i didiffetei	Condition	Min.	Тур.	Max.	Offic
fOCO-S	Low-speed on-chip oscillator frequency		30	125	250	kHz
_	Oscillation stability time		_	10	100	μS
_	Self power consumption at oscillation	VCC = 5.0 V, Topr = 25°C	_	15	_	μΑ

NOTE:

Table 5.40 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition		Unit		
Symbol	Falametei	Condition	Min.	Тур.	Max.	Offic
td(P-R)	Time for internal power supply stabilization during power-on ⁽²⁾		1	=	2000	μS
td(R-S)	STOP exit time ⁽³⁾		ı	Ī	150	μS

- 1. The measurement condition is Vcc = 2.2 to 5.5 V and T_{opr} = 25°C.
- Waiting time until the internal power supply generation circuit stabilizes during power-on.
 Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.



^{1.} The measurement condition is Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

^{1.} Vcc = 2.2 to 5.5 V, Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.41 Electrical Characteristics (1) [Vcc = 5 V]

Cumbal	Dore	matar	Condition	S	tandard		Unit
Symbol	Parameter		Condition	Min.	Тур.	Max.	Unit
Vон	Output "H" voltage		Iон = −5 mA	Vcc - 2.0	_	Vcc	V
			IOH = -200 μA	Vcc - 0.5	_	Vcc	V
Vol	OL Output "L" voltage		IoL = 5 mA	-	_	2.0	V
			Ιοι = 200 μΑ	-	_	0.45	V
VT+-VT-	Hysteresis	INT0, INT1, KI0, KI1, KI2, KI3, RXD0, CLK0		0.1	0.5	-	V
		RESET		0.1	1.0	_	V
Іін	Input "H" current	•	VI = 5 V, Vcc = 5 V	_	_	5.0	μΑ
lıL	Input "L" current		VI = 0 V, Vcc = 5 V	_	_	-5.0	μΑ
RPULLUP	Pull-up resistance		VI = 0 V, Vcc = 5 V	30	50	167	kΩ
VRAM	RAM hold voltage		During stop mode	2.0	-	_	V

^{1.} Vcc = 4.2 to 5.5 V at Topr = -20 to $85^{\circ}C$ (N version) / -40 to $85^{\circ}C$ (D version), unless otherwise specified.

Electrical Characteristics (2) [Vcc = 5 V] **Table 5.42** (Topr = -20 to 85° C (N version) / -40 to 85° C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
Jymbol	i arameter		Condition	Min.	Тур.	Max.	Offic
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode,	High-speed on-chip oscillator mode	High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz No division	-	5	8	mA
	output pins are open, other pins are Vss		High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	=	2	_	mA
		Low-speed on-chip oscillator mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1		130	300	μА
		Wait mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	25	75	μА
			High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	23	60	μА
		Stop mode	Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1)	=	0.8	3	μА
			Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1)	=	1.2	-	μА
			Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0)	-	5	8	μА
			Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0)	-	5.5	_	μА

Timing Requirements

(Unless Otherwise Specified: Vcc = 5 V, Vss = 0 V at Topr = 25°C) [Vcc = 5 V]

Table 5.43 TRAIO Input

Symbol	Parameter Standard Min. Max.		Standard		
Symbol			Max.	Unit	
tc(TRAIO)	TRAIO input cycle time	100	-	ns	
twh(traio)	TRAIO input "H" width	40	-	ns	
twl(traio)	TRAIO input "L" width	40	-	ns	

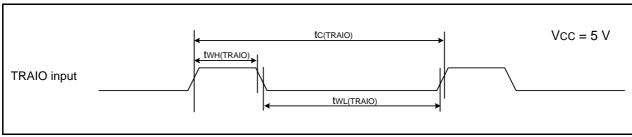


Figure 5.17 TRAIO Input Timing Diagram when Vcc = 5 V

	Table	5.44	Serial	Interface
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Symbol	Parameter		Standard		
Symbol	Farameter	Min.	Max.	Unit	
tc(CK)	CLK0 input cycle time	200	-	ns	
tW(CKH)	CLK0 input "H" width	100	-	ns	
tW(CKL)	CLK0 input "L" width	100	-	ns	
td(C-Q)	TXD0 output delay time	-	50	ns	
th(C-Q)	TXD0 hold time	0	=	ns	
tsu(D-C)	RXD0 input setup time	50	=	ns	
th(C-D)	RXD0 input hold time	90	-	ns	

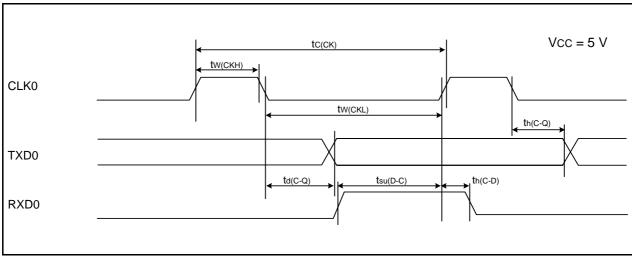
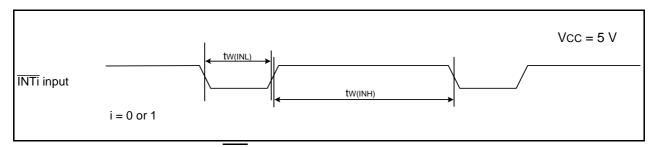


Figure 5.18 Serial Interface Timing Diagram when Vcc = 5 V

External Interrupt INTi (i = 0 or 1) Input **Table 5.45**

Symbol	Symbol Parameter		Standard		
,			Max.	Unit	
tW(INH)	ĪNTi input "H" width	250 ⁽¹⁾	-	ns	
tW(INL)	INTi input "L" width	250(2)	-	ns	

- 1. When selecting the digital filter by the $\overline{\text{INTi}}$ input filter select bit, use an $\overline{\text{INTi}}$ input HIGH width of either (1/digital filter clock frequency \times 3) or the minimum value of standard, whichever is greater.
- 2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency \times 3) or the minimum value of standard, whichever is greater.



External Interrupt INTi Input Timing Diagram when Vcc = 5 V Figure 5.19

Electrical Characteristics (3) [Vcc = 3 V] **Table 5.46**

Symbol	Parar	motor	Condition	5	Unit		
Symbol	Faiai	neter	Condition	Min.	Тур.	Max.	Offic
Voн	Output "H" voltage		Iон = −1 mA	Vcc - 0.5	=	Vcc	V
Vol	Output "L" voltage		IoL = 1 mA	=	=	0.5	V
VT+-VT-	Hysteresis	INT0, INT1, KI0, KI1, KI2, KI3, RXD0, CLK0		0.1	0.3	ı	V
		RESET		0.1	0.4	-	V
Iн	Input "H" current		VI = 3 V, Vcc = 3 V	=	=	4.0	μΑ
lı∟	Input "L" current		VI = 0 V, Vcc = 3 V	=	=	-4.0	μΑ
RPULLUP	Pull-up resistance		VI = 0 V, Vcc = 3 V	66	160	500	kΩ
VRAM	RAM hold voltage		During stop mode	1.8	=	=	V

^{1.} Vcc = 2.7 to 3.3 V at Topr = -20 to $85^{\circ}C$ (N version) / -40 to $85^{\circ}C$ (D version), unless otherwise specified.

Electrical Characteristics (4) [Vcc = 3 V] **Table 5.47** (Topr = -20 to 85° C (N version) / -40 to 85° C (D version), unless otherwise specified.)

0	D		O RC		Standar	d	Unit
Symbol	Parameter		Condition	Min.	Тур.	Max.	Unit
Icc	Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode,	High-speed on-chip oscillator mode	High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz No division	-	5	_	mA
	output pins are open, other pins are Vss		High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	_	2	_	mA
		Low-speed on-chip oscillator mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	=	130	300	μΑ
		Wait mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	25	70	μА
			High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	23	55	μА
		Stop mode	Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1)	_	0.7	3	μΑ
		Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1)	_	1.1	=	μА	
			Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0)	-	5	7	μΑ
			Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0)	_	5.5	_	μА

Timing requirements

(Unless Otherwise Specified: Vcc = 3 V, Vss = 0 V at Topr = 25°C) [Vcc = 3 V]

Table 5.48 TRAIO Input

Symbol	Parameter	Standard Min. Max.		Unit	
Symbol	raidilletei	Min. Max.	Offic		
tc(TRAIO)	TRAIO input cycle time	300	-	ns	
twh(traio)	TRAIO input "H" width	120	-	ns	
twl(traio)	TRAIO input "L" width	120	-	ns	

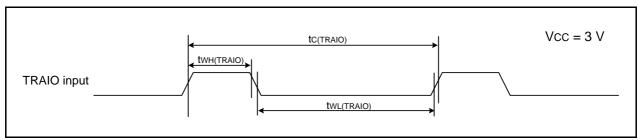
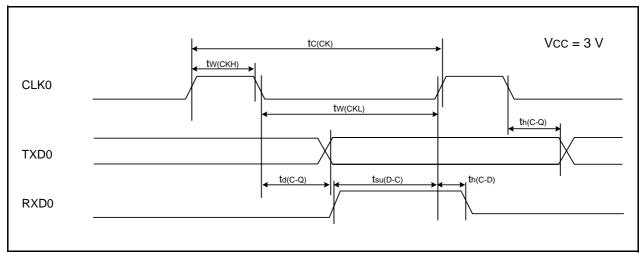


Figure 5.20 TRAIO Input Timing Diagram when Vcc = 3 V

Table 5.49 Seria	I Interface
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Symbol	Parameter		Standard		
Symbol	Falameter	Min.	Max.	Unit	
tc(CK)	CLK0 input cycle time	300	=	ns	
tW(CKH)	CLK0 input "H" width	150	-	ns	
tW(CKL)	CLK0 Input "L" width	150	-	ns	
td(C-Q)	TXD0 output delay time	-	80	ns	
th(C-Q)	TXD0 hold time	0	-	ns	
tsu(D-C)	RXD0 input setup time	70	=	ns	
th(C-D)	RXD0 input hold time	90	-	ns	

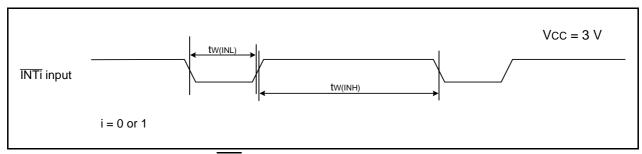


Serial Interface Timing Diagram when Vcc = 3 V Figure 5.21

External Interrupt INTi (i = 0 or 1) Input **Table 5.50**

Symbol	mbol Parameter	Standard		Unit	
,	raidilletei		Max.	Offic	
tW(INH)	INTi input "H" width	380(1)	-	ns	
tw(INL)	ĪNTi input "L" width	380(2)	I	ns	

- 1. When selecting the digital filter by the $\overline{\text{INTi}}$ input filter select bit, use an $\overline{\text{INTi}}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
- 2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.



External Interrupt INTi Input Timing Diagram when Vcc = 3 V Figure 5.22

Electrical Characteristics (5) [Vcc = 2.2 V] **Table 5.51**

Symbol	Doromotor	Condition	5		Unit		
Symbol	Parameter		Condition	Min.	Тур.	Max.	Offic
Vон	Output "H" voltage		Iон = −1 mA	Vcc - 0.5	=	Vcc	V
Vol	Output "L" voltage		IoL = 1 mA	-	-	0.5	V
VT+-VT-	Hysteresis			0.05	0.3	-	V
		RESET		0.05	0.15	-	V
lін	Input "H" current		VI = 2.2 V	-	-	4.0	μΑ
lı∟	Input "L" current		VI = 0 V	-	=	-4.0	μΑ
RPULLUP	Pull-up resistance		VI = 0 V	100	200	600	kΩ
RfXCIN	Feedback resistance	XCIN		-	35	-	MΩ
VRAM	RAM hold voltage	•	During stop mode	1.8	-	_	V

5. Electrical Characteristics

^{1.} VCC = 2.2 V at $T_{OPT} = -20$ to $85^{\circ}C$ (N version) / -40 to $85^{\circ}C$ (D version), unless otherwise specified.

Electrical Characteristics (6) [Vcc = 2.2 V] **Table 5.52** (Topr = -20 to 85° C (N version) / -40 to 85° C (D version), unless otherwise specified.)

Symbol	Parameter	Condition			Unit		
Cymbol	1 diamotoi		Condition	Min.	Тур.	Max.	Offic
Icc	Power supply current (Vcc = 2.2 to 2.7 V) Single-chip mode,	High-speed on-chip oscillator mode	High-speed on-chip oscillator on = 4 MHz Low-speed on-chip oscillator on = 125 kHz No division	=	3.5	=	mA
	output pins are open, other pins are Vss		High-speed on-chip oscillator on = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	=	1.5	=	mA
		Low-speed on-chip oscillator mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	=	100	230	μА
		Wait mode	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	22	60	μА
			High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	20	55	μА
		Stop mode	Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1)	=	0.7	3	μА
			Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit disabled (BGRCR0 = 1)	-	1.1	_	μА
			Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0)	-	5	7	μА
			Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 BGR trimming circuit enabled (BGRCR0 = 0)	-	5.5	_	μА

Timing requirements

(Unless Otherwise Specified: Vcc = 2.2 V, Vss = 0 V at Topr = 25°C) [Vcc = 2.2 V]

Table 5.53 TRAIO Input

Symbol	Parameter		Standard	
Symbol			Max.	Unit
tc(TRAIO)	TRAIO input cycle time	500	=	ns
twh(traio)	TRAIO input "H" width	200	=	ns
twl(traio)	TRAIO input "L" width	200	=	ns

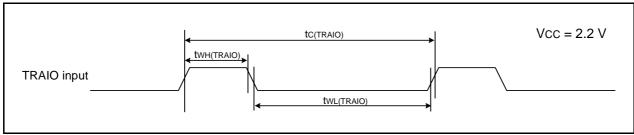


Figure 5.23 TRAIO Input Timing Diagram when Vcc = 2.2 V

Table 5.54 Serial Interface	Table	5.54	Serial	Interface
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Symbol	Parameter		Standard	
	Farameter	Min.	Max.	Unit
tc(CK)	CLK0 input cycle time	800	_	ns
tW(CKH)	CLK0 input "H" width	400	=	ns
tW(CKL)	CLK0 input "L" width	400	-	ns
td(C-Q)	TXD0 output delay time	-	200	ns
th(C-Q)	TXD0 hold time	0	-	ns
tsu(D-C)	RXD0 input setup time	150	=	ns
th(C-D)	RXD0 input hold time	90	-	ns

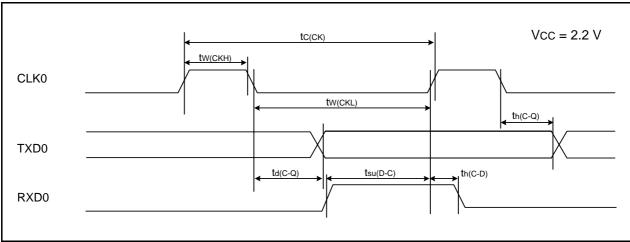
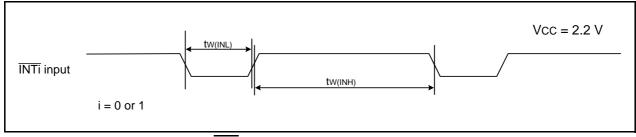


Figure 5.24 Serial Interface Timing Diagram when Vcc = 2.2 V

External Interrupt \overline{INTi} (i = 0 or 1) Input **Table 5.55**

Symbol	Parameter		Standard	
Symbol	i didilietei	Min.	Max.	Unit
tw(INH)	ĪNTi input "H" width	1000(1)	1	ns
tw(INL)	INTi input "L" width	1000 ⁽²⁾	=	ns

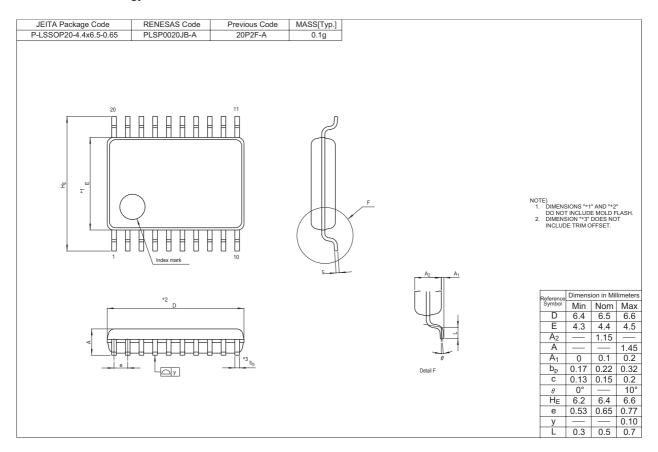
- 1. When selecting the digital filter by the INTi input filter select bit, use an INTi input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
- 2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.



External Interrupt INTi Input Timing Diagram when Vcc = 2.2 V Figure 5.25

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the "Packages" section of the Renesas Technology website.



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REVISION HISTORY

R8C/2H Group, R8C/2J Group Datasheet

D.	Data		Description	
Rev.	Date	Page	Summary	
0.01	Jun 18, 2007	_	First Edition issued	
0.10	Jul 20, 2007	20	Table 4.2: 0038h After reset; "0000X010b" → "1000X010b", "0100X011b" → "1100X011b"	
		31 to 64	5. Electrical Characteristics added	
0.20	Nov 12, 2007	2	Table 1.1 I/O Ports: "• Output-only: 1" added "• CMOS I/O ports: 16" → "• CMOS I/O ports: 15"	
		6	Figure 1.3 revised	
		8	Figure 1.5 revised	
		9	Table 1.5 Pin Number: 4, 6, 16 revised	
		12	Table 1.7 I/O port: "P4_3 to P4_5" $ ightarrow$ "P4_3, P4_5" Timer RE, Output port added	
		19	Table 4.1 0006h "01001000b" → "01011000b"	
		23	Table 4.5 0118h to 011Dh: After reset revised 011Fh "Timer RE Real-Time Clock Precision Adjust Regist added	
		31, 48	Table 5.2, Table 5.31 NOTE2 revised	
		54, 58	Table 5.42, Table 5.47 revised	
		62	Table 5.52 revised	
1.00	Mar 28, 2008	All pages	"Under development" deleted	
		2, 3	Table 1.1, Table 1.2 revised	
		4, 5	Table 1.3, Table 1.4; "(D): Under development" deleted	
		17, 18	Figure 3.1, Figure 3.2; "Expanded area" deleted	
		19	Table 4.1 "002Eh" "002Fh" revised	
		20	Table 4.2 "003Eh" "003Fh" revised	
		32	Table 5.3 revised Old Figure 5.2 deleted	
		35	Table 5.8, Table 5.11 revised Table 5.9 revised, NOTE3 added	
		37	Table 5.13 revised	
		41	Table 5.19 revised	
		45	Table 5.25 revised	
		49	Table 5.32 revised Old Figure 5.17 deleted	
		52	Table 5.37, Table 5.40 revised Table 5.38 revised, NOTE3 added	
		54	Table 5.42 revised	
		58	Table 5.47 revised	

REVISION HISTORY	R8C/2H Group, R8C/2J Group Datasheet
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Rev.	Date	Description			
ixev.	Date	Page	Summary		
1.00	Mar 28, 2008	62	Table 5.52 revised		

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